PROGNOSTICS AND DIAGNOSIS OF CATASTROPHIC FAULTS IN PHOTOVOLTAIC ARRAY AND RELIABILITY CENTERED MAINTENANCE (RCM) FOR POWER CONVERTERS USING SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY (SSTDR)

by

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ABSTRACT

Three major catastrophic failures in photovoltaic (PV) arrays are ground-faults, line-to-line faults, and arc faults. Although the number of such failures is few, recent fire events on April 5, 2009, in Bakersfield, California, and April 16, 2011, in Mount Holly, North Carolina suggest the need for improvements in present fault detection and mitigation techniques, as well as amendments to existing codes and standards to avoid such accidents. A fault prediction and detection technique for PV arrays based on spread spectrum time domain reflectometry (SSTDR) has been proposed and was successfully implemented. Unlike other conventional techniques, SSTDR does not depend on the amplitude of the fault-current. Therefore, SSTDR can be used in the absence of solar irradiation as well. However, wide variation in impedance throughout different materials and interconnections makes fault locating more challenging than prediction/detection of faults.

Another application of SSTDR in PV systems is the measurement of characteristic impedance of power components for condition monitoring purposes. Any characteristic variations in one component will simultaneously alter the operating conditions of other components in a closed-loop system, resulting in a shift in overall reliability profile. This interdependence makes the reliability of a converter a complex function of time and operating conditions. Details of this failure mode, mechanism, and effect analysis

(FMMEA) have been developed. By knowing the present state of health and the remaining useful life (RUL) of a power converter, it is possible to reduce the maintenance cost for expensive high-power converters by facilitating a reliability centered maintenance (RCM) scheme. This research is a step forward toward power converter reliability analysis since the cumulative effect of multiple degraded components has been considered here for the first time in order to estimate reliability of a power converter.

To my parents and my wife, without them I would have been nothing.

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CHAPTER 1

INTRODUCTION

Photovoltaic (PV) installation throughout the world has been increasing exponentially, and the total installed capacity of PV power globally was exceeded 136 GW. At least 37 GW has added in the year of 2013, which represents an increase of about 35% in total capacity [1]. This source of renewable energy will ensure a more sustainable environment in the future, and many larger PV plants (50 MW) are under construction in different countries. Grounding of PV plants is an important safety issue for both the maintenance workers and the power plant itself. Besides the current carrying conductors (CCCs), a PV array has several noncurrent carrying conductors (NCCs) such as module frames, mounting racks, metal enclosures, distribution panels, the chassis of end-use appliances and power converters, etc. All these NCCs are connected through a grounding cable called "equipment grounding conductor (EGC)," and the use of EGC is mandated by National Electrical Code 690.43 regardless of the nominal voltage of the PV system to avoid any potential electric shock to any living beings [2] - [6].

One of the CCCs can be connected to the EGC using ground fault detection and interruption fuse (GFDI) to detect the presence of any accidental circulating current path, and this is termed as system grounding. PV arrays can be divided into two types based on the type of grounding implemented: grounded and ungrounded PV systems [4] [5]. PV

systems with system grounding are known as grounded, and these are more common in the USA. A ground fault occurs if there is any accidental low impedance current path established between a CCC and the EGC/earth. Ground faults may result in a high current flow through the EGC that may exceed the rating of the EGC and initiate a fire [7] - [20].

A similar situation arises when two points on the PV array are connected together through a finite impedance by accident and this type of fault is known as a line-to-line fault. In addition to establishing unintentional solid contacts in PV array, there might be some arc created inside the PV array due to insulation damage. This is called an arc fault and arc faults are one of the major reasons that fires are initiated. Detail of the ground, line-to-line and arc faults, limitations of the existing fault detection and mitigation techniques, together with a review of other analytical and instrument-based techniques proposed in the literature are discussed in Chapter 2.

A PV ground fault detection and locating technique based on spread spectrum time domain reflectometry (SSTDR) is presented in Chapter 3. This chapter covers the basic concepts of SSTDR, the proposed algorithm, advantages and limitations of the proposed fault detection and locating algorithm, the impact of different parameters such as center frequency of the SSTDR, fault resistance, number of parallel strings, operation under different light intensity and double ground fault. Chapter 4 describes the applications of SSTDR in line-to-line and arc fault detection in PV array. These results are so far the most comprehensive investigation of fault detection in PV arrays using SSTDR.

In addition to fault detection in PV arrays, SSTDR can be used for condition monitoring of PV converters. It has been demonstrated in [21] [22] that SSTDR can be used for determining the level of degradation of power metal oxide semiconductor field

effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs) and electrolytic capacitors in live power converters. Moreover, several real-time methods to estimate the state of health of power converters have been proposed in [23] – [30]. Reference [23] proposed a real-time monitoring of capacitor's equivalent series resistance (ESR) based on the power dissipation across the capacitor and the capacitor current. Capacitor voltages and currents are continuously monitored to determine the power dissipation. Junction temperature of power devices is directly related to the operating states of the inverter. An online monitoring method was presented in [24] using the junction temperature of power devices in a voltage source inverter. Online fault diagnosis methods in power electronic drives were described in [25] by measuring the capacitor *ESR*, MOSFET R_{DS} and $V_{CE(sat)}$ of IGBT. *ESR* was calculated from the capacitor's voltage and current. R_{DS} was calculated from the corresponding ripple voltage and ripple current of the MOSFET.

Other online approaches for system health monitoring include data from the current sensors and relays of the protection system, monitoring power loss in different components of the power converter and frequency response [26]. Monitoring solder joint fatigue in power modules using the "case above ambient temperature" (CAAT) was proposed in [27]. The CAAT was measured using a two channel thermometer, and the module power loss was calculated using CAAT. Power loss is directly related to thermal resistance, which is an indicator of aging. An online fault diagnosis technique in DC-DC converters was proposed in [28] by calculating the *ESR* of the DC bus capacitor. *ESR* was calculated from the input current and the output voltage ripple of the converter. In reference [29], R_{DS} of power MOSFETs was calculated as the ratio of drain-source

voltage (V_{DS}) and drain current (I_D) during the on-state. Reference [30] proposed an online diagnosis method considering the variation in parasitic/internal resistors of components in a DC-DC converter. However, this diagnosis method is applicable to diagnose the entire system, not individual components.

A reliability centered maintenance (RCM) scheme that uses data of device degradation or characteristics parameter variation is proposed in Chapter 5. In addition to the proposed time-dependent reliability analysis, the complex interdependence of characteristic parameters, ambient condition, and operating point in closed loop converters is investigated in detail.

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CHAPTER 2

CATASTROPHIC FAULTS IN PV ARRAYS: TYPES, DETECTION AND MITIGATION TECHNIQUES

Recent fire events initiated by PV arrays suggest the necessity of understanding catastrophic failures in PV systems [1] - [3]. Shutting down the PV generation system under different fault conditions requires different mitigation techniques and, in most cases, requires prior knowledge of the type of the fault. This chapter discusses the major faults that may result in damage to a PV array (catastrophic faults), possible causes and detection schemes of these faults and protection techniques.

Among the numerous possible faults such as ground fault, line-to-line fault, hot spot formation, polarity mismatch, arc fault, open fault, bypass diode failure, dust/soil formation, etc. in a PV array, ground fault, line-to-line and arc fault are reported to be the major reasons behind catastrophic failures resulting in electrical fires. This chapter studies the electrical behavior of the PV system during those faults, possible causes for any failure, and the state-of-the-art detection and mitigation techniques for each type. In each fault case, there are specific technical challenges to detection and mitigation. Standards are reviewed and recommendations are provided to ensure more reliable PV arrays. This chapter does not cover faults in the rest of the components of a PV system (AC isolation failure, inverter failure, DC signal injection to the AC side of the inverter,

faults inside battery modules, etc.).

2.1 PV Ground Faults

Typically, a PV array has several exposed noncurrent carrying (NCC) metals/conducting parts (module frames, mounting racks, metal enclosures, distribution panels, the chassis of end-use appliances and power converters, etc.) [4]. These conductors do not carry any current during normal operation. However, there is a potential risk of electric shock hazard from these exposed NCC conductors when an electrical connection is established between the current carrying conductors (CCCs) and NCC conductors due to a fault (e.g., corrosion, loss or melting of insulation, wire cut-off, wrong wiring, etc.). Therefore, all these NCC conductors are connected together to the ground or earth through a current carrying conductor termed a "equipment grounding conductor" (EGC). This is illustrated in Figure 2.1 as green lines.

Equipment grounding is required by National Electrical Code Article 690.43 to protect people and other living animals from being electrocuted [5]. Similarly, any accidental connection between a CCC and EGC/earth can cause significant current flow to the ground circuit, known as a "ground fault". Therefore, proper grounding is required for any electrical system to provide adequate personnel and system safety in the case of one or multiple ground faults. The voltage and current limit for a living being to be electrocuted is proposed as 75 V and 100 mA [6], and to avoiding a potential electric shock, equation (2.1) should be met:

$$R_A I \leq U_L \qquad for \qquad I < I_d \tag{2.1}$$

where R_A is the resistance of the living being exposed to potential electrical shock with a current I from the point of contact at higher potential to the ground. The maximum and average estimated resistances for the human body are approximately 1000 Ω and 650 Ω [4] [6]. I_d and U_L are 100 mA and 75 V, respectively.

2.1.1. Grounded and Ungrounded PV Systems

Grounding practices in PV systems vary depending on the operating voltage, size of the plant, type of installation (ground-mount, roof-top, building mounted etc.), and geographic location. Any PV system with system voltage higher than 50 V requires ground fault protection according to US National Electrical Code (NEC) Art. 690.5. Typically, U.S. PV arrays have an electric connection between ground and one of the CCCs through a ground-fault detection and interruption (GFDI) fuse, known as "system grounding." However, there are alternative ground fault protection schemes, which are more common outside the U.S. including residual current monitoring devices (RCD) and DC insulation resistance (Riso) measurements. These ground fault protection systems often are used on ungrounded ("floating") PV systems which do not have a connection between a CCC and ground. Differences in grounded and ungrounded systems are illustrated in Figure 2.2.

In order to analyze different ground faults, a complete electrical model of a PV array is necessary. Unfortunately, electrical parameters vary between PV systems due to variations in the construction of PV modules (e.g., dimension, material, and ground connection), site (grounded, roof-top, building mounted, etc.), physical layout, etc. Therefore, a generic RC model for a PV array from CCCs to ground is proposed in [7], as

shown in Figure 2.3. R_s, R_p and C_{leak} are series insulation resistance, parallel insulation resistance and leakage capacitance of each module. In addition, long connecting wires may be required in large PV arrays to connect PV panels to the central inverter. These connecting wires add additional impedances [8].

An unintended effect of GFDI protection schemes is that it provides an electrical path for the leakage current to return to the PV conduction path through the ground fault detection fuse. The leakage current is highly dependent on relative humidity, temperature, array voltage, and size of the array [6] - [8]. Moreover, impedance from a CCC to ground in an ungrounded system varies with different meteorological variables (temperature, humidity, etc.), and the design of fault detection devices for both ungrounded and grounded systems requires a safe estimation of detection parameters to avoid system shutdown under normal operating conditions.

2.1.2. Reasons for Ground Fault

A ground fault establishes an unintentional low impedance path between one of the CCCs and the ground/earth, and a large fire in a PV array often destroys the origin of the fault. Several potential reasons for ground faults have been discussed in [4] [9] - [11], and summarized here:

1) Cable insulation damage during the installation, due to aging, impact damage, water leakage, and corrosion

2) Ground fault within the PV modules (e.g., degraded sealant, water ingress)

3) Insulation damage of cables due to chewing done by rodents

4) Accidental short circuit inside the PV combiner box, often at the time of

maintenance

If a ground fault remains undetected, it may generate a DC arc within the fault and cause a fire hazard.

2.1.3. Ground Fault Detection Techniques

Depending on whether a PV system is ungrounded or grounded, and considering the geographic location, several ground fault detection devices are commercially available to be used with PV installations. They are listed in Table 2.1.

2.1.3.1 GFDI Fuse

System grounding provides an intentional circulating path for the ground current during a fault condition and the fuse melts if the current is higher than a safe threshold current limit. If the fuse is cleared (opened), the inverter needs to be turned OFF immediately to isolate the PV array from the rest of the power system, and fault inspection becomes possible. In most grounded PV systems, a fuse with 1-5 A rating is installed inside the PV inverter. UL 1741 sets the upper limits for the ground fault fuse ratings as depicted in Table 2.2. A sensor inside the inverter checks the fuse continuity and shuts down the system in the presence of any ground fault.

The fuse rating needs to be high enough to avoid nuisance tripping due to leakage current, and it should be low enough to trip during actual ground faults. An estimation of leakage current for modules operating at 600V that meet the standard UL 170 [12], IEC 61646 [13] or IEC 61215 [14] has been provided in [8]. It has been estimated that the maximum leakage current for 1.2 m2 crystalline Si modules is 11 μA/kW for a 7-module

string, which can result in 56 mA of leakage current from a 500kW array. Compounding this challenge, the sensitivity of the GFDI fuse is influenced by the leakage current of the PV array, and several papers have investigated the effect of different parameters such as ambient temperature, relative humidity, salt mist, electromagnetic interference (EMI), and resistance of the grounding conductor on the leakage current [6]-[8] [15]-[19].

An ungrounded PV array poses shock hazard in the form of capacitive discharge, and such shock hazards can be avoided by using resistive grounding. Distributed capacitances in a grounded PV array do not pose such danger due to the system grounding.

2.1.3.2 Monitoring Residual Current

Residual current monitoring devices (RCDs) can sense the difference between the current entering and leaving PV system through the positive and negative CCCs. A simple schematic diagram of an RCD is shown in Figure 2.4. RCDs, in general, sense the presence of an alternate current path through the presence of any residual magnetic field and can open the current carrying conductors using switching relays. RCDs can be installed for each string or for the entire array [1]. However, the sensitivity of an RCD should be set by considering the leakage current of the PV modules. In [6], it is recommended that the set point of differential current (ΔI) at which an RCD signals a ground fault should be chosen according to equation (2.2).

$$\Delta I \geq C_{sl} \times I_{leak,max} \tag{2.2}$$

In Figure 2.4, $I_{leak,max}$ is the maximum leakage current that may result from the PV

modules covered by the RCD channel, and the multiplier C_{sl} (>1) is used to avoid the nuisance tripping that may result from external noise, measurement error, etc. RCDs can be installed in both grounded and ungrounded PV systems to protect them against ground and other line-to-line faults.

2.1.3.3 Insulation Monitoring Device

An insulation monitoring device (IMD) measures the resistance between both CCCs and ground and can alarm the system if the resistance falls below a preset value ($R_{fault\_threshold}$) [6] [8]. IMDs can be implemented for detecting ground fault in a grounded system by disconnecting the GFDI fuse at the time of taking measurements, generally at the beginning of the day before the inverter is connected to the array.

Since the insulation resistance is influenced by the ambient conditions, a nuisance trip threshold $R_{fault\_threshold}$ is recommended in [6] and shown in (2.3).

$$R_{fault\_threshold} \leq C_{sr} \times R_{iso\_min} \tag{2.3}$$

R_{iso_min} is the minimum insulation resistance that may result in the PV array under any climatic condition, C_{sr} (<1) is another safety factor.

2.1.4 Blind Spot and Double Ground Fault

A fuse has a threshold current for detecting a ground fault, and the fault may remain undetected if the resultant ground fault current is less than this threshold limit. If a ground fault occurs on a grounded current carrying conductor or at a location in the array where

the potential to ground is small, the fault current is very small. In those cases, a fault can occur that does not trip the GFDI. This gap in traditional ground fault detection fuses is known as the "blind spot" [1] [2] [8] [18] [19]. Any ground fault that results in a blind spot poses a significant risk, because the ground fault in the array remains undetected for an indefinite time, unless otherwise deactivated. A blind spot is extremely important for the safety of the PV array, since any subsequent ground fault will result in a fault current that may bypass the GFDI fuse. The entire array current may flow through the grounding wire, resulting in the possibility of severe damage to the array.

Two well-investigated ground fault events, on April 5, 2009, in Bakersfield, California, and April 16, 2011, in Mount Holly, North Carolina resulted from undetected ground faults within a blind spot range, followed by another ground fault that allowed a large amount of current to flow through the grounding wire [1] [21]. The example of Mount Holly fire, as depicted here in Figure 2.5, is an illustration of double ground fault. A similar incident occurred in the Bakersfield fire. The first ground fault produced a current through the GFDI fuse which had fault current amplitude below the threshold limit and the fault remained undetected for an undetermined period of time. The next ground fault resulted in a flow of an estimated 952 A through the EGC, which ignited a fire before it was cleared by the over current protection fuse.

2.1.5. Limitations of Ground Fault Detection Techniques

In general, ground fault detection devices are based on passive fuses, isolation impedance measurements, or differential current measurement methods, and these

devices suffer from several limitations as discussed here [2] [22]:

1) Ground-fault may result within the blind spot range due to low insolation e.g., during the night, on a cloudy day, at the time of partial shading, etc. and remain undetected.

2) A double ground fault may be established during the night and may result in high fault current and arcing inside the array during daytime.

3) Residual current monitoring devices may be affected by external electrical noise and may result in nuisance tripping of the system [23].

4) If not designed properly, leakage current can deceive the GFDI and IMD devices, especially during the presence of high relative humidity in large PV systems [16].

5) The leakage current may flow in the opposite direction of the ground fault current, reducing the magnitude of the current through the GFDI fuse [1] [18]. This may lead to an undetected ground fault.

2.1.6. I-V Curve Analysis and Effect of MPPT on Ground Fault

Electrical characteristics of a PV array are a nonlinear function of several parameters, i.e., insolation, temperature, humidity, module mismatch, etc., and a change in any of these several factors may result in a change to the array I-V characteristics similar to that caused by a ground fault. In some cases, the maximum power point tracker (MPPT) responds to the ground fault in such a way that it may diminish the onset fault current or the back fed current, making fault detection more challenging.

Effects of the ground fault on the I-V curve of the PV array has been discussed

extensively in [10] [20] [24]-[26], and a summary is presented here.

1) The fault current amplitude through the GFDI fuse depends on the location of the ground fault in the PV string. The higher the voltage at the fault location, the higher the ground fault current that results.

2) If the fault is uninterrupted in a grounded array, the maximum power point tracker (MPPT) will set the new operating power point lower than the level before fault (if the fault is not on the grounded CCC) with a small reduction in operating current (Figure 2.6). Therefore, a permanent reduction in output power can be a sign of a ground fault [10].

2.2. Line-to-Line Faults

An unintentional low impedance current path between two points in a PV array is referred to as a line-to-line fault. This fault may occur within the same string or between two strings, as depicted in Figure 2.7 [10] [24] - [26]. A line-to-line fault may reverse the current flow through the faulty strings. The maximum current that can flow through the faulty string of a PV array with n number of strings connected in parallel is (n-1) × (short circuit current of each string). However, the amplitude of this fault current depends on the potential difference between the points establishing the fault before the fault occurs. The higher the potential difference, the higher the fault current that results. Line-to-line faults are, in general, cleared by over current protection devices (OCPDs), i.e., string fuses, if the fault current is higher than the rated current of the OCPD which is mandated to be at least 56% greater than the string short circuit current by the NEC.

The effects of MPPT, irradiance, and series blocking diodes on PV arrays with

different line-to-line faults have been explained in [26]. In most cases, a line-to-line fault under full illumination results in an open circuit due to melting of the OCPD and the fault can be located through inspection of the affected strings. However, if the line-to-line fault occurs under low illumination (e.g., during the night, night-to-day transition, during morning, day-to-night transition), the current through the affected string/strings is not large enough to melt the OCPD, and the fault may remain undetected until sufficient illumination is present to clear the OCPD. Moreover, the MPPT operation of the inverter may move the operating point to a new position on the I-V curve such that the fault current amplitude decreases over time and remains undetected.

This is illustrated in Figure 2.8 [10]. In this figure, if a line-to-line fault occurs while the PV array is operating at point A and the resultant fault current is less than the melting current of the OCPF (I_{melt_OCPF}), the fault remains undetected, and the MPPT moves the operating point to C where the array seems to be operating at normal condition with lower output power. These types of line-to-line faults will remain undetected for an indefinite time, and thereby any degradation in power output from a PV generator for a long duration requires thorough investigation of the PV array for a line-to-line fault. The use of blocking diodes makes the fault detection more challenging since it prevents the current flow through the affected modules in the reverse direction [10], and any short failure of diodes in absence of an OCPD can be dangerous and may cause a fire due to a high fault current through the PV modules.

2.3. PV Arc Faults

A PV array consists of numerous connections/junctions throughout the array, as depicted in Figure 2.9. A current path may be established through the air via arcing due to a discontinuity in the current carrying conductors or insulation breakdown in adjacent current carrying conductors. A series arc fault occurs when there is an arc fault due to a discontinuity in any of the CCCs resulting from solder disjoint, cell damage, corrosion of connectors, rodent damage, abrasion from different sources, etc. Parallel arc faults in adjacent CCCs occur mostly due to insulation breakdown. Any form of arc fault is harmful and potentially dangerous to the PV array since it may initiate a fire, especially in the presence of any flammable substance present in close proximity of the PV arc [27]-[32]. Unlike AC systems, the current through the DC arc does not possess a periodic zero crossing and, therefore, it is much more likely that an arc in a PV system will result in a sustained arc compared to an AC generation system [33] [35]. The National Electrical Code® (NEC)-2011 requires a series arc-fault protection device, known as an arc-fault circuit interrupter (AFCI), in any rooftop PV array with DC operating voltage equal to or higher than 80 V [33] [34]. The 2014 NEC expands this requirement to all PV systems above 80 V [36].

2.3.1. Physics of Arc

The dielectric constant of an insulating material defines the maximum electric field that the material can withstand before breakdown occurs. A sustained arc results if the energy produced inside the arc is higher than the energy lost due to thermal radiation, light, sound, etc. The dielectric constant of air is approximately 3 V/μm, and it depends

on surrounding pressure, humidity, presence of impurities, etc. [28] [37]. In addition, the initiation/sustainability of an arc also depends on the size/shape of the electrodes, air gap between the electrodes, and presence of chemical products from the arc (melted metals from electrodes, melted/vaporized polymers from glass, wire insulation, etc). An arc is initiated across an air gap when high electric fields ionize air molecules and accelerate the ion towards the opposite electrode. This results in high-velocity particle collisions, which generate additional charged particles. This runaway ion generation converts the normally insulating air medium into a conductive medium.

The voltage-current relationship of an arc is highly nonlinear. The transient behavior of a DC parallel arc in a PV array connected to an inverter undergoing MPPT suggests a decrease in voltage and increase of current during the onset of an electric arc, as depicted in Figure 2.10. An arc can be modeled as simple resistor at steady-state with the resistance being a function of the arc current, voltage, and length [38]. Different V-I characteristics and model equations for a DC arc have been summarized in [39]. Yao *et al.* has proposed a modified Paukert form for describing the V-I relationship of arc in PV system, as shown in equation (2.4) [38]:

$$V_{arc} = \frac{a + bL}{I_{arc}^{c+dL}} \tag{2.4}$$

Here, a,b,c,d are constants while V_{arc}, I_{arc}, L are arc voltage, current, and length.

Two other significant aspects of PV arc faults are arc temperature and burn-through time of CCC insulation. Burn-through time depends on the temperature, power density, and type of the material considered. Arc temperatures of 6000° K and above can vaporize

most metals and adjacent materials, and radiative heating can ignite flammable materials near the arc fault. Therefore, use of fire-retardant materials may help extinguish the arc and abate subsequent fire hazards in a PV array [28].

2.3.2. Types and Reasons for Arc Faults

As shown in Figure 2.9, there are numerous interconnection/junction that exist in a PV array (cell to cell, cell to bus bar, module to module, bypass diode parallel to solar cells, string to string, panel to panel, etc.). In addition, there are several interconnections that exist for mounting safety devices (OCPDs, DC disconnect switches, etc.). These connections are created through soldering, MC4 connectors, or screw terminals inside junction boxes. Any of these connections are potential places for arc fault initiation. Any insulation damage in the CCCs poses a risk of arc fault as well.

Arc faults are categorized as series and parallel categories depending on whether the current through the arc creates a new conduction branch in the existing PV array.

2.3.2.1. Series Arc Faults

Series arc faults are caused by any discontinuity in the existing current path of a PV array and may result from corrosion, thermal cycling, damage from rodents, extreme weather, etc. [28]. Degradation in solder joints, wiring or connections inside the junction box, loosening of screws, or incorrect crimping may increase the connection resistance. Increased operating temperature may result in thermal stress leading to accelerated aging or complete disconnection [33] [40].

It has been shown in [37] that a 5 μm separation of interconnect ribbon to busbar

connection inside a solar module can experience dielectric breakdown from the module's voltage. Only 0.4 mm^2 of arc region may produce enough heat within 2 seconds to shatter the glass and burn off the metal coating and other materials. As PV modules are considered to be very reliable and scheduled maintenance is not performed frequently, small signatures (discoloration of busbar, ribbons, edge of solar cells, small cracked region of glass, etc.) of arc faults may go unnoticed for some time [37] [41]. A well-reported product recall occurred for BP solar modules due to arc hazards from faulty cold soldering [40].

2.3.2.2. Parallel Arc Fault

Parallel arc faults result in a current branch that does not exist under normal operation of a PV array, as depicted in Figure 2.11. Examples of such parallel arc faults are [33]:

a) Intrastring parallel arc-fault: Parallel arc fault between two points on the CCCs of the same string.

b) Cross-string parallel arc-fault: Parallel arc fault between two points on the CCCs of the two different strings.

c) Parallel arc fault to ground: Parallel arc fault between one point on a CCC and another point at ground potential.

Parallel arc faults can result from insulation damage due to mechanical damage, aging, or wildlife [41], as well as previous series arc fault events [40].

2.3.2.3. Differentiating Between Series and Parallel Arc Faults

Series arc faults can be de-energized by opening the inverter terminals to stop the current flow, but this method will not be able to extinguish parallel arc faults. In parallel arc cases, opening the inverter terminals increases the electric field across the arc column, since the operating voltage is moved toward a higher voltage (open circuit voltage of the array), increasing the amount of current circulating through the parallel current. Therefore, it is extremely important to differentiate between the series and parallel arc fault for safe operation of a PV array [27] [33] [41] [42]. Different methods have been proposed in [27] [43] to distinguish series and parallel arc faults in a PV array:

a) Parallel arc faults often result in a drop of array current and voltage, which does not occur in the case of series arc fault or usual irradiance changes. Therefore, a combination of arcing noise and change in current/voltage magnitude can be used as a method for differentiating between series and parallel arc faults.

b) Forcing the operating point of a PV array close to the open circuit voltage will allow extinguishing the series arc fault, and any arc-induced noise at that point ensures the presence of a parallel arc fault.

c) Installing arc-fault detectors (AFDs) at the string level and disconnecting the inverter without disconnecting the parallel strings can be used to select the presence of a parallel arc fault by observation of arc-induced noise.

d) Opening the conduction path, thereby extinguishing all series arc-faults and rechecking for arc-fault noise to determine if the fault is a parallel fault [43].

Moreover, parallel arc faults can be detected similar to other line-to-line faults by comparing the differential string input/return current. The presence of differential current

along with arc-induced noise suggests the existence of a parallel arc fault [45].

2.3.2.4. Effect on PV Operation

The voltage drop across an arc can be subdivided into two components: voltage drop across the positive and negative electrodes and across the ionized/plasma medium. The sum of voltage drops across copper electrodes is 20 V to 30 V, and the voltage drop across the plasma depends on the gap length between the electrodes. Therefore, if the voltage across two copper plates is higher than 30V, there is a chance of arc initiation [40]. However, it is reported in [42] that the voltage and current across an arc in a PV string connected to an inverter changes rapidly due to the transient nature of the arc and the maximum power point tracking (MPPT) operation of the inverter.

One general trend to study the impact of steady-arc on PV is to model the arc as a resistance that may vary from near zero to 45 Ω [34] [38] [42]. Modeling series arc fault as a series resistance suggests a decrease in the fill factor and efficiency of the PV array. Moreover, it introduces mismatch losses among the parallel connected strings in an array. In general, the voltage drop across the arc increases with the increase in arc length, and thereby results in a substantial drop in efficiency [38].

Although the formation of parallel arc faults is unlikely compared to series arc faults, it poses significant threat to the safety of a PV array [40]. Parallel arc faults affect the PV array similarly to other line-to-line faults discussed in the previous section, although the presence of the arc fault adds additional high frequency components to the voltage and current signals.

2.3.2.5. Detection and Mitigation Methods

Arc in both DC and AC systems manifest similar frequency characteristics except the line frequency components in an AC arc [41] [44]. Solar arrays show more dynamic variation than conventional battery backed DC systems installed in automotive systems, due to the variation in solar irradiance, temperature, etc. Although arcs in a PV system are characterized by signatures in both the time and frequency domains, most arc detection techniques already developed for PV systems use frequency spectrum analysis of the voltage or current waveforms, and other complex analytical methods (e.g., wavelet transformation, neural network analysis, etc.) to avoid any nuisance tripping and unwanted down time [29] [38].

The frequency content of an arc is similar to pink noise and shows a 1/f relation (i.e., the amplitude of frequency content decreases with frequency) [34] [41]. The fast fourier transform (FFT) of the current signal of a PV string connected to an inverter with and without arc fault is shown in Figure 2.12. The switching frequency of the converter was 10 kHz. It is expected that analyzing the lower frequency content can be used for detecting arcs. However, frequencies below 1000 Hz are not recommended to avoid nuisance tripping due to signal variations from solar irradiance, partial shadows, movement of humans or vehicles, 50-120 Hz noise from the inverter, etc. [29].

Arcing frequency content above 500 kHz interacts with external RF noise sources and frequencies above 100 kHz contain less arcing energy, so these frequencies are generally not used in AFCIs. Unfortunately, most inverters, charge controllers and DC/DC converters have switching frequencies within the range of 10 kHz to 50 kHz [41] [45], and generate other harmonics and subharmonics. Therefore, it is not possible to develop a

detection technique based on one frequency component. The range of 1-100 kHz is considered to be the most suitable range for designing arc fault detectors and arc fault circuit interrupters (AFCIs) for PV plants irrespective of arc fault type (series or parallel) [29] [32] [34] [35] [45].

Another important aspect of designing an arc-safe PV system is the location and number of arc fault detectors (AFD) and circuit interrupters (AFCI). In general, AFD and AFCI are installed in the inverter in small PV systems and in the combiner box in large systems. However, this method suffers from the following limitations [34] [46] [52]:

1) The arc signal needs to propagate from the location of the arc to the location of the detector. The signal can be attenuated throughout the propagation path at numerous interconnections of the array. Moreover, some high frequency signals may be filtered out by the components of solar cells and other parasitics.

2) Long wiring runs present in a PV plant may work as an RF receiver and may capture signals from other sources to create false tripping of the AFCI.

3) Irrespective of the location of the arc in a string or adjacent strings, AFCIs installed inside the inverter/combiner box disconnects the entire array.

A possible switching scheme for extinguishing parallel arc fault is shown in Figure 2.13 [40]. Here, switches S1 and S2 are used for disconnecting the PV array from the inverter whenever the AFD detects a fault. This will extinguish all the series arc faults, while sustaining any parallel arc faults. If the arc noise still exists, the parallel arc fault can be extinguished by short-circuiting the positive and negative terminals using the switch S3. However, this might not be possible in large PV systems where multiple arrays are connected in parallel.

In order to optimize the accuracy, cost and annual production from a PV generation unit, the possibility of installing AFDs at three different locations: module-level, string-level, array-level are discussed in [31], as illustrated in Figure 2.14. In [47], it is reported that AFDs are able to detect faults irrespective of whether they are located at the string, between the combiner and recombiner, or at the central inverter of a 5 kW system. However, in larger PV systems, installing AFDs in recombiners might be affected by a serious attenuation issue. Therefore, AFDs can be installed in the combiner boxes and AFCI can be installed at the inverter or recombiner.

String level utilization of AFDs can disconnect the affected string or strings while the rest of the strings may operate uninterrupted. However, this is a more expensive option compared to array level protection and may suffer from "crosstalk" noise, where arc noise from one string propagates to unaffected strings (Figure 2.15) [31]. An AFCI needs to be fast enough to de-energize the arc before any fire ignites and be robust enough to avoid nuisance tripping. In [31], it is reported that, in a two-string array, a false arc signature was detected in a nonarced string due to noise from a parallel faulty string within an average delay of 19.5 ms. However, it is expected that the performance of string level detection would be better with a large number of parallel strings since the arc energy will be lower in each healthy parallel string. Also, faster detection schemes might be effective for avoiding crosstalk noise [31].

Module level AFD/AFCIs seem to be more reliable (an expensive option) among all these mounting options and more appropriate for PV modules with DC/DC converters or micro-inverters [31] [40]. Moreover, it is possible to adapt hybrid structures where the AFDs are located at module/string/combiner and AFCIs are located at string/combiner/re-

combiner/central converter. A detailed comparison among all these structures in terms of cost and reliability require further investigation.

Parallel arcs to ground are most common, and it is expected that such faults might involve GFDI or OCPDs to operate. Moreover, the improved ground fault detection capabilities required by 2014 NEC will address the vast majority of parallel arc fault risks in large systems.

Understanding the propagation of arc noise through a PV array requires high frequency models for PV modules as described in [30] [48] [49], and a simplified equivalent AC circuit model for a PV module is shown in Figure 2.16.

We define,

I_{mod} = photo-generated current of the PV module.

R_s = series resistance

$R_p = R_{sh} \parallel R_d$

R_{sh} = shunt resistance

$R_d(V)$ = dynamic resistance of diode

$C_p = C_D \parallel C_T$

$C_D\ (V,\omega)$ = diffusion capacitance

$C_T(V)$ = transition capacitance

V_{ac} = dynamic voltage

ω = signal frequency

The attenuation characteristics of a PV panel vary with solar irradiance and cell voltage. Therefore, the arc noise will be affected by a wide variation in solar irradiance/cell voltage during PV operation [29] [30] [48] [49]. Some arcing dangers are

inherent to regular operation of a PV plant, such as inverter operation during the morning or in the evening, low voltage shutdown resulting from clouds or partial shading, or contact arcing at junction boxes during maintenance operations. An intelligent AFCI should be able to avoid nuisance tripping in the above mentioned cases.

Other arc fault detection and mitigation techniques based on more complex signal processing techniques are discussed in section 2.4.

2.4. Other Analytical Solutions for Detection of PV Faults

This section summarizes methods proposed in the literature for detection, mitigation, and differentiation of different fault types besides the general techniques described in section 2.1-2.3. Most methods use different on-site measurement data such as recorded voltage/current, maximum power point, temperature, irradiance, power loss, fill factor, etc. to detect and classify faults using different numerical and data processing techniques [53]- [63].

A multilayer artificial neural network (ANN) based algorithm has been proposed in [53], where irradiance, cell temperature, voltage and current at maximum power point are used as inputs to estimate the voltage across each module of a two string array, which is used for detection and location of a short line-to-line fault. However, performance of the algorithm with other types of faults (ground or arc faults) has not been reported. Based on the PV array voltage, current, operating temperature and irradiance, a decision tree-based supervised technique is proposed in [54] to detect and classify four fault conditions: line-to-line fault with short circuit, line-to-line fault with 20 Ω resistance, open circuit fault

and partially shaded condition. Similar to other supervised learning algorithms, this method requires suitable training data for each faulty condition along with data from the PV array at normal operating conditions. Accuracy of this algorithm depends on the size of the tree and number of leaves used in the algorithm. In order to overcome the drawback of large training data, a graph-based semisupervised learning technique has been used in [55], with similar accuracy and less of a training data set due the self-training capability of the algorithm.

Less computation intensive fault detection techniques based on the variation in string currents of a PV array only are proposed in [56] [57]. Three different outlier detection rules, 3-sigma, Hampel identifier, and Boxplot are described in [56]. These methods do not require previous training data to detect line-to-line faults (short circuit and 20 Ω resistance), open faults, series resistance faults, and partial shading. However, it was concluded that the Boxplot rule performs best in identifying faults while the 3-sigma method failed to detect any faults. The ratio of string current to the maximum string current operating in parallel is used for identifying faulty string/strings in [57], although this method cannot differentiate the type of fault.

Some inverters are designed to shut down automatically whenever the primary current becomes negative at the onset of a parallel line-to-line or arc fault [64]. In large systems, reverse current detection at the feeder inputs to a recombiner box or inverter is a good method of detecting parallel line-to-line or arc faults because of the contribution to the fault from parallel circuits. Authors in [45] proposed connecting all positive and negative CCCs to ground to extinguish parallel arc faults. Fault detection analysis based on comparing maximum current, voltage, and power from simulation and field data over

a long duration to avoid the effects of partial shading has been described in [58]. A minimum covariance determinant (MCD) estimator based method considering PV fault detection as a clustering problem was described in [59] [60]. This method provides the probability of detection along with the probability of false alarms to determine the presence of a fault. Based on simulation results, it was claimed that the algorithm could detect PV series arc faults and ground faults in a single module. In [61], differences in power losses between simulated and real-world data are used for detecting PV faults. However, no conclusive study has been conducted to determine the comparative performance indices of the proposed techniques describe above. In [62], fuzzy rule-based power estimation from temperature and irradiance data is used for detecting faults in a PV by comparing the real power measurement data and the estimated power from the algorithm.

In addition to the arc detection techniques based on frequency content of current and voltage signals described in section 2.4, several other arc fault detection methods based on time domain signature have been proposed. In [40], the voltage signal of a PV module passes through a finite impulse response band pass filter (FIR filter) and the randomness of the output from the FIR filter is measured in terms of variance. If the variance is higher than a predefined threshold, an arc fault is assumed present. Arc detection using two resonant circuits tuned at a few hundred kilohertz is proposed in [3], based on the assumption that there will be no strong signal in the PV array at those frequencies except in the case of an arc. In addition, discrete wavelet transformation (DWT) of current-based arc fault detection has been proposed in [63] and [38]. DWT is more computationally efficient compared to Fourier transformation since DWT analyzes both time and

frequency signatures in the arc signal.

Fault detection using reflectometry has long been used for detecting faults in extended transmission lines and several reflectometry methods were adapted for use in fault detection of PV arrays. A critical comparison among different reflectometry methods used to detect and locate different wire faults can be found in [65]. In time-domain reflectometry (TDR) detection methods, a step/pulsed voltage signal is sent through the two CCCs (or one CCC and EGC) to observe any deviation of the reflected voltage signal due to short or open faults [66] - [70]. Any high impedance (open fault) compared to the normal characteristic impedance provides positive reflection and the amplitude of the voltage signal at the receiving terminal increases. The opposite effect is observed in the case of decreased impedance compared to characteristic impedance (short circuit fault).

Spread spectrum time domain reflectometry (SSTDR) uses a pseudo-random binary noise (PRBN) modulated, high frequency sine wave to generate an autocorrelation plot using the incident and reflected signals. The autocorrelation plot can be used to detect the presence of a fault. SSTDR is advantageous over TDR since SSTDR can be used without disconnecting the inverter. However, both reflectometry based fault detection techniques require a baseline for comparison to detect the presence of faults. Autocorrelation plots generated by the SSTDR hardware before ground fault and after ground faults at separate locations are shown in Figure 2.17 (a). The presence of a ground fault is detected if the autocorrelation plot of the PV string deviates from the autocorrelation plot generated by the PV string without any fault by a certain threshold, as depicted in Figure 2.17 (b).

All the possible faults in the PV systems discussed in this paper along with the detection techniques are summarized in Table 2.3.

2.5. Fault Locating Technologies

Once the fault has been detected, the system operator must determine the location of the line-to-line fault, ground fault, or arc fault in order to repair or replace the faulty component. This process can be very difficult and time consuming with large PV installations.

Faults will present themselves differently after the fault has been de-energized:

- Ground faults will be low impedance paths from the conduction path to the ground.
- Line-to-line faults will establish a new conduction path in the PV array.
- Series arc-faults will be open connections in the PV conduction path because the arc gap will still exist
- Parallel arc-faults will not contain any changes to the conduction path, but there may be damage to the conductors (e.g., increased resistance) that could be detectable by fault locating devices.

There are existing challenges to determine intermittent connections and faults. If the fault is not persistent, it will be even more challenging to locate the faulty component. Table 2.4 investigates different technologies and commercially available products that could be used to locate faults in PV systems.

2.6. Conclusions

Ground faults, line-to-line faults, and arc faults have been discussed in detail in this chapter. Both grounded and ungrounded PV arrays use different commercial fault detection and mitigation techniques to prevent fires. However, due to some limitations in the conventional detection techniques, ground faults may remain undetected and cause severe damage to the PV array and surrounding environment. Similar situations may arise in the case of line-to-line faults.

Depending on the type of arc fault, different mitigation techniques must be implemented. Therefore, it is imperative to detect both the presence and type of arc. This chapter has presented an overview of different state-of-the-art detection and mitigation techniques along with a literature survey of other proposed methods and recommendations for further improvements in PV fault detection, location, and mitigation.

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Table 2.1. Different types of ground fault detection methods

Type of GFD	Systems	Commonality
GFDI fuse	Grounded PV systems	Widely used in US
RCD	More common on ungrounded systems	Widely used in Europe, some in US
Riso	More common on ungrounded systems	Used in European systems. Often used in conjunction with RCDs and can also be used with GFDIs.

Table 2.2. DC rating of PV inverter versus maximum GFDI fuses rating

DC rating of the inverter (kW)	Maximum GFDI fuses rating (A)
0-25	1
25-50	2
50-100	3
100-250	4
> 250	5

Table 2.3. Summary of different PV faults detection techniques

Fault type	Detection method/ tool	Advantages and Limitations	Ref.
Ground fault	GFDI Fuse	Advantages: • Easy to implement • No electric shock from parasitic capacitance discharge • Passive component • Less expensive compared to RCDs and IMDs Limitations: • Can only be used in grounded PV array • Need external sensor to monitor whether the fuse is cleared • Blind spot	[5]
	Residual current measurement (RCD)	Advantages: • Easy to implement • Can be used in both grounded and ungrounded systems • Measurement during inverter operation Limitations: • External noise may result nuisance tripping • Cannot distinguish between line-to-line and ground faults • Shock hazard	[1]
	Isolation resistance measurement (IMD)	Advantages: • More reliable • Test can be done in absence of sunlight Limitations: • Can be influenced by the environmental variations • GFDI fuse need to be disconnected before taking data • Inverter must be disconnected for measurement	[6] [8]
	Numerical analysis using on-site and pre-recorded data: • Artificial neural network • Decision tree-based supervised technique • Graph-based semisupervised learning technique • Minimum covariance determinant (MCD)	Advantages: • Can be implemented for detecting multiple faults • Some numerical method can classify the type of fault as well Limitations: • Need to process on-site recorded data • External sensors required to collect data • May require data from array with faults • Designed for detecting specific faults and performance under other faults may result in false detection	[53] – [55] [59] [60]
	Comparing current magnitude of parallel connected strings	Advantages: • Need to process less data • Fewer sensors required Limitations: • May not classify different faults • Not effective for few number of parallel strings • Mismatch in parallel strings will affect the decision	[56] [57]
	Reflectometry (TDR, SSTDR)	Advantages: • No voltage or current measurement of the PV array is required • Test can be done in absence of sunlight Limitations: • Requires external signal function generator • High speed sampling required • Requires a baseline from the healthy PV array for comparison	[22] [66] – [69]
Line-to-line fault	OCPD Fuse	Advantages: • Easy to implement • Passive component • Inexpensive • Required by proper codes and standards Limitations: • Fault may result in current below the fuse rating • Fuse may not be fast enough to prevent fire	[5]
	Numerical analysis using on-site and prerecorded data: • Artificial neural network • Decision tree-based supervised technique • Graph-based semisupervised learning	Advantages: • Can be implemented for detecting multiple faults • Some numerical methods can classify the type of fault Limitations: • Need to process a lot of on-site recorded data	[53] – [55] [59] [60]

Table 2.3. Continued

Fault type	Detection method/ tool	Advantages and Limitations	Ref.
	technique	• External sensors required to collect data • May require data with faults from the array • Designed for detecting specific faults and performance under other faults may result in false detection	
	Comparing current magnitude of parallel connected strings	Advantages: • Need to process less data • Fewer sensors required Limitations: • May not classify different faults • Not effective for few number of parallel strings • Mismatch in parallel strings will affect the decision	[56] [57]
	Change in direction of current at the on-set of fault	Advantages: • Easy to detect and implement Limitations: • MPPT operation of the inverter can restore the direction of current fault quickly and fault may remain undetected	[64]
Arc-fault	Frequency spectrum analysis	Advantages: • Widely recommended for arc fault detection • Accuracy is high since decision is taken based on broadband spectrum instead of one/few frequencies Limitations: • Requires Fourier transformation of signals • Noise from power converter may result in nuisance tripping • Cannot distinguish between series and parallel arc fault based on frequency content only	[29] [32] [41] [44] [45] [47]
	Change in direction of current at the on-set of fault	Advantages: • Easy to detect and implement Limitations: • MPPT operation of the inverter can restore the direction of current fault quickly and fault may remain undetected. • Applicable for parallel arc fault only	[64]
	Numerical techniques: • Wavelet transformation • Minimum covariance determinant (MCD)	Advantages: • Less computational expensive compared to FFT • Provides both time and frequency information Limitations: • Noise from power converter may result in nuisance tripping • Cannot distinguish between series and parallel arc fault based on frequency content only	[38] [59] [60] [63]
	Estimating randomness in the voltage signal	Advantages: • Easy to implement • Less computational cost compared to FFT and DWT Limitations: • The threshold for variance to alarm arc needs to be precise • Need efficient FIR estimator for calculating variance	[40]
	Resonance Tuned electrical resonator	Advantages: • Easy to implement • No computation required Limitations: • Highly susceptible to noise • Depends on a few frequencies makes the system less reliable	[3]
	SSTDR	Advantages: • No voltage or current measurement of the PV array is required • Test can be done in absence of sunlight • This method has the potential to predict future arc faults through detection of change in resistance in PV strings Limitations: • High speed sampling required • Inverter's noise may result in nuisance tripping • Requires a baseline of healthy PV array for comparison	[71]

Table 2.4. Summary of different PV fault locating techniques

Detection method/ tool	Fault type	Can locate fault precisely upto	Advantages and Limitations	Ref.
Reflectometry (TDR)	Open fault, short (ground) fault	PV Module	Advantages: • No voltage or current measurement of the PV array is required • Test can be done in absence of sunlight • Sensitive to connection degradation as well Limitations: • Requires external signal function generator • High speed sampling required • Requires a baseline for comparison	[22] [66] - [68]
Earth capacitance measurement (ECM)	Open fault	PV Module	Advantages: • Result does not depend on solar irradiance Limitations: • Requires external LCR meter	[66]
Numerical technique	Open and short fault	Number of PV modules	Advantages: • Can locate number of open and short circuited PV modules of a PV system. Limitations: • Requires external irradiance level, temperature and power measurement. • Requires identical electrical characteristics of each modules	[72]
Line checker/ circuit tracer	Open and short fault	Cell level	Advantages: • Higher resolution compared to other fault locating techniques • Can trace the circuit while the PV is generating power Limitations: • Have to physically trace the entire system	[73] – [76]
String current measurement	Open / Ground fault	String level	Advantages: • Commercially available for grounded systems only Limitations: • Requires current monitoring of all the parallel connected strings	[77]
Voltage measurement of each module during operation	Open fault	Module level	Advantages: • Continuous module level data are available at central unit. Limitations: • Requires voltage measurement. • Requires built-in microcontroller, voltage to frequency converter and communication link in each module. • Expensive	[78] [79]

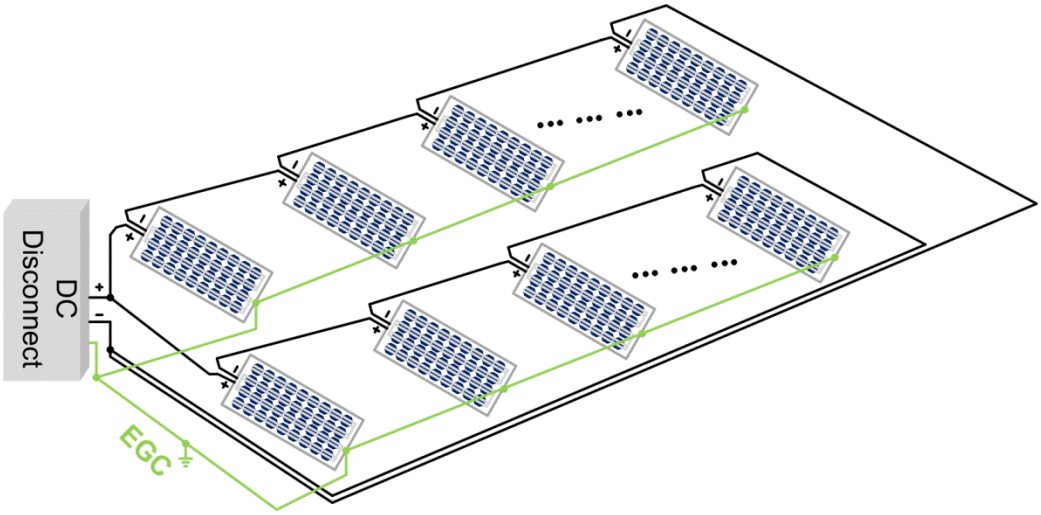
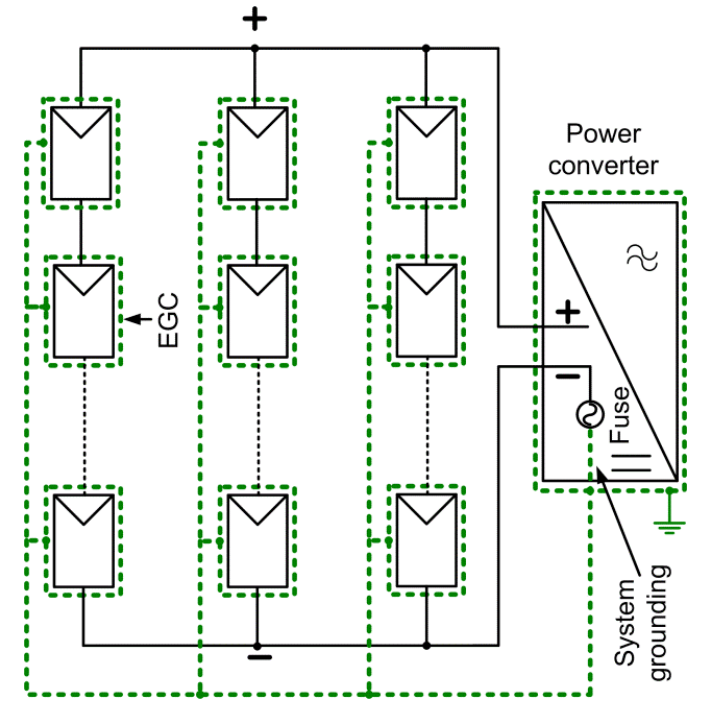
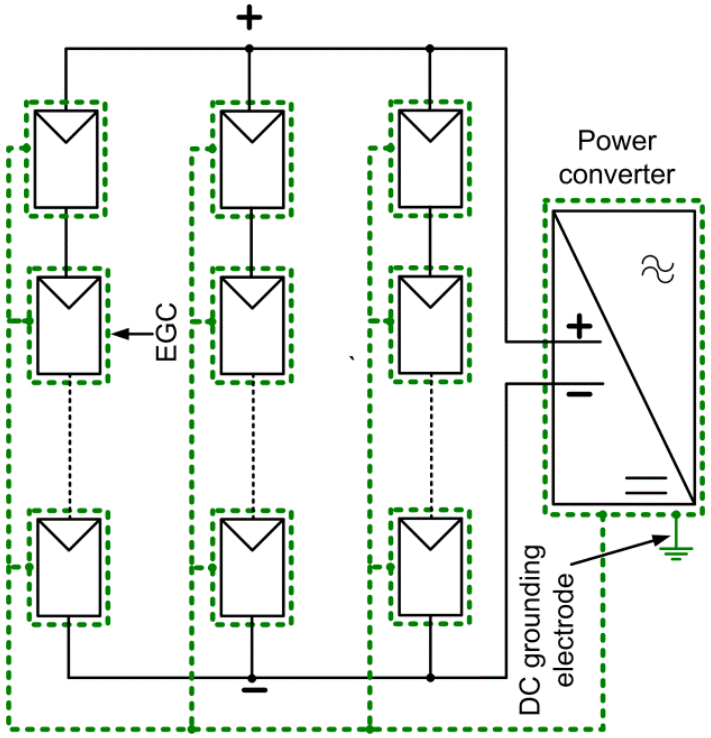


Figure 2.1. Schematic diagram of a simple PV array showing EGC.



(a)



(b)

Figure 2.2. Schematic diagram of (a) grounded and (b) ungrounded PV systems.

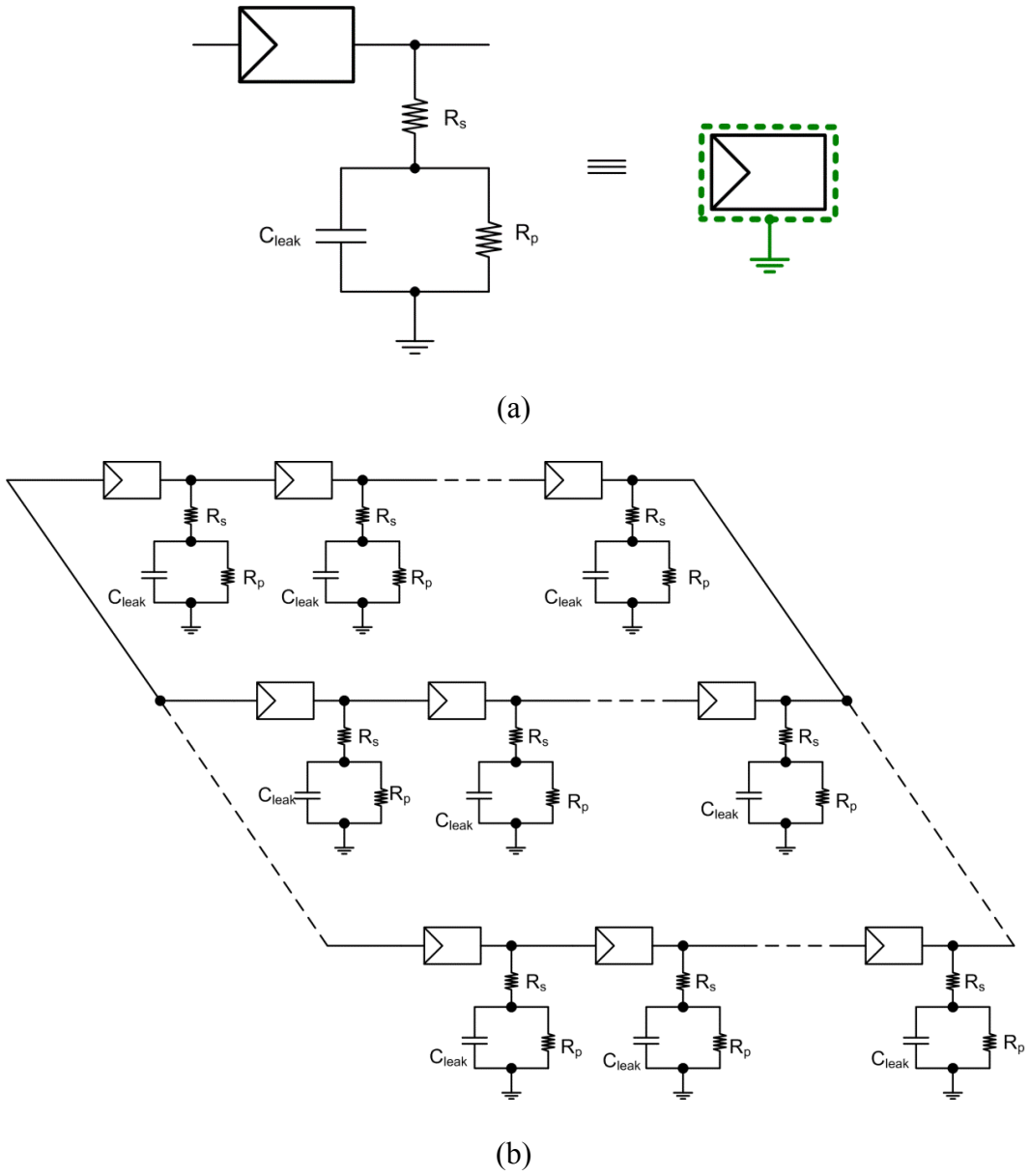


Figure 2.3. Equivalent circuit model of PV (a) module and (b) array.

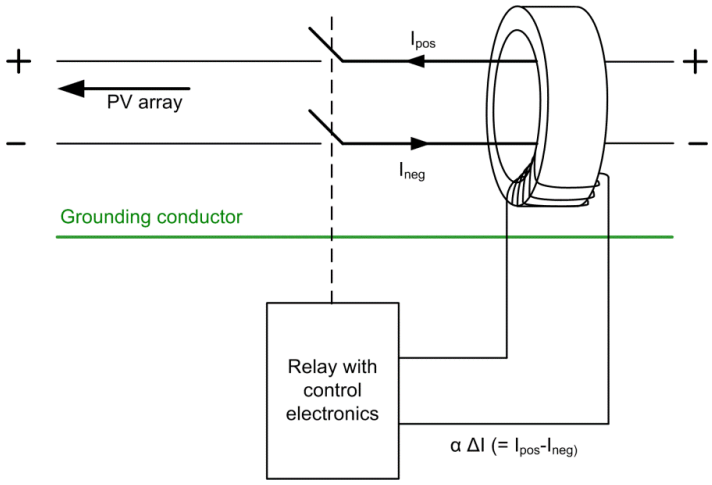
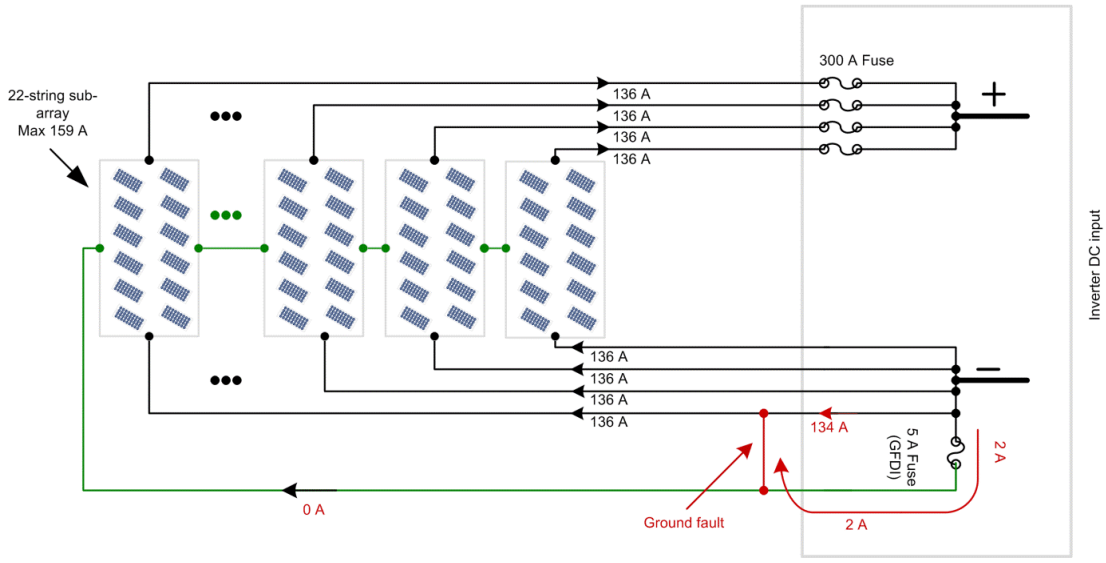
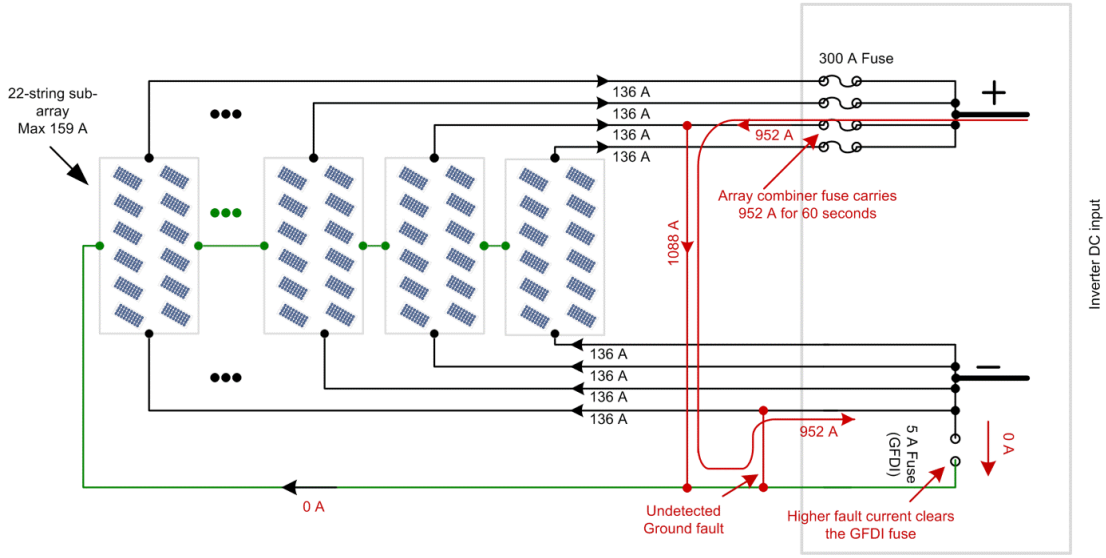


Figure 2.4. Simple schematic diagram explaining operating principle of an RCD.



(a)



(b)

Figure 2.5. Illustrating the fire hazard at Mount Holly. (a) Ground fault was within the range of blind-spot and not cleared by the GFDI fuse, (b) double-ground fault resulted in flow of 952 A through conductors not designed for carrying such high current and resulted in a fire.

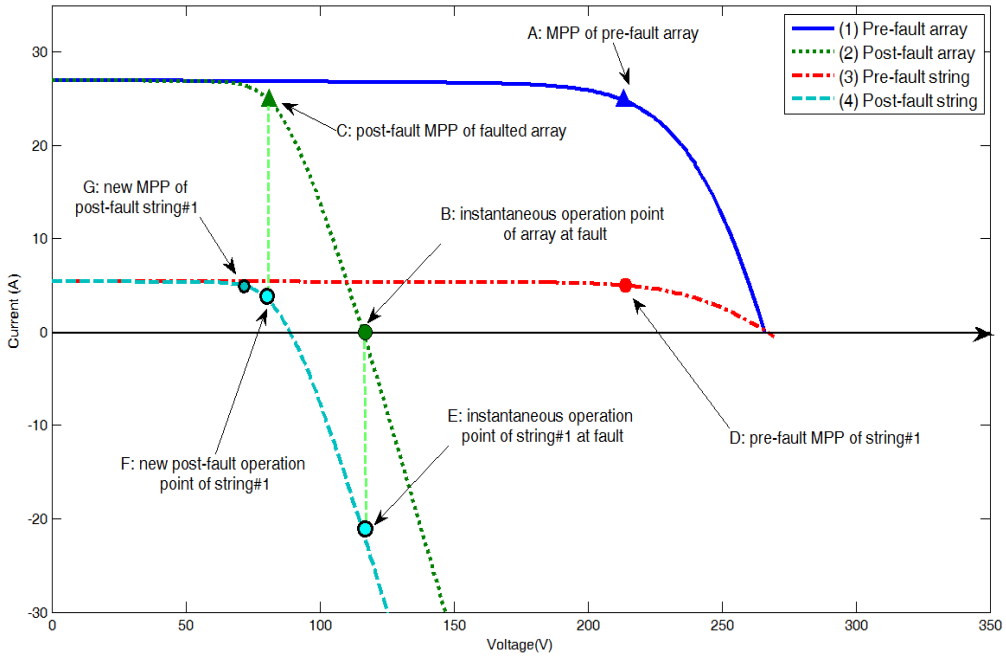


Figure 2.6. Example of I-V characteristics of a PV array before and after ground fault (Reprinted with permission of Ye Zhao, "Fault analysis in solar photovoltaic arrays," M.S. thesis, Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, 2010).

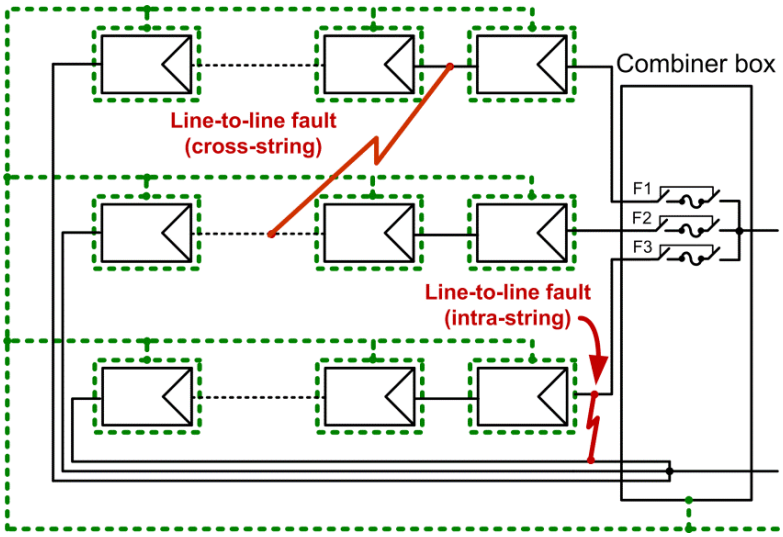


Figure 2.7. Examples of different line-to-line faults in a PV array.

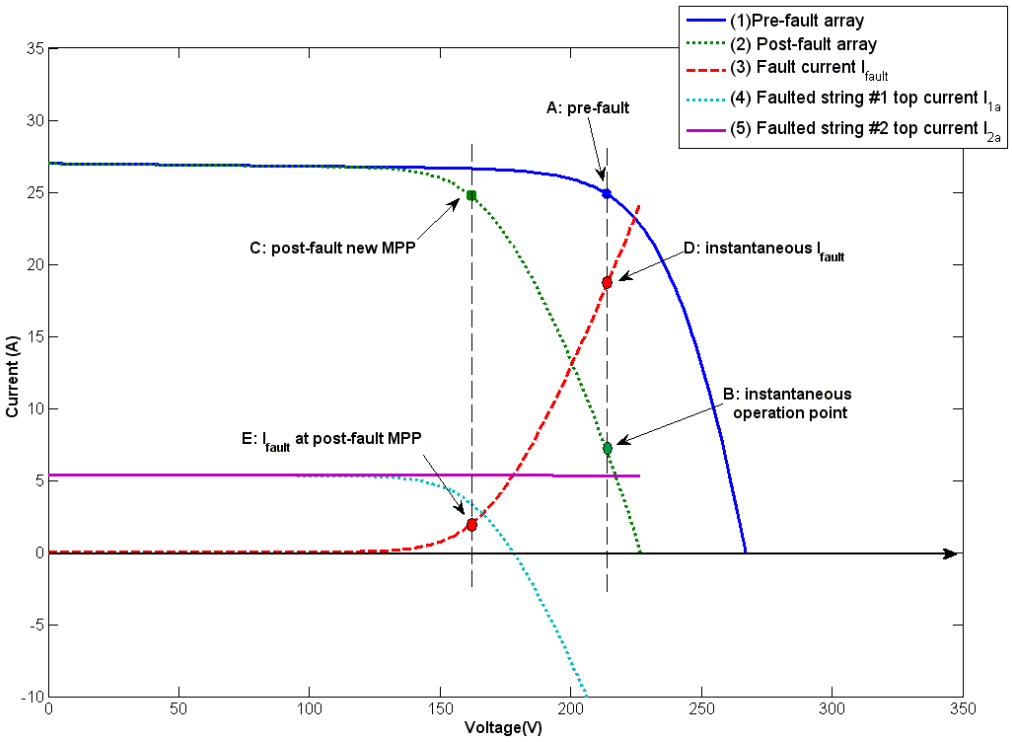


Figure 2.8. Example of change in I-V characteristics of a PV array under a line-line fault (Reprinted, with permission, from Ye Zhao, "Fault analysis in solar photovoltaic arrays," M.S. thesis, Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, 2010).

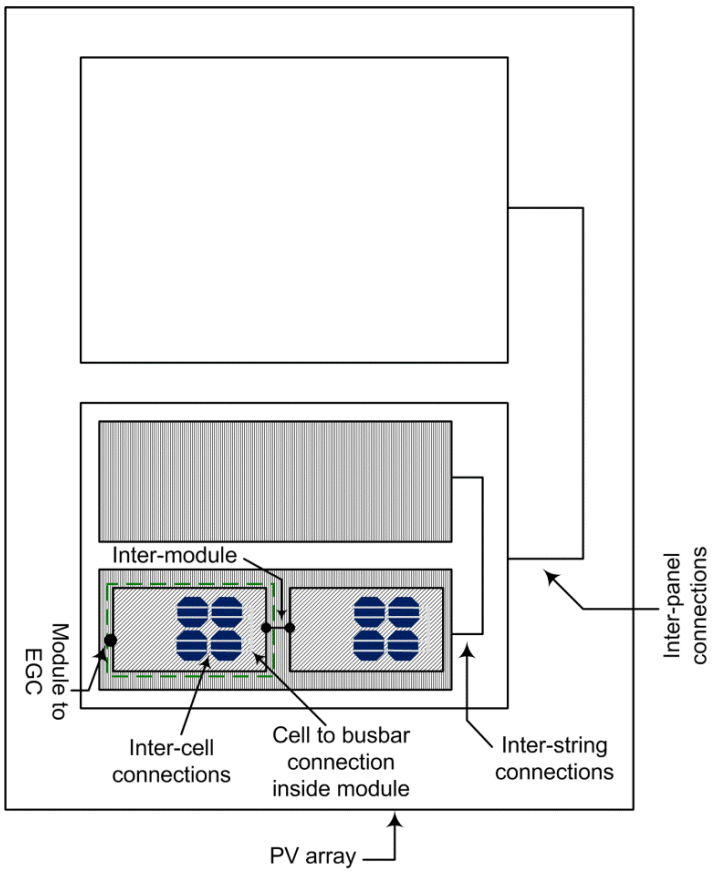


Figure 2.9. Illustration of different interconnections/junctions inside a PV array.

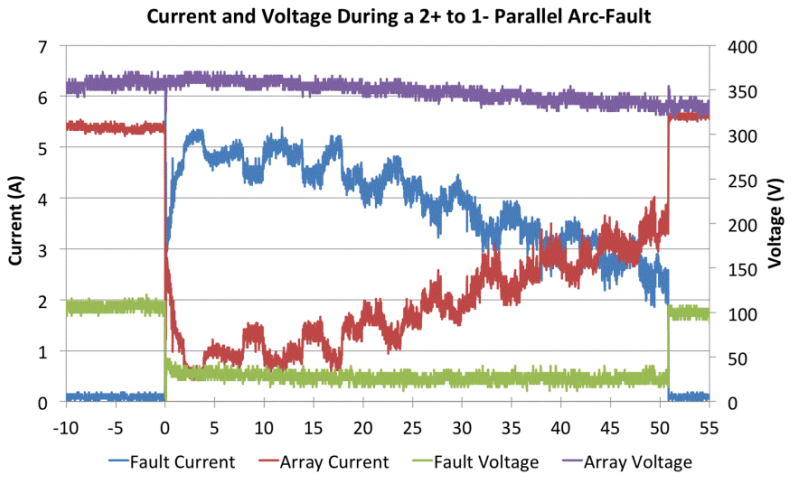


Figure 2.10. Voltage and current variation at the on-set of parallel arc-faults with inverter connected (© 2013 IEEE. Reprinted, with permission, from Jack D. Flicker and Jay Johnson, "Electrical simulations of series and parallel PV arc-faults," in *Proc. IEEE Photovoltaic Specialists Conference (PVSC)*, pp. 3165-3172, 16-21 June 2013).

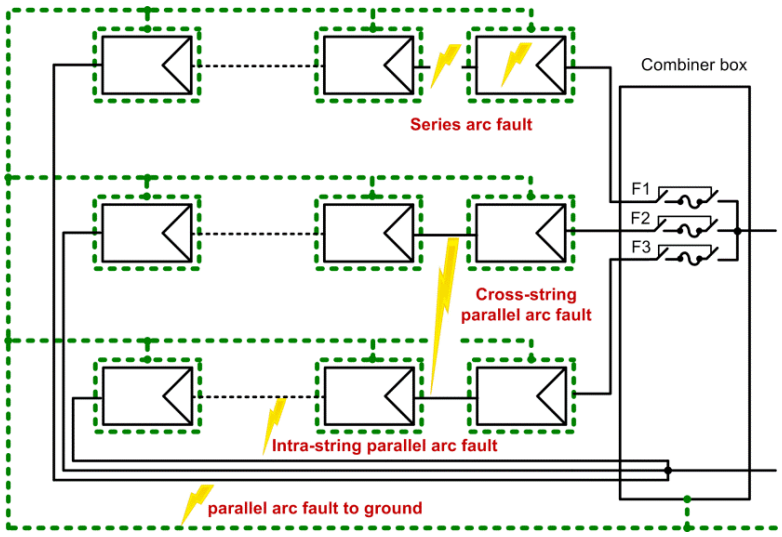


Figure 2.11. Examples of different arc faults in a PV array.

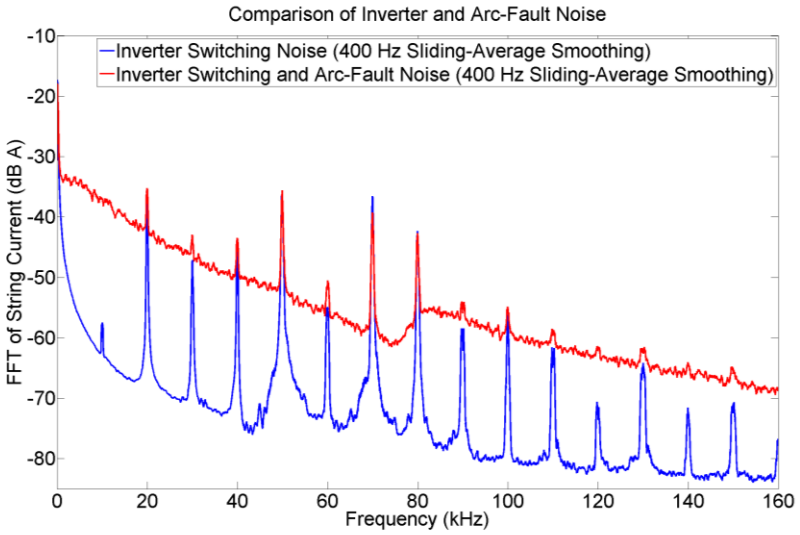


Figure 2.12. Noise from the inverter with and without a series arc fault (© 2012 IEEE. Reprinted, with permission, from J. Johnson and J. Kang, "Arc-fault detector algorithm evaluation method utilizing prerecorded arcing signatures," in *Proc. IEEE Photovoltaic Specialists Conference (PVSC)*, pp. 1378 – 1382, 3-8 June 2012).

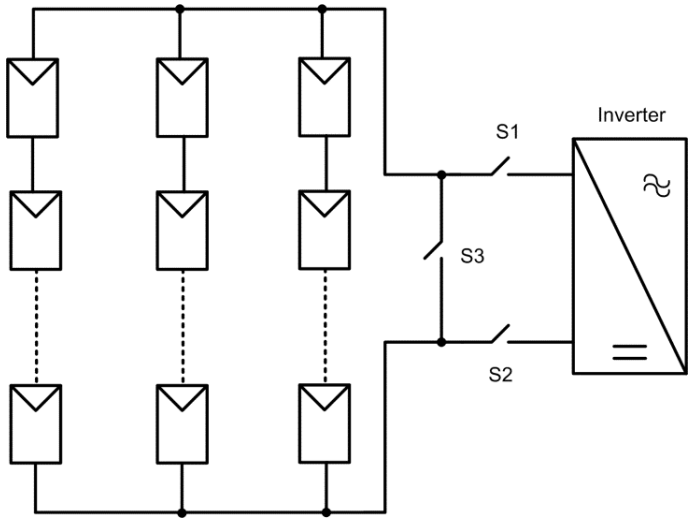
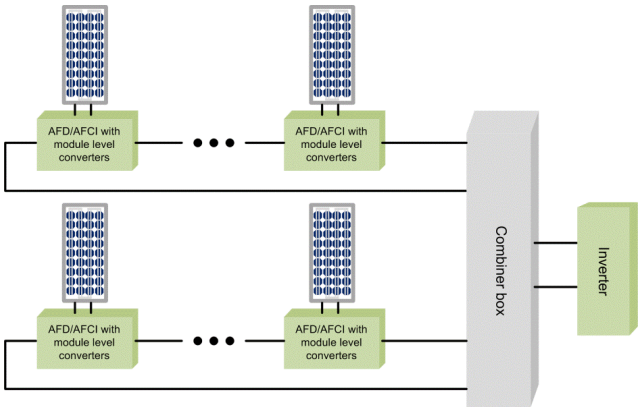
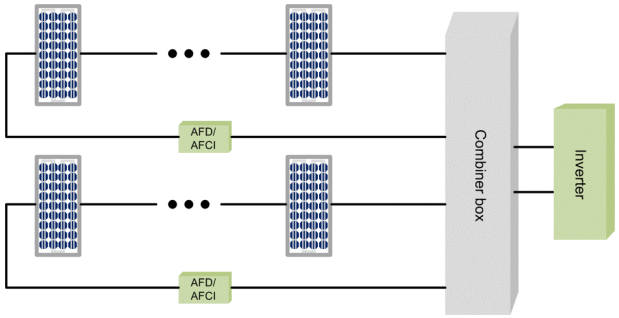


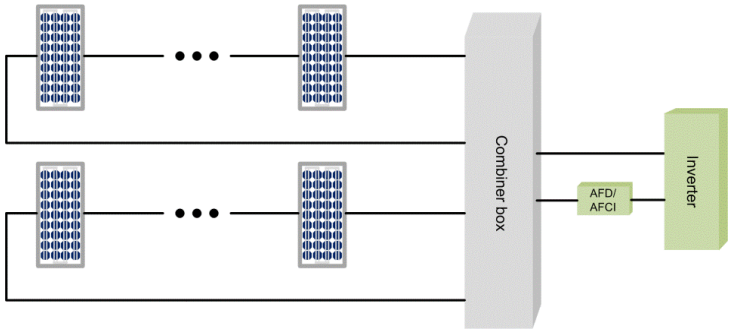
Figure 2.13. Explaining the switching scheme for extinguishing both series and parallel arc faults.



(a)



(b)



(c)

Figure 2.14. Different configurations for installing AFD/AFCI in a PV array: (a) module level, (b) string level, (c) panel/array level.

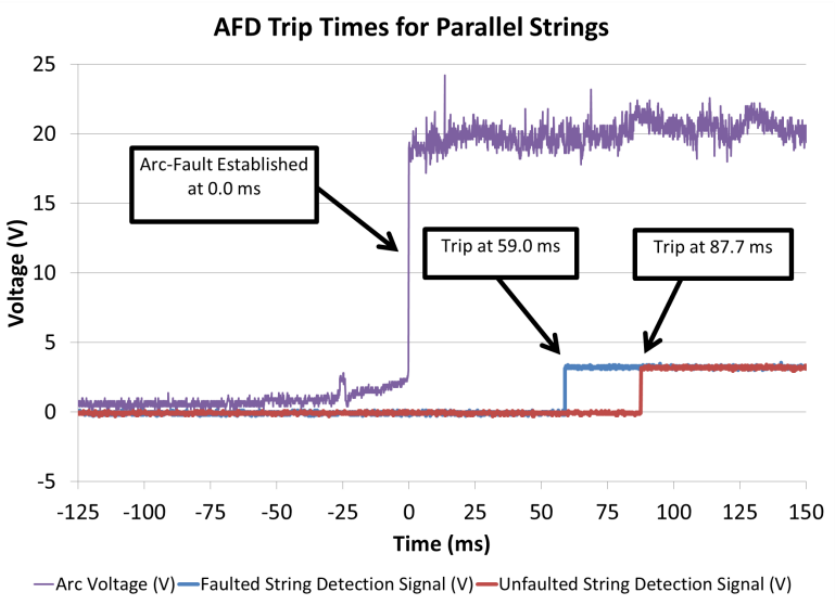
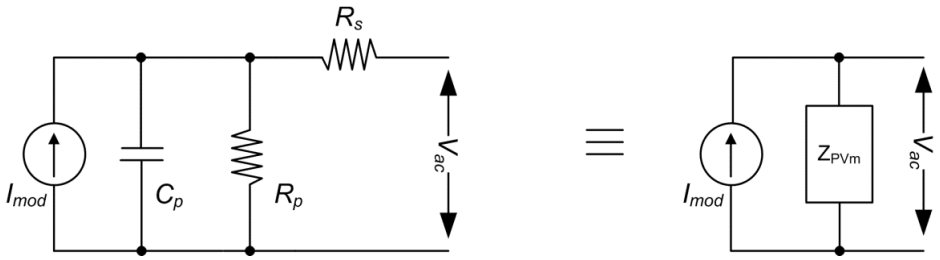
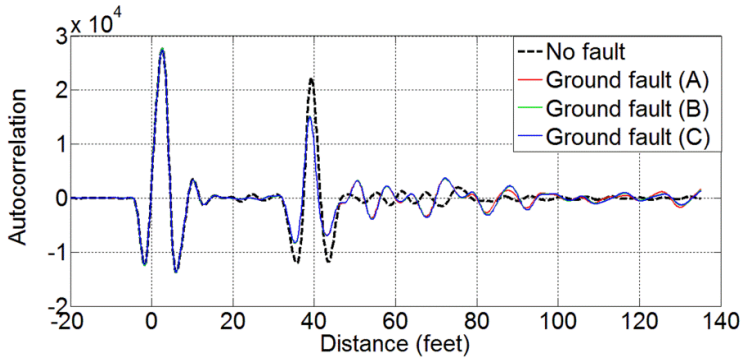


Figure 2.15. Experimental trip times for faulty and healthy strings in which the faulty string AFD tripped first (© 2012 IEEE. Reprinted, with permission, from J. Johnson *et al.*, "Crosstalk nuisance trip testing of photovoltaic DC arc-fault detectors," in *Proc. IEEE Photovoltaic Specialists Conference (PVSC)*, pp. 1383-1387, 3-8 June 2012).

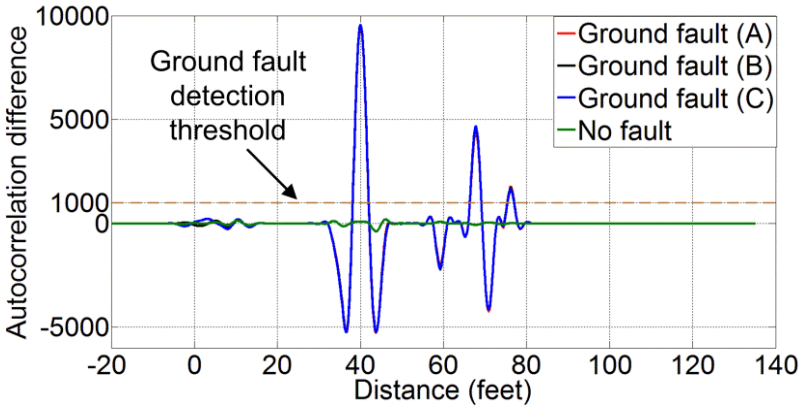


$$Z_{PVm} = \left(R_s + \frac{R_p}{\left(\omega R_p C_p\right)^2 + 1}\right) - j\left(\frac{\omega R_p^2 C_p}{\left(\omega R_p C_p\right)^2 + 1}\right)$$

Figure 2.16. Dynamic electrical circuit model for a PV module.



(a)



(b)

Figure 2.17. SSTDR results for fault detection in a PV array: (a) autocorrelation plot generated by a PV string consists of seven modules without fault and with ground faults in three different locations in the string, (b) difference in autocorrelation response from the PV string with fault and under normal condition for ground fault in three different locations.

CHAPTER 3

GROUND FAULT DETECTION USING SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY (SSTDR)

A healthy PV array has specific impedances between nodes, and any ground fault changes these impedances. High frequency signals can be used to detect these faults, and any reflection of the incident signal at the fault location can be used to detect the fault location. A fault detection algorithm using spread spectrum time domain reflectometry (SSTDR) method is introduced in this chapter. SSTDR is a reflectometry method that has been successfully used for detecting and locating aircraft wire faults. However, wide variation in impedance through different materials and interconnections makes fault detection in PV arrays using reflectometry more challenging. Unlike other conventional PV array ground fault detection techniques, SSTDR does not depend on the amplitude of fault-current. Therefore, SSTDR can be used in the absence of solar irradiation as well. The proposed PV ground fault detection technique has been tested in a real-world PV system and it has been observed that a PV ground fault can be detected confidently for different configurations of the PV array (single and double strings) and different fault resistances (0.5, 5 and 10 Ω). Moreover, it has been experimentally verified that the proposed algorithm works at low irradiance and can detect ground faults that may not be detected using a conventional ground fault detection and interrupter (GFDI) fuse.

3.1 Spread Spectrum Time Domain Reflectometry (SSTDR)

3.1.1 Basic Concepts of Reflectometry

The basic concept of reflectometry is based on the reflection of an electromagnetic signal at the load terminal of a transmission line. In simple words, a transmission line can be considered as a two-port network with each port having two terminals. A schematic diagram of a simple transmission line having length L connecting a source generator to a load through a transmission line of length L is shown in Figure 3.1 [1]. Any incident signal (V_0^+, I_0^+) travels through the transmission line towards the load impedance and a portion of the signal is reflected back (V_0^-, I_0^-) if the load does not match the characteristic impedance of the line. This reflection of signal at the impedance mismatch may be ignored when the length of the transmission line is very small compared to the wavelength (λ) of the propagating signal and becomes important when $L/\lambda \geq 0.01$ [2]. One example of transmission line where reflection can be ignored is the 50/60Hz power transmission line where the length of the wire is very small compared to the wavelength of the signal.

A transmission line is, in general, considered to be a uniform electrical signal-carrying path, and a lumped-element circuit model of typical transmission line consists of four per unit length parameters, as shown in Figure 3.2 [2] – [4]. These are called transmission line parameters and defined as follows:

R' (*Ω/m*): combined per unit length resistance of both of the conductors

L' (*H/m*): combined per unit length inductance of both of the conductors

G' (*S/m*): combined per unit length conductance of both of the conductors

C' (*F/m*): combined per unit length capacitance of both of the conductors

Traveling wave equations for the voltage phasor (*V(d)*) and the current phasor (*I(d)*) through the transmission line shown in Figure 3.1 can be written as equation (3.1):

$$V(d) = V_0^+ e^{-\gamma d} + V_0^- e^{\gamma d} \tag{3.1a}$$

$$I(d) = I_0^+ e^{-\gamma d} + I_0^- e^{\gamma d} \tag{3.1b}$$

where, γ is the complex propagation constant and is defined as in equation (3.2):

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} \tag{3.2}$$

Here, ω is the angular frequency. Two important parameters of the transmission line are the characteristic impedance (Z_0) and the reflection coefficient (ρ). The characteristic impedance Z_0 is defined as the ratio between the voltage and current of the incident and the reflected wave as shown in equation (3.3) [2] – [5].

$$Z_0 = \frac{(R' + j\omega L')}{\gamma} = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} = \frac{V_0^+}{I_0^+} = \frac{-V_0^-}{I_0^-} \tag{3.3}$$

The ratio between the reflected and incident voltage signals is known as the reflection coefficient (ρ) as defined in equation (3.4).

$$\rho = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.4}$$

An open circuit generates a positive reflection of the voltage wave, and a short circuit creates a negative reflection at the load terminal. It should be noted that both impedance (Z_0 or Z_L) and reflection coefficients are complex numbers, and a plot showing the magnitude of the load impedance vs. magnitude of the reflection coefficient for transmission line with characteristic impedance equal to 50 Ω is shown in Figure 3.3. The correlation between the load impedance and the reflection coefficient is not linear through the entire range; however, any increase in load impedance increases the magnitude of the reflection coefficient.

Generating an equivalent transmission line model for a PV string/array is a giant task because of the presence of different materials and interconnections throughout the signal propagation path. Moreover, transmission line parameters vary from one PV plant to another due to the use of different PV modules (solar cell material, shape, size, orientation of conducting ribbons, number of cells in series, orientation of series-connected solar cells, design and material of the metal module, EGC connection variation etc.), spatial orientation of modules, type and length of grounding and current carrying cables, number of modules connected in series, etc. Initiatives have been taken to develop a transmission line model for PV modules considering only the metal connectors of a PV module in [6]. It has been concluded that issues related to the method of installation and presence of multiple reflections occurring at different mismatches makes interpretation of the time domain reflectometry extremely difficult.

3.1.2 SSTDR Theory

There are several fault detecting and locating techniques developed based on reflectometry theory: time domain reflectometry (TDR), frequency domain reflectometry (FDR), mixed signal reflectometry (MSR), sequence time domain reflectometry (STDR), spread spectrum time domain reflectometry (SSTDR), etc. Each of these methods uses a special incident signal pattern and signal processing techniques to detect and locate wiring faults. Among different reflectometry techniques, spread spectrum time domain reflectometry (SSTDR) provides several advantages over other reflectometry techniques such as low-cost fault detection in powered/live cables, very high noise immunity, embedded solution, etc.

SSTDR uses a pseudo random binary signal called pseudo noise code (PN code), and it consists of randomly generated 1 and 0s (each 1/0 is known as a chip) [7] – [10]. The chip rate of the PN code is defined as the number of chips generated each second, and the length of the PN code is defined as the number of bits after the sequence is repeated. SSTDR can be implemented in several ways as discussed in [1] [11] – [16], and a simple schematic diagram is shown in Figure. 3.4.

The PN code is modulated with a carrier sine wave with a frequency equal to the chip rate of the PN code to generate the incident signal. The reflected signal is first multiplied and then summed to generate a point on the autocorrelation plot at a fixed lag/delay. A variable phase delay generator introduces a phase delay in the carrier signal to generate other points along the autocorrelation plot. The frequency of the carrier sine wave is also known as center frequency of SSTDR. Any mismatch from the characteristic impedance at the load terminal generates a lobe at a time delay in the autocorrelation plot

corresponding to the distance from the source terminal. A lobe with a positive peak indicates a positive reflection coefficient and a negative peak indicates a negative reflection coefficient.

Figure 3.5 shows a portion of the PN code of length 1023. Figure 3.6 and Figure 3.7 show the corresponding carrier signal and the incident signal. This is similar to data encryption techniques used in cellular communications for transmitting and receiving signals through a noisy network. The FFT of the PN code and the incident signal are shown in Figure 3.8 and Figure 3.9. The FFT of the PN code is similar to a sinc function where the width of the main lobe is twice the chip rate of the PN code or center frequency. Fourier transformation of the incident signal is similar to a double sideband suppressed carrier signal where the signal has a large spectral distribution, since the PN code has been used as the modulating signal.

A WILMA LWG40414 hardware device (Figure 3.10) based on SSTDR technology from Livewire Innovation has been used in this research in static mode. Static mode operation allows scanning of the system connected to the hardware with center frequencies equal to 96, 48, 24, 12, 6, 3, 1.5, 0.75 and 0.375 MHz, and provides 92 points on the autocorrelation plot for each scan. There are eight points on the autocorrelation plot calculated within the time period of the carrier signal and, thereby, the maximum fault distance in the autocorrelation plot is inversely proportional to the center frequency, as shown in equation (3.5):

$$FD_{max} = \frac{v_p \times c \times (N_{total} - N_{offset})}{N_{delay} \times f_{center}} \tag{3.5}$$

where,

FD_{max} = maximum fault distance with a specific center frequency

c = velocity of light in free space ≈ 3 X 108 m/s

v_p = velocity of propagation of the electrical signal as a percent of velocity of light in free space

N_{total}= total number of points on the autocorrelation plot provided to the user by WILMA LWG40414

N_{offset} = number of offset points that defines the starting point for distance calculation

N_{delay} = number of points on the autocorrelation plot corresponding to the time period of the carrier signal

f_{center} = frequency of the carrier signal

Autocorrelation plots generated by the SSTDR hardware for open circuit and short circuit at the end of a ~50 feet RG-6U (v_p = 66%) coax cable are shown in Figure 3.11. The initial peak in the autocorrelation plots is due to a mismatch between the output impedance of the hardware and the characteristic impedance of the RG-6/U coax cable (Z_0= 75 Ω). The other peak at an approximate distance of 50 feet is due to the short or open circuit. There might be other peaks in the autocorrelation plot due to multiple reflection of the signal at the mismatch, since the first reflection may reflect back at the input terminal and generate another reflection at the impedance mismatch [18].

3.2 Ground Fault Detection Using SSTDR

The proposed ground fault detection algorithm was implemented at the Distributed Energy Technologies Laboratory (DETL) of Sandia National Laboratories (SNL) (Figure

3.12). A PV string consisting of seven, series-connected PV modules, was interfaced with the WILMA LWG40414, as depicted in the schematic diagram in Figure 3.13. Specifications of the PV modules are listed in Table 3.1. The inverter was disconnected from the PV string, and the open circuit voltage was approximately 415V. Output terminals of the WILMA LWG40414 board were connected to the positive CCC and the EGC of the PV string. The ground fault detection algorithm developed here is based on three steps described below, and a flowchart of the algorithm is shown in Figure 3.14.

3.2.1. Creating Baseline

As mentioned earlier, every PV array has different reflection patterns, and it is necessary to create a baseline for a PV array, under consideration here, that will work as a reference to detect ground faults later. In order to create the baseline, the PV string without any ground fault was scanned in static mode five times, and autocorrelation plots were interpolated at the rate of 10 using the interp() function in MATLAB.

Autocorrelation plots with different carrier/center frequencies for the same scan are shown in Figure 3.15. The abscissa of the autocorrelation plots are changed to time delay, since the velocity of propagation through the PV string is unknown and expected to vary throughout the PV string. The autocorrelation data generated by the WILMA LWG40414 for the same setup are not identical and show some variation, as shown in the error plot for a carrier frequency equal to 96 MHz in Figure 3.16. Only autocorrelation data for carrier frequency = 96 MHz are shown due to space limitations. These variations in the autocorrelation plot are expected due to thermal noise, noise from the analog to digital conversion etc. The average of these five autocorrelation plots for each center frequency

is considered as a baseline for differentiating PV array without ground fault (healthy PV array) and with ground fault.

It should be noted that scanning a system five times and interpolating at the rate of 10 are both chosen arbitrarily, and a higher number of scans or interpolation rate is recommended if the system can handle a big amount of data.

3.2.2. Estimating System Noise

The same PV array was scanned five times, and the autocorrelation data were interpolated and averaged following the same steps described in section 3.2.1. The baseline calculated in the previous subsection was subtracted from the average data calculated here and the absolute values of the differences were taken. The sum of the absolute differences between the average autocorrelation data and the baseline is considered as an estimate of system noise since both data were collected for the same healthy PV string. This sum of absolute differences is called the “area” in this manuscript and an area considerably higher than the estimated system noise will be assumed to indicate the existence of a ground fault in the PV string.

3.2.3. Fault Detection

Artificial ground faults were created at different nodes between the modules using a 0.5Ω fuse to validate the fault detection algorithm. There was no circulating current flowing through the PV string since the string was disconnected from the inverter. The PV string was scanned five times with ground faults at different nodes, shown in Figure 3.13, and average autocorrelation plots were generated as described in section 3.2.1 for

faults at different locations in the PV string. The difference between the average autocorrelation plot with ground fault in a specific location and the baseline was calculated, and the area under the absolute autocorrelation difference plots was calculated following the procedure described in section 3.2. The area for ground faults at different locations in the same PV string along with the system noise is shown in Figure 3.17 for a center frequency equal to 96 MHz, and it can be noticed that the PV array generates an area which is higher than the system noise whenever there is a ground fault in the array.

3.3. Influence of Different Parameters on Fault Detection Algorithm

The influence of different parameters, i.e., center frequency of SSTDR, impact of fault resistance, solar irradiance (to test the feasibility of fault detection during the night and cloudy days), parallel strings and double ground fault, on the robustness of the algorithm are discussed in this section.

3.3.1. Impact of Carrier Frequency

The Fourier transform of the incident SSTDR signal was shown in Figure 3.9. The spectral distribution of the signal is highly dependent on the carrier frequency because the PN code generated using the carrier frequency and chip rate of the PN code varies in proportion to the carrier frequency. The width of the main lobe of the Fourier transform of the incident signal is twice the carrier frequency starting from 0 Hz, and most of the energy of the incident signal is confined within that bandwidth. The power density of the incident signal spreads over a wider bandwidth with an increase in carrier frequency and,

thereby, the response (reflected signal) is expected to vary with the variation in the carrier frequency.

The area under the absolute average autocorrelation difference plots for the same PV string with ground faults at different nodes and fault resistance equal to 0.5 Ω are shown in Figure 3.18. Interestingly, carrier frequencies lower than 6 MHz produce more reliable results compared to higher carrier frequencies for ground faults in the PV string. As an example, in Figure 3.18 (a) the area with ground faults is lowest at location 6_5 and it is only ~1.29 times the system noise for a center frequency equal to 96 MHz. For 6MHz, 3MHz, 1.5 MHz, 0.75 MHz and 0.375 MHz; these ratios are about 2.5, 7.96, 5.54, 48.04 and 31.89, respectively. Moreover, minimum area is observed at different locations of the PV string for different center frequencies. An extensive impedance domain mapping is required to explain the pattern of variation in area. One possible reason for smaller change in area due to ground fault at 96 MHz center frequencies compared to 6 MHz is the presence of higher internal thermal noise and external noise from other communication channels at higher frequencies [19]. Further investigations need to be performed to figure out the exact reason behind this phenomenon, but it was decided to concentrate on the center frequency range of 375 kHz - 3MHz in order to avoid any false ground fault detection at this point.

3.3.2. Impact of Fault Resistance

The ground fault resistance is an important aspect in a fault detection scheme, since it may create a fault within the blind spot of the GFDI fuse. Ground faults ware created at different locations in the PV string for the following fault resistances: 0.5 Ω, 5 Ω and 10

Ω. The correlation area plots for different fault resistances and center frequencies (375 kHz - 3MHz) are shown in Figure 3.19. The same baseline and system noise were used for all fault resistances since these two parameters (baseline and system noise) are independent of the fault resistance. It is expected that the area will decrease with the increase in fault resistance for the same center frequency and fault location because a healthy PV string has a very high resistance from any point on the CCCs to the EGC. Although an overall decrease in area is observed with an increase in fault resistance, no specific pattern is observed for an increase in fault resistance for all fault locations. As an example, with a center frequency equal to 0.75 MHz and fault location 5_4, the area decreases from 1.451e6 for 0.5 Ω to 0.9529e6 for 5Ω, and then to 0.6221e6 for 10Ω fault resistance. However, the area with 10 Ω is 20.59 times higher than the system noise (0.0302e6). In contrast, a closer look at Figure 3.19 (c), (g) and (k) reveals that the area for fault location 1_0 with center frequency 0.75 MHz is smaller than the area for fault location 2_1 for a fault resistance equal to 0.5 Ω, and is higher for fault resistances 5 Ω and 10 Ω. This might be due to the high frequency response of the resistor and connections created to introduce the ground fault. However, it can be concluded that the presence of a ground fault can be detected confidently for center frequencies lower than 6 MHz irrespective of the fault resistances (0.5 Ω, 5 Ω and 10 Ω).

3.3.3 Impact of Parallel Connected Strings

In a larger PV array, it is expected that there will be several PV strings connected in parallel, and it might not be a feasible option to disconnect all the parallel strings to perform tests to detect ground faults. In order to verify the algorithm, two PV module

strings were connected in parallel at the same facility, shown in Figure 3.12, and ground faults were created at different interconnecting nodes in one of the PV strings using a 0.5 Ω resistor, as depicted in Figure 3.20. Baseline autocorrelation plots for single string and two parallel strings without any ground fault are shown in Figure 3.21 for center frequency 1.5 MHz, and there are some differences between the plots.

Ground faults were created in one of the parallel strings. Area plots for different center frequencies (0.375 MHz to 3MHz) are shown in Figure 3.22. In every fault condition, the area plot height is significantly higher than the system noise (no fault). Therefore, it can be concluded from the bar charts that SSTDR can be used for ground fault detection in parallel-connected PV modules as effectively as in single PV strings. It is possible to locate the string with the PV fault using SSTDR, since the algorithm can detect the ground fault in parallel connected strings, and each string can be examined with respect to its own baseline by disconnecting the parallel connection to detect ground faults after a ground fault has been observed in the array.

3.3.4. Impact of Solar Irradiance

Nominal changes occur in the electrical equivalent impedance of the solar cells when there is a change in solar irradiance, and this works in favor of reflectometry based fault detection schemes. In order to investigate the feasibility of ground fault detection using SSTDR during the night or at low irradiance, a test was performed in a laboratory environment (< 5 W/m2 solar irradiance) with a PV string consisting of seven 100W series-connected PV modules. Specifications of the PV modules are provided in Table 3.2. A test setup similar to the schematic shown in Figure 3.13 was built and ground

faults were created at different nodes by creating a short circuit connection. Similar tests were performed as described in section 3.2, and the results are shown in Figure 3.23.

It should be noted that the PV modules used inside the laboratory were smaller than the outdoor PV modules. Therefore, they are expected to have different patterns for same the carrier frequency since the equivalent lumped-circuit parameters (shown in Figure 3.2) are different. However, it can be concluded from Figure 3.23 that the proposed algorithm can be used for ground fault detection in very low irradiance as confidently as in an outdoor environment.

3.3.5. Double Ground Fault

A double ground fault test was performed using the same PV string described in section 3.3.4 inside the laboratory facility, since it is not safe to create a double ground fault in an outdoor PV string. A similar situation occurs in a real PV system when a ground fault remains undetected and another fault occurs during the night. Two short circuits were created at 8_7 and 6_5 (arbitrarily chosen locations) positions and the PV string was scanned using the SSTDR hardware. A double ground generates higher area under the absolute autocorrelation difference plot than the system noise and can be detected confidently, as shown in Figure 3.24.

3.3.6. Impact of Number of Scans on the Estimation of System Noise

This section investigates the impact of number of scans considered to estimate the system noise. Correct estimation of system noise is crucial since it provides the threshold

for fault detection in the PV arrays. A PV string consisting of seven series-connected PV modules was scanned in intermittent scan mode for different center frequencies (375 kHz -96 MHz) and system noise was estimated using different number of scans. These results are shown in Figure 3.25.

It is apparent from the results that the estimation of system noise varies the increase of number of scans considered for the system noise. However, results are more consistent for center frequencies below 3 MHz. System noise decreases with increased number of scans for these frequencies. However, no conclusive results were found for center frequencies above 3 MHz. Therefore, it is recommended to use center frequencies lower than 3 MHz and increase the number of scans to achieve higher accuracy in fault detections.

3.4. Limitations of the Proposed Technique

The proposed algorithm is very robust, and it has many advantages compared to existing solutions. However, the proposed technique still has several limitations.

1) It does not perform well with an inverter connected to the PV array.

2) The existing hardware does not provide arbitrary frequency sweep of the carrier/center frequency.

3) The method requires separate calibration (baseline and estimation of noise) for different PV array.

4) The method may require new baseline and estimation of system noise to address change of wires, connections or modules.

3.5. Conclusions

A novel SSTDR based ground fault detection algorithm was presented in this chapter. Detection of ground faults in PV arrays using reflectometry is challenging because there exist hundreds of interconnections and impedance mismatches inside a single PV string. It was demonstrated that the proposed algorithm can be successfully used for detecting ground faults in a PV array. Moreover, this technique can be implemented for testing ground faults during night or at low illumination, when the PV array is expected to generate no power. This makes the proposed technique more accurate and effective compared to any existing methods. This chapter has presented the feasibility of using the SSTDR-based algorithm with any variation in the number of strings, fault resistance and number of faults, and the proposed method can effectively detect complex fault conditions as well.

3.6. References

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Table 3.1. Specification of a PV module used in the test setup (at 1000W/m^2, 25ºC cell temperature)

Maximum power (P_{max})	200W
Short circuit current (I_{sc})	3.83 A
Open circuit voltage (V_{oc})	68.7 V
Maximum power current (I_{pmax})	3.59 A
Maximum power voltage (V_{pmax})	55.8 V

Table 3.2. Specification of a 100W PV module used inside the lab setup (at 1000W/m^2, 25ºC cell temperature)

Maximum power (P_{max})	100 W
Short circuit current (I_{sc})	5.75 A
Open circuit voltage (V_{oc})	22.5 V
Maximum power current (I_{pmax})	5.29 A
Maximum power voltage (V_{pmax})	18.9 V

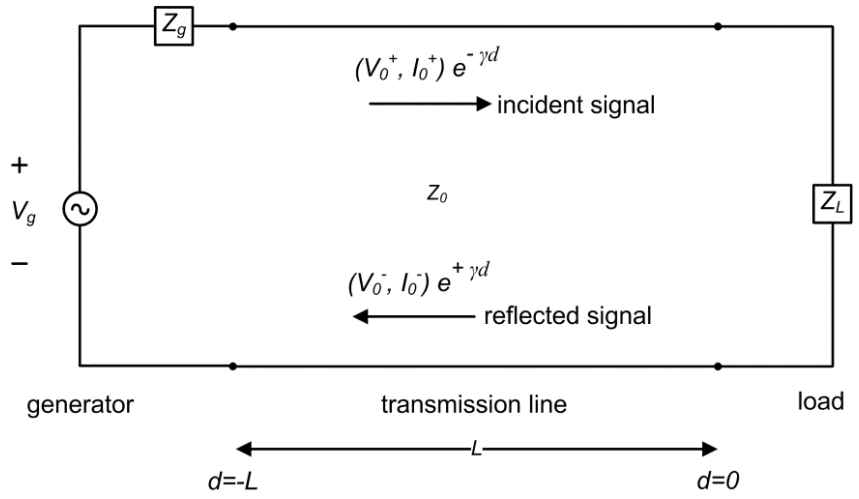


Figure 3.1. Schematic diagram of a transmission line of length L and characteristic impedance equal to Z_0. A generator circuit is connected at one end (d=-L) and the other end (d=0) is connected to load Z_L. An incident signal with voltage and current (V_0^+, I_0^+) traveling towards the load and a reflected t signal with voltage and current (V_0^-, I_0^-) traveling towards the load.

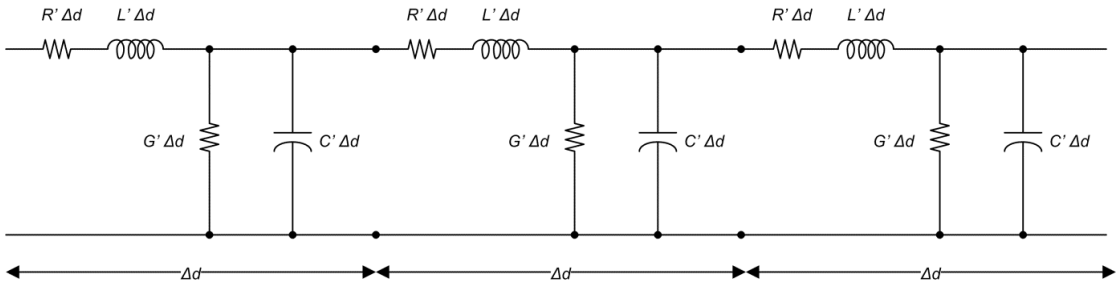


Figure 3.2. Lumped-element circuit model of a typical transmission line. Here Δd represents a finite and infinitesimal length of transmission line.

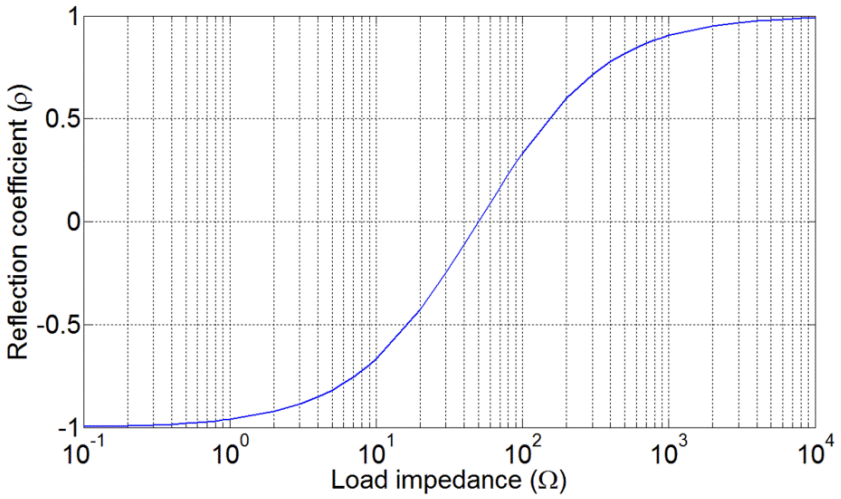


Figure 3.3. Relation between the magnitudes of load impedance and reflection coefficient.

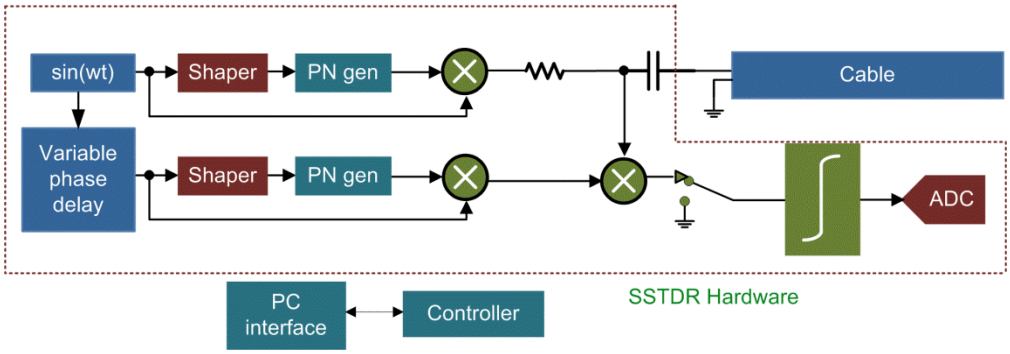


Figure 3.4. Schematic diagram of the SSTDR hardware.

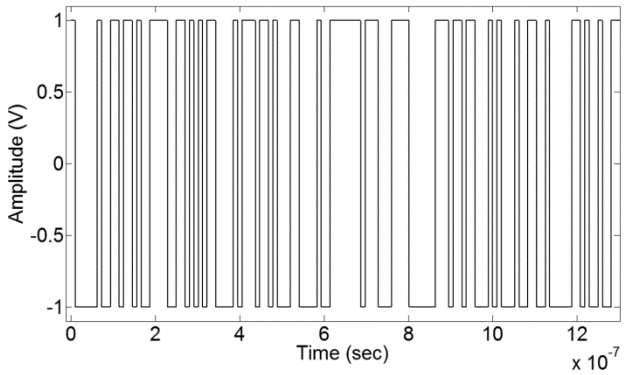


Figure. 3.5. Example of PN code with chip rate 96 X 10^6 chips/sec.

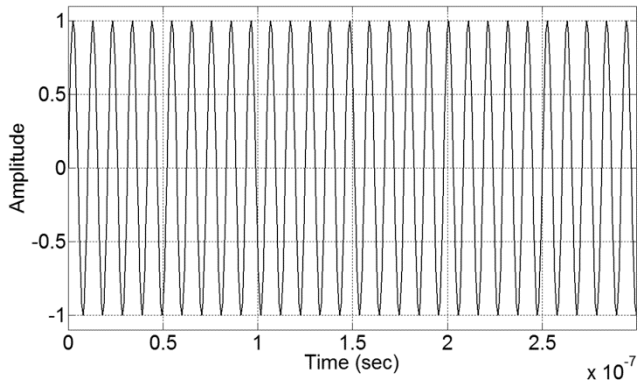


Figure 3.6. Carrier signal of 96 MHz.

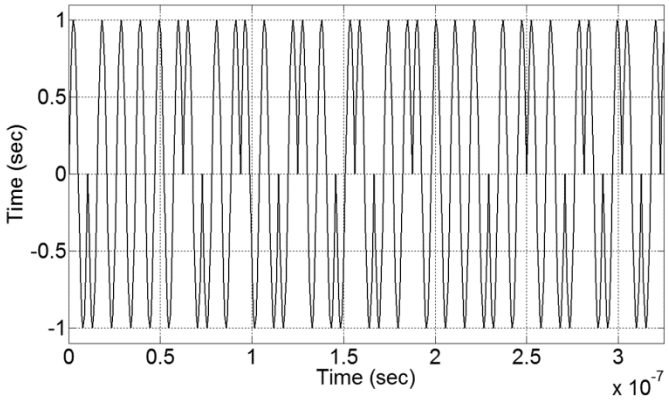


Figure 3.7. Incident signal of SSTDR with carrier/center frequency equal to 96 MHz.

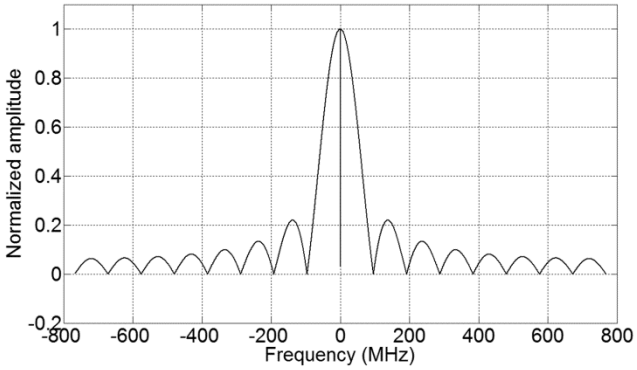


Figure 3.8. FFT of the PN code shown in Figure 3.6.

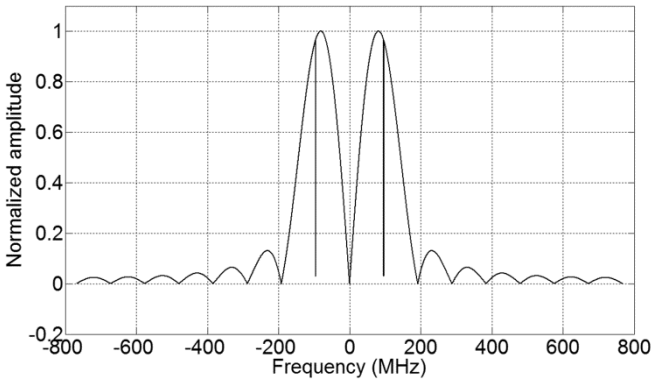


Figure 3.9. FFT of the incident signal generated by SSTDR with center frequency equal to 96 MHz.

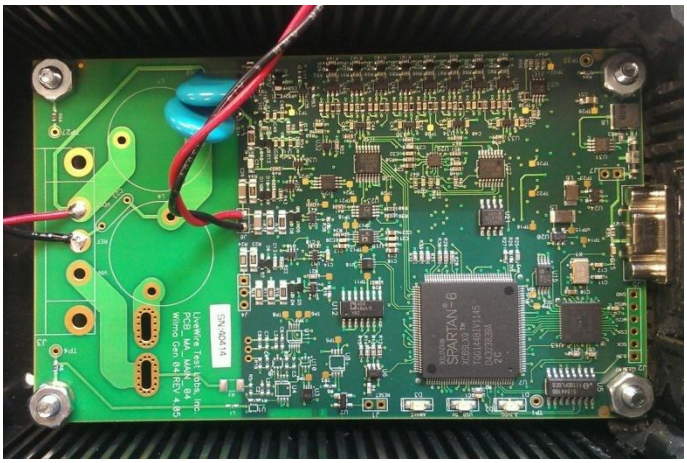
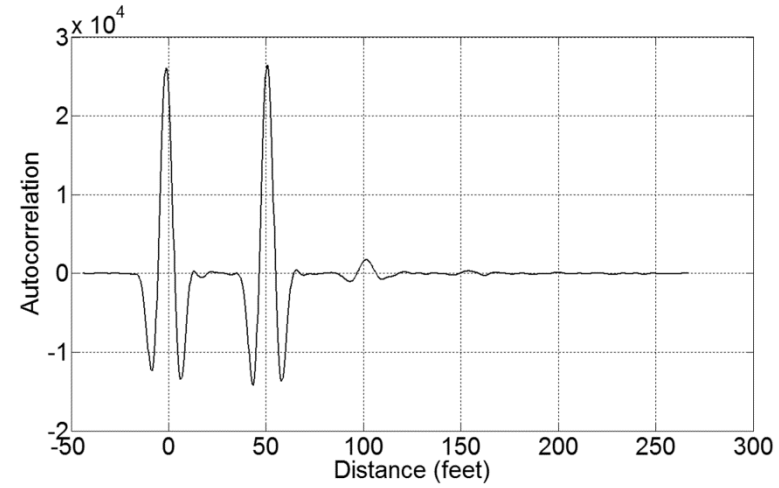
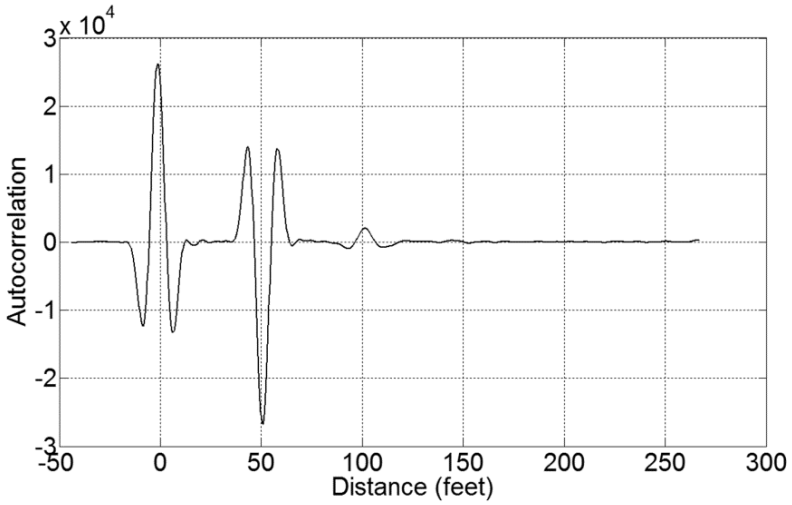


Figure 3.10. WILMA LWG40414 hardware.



(a)



(b)

Figure 3.11. SSTDR response for (a) open and (b) short circuit at the end of ~50 feet RG-6/U coax cable for center frequency equal to 12 MHz.

(a)

(b)

Figure 3.12. Facilities used at DETL of Sandia National Lab to perform the tests: (a) front view, (b) test setup.

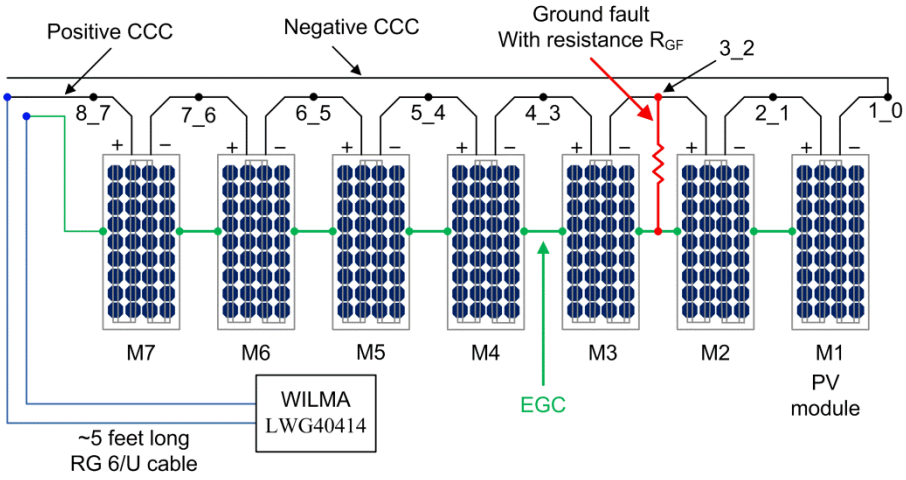


Figure. 3.13. Schematic diagram of the test setup.

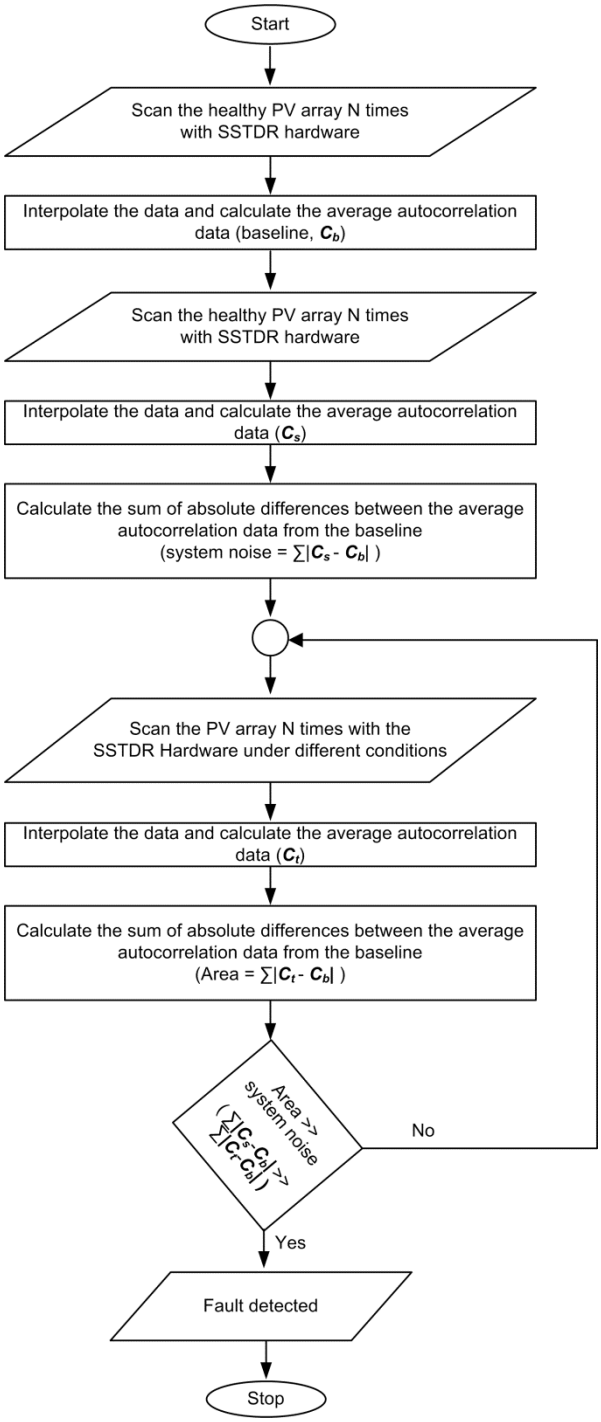


Figure 3.14. Flowchart of the ground fault detection algorithm.

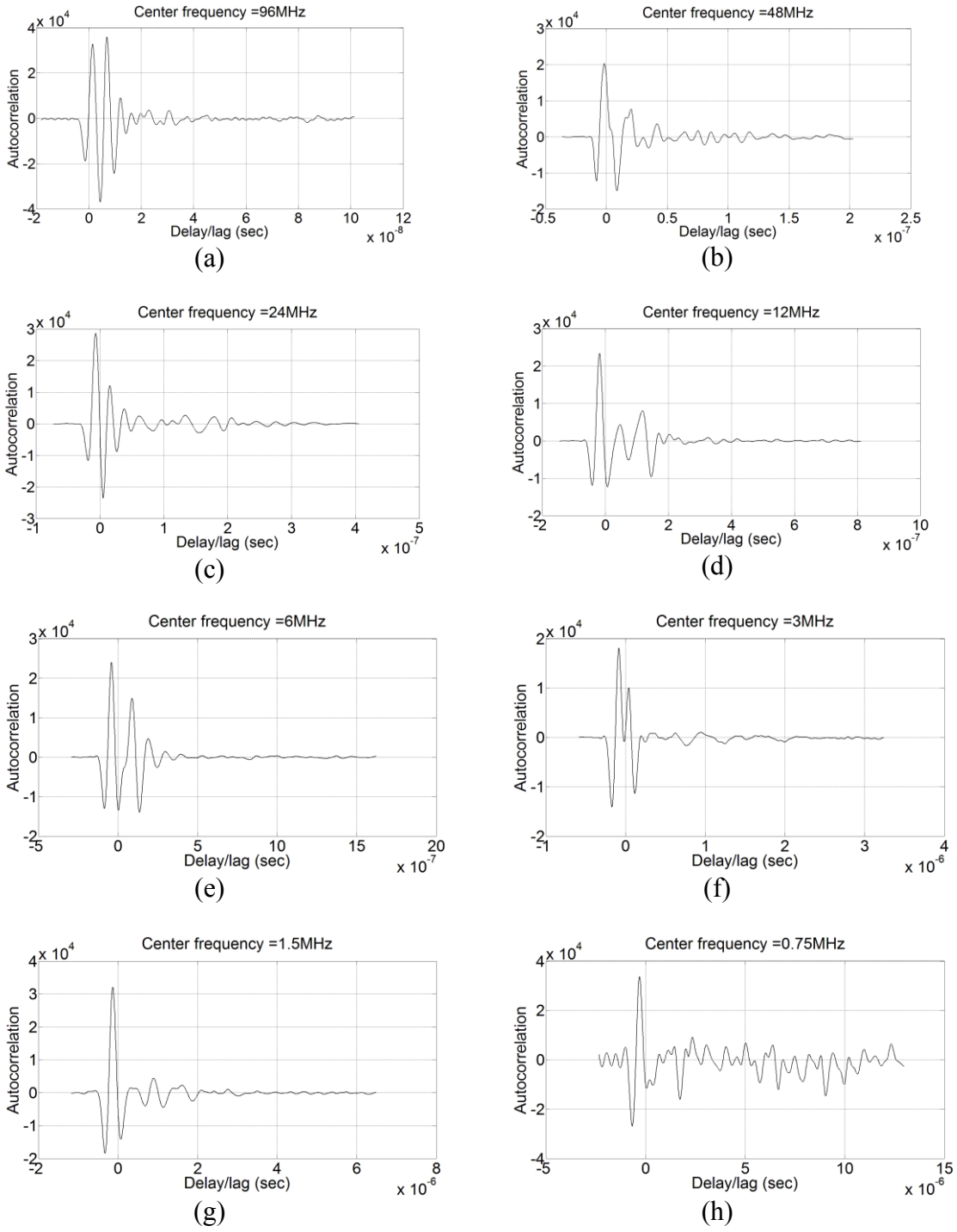
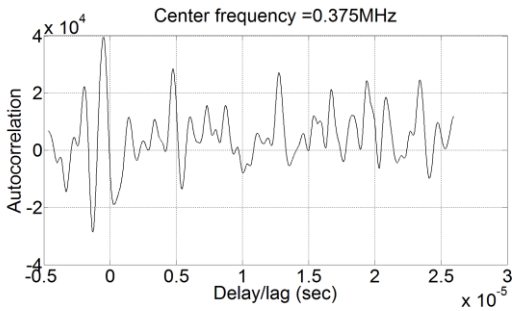


Figure 3.15. Baseline autocorrelation plots for ground fault detection for different center frequencies: (a) 96 MHz, (b) 48 MHz, (c) 24 MHz, (d) 12 MHz, (e) 6 MHz, (f) 3 MHz, (g) 1.5 MHz, (h) 750 kHz, (i) 375 kHz.



(i)

Figure 3.15. Continued

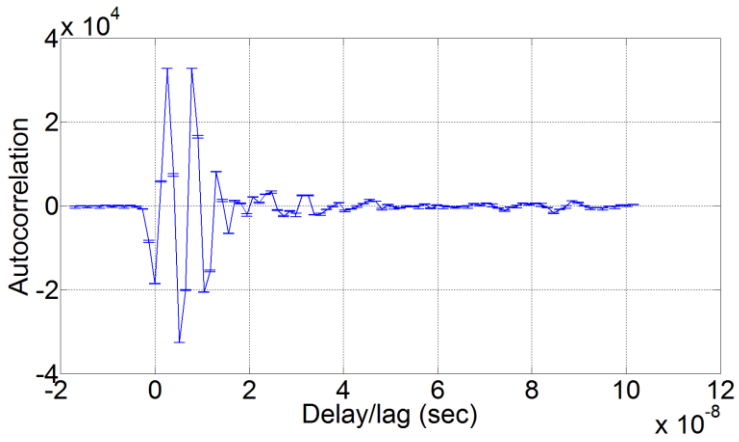
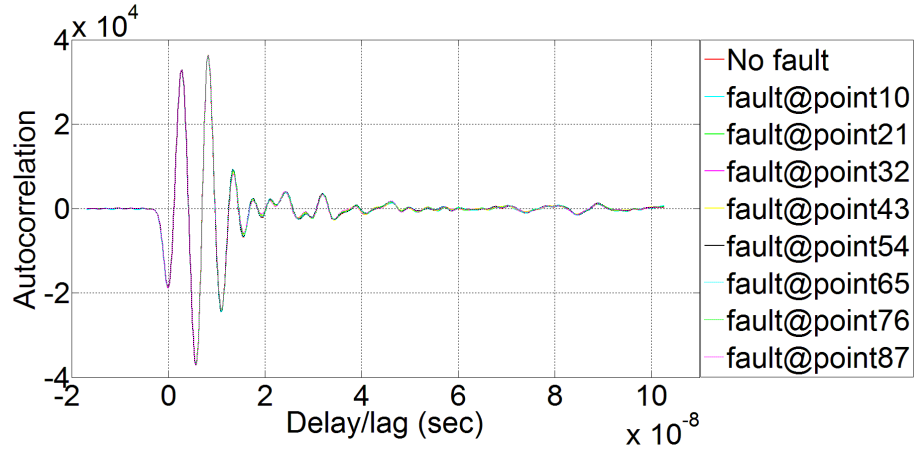
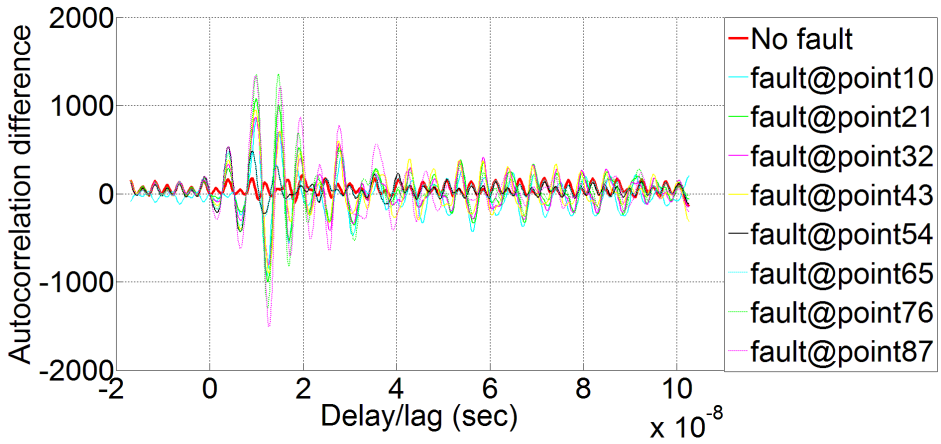


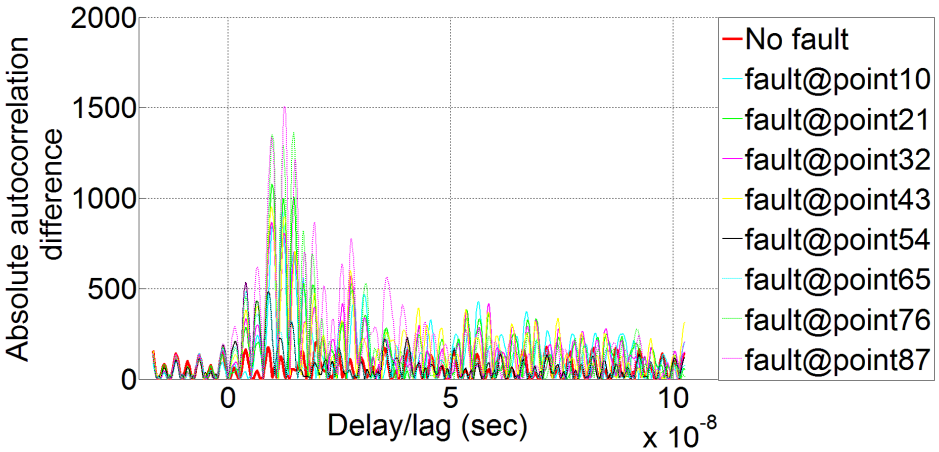
Figure 3.16. Error plot of autocorrelation data for center frequency = 96 MHz.



(a)

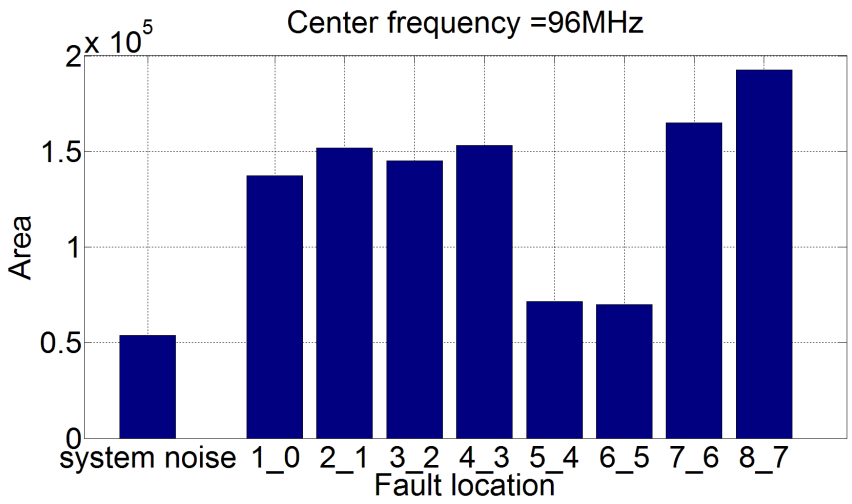


(b)



(c)

Figure. 3.17. Details of the algorithm developed: (a) average autocorrelation plots using the same PV string without any ground fault and ground fault in different locations, (b) difference between average autocorrelation data and the baseline, (c) absolute values of the differences, (d) sum of absolute differences between the average autocorrelation data and the baseline (area).



(d)

Figure. 3.17. Continued

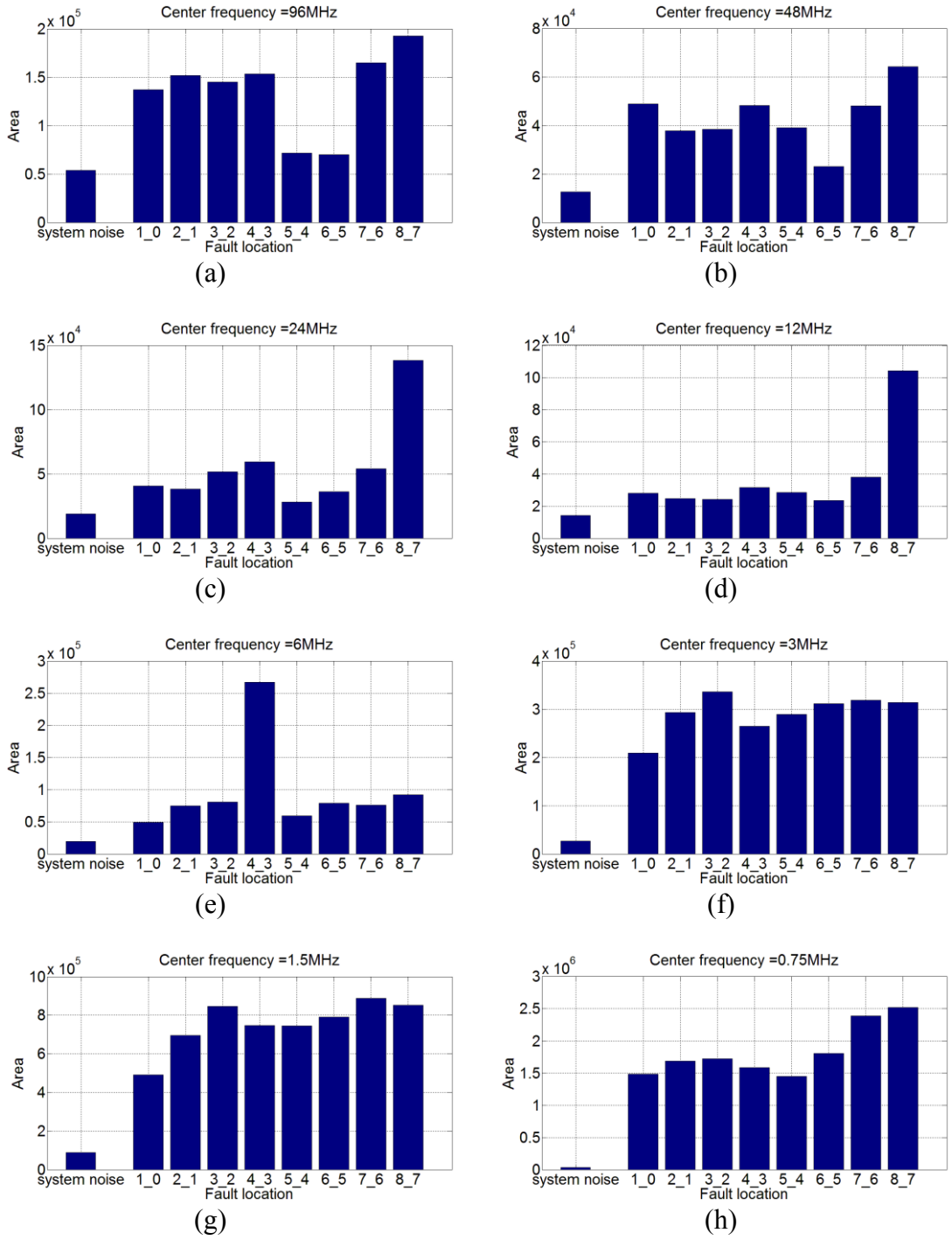
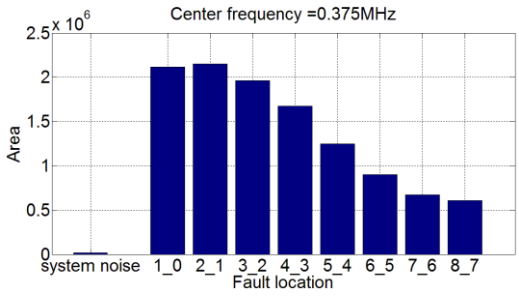


Figure 3.18. Area under absolute autocorrelation difference plots for healthy PV string (system noise) and ground faults at different locations in the PV string using 0.5 Ω resistance with different center frequencies: (a) 96 MHz, (b) 48 MHz, (c) 24 MHz, (d) 12 MHz, (e) 6 MHz, (f) 3 MHz, (g) 1.5 MHz, (h) 750 kHz, (i) 375 kHz.



(i)

Figure 3.18. Continued

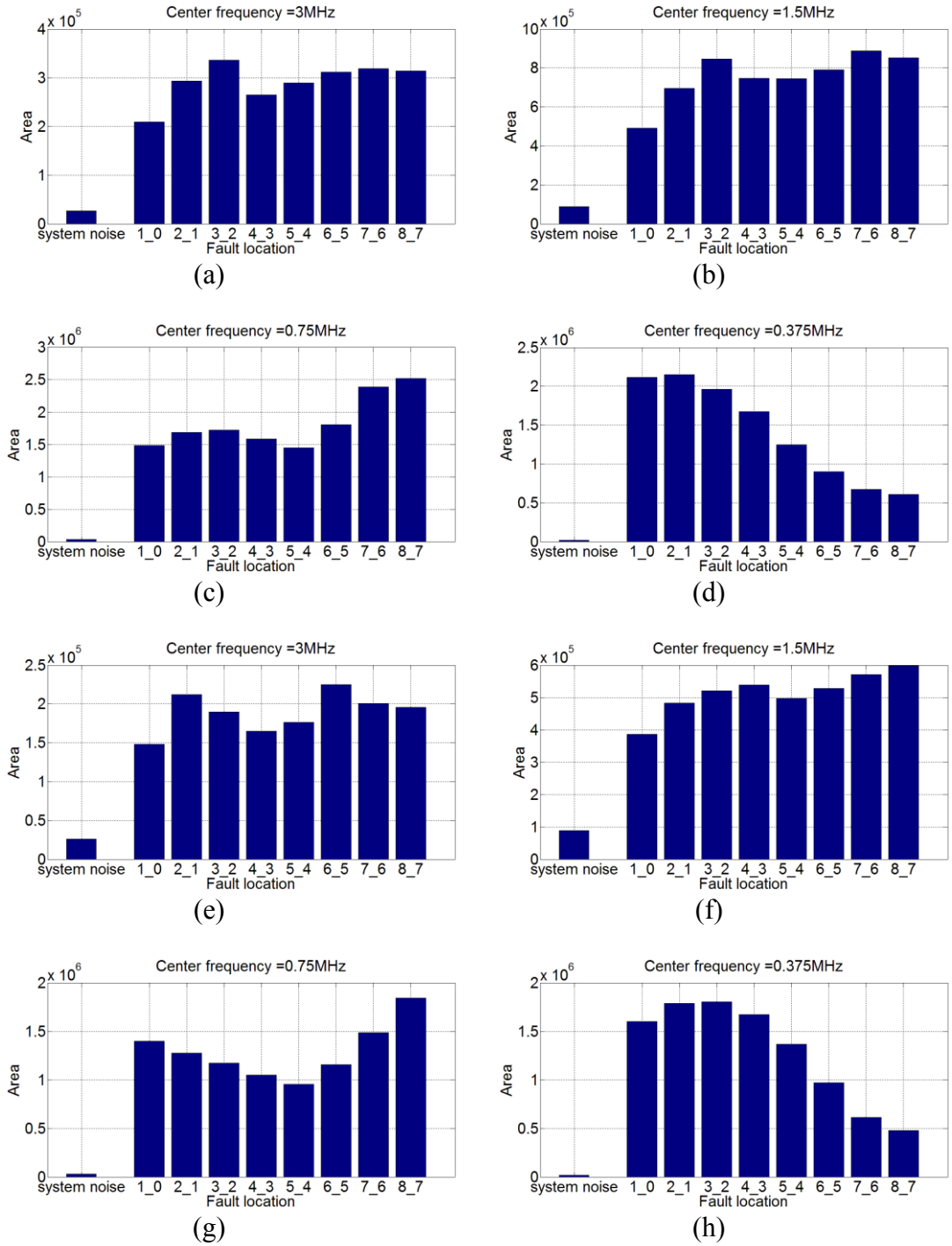


Figure 3.19. Area plots for center frequencies 3 , 1.5, 0.75, 0.375 MHz and fault resistances (a) - (d) 0.5 Ω, (e) - (h) 5 Ω, (i) - (l) 10 Ω.

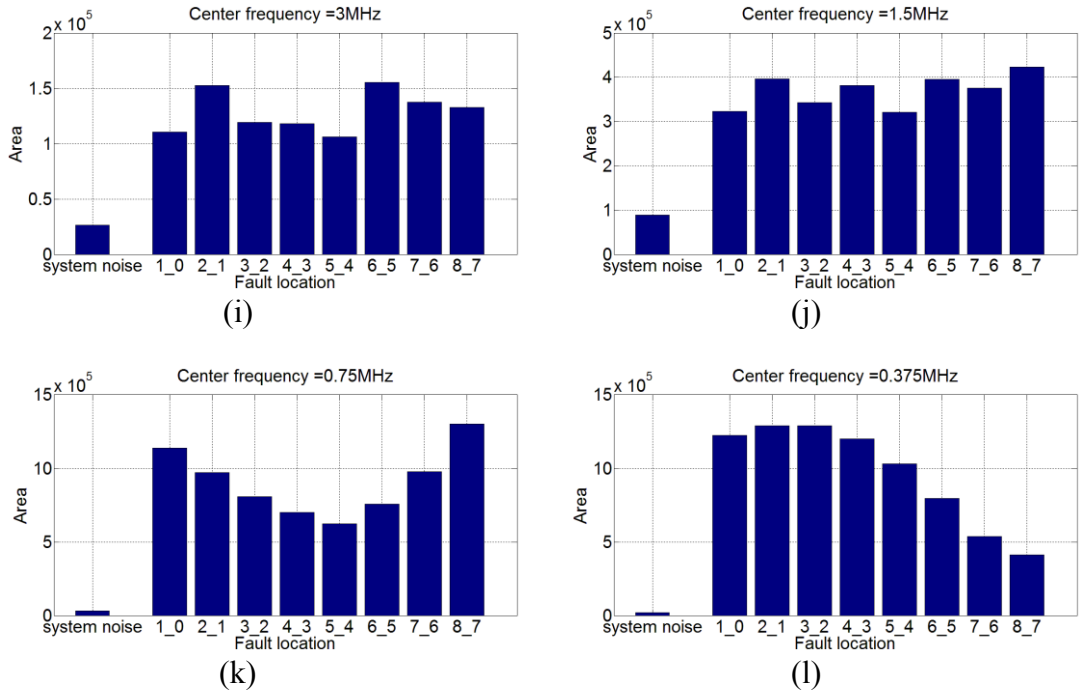


Figure 3.19. Continued.

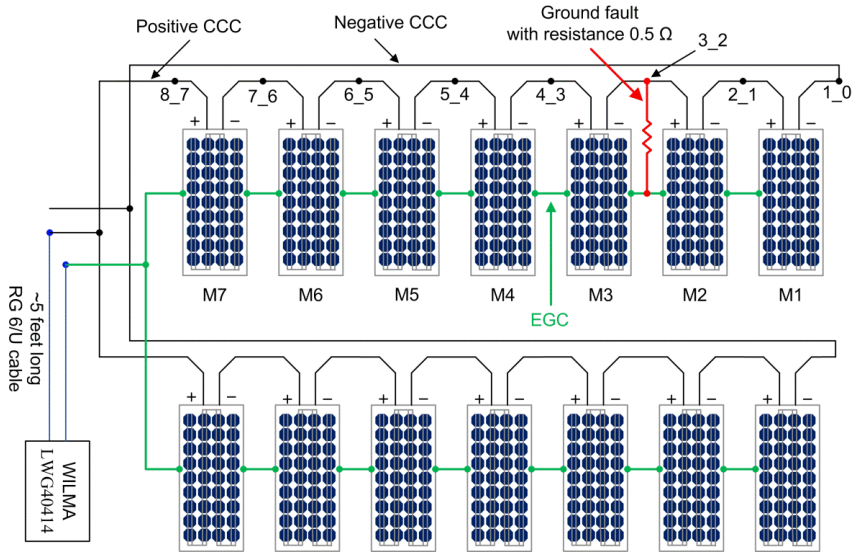


Figure. 3.20. Schematic diagram of the test setup for two parallel strings.

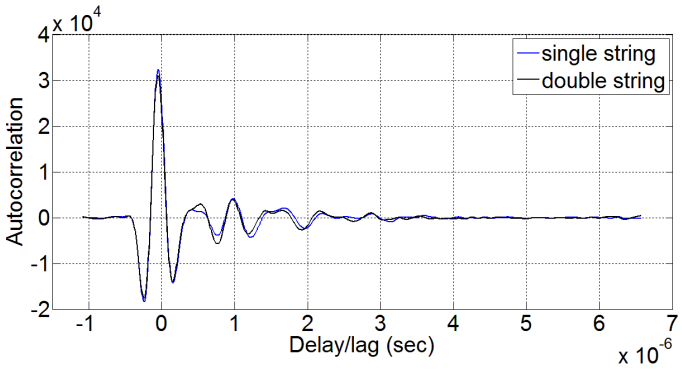


Figure 3.21. Comparison of baseline autocorrelation plots for string and double strings.

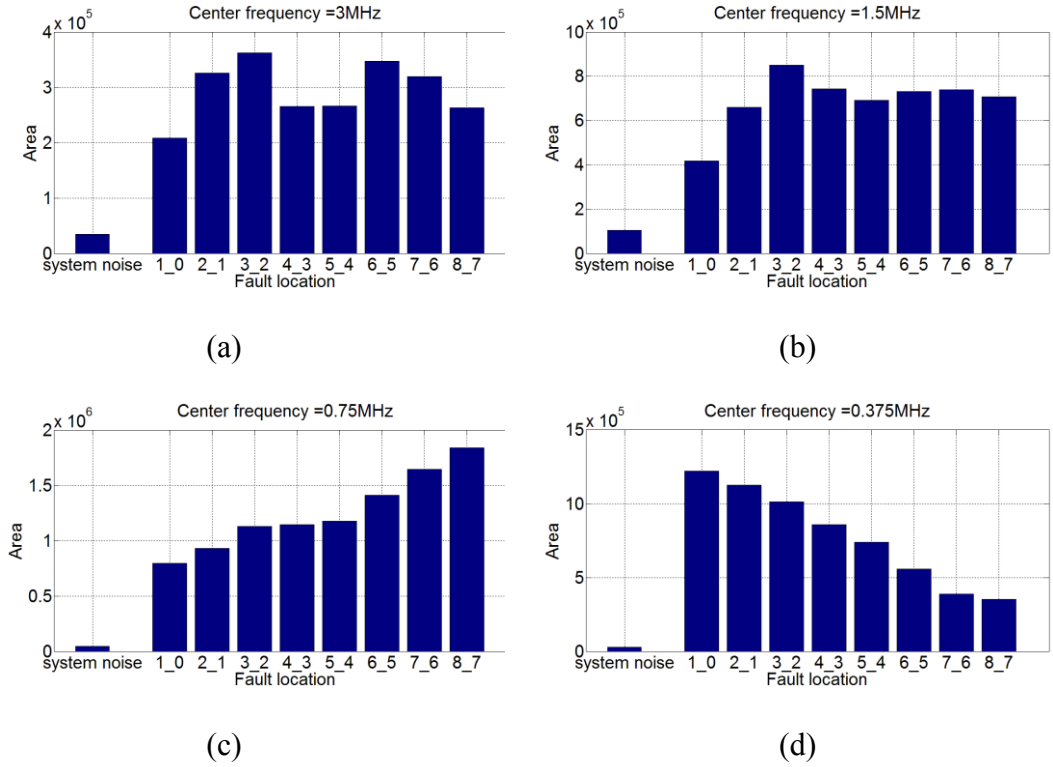


Figure 3.22. Area plot for PV array consists of two parallel strings with and without ground faults: (a) 3 MHz, (b) 1.5 MHz, (c) 750 kHz, (d) 375 kHz.

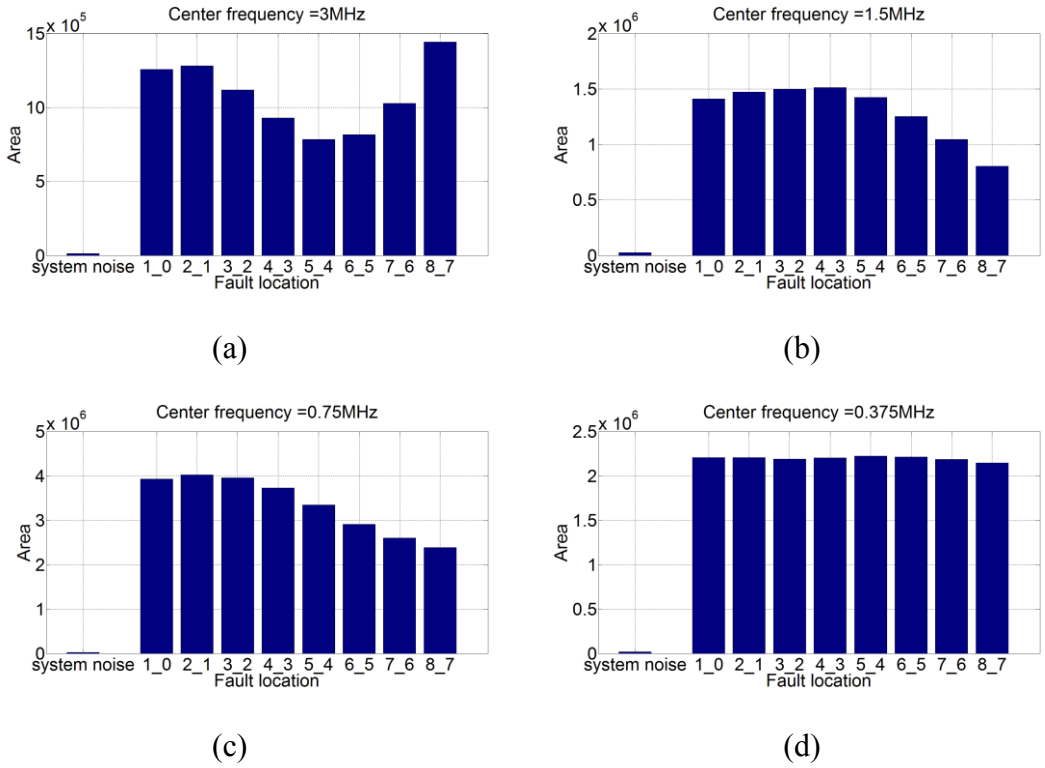


Figure 3.23. Area plot for PV string inside laboratory with and without ground faults: (a) 3 MHz, (b) 1.5 MHz, (c) 750 kHz, (d) 375 kHz.

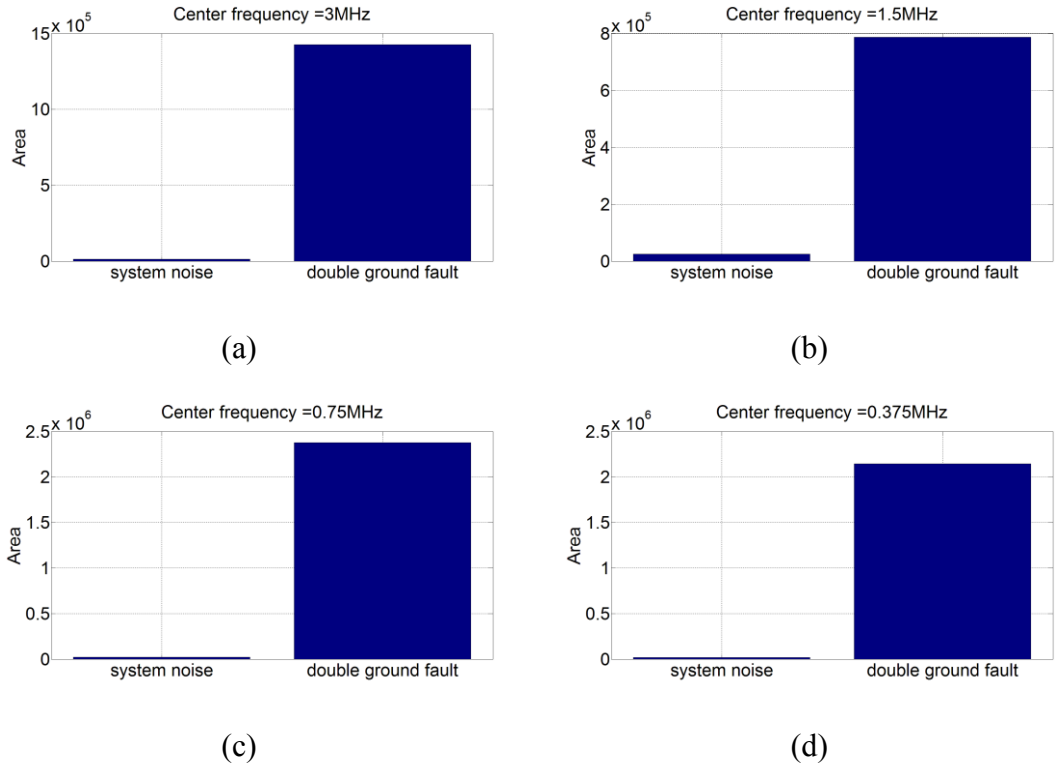


Figure 3.24. Area plot for PV string with and without double ground fault for different center frequencies: (a) 3 MHz, (b) 1.5 MHz, (c) 750 kHz, (d) 375 kHz.

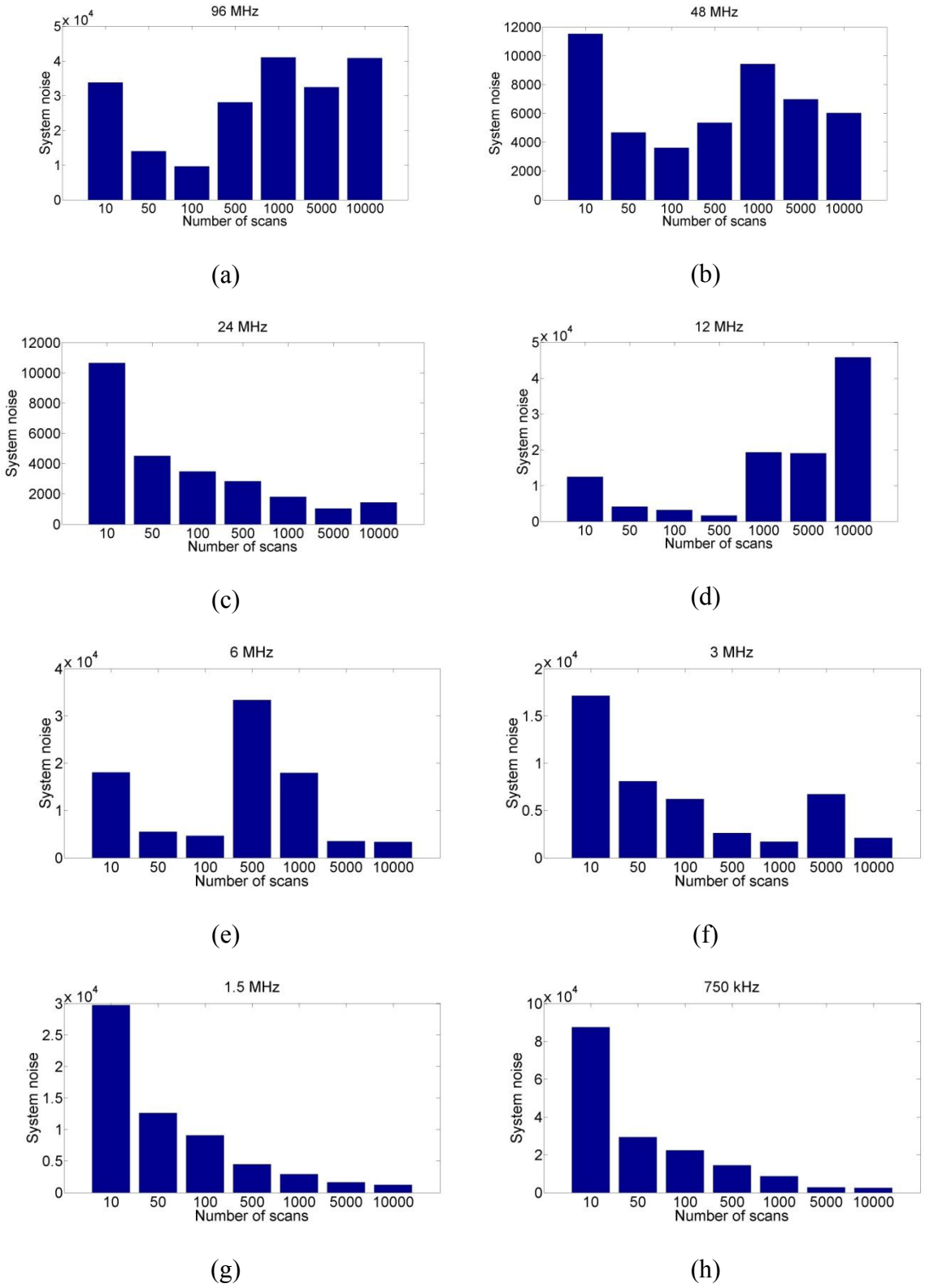
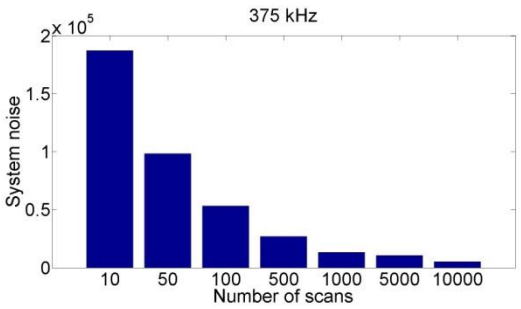


Figure 3.25. Impact of number of scans on the estimation of system noise: (a) 96 MHz, (b) 48 MHz, (c) 24 MHz, (d) 12 MHz, (e) 6 MHz, (f) 3 MHz, (g) 1.5 MHz, (h) 750 kHz, (i) 375 kHz.



(i)

Figure 3.25. Continued

CHAPTER 4

OPEN (ARC) FAULT DETECTION USING SPREAD SPECTRUM TIME DOMAIN REFLECTOMETRY (SSTDR)

An arc fault occurs when a current path is established through the air via arcing due to a discontinuity in the current carrying conductors/junction or to insulation breakdown in adjacent current-carrying conductors. There are numerous interconnections present in a PV array. Due to continuous mechanical and thermal stresses, any of these interconnections may result in a sustained arc. A series arc fault occurs due to discontinuity in any of the current carrying conductors (CCCs) as a result of solder disjoint, cell damage, corrosion of connectors, damage caused by rodents, abrasion from different sources, etc. Parallel arc faults occur between two adjacent CCCs mostly due to insulation breakdown.

Regardless of the origins and types of fault, an arc fault is harmful and potentially dangerous to a PV array since it may initiate a fire and spread to the surrounding areas, especially in presence of flammable substances in close proximity of the PV array [1]-[4]. Since the current through a DC arc does not possess a periodic zero crossing similar to an arc in AC systems, it is much more likely that an arc in a PV system will result in more sustained ignition compared to an AC generation system [5] [6]. The National Electrical

Code® (NEC)-2011 requires a series arc-fault protection device, known as an arc-fault circuit interrupter (AFCI), to the installed rooftop PV arrays with DC operating voltage equal to or higher than 80 V [5] [7].

There are several arc fault detection devices commercially available, and several other arc fault detection techniques have been proposed in the literature. Most of these methods are based on frequency spectrum analysis [8] - [12], and the presence of an arc is confirmed if the amplitude of a specific frequency or a band of frequencies increases beyond a certain threshold value. Arc fault detection using discrete wavelet transformation is presented in [13]. Examples of other methods are use of direction of current flow at the onset of the arc fault [14], numerical analysis of the voltage and current of PV array [15] [16], and others.

The proposed technique has the following advantages and limitations:

(1) SSTDR can be used for both ground fault and arc fault detections.

(2) The method can predict the presence of a potential arc in the PV array.

(3) The method does not require voltage and current information of the PV array.

(4) The method can predict a potential arc in the absence of or at very low solar irradiance.

(5) The proposed technique requires baseline data obtained from the PV array without arc fault to compare with the data obtained from the PV array under test.

4.1 ARC Fault Detection: Intermittent Scan

The WILMA LWG40414 has been used with the positive and negative CCCs of the PV array connected to the SSTDR hardware. The center frequency was fixed at 24 MHz

considering the length of the PV string and the desired distance resolution. There are two major modes of operation in the SSTDR workbench: static and intermittent. The static mode requires external triggering for initializing each scan, and the intermittent scan mode continuously scans the PV array once it is started. The scan speed during intermittent scanning may vary depending on the setup, and it was ~1200 scan/second during this experiment. This means about 1200 autocorrelation plots were generated per second for the PV array under test.

Experiments were performed at the Distributed Energy Technologies Laboratory (DETL) of Sandia National Laboratories (SNL), and a photograph of the arc generator used in this experiment is shown in Figure 4.1. Schematics of the experimental setups for series and parallel arcs are shown in Figure 4.2. Tests were performed using the intermittent test mode to detect the presence of any arc. Each string consists of seven series-connected PV modules, and the specifications of each module can be found in [17]. In the case of series arc generation, two parallel strings were used, as shown in Figure 4.2(a), and the inverter was ON during the series arc generation only, since the inverter may shut down during parallel arc generation due to low voltage at the terminals.

The arc generator was installed at position 1_0 during series arc tests, and the autocorrelation plots generated by the SSTDR hardware are shown in Figure 4.3. It is possible to detect the presence of an arc fault by observing the noise at the autocorrelation plots. A more efficient fault detection algorithm can be developed by calculating area under autocorrelation difference plots using the static operation of the SSTDR hardwire, which is discussed in the next section.

Autocorrelation plots generated by the SSTDR hardware during parallel arc fault by

connecting the arc generator between location 1_0 and 5_4 are shown in Figure 4.4. Data were captured for parallel arc faults at different locations of the PV string e.g., between 8_7, 7_6 etc. and 1_0, and similar results were obtained. It is clear from the plots that any arc (series or parallel) adds significant noise in the autocorrelation plots. It should be noted that whenever a series arc is detected in the system, the inverter is required to be turned OFF to extinguish the arc. However, any parallel arc fault may sustain even after the inverter is turned OFF, and SSTDR can detect the presence of this parallel arc without any baseline subtraction.

4.2 Open Fault Detection

Open fault detection of PV array can be performed during the night or at low irradiance when the inverter is OFF, and the SSTDR hardware needs to work in static mode. SSTDR is based on the concept of reflectometry, and any open fault in a PV string results in a change of reflection coefficient at the location of the open fault. The schematic diagram of the experimental setup is shown in Figure 4.5. A baseline autocorrelation value is obtained from a healthy (without open fault) PV array, and is compared with test data derived from the PV array under the test condition to detect any impedance variation.

An arc fault is confirmed if the area under the absolute autocorrelation difference plot is higher than a predefined threshold obtained from the baseline data. Any open circuit introduced in series-connected PV modules will result in higher reflection at the point of discontinuity, and it results in higher oscillation of the signal generated by the SSTDR hardware. Therefore, the area under the absolute autocorrelation plot increases if there is

any open or short circuit introduced in a healthy PV string. Step by step procedures for generating absolute autocorrelation difference plots for open fault detection are similar to the algorithm described in Chapter 3.

The area under the absolute autocorrelation difference can detect the presence of an open fault at all the locations in the PV string, as shown in the bar graph in Figure 4.6 (a). Therefore, SSTDR can be used for the detection of open faults at different locations with the proposed algorithm, and this method does not require measurements of the current or voltage of the array.

4.3. Impact of Fault Resistance

SSTDR can be used for the detection of any increase in series resistance in a PV array. In order to demonstrate this phenomenon, a series resistance was inserted at various locations of a PV string, as shown in Figure. 4.5. Three different resistors were tested: 0.5 Ω, 5 Ω, and 10 Ω. In all these cases, SSTDR can detect the increased resistance by calculating the area under the absolute autocorrelation difference plot described in the previous section; results are listed in Table 4.1.

Similar tests were repeated with single strings as shown in Figure 4.7. A parallel arc fault creates a low resistance path between two CCCs, and this was emulated using 0.5 Ω, 5 Ω, and 10 Ω resistors, as depicted in Figure 4.8. Any considerable increase in resistance in an existing current path, or decrease in insulating resistance between two CCCs, implies an indication of connection deterioration and can be considered a sign of future arc. The proposed algorithm can confidently detect the presence of such increased resistances (Table 4.1). Therefore, SSTDR can be used for early onsite inspection before

any hazardous event occurs.

4.4. Conclusions

A PV arc fault prediction and detection technique was introduced in this chapter. The proposed techniques can be applied for the detection of both ground and arc faults and do not depend on the solar irradiance or measurement of DC voltage and current of the PV array. Experiments were performed using different arc fault resistances and at different fault locations. The proposed technique can confidently detect the presence of fault resistance irrespective of the value of fault resistances and fault locations inside the array. A detailed analysis of all the test cases along with the potentials and limitations of the proposed arc fault prediction and detection techniques was presented.

4.5. References

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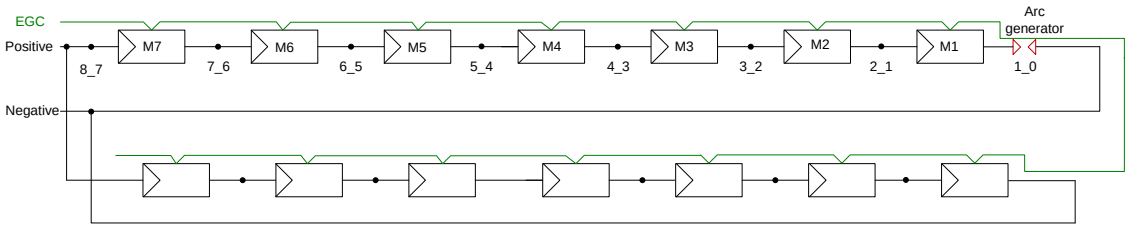
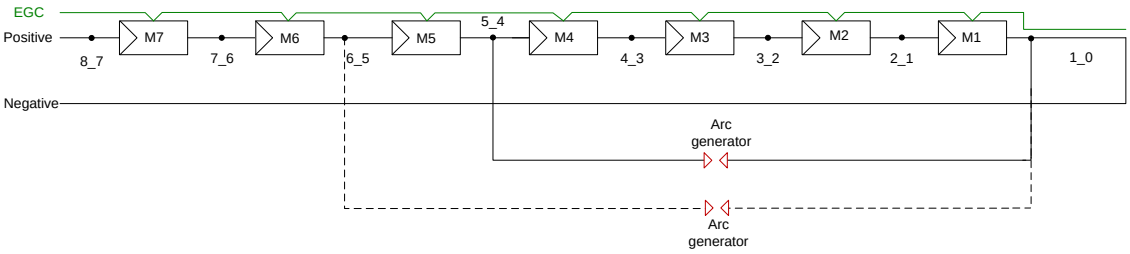
Table 4.1 Area under absolute autocorrelation difference plot for different fault resistances

Fault type	series arc fault and single string			series arc fault and two parallel strings			Parallel arc fault		
Fault resistance =>	10 Ω	5 Ω	0.5 Ω	10 Ω	5 Ω	0.5 Ω	Fault resistance =>	10 Ω	22 Ω
Fault location							Fault location		
System noise	0.0597 e5	0.0597 e5	0.0597 e5	0.0843 e5	0.0843 e5	0.0843 e5	System noise	0.1281 e5	0.1281 e5
1_0	4.7705e5	4.7100e5	4.1193e5	4.1655e5	3.8665e5	2.5320e5	1	1.0086e5	1.0441e5
2_1	0.2140e5	0.1989e5	0.1788e5	0.6458e5	0.6572e5	0.6988e5	2	1.0092e5	0.9742e5
3_2	0.1594e5	0.1700e5	0.1408e5	0.7987e5	0.7908e5	0.8077e5	3	1.0359e5	1.0658e5
4_3	0.1620e5	0.1663e5	0.2154e5	0.8603e5	0.8917e5	0.8642e5	4	0.9790e5	1.0027e5
5_4	0.5639e5	0.5490e5	0.5560e5	0.9097e5	1.0168e5	1.0758e5	5	1.0762e5	1.0081e5
6_5	0.6959e5	0.6561e5	0.6053e5	1.1601e5	1.4942e5	1.2185e5	6	1.3217e5	1.2994e5
7_6	0.8480e5	0.8803e5	0.7853e5	1.5234e5	1.5093e5	1.4558e5	7	2.0328e5	1.9006e5
8_7	8.4074e5	8.6770e5	6.7933e5	4.8628e5	4.9605e5	3.9797e5			

Figure 4.1. Photograph of the arc generator.



(a)



(b)

Figure 4.2. Schematic diagram of (a) the set-up used for series arc fault detection, (b) the set-up used for parallel arc fault detection.

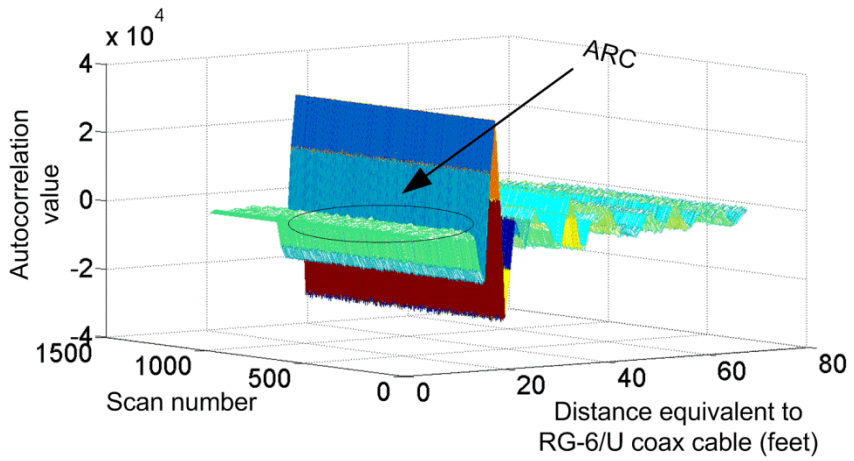


Figure 4.3. Presence of noise in autocorrelation plots during series arc faults.

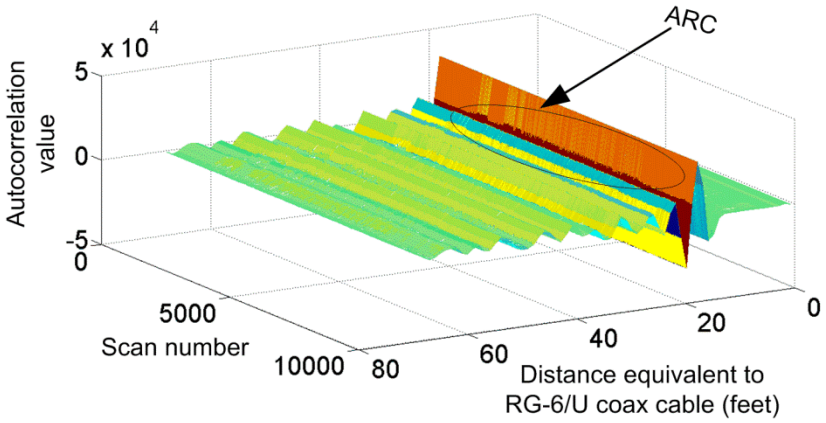


Figure. 4.4. Presence of noise in autocorrelation plots during parallel arc faults.

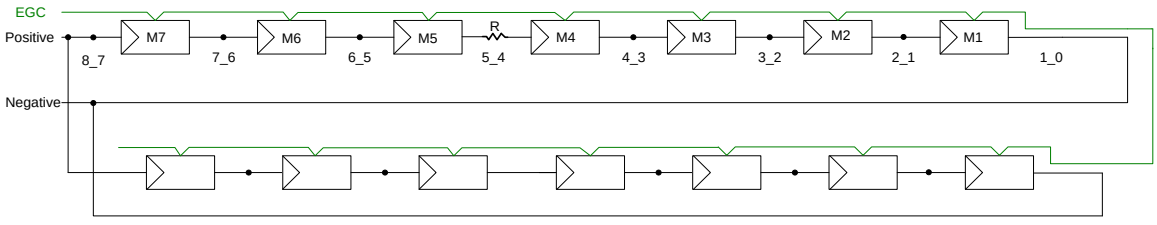


Figure 4.5. Schematic diagram of experimental setup for analyzing the impact of fault resistance in series arc fault with two parallel strings.

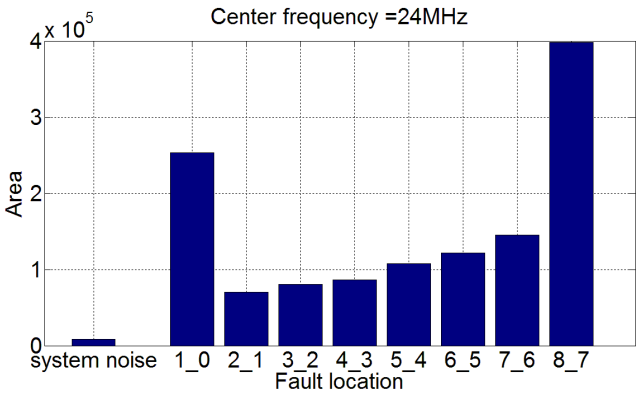


Figure 4.6. Area under absolute autocorrelation difference plot at different fault locations.

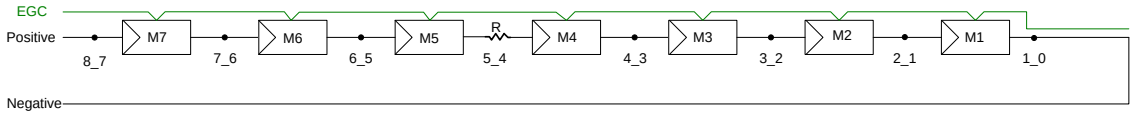


Figure. 4.7. Schematic diagram of experimental setup for analyzing the impact of fault resistance during series arc fault.

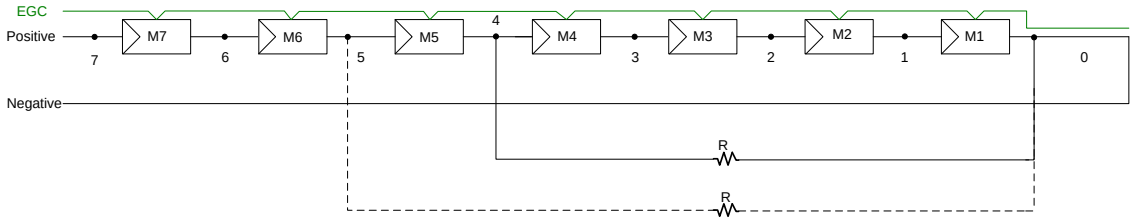


Figure 4.8. Schematic diagram of experimental setup for analyzing impact of fault resistance in parallel arc fault.

CHAPTER 5

RELIABILITY ANALYSIS AND PERFORMANCE DEGRADATION OF A BOOST CONVERTER

The reliability and failure study of individual components used in power converters has been well researched as found in the literature [1]-[4]. The bathtub curve of the failure rate is the most accepted model for any electronic component [5] [6], and is shown in Figure 5.1 (a). The infancy failure of the components is generally linked to poor design, poor installation or misapplication, while the constant failure rate defines the useful lifetime of the component. However, disagreements that argue the bathtub curve are also present in the literature [8] [9]. According to our study, this constant failure rate changes due to any characteristic variation of the components because of the aging involved in the entire power converter. Therefore, a proper maintenance program is required to ensure a safe, efficient and effective operation of a system having power converters.

Reactive maintenance is the most dominant type of maintenance program in industry. In this method, all converters and drives are allowed to run until they fail. Any replacement/repair is performed after the failure occurs. This results in a high downtime cost and may damage other components in the system. Other maintenance schemes attempt to predict the failure of any component and replace/repair the components before

any failure takes place. A relative cost analysis for different pump maintenance schemes is shown in Figure 5.1(b) [5] - [7]. The reliability centered maintenance (RCM) is the most efficient maintenance program although it requires a sophisticated prognostics and diagnosis technique.

Power converters are used in a wide variety of applications, and some applications require very high reliability such as commercial and military aircrafts, space applications etc. [10]. Moreover, the relevant cost of failure of a converter can be higher than 80% of the system cost in some highly integrated products intended to be maintenance free [11]. Therefore, a safe estimation of reliability would be crucial in those cases. However, standards for estimating the failure rates of power converters are still evolving and often refer to the military handbook, MIL-HDBK-217F [2] [10] [12] - [16]. Reliability centered design of power converters requires prior knowledge of failure mode, mechanism and effect analysis (FMMEA) of different components; guidelines for reliability centered design have been provided in [10] [17] - [20].

Most of the power converters are being operated in a closed-loop system in order to maintain expected voltages and currents at different nodes. The control system also protects the converter from any potential overload or short-circuits. Therefore, the operating condition of a power converter is affected by any variation in the components' electrical parameters, input/output loading and ambient conditions. Any variation in one component may simultaneously affect the operating condition and the corresponding thermal stress of all components. This may accelerate the aging process of that component as well as the remaining components of the converter.

It is important to identify the failure prone components and corresponding parameters

that need to be monitored for designing an effective prognostics and health management (PHM) scheme of a power converter. Cheng *et al.* described the process of identifying a potential failure precursor of a component in terms of failure modes, mechanism, and effect analysis (FMMEA) [20]. Yang *et al.* reported a survey on the reliability of power converters and provide statistics on fragile components used in power converters, as shown in Figure 5.2 [11] [23]. Different condition monitoring techniques of power switches are well explained and compared in [24]. In addition, monitoring of different converter electrical characteristics requires in situ measurement of different parameters such as temperature, vibration, voltage, current, magnetic field etc. Pecht *et al.* summarize common sensors and their sensing principles used in PHM for different systems in [19].

It is widely accepted that power switches and capacitors are the most failure-prone components in power converters [11] [17] [21] - [25]. In this regard, variations in the reliability function as a function of MOSFET ON-resistance ($R_{DS(ON)}$), capacitance (C) and ESR of the capacitor in a closed-loop boost converter circuit is analyzed in this chapter.

A simple boost converter with a feedback control loop intended to maintain only the output voltage (no current control) is considered. The voltage conversion ratio (CR) of an ideal boost converter operating in continuous conduction mode (CCM) is related to the duty ratio (d) of the gate signal, as shown in equation (5.1).

$$CR = \frac{V_{out}}{V_{in}} = \frac{1}{1 - d} \tag{5.1}$$

A detailed analysis of this well-known topology can be found in [26] [27]. A schematic diagram of the boost converter is shown in Figure 5.3, and various circuit parameters are listed in Table 5.1. Although different control techniques for switched-mode power converters have been proposed in the literature, a simple proportional-integral (PI) controller is considered here to control the output voltage of the converter using duty ratio control [28] - [34].

It has been shown in [2] that increased MOSFET ON-resistance of an interleaved boost converter operating in an open-loop system increases the reliability of the converter due to a decrease in output voltage across the capacitor. However, this analysis cannot be applied to boost converters operated in closed-loop and, therefore, needs modifications to accommodate the closed-loop operation of the converter. It appears that no analysis has been presented yet to address the reliability degradation of any closed-loop power converter.

5.1. Reliability Estimation of a Boost Converter

Reliability estimation of a boost converter based on MIL-HDBK-217F and considering no variation of characteristic parameters of components is presented in this section.

Considering a constant failure rate ($\lambda_{SYSTEM0}$), the reliability of the system can be calculated as shown in equation (5.2) [1] [3] as follows:

$$R_S(t) = e^{-(\lambda_{SYSTEM} \times t)} \tag{5.2}$$

where, $R_S(t)$ is the probability of having no failure within a duration of t. The mean-time-to-failure (MTTF) can be calculated from the reliability probability function as shown in equation (5.3), and the failure rate of an N-channel MOSFET can be written as in equation (5.4) [1].

$$MTTF = \int_0^\infty R_s(t)dt = \frac{1}{\lambda_{SYSTEM}} \tag{5.3}$$

$$\lambda_{sw} = \lambda_B \pi_T \pi_A \pi_E \pi_Q \tag{5.4}$$

The base failure rate has a constant value of 0.012, and the application factor and quality factor are both equal to 8 for switches rated at 135 W. The environment factor is 9 for equipment installed on wheeled or tracked vehicles [1]. The temperature factor and junction temperature can be calculated using equation (5.5) as follows:

$$\pi_T = temperature \quad factor = exp \quad [-1925 \quad (\frac{1}{T_J + 273} - \quad \frac{1}{298})] \tag{5.5}$$
$$T_J = T_a + (\theta_{JA})P_{sw}$$

with ambient temperature set to 25ºC and an junction to ambient thermal resistance set to 18.0 ºC/W for D2PAK packaging [38].

The total power dissipation (conduction loss + switching loss) of the switching device is P_{sw}. Considering the values stated above, the failure rate of the MOSFET can be calculated using equation (5.6) as follows:

$$\lambda_{sw0} = \lambda_B \pi_T \pi_A \pi_E \pi_Q = 0.012 \times \pi_T \times 8 \times 9.0 \times 8 = 6.912 \times \pi_T \tag{5.6}$$

Considering that the power loss (conduction loss + switching loss) in a switch is 1.3532 watt, the failure rate of the MOSFET is calculated in equation (5.7).

$$\begin{aligned} T_J &= T_a + (\theta_{JA}) P_{sw} = 25 + (18 \times 1.3532) = 49.3576 \\ \pi_T &= exp\ \ [-1925\ \ (\frac{1}{T_J + 273} - \frac{1}{298})] \ \ = 1.6292 \\ \lambda_{SW0} &= 6.912 \times 1.6292 = 11.2610\ failure / million\ \ \ hours \end{aligned} \tag{5.7}$$

Similar analysis can be performed for the inductor, diode and capacitor. For the boost converter under consideration, the failure rate and *MTTF* of the converter is shown in equation (5.8) and (5.9), respectively.

$$\begin{aligned} &\lambda_{SYSTEM\,0} = \lambda_{sw0} + \lambda_{CAP0} + \lambda_{DIODE0} + \lambda_{INDUCTOR0} \\ &= 6.912 \times exp\ \ [-1925\ \ (\frac{1}{T_a + (\theta_{JA}) P_{sw} + 273} - \frac{1}{298}] \\ &+ 120 \times (0.0028 \times [(\frac{S_{CAP}}{0.55})^3 + 1] \times exp(4.09 \times (\frac{T + 273}{358})^{5.9})) \times \\ &0.495621 + 0.011664 \times exp\ \ [-3091\ \ (\frac{1}{T_a + (\theta_{JA}) P_{diode} + 273} - \frac{1}{298})] \\ &+ 0.00108 \times exp\ \ [-\frac{0.11}{8.617\ x\ 10^{-5}} (\frac{1}{T_{HS} + 273} - \frac{1}{298})] \ = \\ &11.2610 + 4.2600 + 0.0283 + 0.9225 = 16.4718\ failure / million\ \ \ hours \end{aligned} \tag{5.8}$$

$$\begin{aligned} MTTF &= \frac{1}{\lambda_{SYSTEM}} = \frac{10^6}{16.4718} hours / \ failure \\ &= 6.930\ years / \ failure \end{aligned} \tag{5.9}$$

5.2. Effect of Variations in Different Component Parameters

The reliability function as a function of any change in MOSFET ON-resistance ($R_{DS(ON)}$), capacitance (C) and ESR of the capacitor (ESR) in a simple boost converter circuit operated in closed loop is analyzed in this section.

5.2.1 Effect of Variation in $R_{DS(ON)}$

Any increase in $R_{DS(ON)}$ of a MOSFET is the dominant precursor of failure for a power MOSFET [21] [22]. Variation in $R_{DS(ON)}$ has been well studied in several papers [4] [35] - [36]. For a fixed gate to source voltage, $R_{DS(ON)}$ of the MOSFET depends on the present value of $R_{DS(ON)}$, temperature, and the power loss in the MOSFET. Any increase in the value of $R_{DS(ON)}$ affects the thermal stress on the switch, increases the junction temperature, changes the operating point of the converter, and decreases the reliability according to equation (5.5). The corresponding effect is shown in Figure 5.4(a).

The failure rate of the MOSFET can be updated, as shown in equation (5.10), as follows:

$$\lambda_{sw}(t) = \lambda_{sw0} \times f_1(\Delta R_{DS}) \tag{5.10}$$

where λ_{sw0} is the failure rate of the MOSFET, considering no change in $R_{DS(ON)}$ over time. The function f1 depends on the change in MOSFET's ON-resistance. In addition, increased thermal stress changes the gate capacitance of the MOSFET, which may cause degraded switching performance, and may result in a higher thermal stress because of the

elevated switching loss. Therefore, reliability of a switch is highly dependent on the prolonged operation of the converter, and cannot be accurately predicted by assuming a constant rate of failure.

5.2.2 Change in Capacitance (*C*) and *ESR*

A state diagram for characteristic variation of a capacitor used in a power converter is shown in Figure 5.4 (b). Both the base failure rate and the capacitance are considered as time-varying in this model. The time-dependent failure rate of the capacitor is shown in equation (5.11).

$$\begin{aligned} \pi_{CV}(t) &= \pi_{CV0} \times \Delta\pi_{CV} = \pi_{CV0} \times f_2(\Delta C) \\ \lambda_b(t) &= \lambda_{b0} \times \Delta\lambda_b = \lambda_{b0} \times \\ & f_3\left(\Delta C, T_a, \Delta T_{power\_loss\_in\_MOSFET\_diode, and\_ESRs}\right) \\ \lambda_{CAP}(t) &= \lambda_{CAP0} \times f_2 \times f_3 = \lambda_{CAP0} \times f_4 \end{aligned} \tag{5.11}$$

π_{CV0}, λ_{b0} are the capacitance factor and base failure rate of the capacitor considering no variation in capacitance over time.

The gradual change/degradation in capacitance depends on the type of capacitor used, and this change is highly dependent on the ambient temperature. Thermal stress is the dominant factor for electrolytic capacitor failure, and power loss in other components (MOSFET, diode, equivalent series resistance of the inductor, ESR of the capacitor itself) may increase the ambient temperature of the capacitor. Output voltage ripple increases with any decrease in capacitance, and increases the voltage stress in the capacitor as well. Higher voltage and ripple current stress play significant roles in increasing the ESR, and

any increase in the ESR results in higher power losses and ambient temperature [38] [39]. *f1*, *f2*, and *f3* are unknown functions that need to be identified.

Consider the boost converter shown in Figure 5.3. The following analysis will consider variations in device parameters and define reliability of the converter as a time varying function. Therefore, the failure rate of the converter (λ_{SYSTEM}) and *MTTF* will no more be a constant, and can be expressed as shown in equation (5.12).

$$\begin{aligned}
&\lambda_{SYSTEM}(t) = \lambda_{sw}(t) + \lambda_{CAP}(t) + \lambda_{DIODE}(t) + \lambda_{INDUCTOR}(t) \\
&MTTF = \int_0^\infty R_s(t)dt = \int_0^\infty e^{-(\lambda_{SYSTEM}(t)\times t)}dt \neq \frac{1}{\lambda_{SYSTEM}(t)} \\
&MTTF = \int_0^\infty e^{-(\lambda_{sw}(t)+\lambda_{CAP}(t)+\lambda_{DIODE}(t)\times t+\lambda_{INDUCTOR}\times t)}dt \\
&= \int_0^\infty e^{-(\lambda_{sw}(t)\times t)} e^{-(\lambda_{CAP}(t)\times t)} e^{-(\lambda_{DIODE}(t)\times t)} e^{-(\lambda_{INDUCTOR}(t)\times t)}dt
\end{aligned} \tag{5.12}$$

This approach works for circuits with a limited number of components, and this is why the reliability analysis of power converters could benefit from this method. An initial reliability of a converter can be estimated based on the measurable quantities such as $R_{DS(ON)}$, *ESR*, *C* and so on. It can be updated periodically by measuring those parameters with a regular interval. Variation of reliability function with the variation in $R_{DS(ON)}$, *C* and *ESR* of the closed-loop boost converter has been presented in section 5.3.

5.3. Sample Reliability Model: A Test Case

The reliability of the closed-loop boost converter for a change in MOSFEST's ON-resistance from 34 mΩ to 44 mΩ, capacitance variation from 5μF to 10μF, and *ESR* variation from 0.1 Ω to 0.18 Ω is presented here.

5.3.1 Change in MOSFET ON-resistance ($R_{DS(ON)}$)

The boost converter shown in Figure 5.3 was simulated in PSIM and the results were imported to MATLAB to calculate the reliability. The feedback controller was implemented using a simple proportional-integrator (PI) controller with gain 0.1 and time-constant set to 0.001. The output capacitor's capacitance and ESR were set to 10 μF and 0.1 Ω, respectively. $R_{DS(ON)}$ of the MOSFET varied from 34 mΩ to 44 mΩ. This variation of ON-resistance is consistent with the experimental data reported in [22] (as a result of accelerated thermal aging of a MOSFET).

The simulation results are shown in Figure. 5.5. Figure 5.5(a) shows that power loss in the MOSFET (sum of the switching and conduction loss) increases with any increase in ON-resistance, and Figure 5.5(b) and (c) show the output voltage and duty cycle of the converter, respectively. The PI controller maintains a fixed output voltage by changing the duty ratio to compensate for any variation in $R_{DS(ON)}$. Failure rate of MOSFET increases with any increase in $R_{DS(ON)}$ due to increased thermal stress, and thereby increases the failure rate of the converter as well. These are shown in Figure 5.5(d) and (e), respectively. It should be noted that increased $R_{DS(ON)}$ in a closed-loop system does not increase the reliability of the converter as opposed to the open-loop system discussed in [2]. MTTF of the converter is reduced by about 2,238 hours (0.2556 years) for the variation in $R_{DS(ON)}$ from 34 mΩ to 44 mΩ, as shown in Figure 5.5(f).

Reporting a real time variation of a power converter may take years of continuous observation in a controlled ambient condition, and this is not feasible. Therefore, a test case is considered here. The results of assuming a rate of increase in $R_{DS(ON)}$ of 2 mΩ/10,000 hours are plotted in Figure 5.6. There is about 3.75% variation in reliability

after 60,000 hours of operation or 2,238 hours variation in *MTTF* if the variation in MOSFET's ON resistance is taken into account.

5.3.2 Change in Capacitance (*C*)

The effect of capacitance variation on the reliability and MTTF of the converter is discussed in this section. The output capacitance of the converter varied from 10 μF to 5 μF in steps of 1μF. $R_{DS(ON)}$ and ESR were set to 34 mΩ and 0.1 Ω, respectively. The failure rate of an aluminum electrolytic capacitor is given in equation (5.13) as follows:

$$\lambda_{CAP0} = \lambda_{b0}\pi_{CV0}\pi_E\pi_Q$$

$$\lambda_{b0} = base\ failure\ rate = 0.0028 \times [(\frac{S_{CAP}}{0.55})^3 + 1]\, exp(4.09(\frac{T+273K}{358K})^{5.9}) \qquad (5.13)$$

$$\pi_{CV0} = capacitance\ \ factor = 0.32(C\mu F)^{0.19}$$

Here, λ_b is the base failure rate and is a function of the voltage ripple across the capacitor. S_{CAP} is the ratio of the operating voltage to the rated voltage, and the rated voltage is defined as the sum of applied average DC voltage and peak A.C. voltage. T is the ambient temperature and π_{CV} is the capacitance factor.

Starting from 10μF, a decreasing capacitance increases the voltage ripple across the capacitor and thereby increases the base failure rate. However, the capacitance factor decreases with any decrease in capacitance. Therefore, the failure rate of the converter decreases with any reduction in capacitance and starts to increase when the base failure rate becomes dominant over the capacitance factor. The failure rate and MTTF of the converter vs. output capacitance is shown in Figure 5.7. The MTTF of the converter is

reduced by about 330 hours for a variation of C from 10 μF to 5 μF. However, any variation in the output capacitance does not have any significant effect on the failure rates of other components of the converter.

5.3.3 Change in *ESR* of the Output Capacitor

The effect of capacitor's *ESR* on the reliability and MTTF of the converter are discussed in this section. The *ESR* of the output capacitor was varied from 0.1 Ω to 0.2 Ω in steps of 0.02 Ω. $R_{DS(ON)}$ and *C* were set to 34 mΩ and 10 μF, respectively. Similar to the $R_{DS(ON)}$ variation, the failure rate of the converter increases with any increase in *ESR*. However, the failure rate of the converter is less sensitive to *ESR* compared to $R_{DS(ON)}$. The failure rate and *MTTF* of the converter vs. ESR is shown in Figure 5.8. The MTTF of the converter is reduced by approximately 140 hours for a variation in ESR ranging from 0.1 Ω to 0.2 Ω.

5.4. Experimental Analysis

This section presents an experimental analysis to study the operation of a boost converter with open loop and closed loop control from the reliability perspective. The off-the-shelf boost converter shown in Figure 5.9 (a) was used for this purpose [40]. The converter has a 1000 μF capacitor connected at the output and a MOSFET (STB75NF75) with $R_{DS(ON)}$ equal to 8.41 mΩ measured at gate voltage and drain current equal to 12 V and 4 A, respectively. The control circuit of the converter was disconnected and an external gate signal was provided on purpose. Three different test cases of the converter's operation were studied, as discussed below.

Test case 1 was operation with the new converter. The boost converter was operated at 100 kHz switching frequency and the input voltage was fixed at 15 V. The output was connected to a DC electronic load with fixed load resistance equal to 6 Ω. The boost converter was operating in continuous conduction mode (CCM), and a screenshot of the output voltage, voltage across the inductor and the gate signal generated by the arbitrary signal generator (GW INSTEK AFG-2125) is shown in Figure 5.9 (b). The output voltage of the converter was 19.02 V with a duty ratio equal to 23.4%. A thermal image of the converter was taken using a FLIR T420 infrared camera, as shown in Figure 5.9 (c). Details of other experimental parameters are listed in Table 5.2.

Test case 2 was operation with MOSFET of higher $R_{DS(ON)}$ and open loop control. In order to demonstrate the impact of a higher $R_{DS(ON)}$, the MOSFET of the converter was replaced by a device, IRFZ34, with $R_{DS(ON)}$ equal to 25.45 mΩ measured at gate voltage and drain current equal to 12 V and 4 A, respectively. The output voltage of the converter dropped to 18.68 V for the same input voltage, duty ratio and output load resistance as described in test case 1. This operation is similar to open loop control where the duty cycle is not changed with the variation of the output voltage of the converter, since the input voltage is fixed to 15V.

Test case 3 was operation with MOSFET of higher $R_{DS(ON)}$ and closed loop control. The duty cycle of the converter was increased to 24.7% to achieve 19.02 V at the output, resembling the operation of the boost converter in closed loop.

During all the test cases, the ambient temperature was fixed at 25 C in the laboratory set-up and no forced cooling was provided. The output voltage ripple was almost75 mV.

Test case 1 was performed to get a reference for open-loop and closed-loop control

with increased $R_{DS(ON)}$. The output voltage drops with increase in $R_{DS(ON)}$ during test case 2. Since the ambient temperature (T) in equation (5.13) was fixed at 25 °C, a decreased voltage stress across the output capacitor will result in a smaller failure rate (λ_{CAP0}). Moreover, the power loss in the MOSFET was decreased due to a smaller input current (4.15 A) compared to 4.28 A in test case 1. The case temperature of the MOSFET was decreased from 44.6 °C to 40.4 °C. Therefore, these observations agree with the fact that increased ON resistance of the MOSFET in an open-loop boost converter will increase the reliability of the entire power converter since the MOSFET and capacitor are the most failure-prone components [2].

It was shown in section 5.3 that increased $R_{DS(ON)}$ resulted in higher duty ratio (d) and, consequently, higher power losses in the MOSFET in closed-loop operation of the converter. Similar results were observed in test case 3 as the duty ratio increased from 23.4% (test case 1) to 24.7% to maintain the output voltage at 19.02 V. The increased duty ratio resulted in higher power losses across the MOSFET and case temperature increased from 44.6 C to 45.3 C. Moreover, there is no change in the failure rate of the output capacitor since the voltage stress and the ambient temperature were same in both test cases 1 and 3. Therefore, it can be concluded that increased RDS(ON) of the MOSFET in a closed-loop boost converter will not increase the reliability of the entire power converter.

5.4. Conclusions and Future Work

An analysis of reliability degradation of a boost converter operated in closed-loop was presented in this chapter. Components used in this converter exhibit parameter variations due to aging of the entire converter. The effect of any variation in MOSFET

ON-resistance ($R_{DS(ON)}$), capacitance (C) and ESR of the output capacitor on the reliability of the power converter have been analyzed, and a summary is presented in Table 5.3. The MTTF of the closed-loop converter decreases with the gradual increase in both $R_{DS(ON)}$ and ESR. However, any variation in $R_{DS(ON)}$ significantly impacts the reliability of the entire converter compared to C and ESR. In addition, the reliability of the converter varies in a more complex manner when it is expressed as a function of the capacitance C. The impact of any variation associated with one component on the remaining components has been studied as well. We believe that this technique could be applied to many other high power converters where predicting the failure rate and the reliability is critical.

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Table 5.1: Circuit parameters of the boost converter

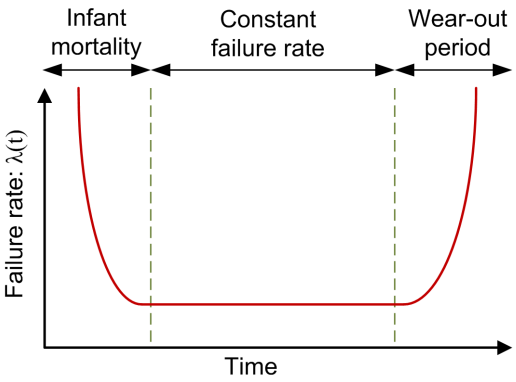
Symbol	Description	Value
V_{in}	Input voltage	40 V
V_{out}	Output voltage	100 V
L	Inductance	1 mH
r_L	Equivalent series resistance (ESR) of the inductor	0.1 Ω
$R_{DS(ON)}$	MOSFET ON resistance	0.034 - 0.044 Ω
r_D	Diode on resistance	0.05 Ω
V_f	Diode forward voltage	0.5 V
C	Output capacitance	5-10 μF
ESR	ESR of the capacitor	0.1-0.18 Ω
R_{out}	Output load resistance	50 Ω
f_{sw}	Switching frequency	10 kHz
P_{rated}	Rated power of the converter	215 W

Table 5.2. Different parameters of the experimental tests with the commercial boost converter

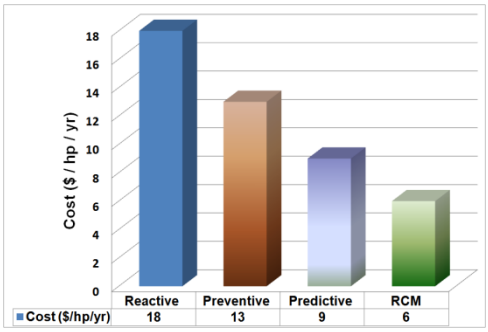
	Test case 1 (reference)	Test case 2 (open loop with increased $R_{DS(ON)}$)	Test case 3 (closed loop with increased $R_{DS(ON)}$)
Input voltage	15 V	15 V	15 V
Input current	4.28 A	4.15 A	4.30 A
Output voltage	19.02 V	18.68 V	19.02 V
Output load resistance	6 Ω	6 Ω	6 Ω
Output power	60.3 W	58.2 W	60.3 W
Output voltage ripple	~ 75 mV	~ 75 mV	~ 75 mV
Duty ratio	23.4 %	23.4 %	24.7%
MOSFET $R_{DS(ON)}$ (at V_{GS}=12V and I_d= 4 A)	8.41 mΩ	25.45 mΩ	25.45 mΩ
MOSFET's case temperature	44.6 °C	40.4 °C	45.3 °C
Ambient temperature	25 °C	25 °C	25 °C
Switching frequency	100 kHz	100 kHz	100 kHz

Table 5.3. System failure rate for characteristics variation of $R_{DS\ (ON)}$, C and ESR

$R_{DS\ (ON)}$ (mΩ) C=10μF, ESR=0.1Ω	System failure rate (λ_{SYSTEM}) (failure/million-hours)	Capacitance (μF) $R_{DS\ (ON)}$ = 34 mΩ ESR=0.1 Ω	System failure rate (λ_{SYSTEM}) (failure/million-hours)	ESR (Ω) C=10 μF, $R_{DS\ (ON)}$ = 34 mΩ	System failure rate (λ_{SYSTEM}) (failure/million-hours)
34	16.5048	10	16.5048	0.10	16.5048
36	16.6294	9	16.4860	0.12	16.5112
38	16.7551	8	16.4789	0.14	16.5177
40	16.8817	7	16.4836	0.16	16.5241
42	17.0094	6	16.5065	0.18	16.5367
44	17.1380	5	16.5690	0.20	16.5432



(a)



(b)

Figure.5.1: Failure rate over time and different maintenance schemes: (a) bathtub curve for component failure rate, (b) cost analysis for different maintenance schemes applied to electric pumps.

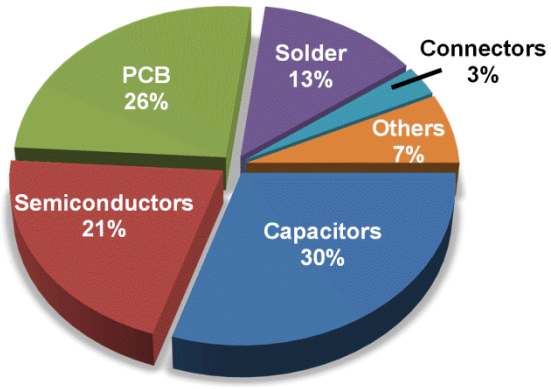


Figure 5.2. Survey of different fragile components responsible for converter failure.

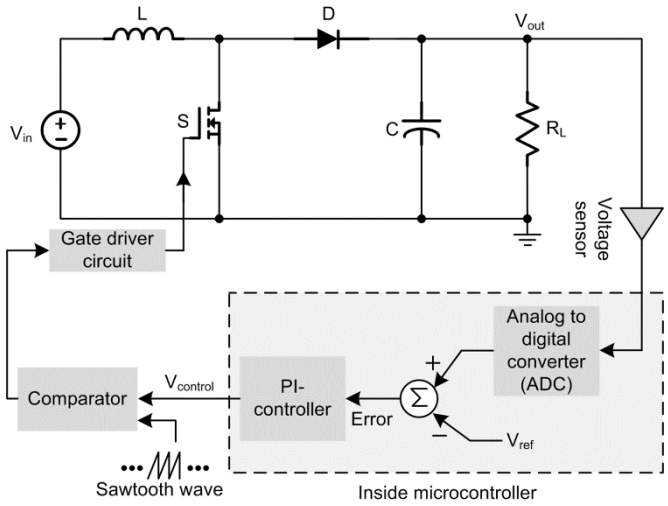
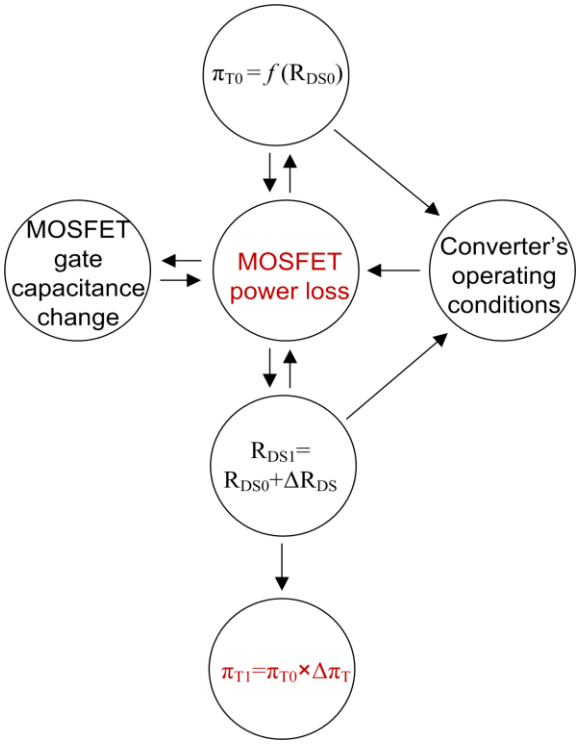
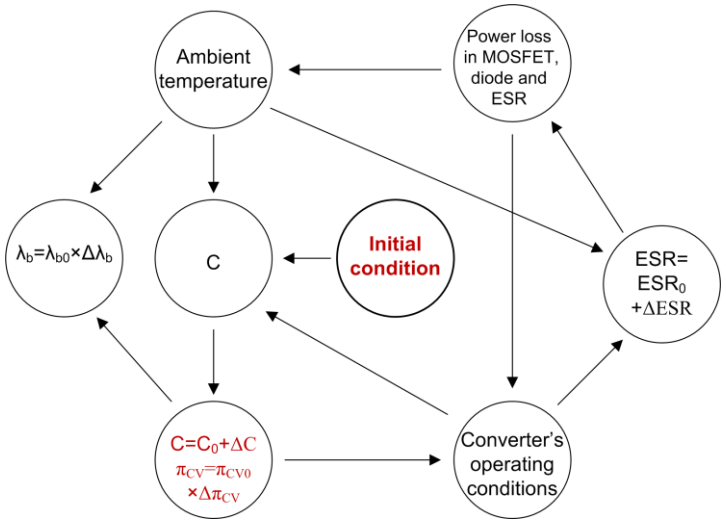


Figure 5.3: Schematic diagram of the closed-loop boost converter.

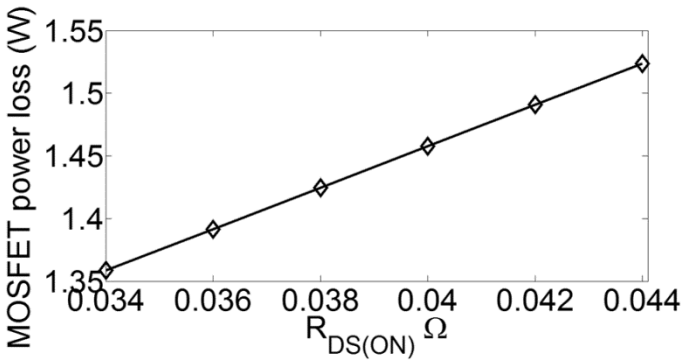


(a)

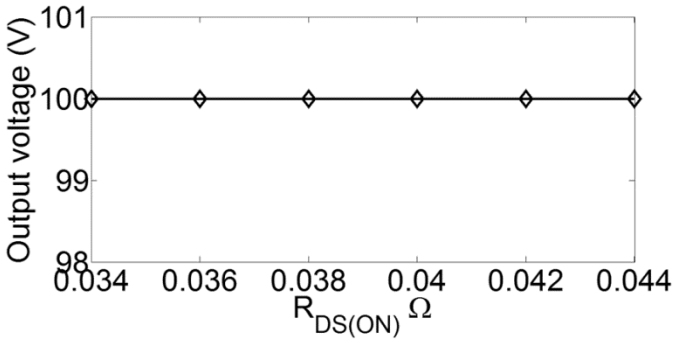


(b)

Figure 5.4. State diagrams describing (a) effect of $R_{DS(ON)}$ variation of the MOSFET on the reliability of the converter, (b) effect of capacitance and (*C*) *ESR* variation on the reliability of the converter.



(a)



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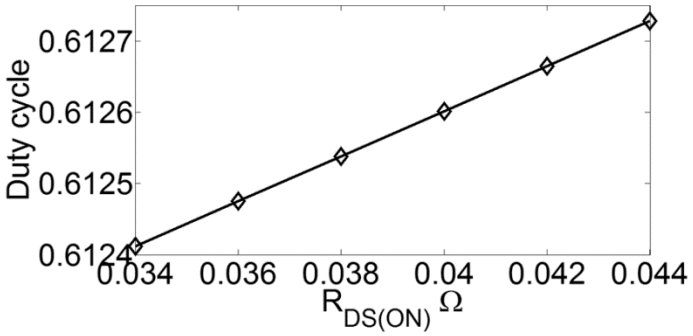
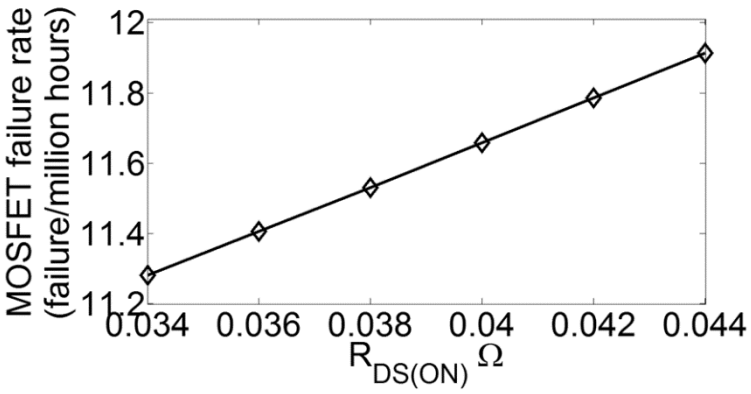


(c)

Figure 5.5. Effect of $R_{DS(ON)}$ variation on the operating condition and reliability of the closed-loop boost converter. (a) Variation in power loss in MOSFET, (b) output voltage, (c) duty cycle variation**,** (d) failure rate of the MOSFET, (e) converter failure rate, and (f) MTTF of the converter as a function of $R_{DS(ON)}$.



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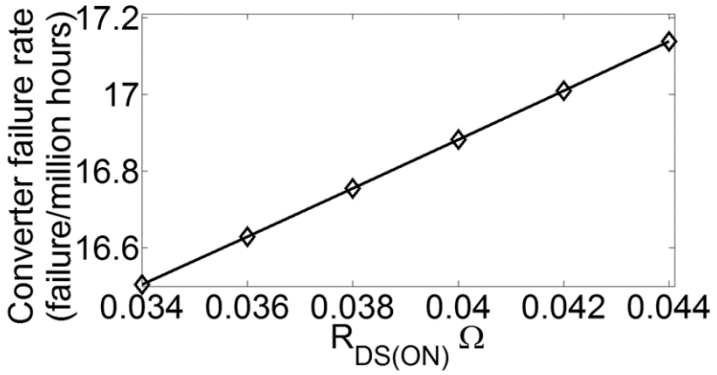

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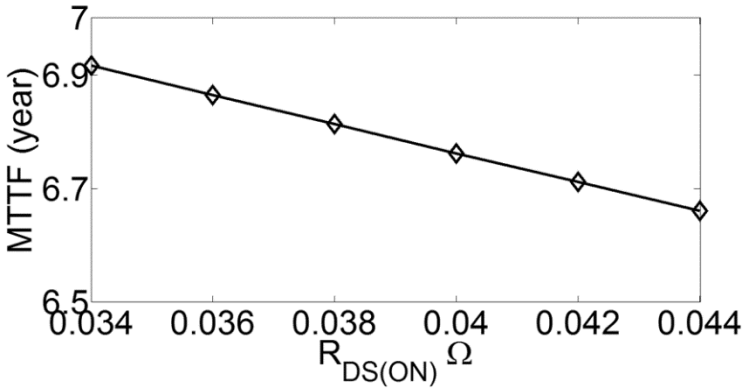
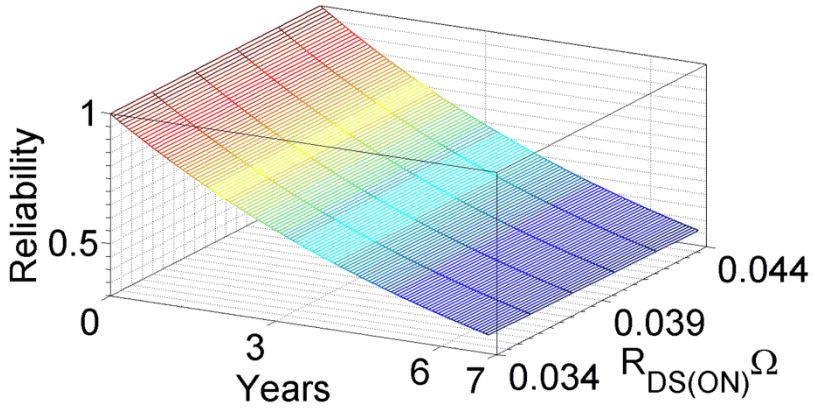
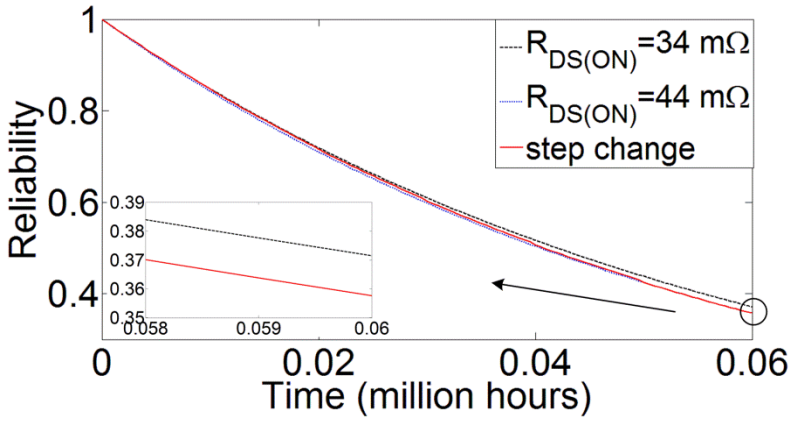


(f)

Figure 5.5. Continued

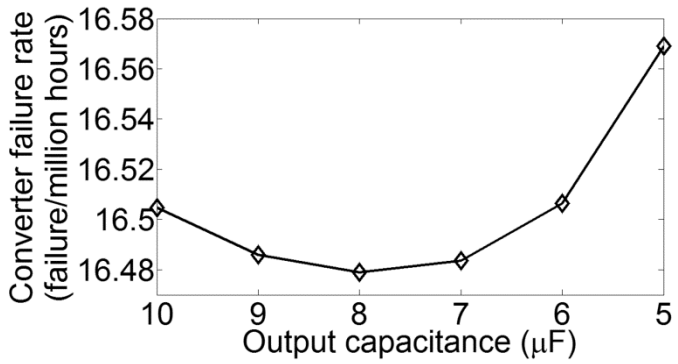


(a)

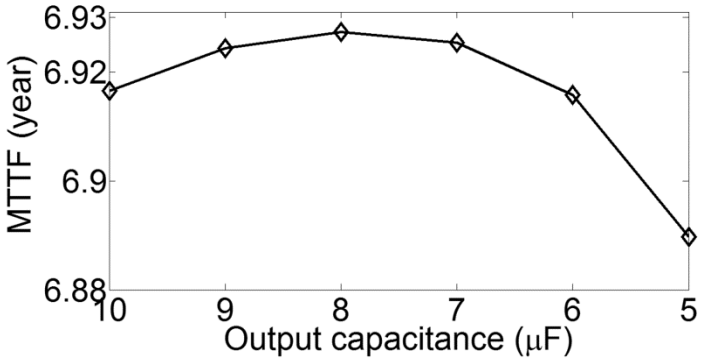


(b)

Figure 5.6. Variation in Reliability over time. (a) Reliability probability function of a closed loop boost converter for the variation in $R_{DS(ON)}$, (b) reliability probability function variation for step change in $R_{DS(ON)}$.

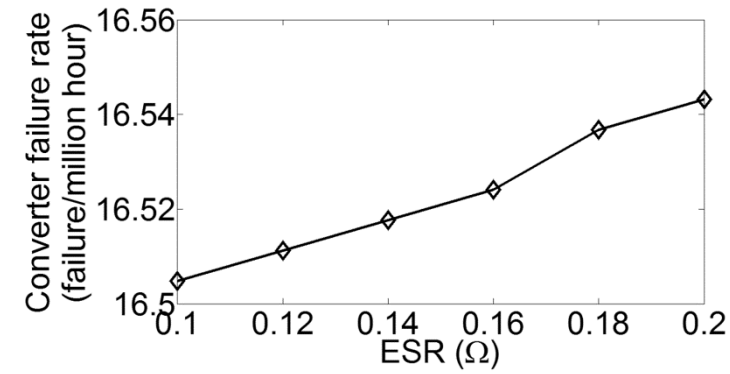


(a)

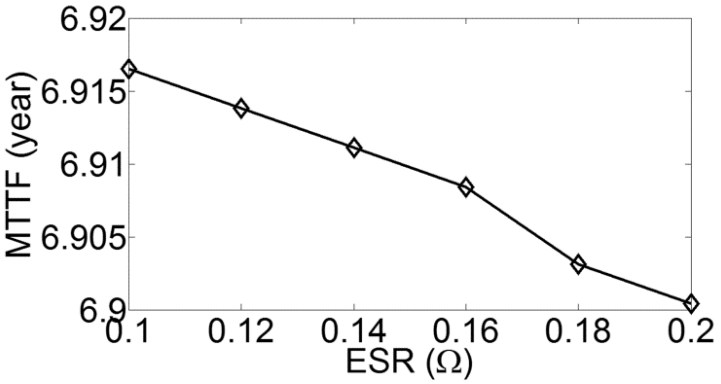


(b)

Figure 5.7. Impact of output capacitance degradation. (a) Converter failure rate vs. output capacitance, *C*, (b) *MTTF* of the converter vs. output capacitance, *C*.

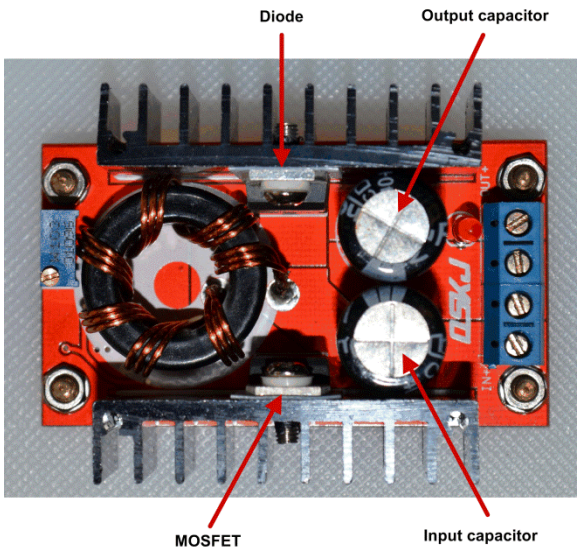


(a)

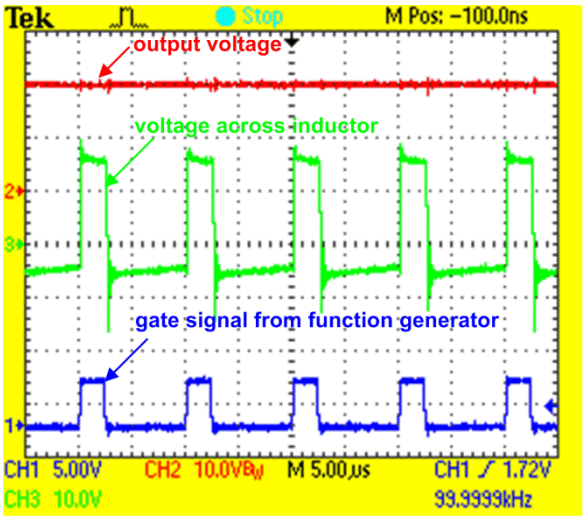


(b)

Figure.5.8. Impact of ESR variation. (a) Converter failure rate vs. *ESR*, *C*, (b) *MTTF* of the converter vs. *ESR*.

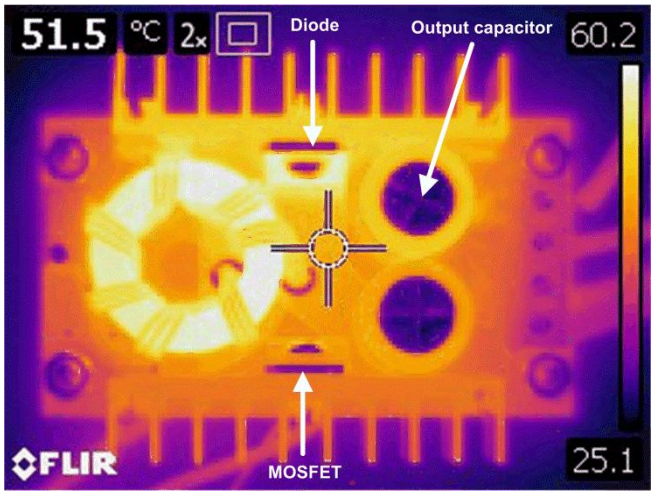


(a)



(b)

Figure 5.9. Experimental results. (a) photograph of the boost converter, (b) oscilloscope capture of gate signal, voltage across the inductor and the output voltage, (c) thermal image of the boost converter.



(c)

Figure 5.9.Continued.

CHAPTER 6

CONCLUSIONS

Fault detection is important to ensure safe operation of PV arrays and an effective fault locating technique can reduce the required maintenance cost and downtime. Among various faults in PV arrays ground faults, line-to-line faults and arc faults are the most common that may result in fire in the PV arrays. With the exponentially increasing rate of global PV installed capacity, an effective fault detection method is becoming more important than ever before.

Power converters are required to extract maximum power from the PV arrays and to interface with the power grid. An efficient maintenance scheme can improve the reliability of power converters and decrease the maintenance cost. Reactive, preventive, predictive and reliability centered maintenance are the most common maintenance (RCM) techniques practiced in industries and RCM is considered to be the most cost effective among all these maintenance techniques.

Electrical characteristics of a PV array are function of solar irradiance, temperature and electrical load. Therefore, fault detection methods based on the electrical characteristics of the PV arrays are challenging and require extensive data collection and postprocessing of these data. A fault detection technique based on spread spectrum time

domain reflectometry (SSTDR) that uses external high frequency signal to detect the presence of fault in the PV array was proposed here.

This method was effectively implemented for ground, line-to-line and arc fault detection in real-time. Impact of different operating conditions such as power rating of PV modules, number of parallel connected PV strings, number of faults, fault resistance, and solar irradiance were investigated in detail. It was found that it is possible to successfully detect the presence of faults under different conditions for carrier frequency of SSTDR signal below 6 MHz.

Reliability estimation of power components is in the evolving phase and in most cases based on the nominal parameters of the power components. These parameters show variation over the time of operation depending on the operating conditions and environmental stresses. Moreover, variation in one component impacts both the operating conditions and environmental stresses due to closed-loop operation. Impact of variation in parameters of different power components was extensively studied here and a reliability estimation method that can account for degradation of different power components in power converters was proposed.