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A new circuit technique for reduced leakage current in Deep Submicron CMOS technologies

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Abstract. Modern CMOS processes in the Deep Submicron regime are restricted to supply voltages below 2 volts and further to account for the transistors' field strength limitations and to reduce the power per logic gate. To maintain the high switching performance, the threshold voltage must be scaled according with the supply voltage. However, this leads to an increased subthreshold current of the transistors in standby mode (V_{GS}=0). Another source of leakage is gate current, which becomes significant for gate oxides of 3nm and below.

We propose a **S**elf-**B**iasing **V**irtual **R**ails (SBVR) – CMOS technique which acts like an adaptive local supply voltage in case of standby mode. Most important sources of leakage currents are reduced by this technique. Moreover, SBVR-CMOS is capable of conserving stored information in sleep mode, which is vital for memory circuits.

Memories are exposed to radiation causing soft errors. This well-known problem becomes even worse in standby mode of typical SRAMs, that have low driving performance to withstand alpha particle hits. In this paper, a 16-transistor SRAM cell is proposed, which combines the advantage of extremely low leakage currents with a very high soft error stability.

1 Introduction

Low leakage currents in standby mode are crucial for battery-driven devices with increasing complexity. The discharge time of a battery is basically given by the power consumption in sleep mode, rather than in actice mode. Since also memories are integrated on a chip, there is the need for a new circuit topology which helps to reduce standby currents, and prevents losses of information.

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2 Leakage current components

The main sources of leakage currents are subthreshold current, DIBL, GIDL, and gate leakage. **D**rain-**I**nduced **B**arrier **L**owering is known as the DIBL effect. High voltages between drain and source reduce the charge being controlled by the gate, thus having the same effect as lowering the threshold voltage (Tsividis, 1987).

Gate-**I**nduced **D**rain **L**eakage (GIDL) is mainly based on band-band tunneling between the overlap region of gate and drain because of deep depletion in this area (Chan, 1987).

Gate leakage current is a tunneling effect between gate and drain, or source, respectively. This leakage current plays a decisive role in deep submicron technologies with very thin gate oxide thicknesses (v. Ardenne et al., 1997).

Due to the limited subthreshold current slope, MOS transistors are prone to high subthreshold currents if threshold voltages become too low. Clever combination of low-vt transistors for high switching speed and high-vt transistors for reduced leakage current can be a good compromise for circuit designs, in order to reach an acceptable overall performance.

3 Rules for the dimensioning of MTCMOS circuits

The MTMCOS technique (Mutoh et al., 1995) is a well-known way to combine high switching speed with low standby current, by using low-vt transistors for the logic part and high-vt transistors for the so-called sleep transistors. However, a practical analytic formula, how to correctly dimension the sleep transistor for a demanded performance, has not been provided.

MTCMOS circuits can be simplified by using only NMOS sleep transistors, see Fig. 1. These transistors will be in their linear mode when the circuit is active. The logic transistors, however, will work in the saturation region. Since the current through logic and sleep transistor must be identical, the

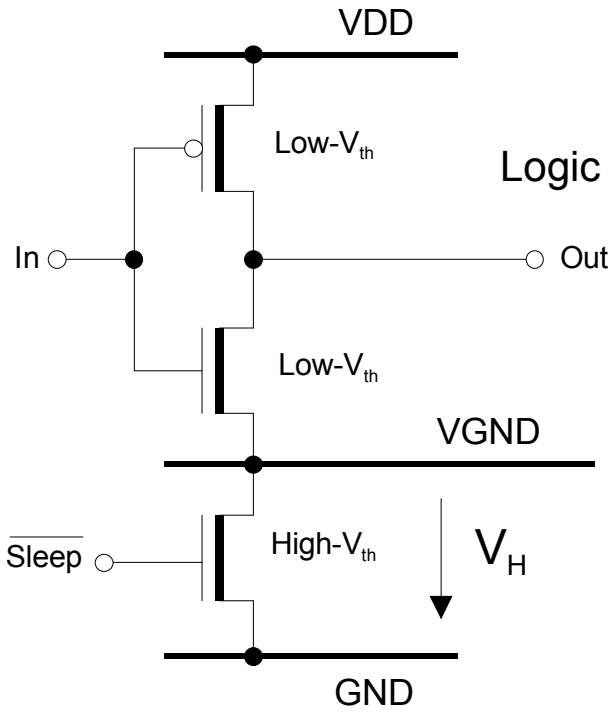

Fig. 1. Modified MTCMOS design with NMOS sleep control transistor.

following equation describes the resulting "ground shift" V_H due to the sleep transistor.

$$V_H = \frac{q-1}{q} \cdot (V_0 - V_{thL}) \,. \tag{1}$$

The factor q (q>1) is used to describe the specified delay time factor of the MTCMOS circuit in comparison to a standard CMOS configuration.

With the help of Eq. (1) it is possible to calculate the necessary width W_H of a sleep transistor, with W_L as the accumulated width of all low-Vt logic transistors that are controlled by the sleep transistor.

$$W_H = 0.625 \cdot \frac{W_L}{2} \cdot \frac{V_0 - V_{thL} - V_H}{(V_0 - V_{thL}) \cdot V_H - \frac{V_H^2}{2}} \,. \tag{2}$$

A drawback of the common MTCMOS technique is the floating of nodes in the circuits. To prevent data from being lost, circuitry must be added to each flipflop.

By use of Eq. (2) the logic part of a 256kBit-SRAM has been redesigned from standard CMOS to MTCMOS. Measured read access times are negligibly longer compared to CMOS (<5%), but leakage current can be reduced by a factor of 30. Figure 2 shows a picture of the fabricated SRAM chip.

Since SRAM cells cannot be realized in MTCMOS due to the loss of information in standby mode this technique is limited to normal logic applications. Besides, other leakage currents than subthreshold current are not well reduced, e.g. DIBL and gate leakage current.

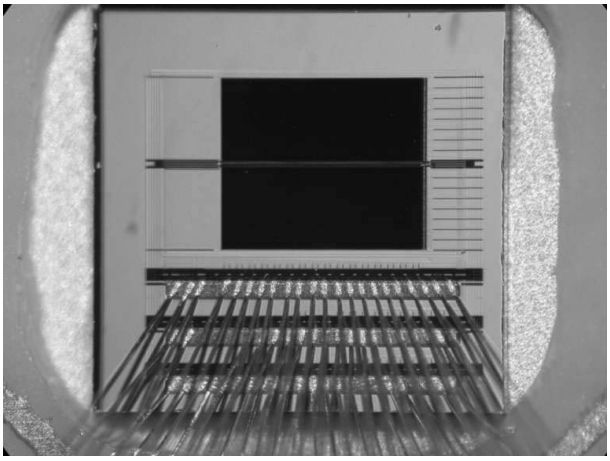

Fig. 2. Picture of MTCMOS SRAM chip.

4 Proposed SBVR-CMOS technique

Lower gate leakage currents in standby mode require lower supply voltages. Based on the MTCMOS technique a new idea of self-biasing virtual rails (SBVR-)CMOS was developed. Sleep transistors connect the circuit's virtual rails with the supply rails providing a low-ohmic path to VDD or GND, respectively. Another MOS transistor connected as a diode is in parallel to the sleep transistor, see Fig. 3. It defines the internal supply voltage in standby mode, thus avoiding floating nodes within the circuit. During active mode, it is shorted by the sleep transistor. The logical potential of each individual node prevails. The influence of the four most dominant leakage current effects, such as sub-vt, DIBL, GIDL, and gate leakage current is reduced enormously. Therefore, this concept is ideal to reduce leakage currents in standby mode.

In modern technologies the decreasing gate oxide thickness results in increased gate leakage currents. A simple model for simulating gate leakage currents was used. It consists of current sources between gate and source as well as between gate and drain, which add the gate leakage currents to the used transistor model (Zoghlami, 2001).

Equation (3) is used to calculate the W/L ratio of the MOS diode for a desired shift on the virtual rail VGND in standby mode. Index 1 refers to the logic transistors and index 2 refers to the MOS diode.

$$\left(\frac{W}{L}\right)_2 = \frac{4 \cdot \left(\frac{W}{L}\right)_1 \cdot \left(\frac{kT}{q}\right)^2 \cdot e^{\frac{q}{2kT} \cdot \left(-V_{Tn1} - \frac{2kT}{q}\right)}}{VGND - V_{Tn2}} \,. \tag{3}$$

This theoretic formula is in good agreement with simulation results. Figure 4 shows simulation results of the gate leakage current reduction in standby mode of an example circuit implemented in SBVR-CMOS for different technologies.

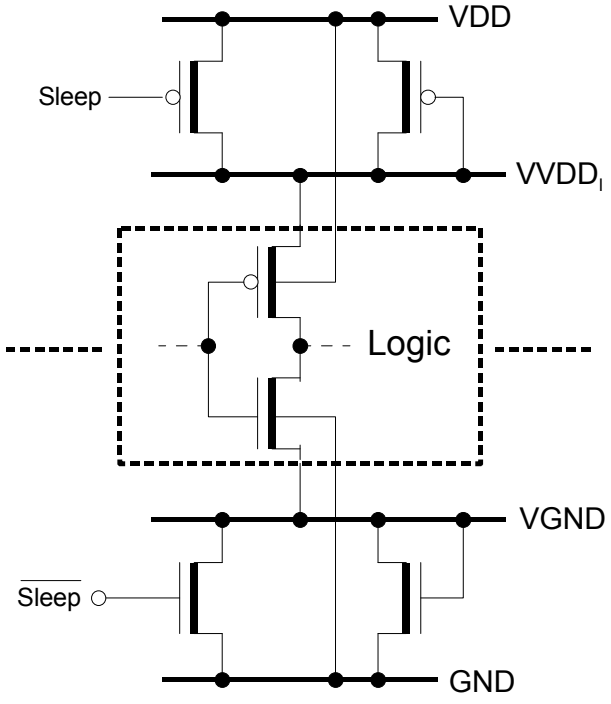

Fig. 3. Principle of "Self-Biasing Virtual Rails" (SBVR).

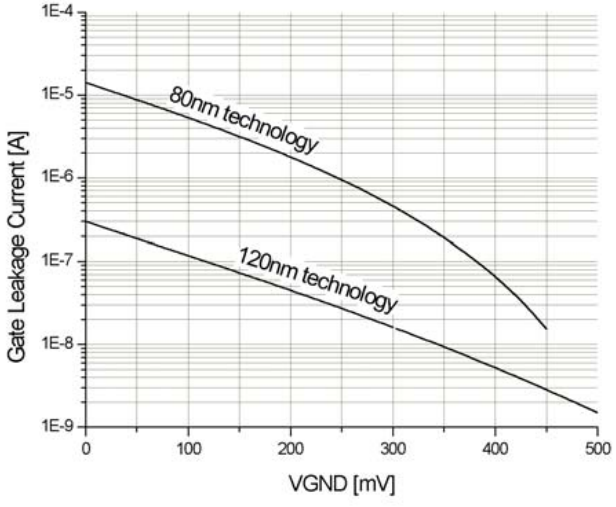

Fig. 4. Gate leakage current in SBVR-CMOS standby mode vs. voltage on VGND.

5 The 16-T SRAM cell

The large number of transistors in SRAM memories contribute to a high total leakage current. On the one hand, the SRAM cell should be fast, and therefore relies on low-vt transistors. On the other hand, leakage current in a big SRAM memory should not exceed a specified range. Special attention must be given to the problem of soft errors (May and Woods, 1978). Low leakage currents and high soft error

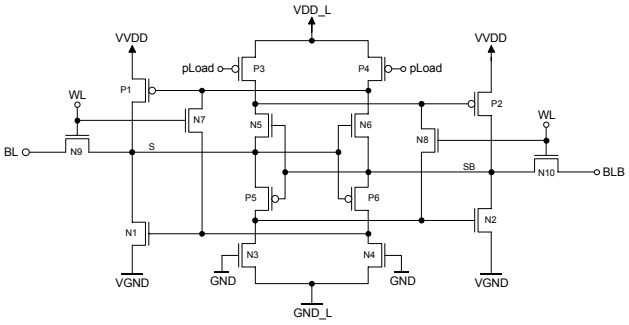

Fig. 5. 16-T SRAM cell with low leakage current and high soft error immunity.

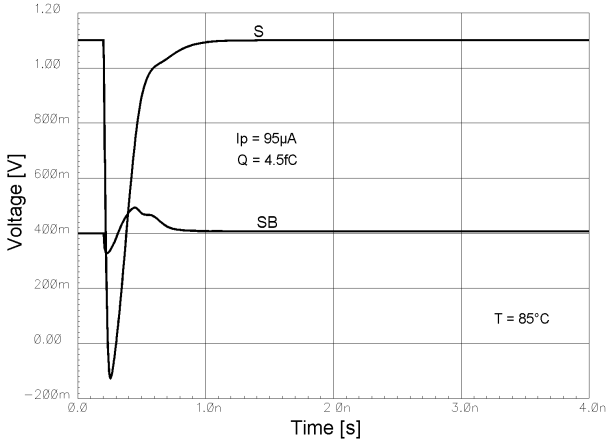

Fig. 6. 16-T SRAM cell showing stable behaviour against alpha particle attack.

stability should be combined in a modified circuit topology.

The novel 16-transistor SRAM cell, as shown in Fig. 5, reduces the total leakage current by a factor of 200 compared to a common 6-transistor cell (Schmitz, 2002). Read and write performance are not affected. Additionally, its soft error stability, i.e. the critical charge injection before an error occurs, is five times higher than that of a standard SRAM cell.

In standby mode, the 16-T SRAM cell uses two sets of virtual rails for power supply and ground. Thus, most transistors can be kept in accumulation which helps to reduce subthreshold current significantly. Since the absolute drain-source voltage of all transistors is lowered, also DIBL, GIDL, and gate leakage currents are minimized. Simulation results show an overall leakage current reduction of a factor 400 for the 16-T cell when going into sleep mode.

Since direct coupling between normally interacting nodes is avoided in sleep mode the soft error stability is largely enhanced. This is demonstrated by the simulated transient response of the critical cell node *S* at an alpha particle hit event in the vicinity of this node, see Fig. 6. The node is able to recover to its original state without affecting the opposite node SB.

6 Conclusion

Large reduction of standby power can be obtained by avoiding some limiting physical effects on transistor level. Conventional CMOS design flows can be used as the basis for the suggested extensions of the proposed technique. The four dominant leakage current phenomena are effectively reduced by SBVR-CMOS. The proposed 16-T cell is an effective replacement for the 6-T SRAM, if both low standby currents and a high soft error stability is required. In radiation-hard applications this cell might be a good choice, despite of the larger cell area.

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