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# COMPARISON OF GAMMA RAY EFFECTS ON EPROMs AND E<sup>2</sup>PROMs

by

# Miloš VUJISIĆ<sup>1</sup>, Koviljka STANKOVIĆ<sup>2</sup>, and Aleksandra VASIĆ<sup>3</sup>

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This paper compares the reliability of standard commercial Erasable Programmable Read Only Memory (EPROM) and Electrically Erasable Programmable Read Only Memory (E<sup>2</sup>PROM) components exposed to gamma rays. The results obtained for CMOS-based EPROM (NM27C010) and E<sup>2</sup>PROM (NM93CS46) components provide the evidence that EPROMs have greater radiation hardness than E<sup>2</sup>PROMs. Moreover, the changes in EPROMs are reversible, and after erasure and reprogramming all EPROM components restore their functionality. On the other hand, changes in E<sup>2</sup>PROMs are irreversible. The obtained results are analyzed and interpreted on the basis of gamma ray interaction with the CMOS structure.

Key words: EPROM,  $E^2$ PROM, gamma rays, radiation hardness

## **INTRODUCTION**

The major advantages of Electrically Erasable Programmable Read Only Memory (EEPROM or  $E^2$ PROM) over Erasable Programmable Read Only Memory (EPROM) components are the elimination of UV erase equipment and the much faster in-the-system erasing process (measured in milliseconds compared with minutes for high-density EPROM). On the other hand, the major drawback of  $E^2$ PROMs is the large size of their two transistor memory cells compared to single transistor cells of EPROMs [1]. Following the shift from NMOS to CMOS transistor technology, present day programmable non-volatile

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<sup>1</sup> Faculty of Electrical Engineering, University of Belgrade

73, Bulevar Kralja Aleksandra, 11000 Belgrade, Serbia <sup>2</sup> Radiation and Environmental Protection Department,

- Vinča Institute of Nuclear Sciences P. O. Box 522, 11001 Belgrade, Serbia <sup>3</sup> Faculty of Mechanical Engineering,
- University of Belgrade 16, Kraljice Marije, 11120 Belgrade, Serbia

E-mail address of corresponding author: vujsa@ikomline.net (M. Vujisić)

memories are mostly CMOS-based, as it is the case with both memory models investigated in this paper.

The influence of neutron displacement damage, primarily reflected in the change of the minority carrier lifetime, is negligible in all MOS (Metal-Oxide Semiconductor) structures, since their operation is not significantly affected by the minority carrier lifetime. Other types of neutron damage, including secondary ionization and carrier removal, are minimal and indirect [2, 3].

CMOS structure is naturally immune to alpha radiation, due to the shallow well. The formation of electron-hole pairs by an alpha particle will primarily take place in the substrate below the well. The well forms an electrical barrier to the carriers, preventing them from reaching the gate and influencing transistor operation. Any carriers generated in the well itself recombine quickly or get lost in the flow of majority carriers [1, 4].

Gamma radiation may cause significant damage to programmable memories, deteriorating properties of the oxide layer, and has been therefore considered in this paper.

#### **EXPERIMENTAL PROCEDURE**

The examination of EPROM and  $E^2$ PROM radiation hardness was carried out in a cobalt-60 ( $^{60}$ Co) gamma radiation field at the Vinča Institute of Nuclear Sciences, Belgrade, Serbia. The absorbed dose dependence of the changes in the memory samples caused by irradiation was monitored.

The <sup>60</sup>Co source was manufactured at Harwell Laboratory. The air kerma rate was measured at various distances from the source with a Baldwin-Farmer ionization chamber. The absorbed dose was specified by changing the duration of irradiation and the distance between the source and the examined memory samples. The absorbed dose in Si was calculated from the absorbed dose in air, by using the appropriate mass energy-absorption coefficients for an average energy of <sup>60</sup>Co gamma quanta equal to 1.25 MeV. Mass energy-absorption coefficients for silicon and air –

 $_{enSi}(1.25 \text{ MeV}) = 0.02652 \text{ cm}^2/\text{g}, \quad _{enAIR}(1.25 \text{ MeV}) = 0.02666 \text{ cm}^2/\text{g} - \text{were obtained from the NIST tables}$ [5].

The testing was performed on the samples of COTS (Commercial Of The Shelf) EPROMs and E<sup>2</sup>PROMs. The EPROMs used for the investigations were NM27C010 components, with 1.048.576-bit storage capacity, organized as 128K-words of 8 bits each, in a 32-Lead PLCC package. The E<sup>2</sup>PROM samples used were NM93CS46 components, with 1024-bit storage capacity, organized as a 64 16-bit array, packaged in an 8-pin DIP chip carrier. Forty samples were used for both EPROM and E<sup>2</sup>PROM testing, on the basis of which the average results presented in the paper were obtained. All tests were performed at the room temperature (25 °C). The irradiation of a 40-sample batch was conducted in consecutive steps, corresponding to the increase of the total absorbed dose. The dose increment was 30 Gy per irradiation step for EPROMs and 50 Gy for E<sup>2</sup>PROMs.

All memory locations (cells) were initially written into a logic '1' state, corresponding to an excess amount of the electron charge stored on the floating gate. This state has been shown to be more radiation sensitive than the '0' state, responding with a greater threshold voltage shift for the same absorbed dose [6]. The effects of gamma radiation were examined in terms of the number of "faults" in memory samples following the irradiation. A fault is defined by the change of a memory cell logic state as a consequence of irradiation. The content of all memory locations was examined after each irradiation step, whereby the number of read logic '0' states equaled the number of faults.

Although ionizing radiation effects in MOS structures are generally dose-rate dependent, effects in EPROM and  $E^2$ PROM cells don't depend on the dose rate. Radiation induced charge changes on the floating gate occur extremely fast, and so are in phase with any incident radiation pulse [7].

#### **RESULTS AND DISCUSSION**

The plots presented in the paper are based on the mean values taken for over 40 samples. Both the dif-



Figure 1. Average relative change of the number of faults vs. the absorbed dose in irradiated EPROM samples: (a) differential, (b) aggregate ( $N_{tot} = 1.048.576$  bits,  $N_0 = 0$ )

ferential and aggregate relative change of the number of faults with the absorbed dose in EPROM samples is shown in fig. 1 (a) and (b). First faults, of the order of 2%, appeared at 1120 Gy. The number of faults increased with the rise of the absorbed dose. At dose values above 1240 Gy, significant changes in memory content were observed.

Changes in EPROMs proved to be reversible, *i. e.* after UV erasure and reprogramming all EPROM components became functional again – consecutive erasing, writing and reading of the previously irradiated samples was efficiently performed several times.

A repeated irradiation procedure of EPROM samples, following erasure and reprogramming to '1' state, produced faults already at 220 Gy, with significant failures in memory content occurring above 310 Gy, as shown in fig. 2 (a) and (b). The lower threshold of fault occurrence upon repeated irradiation testifies of the cumulative nature of radiation effects.

The differential and aggregate relative change of the number of faults with the absorbed dose in irradiated E<sup>2</sup>PROM samples is shown in fig. 3 (a) and (b). First faults appeared at 900 Gy, proving E<sup>2</sup>PROMs to be more sensitive to gamma radiation than EPROM components. With further dose increase, the number of faults also increased. Moreover, the changes in



Figure 2. Average relative change of the number of faults vs. the absorbed dose in reprogrammed and repeatedly irradiated EPROM samples: (a) differential, (b) aggregate ( $N_{tot} = 1.048.576$  bits,  $N_0 = 0$ )

 $E^2$ PROMs appeared to be irreversible. The irreversibility of radiation damage in  $E^2$ PROMs was established based on the fact that the standard erasure procedure was unable to erase the contents of any of the irradiated memory samples.

In CMOS EPROMs and  $E^2$ PROMs, utilizing either N-well or P-well technology, the dual polysilicon gate, consisting of the control and the floating gate, resides over an N-channel transistor. The polysilicon layer floating gate, insulated from the control gate above it and the silicon channel below it by the gate oxide, is used to store the charge and thus maintain a logical state. The charge is stored on the floating gate through the hot electron injection from the channel in EPROMs, and through the cold electron tunneling from the drain in  $E^2$ PROMs. The stored charge determines the value of the transistor threshold voltage, making the memory cell either 'on' or 'off' at the readout [1].

Passing through the gate oxide (SiO<sub>2</sub>), gamma radiation breaks Si–O and Si–Si covalent bonds, creating electron/hole pairs. The number of generated electron/hole pairs depends on the gate oxide thickness. The recombination rate of these secondary electrons and holes depends on the intensity of the electric field in the irradiated oxide, created by the charge stored at the



Figure 3. Average relative change of the number of faults *vs.* the absorbed dose in irradiated  $E^2$ PROM samples: (a) differential, (b) aggregate ( $N_{tot} = 1024$  bits,  $N_0 = 0$ )

floating gate, and modulated by the change in the charge carrier concentration and their separation within the oxide. The greater the electric field, the larger the number of carriers evading recombination. Incident gamma photons generate relatively isolated charge pairs, and recombination is a much weaker process than in the case of highly ionizing particles.

Secondary electrons which escape recombination are highly mobile at the room temperature. In the '1' state of the memory cell, the excess amount of the electrons stored on the floating gate maintains an electric field in both oxide layers, that swiftly drives the secondary electrons away from the oxide to the silicon substrate and the control gate. The direction of the electron motion is generally dependent on the gate voltage polarity at the time of irradiation. The electron drift occurs even with no external voltage applied to the gate, due to work function potentials. The logic '1' state (the excess amount of the negative charge stored on the floating gate) has been chosen as the starting state in this paper, since it is more liable to fault occurrence. The energy band diagram of the dual polysilicon gate when programmed into the excess electron (logic '1') state is shown in fig. 4. The diagram also illustrates the electric field direction in the oxide  $(SiO_2)$  and the charge stored on the floating gate.



Figure 4. Energy band diagram of the dual polysilicon gate when programmed into the logic '1' state

In addition to electron/hole pair creation, secondary electrons may produce defects in the oxide by way of impact ionization. Colliding with a bonded electron in either an unstrained silicon-oxygen bond (Si-O-Si), a strained silicon-oxygen bond, or a strained oxygen vacancy bond ( Si-Si ), a secondary electron may give rise to one of the hole trapping complexes. Interaction with an unstrained silicon-oxygen bond gives rise to one of the energetically shallow complexes ( Si-O +Si or Si-O+ Si , where denotes the remaining electron from the bond). Strained silicon-oxygen bonds, distributed mainly near the oxide/substrate and oxide/floating gate interfaces, are easily broken by the passing electrons, giving rise to the amphoteric non-bridging oxygen (NBO) center (Si-O) and the positively charged Si<sup>+</sup> center (known as the  $E_s$  center). The collision of the secondary electron with one of the strained oxygen vacancy bonds, also concentrated near the interfaces, leads to the creation of the  $Si^+$  Si center (known as the E center). Hole traps generated in the bulk of the oxide are shallow, while the centers distributed in the vicinity of the interfaces (NBO,  $E_s$ ,  $E_s$  and their variants) act as deep hole traps at which the long-term trapping of holes occurs [8, 9]. The latter are referred to as interface traps, surface states, or border traps [10].

While traversing the oxide, radiation-generated secondary electrons themselves create additional electron/hole pairs. Some of the secondary electrons may be trapped within the oxide, but this is a low-probability event, due to their high mobility and the low concentration of electron trapping sites in thermally grown SiO<sub>2</sub> [11].

The holes generated in the oxide by incident gamma radiation and through secondary ionization are far less mobile than the electrons. They are either trapped in the oxide, or move toward the floating gate under the influence of the electric field in the logic '1' state. Hole transport through the oxide occurs by means of two mechanisms: hopping transport via direct hole tunneling between localized trap sites, and trap-mediated valence band hole conduction.

The probability of holes moving through the oxide breaking unstrained silicon-oxygen bonds is low. However, since hydrogen atoms and hydroxyl groups are always present in thermally grown oxides as impurities, migrating holes may create defects by interacting with either =Si-H or Si-OH bonds, whereby hydrogen atoms and ions (H° and H<sup>+</sup>) are released. Once reaching the oxide/floating gate interface, holes can break both strained silicon-oxygen bonds and strained oxygen vacancy bonds, producing NBO, E<sub>s</sub>, and E centers. Holes trapped at the oxide/substrate interface which recombine with electrons injected from the substrate may produce another kind of amphoteric defect (Si<sub>3</sub> Si, a silicon atom at the interface back bonded to three silicon atoms from the floating gate), called the  $P_{\rm b0}$  center [12-14].

Radiation produced bulk defects may themselves migrate in the strained region near either the oxide/floating gate or the oxide/substrate interface and result in the formation of interface traps [15, 16].

Another mechanism of interface trap buildup includes hydrogen atoms and ions released by the holes in the oxide. Hydrogen atoms and ions diffuse and drift toward the oxide/floating gate interface. When an  $H^+$  ion arrives at the interface, it picks up an electron from the floating gate, becoming a highly reactive hydrogen atom  $H^\circ$ , which is able to produce interface traps [17, 18].

Interface traps may also be generated through direct interaction of incident gamma photons [19, 20].

Holes not trapped in the oxide are injected into the floating gate, reduce the net amount of the electron charge stored on it, and thereby decrease the threshold voltage of the cell's NMOS transistor. The trapping of holes occurs mostly at the oxide/floating gate interface, where the concentration of deep hole traps is high. The positive charge of these trapped holes will tend to mask the negative electron charge on the floating gate, again reducing the transistor threshold voltage. Thus, the trapped and the injected holes both produce a negative threshold voltage shift.

The small oxide thickness gives rise to the considerable fluctuation of the absorbed energy, directly influencing the number of faults in the examined samples. Moreover, the amount of radiation-induced defects acting as electron and hole traps is a complex function of the gate oxide material, as well as of the doping and processing methods used in securing the oxide onto the silicon surface. These are the reasons for the observed variation in the number of faults among the examined memory samples. Another effect caused by gamma radiation is electron emission from the floating gate. This kind of emission is the basis for standard EPROM erasure by UV radiation. During the irradiation, gamma photons cause electrons to be emitted over the floating gate/oxide potential barrier. Once in the oxide, electrons are swept to the substrate or the control gate by the electric field. The loss of electrons from the floating gate causes the additional decrease of the threshold voltage [21, 22].

The net effect of charge trapping in oxide and at oxide/floating gate interfaces, as well as of floating gate hole injection and electron emission, is the change of the NMOS transistor threshold voltage. The radiation induced change of the threshold voltage may affect the memory cell logic state at the readout. The threshold voltage  $V_{\rm T}$  is, hence, the key parameter of the memory cell state. Modeling the charge stored at the NMOS floating gate as the charge on a parallel plate capacitor, the threshold voltage can be expressed as

$$V_{\rm T} \quad V_{\rm T0} \quad \frac{q_{\rm s}d}{\varepsilon} \tag{1}$$

where  $V_{\rm T0}$  is the initial transistor threshold voltage due to processing,  $q_{\rm s}$  – the floating gate surface charge density, d – the oxide thickness between the control and floating gate, and  $\varepsilon$  – the oxide dielectric constant. This model disregards the dependence of the threshold voltage on the actual position of the trapped charge sheet within the oxide. The influence of gamma irradiation on programmable memories is manifested through the change of the net gate surface charge density. The threshold voltage as a function of the absorbed dose can be represented by the empirical relation

$$V_{\rm T}(D) \quad V_{\rm T}^{\rm eq} \quad (V_{\rm T0} \quad V_{\rm T}^{\rm eq}) e^{-\alpha D} \tag{2}$$

where  $\alpha$  is a constant dependent on the type and energy level density of the traps in the oxide, and  $V_T^{eq}$  – the threshold voltage at extremely high doses (also called the radiation saturation voltage), when an equilibrium of the dominant processes causing the change of the gate surface charge density – hole trapping, hole injection, electron emission, and electron-hole recombination – is achieved.

UV photons with the energy lower than the bandgap of silicon dioxide (9 eV) are incapable of creating electron-hole pairs in the oxide, but are capable of exciting electrons from the silicon substrate into the oxide where they recombine with the trapped holes [23]. The irradiation of EPROMs by UV light during erasure partially reduces the radiation-induced trapped charge from the previous exposure to gamma photons. This light-induced annealing of trapped holes can account for the observed reversibility of changes in EPROMs.

The cumulative nature of gamma radiation effects observed in EPROM components can be attrib-

uted to the fact that not all holes trapped at radiation induced interface states are annealed during UV erasure at the ambient temperature.

Since the E<sup>2</sup>PROM erasing process involves no UV irradiation, there can be no light-induced annealing of trapped holes in these components. The thermal annealing of holes trapped at deep interface traps is not evident at ambient temperatures. The current-induced annealing of trapped holes, due to recombination of holes with electrons being driven from the floating gate to the drain, could be expected to occur during E<sup>2</sup>PROM electrical erasure. However, this kind of annealing is known to require much longer time compared to the duration of a standard E<sup>2</sup>PROM erasing procedure [24, 25]. On the whole, no significant annealing of trapped holes occurs in E<sup>2</sup>PROMs, and hence radiation-induced changes in these components appeared irreversible on the time scale of the experiments performed in this paper ( $\sim 10$  hours).

The higher sensitivity of the tested  $E^2$ PROM components to gamma radiation is a consequence of a more pronounced radiation induced electron emission from the floating gate over the thin oxide region (10 nm) between the floating gate and the drain, due to a lower potential barrier [2].

## CONCLUSIONS

This paper presents the results of the examination of programmable ROMs' radiation hardness. The influence of 60Co gamma radiation was tested on EPROM and E<sup>2</sup>PROM components. EPROM components exhibited higher radiation reliability than E<sup>2</sup>PROMs. Significant faults in EPROM and E<sup>2</sup>PROM components appeared at 1240 Gy and 900 Gy, respectively. Changes in EPROMs are reversible, and after erasing and reprogramming, all EPROM components restored their functionality. The reversibility of changes in EPROMs is attributed to the partial light-induced annealing of trapped holes during UV erasure. Due to the cumulative radiation effects, first failures of the previously irradiated EPROMs appear at significantly lower doses. On the other hand, E<sup>2</sup>PROM changes are irreversible. All observed phenomena have a plausible theoretical explanation, based on the interaction of gamma rays with the oxide layer of memory cell MOS transistors. The influence of gamma radiation is basically manifested through the change of the net floating gate surface charge density, and consequently of transistor threshold voltage.

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## Милош ВУЈИСИЋ, Ковиљка СТАНКОВИЋ, Александра ВАСИЋ

## ПОРЕЂЕЊЕ УТИЦАЈА ГАМА ЗРАЧЕЊА НА ЕРROM И Е<sup>2</sup>PROM МЕМОРИЈЕ

У овом раду пореди се поузданост стандардних комерцијалних ЕРROM и  $E^2$ PROM меморија при излагању гама зрачењу. Резултати добијени за ЕРROM (NM27C010) и  $E^2$ PROM (NM93CS46) компоненте израђене у CMOS технологији показују да ЕРROM меморије поседују већу радијациону отпорност од  $E^2$ PROM меморија. Поред тога, промене настале у ЕРROM-има су реверзибилног карактера и након брисања и поновног уписа све ЕРROM компоненте су повратиле функционалност. Насупрот овоме, промене које зрачење изазива у  $E^2$ PROM чиповима су трајне. Добијени резултати су анализирани и протумачени на бази интеракције гама зрачења са CMOS структуром.

Кључне речи: ЕРROM, Е<sup>2</sup>PROM, *гама зрачење*, радијациона ошиорносш