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10 Gb/s Bang-Bang Clock and Data Recovery (CDR) for optical transmission systems

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Abstract. A Bang-Bang Clock-Data Recovery (CDR) for 10 Gb/s optical transmission systems is presented. A direct modulated architecture is used for the design. Its loop characteristics can be derived using an analogy to $\Sigma\Delta$ theory. The circuit was produced and measured in a commercial 0.25 μm BiCMOS technology with a transition frequency f_T=70 GHz.

1 Introduction

Linear charge pump-PLLs with the so-called "Hogge" phase detector (Hogge, 1985) played a long time a favorite role in realizing Clock-Data-Recovery circuits for optical transmission systems. Its loop characteristic is well known (Gardner, 1980) and the low complexity of the phase detector allows efficient implementation. However, with the migration to higher data rates the influence of second order effects in the phase detector grows rapidly. Transition mismatches in the data paths can result in a constant phase error, which is worsening the bit-error-rate(BER) of the system. The trend to higher integration density, system-on-chip and smaller packages made the search for other solutions inevitable.

2 Bang-Bang PLLs

The output characteristic of a Bang-Bang phase detector does not contain any information about the absolute value of the phase error $|\phi_e|$, but only about its sign, as it can be seen at Fig. 1. Thus a linearized analysis of the loop behavior as done in (Gardner, 1980) is not possible.

The first systematical analysis of the bang-bang PLL (Walker, 2003) describes its loop behavior using $\Sigma\Delta$ conversion theory in the phase domain.

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2.1 System analysis of 1st-order Bang-Bang PLL

To understand the system behavior of the Bang-Bang-PLL we will priorly examine a simplified model of a 1st-order Bang-Bang PLL (see Fig. 2).

It consists of a D-flip-flop and a voltage-controlled-oscillator (VCO), that can be switched between two discrete frequencies, which have a distance of f_{bb} to its center frequency f_0. The flip-flop has the function of a Bang-Bang phase-detector for a clock signal, instead of a NRZ-data signal as input signal. The applied clock signal with the frequency f_{in} is sampled by the flip-flop at the rising edge of the VCO signal.

The VCO is controlled by the output Q of the flip-flop. For its output frequency f_{out} holds:

$$f_{out}(K_{in}) = \begin{cases} f_0 + f_{bb} & \text{if } K_{in} = 0 \\ f_0 - f_{bb} & \text{if } K_{in} = 1 \end{cases} \quad (1)$$

2.2 Control mechanism of PLL for frequency deviation δf

We assume that the input signal has a clock frequency f_{in} which has a frequency deviation of δf to the VCOs center frequency f_0. Furthermore should be $|\delta f| < f_{bb}$. Under these conditions a square wave is generated at the control node K_{in} of the VCO. The duty cycle C of this square wave is dependent to the frequency deviation δf of the input signal. The duty cycle C is given by (Walker, 2003)

$$C = \left(\frac{1}{2} + \frac{\delta f}{2 f_{bb}}\right). \quad (2)$$

2.3 Control mechanism of PLL to sinusoidal input jitter

To examine the control mechanism of the circuit to sinusoidal input jitter, we presume that the clock frequency of the input f_{in} is equal to the center frequency of the VCO (δf=0). Thus the signal at the control node of the VCO has a duty cycle C=0.5.

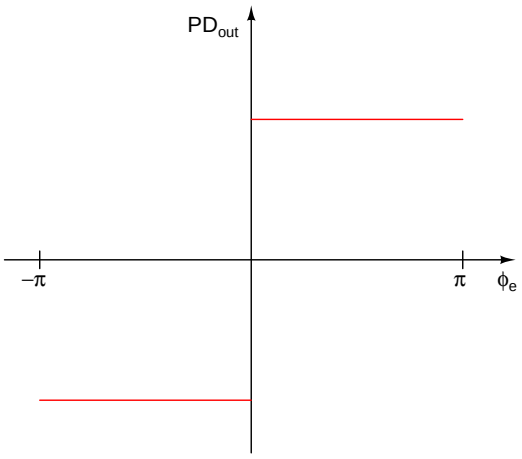


Fig. 1. Output characteristic of a Bang-Bang phase-detector

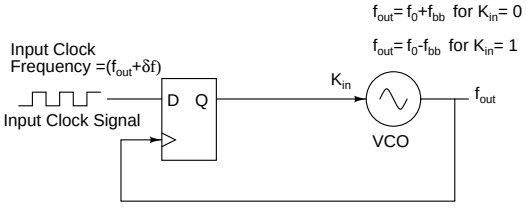


Fig. 2. 1st-order Bang-Bang PLL.

The input signal should now exhibit a sinusoidal jitter $\phi_D(t)$. This jitter has a amplitude $\hat{J}_{UI}$(UI means *Unit Interval* that is equivalent to a bit length T_B) and a frequency f_{jitter} and is defined by

$$\phi_D(t) = 2\pi \cdot \hat{J}_{UI} \cdot \sin\left(2\pi f_{jitter} t\right) \tag{3}$$

moreover the following assumption should be made:

$$f_{in} = \frac{1}{T_B} >> f_{jitter}\,. \tag{4}$$

As priorly presumed the data rate $1/T_B$ (the clock frequency f_{in} respectively) is now equal to the center frequency f_0, but the VCO frequency changes from $(f_0 - f_{bb})$ to $(f_0 + f_{bb})$ and vice-versa. Thus during every sample period T_B the VCO phase experiences a phase deviation ϕ_{bb} to the phase of the ideal input signal without jitter.Which is

$$\phi_{bb} = 2\pi \cdot f_{bb} \cdot T_B \quad \hat{=} \quad 2\pi \cdot \frac{f_{bb}}{f_0}\,. \tag{5}$$

Now we can define a slew-rate SR_{bb} of the PLL. It can be calculated to

$$SR_{bb} = \frac{\phi_{bb}}{T_B} = 2\pi \cdot f_{bb}\,. \tag{6}$$

This slew rate determines the maximum input jitter deviation that could be transferred to the output. It follows for a given input jitter ϕ_D that

$$\frac{\delta\phi_D}{\delta t} \leq SRT_{bb}\,. \tag{7}$$

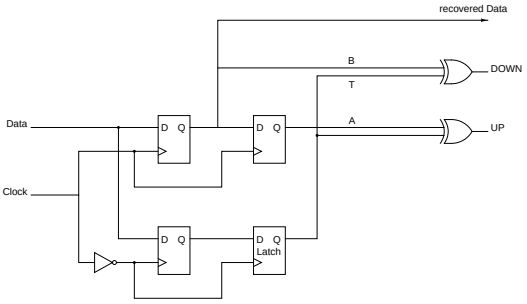
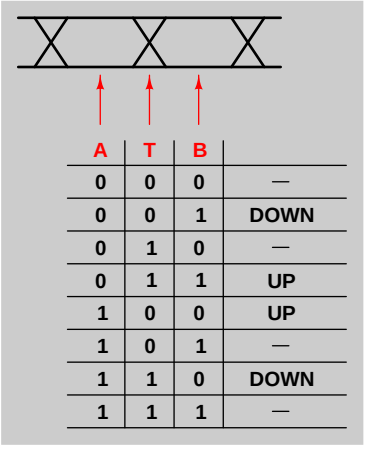


Fig. 3. Bang-Bang phase detector.



A	T	B	
0	0	0	—
0	0	1	DOWN
0	1	0	—
0	1	1	UP
1	0	0	UP
1	0	1	—
1	1	0	DOWN
1	1	1	—

Fig. 4. Timing diagram of the Bang-Bang phase detector.

With the sinusoidal input jitter of Eq. 3 and Eq. 6 follows that

$$\hat{J}_{UI} \cdot 4\pi^2 f_{jitter} \cdot \cos\left(2\pi f_{jitter} t\right) \leq 2\pi \cdot f_{bb}\,. \tag{8}$$

Thus the loop condition is

$$2\pi\, \hat{J}_{UI} \cdot f_{jitter} \leq f_{bb}\,. \tag{9}$$

A Bang-Bang PLL is a so-called slew rate limited system.

3 Bang-Bang phase detector

Until now we assumed that the PLL input signal is a clock signal, in this case a D-flip-flop is sufficient as phase detector. To implement the phase detector function for a NRZ-data stream as PLL-input signal we will use the so called Alexander-PD (Alexander, 1975).

The block diagram of this phase detector is shown on Fig. 3.

The circuit samples two consequent data bits A and B as well as the transition T between the two bits. In two XOR-gates the VCO-control signals *UP* and *DOWN* are created (see Fig. 4).

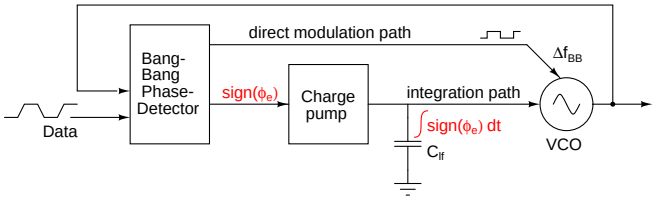


Fig. 5. 2nd-order Bang-Bang PLL with Integrator for frequency control.

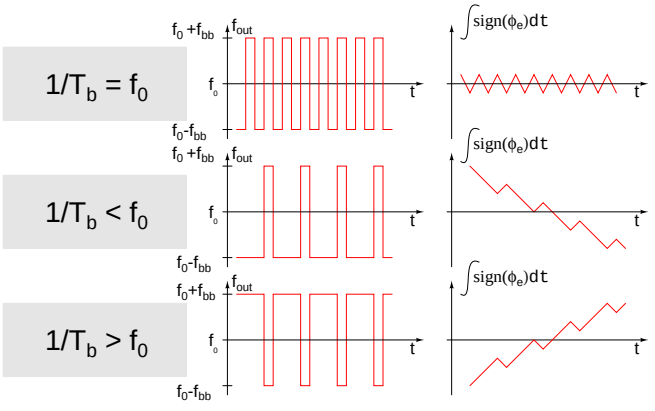


Fig. 6. Frequency control with a integrator in a 2nd-order Bang-Bang PLL.

3.1 2nd-order Bang-Bang PLL

In the analysis in 2.3 we assumed that the data rate $1/T_B$ (the clock signal f_{in} in the simplified model respectively) of the system is equal to the center frequency of the VCO f_0. Furthermore we have seen in 2.2 that the 1st-order Bang-Bang PLL has a very limited frequency range of $2 \cdot f_{bb}$ around the center frequency f_0.

In a real circuit the center frequency of the VCO has to be guided towards the data rate $1/T_B$. This is achieved by the means of a integrator consisting of a charge pump and a capacitor C_{lf}, as depicted in Fig. 5. The output of this integrator is connected to a separate control node of the VCO.

The mechanism of this frequency control is shown in detail on Fig. 6. Assuming a data rate $1/T_B$ equal to the center frequency of the VCO, we get from Eq. 2 a duty cycle C of 0.5. Thus a triangle signal with constant average can be seen at the output of the integrator. The system is in equilibrium. If the data rate $1/T_B$ is lower than the center frequency f_0 of the VCO the duty cycle C of the phase detector output will be smaller than 0.5. Thus the average of the triangle signal will decrease, which again regulates the VCO frequency versus a lower frequency. An analogous behavior can be seen for data rates $1/T_B$ higher than the center frequency f_0.

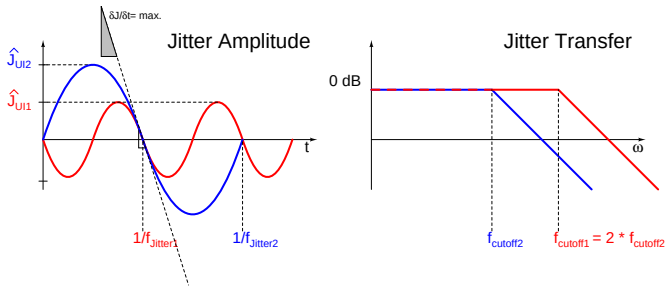


Fig. 7. Jitter transfer characteristics for two different jitter amplitudes.

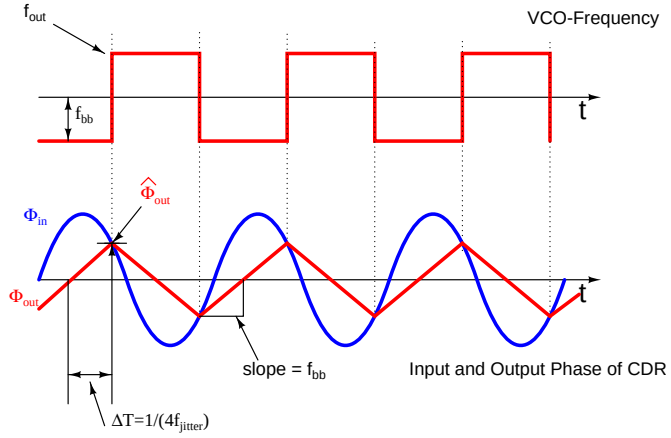


Fig. 8. Effect of slewing on the jitter transfer

4 Dimensioning for SONET-Specifications

The most important specifications of a CDR circuit are its

1. Jitter transfer
2. Jitter tolerance
3. Jitter generation

The following section explains the way how PLL-parameters have influence on these specifications.

4.1 Jitter transfer

The jitter transfer gives the quantity of jitter that is passed from the CDR-input to its output.

In 2.3 we showed that the control behavior of the Bang-Bang-CDR is limited by its slew rate. From Eq. 9 follows that the jitter transfer is dependent on the jitter amplitude. The jitter transfer for two different jitter amplitudes $\hat{J}_{UI1}$ and $\hat{J}_{UI2}$ is shown on Fig. 7.

For jitter frequencies $< f_{\text{cutoff}}$ the control condition Eq. 9 is fulfilled. Thus for jitter transfer can be written

$$\frac{J_{out}}{J_{in}} \approx 1\,. \tag{10}$$

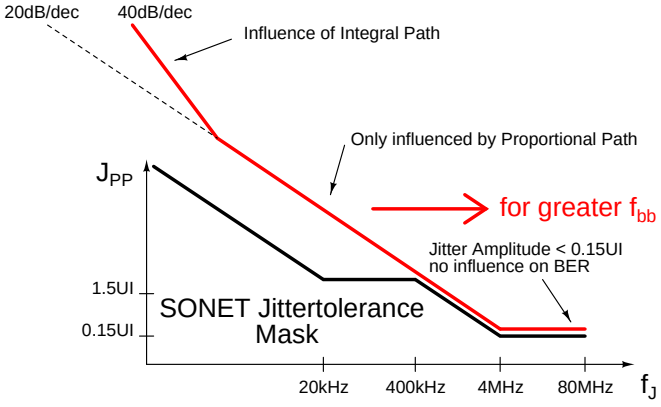


Fig. 9. Jitter tolerance.

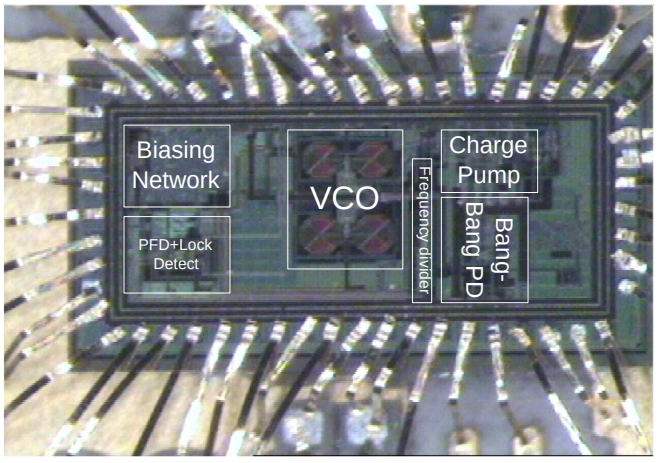


Fig. 11. CDR – die photography.

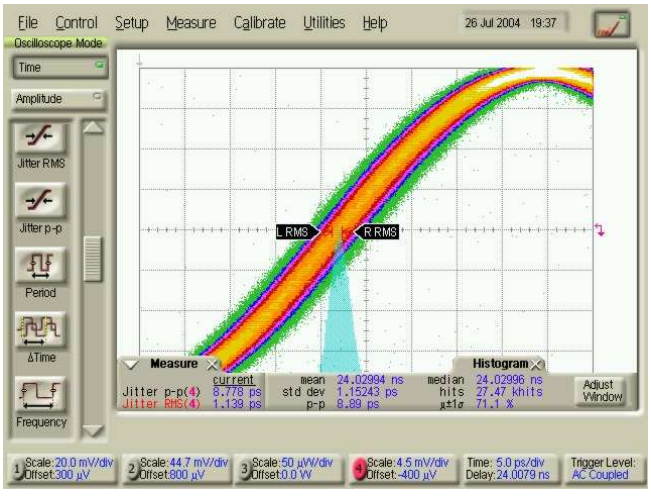


Fig. 10. Measurement results: clock jitter.

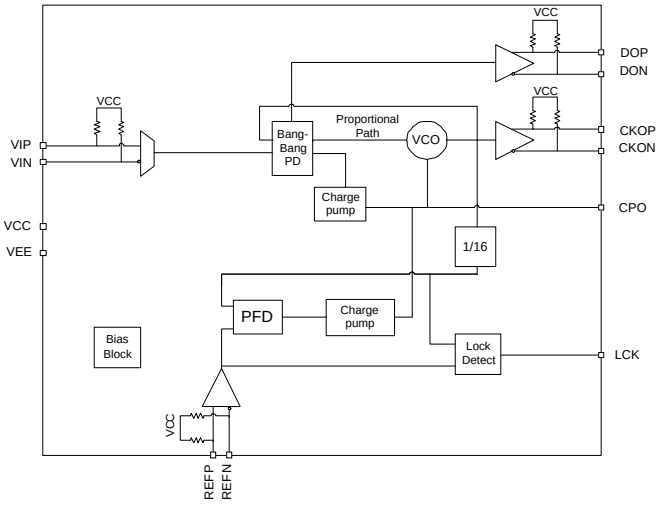


Fig. 12. CDR – Block diagram.

When control condition Eq. 9 is not fulfilled the slewing begins. As it can be seen on Fig. 8 the output phase Φ_{out} is now triangle-shaped for a sinusoidal input phase Φ_{in}. The jitter transfer function can now be approximated.(Lee et al., 2004)

$$\left|\frac{\Phi_{out}}{\Phi_{in}}\right| \approx \frac{\hat{\Phi}_{out}}{\hat{\Phi}_{in}} = \frac{f_{bb} \cdot \Delta T}{\hat{\Phi}_{in}} = \frac{f_{bb}}{4 \cdot f_{jitter} \cdot \hat{\Phi}_{in}} . \qquad (11)$$

This function has a slope of -20 dB/Decade.

4.2 Jitter tolerance

The jitter tolerance determines the peak-to-peak value J_{P-P} of the input jitter for a jitter frequency f_{jitter}, that can be applied to the CDR input without worsening the bit-error-rate (BER) of 10^{-12}.

In the SONET specifications a jitter tolerance mask is given that must be respected by the jitter tolerance characteristic of the Bang-Bang CDR (see Fig. 9).

The jitter tolerance characteristic of a Bang-Bang CDR can be divided in three different regions. The slew-rate-limiting leads to a slope of -20dB/Decade in the middle region of the characteristic(see Eq. 11). In the low frequency regions the increasing influence of the integrator path of the frequency control results in a slope of -40dB/Decade. For jitter amplitudes lower than 0.15 UI the jitter has no influence on the BER, thus the jitter tolerance characteristic is flat in this region.

4.3 Jitter generation

The jitter generation numbers the amount of jitter that exhibits the recovered clock of the CDR with a ideal input signal without jitter.
The SONET-Specification allows a jitter generation of

$$J_{P-P} \leq 0.1\text{UI} \qquad \text{for} \quad 50\,\text{kHz} \leq f_{jitter} \leq 80\,\text{MHz} \qquad (12)$$

For a Bit-Error-Rate of 10^{-12} we get a rms-value of the jitter

$$J_{RMS}=\frac{J_{P-P}}{2\cdot\sqrt{2}\mathrm{erfc}^{-1}(2\cdot\mathrm{BER})}\approx\frac{J_{P-P}}{14}\widehat{=}0.7\,\mathrm{ps}\,. \quad (13)$$

The two dominant sources for jitter in a Bang-Bang-CDR are the phase noise $\mathcal{L}$ of the VCO and the so-called "hunting"-jitter $J_{rms_{BB}}$ that is generated by the VCO switching.
The phase noise $\mathcal{L}$ is high-pass filtered in the PLL with a transfer function

$$G_{HP}(s)=\frac{s}{1+s/\omega_{-3dB_{PLL}}}\,. \quad (14)$$

The resulting jitter $J_{rms_{vco}}$(in UI) can be calculated with

$$J_{rms_{vco}}=\frac{1}{2\pi}\sqrt{2\cdot\int_{f1}^{f2}|G_{HP}(j2\pi f)|\mathcal{L}(f)df}\,. \quad (15)$$

With a NRZ-coded PRBS data stream V_{Data}

$$V_D(t-nT_B)\in[0;1]\quad \text{mit } n=1,2,3,4...\\ \text{und } T_B=\text{bit length} \quad (16)$$

as input signal results a VCO output signal

$$V_{VCO}(t)=\hat{V}\cdot\sin\left[(\omega_0+\omega_{bb}\cdot\mathcal{X}_{mod}(t))\cdot t\right] \quad (17)$$

with

$$\mathcal{X}_{mod}(t)=\begin{cases}0 & \text{if } V_D(t-nT_B)=V_D(t-(n-1)T_B)\\ \pm1 & \text{if } V_D(t-nT_B)\neq V_D(t-(n-1)T_B)\end{cases} \quad (18)$$

The rms-value of the jitter can be calculated integrating the spectrum of Eq. 17 over the frequency range

$$J_{rms_{BB}}=\frac{1}{2\pi}\sqrt{2\cdot\int_{f_1}^{f_2}\mathcal{FT}[V_{VCO}(t)](f)df}\quad(\text{in UI})\,. \quad (19)$$

As both jitter sources are uncorrelated, the overall jitter can be calculated with

$$J^2_{rms_{ges}}=J^2_{rms_{VCO}}+J^2_{rms_{BB}}\,. \quad (20)$$

5 Measurement results

A CDR-prototype was produced in a commercial $0.25\,\mu m$ BiCMOS technology. Figure 12 shows the CDR block diagram and Fig. 11 the die photography of the prototype. The power consumption of the IC is 750 mW. On Fig. 10 is shown the jitter histogram of the recovered clock from a $2^{31}-1$ PRBS-input signal. The measured rms-value of the jitter is 1.15 ps.

6 Conclusions

The use of linear charge pump PLLs with "Hogge"-phase detector for clock-data-recovery in optical 10 Gb/s systems is limited by the increasing influence of parasitic effects on the loop performance. Bang-Bang-CDRs present a promising alternative to linear CDRs. A direct modulated Bang-Bang-CDR for 10 Gb/s SONET application was presented. The system behavior of the circuit was described be the means of a non-linear approach (Walker, 2003). These insights were used to determine the PLL-parameter which have influence on the most important SONET-specifications.

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