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Best usage of free-space capacitors in ASIC regulators

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Abstract. In this work we examine how to improve the performance of voltage regulators in application specific integrated circuits (ASICs) by placing capacitors into free layout space. The problem arising after layout, when there are areas not covered by functional elements, is where to connect the free-space capacitors (FSCs), as they can be connected to the input or the output net of a voltage regulator. Therefore we designed a testbench for mathematical calculations and one for simulations to identify the influence of a capacitance connected at these certain positions. We mainly focused on PSR analysis while not losing sight of transient effects. The results of calculation and simulation illustrate that the best solution is to split the capacitance half by half to both possible nets if no output capacitance was installed during design. Otherwise a ratio of one to one for input capacitance to output capacitance has to be set up for best performance.

1 Introduction

In application specific integrated circuits (ASICs) regulators are used to create an output voltage from a certain input voltage range. The ideal regulator has a constant output voltage independent of a load change and without any influence from the input voltage. This influence not only includes DC voltage levels (line regulation), but also any AC distortion. The independence of the output voltage from the input is called power supply rejection (PSR) (Ong and Chan, 2010). In literature also often the term PSRR (power supply rejection ratio) (Baker, 2010; Holberg, 2010) is found, which is more true for amplifier as there a ratio between the signal amplification and the power distortion damping exists, while in regulators only the power distortion damping is of interest. Nonideal regulators, which are in fact all implemented regulators, suffers from both, AC distortions and transient load changes. The PSR is limited in its damping and also frequency dependent, i.e. in most cases the PSR gets worse with higher frequencies due to capacitive coupling. Load changes create a distortion at the output voltage as the regulation loop needs time to settle to the adopted IR drop. The investigations of improvement of PSR and load stability are important, especially if there are sensitive front-ends on the ASIC. They would be disturbed by these effects and then wrong data would be returned by precious analog to digital converters (ADCs) to signal processing devices like on- or off-chip microcontrollers or DSPs. Therefore a better ASIC performance should be reached by increasing the PSR of the regulator.

Many authors have been dealing with topics concerning regulators. New methods to increase PSR or faster load regulation loops are e.g. 2-stage regulation (Yang et al., 2009) or double regulation (Lim et al., 2011). Newest trends also tend to capacitor-less low dropout regulators, where a high PSRR could be reached by an additional fast output buffer, which drives the regulation transistor (Abbasi et al., 2010). Another method to increase PSRR is to add a left-hand zero by nested Miller compensation (Huang and Liu, 2011) or to use a negative feedback loop (Shirahatti et al., 2010). Capacitor-less regulators are voltage regulators, which don't need an external bypass or stabilization capacitor as the Texas Instruments TPS78915 (TI, 2000) would need. Nevertheless, capacitorless does not exclude capacitors at all, as internal capacitors are still used for these regulators. An advantage of on-chip capacitors is that they have very low ESR(QuadTech, 2003) values due to the short metal connections. For on-chip capacitors, often the leakage is stated in the design documents. A typical leakage value is around 1e-8 to 1e-7 $\mathrm{A\,cm^{-2}}$ (TI, 2009) which would result in a minimum parallel resistance value for 1.8 V and 1 $\mathrm{mm^2}$ of around 1.8 GΩ. Smaller ESR value as typical off-chip capacitors and low leakage makes capacitor choice discussion for ESR (Morita, 2011) and leakage obsolete.

As this work researches PSR effects, noise reduction techniques like low-pass filtering of the Bandgap reference

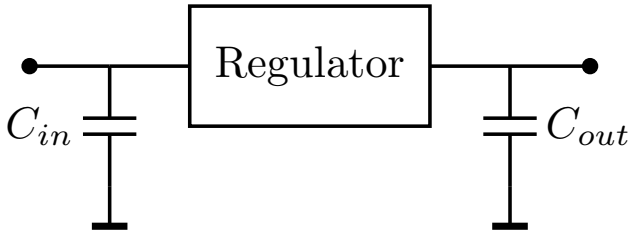

Fig. 1. Possibel positions for free-space capacitor

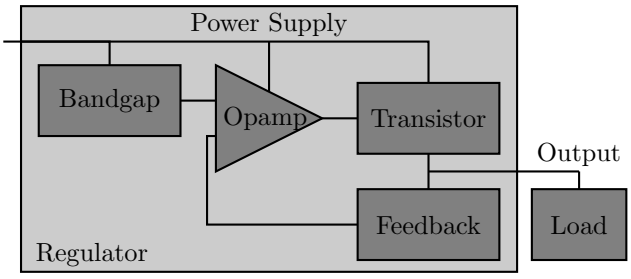

Fig. 2. Regulator under research

voltage with external (TI, 2000) or possible internal capacitors are not further investigated.

This work deals with the question, which net is the best to connect free-space capacitors (FSCs). A free-space capacitor is a capacitor, created in ASIC areas, which are not covered by functional elements after layout. These areas are often gaps between elements of the regulator. More free space therefore leads to more capacitance. The FSCs are placed into the finished layout and their capacitance values are derived from their size, which is then back-annotated from the finalized layout to the corresponding schematic. As a higher capacitance would increase the PSR performance more and the capacitor has no need to have an exact value over process variations and temperature, the most important parameter, when choosing an appropriate capacitor from the design kit, is the capacitance per area. As the functionality of the regulator was already proved through simulations before layout, the additional capacitors are used to further improve the regulator and not for stability reasons.

The free-space capacitors are connected to ground with one side in every case, but which is the best net to connect the other side of the capacitors?

Should FSCs be connected to the input or the output net of the regulator (see Fig. 1), or should it be split to both nets? Both nets can be seen as supply nets, which could be stabilized by an additional capacitance. There are the same arguments for both nets, e.g. the capacitance between a net and ground serves as a low pass, which rejects AC distortions when taking net resistances into account or that FSCs are a charge storage which helps with transient load changes.

It should be mentioned that the reliability of an ASIC should not be decreased by additional free-space capacitors as on-chip capacitors generally have a low leakage. Of course the designer should pay attention that the regulator is still stable with an additional output capacitance, what is normally the case. A capacitor at the input could only have an effect on the time, the regulator needs to start up, if the capacitance is very large. Nevertheless it is worth to re-simulate the regulator after all changes from layout are back annotated.

2 Regulator under research and testbench

2.1 Regulator under research

For this work, the regulator under research is a low-dropout regulator (LDO), on which the best usage of a free-space capacitor is investigated. The LDO consists of 4 major elements, shown in Fig.2. The first one is a bandgap that is used to create a reference voltage to which the output voltage is compared. Next, there is an operational amplifier (op-amp) which is used to compare the bandgap voltage to the feedback voltage and to set the regulation transistor's gate voltage corresponding to the result of the comparison. This regulation transistor is the LDO's third element and is used to regulate the voltage drop between supply net and output net. Generally the transistor can be a n-MOS or p-MOS transistor and here a n-MOS device is used.

The voltage drop thereby is generated through an IR drop, where the current I is the current of the load plus the current of the feedback network and the resistance R is the resistance of the transistor, R_{ds_on}. This resistance is regulated by the gate voltage, set by the op-amp. For the regulation transistor it is necessary that its area is big enough so that the maximum current flow density is not exceeded for any load. Large area also helps transporting away the generated heat in the transistor.

The 4th element used in the LDO is the feedback network. In most applications it exists of two resistors forming a voltage divider, dimensioned in a way that the divided voltage corresponds to the bandgap voltage, when the output voltage of the LDO has the nominal value (Baker, 2010). The load in this work is a constant resistive load plus a parallel variable current source. An additionally capacitor is also taken into account at the later part of this work.

2.2 Testbench

For a good prediction to which net the capacitance should be connected, a good testbench is necessary. Aside to the regulator itself and the load, the testbench also includes the pads, the bond wires and the metal resistances from the on-chip wires. For the calculations, the circuit was simplified to reduce the number of elements. The inner circuitry

of the bandgap and the op-amp, connected between the supply wire *VDD3V* and ground, are included to the testbench by a impedance $Z(s)$. This impedance is assumed to have one pole, based on simplified simulation results. Including the PSR transfer characteristic of the bandgap $A_{\mathrm{BG}}(s)$ and the op-amp $A_{\mathrm{op}}(s)$ is done by the regulation transistor's gate voltage V_{G}. The Feedback influence from the resistive voltage divider (V_{FB}) is also included in $V_G = A_{\mathrm{op}}(s)\,(A_{\mathrm{BG}}(s)\,(V_{\mathrm{in}} - V_{\mathrm{drop}}) - V_{\mathrm{FB}})$ where $V_{\mathrm{drop}} = I_1\,(2s\,L_{\mathrm{bond}} + R_{\mathrm{met}})$ is the voltage drop of the package circuitry.

3 Calculation and simulation

3.1 Calculations

Based on the testbench, shown in Fig.3 calculations were effected to estimate the results and to verify that the diagrams gained by simulation show the correct behavior. The testbench has two input variables, V_{in} and I_{load}, but the calculations are done only for V_{in} as the point of interest is the PSR analysis. As the results depend on many parameter (e.g. $R_{\mathrm{FB1}}, R_{\mathrm{FB2}}, R_L, R_{\mathrm{met}}, L_{\mathrm{bond}}$) only the generalized zero pole forms are shown in Eqs. (1) and (4). The highest order coefficients of numerator denominator from Eqs. (1) and (4) are shown in Eqs. (2),(3) and (5) respectively, for the parameters directly affected by the FSCs, C_{in} and C_{out}. All other parameters are substituted by c_{ni} and c_{di}.

For the frequency behavior of *VDD3V*, Eqs. (1),(2) and (3) show that the number of poles and zeros keeps constant if either C_{in} or C_{out} or both are added. This is due to $Z(s)$ already having a pole, as the additional C_{in} would create. But Eqs. (2) and Eq. (3) show that the poles and zeros are shifted to lower frequencies especially at the change of C_{in}.

$$\frac{a_{2,VDD3V}\,s^2 + a_{1,VDD3V}\,s + a_{0,VDD3V}}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{1}$$

$$a_{2,VDD} = (c_{n1}\,C_{\mathrm{out}} + c_{n2})\,C_{\mathrm{in}} + c_{n3}\,C_{\mathrm{out}} + c_{n4} \tag{2}$$

$$\begin{aligned} b_4 = {} & (c_{d1}\,C_{\mathrm{out}} + c_{d2})\,{C_{\mathrm{in}}}^2 \\ & + (c_{d3}\,C_{\mathrm{out}} + c_{d4})\,C_{\mathrm{in}} + c_{d5}\,C_{\mathrm{out}} + c_{d6} \end{aligned} \tag{3}$$

The frequency behavior of *AVDD* to V_{in} (Eq. 4) is similar to that of *VDD3V* (Eq. 1). As both have the same denominator, the poles are shifted the same amount, but Eq. (5) shows that zeros are shifted otherwise.

$$\frac{AVDD}{V_{\mathrm{in}}} = \frac{a_{2,AVDD}\,s^2 + a_{1,AVDD}\,s + a_{0,AVDD}}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{4}$$

$$\begin{aligned} a_{2,AVDD} = {} & (c_{n21}\,C_{\mathrm{out}} + c_{n22} + c_{n23}\,C_{\mathrm{in}})\,s^2 \\ & + (c_{n24}\,C_{in} + c_{n25}\,C_{\mathrm{out}} + c_{n6})\,s + c_{n27} \end{aligned} \tag{5}$$

3.2 Simulation

After the calculations showed the principal behavior, simulations were executed. A simulation testbench was implemented, containing the elements added for package and the transistor level circuitry of the bandgap and the operational amplifier. To see the effects of a capacitor added to the input or the output clearly, the AC effects of the metal resistance and the bond inductances were simulated separately. *AVDD* is affected by a metal resistance change only by a pole movement towards lower frequencies. Adding the bond inductances adds a pole at about $f \propto \frac{1}{L_{\mathrm{bond}}}$ to the transfer functions, i.e. the higher the bond inductance the lower the frequency of the pole.

The complete regulator is supplied by a voltage of 3.3 V and has an output voltage of 1.8 V. The values for bond inductances were zero, 5 nH and 50 nH to see the effect of the inductance. With generally assumed value of $\approx 1\,\mathrm{nH\,mm^{-1}}$ (Lee, 2003) inductance per bondwire length, a value of 5 nH was used for the later simulations.

The resistance was varied between zero, 5 Ω and 50 Ω for the simulation of the wire effects. From earlier layout extractions a value of 5 Ω for thick supply wires is assumed for further simulations.

For output transistor a n-MOS transistor is chosen, while the opamp was implemented as folded-cascode. The total capacitance available for connection was extracted from layout with 114 unit capacitors, each with a value of 401 fF. So the total amount of capacitance is around 45.7 pF.

In Fig.4 the AC influence of the free-space capacitor towards *VDD3V* and *AVDD* is the point of interest. For the *VDD3V* net (upper 3 curves) the AC behavior is quite simple. Adding the capacitance to the output net has no effect to the input net in the frequency range of interest. The more capacitance is added to the input net the earlier *VDD3V* is damped and so has higher damping values at higher frequencies. I.e. the more capacitance is added to the net *VDD3V*, the lower is the frequency of the first pole, what corresponds to the calculation results. Of course the effects on *VDD3V* directly affect *AVDD*, as *AVDD* is derived from *VDD3V*.

For *AVDD* (lower curves in Fig.4) the influence is clearly visible, but very depending on the position of the capacitor. If the capacitor is at the input supply net (solid style), the curve is the worst of all three in middle frequencies. It profits from the shift of the pole of the input net from far right towards lower frequencies in the range of low gigahertz. Connecting the capacitor to the output or regulated net (dashed-dotted style) shows a high improvement in the mid frequency area. This improvement profits from the pole shift beginning from some tens of megahertz towards high frequencies. The third possible option, splitting the capacitor and connecting half the amount to the input and the other half to the output net, generates the dashed curve. As only half the amount is connected to the output net, the pole movement is quite good, but not so far towards lower frequencies as if all the capacitance

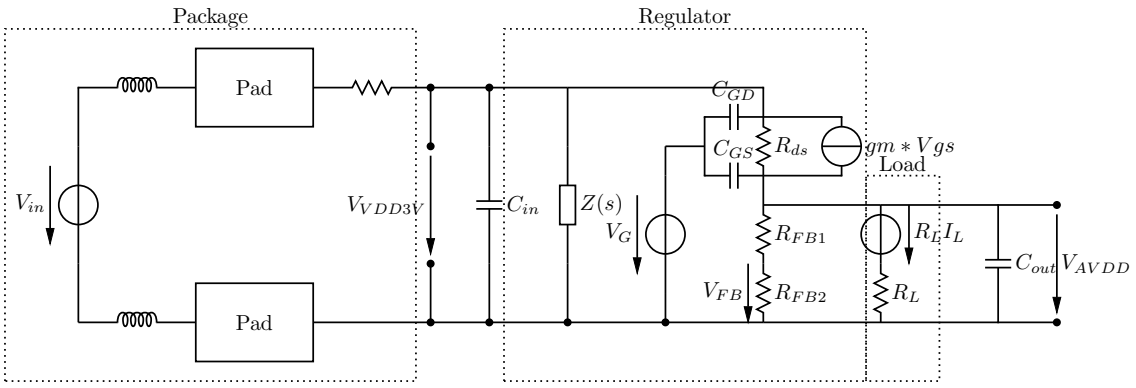

Fig. 3. Complete testbench for calculation

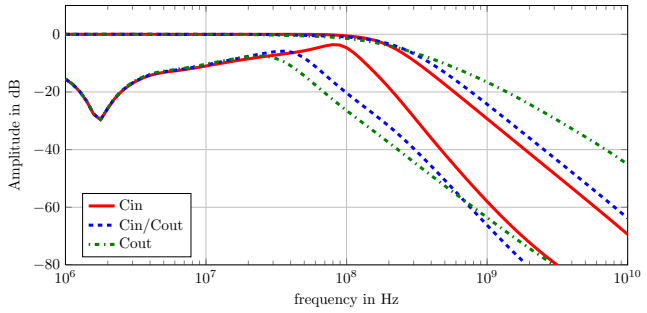

Fig. 4. Effect of FSC to VDD3V and AVDD

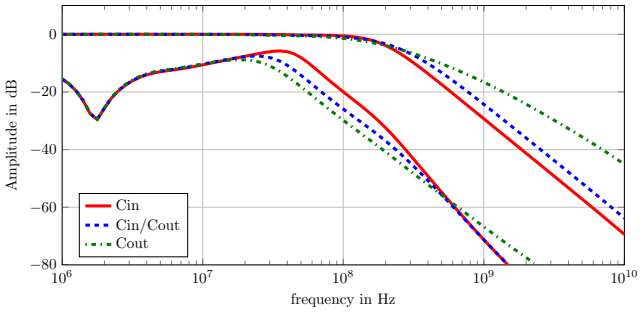

Fig. 5. Effect of FSC plus add. cap to VDD3V and AVDD

is connected to the output net. The additional shift of the input net pole towards lower frequencies by the connection of the 2nd half of the capacitance to the input net, helps to improve the frequency behavior of the regulator at higher frequencies. So splitting could be called the best solution as in mid-frequency range it already damps very well and at high frequencies shows the best damping.

Another point of interest is shown in Fig.5, where again the frequency behavior of *AVDD* and *VDD3V* is shown. The changed parameter now is again the capacity, in this case not only for the additional FSC, but rather for the FSC and a fixed capacitor at the output net. Often a capacitor is installed at the output net for e.g. better transient behavior or stability. There also the question arises where to best connect the additional FSCs.

Again the diagrams were plotted for three cases: All capacitance at the input net (solid curves), all at the output net (dashed-dotted curve) and a half-half split of the capacitance(dashed curve).

For the net *AVDD* (lower 3 curves) the best mid frequency behavior is again reached by connecting all capacitance to the output net. But then the high frequency behavior is very bad because of the missing early pole on the net *VDD3V* (upper 3 curves), which supplies the regulator. Connecting all the capacitance to the input net leads to very bad mid frequency behavior, but a better high frequency behavior as if connecting all capacitance to the output. This is due to the earlier pole in *VDD3V*. With splitting the capacitance, the mid frequency behavior is lying between the two other cases but is not much worse as if connecting all FSC to the output. But with split FSCs, AC behavior of net *AVDD* profits from the *VDD3V* pole and therefore shows the same high frequency behavior as if connecting all the FSC to the input. So splitting is again the best solution.

Simulations show that splitting is best as long as splitting can create an allover ratio of 1 : 1 for all the capacitance at the input net to all the capacitance at the output net. If the output capacitance is greater than the free-space capacitance at all, the best solution is connecting all FSC to the input net.

In the diagrams in Figs. 4 and 5 the shape of AC response is only visible in the range between 1 MHz and 10 GHz. In Fig.6 the complete shape is visible for the configuration with a constant capacitance and the free-space capacitance.

What is investigated in the upper and lower curves of Fig.6 is the influence of the bandgap to the regulator. In the lower curves, the bandgap voltage and especially the bandgap currents are kept constant while in the upper curves, the bandgap voltage and currents are that of the simulated transistor circuit. The influence is clearly visible especially at very low frequencies, where the difference is about 20 dB.

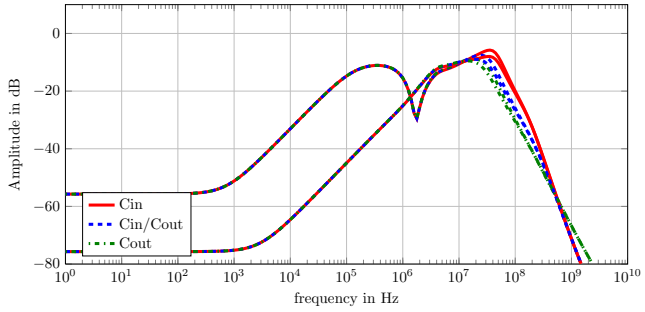

Fig. 6. Influence of bandgap to AVDD

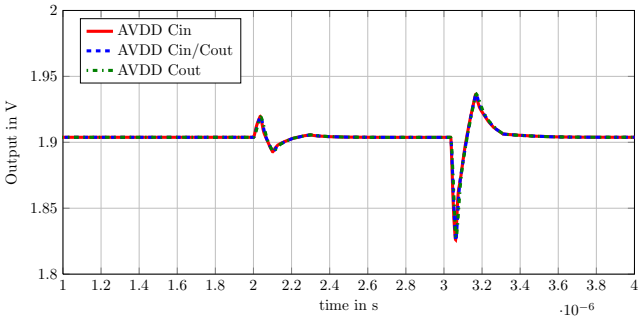

Fig. 7. Transient behavior of AVDD at load change

This simulation is done to prove the necessity to damp the input net, as the bandgap, the operational amplifier and the regulation transistor are connected to that net and so a damping on that net helps improving the output net very much. The diagram also shows that the values of the free-space capacitors are too small to damp the low frequencies where the PSR distortion from bandgap reaches the output net in the range from DC to about 1 MHz.

So far, all the simulations only cover AC behavior and point out how the FSCs influence the frequency behavior. When simulating the transient behavior of load changes, the effects are only very small on the nets *AVDD* (see Fig.7) and *VDD3V*. As it can be seen in the diagram, the effect of a load change at the output is almost the same, independent to which net the FSC is connected. The explanation for this effect is that the charge, stored on the capacitor, is very small as the capacitor itself is very small. Therefore the capacitor could only stabilize the voltage for a very short time before the voltage on the capacitor drops together with the output voltage.

4 Conclusions

In this work, we show that it is possible to improve PSR effects of LDOs by the application of FSC during post-layout optimization. We especially point out that FSCs placed half by half to the input and output net of a LDO improve AC performance more than just adding them to one of the two nets. If the LDO already has an output capacitor installed, the best solution is to add capacitance to the input net till the input and output nets have the same amount of capacitance and split the rest of the capacitance.

Splitting the capacitance shifts the main poles of input and output net towards lower frequencies, decreasing PSR effects in mid-frequency range with the output capacitance and in high-frequency range with the input capacitance. It is worth mentioning that due to the small capacitance, placed into the rare free space, the damping AC effects on the output net are also only very small. An additional free-space capacitor also does not have a significant effect on transient load changes.

This work emphasizes, that in contrast to other work, where the focus is on changes in error-amplifier or improvement of control loop, a simple, well understood design can still be improved if the cooperation between design and layout is excellent and all space on the expensive ASIC is utilized.

Therefore the analog designer should already pay attention to post-layout optimization opportunities during design of the circuit to advise layouter where to connect free-space capacitors. An important instrument to fulfill that job is the creation of a proper testbench, containing next to most of the parasitic elements also opportunity devices for post-layout optimization. These could be ideal devices with an estimated value of FSCs which are later replaced by PDK (process developent kit) devices where the real value is back-annotated. This approach is legitimately if the regulator is stable with and without the FSCs and just improved by additional input or output capacitance.

Nevertheless a simulation with extracted parasitics from layout needs to be done in every case.

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