Design of Relaxation Digital-to-Analog Converters for Internet of Things Applications in 40nm CMOS

Design of Relaxation Digital-to-Analog Converters for Internet of Things Applications in 40nm CMOS

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***Abstract*—A 10-bit-400kS/s and a 10-bit-2MS/s Relaxation Digital to Analog Converters (ReDAC) in 40nm are presented in this paper. The two ReDACs operate from a 600mV power supply, occupy a silicon area of less than $1,000\mu m^2$. The first/second DAC achieve a maximum INL of 0.33/0.72 LSB and a maximum DNL of 0.2/1.27 LSB and 9.9/9.4 ENOB based on post-layout simulations. The average energy per conversion is less than 1.1/0.73pJ, corresponding to a FOM of 1.1/1.08 fJ/(conv. step), which make them well suited to Internet of Things (IoT) applications.**

***Index Terms*—Relaxation Digital to Analog Converter (ReDAC), Digital to Analog Converter (DAC), Fully Synthesizable DAC, Ultra Low Power, Internet of Things.**

I. Introduction

Traditional analog design techniques are generally unsuitable to address the tight requirements of ultra-low power, ultra-low voltage operation, low cost and design effort of interfaces for Internet of Things (IoT) applications and mostly digital solutions and IC design approaches suitable to replace conventional analog and mixed signal circuits are therefore intensely investigated in the last years [1-2].

Focusing on digital-to-analog converters (DACs), which are key building blocks in themselves and also as part of analog-to-digital converters (ADCs), topologies based on weighted capacitors arrays [3-5] are in general extremely energy efficient but can be sensitive to parasitics and have in general stringent matching requirements, which may result in increased total capacitance (with a penalty in energy and area), design time and layout effort. An analog intensive design is also required for multi-bit sigma-delta ($\Sigma\Delta$) DACs [6], while single $\Sigma\Delta$ and dyadic DACs are fully digital and matching insensitive, but operate either at high clock frequencies or require large passive components unsuitable to integration [7-8].

Recently, the Relaxation Digital to Analog Converter (ReDAC) has been proposed in [10] as a low-cost alternative for bitstream data conversion in ultra-low voltage, tightly energy constrained IoT applications and has been demonstrated by a field-programmable gate array (FPGA) proof-of-concept prototype.

In this paper, the design of two fully synthesizable ReDACs in 40nm CMOS is discussed and their performance is demonstrated by post-layout simulations. The paper has the following structure: the principles and main features of ReDACs are revised in Sect.II. Then, in Sect.III, the design of the converters is addressed focusing on the tradeoffs and on the optimization of passives to obtain the best energy-accuracy tradeoff. In Sect.IV, the performance of the ReDACs is discussed based on post-layout simulations. Finally, in Sect.VI, some conclusions are drawn.

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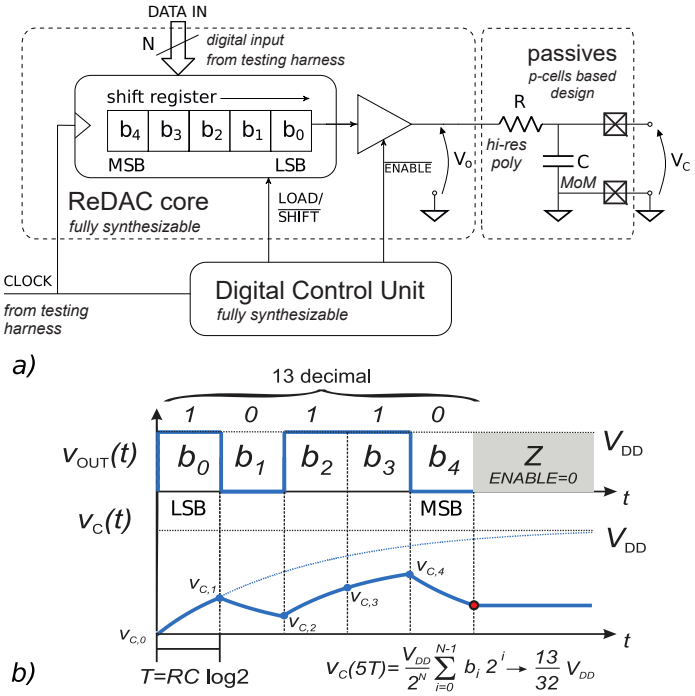

Fig. 1. Relaxation DAC Block Diagram (a) and principle of operation (b)

II. Relaxation Digital-to-Analog Conversion Concept and Features

The ReDACs proposed in this paper exploit the impulse response of an RC network as a mean to generate binary weighted voltages and sum them up according to the digital input

$$n = \sum_{i=0}^{N-1} b_i 2^i, \tag{1}$$

to be converted. The ReDAC operation principle and its main features, which have been described in [10], are shortly revised in what follows.

A. Relaxation DAC Operation Principle

A ReDAC includes a first-order RC network driven by a three-state digital buffer, as depicted in Fig.1a. When enabled, the buffer drives the RC network by a sequence of N rectangular pulses of the same duration T and amplitude $V_{\rm DD}b_i$, which is equal to $V_{\rm DD}$ or 0V, depending on the logical value of the N bits b_i of the digital input n to be converted, starting from the least significant bit (LSB) b_0 up to the most significant bit (MSB) b_{N-1} as in Fig.1b. This is easily accomplished in practice by driving the input of the buffer by an N-bit shift register loaded by the input n to be converted.

The operation of the circuit in Fig.1a as a D/A converter can be explained considering that the evolution of the capacitor voltage $v_{\rm C}(t)$ during the i^{th} time interval $[(i-1)T, iT]$ can be expressed as a function of the initial capacitor voltage at the beginning of the interval, i.e. $v_{{\rm C},i-1} = v_{\rm C}(t)|_{t=(i-1)T}$, of the steady-state voltage $v_{{\rm C},i}(\infty)$, which is $V_{\rm DD}$ for $b_i = 1$ and 0V for $b_i = 0$, and of the time constant $\tau = RC$, as

$$v_{\rm C}(t) = v_{{\rm C},i}(\infty)\left[1 - {\rm e}^{-\frac{t-(i-1)T}{\tau}}\right] + v_{{\rm C},i-1}{\rm e}^{-\frac{t-(i-1)T}{\tau}} \quad (2)$$

Assuming $v_{{\rm C},0} = v_{\rm C}(0) = 0$ as a reset condition, (2) can be iterated to express $v_{{\rm C},i}$ for $i = 1 \ldots N-1$ in function of $V_{\rm DD}$, b_i and τ and the capacitor voltage after N clock periods can be finally expressed as:

$$v_{\rm C}(NT) = V_{DD}\left(1 - {\rm e}^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{N-1} b_i {\rm e}^{-\frac{(N-i-1)T}{\tau}}. \quad (3)$$

Based on (3), if T is chosen so that:

$${\rm e}^{-\frac{T}{\tau}} = \frac{1}{2} \qquad \Longrightarrow \qquad T = \tau \log 2 \quad (4)$$

by substituting condition (4) in (3)

$$v_{\rm C}(NT) = \frac{V_{\rm DD}}{2^N} \cdot \sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N} V_{\rm DD}, \quad (5)$$

i.e., it follows that $v_{\rm C}(NT)$ is proportional to the binary input value n expressed by (1), as demanded in D/A conversion. The capacitor voltage $v_{\rm C}(NT)$ is finally held constant by releasing the enable signal of the three-state buffer.

B. Relaxation DAC Features

Based on the results presented in [10], a ReDAC is particularly appealing for low cost, low power IoT systems. Unlike in binary weighted capacitors array DACs [3-4], in fact, it requires a single capacitor and its linearity is not affected by matching. In view of that, a ReDAC can be extremely area and energy efficient since the minimum capacitance C is not constrained neither by matching nor by the minimum unit capacitance available in the process design kit (PDK).

Moreover, the ReDAC linearity depends on the single process-sensitive quantity T/τ and the worst case integral nonlinearity error (INL), expressed in least significant bits (LSBs) has been found to be

$${\rm INL}_{\rm max} \simeq 2^{N-1} \log 2 \cdot \frac{\Delta T}{T} \quad (6)$$

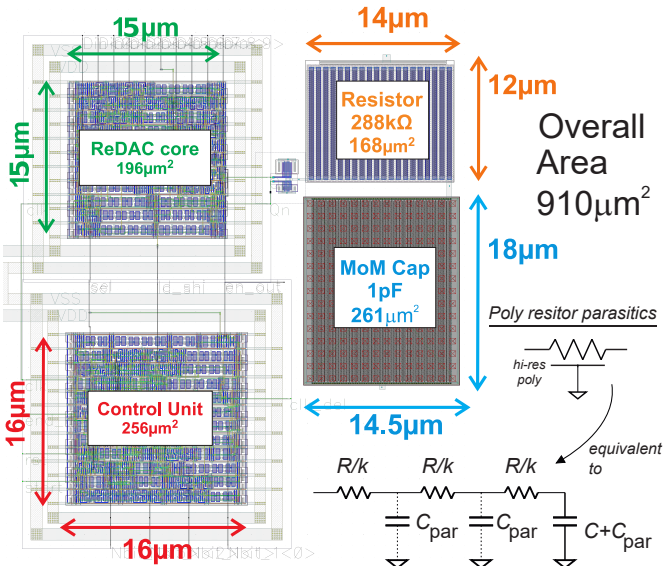

Fig. 2. Poly resistor parasitics and layout of the ReDAC design #1.

where ΔT is the error in the clock period T compared to the requirement (4) for ReDAC operation.

Since time intervals, unlike voltages, currents and active/passive component parameters, can be finely controlled and tuned with a high resolution and the value of T required to meet condition (4) can be conveniently enforced by the digital dichotomic calibration procedure presented in [10], a ReDAC can easily achieve a resolution exceeding 10 bits and is particularly well suited to IoT applications.

III. ReDAC Design in 40nm CMOS

The design of two 10-bit ReDACs in 40nm CMOS targeting 400kS/s sample rate and best accuracy (design #1) and 2MS/s sample rate (design #2) is now addressed. Both the ReDACs include a digital core, a control unit and an integrated RC network, as in the block diagram of Fig.1a, and are assumed to be operated by a clock signal with a period T calibrated by the dichotomic procedure presented in [10] so that to enforce condition (4) (the calibration procedure will not be considered hereafter). The design of the RC network and of the digital blocks is discussed in what follows.

A. RC Network Design

In both the ReDACs, the capacitor of the RC network is implemented by a Metal-oxide-Metal (MoM) capacitor available in the PDK. Since there is no matching requirement in a ReDAC converter, a capacitance C close to the limit dictated by thermal noise to keep the 3σ value of the $\kappa T/C$ noise below 1/2 LSB, i.e.:

$$C_{\rm min} \simeq 9 \cdot 2^{2N+2} \kappa T / V_{\rm DD}^2 \quad (7)$$

can be chosen to minimize the silicon area and the energy per conversion. At 10 bit resolution and 0.6V supply voltage, based on Eqn.(7), $C_{\rm min} = 436$fF. A capacitance of C=1pF, i.e. nearly twice $C_{\rm min}$, is therefore chosen in the ReDAC design

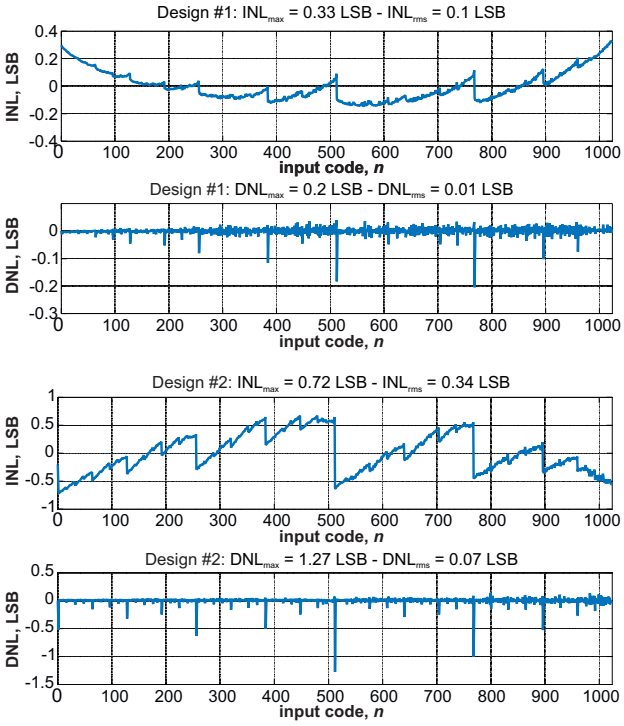

Fig. 3. Integral nonlinearity error (INL) and differential nonlinearity error (DNL) of design #1 and desing #2 obtained by post-layout simulations.

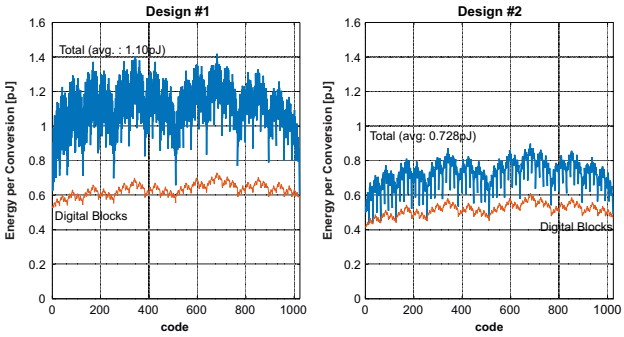

Fig. 4. Energy per conversion versus input code

#1 to make the thermal noise contribution negligible, while a capacitance of C=450fF, close to the thermal noise limit, is chosen for ReDAC #2.

The resistor R is implemented by high-resistivity (HiRes) polysilicon resistors in the PDK and its resistance value R is designed for a target time constant, based on the capacitance values C derived above, as

$$R = \frac{\tau}{C} \tag{8}$$

where the target value of τ is related to the bit time T by (4), and is in turn related to the target sample rate of the circuit, being

$$T_{\text{conv}} = (N+2)T = (N+2)\tau \log 2 \tag{9}$$

where N is the number of bits and a $2T$ hold phase is assumed. Based on (9) and (8), a resistance $R = 288\text{k}\Omega$ is chosen

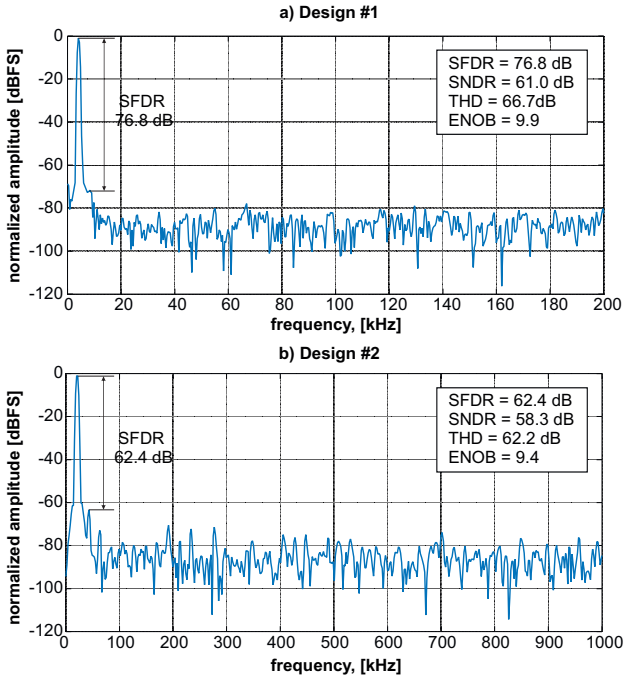

Fig. 5. Spectrum of the DACs output (sampled in the hold phase) and dynamic parameters: a) design #1 at 3.4kHz sine wave input 90% full-swing amplitude; b) design #1 at 16.8kHz sine wave input 90% full-swing amplitude.

in design #1 for a 400kS/S sample rate and a resistance of $R = 128\text{k}\Omega$ is chosen in design #2 for a 2MS/s sample rate.

In practice, two more contrasting requirements need to be considered in the choice of R to avoid accuracy degradation. First, R should be much larger than the output impedance of the buffer in Fig.1a so that to avoid nonlinear loading effect; second, the total distributed parasitic capacitance of R highlighted in Fig.2 should be negligible compared to C at the target resolution ($\sim 2^N$ times less) to have a true first-order RC response, as demanded for the validity of the analysis in Sect.II. Since the absolute value of the resistance is not critical in a ReDAC and it can be compensated by period T calibration [10], the physical width of the poly resistor has been set to the minimum allowed by the PDK to reduce the distributed capacitance. Moreover, the loading effect and the parasitics have been verified to be negligible for the resistance values considered in the design.

B. Digital Core and Control Unit Design

The 10-bit shift register ReDAC core and the control unit finite state machine (FSM), which generates the LOAD/$\overline{\text{SHIFT}}$ and $\overline{\text{ENABLE}}$ signals according to the timing in [10], are both synthesized in standard cell logic starting from a behavioral Verilog description. Both the netlist and the layout view have been automatically generated in a standard digital flow.

The strength of the three-state buffer driving the RC circuit has been manually constrained to be 6X the minimum, which has found to be a good compromise for a low output impedance, resulting in a negligible loading effect, and for negligible charge injection and leakage during the hold phase.

IV. Post-Layout Simulation Results

The designed ReDAC circuits occupy a silicon area of $910\mu\mathrm{m}^2$ and $677\mu\mathrm{m}^2$, respectively (layout of design #1 is shown in Fig.2) and have been characterized under static and dynamic conditions by post-layout simulations including the transistor-level extracted views and all the parasitics of the RC network and of the digital blocks.

The static characterization of the ReDACs reported in Fig.3 reveals a maximum (rms) INL of 0.33 LSB (0.1 LSB) and a maximum (rms) DNL of 0.2 LSB (0.01 LSB) for design #1, while for design #2 the maximum (rms) INL is 0.72 LSB (0.34 LSB) and the maximum (rms) DNL is 1.27 LSB (0.07 LSB).

The energy per conversion for each input code is reported in Fig.4. The average energy per conversion is 1.1pJ for design #1 and 730fJ for design #2 and in both cases the energy absorbed by the digital blocks (i.e., excluding the energy delivered to the RC network) accounts for more than 50% of the total energy, due to the low capacitance C and to the intrinsic energy efficiency of the ReDAC.

The operation of the ReDACs under dynamic conditions has been simulated for a sine wave input with amplitude of 90% of the input swing and with frequency $f_0 = 1/(124T_{\mathrm{conv}})$, which corresponds to 3.4kHz for design #1 and to 16.8kHz for design #2. The spectra of the output, sampled in the hold phase of the ReDAC, are reported in Fig.5 and reveal, for design #1, an SFDR of 76.8dB, a THD of 66.7dB and a SNDR of 61dB, corresponing to 9.9 effective bits (ENOB). From the same figure, design #2 achieves an SFDR of 62.4dB, a THD of 62.2dB and a SNDR of 58.3dB, corresponding to 9.4 ENOB.

Based on Montecarlo simulations performed on 100 samples, it has been found that, keeping T constant, errors due to process variations in R and C affect the accuracy of the converter as expected from (6). By the way, it has been verified that the nominal accuracy can be always fully recovered by performing the calibration procedure described in [10] to re-enforce (4) under process-related variations of τ.

The simulated ReDACs performance is summarized in Tab.I. As expected, the 40nm ReDACs achieve strongly improved performance in terms of sample rate, static and dynamic linearity compared to the FPGA prototype considered in [10]. Moreover, compared with the capacitive DAC in the SAR ADC in [4], where the DAC energy contribution has been extrapolated based on the ADC energy breakdown for fair comparison, the proposed ReDACs show more than 10X lower feature-size normalized area and a 2.3X lower figure of merit (FOM), expressed in energy per conversion per steps. Further energy improvements can be expected by the optimization of the logical blocks for low power consumption.

TABLE I
DAC Performance Comparison

	Units	**[5]**[c]	**[10]**	**This work #1**	**This work #2**
Type		C-DAC	ReDAC	ReDAC	ReDAC
Valid.		Meas.	Meas.	Sim.	Sim.
Techn.	nm	180	FPGA	40	40
Supply	V	0.6	1.8	0.6	0.6
R[a]	kΩ	N/A	100	288	128
C[a]	pF	9.2[d]	2,200	1	0.45
Area	$\mu\mathrm{m}^2$	163,000	N/A	910	677
Norm. Area	$10^6 \cdot F^2$	5.03	N/A	0.5	0.3
Resolution	bit	10	10	10	10
Sample Rate	kS/S	20	0.3	400	2,000
$\mathrm{INL}_{\mathrm{max}}$	LSB	0.46[c]	2.4	0.33	0.72
$\mathrm{INL}_{\mathrm{rms}}$	LSB	N/A	0.9	0.10	0.34
$\mathrm{DNL}_{\mathrm{max}}$	LSB	0.44[c]	3.3	0.2	1.27
$\mathrm{DNL}_{\mathrm{rms}}$	LSB	N/A	0.62	0.01	0.07
SNDR[b]	dB	58.3[c]	43.27	61.0	58.3
SFDR[b]	dB	67.7[c]	51.36	76.8	62.4
THD[b]	dB	N/A	47.52	66.7	62.2
ENOB[b]	bit	9.4[c]	7.13	9.9	9.4
En./conv. Tot./Analog	pJ	1.7[c]/1.3	N/A	1.1/0.47	0.73/0.21
FOM	fJ/(c·s)	2.49[c]	N/A	1.1	1.08

[a] for ReDAC only; [b]best reported @ 90% swing . sine input.
[c]CDAC performance estimated from the ADC characterization, CDAC energy estimated from ADC energy and power breakdown.
[d]Total CDAC capacitance.

V. Conclusions

The design of two 10-bit ReDACs with 400kS/s and 2MS/s sample rate operating at 600mV power supply in 40nm has been proposed. Based on post-layout simulations, the ReDACs achieve a maximum INL of 0.33/0.72 LSB, a maximum DNL of 0.2/1.27 LSB and a 9.9/9.4 ENOB effective resolution under sine wave input, significantly outperforming the previous ReDAC FPGA-based proof-of-concept prototype. Both the circuits occupy a silicon area of less than $1,000\mu\mathrm{m}^2$ and show an extremely competitive FOM of 1.1/1.08 fJ/conv.step., which make them well suited to IoT applications.

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