Advances in Radio Science (2003) 1: 289–293

Advances in Radio Science

A new BIST scheme for low-power and high-resolution DAC testing

H. Li[1], **J. Eckmueller**[1], **S. Sattler**[2], **H. Eichfeld**[1], **and R. Weigel**[3]

[1]SMS TI MT MS, Infineon AG, Postfach 80 09 49, D-81609 München, Germany
[2]CTT TS ADT, Infineon AG, Postfach 80 09 49, D-81609 München, Germany
[3]Lehrstuhl Technische Elektronik, Friedrich-Alexander-Universität Erlangen-Nürnberg, Cauerstr. 9, 91058 Erlangen, Germany

Abstract. A BIST scheme for testing on chip DAC is presented in this paper. We discuss the generation of on chip testing stimuli and the measurement of digital signals with a narrow-band digital filter. We validate the scheme with software simulation and point out the possibility of ADC BIST with verified DAC

1 Introduction

Due to the increasing complexity of electronic systems and the capabilities of very deep sub-micron technologies, in recent years more and more system functionality has been integrated onto a single chip (SoC). Consequently an increasing number of chips that combine digital and analogue functions is designed. High-performance applications of mixed-signal (MS) integrated circuits (IC's) in many areas such as wireless telecommunications, data exchange systems and satellite communications have been realized. But this development makes big challenge on the testing of Mixed-signal circuits for such applications is more and more difficult, because it becomes both expensive and time consuming. Then an attractive alternative for the Mixed-signal testing is the Built-in Self-Test (BIST) approach in which testing (test generation and test application) is accomplished through built-in hardware features. Recently, several BIST concepts for DA and AD converters were proposed. In Toner and Roberts (1995), the authors proposed a BIST approach for testing the SNR of a delta-sigma ADC. This method employs a sine wave generator based on delta- sigma technique and digital signal processing techniques for data analysis. But the technique needs both on chip ADC and DAC, and powerful computation ability on chip, which is not always possible. The BIST approach in Sunter and Nagi (1997) refers to approximating the transcharacteristic of an ADC with the best fitting a 3rd order polynomial. Then the offset, gain, and harmonic distortion will be computed out from this polynomial. Its drawback is that it is very sensitive to the noise level and needs also a powerful DSP-core on chip. By the oscillation test method proposed in Arabi and Kaminska (1996), test vector generation problem is eliminated and the test time is very small. Nevertheless, the impact of control logic delay and the imperfect analog BIST circuitry on the test accuracy are not clear. In Azaies et al. (2000), the authors present a histogram BIST method for ADC, which shows how many times each different digital code word appears on the outputs. Because ADC errors will modify the output code count and so impact the histogram shape, offset, gain, DNL and INL can be extracted from the results. However, the number of input patterns is so huge that the testing time is much longer than that in other methods. The work in Ohletz (1991) proposes a BIST approach for testing DAC-ADC pair with a Pseudo-Random Bit Sequence (PRBS) generated by a Linear-Feedback Shift Register (LFSR) as stimulus and a second LFSR, which compacts the digital output of the ADC to generate a signature compared to a value stored in memory. The drawback is again the need of a powerful DSP core on chip. And all the above methods are devoting either to the testing of ADC or to the testing of ADC-DAC pair. In Hajjar and Roberts (1998), the authors show a BIST method for testing a single DAC without ADC on chip based on IEEE 1149.4. It takes advantage of the period character of testing stimuli to trade the analog nature of the DAC output. Nevertheless, it is not suitable to the testing of high-speed and low voltage DAC because the testing time is too long and the requirement on the comparator is too fine to implement on chip.

Our work is concerned with an improved BIST scheme for the testing of a high-speed and low voltage DAC. By this work, we use a full digital way to produce a sine wave with a good Signal-to-Noise Ratio (SNR). Since we do not relay on the on chip ADC and DAC to produce our testing stimuli, our BIST strategy does not need the presence of on chip ADC and DAC at the same time, which means our approach is more feasible and flexible. For DAC testing, we employ the one-points-multi-comparison algorithm

Correspondence to: H. Li
(hongzhi.li@ieee.org)

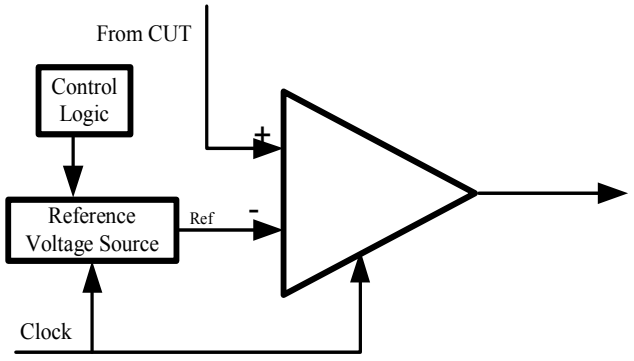

Fig. 1. On-Chip Digitizer.

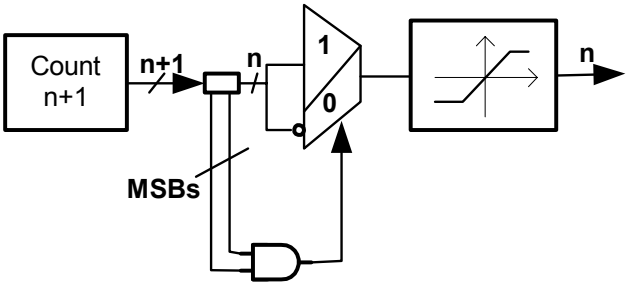

Fig. 2. Trapezoid Wave Generator.

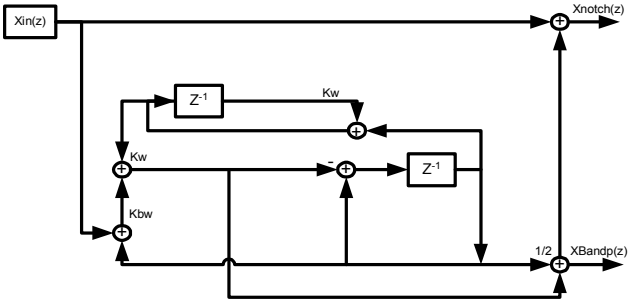

Fig. 3. Digital Notch Filter.

instead of multi-points-one-comparison algorithm in Hajjar and Roberts (1998). Moreover, we apply two-step comparison to decrease the requirement of the comparator resolution.

For the evaluation of the digitized signal, we use a digital notch filter to separate the signal from noise, which is based on an approach for on chip time recursive implementation of an arbitrary transform described in Padmanabhan and Martin (1993). Thus we can avoid the application of a DSP on chip, which makes our proposal more comm.

This paper is organized as follows. The method in Hajjar and Roberts (1998) and some discussion about it are presented briefly in Sect. 2. Then, we introduce some preliminaries of our work. The BIST approach we use for on chip DAC testing is present in Sect. 4. Simulation results are shown in Sect. 5 to demonstrate our ideas. We conclude the work in Sect. 6.

2 Present DAC BIST method

In Hajjar and Roberts (1998), an on chip signals extractor is presented. The extractor consists of a single comparator and a robust on chip reference voltage generator. Subampling technique is used to enable the capture of analog waveforms using a single comparator clocked appropriately (Fig. 1). Arbitrary amplitude resolutions are achieved by varying the reference comparison level input to the comparator, Vref, which is held constant for a duration equal to the time it takes the comparator to compare all samples of the UTP (Unit Testing Period) to this reference level. Once all comparisons are made, Vref is incremented to the next quantization level, and the process is repeated.

However, this technique can not be used for the high-resolution and low voltage DAC. For instance, for a 16 bits DAC with the full scale of 3.7 V (+1.85 V ~ -1.85 V), whose least significant bit (LSB) is 56 uV, if the testing signal is a 1 kHz sine waveform (a typical situation for the testing of voice-band chip), the testing time will be at least 1 ms $\times$ 2^{16}= 65.536 s, and that does not include the time for post-processing. Besides this, the amplitude resolution of the comparator will be half the LSB, namely 28 uV. Both of these terms are no good specification for our testing and design. We must make some improvement in order that we can employ such similar structure to the applications with high resolution and low supply voltage on chip.

3 Preliminaries

3.1 Testing stimuli generation

For the generation of testing stimuli, we use the following method. Every periodic waveform $f(x)$ can be expressed by a Fourier series, which is an infinite sum of sine and cosine waveforms (Oppenheim and Schafer, 1989). When a filter is used to attenuate higher harmonics, a sinusoidal waveform with the same period wave will be obtained at the output. Because the trapezoid wave has very good transition band character, if its discrete period is a multiple of 6, we will employ such a trapezoid wave by saturating a triangular wave to generate our testing stimuli (Fig. 2). After downsampling the frequency to decorrecelate the sampling and generated frequency, the signal is fed into a low pass filter (LPF) to filter out the harmonic frequencies (Crochiere and Rabiner, 1983) so that we get a sinewave, which is lastly interpolated to the frequency of the DAC under test.

3.2 Delta-Sigma modulation based reference voltage generator

For reference voltage generator in Fig. 1, we employ the delta sigma modulation based approach proposed in Hawrysh and Robert (1996). A software delta-sigma modulator converts the desired signal into a 1-bit stream. Then this bit stream

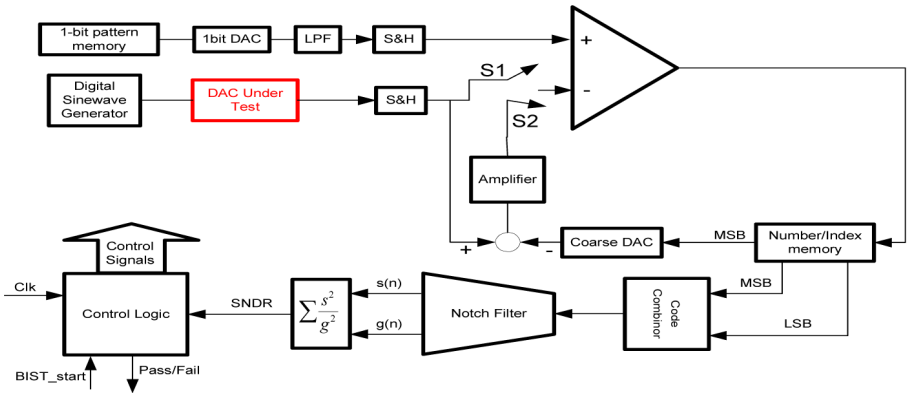

Fig. 4. The BIST scheme.

is transmit into a 1-bit DAC which is followed by an analog low pass filter. The LPF attenuates the out-of-band high-frequency modulation noise and therefore restores the original waveform. In our implementation, we extract a set of points from the bit stream which contains an integer number of signal periods under the terms of some criteria, since the bit stream of a periodic signal is even not a periodic one. Then we store it in the on chip memory, which is applied to 1-bit DAC and low-pass filter periodically to generate the desired signal.

3.3 SNDR estimation via digital notch filter

The standard industry method of SNR measurement involves taking an FFT of the digitized signal. But it needs a DSP core on chip, which is not always possible by BIST for mixed-signal circuit. We will give another approach – digital narrow band method – proposed in Padmanabhan and Martin (1993). This filter showed in Fig. 3 has two outputs: one is band-pass output tuned to the desired signal frequency; another one is band-stop output including all the harmonic frequency and noise. $X_{in}(z)$ is the filter input, and $X_{bandp}(z)$ is the band-pass output, and $X_{notch}(z)$ is the band-stop output. If we note $A_2(z)$ as:

$$A_2(z) = \\ = \frac{k_{bw} + k_w + (1 + k_{bw})z^{-1} + z^{-2}}{1 + k_w(1 + k_{bw})z^{-1} + k_{bw}z^{-2}} \quad (1)$$

Then we can get the following equation:

$$H_{notch}(z) = \frac{X_{notch}(z)}{X_{in}(z)} = 1 + A_2(z)$$
$$H_{bandp}(z) = \frac{X_{bandp}(z)}{X_{in}(z)} = 1 - A_2(z) \quad (2)$$

where k_w and k_{bw} are determined by the desired frequency f_0 and 3 dB bandwidth $\omega_{3\,\mathrm{dB}}$:

$$K_w = -\cos(2\pi f_0 T)$$
$$K_{bw} = \frac{1 - \tan(\frac{w_{3dB}}{2})}{1 + \tan(\frac{w_{3dB}}{2})} \quad (3)$$

The narrow band filter is connected to the output of on chip digitizer. If $s(n)$ is the digital sequence of band-pass output and $g(n)$ is the sequence of band-stop output, then the SNDR of input is given by:

$$SNDR = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_g^2}\right) = 10\log_{10} \\ \left(\frac{\frac{1}{M-1}\sum_{n=1}^{M}(s(n))^2}{\frac{1}{M-1}\sum_{n=1}^{M}(g(n))^2 - \frac{1}{M(M-1)}\sum_{n=1}^{M}(g(n))^2}\right) \quad (4)$$

Mathematically, it has been demonstrated that this SNDR can be used as a preliminary estimate of the desired SNDR.

3.4 Two steps AD conversion technique

By AD conversion, the two steps AD conversion technique is usually used when the resolution requirement is too small. This two-steps architecture consists of a sampling-and-hold circuit, a coarse flash ADC, an analog substractor, a fine ADC, a DAC stage and a digital bits-combinator. By two-step testing, first the S&H tracks the analog input and holds it for coarse conversion and subtraction operation. Then the coarse flash ADC makes a coarse digital estimate of the analog input (discrete-time signal) to yield a small voltage range around the input level. The DAC stage converts this digital estimate into an analog signal, which is deducted from the original analog signal through the substractor. The fine ADC subsequently digitizes the residue signal. Lastly the digital outputs of the coarse ADC and fine ADC are combined to the final output.

4 The New BIST Scheme

The overall BIST topology for the proposed DAC BIST scheme is depicted in Fig. 4. The required functional blocks and control signals are as following (assuming that the full-scale voltage of Mbits-DAC is 2Vref):

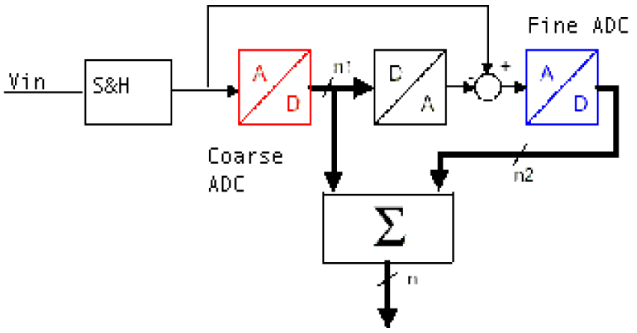

Fig. 5. Two-step conversion.

- 1-bit pattern memory, 1-bit DAC and LPF together produce the reference voltage, which rise from −Vref to +Vref with 2^M small stages and each stage lasts UTP/2^M.
- Digital Sine wave generator generates a digital sinus stimulus using the method we have introduced in Sect. 3.
- The two S&H before the comparator resample the signal with coherent sampling technique (Mahoney, 1988) in order that the DAC output will hold constant while the reference voltage rises through the full scale, which is on the contrast to Hajjar and Roberts (1998), because the testing signal in our application is 1 kHz.
- Notch filter and SNDR meter are the signal evaluation systems on chip.
- Control logic controls the BIST processing and gives the testing result out.
- Comparator, Code/Index memory, coarse DAC, amplifier and substractor build up a two step conversion unit. In fact, we employ a switched-capacitor ADC reported in Song and Lee (1990) to eliminate coarse DAC, substractor, S&H and amplifier.
- Switch S1 and S2 control the comparison step. By coarser comparison, S1 close and S2 open: while by fine comparison, S2 close and S1 open.

5 Simulation results

To validate the proposed technique, we perform numerical simulation by applying the sine wave signal to DAC under test. Our DAC is a 16 bit DAC (13 effective bits) with the full scale voltage of 3.7 V. The testing frequency is 1 kHz with a peak to peak voltage of 3.7 V, too. Thus the SNR of our testing stimuli must be not less the SNR of our DAC, which is 6.02×(13+2) + 1.76 dB = 92.06 dB according to Norsworthy et al. (1997). The testing points must be not less than 2^{14} = 16384. If we test so many points within

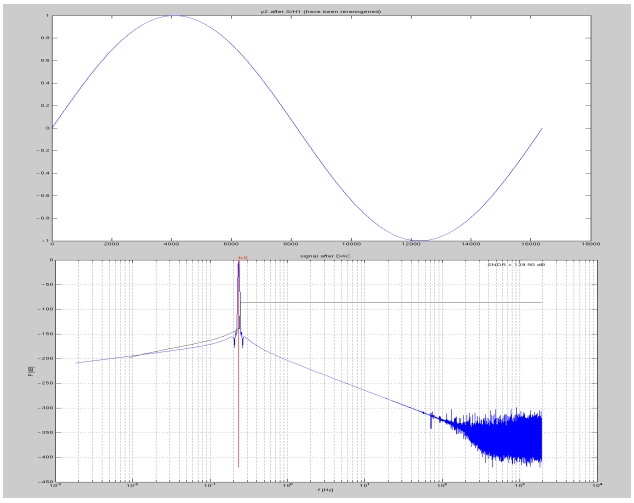

Fig. 6. Simulation on Sinewave Generator.

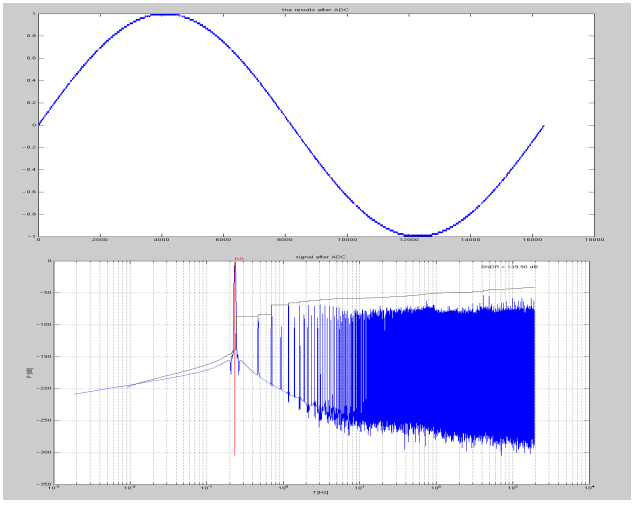

Fig. 7. Simulation on BIST scheme.

1001 testing periods. Therefore, the total testing time is 1 ms × 1001 = 1001 ms = 1.001 s. Without two steps multi-level comparison, we should complete each comparison in $1.001/(2^{14}\times 2^{14})\ s = 3.73$ ns, and the min. voltage resolution of comparator is $3.7/2^{14}\times 2^{14}$ V = 0.55 mV. That is a big challenge for design and layout. For two steps, the coarse comparison takes place firstly (get the MSB of the "ADC") and then LSB will be worked out through the fine comparison. The coarse and fine multi-level comparison times are both 2^7, thus the comparison time for each level is $1.001/(2^{14}\times 2\times 2^7)$ s = 238.67 ns, and the voltage resolution of comparator is $3.7/2^7$ V = 29 mV. This is obviously not a difficulty for design engineers.

First, we make a simulation on the digital sinus generator, which can achieve a SNDR over 110 dB (Fig 6.). Then we simulate the whole system in Matlab/Simulink (Fig. 7), and the simulation results demonstrate that our BIST method works very well.

6 Conclusion and discussion

We present a BIST scheme for testing on chip DAC. The main advantage are (1) it does not need the presence of a powerful DSP core on chip, (2) does not need both ADC and DAC on chip, and (3) can test low power and high resolution DAC. We also show how to get an accurate testing stimulus and how to evaluate digital signal without DSP on chip. And the simulation results verify our BIST scheme.

If there is ADC on chip and the resolution of DAC is better than that of ADC, we can test it with our verified DAC by connecting the their analog part together, then send digital signal to DAC and collect/analyze the output digital signal from the ADC.

Considering the difference between the ideal model under Matlab and the real situation, we are devoting to design a test chip for verifying our ideas further. Owing to the nonlinearly and mismatch of the capacitor by CMOS technology, we will first implement a 10 bits DAC BIST design. Moreover, future work involves also the development error model of BIST components and the research of their effect on final testing results.

Acknowledgements. This work has been funded within the AZTEKE project under label 01M3063A by the German Ministry for Education and Research (BMBF = Bundesministerium für Bildung und Forschung). Their support is gratefully acknowledged.

References

Arabi, K. and Kaminska, B.: Oscillation Built-in Self-test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits, IEEE Design & Test of Computers, Fall 1996.

Azaies, F., Bernard, S., Bertrand, Y., and Renovell, M.: Towards an ADC BIST Scheme using the Histogram Test Technique, IEEE European Test Workshop, Cascais, Portugal, May, 23–26, 2000.

Crochiere, R. E. and Rabiner, L. R.: Multi-rate Digital Signal Processing, Prentice-Hall Signal Processing Series, 1983.

Hajjar, A. and Roberts, W.: A High Speed and Area Efficient on-chip Analog Waveform Extractor", International Test Conference 1998, pp. 688–697, 1998.

Hawrysh, E. M. and Robert, G. W.: An integrated memory-based analog signal generation into current DFT architecture, Proc. Int. Test Conf., 1996, pp. 528–537, 1996.

Mahoney, M.: DSP based Testing of Analog and Mixed-signal Circuit testing, IEEE Computer Society Press, 1988.

Norsworthy, S. R., Schreier, R., and Temes, G. C. (Eds.): Delta-Sigma DataConverters: Theory, Design, and Simulation, New York IEEE Press, 1997.

Ohletz, M. J.: Hybrid BIST for Mixed Analogue/Digital Integrated Circuits, Proc. 1991 European Test Conference, pp. 307–316, April 1991.

Oppenheim, A. V. and Schafer, R. W.: Discrete-Time Signal Processing, Prentice-Hall Signal Processing Series, 1989.

Padmanabhan, M. and Martin, K.: Filter Banks for Time-Recursive Implementations of Transforms, IEEE Trans. Circuits and systems, 40, 1, 41–50, 1993.

Song, B. and Lee, S.: A 10b 15 mHz COMS recycling Two step ADC, IEEE J. Solid-State Circuit, 25, 6, 1328–1338, 1990.

Sunter, K. and Nagi, N.: A Simplified Polynomial-Fitting Algorithm for DAC and ADC BIST, International Testing Conference 1997, 389–395, 1997.

Toner, F. and Roberts, W.: A BIST SNR, gain tracking and frequency response test of a sigma-delta ADC, IEEE Trans. Circuits Syst. II, 42, 1–15, 1995.