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Editorial

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With the rapid growth of internet access and voice/data-centric communications, many access technologies have been developed to meet the stringent demand of high-speed data transmission and bridge the wide bandwidth gap between ever-increasing high-data-rate core networks and bandwidth-hungry end-user networks. To make efficient utilization of the limited bandwidth of existing access routes and cope with the adverse channel environment, many standards have been proposed for a variety of broadband access systems over different access environments (twisted pairs, coaxial cables, optical fibers, and fixed or mobile wireless access). These access environments may create different channel impairments and dictate unique sets of signal processing algorithms and techniques to combat specific impairments. In the design and implementation domain of those systems, many research issues arise.

Motivated by this design trend, the aim of this special issue is to present state-of-the-art signal processing techniques and implementation issues for broadband access systems over different access channels. We have selected nine high-quality papers covering the algorithm development, design, implementation, and application aspects of current and emerging wireline/wireless access technologies. In terms of technical contents, the nine papers can be loosely grouped into the areas of (1) efficient DSP algorithms for high-quality and secure data transmissions, and (2) implementation of DSP processing engines (e.g., FFT, FEC codec, and DSP core) for access-transceiver designs. These designs can be readily applied to emerging access systems such as xDSL, cable modem, FTTC, FTTH, 10G/Gigabit Ethernet, Bluetooth, wireless LAN, broadband wireless access, digital audio/video broadcasting, and so forth.

The first three papers focus on advanced DSP algorithm development. The first paper by Lakhzouri et al. considers the problem of line-of-sight (LOS) detection in WCDMA for mobile positioning. Mobile phone positioning in a cellular network with accurate position information has attracted great interest (e.g., FCC-E911 in USA and the coming E112 in the European Union). One method for locating the mobile station (MS) in two dimensions requires the measurement of LOS distance between the MS and at least three base stations. However, in many cases, the non-LOS (NLOS) signal components arrive with delay less than one chip at the receiver, thus obscuring the LOS signals. In this paper, the extended Kalman filter (EKF) is used to jointly estimate the delays and complex channel coefficients. The technique can provide an accurate decision whether LOS component is present or not, which is suitable for WCDMA receiver designs. The second paper by Martin et al. deals with the time-domain equalization (TEQ) algorithm that plays a crucial role in reducing intercarrier interference (ICI) and intersymbol interference (ISI) in multicarrier communication systems. This

paper analyzes two TEQ design methods for cost-effective real-time implementation: minimum mean squared error (MMSE) and maximum shortening SNR (MSSNR) methods, which can significantly reduce the computational complexity in performing channel shortening compared with existing TEQ approaches, without degrading performance. The third paper by H. C. Chen et al. proposes a new signal security system and its VLSI architecture for real-time multimedia data transmission applications. By defining first two bit-circulation functions for one-dimensional binary array transformations, the authors exploit a chaotic system in generating a binary sequence to control the bit-circulation functions to perform the successive data transformation on the input data. The proposed chaotic security design features low computational complexity and regular operations, which leads to high feasibility for easy integration with commercial multimedia storage and transmission applications.

The next six papers deal with the VLSI algorithms and implementations of various important processing modules in modern access systems such as FFT, FEC codec, and DSP core. Due to the prevalence of multimode/multistandard communication systems, it is desirable to have a configurable/programmable DSP processing engine for various access systems. The first two papers in this category are the variable-length FFT/IFFT design by Kuo et al. and the configurable Viterbi decoder design by Benaissa and Zhu. In the FFT design, the authors design and implement a variable-length FFT/IFFT processor by using the techniques of cached-memory FFT architecture as well as the mixed-scaling-rotation CORDIC (MSR-CORDIC) scheme for the butterfly processing element. In the online reconfigurable Viterbi decoder design, the authors propose an area-efficient ACS architecture, in which the constraint length and traceback depth can be dynamically reconfigured. In addition, a scheduling program is used to systematically determine the maximum level of pipelining (speed-up) that can be applied to the decoder in an area-efficient/foldable architecture with in-place path-metric updating. This enables the exploration of the trade-off of decoding speed (throughput) versus area (number of ACS units) for a range of constraint lengths.

The next two papers discuss the advanced FEC algorithms and implementations for modern communication systems. The sixth paper by Kong and Parhi discusses the interleaved convolutional code that can further randomize the error bursts and can be used for burst-error correction. In this paper, an area-efficient high-speed Viterbi decoder architecture is proposed to decode $(n, 1, mI)$ interleaved convolutional code. This paper shows that hardware complexity reduction can be achieved with higher interleaving degree, which leads to area-efficient design for interleaved Viterbi decoder. The next paper by Y. Chen and Parhi demonstrates low-complexity decoding of block turbo-coded system with antenna diversity. This work tries to reduce the decoding complexity of space-time block turbo-coded system with low performance degradation. It considers two block turbo-coded systems with antenna diversity, including the simple serial concatenation of error-control code with space-time block code (STBC), and the recently proposed transmit antenna diversity scheme using FEC techniques. The overall decoding complexity is approximately ten times less than that of the near-optimum block turbo decoder but with only 0.5 dB loss of coding gain at the BER of 10^{-5} over an AWGN channel.

The final two papers are related to the communication DSP core implementations for access systems. The eighth paper, authored by Lee et al. presents new application-specific DSP (ASDSP) instructions and hardware accelerator to efficiently implement Reed-Solomon (RS) encoding and decoding. The ASDSP architecture can implement various programmable primitive polynomials, and significantly reduce the number of clock cycles compared with existing DSP chips. Thus, hardwired RS codecs can be replaced by ASDS accelerators. The final paper by Tsao et al. proposes a low-power embedded DSP core for communication systems. The features of the DSP core include parameterized data path, dual MAC unit, subword MAC, and optional function-specific blocks for accelerating communication system modulation operations. It is also a parameterized design so that the users can select the parameters and special functional blocks based on the characteristics of their applications, and then generate a DSP core in a very short time-to-the-market period.

Overall, the nine papers cover different aspects of advanced signal processing techniques and low-complexity/reconfigurable/programmable DSP implementations for broadband access systems. We thank the authors, the reviewers, the publisher, and the Editor-in-Chief for their tremendous amount of efforts to make this special issue successful. We hope the readers will find the results presented in this special issue helpful in their own design and implementation problems for communication systems.

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An-Yeu (Andy) Wu received the B.S. degree from National Taiwan University in 1987, and the M.S. and Ph.D. degrees from the University of Maryland, College Park, in 1992 and 1995, respectively, all in electrical engineering. During 1987–1989, he served as a Signal Officer in the Army, Taipei, Taiwan, for his mandatory military service. From August 1995 to July 1996, he was a member of the technical staff at AT&T Bell Laboratories, Murray Hill, NJ, working on high-speed transmission IC designs. From 1996 to July 2000, he was in the Electrical Engineering Department of National Central University, Taiwan. He is currently an Associate Professor in the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taiwan. His research interests include low-power/high-performance VLSI architectures for DSP and communication applications, adaptive/multirate signal processing, and reconfigurable broadband access systems and architectures.

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