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Research Article

Characterization and Modeling of DHBT in InP/GaAsSb Technology for the Design and Fabrication of a Ka Band MMIC Oscillator

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This paper presents the design of an MMIC oscillator operating at a 38 GHz frequency. This circuit was fabricated by the III–V Lab with the new InP/GaAsSb Double Heterojunction Bipolar Transistor (DHBT) submicronic technology (We = 700 nm). The transistor used in the circuit has a 15 μm long two-finger emitter. This paper describes the complete nonlinear modeling of this DHBT, including the cyclostationary modeling of its low frequency (LF) noise sources. The specific interest of the methodology used to design this oscillator resides in being able to choose a nonlinear operating condition of the transistor from an analysis in amplifier mode. The oscillator simulation and measurement results are compared. A 38 GHz oscillation frequency with 8.6 dBm output power and a phase noise of −80 dBc/Hz at 100 KHz offset from carrier have been measured.

1. Introduction

The developments in modern electronics (analog, digital, or mixed), whatever their intended applications (telecommunications, spectroscopy and astrophysics, plasma analysis, medical imaging, etc.) now concern applications operating from RF frequency spectrum up to the optical frequencies. In order to develop solid-state circuits operating in the millimeter wave range, new technological processes are emerging for manufacturing semiconductors operating in these domains. To achieve the performances required by such applications, a suitable solid-state technology must be available. III–V Lab provides a new InP/GaAsSb DHBT technology [1], which contains antimony in the base of the transistors and permits submicronic emitter sizes. The structure has been optimized to get an $F_{\max}$ greater than 300 GHz and an F_T equal to 200 GHz. In this context, the work presented in this paper demonstrates the feasibility of designing and manufacturing a low phase noise MMIC frequency source with this new technology. To provide the oscillator designer with the most relevant devices, various multifinger transistors have been measured, a number ranging from 2 to 8 have been compared and reported in [2]. For the higher-frequency applications, 2-finger devices were found to be best suited and selected for this design. In Section 2, we present the complete characterization and nonlinear modeling of the transistor, including its thermal behavior. Section 3 deals with the cyclostationary LF noise source modeling. Section 4 is devoted to the description of the oscillator design according to the new proposed methodology including the drawing of the MMIC layout. In Section 5, all the measurements are detailed and compared with the results predicted by the simulation. The last section concludes the article.

2. Transistor Modeling

In order to design oscillators with improved characteristics, we need accurate models of the passive and active elements of these circuits. The models of passive elements of this process fabricated on coplanar waveguide technology (CPW) have been developed by the MC2 Technology Company. The

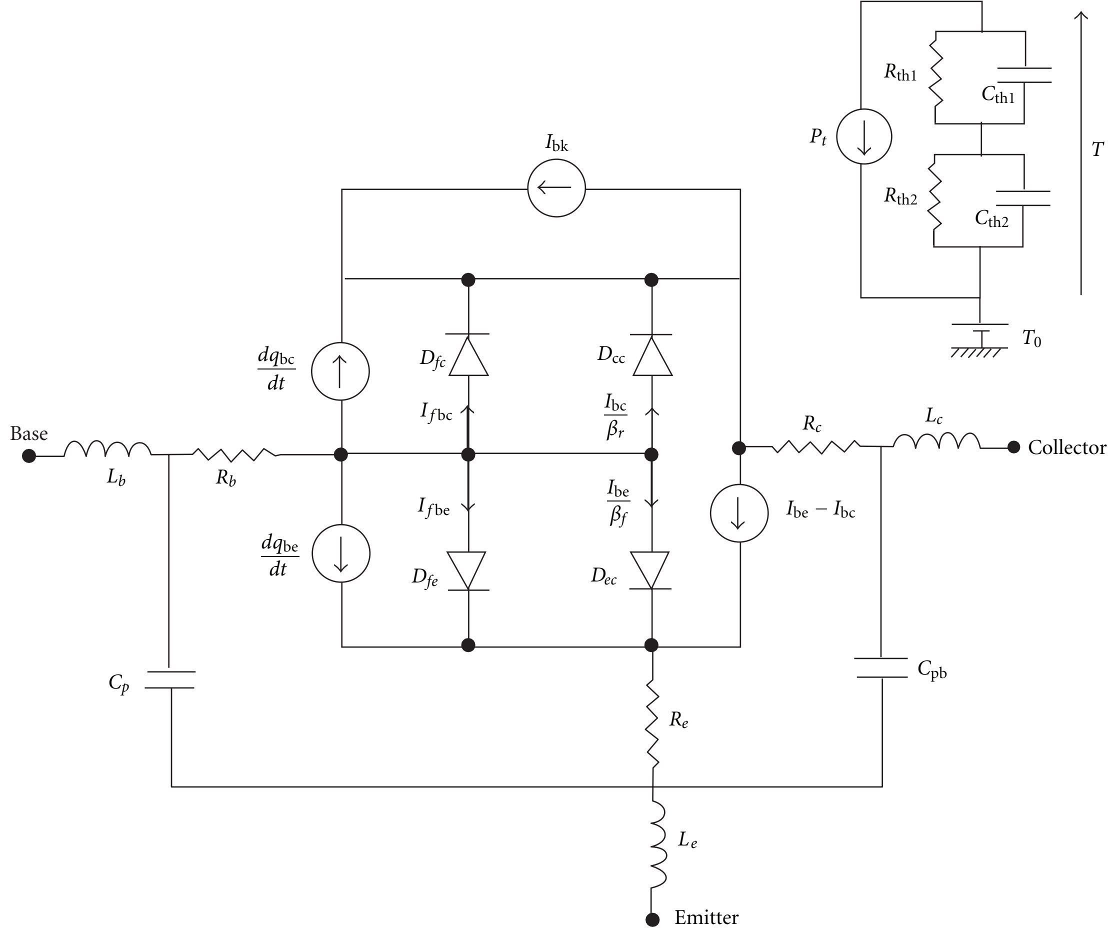


Figure 1: DHBT model π-topology with a two-pole RC thermal subcircuit.

DHBT π model is based on the Gummel and Poon model [3] improved in [4]. It is presented in Figure 1 with its associated thermal circuit formed by two-pole RC cells. The intrinsic part of the convective equivalent circuit is described by four diodes and one voltage-controlled current source: D_{ec} and D_{cc} control the current source with, respectively, a direct gain β_f and a reverse gain β_r, D_{fe}, and D_{fc} model leakage currents. The base collector charge q_{bc} results from the sum of the junction charge with "punchthrough effect" charge, and the depletion charge. The base emitter charge q_{be} results from the sum of three charges: the junction charge, the depletion charge due to the collector transit time, and the Kirk effect charge. These charges depend on the V_{ce} and V_{be} voltages. The extraction of parameters describing the non linear transistor model is performed from pulsed I–V, pulsed $[S]$-parameters measurements. More details on this currently conventional operation are given in [5, 6]. Note that this paper is a detailed version of [7] in which we will explain all the measurement and extraction procedure for the modeling and the design methodology of the oscillator.

To determine the thermal circuit elements, the new method proposed here is a good trade-off between speed and accuracy. This method involves the determination of the impedance and thermal time constant from the measurement of the transistor input impedance at low frequencies. Indeed, the thermal resistance can be estimated from the input impedance Z_{BE} by (2):

$$\begin{aligned} Z_{\text{BE}} &= \frac{V_{\text{BE}}}{I_B} \\ &= h_{11_{\text{ISO}}} + \phi \cdot Z_{\text{TH}}(\omega) \cdot h_{21} \cdot \left(V_{\text{CE}_0} - R_2 \cdot I_{C_0}\right), \end{aligned} \quad (1)$$

with

$$\phi = \left.\frac{\partial V_{\text{BE}}}{\partial T}\right|_{I_B=\text{CTE}}, \quad (2)$$

where V_{BE} and I_B are HBT Base-Emitter voltage and base current, $h_{11_{\text{ISO}}}$ is the h_{11} isothermal parameter, Z_{TH} is the thermal impedance, V_{CE_0} and I_{C_0} are the bias Collector-Emitter voltage and Collector current, R_2 is the load resistance on the collector (see Figure 2).

So, according to this equation, we must determine the ϕ, h_{21}, and $h_{11_{\text{ISO}}}$ parameters to deduce the thermal impedance Z_{TH}. The ϕ parameter is determined using the I_b measurement as a function of V_{be} for a constant current I_c at different temperatures in DC mode. The methodology is detailed in [8]. The h_{21} parameter is determined using the following four quantities shown in Figure 2 where Z_{in} is the input impedance, Z_{out} is the output impedance, Z_{in_0} is the input impedance when the transistor output is

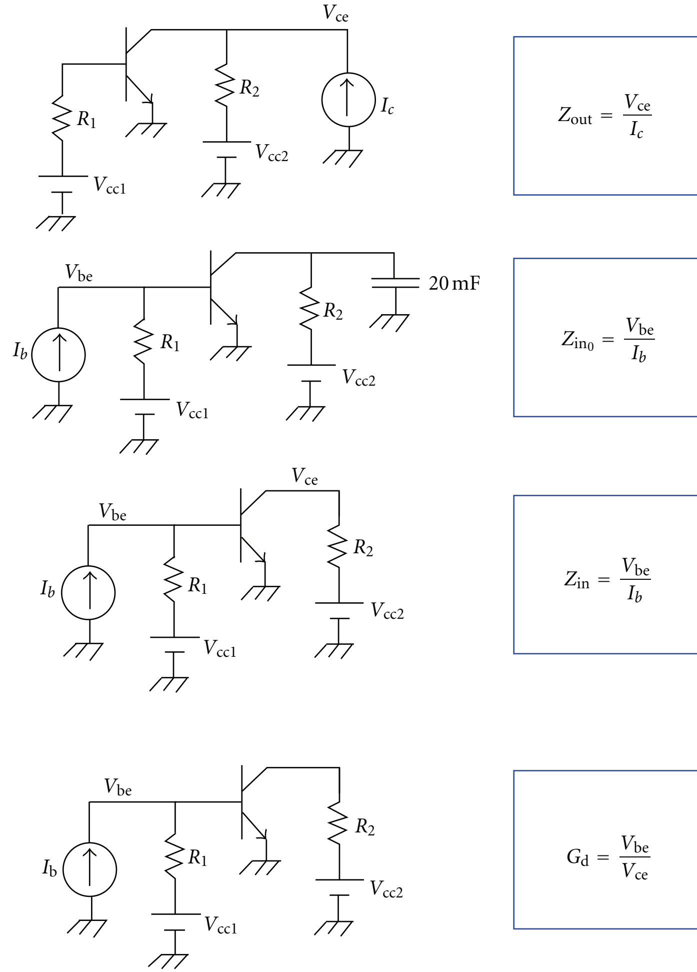


Figure 2: Measurements used to determine the h_{21} parameter.

short circuited at LF, and G_d is the transistor voltage gain. Thus, it is possible to extract the h_{21} parameter from these four measures by using the hybrid equivalent circuit of the transistor, and with (3) [9]:

$$h_{21} = \frac{Z_{in} \cdot G_d \cdot R_1}{Z_{out}\left(Z_{in_0} - R_1\right)}, \tag{3}$$

where R_1 is the base resistance (see Figure 2). The $h_{11_{ISO}}$ parameter is determined by measuring the transistor input impedance with $R_2 = V_{ce_0}/I_{c_0}$. In this case, the measured impedance is defined by $Z_{BE} = h_{11_{ISO}}$. At last, the input impedance is measured with a resistor R_2 different from the previous value, but at the same bias point (Figure 3). Knowing the parameters of the equation, we can deduce the thermal impedance Z_{th}. To implement this self-heating effect in a simulator, we include a low-pass equivalent electrical circuit with two RC parallel cells in series whose impedance fits the measured Z_{th}. Thus, it is possible to obtain an equivalence between *voltage/temperature* and *current/power* as shown in Figure 3.

To conclude this first modeling step, we compare the convective model simulation with measurements. For example, Figure 4 shows the comparison of the $I_c(V_{ce})$ network, the current gain β as a function of V_{ce} and V_{be} versus V_{ce} for an I_b current range from 0.5 mA to 3 mA in steps of 0.5 mA at a temperature equal to 25°C.

The last modeling step is the determination of the nonlinear charges q_{bc} and q_{be} by means of the pulsed [S] parameters measurements. The final modeling verification consists in comparing the complete electrothermal nonlinear model simulation with measurement. Figure 5 shows the comparison between simulation and measurement of the [S] parameters, the maximum available gain (MAG) and h_{21} parameter versus frequency for a I_b current equal to 2 mA and V_{ce} voltage equal to 1, 2, and 2.5 V. Thus, we get a good agreement between the two results.

3. Modeling of Transistor Low-Frequency Noise Sources

An accurate prediction of oscillator phase noise requires a cyclostationary model of the LF noise sources of the transistor [10]. A transistor model with internal LF noise sources [11] with cyclostationary properties has been developed for a GaInP/GaAs HBT technology. This model is only based on low-frequency measurements around DC bias. The noise

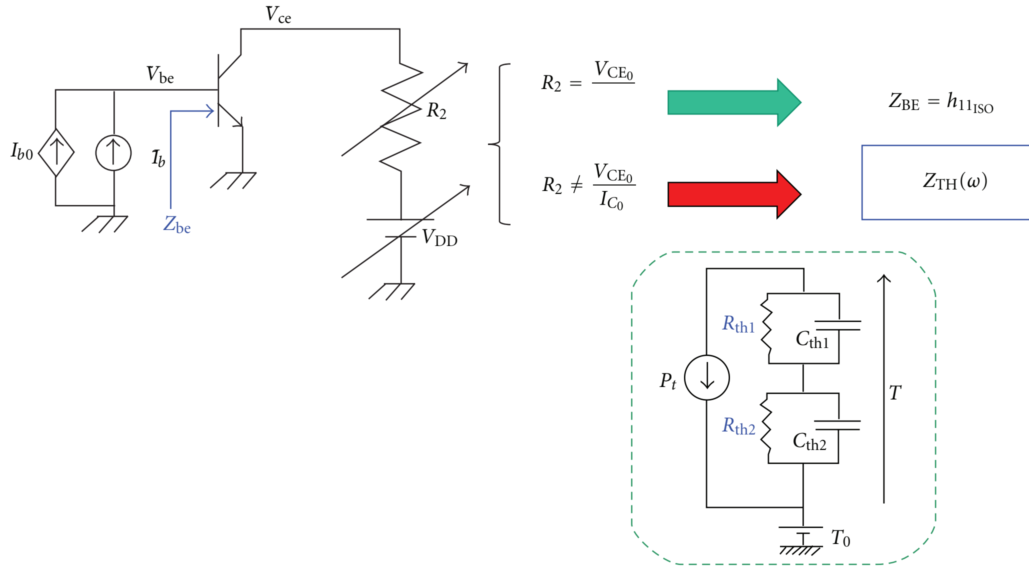


Figure 3: Determination of thermal impedance.

(a)

(b)

(c)

Figure 4: Comparison between model (red) and I(V) measurement (blue cross) with I_b current ranging 0.5 to 3.5 mA and a V_{ce} voltage ranging 0 to 3.5 V for a temperature equal to 25°C.

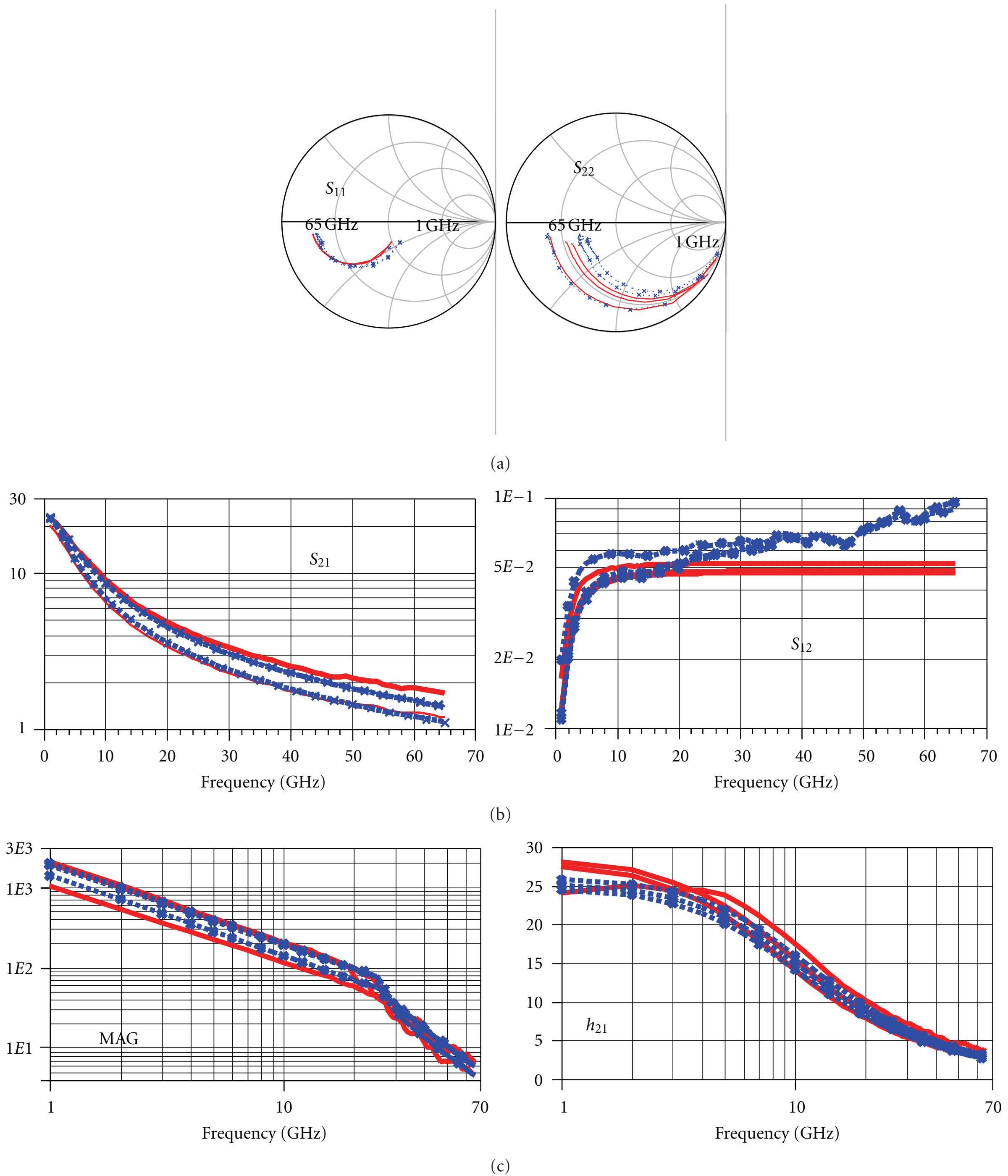


Figure 5: Comparison between model simulation results in red and measurements (blue cross) for the MAG, S_{11}, S_{12}, S_{22}, S_{21}, and h_{21} parameters with $I_b = 2$ mA and $V_{ce} = 1 - 2 - 2.5$ V.

sources variations versus the DC collector current are taken into account to elaborate cyclostationary noise model. We propose to reuse this topology (Figure 6) for this InP/GaAsSb technology with the new extraction method presented here.

This LF model of the transistor (the nonlinear charges are not represented here) is based on the original representation of Ebers and Moll (Model T), called injection model, which is based on current-controlled current sources. He directly comes from the equations of physics and models the injection currents of the transistor. α is the large-signal forward mode current gain of a common-base transistor. More details on its equivalence to the Gummel-Poon model are given in [12]. Moreover, the extraction of noise sources from measurement is easier with this model. The diode

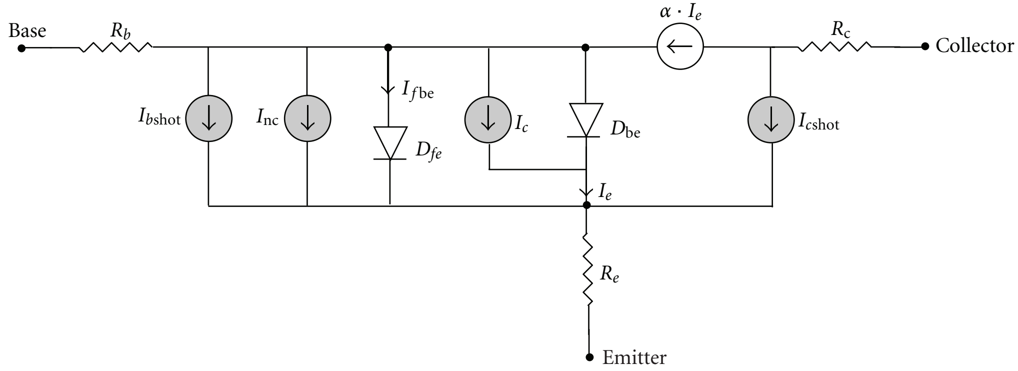


Figure 6: LF equivalent circuit of the transistor with noise sources.

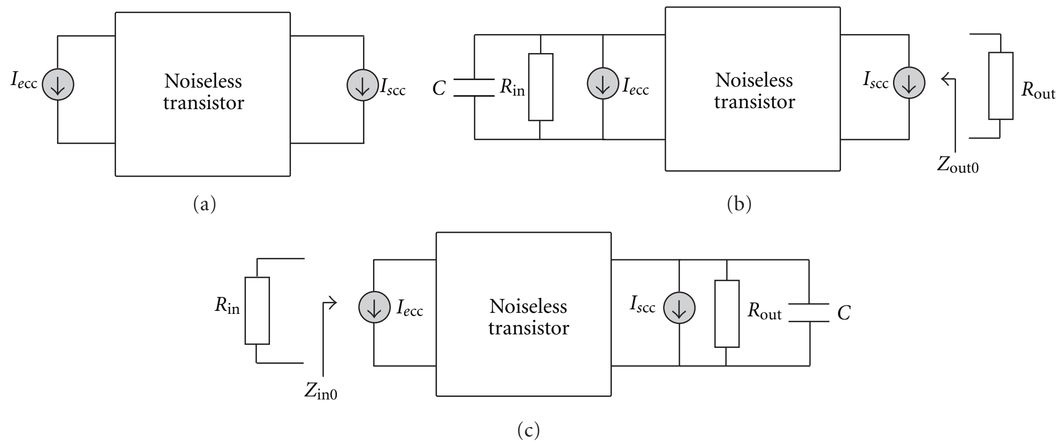


Figure 7: Equivalent circuit of a noisy transistor with current noise sources.

D_{be} represents the base-emitter junction, D_{fe} represents the leakage current of the base-emitter junction. The transistor effect is modeled by the controlled current source $\alpha \cdot I_e$. The current sources $I_{c\text{shot}}$ and $I_{b\text{shot}}$ are the shot noise sources, I_c and I_{nc} represent the LF noise sources ($1/f$ and GR). The thermal noise sources of access resistors are negligible. The noise source I_c is generated within the base-emitter junction and it is associated to the D_{eb} diode. It participates in the transistor effect through the controlled current source $\alpha \cdot I_e$. The origin of the I_{nc} source comes from the periphery of the base-emitter junction and can be associated with the leakage diode D_{fe}. This representation with only two LF sources results from many measurements and simulations of oscillators which have shown that this transistor model is sufficient to accurately simulate oscillator phase noise. The purpose of the modeling is to extract the sources I_c and I_{nc} from noise measurement. In order to do that, we suppose that the transistor low-level model with its noise sources can be represented by the conventional schema of Figure 7(a) with a Norton equivalent current source at each access of the transistor. Noise measurements consist in successively measuring these two noise sources I_{ecc} and I_{scc}. To do that, two low value resistances R_{in} and R_{out}, properly chosen ($R_{\text{in}} \ll Z_{\text{in}_0}$ and $R_{\text{out}} \ll Z_{\text{out}_0}$), are successively connected to each access in order to short-circuit the corresponding source [13]. Moreover, to achieve this condition, a huge capacitance is successively connected to the transistor access (in parallel with R_{in} or R_{out} of Figure 7(b) and 7(c)) where we do not measure the noise. The voltage thus generated is then amplified by the voltage amplifier and its output is connected to the FFT spectrum analyzer in order to measure the noise voltage spectral density.

The schema used to obtain the noise sources of the transistor accesses is presented in Figure 8.

This schema is the same at each access of the transistor. The amplifier is represented by its noise voltage source e_{at} and by its input impedance Z_{at}. The voltage V_s is amplified with a gain G to be measured on the FFT analyzer. The [ABCD] matrix represents all the passive elements considered in the measurement (bias tees, lines, etc.). R can be either R_{in} or R_{out}, I_R is the thermal current noise source associated to R, I_{dut} can be either I_{ecc} or I_{scc}, and Z_{dut} can be either Z_{in_0} (with the collector short-circuited) or Z_{out_0} (with the base short-circuited). Thus, applying Kirchoff's laws, we obtain (4):

$$V_s = \frac{N_2 \cdot I_{\text{dut}} + N_3 \cdot e_{\text{at}} + N_4 \cdot I_R}{N_1}, \tag{4}$$

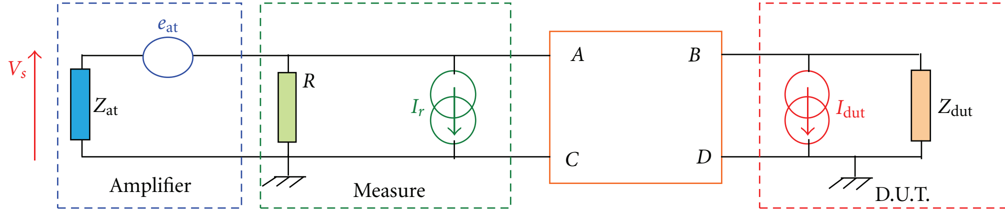
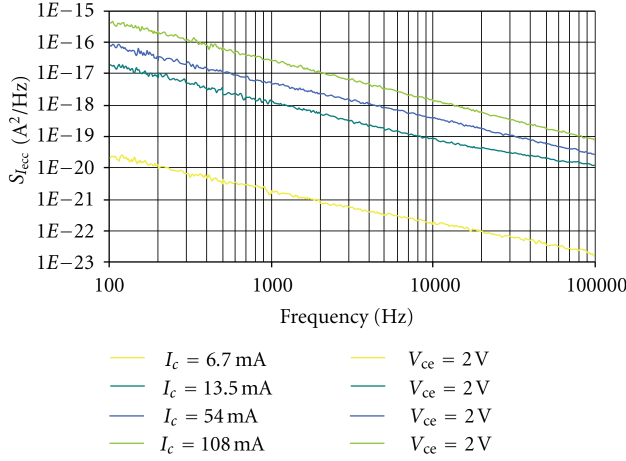
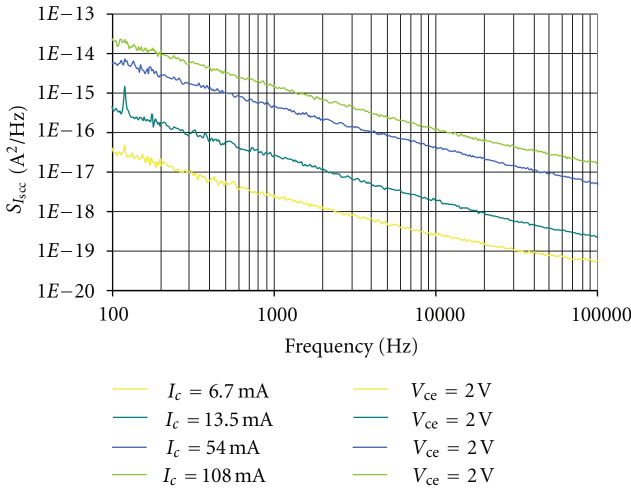


FIGURE 8: Equivalent schema for the extraction of short-circuit noise current spectral density at transistor accesses.

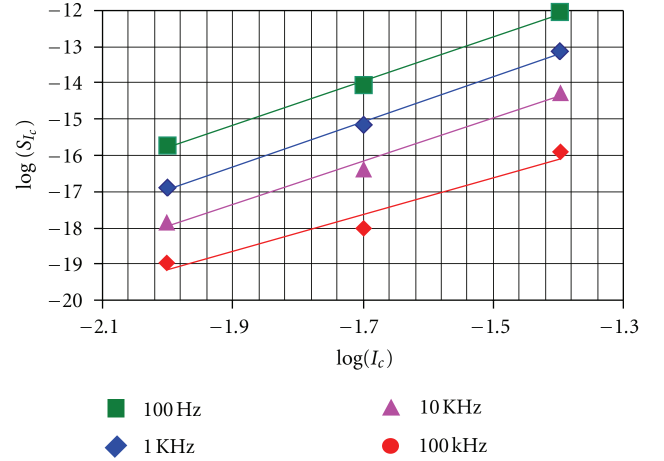


(a)

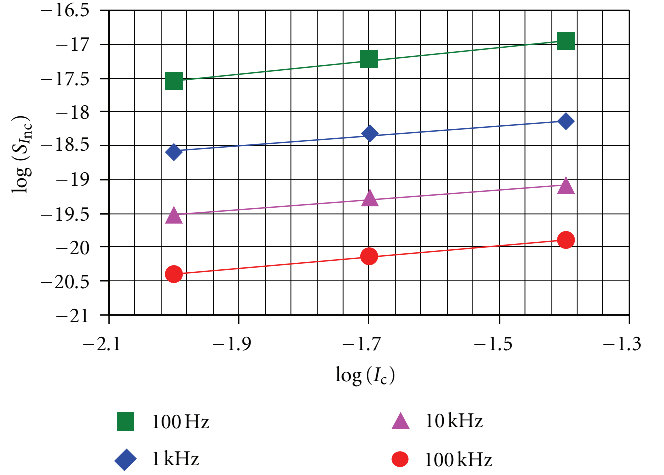


(b)

FIGURE 9: Spectral densities plot of the short-circuit noise current at transistor access for collector currents $I_{c_0} = 6.7, 13.5, 54, 108$ mA.



(a)



(b)

FIGURE 10: Plot of S_{ic} and SI_{nc} noise current spectral densities.

Now, we must determine the noise voltage spectral densities at each access:

$$S_{V_s} = \left|\frac{N_2}{N_1}\right|^2 S_{I_{dut}} + \left|\frac{N_3}{N_1}\right|^2 S_{e_{at}} + \left|\frac{N_4}{N_1}\right|^2 S_{I_R}, \quad (5)$$

with

$$\begin{aligned} N_1 &= Z_{at} \cdot R \cdot D + Z_{at} \cdot R \cdot Z_{dut} \cdot C + Z_{polar} \cdot Z_{dut} \cdot A \\ &\quad + R \cdot B + Z_{at} \cdot Z_{dut} \cdot A + Z_{at} \cdot B, \\ N_2 &= Z_{at} \cdot Z_{dut} \cdot R \cdot (A \cdot D - B \cdot C), \\ N_3 &= Z_{at} \cdot (-R \cdot D - R \cdot Z_{dut} \cdot C - Z_{dut} \cdot A - B), \\ N_4 &= Z_{at} \cdot (Z_{dut} \cdot R \cdot A + R \cdot B). \end{aligned} \quad (6)$$

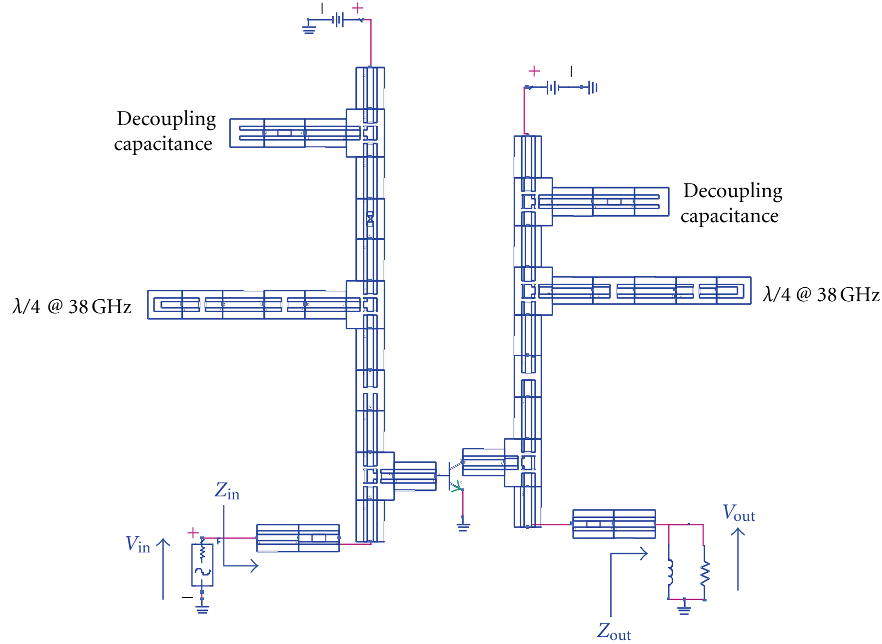


FIGURE 11: Circuit for nonlinear amplifier simulation.

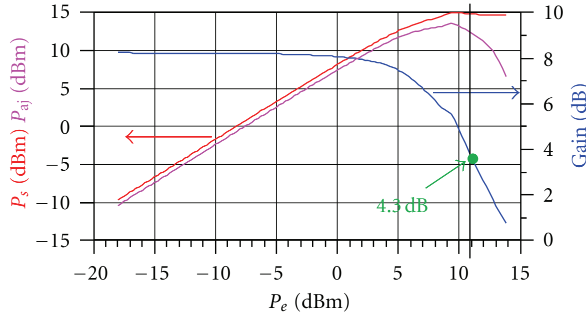


FIGURE 12: Amplifier simulation results.

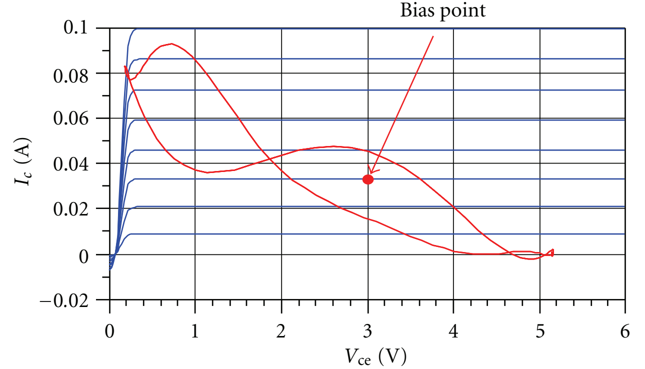


FIGURE 13: Simulation of amplifier load line.

Now, we can define the short-circuit noise current spectral density, which is expressed by the following equation:

$$S_{I_{\text{dut}}} = \left|\frac{N_1}{N_2}\right|^2 S_{V_s} - \left|\frac{N_4}{N_2}\right|^2 S_{I_R} - \left|\frac{N_3}{N_2}\right|^2 S_{e_{\text{at}}}. \quad (7)$$

From the previous equation applied to each access of the transistor, we thereby obtain the expressions of the noise current spectral densities $S_{I_{\text{ecc}}}$ or $S_{I_{\text{scc}}}$. The last step of this noise modeling consists in extracting the two internal noise sources spectral densities S_{I_c} and $S_{I_{\text{nc}}}$ in Figure 6 with (8):

$$S_{I_{\text{nc}}} = -\frac{R_1^2}{R_D^2 \cdot \beta^2} \cdot S_{I_{\text{scc}}} + \frac{R_1^2}{R_D^2} \cdot S_{I_{\text{ecc}}} - S_{Ib_{\text{shot}}} - \frac{R_e^2 \cdot \beta^2 - R_3^2}{R_D^2 \cdot \beta^2} \cdot S_{Ic_{\text{shot}}},$$

$$S_{I_c} = -\frac{R_2^2 \cdot R_1^2}{R_D^2 \cdot R_{\text{be}}^2 \cdot \beta^2} \cdot S_{I_{\text{scc}}} - \frac{R_4^2 \cdot R_1^2}{R_D^2 \cdot R_{\text{be}}^2} \cdot S_{I_{\text{ecc}}} + \frac{R_4^2 \cdot R_e^2 \cdot \beta^2 - R_2^2 \cdot R_3^2}{R_D^2 \cdot R_{\text{be}}^2 \cdot \beta^2} \cdot S_{Ic_{\text{shot}}} - \frac{R_b^2}{R_{\text{be}}^2} \cdot S_{I_{\text{rbb}}} - \frac{R_e^2}{R_{\text{be}}^2} \cdot S_{I_{\text{rbe}}}, \quad (8)$$

with

$$\begin{aligned} R_1 &= (\beta+1)(R_{\text{be}}+R_e)+R_b, \\ R_2 &= (\beta+1)\cdot R_{\text{be}}+\beta\cdot R_e, \\ R_3 &= (\beta+1)\cdot R_{\text{be}}+R_e+R_b, \\ R_4 &= R_e+R_b, \\ R_D^2 &= [(\beta+1)R_{\text{be}}+\beta R_e]^2-(R_e+R_b)^2. \end{aligned} \quad (9)$$

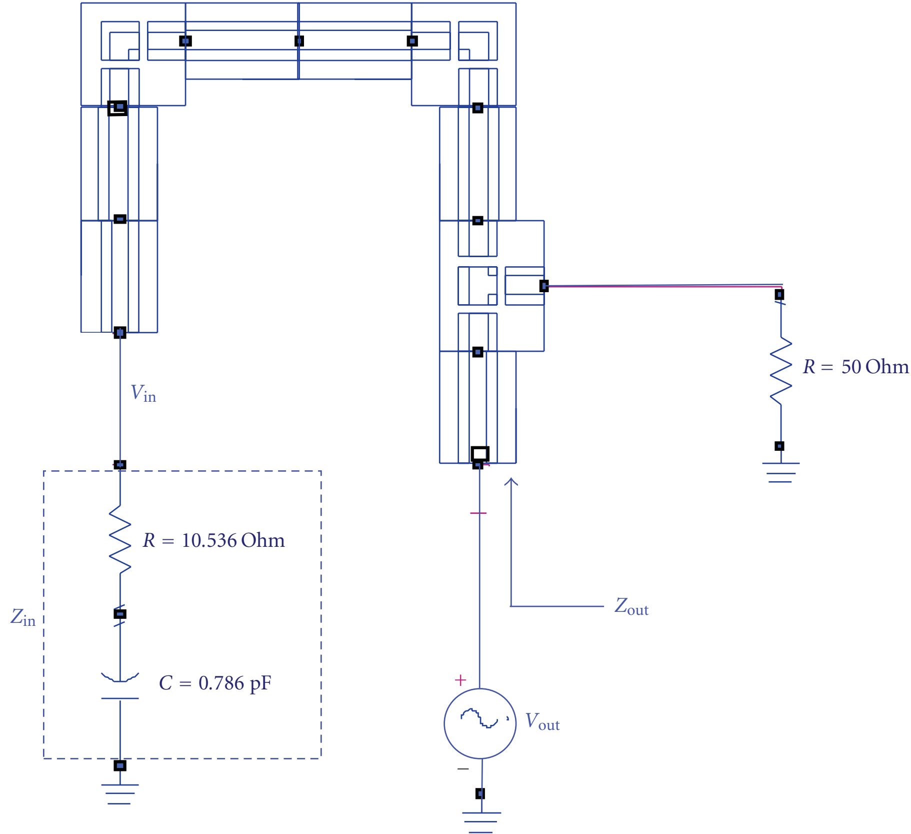


Figure 14: Feedback loop circuit.

Table 1: K_x and a_x values of the internal LF noise sources for each frequency.

	S_{I_c}		$S_{I_{nc}}$	
Frequency	a_{I_c}	K_{I_c}	$K_{I_{nc}}$	$a_{I_{nc}}$
100 Hz	2.3	$6.607e-11$	2.55	$3.63e-13$
1 KHz	2.33	$7.9433e-12$	2.39	$1.585e-14$
10 KHz	2.28	$7.08e-13$	2.13	$3.981e-15$
100 KHz	2.36	$5.012e-14$	1.97	$1.585e-17$

Table 2: Load pull simulation results.

P_e (mW)	P_s (mW)	$P_{aj\ max}$ (mw)	Gain (dB)	C (dB)
11.56	27.1	17.6	8.2	4.3

In order to limit the LF noise measurement time while obtaining a relatively accurate model, we will only measure the noise sources in the normal, active region where the transistor operates in oscillation condition: the area of the transistor optimum load cycle for low-phase noise operation is defined in [14], by minimizing the LF noise sources conversion. Moreover, some noise measurements have shown that in the area where the base-collector junction is negatively biased, the noise level is independent of V_{ce}. Thus, the measurements will only consist in noise source measurements versus collector current, for a given V_{ce} close to the transistor bias point for low-phase noise oscillator operation. Following this procedure, Figure 9 shows the spectral densities of the short circuit noise current at transistor access for collector currents $I_{c_0} = 6.7, 13.5, 54, 108$ mA.

Then, from (8), the spectral densities S_{I_c} and $S_{I_{nc}}$ are computed and plotted versus I_{c_0} in log-log plot (Figure 10) for four frequencies 100 Hz, 1 KHz, 10 KHz, and 100 KHz, which correspond to the frequencies at which oscillators are generally qualified. Note that, from the point of view of the phase noise simulation, these frequencies are independent.

The final step of noise modeling is to determine the spectral density equation of S_{I_c} and $S_{I_{nc}}$ obtained by fitting the curves of (Figure 10) with an equation of the form:

$$S_{I_x} = K_x \cdot I_c^{a_x}, \tag{10}$$

where I_c is the collector current, x is taken for nc or c.

The values of K_x and a_x are given in Table 1.

In summary, we extracted the LF noise model of the HBT with internal noise sources. This model was implemented in ADS [15] and will enable us to simulate the phase noise of the oscillator while taking into account the cyclostationary property of noise sources.

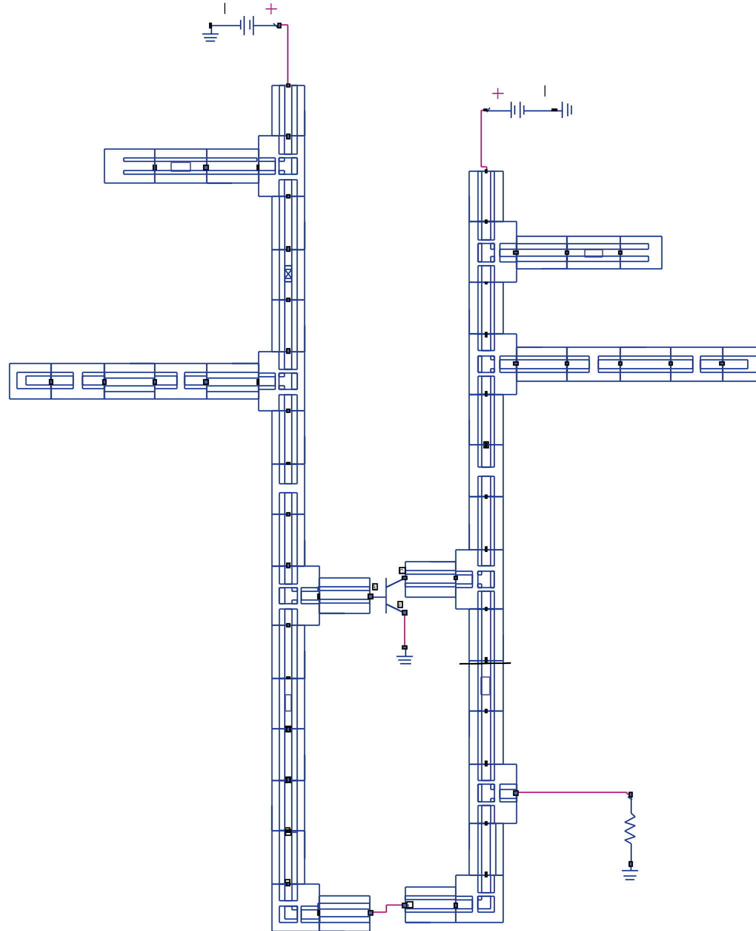


Figure 15: First oscillator circuit.

4. Oscillator Design

The main objective of this design is to reduce the oscillator-phase noise while retaining a significant output power (few dbm). The desired oscillation frequency is 38 GHz and the MMIC uses the CPW technology. These two goals can be controlled by the intrinsic load cycle form of the transistor in oscillation [14]. This section describes the original design methodology used to reach these objectives by controlling the nonlinear behavior of the transistor when it operates as an oscillator circuit, by means of conventional amplifier nonlinear simulation. Its specific interest is the simulation rapidity and the easy control of the load cycle shaping. Then, by computing the load impedances at transistor input and output and the corresponding voltages, we are able in oscillation to obtain a nonlinear state as close as possible to that obtained in amplifier simulation. For this purpose, the three following steps are necessary.

4.1. Transistor Analysis in Large Signal Amplifier Mode. The schema of the transistor with its bias circuits (in CPW technology) and load impedance (synthesized with an inductor and a resistor in parallel) for nonlinear amplifier simulation is presented in Figure 11.

Table 3: Simulated oscillator preformances.

P_e (mW)	P_s (mW)	$P_{aj\ \max}$ (mw)	Gain (dB)	C (dB)
13.9	50.3	7.3	5.6	4.3

Table 4: Contribution of elementary noise sources to total phase noise at 100 kHz from the carrier.

Total PN noise	−76.94 dBc/Hz
PN due to source S_{Ic}	−76.94 dBc/Hz
PN due to source S_{Inc}	−106.3 dBc/Hz
PN due to shot noise source at collector	−119.8 dBc/Hz

After some tuning of the bias point and load impedance, the gain, the output, and added powers versus the input power are plotted in Figure 12 and the load cycle in Figure 13.

Thus, we obtain the values given in Table 2 for the following bias points $I_{b_0} = 1.5$ mA, $V_{ce_0} = 2.2$ V, $I_{c_0} = 35$ mA, where P_e and P_s represent the transistor input and output powers, C the gain compression. Note that to reach a sufficient output power and compression gain (to ensure oscillation after manufacturing despite technological spread), the load cycle must be close to the area where the

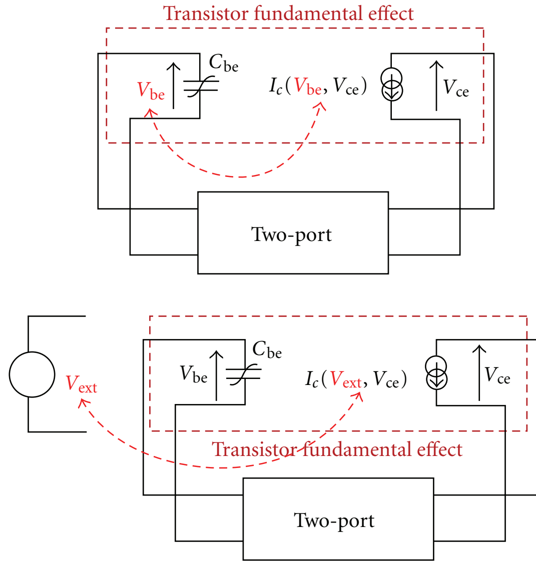
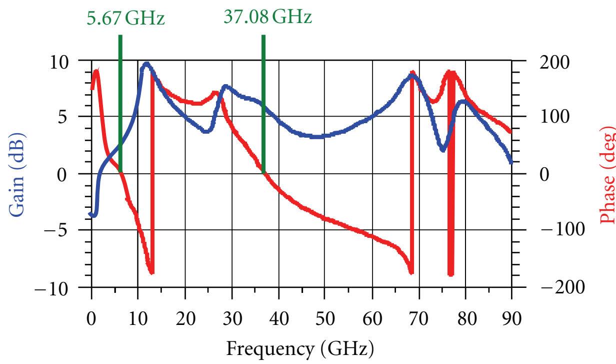
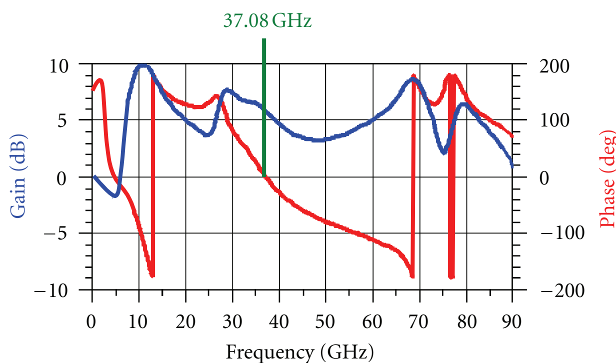


Figure 16: The open loop operation.



(a)



(b)

Figure 17: Magnitude and phase of open loop gain.

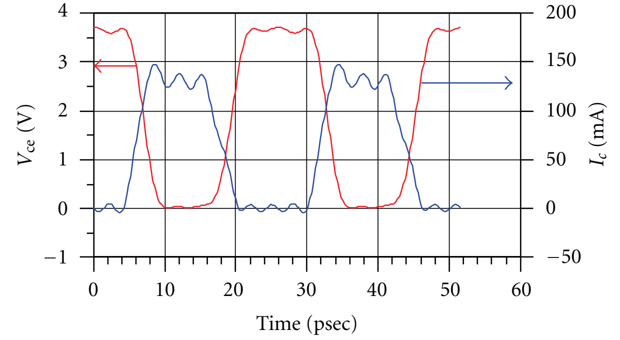


Figure 18: Intrinsic time domain waveform of I_c current and V_{ce} voltage.

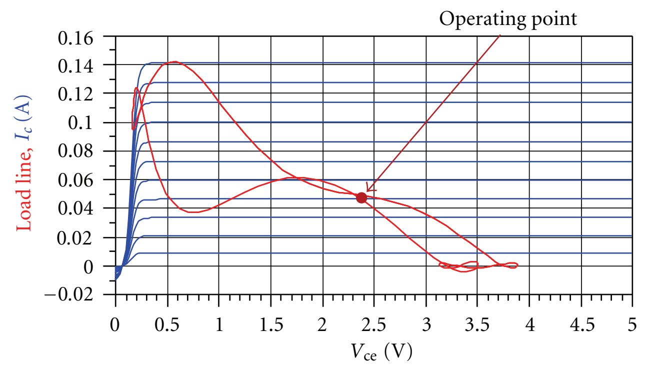


Figure 19: Oscillator intrinsic load line.

Table 5: Comparison of oscillator performances.

(a)

Technology	f_0(GHz)	TB (%)	$\mathcal{L}\{f_{offset}\}$(dBc/Hz)
Si/SiGe [16]	38	not	−55
InGaP/GaAs [17]	40.8	<1%	−95
GaAs [18]	38	not	−104
AlInAs/InGaAs [19]	39	9	−75
AlInAs/InGaAs [20]	38.1	<1%	−85
InP [21]	39.9	<1%	−84
InP (this work)	**37.1**	**not**	**−80**

(b)

Δf_{offset} (KHz)	P_{out} (dBm)	FOM (dBc/Hz)
100	2	−53.2
100	5.3	−90.5
1000	11.9	−67.3
100	5	−89.5
100	8.4	−76.8
100	5	−79.6
100	**5.18**	**−74.8**

base-collector junction conducts. From this simulation, we compute the input and output impedances Z_{in} and Z_{out} and voltage gain $G = V_{out}/V_{in}$. These data will serve to design the feedback circuit in order to keep this nonlinear state in oscillation as explained in the next section.

4.2. Determination of the Feedback Circuit. This step involves the determination of the feedback loop designed with transmission line and of the output circuit (matching circuit) whose schema is given in Figure 14. In this schema, the

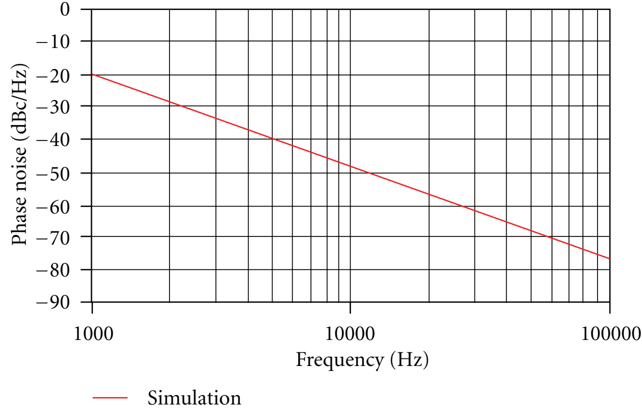


Figure 20: Phase noise simulation result.

transistor input impedance Z_{in} is synthesized with an RC circuit.

The goal of the linear optimization of the line widths and lengths is to obtain the same output impedance Z_{out} and voltage gain $G = V_{out}/V_{in}$ as in the previous section and by taking into account the technology and geometric constraints. Thus, the first draft of the oscillator circuit is given in Figure 15.

4.3. Oscillator Simulation. This section describes all the necessary simulations to ensure good performances of the oscillator (stability, phase noise, etc.). The first simulation is an open-loop simulation [22]. This simulation allows us to determine the starting oscillation frequency and to verify that no other parasitic oscillations exist. In order to open the oscillation loop, a new circuit is drawn (Figure 16): the voltage-controlled current source of the transistor fundamental effect is isolated from the other elements of the transistor model and is now controlled by an external generator V_{ext}. All the other circuit elements are included in the feedback two-port circuit.

Then the open loop gain is defined by

$$G_{OL}(\omega) = \frac{V_{be}(\omega)}{V_{ext}(\omega)}. \quad (11)$$

The conditions to obtain oscillation starting are given by (12):

$$\begin{gathered} |G(j\omega_0)\cdot H(j\omega_0)| > 1, \\ \arg(G(j\omega_0)\cdot H(j\omega_0)) = 0, \\ \left.\frac{\partial \arg(G(j\omega)\cdot H(j\omega))}{\partial\,\omega}\right|_{\omega_0} < 0, \end{gathered} \quad (12)$$

Figure 17(a) shows this simulated open-loop gain for the oscillator circuit of Figure 15. A parasitic oscillation appears at frequency 5.67 GHz. An RC series circuit has been added in parallel with the bias circuit to eliminate these oscillations. The new open loop gain is shown in Figure 17(b).

We can note only one starting oscillation frequency at 37.08 GHz. This open-loop analysis also allows to compute the oscillator loaded quality factor with expression (13) [23]:

$$Q_{Loscill}(\omega_0) = \frac{\omega_0}{2}\left|\left|\frac{d\arg\left(\tilde{G}_{ol}(j\omega)\right)}{d\omega}\right|\right|_{\omega_0}. \quad (13)$$

The quality factor obtained by this simulation is equal to 33. Now, we perform a Harmonic Balance simulation of the oscillator. The time domain waveform of I_c current and V_{ce} voltage are shown in Figure 18.

The intrinsic load line cycle is shown in Figure 19.

Finally, the oscillator electrical performances are detailed in Table 3.

The simulation of the oscillator phase noise (PN) is shown Figure 20.

Table 4 presents the contribution of elementary noise sources of the internal transistor at the 100 KHz frequency.

The final layout, taking into account all the technological constraints, including stabilizing circuits and a 3 dB attenuator at the output to reduce pulling effect, is shown Figure 21. The circuit was fabricated by III–V Lab.

5. Oscillator Measurement

5.1. Power and Oscillation Frequency Measurement. To test the robustness of the oscillation, measurements have been performed on 15 oscillators of the wafer for various DC I_c currents. Figure 22 presents the oscillation frequency and the output power versus I_{c_0} current for different V_{ce_0} voltages and a V_{be_0} voltage equal to 0.8 V.

The output power increases by 5 dB over the variation range of I_{c_0}, while the oscillation frequency shows a variation of 1 GHz over the same range. This shows that the oscillation frequency remains stable for an I_{c_0} current variation between 35 and 60 mA.

5.2. Phase Noise Measurement. The XLIM Laboratory has an AEROFLEX PN9500 bench (Figure 23) to perform the phase noise measurement of the oscillator. This bench enables us measure the phase noise of the oscillator in the 250 MHz–26.5 GHz bandwidth with down-converter. The oscillation frequency of the circuit being out of range, we developed our own down-converter to reduce the oscillation frequency in the PN9500 bandwidth. Thus, the system using the delay line method is presented Figure 24.

It is composed of a mixer in which an LO signal at frequency 10.75 GHz is generated by a high spectral purity synthesizer PN9276-20 from the PN9500 setup bench. The RF signal comes from the measured oscillator. The IF output is connected to the PN9718 input. Before measuring the oscillator phase noise, we must ensure that the measurement chain will not add noise. To do that, we replace the oscillator by a high spectral purity synthesized source (ANRITSU 68367C). The phase noise of the system measured with this source is represented in Figure 25 and gives the noise floor of the system.

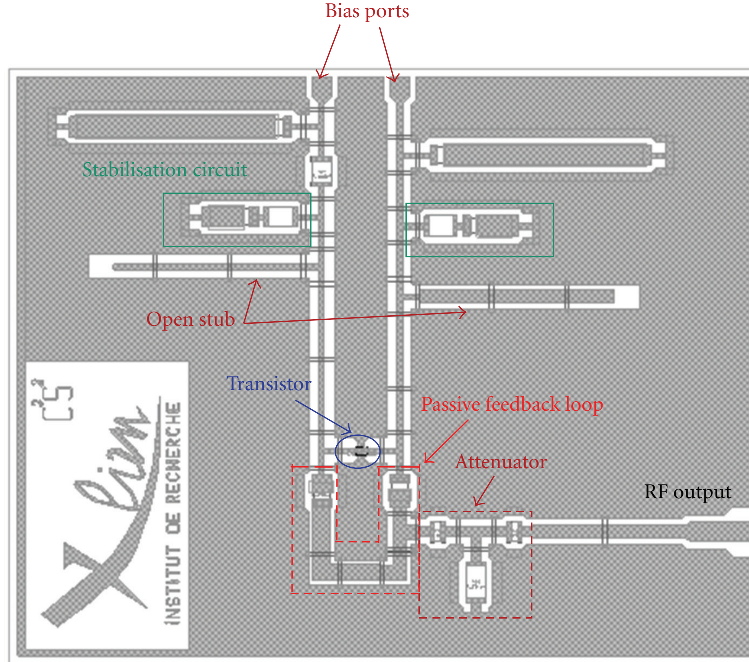


FIGURE 21: Oscillator layout ($2070 \times 1635\,\mu\text{m}^2$).

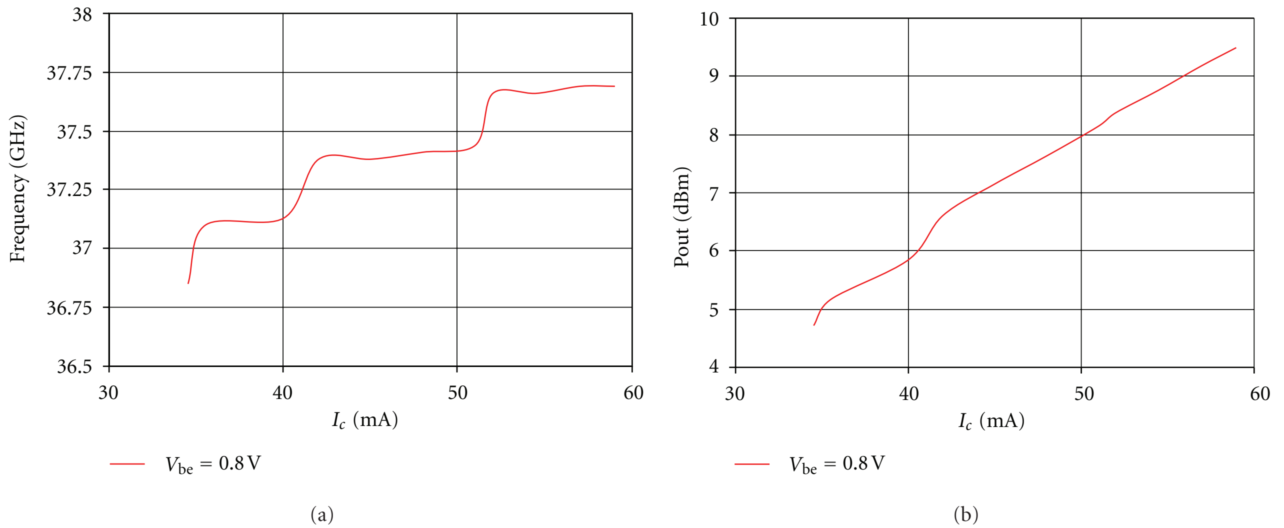


FIGURE 22: Measurement result of oscillation frequency and output power versus I_c current for V_{be_0} voltage equal to 0.8 V.

Figure 26 shows the plot of the phase noise measurement of the 15 oscillators on the wafer and the simulated phase noise for the bias point $V_{\text{be}_0} = 0.8$ V and $V_{\text{ce}_0} = 2.2$ V.

We can note that the phase noise simulation coincides with the average results of measurement. The oscillation frequency measurement for the nominal bias point is close to 37.1 GHz with an output power equal to 5.2 Bm. The phase noise measure is much higher than the system PN floor (> 15 dB), so we can confirm that the phase noise is that of the oscillator. To compare our oscillator with published oscillators with an oscillation frequency close to 38 GHz, we will use a figure of merit described by (14):

$$\text{FOM} = \mathcal{L}\left\{f_{offset}\right\} - 20\log\left(\frac{f_0}{f_{\text{ref}}}\right) - 25\log\left(\frac{f_{offset_{\text{ref}}}}{f_{offset}}\right) - 20\log\left(\frac{\text{TB\%}}{100}\right) - 10\log\left(\frac{P_{\text{out}}}{1\,\text{mW}}\right) \tag{14}$$

where $\mathcal{L}\{f_{offset}\}$ is the oscillator phase noise at a frequency offset from carrier f_{offset}. The oscillation frequency of the

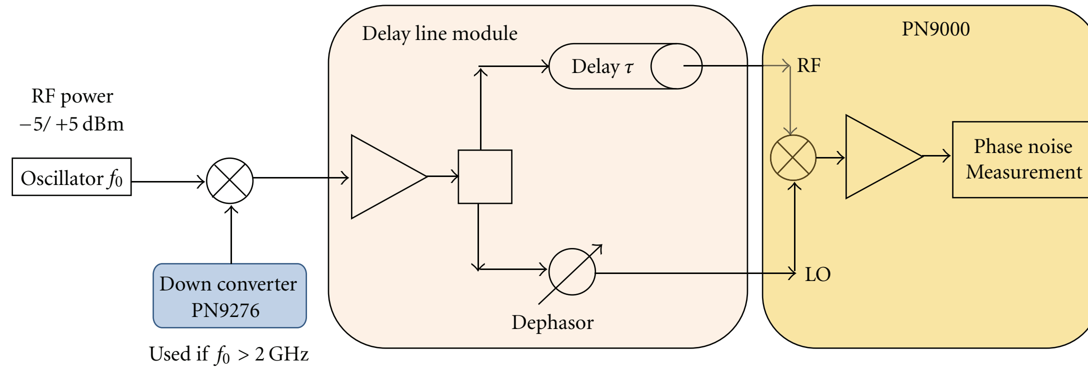


Figure 23: Synoptic of PN9500 phase noise bench.

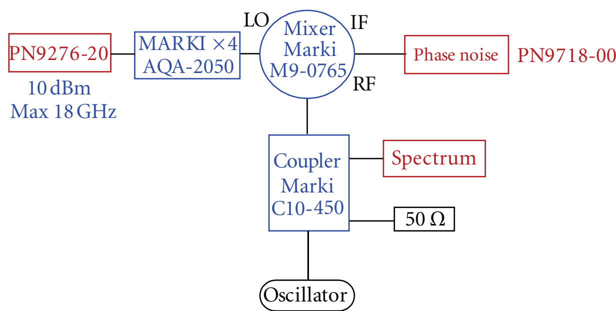


Figure 24: Principle of realized phase noise bench.

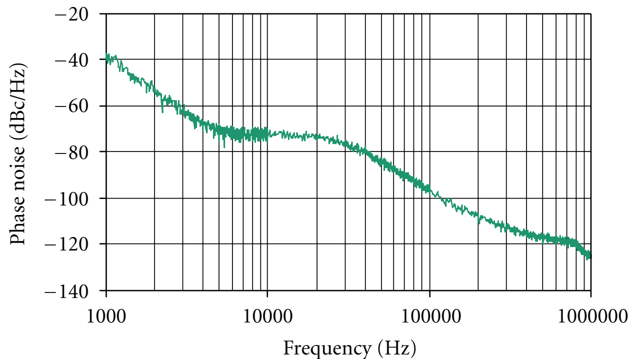


Figure 25: PN floor of the system.

various oscillators (f_0) is reduced to a reference frequency (f_{ref} = 37.1 GHz) which is the oscillation frequency of the oscillator of this work. The carrier frequency offset is reduced to a distance $f_{offset_{ref}}$ = 100 KHz. The multiplier factor is equal to 25 because the oscillator phase noise of this work has a slope of −25 dB/decade. The tuning bandwidth TB (in percentage) is also taken into account. The oscillator output power P_{out} is reduced to a reference of 1 mW. This figure of merit is valid for oscillator with a tuning bandwidth of more than 1%: otherwise, these oscillators are considered as fixed-frequency oscillators. The results are summarized in Table 5. We have chosen a value of phase noise of −80 dBc/Hz which corresponds to an average value of all those measured.

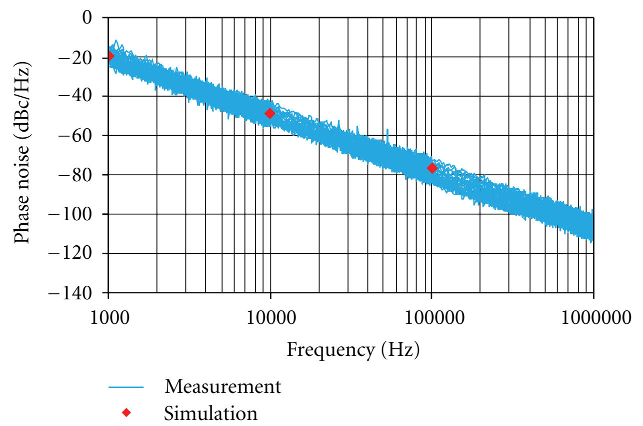


Figure 26: Comparison between measurement and simulation of oscillator phase noise.

We can verify that we obtain an average performance as regarding the figure of merit compared to those published.

6. Conclusion

In conclusion, this work enables us to build an MMIC Ka-band oscillator with good performances. An electrothermal nonlinear model of the transistor was proposed, including cyclostationary noise sources to accurately predict its phase noise. The design method used allowed us to define a nonlinear operation of the transistor to limit the contributions of low-frequency noise sources responsible for the phase noise. This amplifier nonlinear state has been kept in oscillation operation. This evaluation of the III–V Lab process has given encouraging results concerning the feasibility of efficient Ka-band circuits.

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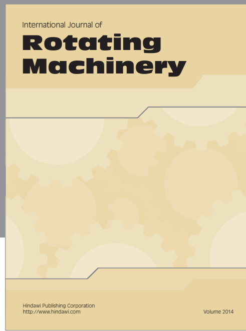
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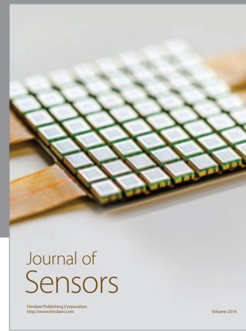
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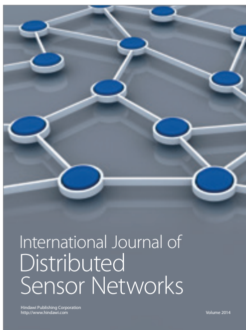
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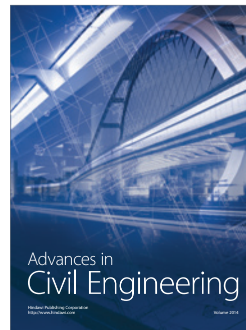
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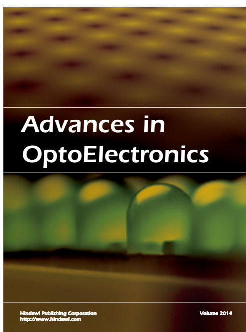
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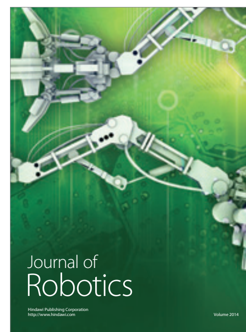
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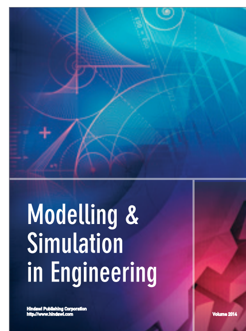
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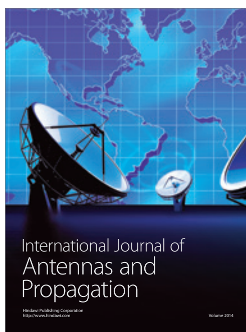
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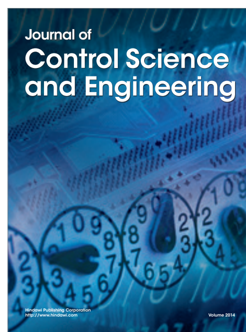
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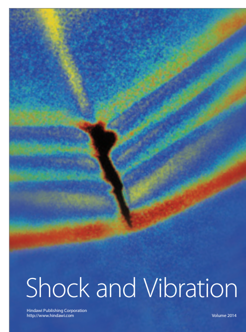
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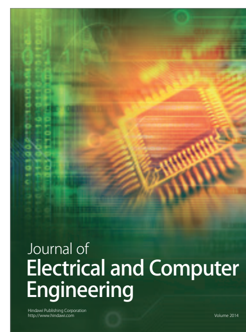
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