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Regular paper

Evolutionary Computing Based Area Integration PWM Technique for Multilevel Inverters

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The existing multilevel carrier-based pulse width modulation (PWM) strategies have no special provisions to offer quality output, besides lower order harmonics are introduced in the spectrum, especially at low switching frequencies. This paper proposes a novel multilevel PWM strategy to corner the advantages of low frequency switching and reduced total harmonic distortion (THD). The basic idea of the proposed area integration PWM (AIPWM) method is that the area of the required sinusoidal (fundamental) output and the total area of the output pulses are made equal. An attempt is made to incorporate two soft computing techniques namely evolutionary programming (EP) and genetic algorithm (GA) in the generation and placement of switching pulses. The results of a prototype seven-level cascaded inverter experimented with the novel PWM strategies are presented.

Keywords: Area integration pulse width modulation (AIPWM), evolutionary programming (EP), genetic algorithm (GA), multilevel inverter, total harmonic distortion (THD).

1. INTRODUCTION

In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]. Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD). Various circuit configurations namely cascaded, diode clamped and flying capacitor etc., have been proposed [2]. Figure 1 shows the cascaded inverter configuration and its output waveform. It is formed by connecting several single-phase H-bridge inverters in series. Each module generates a quarter wave symmetry square voltage waveform with different duty ratios, which together generate the output voltage. Most of the control strategies of multilevel inverter are extension of basic three-level strategies, which offer many degrees of freedom and hence the control methods have an edge over circuit topologies [1], [3-9]. During past two decades, varieties of multilevel PWM methods have been proposed and researched, which have significantly promoted the development of the field. As a rule, the multilevel inverter (multi-carrier) control strategies require large memory when implemented digitally due to more than one (level dependent) carrier/reference functions. In addition, the existing multi-carrier schemes are high switching frequency methods (hence switching losses) since they are basically sinusoidal PWM (SPWM) schemes.

The pioneering work in multilevel inverter control strategies has been reported in 1983 by Bhagwat and Stefanovi who have given a generalized control structure [10]. In 1992, Carrara et al. have proposed a multilevel PWM method and proved its betterment by the lowest harmonic distortion than the other PWM methods [6]. They have developed multilevel sub-harmonic PWM (SHPWM). For an m-level inverter, $m-1$ carriers with the

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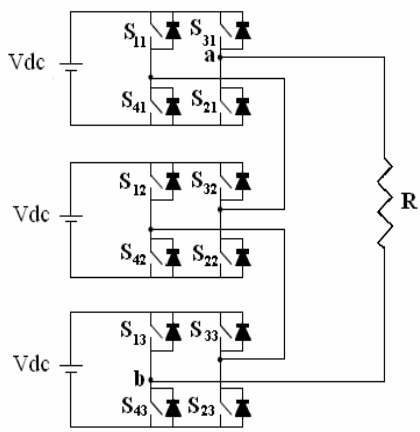
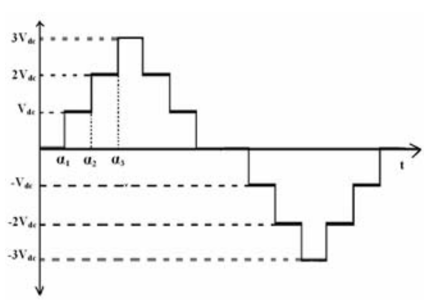
same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are contiguous. The reference or modulation waveform has peak-to-peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device is switched off. In 1999, Tolbert et al. have found that the implementation of the existing control strategies for the diode-clamped inverter affects the switch utilization and thus increasing the losses. With their two carrier based control methods namely switching frequency optimal (SFO) method and variable frequency carrier bands (VFCB) method, they have concluded that by introducing phase shift in the carriers, the effective switching is reduced, besides the VFCB equalizes the number of switching in all levels and results in uniform depreciation of power devices [11]. In 2000, Mcgrath and Holmes have performed an analytical solution of PWM techniques for multilevel inverter and found that the harmonic components produced by alternative phase opposition disposition (APOD) technique in diode clamped inverter is same as that of phase shifted carrier (PSC) technique in cascaded inverter [9]. Calais et al. have analyzed the multi-carrier PWM methods for a single-phase five level inverter [12]. Salam et al. have worked on regular sampled single-carrier PWM method, which has given fairly accurate results due to the fact that the modulating wave is approximate [13].



(a) Circuit configuration



(b) Output waveform for fundamental switching

Figure 1: Seven-level cascaded inverter

Genetic algorithm (GA) is used for many diverse applications such as the traveling salesman problem (TSP), optimal ordering problems, numerical optimization problems, and machine learning methods and is atypical in the field of power electronics. Schutten and Torrey have successfully showed a way to optimize converter control laws related to performance index using GA [14]. Following the same, Ozpineci *et al.* have used GA for optimizing the pulses in a pulse density modulated high frequency ac-ac converter [15]. In 2004, the optimal harmonic output in multilevel converters has been obtained with GA and proved the competence of GA with numerical methods [16]. GA has also been used in inverters by Maswood *et al.* to generate specific harmonic elimination PWM (SHEPWM) switching patterns [17]. The state-of-art shows that GA is used for harmonic elimination in both three-level and multilevel converters and there is no evidence of evolutionary programming (EP) in power electronics.

This paper proposes area integration PWM (AIPWM) method for multilevel inverters. The proposed AIPWM method equalizes the total area of the output pulses with that of the required sine. EP is used in positioning the AIPWM pulses in the respective sampling periods. The results obtained from GA and EP cuddles the AIPWM methods to render minimal THD and higher fundamental voltage. The hardware results of the constructed prototype inverter corroborate the simulation results.

2. AIPWM TECHNIQUE

The methods discussed in the previous section have many drawbacks viz. high frequency switching, discriminating the pulses for different levels, unequal switching of switches, unused levels at low amplitude modulation indices etc. A new technique is proposed in which the total area of the pulses is equalized with the (integrated) area of the required sine and thus it is named as *area integration PWM*. The basic idea of the AIPWM method is shown in Figure 2 for a seven level output with six pulses per half cycles. In the figure the area of the required fundamental output (A_{sine}) is made equal to total area of the pulses, A_{pul} ($A_1 + A_2 + ... + A_6$). The scheming of the pulses is as follows:

Total area of the required sine per half cycle,

$$A_{\text{sine}} = V_m \int_0^{\pi} \sin(\omega t)dt \tag{1}$$

where, V_m is the maximum value of desired output voltage $v_0(t)$. Let 'n' be the number of switching per cycle (should be assumed), 'm' be the number of levels and 'k' be the number of pulses for each level.

$$k = \frac{n}{m-1} \tag{2}$$

$$A_{pul} = \sum_{i=1}^{k} W_{a_i} V_{dc1} + \sum_{i=1}^{k} W_{b_i} V_{dc2} + \sum_{i=1}^{k} W_{c_i} V_{dc3} + \dots \tag{3}$$

where, W_{a_i}, W_{b_i}, W_{c_i} …are the widths of i^th pulse in level 1, level 2, level 3… level m respectively. V_{dc1}, V_{dc2}, V_{dc3} etc. are the voltage values of level 1, level 2, level 3, etc. respectively. The pulse widths for each half cycle can be calculated as follows:

$$A_{tot} = A_{pul} \tag{4}$$

The calculations are done for one half-cycle due to fact that irrespective of level the pulse widths of positive and negative half cycles are the same (quarter wave symmetry). After finding the pulse-widths, the pulses are placed in the respective sampling periods. The sampling period can be computed by dividing the total output cycle by the number of pulses, n. For an 'm' level inverter the minimum value of 'n' is $2(m-1)$. Thus for a seven-level inverter, the number of samples (pulses) per output half cycle can be 6 or 12 or 18 and so on, and thus the minimum number of pulses per half cycle is six. This method may have many optimal solutions as (4) may be satisfied by number of pulse width combinations and thus a probabilistic approach may be applied to find the possible solutions. However, a better output quality may be achieved by proper placement of optimized (AIPWM) pulses in the sampling periods. This control degree of freedom unwraps the opportunity for applying optimization techniques, which could yield even still better performance.

Since the total area of the sine is considered and also there is no restriction in the placement of the pulses, the problem has a larger solution boundary. The probabilistic approaches can solve this problem to a certain extent due to the size of the solution boundary while artificial intelligence techniques can be useful in effective convergence.

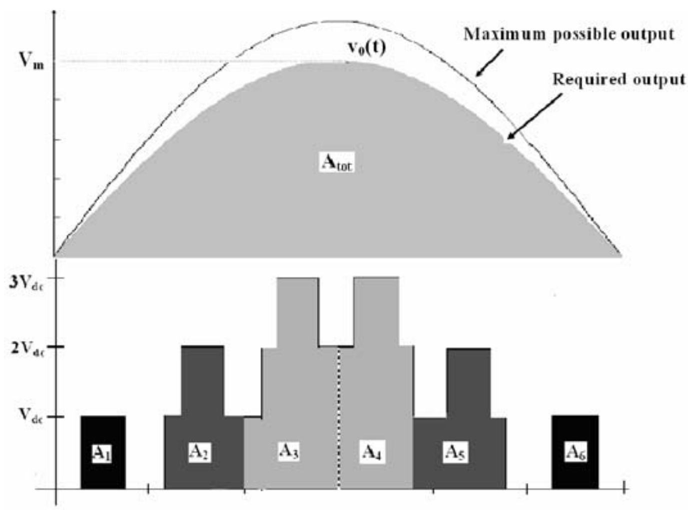


Figure 2 AIPWM scheme for 7-level inverter.

3. EVOLUTIONARY COMPUTING FOR EST

The AIPWM allows the freedom of optimization of the pulse placement to yield better performance. The pulse placements are optimized using evolutionary computing. The state-of-art shows very less evidence of such approach in this field. GA and EP are the optimization tools used to accomplish the task.

3.1 Genetic Algorithm (GA)

GA is a nonlinear problem solving search method, which mimics the biological evolutionary processes [18]. When the same is applied for obtaining pulse positions, the objective function (THD) converges faster to a better value. Since the optimization parameter is real, real-coded GA is used. GA cuddled AIPWM brings faster convergence than the traditional probabilistic approach. The steps involved in GA are as follows.

A. Formation of chromosome

Here, ‘ n ’ sets of output pulses are obtained by AIPWM and then they are placed in the sampling periods. These ‘ n ’ sets are sort in terms of THD and the first 10 sets are chosen as the initial population. The probability of getting lower distortion is high, if the value of ‘ n ’ is chosen high (say 1000). Since this involves genetic processes; the initial population can be named as chromosome.

B. Selection

The chromosome is evaluated for the objective function (THD) and the values of the THD are added and the probability and cumulative probability for each are calculated and assigned. An array of random numbers (size 10) from 0 to 1.0 is generated and for each value, a set from the chromosome is chosen such that its cumulative probability is greater than the random number and that of the previous is less than the random number. The same is repeated for all ten random numbers. This process brings out the fittest chromosome.

C. Cross-over

Cross-over is the exchange of the values in a chromosome. Like the selection process, here also the cross-over probability should be chosen to determine the chromosomes fit for cross-over but in this case, the cross-over probability is not used with the assumption that selection brings out only the fittest. The survival of the fittest is observed in the selection process and they are ready for cross-over. The values of the parameters are exchanged among the chromosomes provided the different levels don’t overlap.

D. Mutation

After selection and cross-over, a random variable is acquired for the chromosome available and the off-springs are obtained by simple addition. After obtaining the off-springs, the performance is evaluated and they are concatenated with the chromosome and again the set is sort in terms of THD. The next set of chromosome is the first 10 sets and the process is repeated until all iterations are over. The logic flow for GA can be understood from the Figure 3.

3.2 Evolutionary Programming (EP)

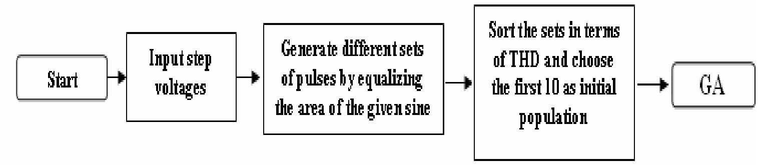
Evolutionary Programming is a powerful computational algorithm for optimization of the control variables to achieve the objective. The following are the progressive steps in EP to the desired output.

A. Formation of initial population

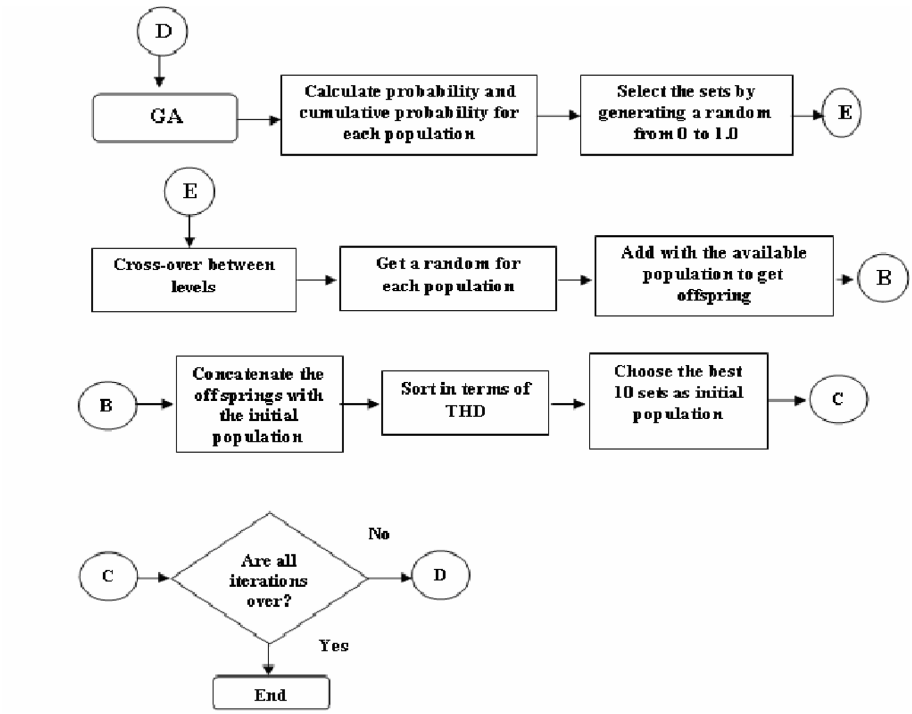
This is similar to that of formation of chromosome in GA and here, ‘n’ sets of output pulses are obtained by AIPWM and then they are placed within the sampling periods. These ‘n’ sets are sort in terms of THD and the first 10 sets are chosen as the initial population. Since EP is a powerful optimization tool; it can give better results even when the value of ‘n’ is lower than in GA.

B. Random variable for each population

To get an off-spring for every population, a random variable is obtained and added with each initial population. After obtaining the off-springs, the performance is sorted in terms of THD. The next set of initial population is the first 10 sets and the process is repeated until all iterations are over. This method involves very less number of steps, thus reduces the computational time and also gives better performance than GA. The logic is explained in Figure 4.



(a) Formation of initial population



(b) Logic flow of GA

Figure 3: GA cuddled AIPWM -Algorithm

4. PERFORMANCE ANALYSIS

The results presented in this section are specially chosen to provide a comparative basis for assessing the performance of the new area integration based switching strategy. The simulation results are obtained using the MATLAB software package.

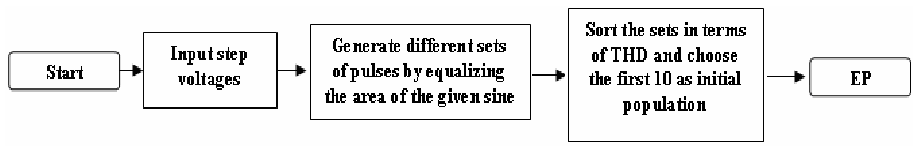
4.1 Simulation Results

The simulation results of AIPWM, GA cuddled AIPWM and EP cuddled AIPWM along with basic SHPWM are presented. In the basic AIPWM, the pulse patterns obtained are sorted in terms of THD and the best is chosen, while GA/EP cuddled AIPWM includes pulse positioning as well. Separate voltage sources (SDC's) of 100V each are considered while the output target is 300V. The AIPWM simulations are performed for $n = 12$ and SHPWM carrier frequency is adjusted for same number of pulses ($f_c = 300\text{Hz}$). Figure 5 (a), (b), (c) and (d) show the harmonic spectrum of output voltages obtained from SHPWM, AIPWM, GA cuddled AIPWM and EP cuddled AIPWM respectively. The following are tacit from the simulated results. By EP, the reduction in THD is found to be around 5%

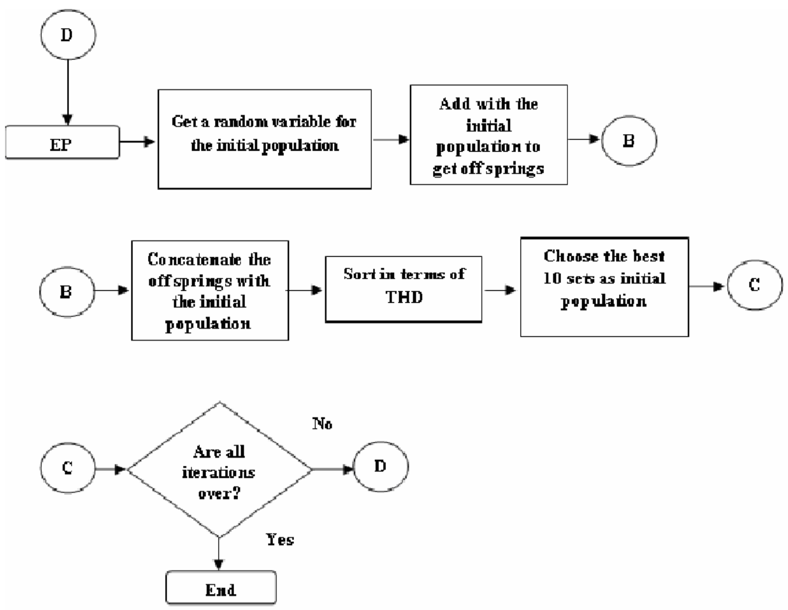
iteration above 135 gives the same response. In GA, the objective function converged in 100 iterations to 13.26% and thus the reduction is found to be around 4%.

Table 1 compares the THD, fundamental and other dominate harmonics for the above methods. The GA and EP are more helpful in reducing harmonics even in lower switching frequencies.

Figure 6 (a) shows the converging rate of program for GA and EP while Figure6 (b) proves the repeatability/reliability of the software. Hence the freedom, which lets the optimization of the pulse positions, gives better performance in both GA and EP.



(a) Formation of initial population

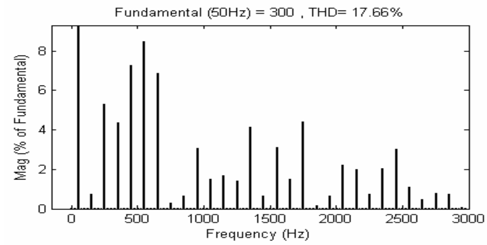


(b) Logic flow of EP

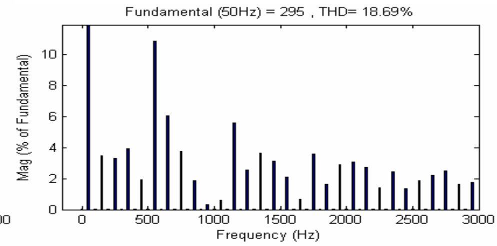
Figure 4: EP cuddled AIPWM –Algorithm

4.2 Hardware Results

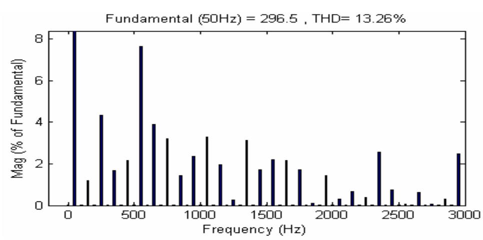
The proposed control strategies are implemented in a seven level-cascaded inverter with the input step voltages of 100V. A Texas Instruments digital signal processor (DSP) TMS320F2407 is employed to generate gate control signals for the switches. The pulses in Figure 7(a) represents pulses of both positive and negative group of devices in bottom H-bridge while Figure 7(b) represents pulses of middle and top H-bridges positive group devices. The representative output waveform is shown in Figure 8 for EP cuddled AIPWM and the harmonic spectrums for all cases are shown in Figure 9. It can be understood that the proposed AIPWM method delivers equal number of switching in all levels. To achieve the same, intensive frequency calculations for different carrier bands (VFCB) is required in the basic carrier based regular sampled SHPWM method [11]. Table 2 reveals the close comparison of the harmonics obtained through simulation and experiment. The AIPWM techniques serve to offer a lower THD and reduced harmonics when compared to SHPWM.



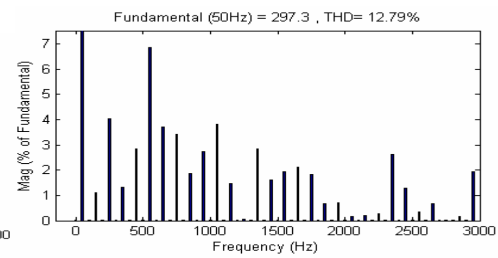
(a) SHPWM



(b) AIPWM



(c) GA cuddled AIPWM

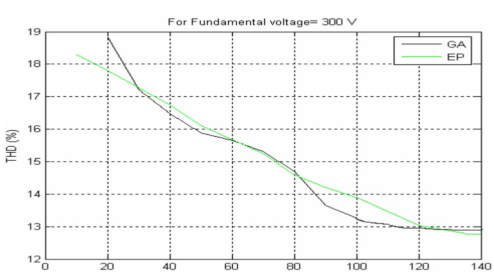


(d) EP cuddled AIPWM

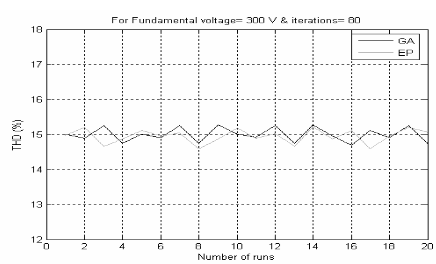
Figure 5: Harmonic spectrum of output voltage

Table 1 Comparison of AIPWM methods

Index	*SHPWM*	*AIPWM (GA)*	*AIPWM (EP)*
THD (%)	17.66	13.26	12.79
V_1 (V)	300	296.5	297.3
V_3 (%)	0.75	1.10	1.10
V_5 (%)	5.32	4.33	4.03
V_7 (%)	4.35	1.66	1.33
V_9 (%)	7.3	2.16	2.83
V_{11} (%)	8.46	7.36	6.85
V_{13} (%)	6.88	3.90	3.73

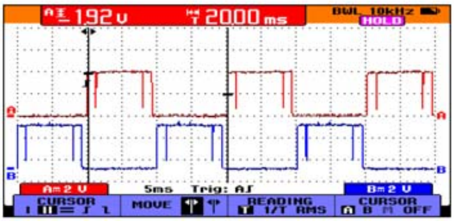


(a) Iterations V_s THD

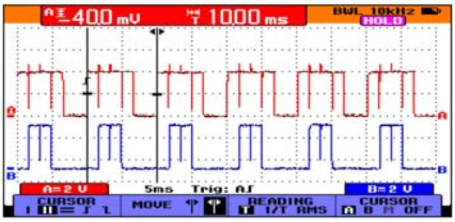


(b) Runs V_s THD

Figure 6: EP V_s GA



(a) Pulses for bottom H-bridge module positive and negative half cycles



(b) Middle and top H-bridge positive half cycle

Figure 7: EP cuddled AIPWM pulses -12 pulses per cycle

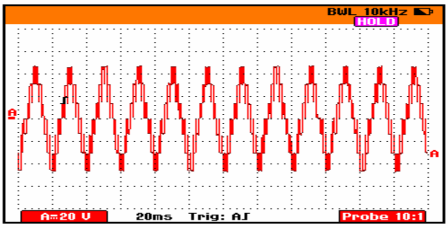
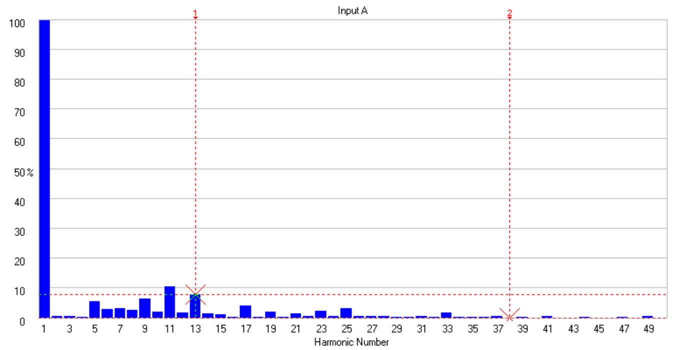


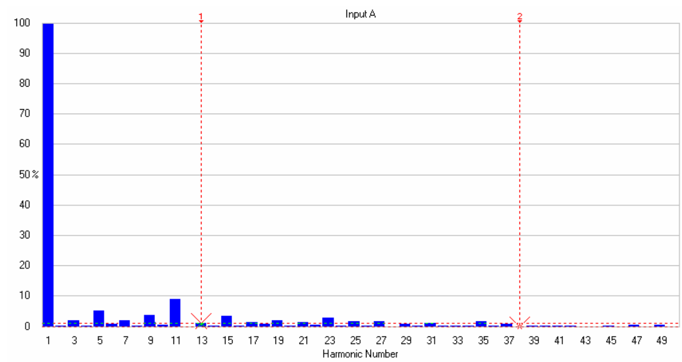
Figure 8: Output waveform-EP cuddled AIPWM

Table 2 Comparison of simulation and experimental results

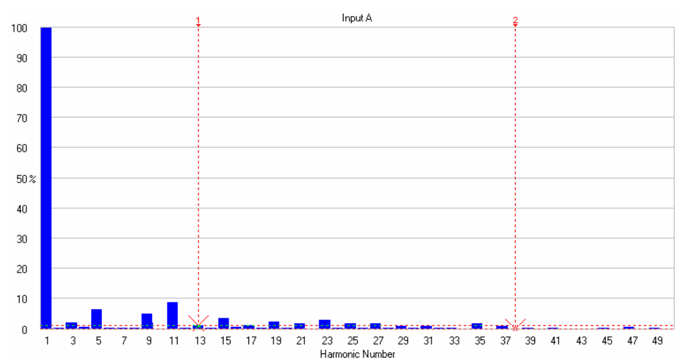
Harmonics		Harmonics		
		SHPWM	**AIPWM (GA)**	**AIPWM (EP)**
THD (%)	Simulation	17.66	13.26	12.79
	Experimental	18.02	13.79	13.09
V_3 (V)	Simulation	0.75	1.10	1.10
	Experimental	1.02	1.34	1.42
V_5 (V)	Simulation	5.32	4.33	4.03
	Experimental	5.78	5.4	4.87
V_7 (V)	Simulation	4.35	1.66	1.33
	Experimental	5.10	2.23	1.78
V_9 (V)	Simulation	7.3	2.16	2.83
	Experimental	8.3	2.56	3.12
V_{11} (V)	Simulation	8.46	7.36	6.85
	Experimental	9.10	8.34	7.23
V_{13} (V)	Simulation	6.88	3.90	3.73
	Experimental	7.12	4.23	3.89



(a) SHPWM



(b) GA cuddled AIPWM



(c) EP cuddled AIPWM

Figure 9: Harmonic spectrum

5. CONCLUSION

This paper has presented a new method of controlling multilevel inverter. The principle of the proposed area integration pulse width modulation technique is equalizing the total area of the output waveform with that of the required sine output per half cycle irrespective of the number of the sample per cycle. The EP and GA calculate the optimal pulse positions based upon the desired inverter fitness function while AIPWM computes the pulse widths. The EP and GA have solved the problem with a simpler formulation and with any number of levels without extensive derivation of analytical expressions. The simulation and hardware results show that for a seven level inverter, the GA/EP cuddled AIPWM can enhance the total harmonic distortion by 5%. These novel methods have served better for low frequency switching (hence high circuit efficiency).

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