COMPUTATIONAL CIRCUITS BASED ON CMOS OPERATING IN SUBTHRESHOLD REGION

BY

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LIST OF ABBREVIATIONS

MOSFET	:	Metal Oxide Semiconductor Field Effect Transistor.
BJT	:	Bipolar Junction Transistor.
KVL	:	Kirchoff's Voltage Law.
NMOS	:	n-channel MOSFET.
PMOS	:	p-channel MOSFET.
OTA	:	Operational Transconductance Amplifier.
AC	:	Alternating Current.
DC	:	Direct Current.
CM	:	Current Mode.
DSBSC	:	Double-Side Band Suppressed Carrier.
THD	:	Total Harmonic Distortion.

ABSTRACT

Full Name : Eyas Saleh Al-Suhaibani

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Analog Computational circuits are used in many analog signal processing systems. Some current mode analog computational circuits using MOSFETs operating in subthreshold region were investigated. Consequently, three computational circuits based on MOSFTs operating in subthreshold region are designed. The first proposed circuit is a multi-function analog computational circuit. This circuit can be used as 4-Q multiplier, 2-Q divider, current-mode differential amplifier, differential-input-single-output current amplifier, and controllable gain current amplifier. The second proposed circuit is a controllable gain square-rooting circuit. This circuit can also be used to compute the geometric mean between two signals with controllable gain. The third proposed circuit is a multi-input analog multiplier. This circuit can be used to multiply three different signals simultaneously. It also can be used to find the cubic of a signal. The designed circuits were simulated using 0.35μm and 0.18μm CMOS technology in Tanner tools to confirm its functionality. Mismatch analysis for all the circuits were carried out to see the effect of mismatch on the performance of the proposed circuits.

ملخص الرسالة

الاسم الكامل: إياس صالح السحيباني

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تعتبر الدوائر التماثلية الحاسوبية مهمة لمعالجة الإشارات في كثير من التطبيقات. في هذا الصدد، تمت دراسة عدة دوائر حسابية تماثلية باستخدام MOSFET يعمل في منطقة تحت جهد العتبة. بعد ذلك، تم تصميم ومحاكاة ثلاث دوائرتماثلية حسابية جديدة. الدائرة الأولى هي دائرة تماثلية متعددة الدوال، هذه الدائرة يمكن ان تستخدم لضرب اشارتين تماثليتين، او لقسمه اشارتين تماثليتين، كما يمكن استخدامها لتضخيم الفرق بين اشارتين او كدائرة تضخيم لتيار اشارة تماثلية. الدائرة الثانية هي دائرة تقوم بحساب الجذر التربيعي مع المقدرة على التحكم بمعامل التضخيم. أما الدائرة الثالثة فهي دائرة تماثلية تقوم بعملية الضرب لعدة اشارات تماثلية. وللتحقق من التصميم النظري تم استخدام برنامج محاكاة تانر لتقنية 0,35 و 0,18 ميكرو متر. ومن ثم تم تحليل الدوائر بافتراض عدم توافق مقاسات الترانزستورات لدراسة تأثير عدم التوافق على اداء هذه الدوائر.

CHAPTER 1

INTRODUCTION

1. 1 Background

As electronics fabrication technology advances, more electronic circuits are observed working in many applications. Nowadays, more and more electronic devices are being used in our daily life. Advances in computational circuits helped utilizing electronic devices to make our life easy. Many of these electronic devices operate from batteries which make a lot of these devices portable. As the number of these portable electronic devices being used increases, it becomes necessary to design computational circuits with very low power consumption. Designing circuits using MOSFETs operating in subthreshold is very good approach to achieve low power consumption. Multiplication, division, squaring, and square-rooting circuits are important analog signal processing blocks. Having such circuits operating in low voltage and low power can add a great advantage for many applications such as wireless sensor networks and biomedical applications.

There are different approaches in designing analog computational circuits. The most commonly used approach is the translinear principle. Although, translinear principle was first applied to BJTs, the same concept is also applicable to MOSFETs as will be discussed in the following section.

1.1.1 Translinear Principle in BJTs

The translinear principle was first introduced by Gilbert in 1975 [2]. Figure 1.1 shows the basic BJT translinear loop.

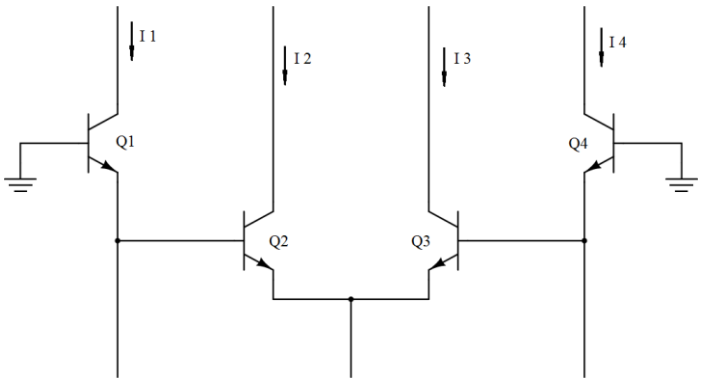


Figure 1.1: Translinear loop formed by BJTs.

Translinear principle states that having an even number of matched PN junctions in a loop with half of them oriented clockwise and the other half oriented counterclockwise, then the following result can be obtained [2]:

$$\prod_{clockwise} I_C = \prod_{counter-clockwise} I_C \quad (1.1)$$

Where I_C represents the current passing through the PN junction. This result opens a door for many analog functions to be implemented using simple circuits. In [2], several mathematical functions were implemented using BJTs.

1.1.2 Translinear Principle in MOSFETs

The fabrication process for CMOS is cheaper and more advanced than that of BJTs. This fact made the MOSFETs more popular nowadays than BJTs. The translinear principle for MOSFETs operating in saturation (strong inversion) can be derived as:

Applying KVL to the translinear loop shown in Figure 1.2 yields the following:

$$\sum_{i=1}^{M/2}(V_{GS})_i = \sum_{j=1}^{M/2}(V_{GS})_j \quad (1.2)$$

Where M is the total number of MOSFETs forming the translinear loop.

Now, since

$$I_D = 0.5KP_n \frac{W}{L}(V_{GS} - V_{Th})^2 \Rightarrow V_{GS} = \sqrt{\frac{I_D}{0.5KP_n \frac{W}{L}}} + V_{Th} \quad (1.3)$$

Where KP_n is the transconductance parameter, W/L is the transistor aspect ratio, V_{GS}, is the gate to source voltage, and V_{Th} is the threshold voltage for the MOSFETs [3]. Then, equation (1.2) can be written as:

$$\sum_{i=1}^{M/2} \left(\sqrt{\frac{I_D}{0.5KP_n \frac{W}{L}}} + V_{Th} \right)_i = \sum_{j=1}^{M/2} \left(\sqrt{\frac{I_D}{0.5KP_n \frac{W}{L}}} + V_{Th} \right)_j \quad (1.4)$$

If all the transistors are identical, then equation (1.4) can be reduced to:

$$\sum_{i=1}^{M/2} \left(\sqrt{I_D} \right)_i = \sum_{j=1}^{M/2} \left(\sqrt{I_D} \right)_j \quad (1.5)$$

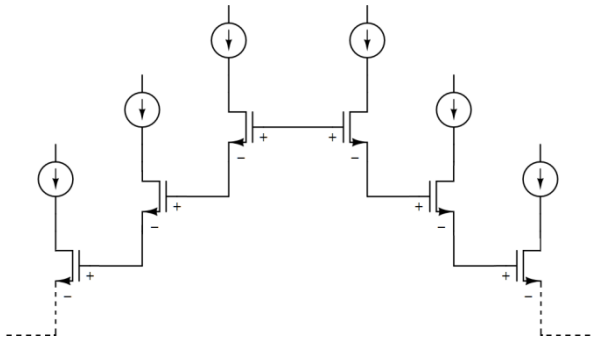


Figure 1.2: Translinear Loop in MOSFET [1].

Thus, for MOSFETs operating in strong inversion, if all transistors are identical then, the summation of the square-root of the currents in one half equals to the summation of square-root of the currents in the other half [1].

Although the result of applying the translinear loop principle on MOSFETs operating in saturation region is not the same as the result if BJTs were used, it is still very helpful and useful. Many circuits were designed using this approach such as the circuits reported in [1] and [4].

To obtain a similar translinear principle of the BJTs using MOSFETs, they must operate in the subthreshold region (weak inversion) since the drain current in this region has an exponential relation with the V_{GS} [3]. The MOSFET drain current in subthreshold region is given by [5]:

$$I_D = \frac{W}{L} I_0 e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} (1 - e^{\frac{-V_{DS}}{V_T}}) \quad (1.6)$$

Where n is the subthreshold exponential slope factor, V_{Th} is the threshold voltage, V_T is the thermal voltage, and I_0 is the current that follows when ($V_{GS} = V_{Th}$) [3]. If the drain to source voltage (V_{DS}) is sufficiently greater than the thermal voltage (V_T), then equation (1.6) can be reduced to [5]:

$$I_D = \frac{W}{L} I_0 e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)} \quad (1.7)$$

Then, V_{GS} can be written as follows:

$$V_{GS} = nV_T \, ln\left(\frac{I_D}{I_0}\frac{L}{W}\right) + V_{Th} \quad (1.8)$$

with reference to Figure 1.2, applying KVL around the translinear loop gives us:

$$\sum_{i=1}^{M/2} (V_{GS})_i = \sum_{j=1}^{M/2} (V_{GS})_j \quad (1.9)$$

Where M is the total number of MOSFETs forming the translinear loop. Substituting equation (1.8) in equation (1.9) yields:

$$\sum_{i=1}^{M/2}\left(nV_T ln\left(\frac{I_D}{I_0}\frac{W}{L}\right)+V_{Th}\right)_i = \sum_{j=1}^{M/2}\left(nV_T ln\left(\frac{I_D}{I_0}\frac{W}{L}\right)+V_{Th}\right)_j \quad (1.10)$$

and if all the transistors are identical, then equation (1.10) can be written as:

$$\prod_{i=1}^{M/2}(I_D)_i = \prod_{j=1}^{M/2}(I_D)_j \quad (1.11)$$

Although this result is obtained by using NMOS transistors, the same result can be obtained when PMOS transistors are used.

1. 2 Design Considerations for MOFETs operating in Subthreshold Region

There are several points to be considered when designing circuits using MOSFETs operating in subthreshold region. In order to discuss these points, the drain current for a MOSFET working in subthreshold must be considered and analyzed. Referring to equation (1.6), it is very clear that V_{DS} voltage has to be sufficiently larger than the thermal voltage throughout the operating voltage range in order for equation (1.11) to be applicable.

The bulk voltage plays a great role in the behavior of the CMOS circuits in subthreshold. This is why many model equations for a MOSFET operating in subthreshold contain this variable [6]. Figure 1.3 shows the subthreshold characteristics for NMOS and PMOS transistors under different V_{DS} conditions and for different values of V_{SB}. As it is clear from the figure, setting V_{SB} to zero makes the characteristics almost independent of any variation in V_{DS} voltage. This can be considered an advantage of setting V_{SB} to zero. It is also clear from the figure that PMOS transistor is more insensitive to V_{DS} variation than NMOS transistors.

Another parameter that must be kept in mind is the subthreshold slope factor (n). This factor is not necessarily constant but setting V_{SB} to zero makes it constant [6]. This is another advantage of setting V_{SB} to zero. Lastly, threshold voltage variation is smaller for PMOS

transistors than for NMOS transistors [6]. There are some problems of using MOSFETs operating in subthreshold region, namely, noise, limited bandwidth, and mismatch between different transistors [3].

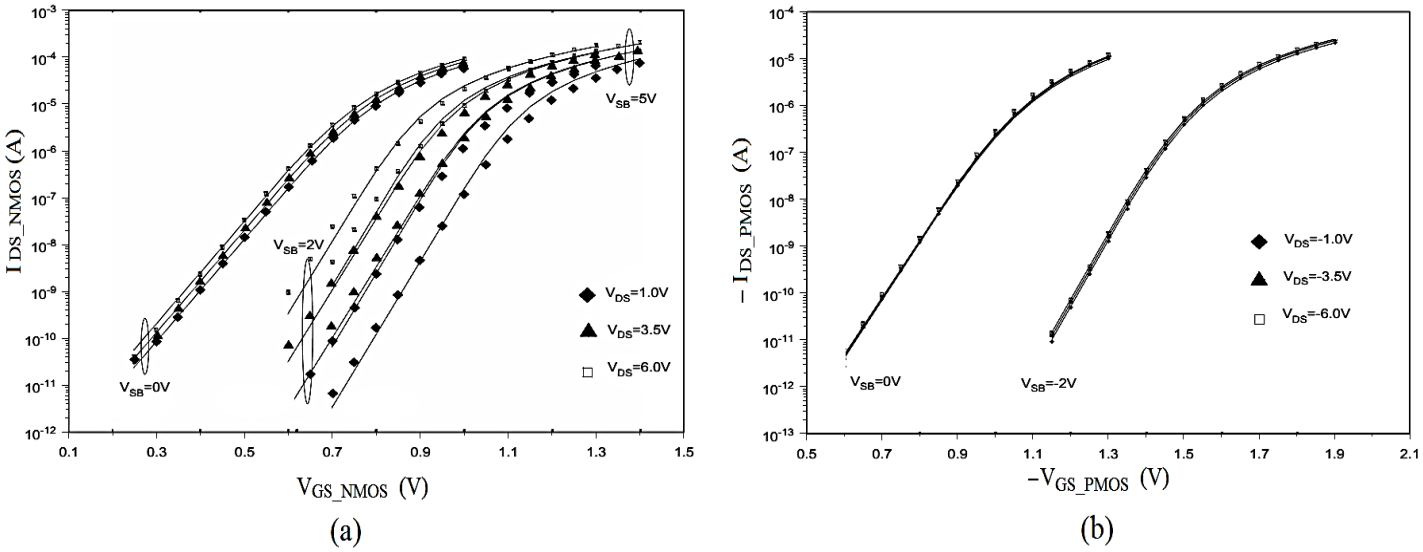


Figure 1.3: Subthreshold characteristics for NMOS and PMOS transistors under different V_{DS} conditions and for different values of V_{SB} [6]. (a) for NMOS and (b) for PMOS.

1. 3 Motivation

Since electronic devices are being used almost everywhere nowadays, and since CMOS fabrication is improving rapidly, it is a good idea to use MOSFETs operating in subthreshold region to design computational circuits. This approach is very suitable for low power applications such as wireless-sensor nodes, and biomedical applications.

1. 4 Problem Definition

Analog computational circuits are important building blocks in analog signal processing. It is desireable to obtain a computational circuit that consumes low power and can implement many functions such as multiplication, and division. It is the aim of this thesis to design and

simulate analog computational circuits that utilizes MOSFETs operating in subthreshold. The analog functions to be obtained are multiplication, division, squaring and square rooting.

1. 5 Thesis Organization

This thesis is organized as follows: Chapter 2 discusses the previously published works. A new multi-function circuit is proposed in chapter 3. In chapter 4, a controllable gain square rooting circuit is presented. Chapter 5 presents the proposed multi-input multiplier. Conclusion and future works are discussed in chapter 6.

CHAPTER 2

LITERATURE REVIEW

There are many approaches reported in the literature to design computational circuits. One approach utilized commercially available devices such as OTAs to implement some computational circuits. In [7] an OTA-based multiplier/divider is proposed. This approach consumes more power than transistor level approach. Another approach uses switched current technique as reported in [8]. This approach suffers from noise associated with the switching. Another approach is to use MOSFETs in saturation region such as the circuits reported in [9] to [11]. In [12], the authors used floating-gate MOS transistors to implement a four quadrant multiplier. Implementing circuits using MOSFETs in saturation region consume more power than if the circuits were designed using MOSFETs in subthreshold region. A good approach is the approach where MOSFETs operating in subthreshold is used. Using this approach, the circuits will consume less power which is a great advantage. Several circuits were proposed in the literature that use MOSFETs in subthreshold. In [13] to [15], voltage mode multipliers were proposed using MOSFETs in subthreshold region. The dynamic range of these circuits is limited because the transistors are working in subthreshold region and because the design involves some approximations such as Taylor series expansion. In [16], and [17], the authors utilize the relation between the drain current and the gate to bulk voltage to achieve a multiplier. This approach suffers from the error associated with body effect. A very promising approach is the approach where translinear principle using MOSFETs operating in subthreshold is used. This approach is very attractive because multiplication and division processes exist inherently once the translinear loop is formed. There are several designs reported in the literature that use this approach. Below,

some designs that utilize the translinear principle for MOSFETs operating in subthreshold are discussed.

2. 1 Multipliers

In the following subsections, some multipliers designed using MOSFETs operating in subthreshold are discussed.

2.1.1 Four-Quadrant analog Multiplier/Divider

A four-quadrant multiplier/divider based on the translinear principle of MOSFET working in subthreshold was reported in [5]. The reported circuit is shown in Figure 2.1.

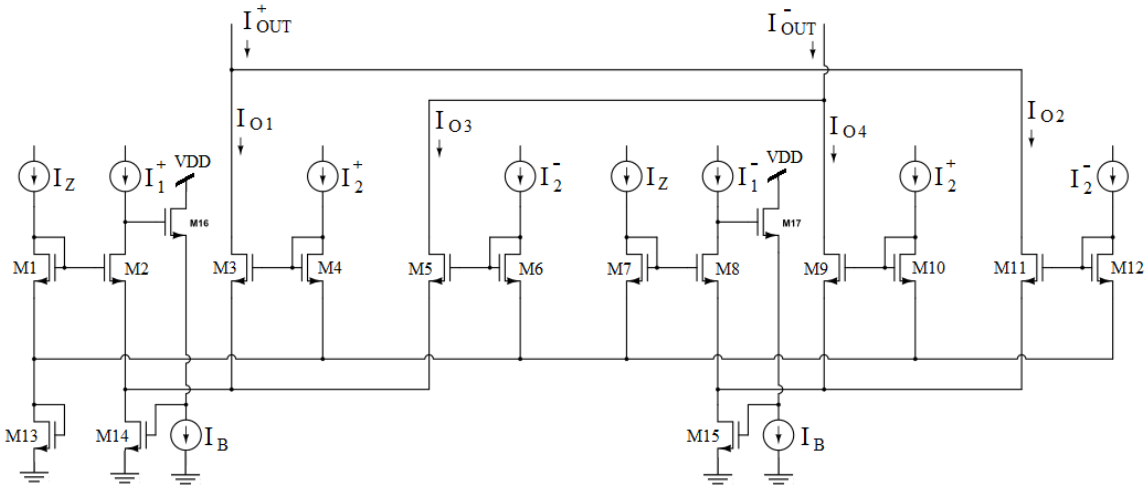


Figure 2.1: Multiplier/divider reported in [5].

The circuit requires two differential input currents which are I_1^+, I_1^- , I_2^+ , and I_2^-. They are differential AC currents with a DC offset to allow the four-quadrant multiplication. The circuit has also a third input current which can be thought as a reference current when performing multiplication and an input signal when performing a division. The circuit consists of four translinear loops. They are formed by these transistors:

1. M_1 ,M_2, M_3, and M_4.

2. M_7 ,M_8, M_{11}, and M_{12}.

3. M_1 ,M_2, M_5, and M_6.

4. M_7 ,M_8, M_9, and M_{10}.

The output current can be derived to be:

$$I_{out} = \frac{4\, i_x i_y}{I_Z} \tag{2.1}$$

The following points can be said about the circuit in Figure 2.1 above:

- It utilizes large number of transistors.
- It requires duplicated and inverted copies of the two input currents.
- The output is taken by subtracting the two output currents which requires a couple of transistors to form a current mirror.
- In [5], it was reported that the bandwidth of the circuit is 19MHz. However, the frequency response was shown in a figure in [5] and the figure shows a -3dB point at frequency less than 10MHz; See Figure 2.2. Also, the circuit has large number of transistors which is expected to limit the bandwidth of operation.

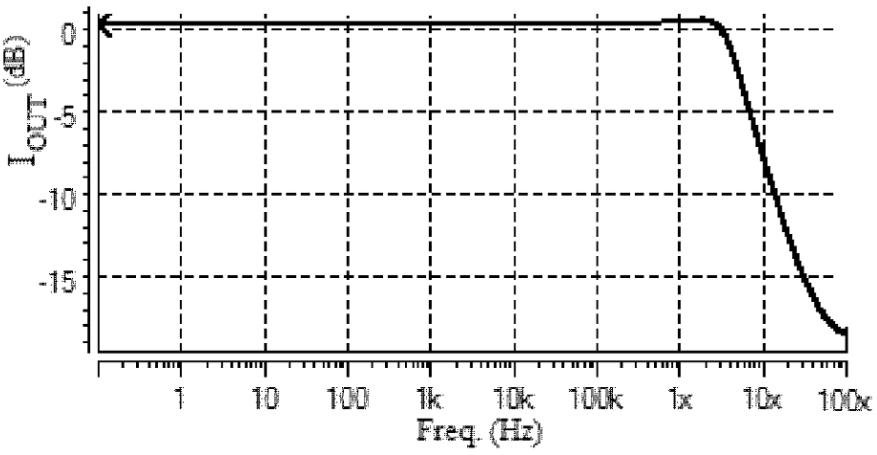


Figure 2.2: Frequency response figure shown in [5].

2.1.2 VLSI Analog Multiplier/Divider Circuit.

Another four-quadrant multiplier/divider based on the translinear principle of MOSFET working in subthreshold was reported in [18]. The work is based on the circuit shown in Figure 2.3.

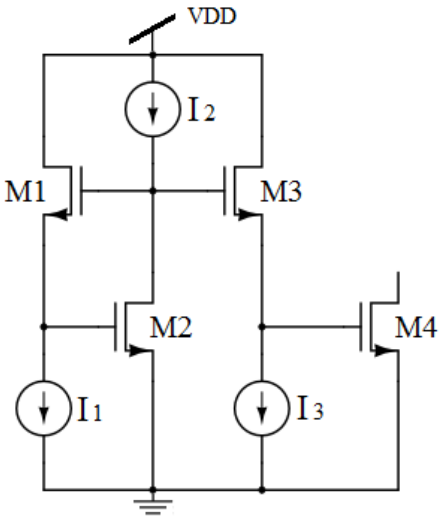


Figure 2.3 Multiplier circuit reported in [18].

The circuit consists of four matched transistors which form a translinear loop. The output current can be proved to be as follows:

$$I_{out} = I_4 = \frac{I_1 I_2}{I_3} \qquad (2.2)$$

Now, two simple modifications can be done so that the circuit can achieve a four quadrant multiplier. The modifications are as follows:

1. All the input currents have equal DC biasing current (I_0). The input signals are added or subtracted from this DC current [18].
2. Three components (I_0, i_1, and i_2) must be subtracted from the output current of the translinear loop [17].

With these modifications, the output current can be shown to be:

$$I_4 = I_0 + i_1 + i_2 + \frac{i_1 i_2}{I_0} \quad (2.3)$$

After subtracting the three components mentioned above,

$$I_{OUT} = I_4 = \frac{i_1 i_2}{I_0} \quad (2.4)$$

I_0 can be considered to be as a reference current when performing a multiplication and an input signal when performing a division [17].

2.1.3 Four quadrant Multiplier

A four quadrant multiplier was reported in [19] and it is shown in Figure 2.4 below. It is an improved version of the conventional multiplier used in [20]. It consists of six transistors that form two overlapping transliear loops. The first translinear loop is formed by the transistors M_1, M_2, M_3 and M_4. The second tranlinear loop is formed by the transistors M_1, M_2, M_5, and M_6.

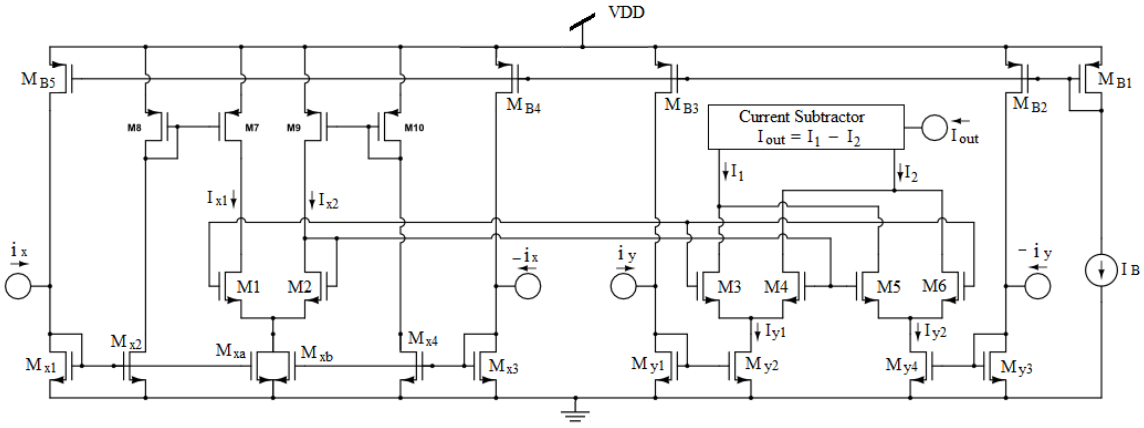


Figure 2.4: Four quadrant multiplier reported in [19].

Assuming all transistors are matched and working in subthreshold. It was reported in [19] that the output current to be:

$$I_{out} = \frac{2 i_x i_y}{I_B} \quad (2.5)$$

The following points can be said about the circuit shown in Figure 2.4 above:

- The circuit requires two differential input signals which require several current mirrors.
- The two differential inputs are AC signals added to or subtracted from the biasing current I_B [19].
- The output current is the difference between I_1 and I_2. Thus, a current mirror is needed at the output.
- Since the circuit utilizes large number of current mirrors, it is very sensitive to device mismatch. For example, if there is a mismatch between M_{xa} and M_{xb}, there will be some error associated with the input i_x.

2. 2 Comparison

Table 1 below summarizes the simulation results of some of the proposed analog multipliers.

Table 1: Simulation results of some reported works in the literature.

Reference	**[5]**	**[21]**	**[19]**	**[22]**
Year	2007	2005	2011	2013
Power Supply	2V	2V	1V	±0.75V
Technology (µm)	0.35	0.35	0.18	0.35
Bandwidth	<10MHz*	200kHz	768kHz	2.3MHz
THD	<1%	0.90%	1.30%	0.7%
Linearity error	2.8%	5%	0.88%	0.3%
Power Consumption (W)	9µ	5.5µ	1.12µ	2.3µ

* See section 2.1.1 and Figure 2.2.

2. 3 Squaring and square rooting circuits

Square rooting circuit is one of the most important analog blocks as it is used in instrumentation and measurement systems [23]. There are many square rooting circuits reported in the literature. OTA based square rooting circuits reported in [23] and [24] consume relatively more power than those designed using MOS transistors. Many of the MOSFET based square rooting circuits utilize MOSFETs operating in strong inversion as in [25]. Square rooting CMOS circuits operating in strong inversion are more popular than square rooting circuits operating in subthreshold. Two published works [26] and [27] use CMOS circuits operating in subthreshold region to implement square rooting circuit. In [27] the authors use a floating gate MOS to obtain a n-th root circuit. Two circuits were reported in [26] one for square rooting and the other one is for squaring. Square rooting circuit is shown in Figure 2.5. As it is clear from the figure, the circuit consists of four MOSFETs that form a transliear loop.

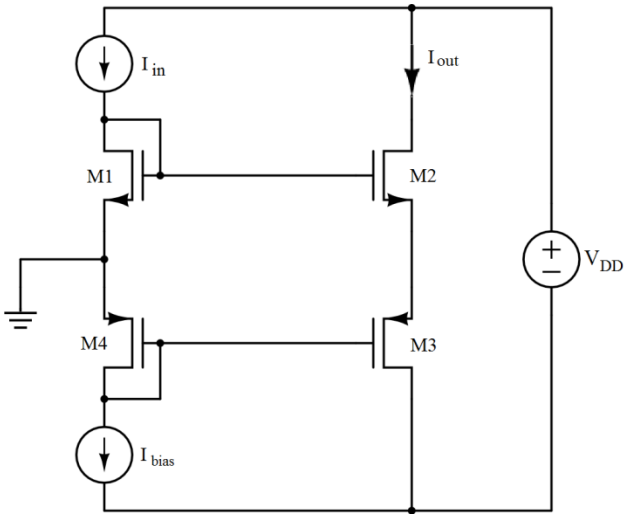


Figure 2.5: Square rooting circuit reported in [26].

A transliear loop is formed by the transistors M_1 to M_4. Assuming all of the four transistors are identical and referring to equation (1.8), the output current can be derived to be [26]:

$$I_{out} = I_2 = I_3 = \sqrt{I_{in}\, I_{bias}} \qquad (2.6)$$

The following points can be said about the circuit shown in Figure 2.5 above:

- In [26], the subthreshold slope factor (n) was omitted from the drain current equation or assumed to be equal to 1 for both PMOS and NMOS. This is not necessarily correct.
- In [26], a large resistor was used to minimize the error for square rooting circuit. The resistor is placed between M_2 and M_3. This resistor will occupy large area on the chip which increases the fabrication cost.
- Its gain control is very limited since only I_{bias} can control the gain.

The squaring circuit is shown in Figure 2.6. It is very similar to the circuits shown in Figure 2.3 but with small modification. That is, two transistors that form the transliear loop are diode connected and they are connected in series.

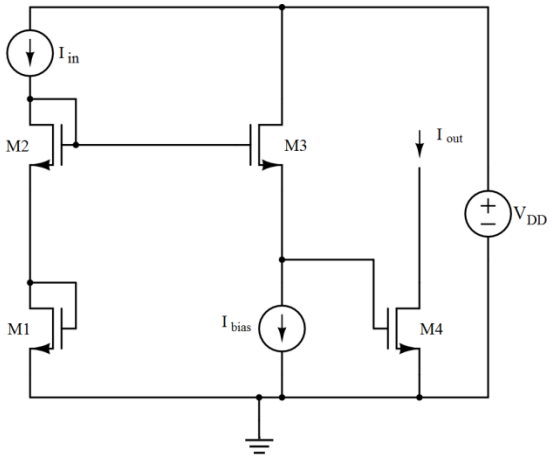


Figure 2.6: Squaring circuit reported in [26].

The output current was reported to be:

$$I_{out} = I_4 = \frac{I_{in}^2}{I_{bias}} \quad (2.7)$$

The following points can be said about the circuit shown in Figure 2.6 above:

- Its gain control is very limited since only I_{bias} can control the gain.
- The output current can be applied to non-grounded load. If it is to be used for grounded load, a current mirror is needed.

CHAPTER 3

PROPOSED CMOS CURRENT-MODE ANALOG MULTI-FUNCTIONS CIRCUIT

Although there are many published current-mode analog multipliers and dividers like the ones discussed in chapter 2, many of them are designed to work only as multipliers and dividers such as the circuits proposed in [5], [19], and [21]. Having a single circuit that can perform more than one function is preferable. In this chapter, a circuit that can do five functions using CMOS transistors working in subthreshold region is proposed. The five functions are multiply, divide, controllable-gain current amplifier, current-mode differential amplifier, and differential-input-single-output current amplifier.

3. 1 Proposed circuit

The proposed circuit is shown in Figure 3.1. It consists of six transistors operating in subthreshold. These transistors form two overlapping translinear loops. The first transistor loop is formed by transistors M_1, M_2, M_3, and M_4. The second translinear loop is formed by transistors M_1, M_3, M_5, and M_6.

Appling KVL to the two translinear loops yields the following:

$$V_{SG1} - V_{SG3} + V_{SG2} - V_{SG4} = 0$$

$$\Rightarrow V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \quad (3.1)$$

$$V_{SG1} - V_{SG3} + V_{SG5} - V_{SG6} = 0$$

$$\Rightarrow V_{SG1} + V_{SG5} = V_{SG3} + V_{SG6} \quad (3.2)$$

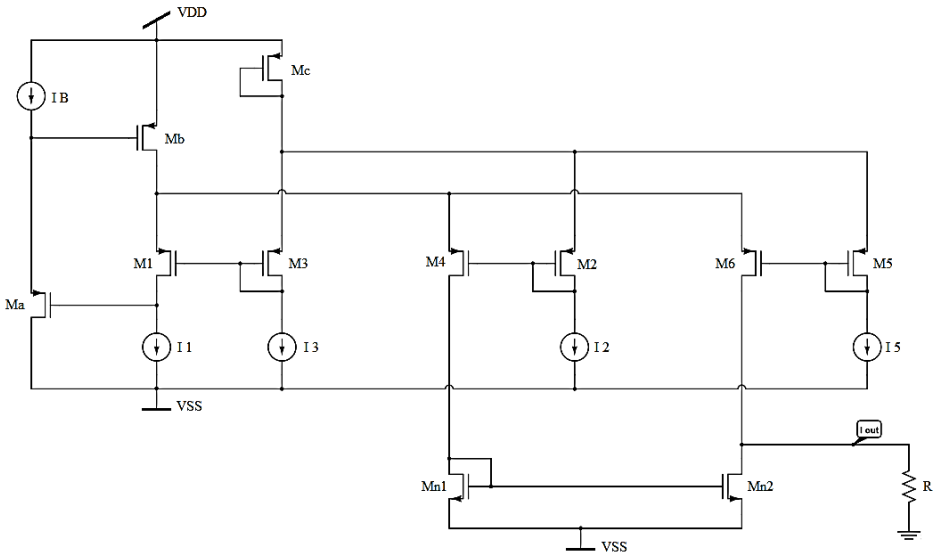


Figure 3.1: The proposed multi-function circuit.

Assuming all transistors forming the translinear loops are matched and substituting the PMOS version of equation (1.8) back into equations (3.1) and (3.2) yields equations (3.3) and (3.4):

$$I_1 I_2 = I_3 I_4 \tag{3.3}$$

$$I_1 I_5 = I_3 I_6 \tag{3.4}$$

Where, I_i is the drain current for the transistor M_i.

Let I_4 be the output of the first translinear loop and I_6 be the output of the second transliear loop. The difference between the two output currents is considered as the output of the proposed circuit and is given by:

$$I_{out} = I_4 - I_6 = \frac{I_1(I_2 - I_5)}{I_3} \tag{3.5}$$

By modifying the input currents, the proposed circuit can implement many functions as will be shown in the next subsections. Table 2 summarizes these functions.

Table 2: Functions that can be implemented using the proposed multi-function circuit.

Function	Conditions	$I_{out} = I_4 - I_6$
4-Q Multiplier	$I_1 = I_0 + i_{in1}$ $I_2 = I_0 + i_{in2}$ $I_3 = I_0$ $I_5 = I_0 - i_{in2}$ And $2i_{in2}$ must be subtracted from the output.	$I_{out} = \frac{2i_{in1}i_{in2}}{I_0}$
2-Q Divider	$I_1 = I_{Gain}$ $I_2 = I_0 + i_{in1}$ $I_3 = I_{in2}$ $I_5 = I_0 - i_{in1}$	$I_{out} = 2I_{Gain}\frac{i_{in1}}{I_{in2}}$
CM Differential Amplifier	$I_1 = I_{Gain1}$ $I_2 = I_0 + i_{in1}$ $I_3 = I_{Gain2}$ $I_5 = I_0 + i_{in2}$	$I_{out} = \frac{I_{Gain1}}{I_{Gain2}}(i_{in1} - i_{in2})$
Differential Input Single Output Current Amplifier	$I_1 = I_{Gain1}$ $I_2 = I_0 + i_{in1}$ $I_3 = I_{Gain2}$ $I_5 = I_0 - i_{in1}$	$I_{out} = 2\frac{I_{Gain1}}{I_{Gain2}}(i_{in1})$
Controllable Gain Current Amplifier	$I_1 = I_{Gain1}$ $I_2 = I_0 + i_{in1}$ $I_3 = I_{Gain2}$ $I_5 = I_0$	$I_{out} = \frac{I_{Gain1}}{I_{Gain2}}(i_{in1})$

3.1.1 Four-quadrant multiplier

The proposed circuit can be used as a four-quadrant multiplier if the currents I_1, I_2, I_3, and I_5 are set to the value shown below:

$I_1 = I_0 + i_{in1}$

$I_2 = I_0 + i_{in2}$

$I_3 = I_0$

$I_5 = I_0 - i_{in2}$

The currents i_{in1} and i_{in2} are AC input signals shifted by a DC quantity (I_0). Substituting the above values into equation (3.5), it is easy to show that:

$$I_4 - I_6 = 2i_{in2} + \frac{2i_{in1}i_{in2}}{I_0} \quad (3.6)$$

If the $2i_{in2}$ term is subtracted from equation (3.6), a four-quadrant multiplier can be achieved , and the output current is given by:

$$I_{out} = \frac{2i_{in1}i_{in2}}{I_0} \tag{3.7}$$

It is very clear that this four-quadrant multiplier can implement squaring function if $i_{in1} = i_{in2} = i_{in}$. Then, the output current is given by:

$$I_{out} = \frac{2{i_{in}}^2}{I_0} \tag{3.8}$$

3.1.2 Two-quadrant divider

The proposed circuit can implement a two-quadrant divider as follows. With reference to equation (3.5), if currents I_1,I_2, I_3, and I_5 were set to the values shown below:

$I_1 = I_{Gain}$

$I_2 = I_0 + i_{in1}$

$I_3 = I_{in2}$

$I_5 = I_0 - i_{in1}$

Then the output current is given by:

$$I_{out} = I_4 - I_6 = 2I_{Gain}\frac{i_{in1}}{I_{in2}} \tag{3.9}$$

It is clear that equation (3.9) implements a divide function with controllable gain.

3.1.3 Current Mode Differential Amplifier

Referring to equation (3.5), the proposed circuit can also be used as a current mode differential amplifier. Consider the following values for the translinear loop currents:

$I_1 = I_{Gain1}$

$I_2 = I_0 + i_{in1}$

$I_3 = I_{Gain2}$

$I_5 = I_0 + i_{in2}$

The currents I_1, and I_3 are used to control the gain of the differential amplifier, the output current is given by:

$$I_{out} = I_4 - I_6 = \frac{I_{Gain1}}{I_{Gain2}}(i_{in1} - i_{in2}) \quad (3.10)$$

3.1.4 Differential Input Single Output Current Amplifier

Differential-input-single-output current amplifier is achieved, if the translinear loop currents are set to be as follows:

$I_1 = I_{Gain1}$

$I_2 = I_0 + i_{in1}$

$I_3 = I_{Gain2}$

$I_5 = I_0 - i_{in1}$

The output is given by:

$$I_{out} = I_4 - I_6 = 2\frac{I_{Gain1}}{I_{Gain2}}(i_{in1}) \quad (3.11)$$

It is clear that equation (3.11), implements a differential input single output amplifier with flexible gain control using currents I_{Gain1} and I_{Gain2}.

3.1.5 Controllable Gain Current Amplifier

If one of the inputs (say i_{in2}) in the current mode differential amplifier is set to zero, then a controllable gain current amplifier is obtained. That is, if the translinear loop currents are set the following values:

$I_1 = I_{Gain1}$

$I_2 = I_0 + i_{in1}$

$I_3 = I_{Gain2}$

$I_5 = I_0$

Following the same procedure, the output will be as follows:

$$I_{out} = I_4 - I_6 = \frac{I_{Gain1}}{I_{Gain2}}(i_{in1}) \quad (3.12)$$

3. 2 Simulation Results

Tanner T-spice with 0.35µm CMOS technology is used to confirm the functionality of the proposed circuit. Table 3 shows the aspect ratios for all transistors used in the simulation. The circuit operates from ±0.75V DC supply, I_B was set to 10nA, and the input currents for the multiplier were swept from -20nA to 20nA. Simulation result shown in Figure 3.2 confirms the functionality of the four-quadrant multiplier and it may be clear that there is a very small offset. This offset is the result of having a small mismatch between the DC biasing currents.

Table 3: Transistors aspect ratio of the proposed multi-function circuit.

Transistor	M_a and M_b	M_c	$M_1 – M_6$	$M_{n1} – M_{n2}$
W(µm)/L(µm)	50/0.4	10/0.4	9.2/5	1.5/4.5

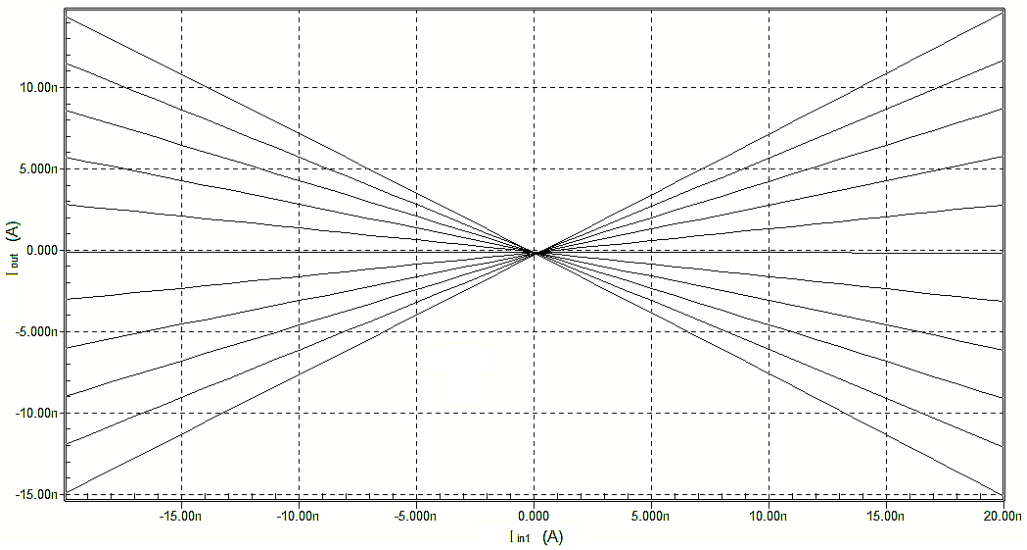


Figure 3.2: Multiplier DC transfer curve.

Application of the multiplier as DSBSC modulator was simulated and the simulation result is shown in Figure 3.3. In that figure, i_{in1} is a sinusoidal signal with frequency of 50kHz and i_{in2} is a sinusoidal signal with frequency of 1kHz.

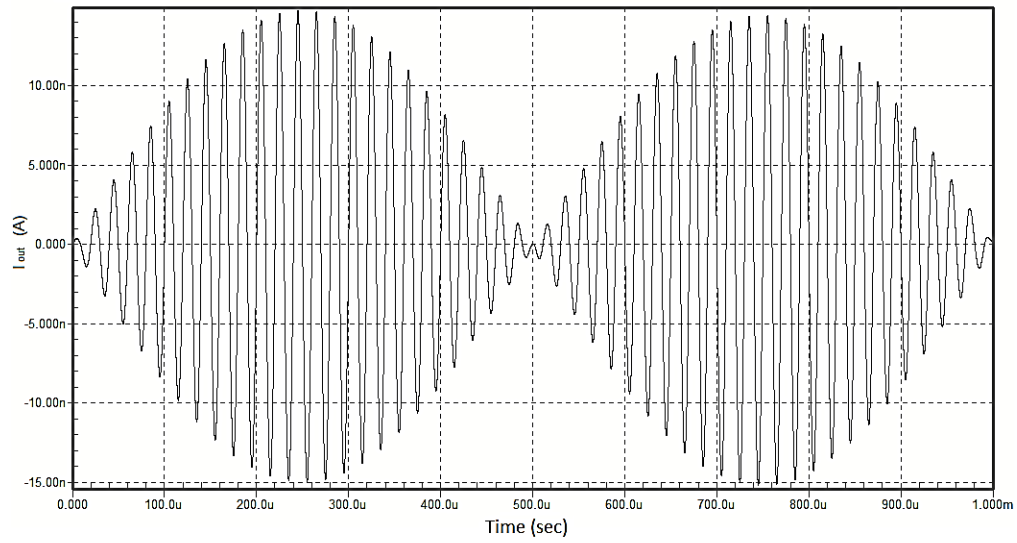


Figure 3.3: Multiplier as DSBSC AM modulator.

A squaring function can be achieved if the same input signal is applied to both inputs of the multiplier. Figure 3.4 shows the DC transfer curve of the squaring function. Figure 3.5 shows the simulation result of squaring an input sinusoidal signal with frequency of 1kHz and amplitude of 20nA. Simulation result confirms the functionality of the circuit. Also, the offset is may be obvious in this case.

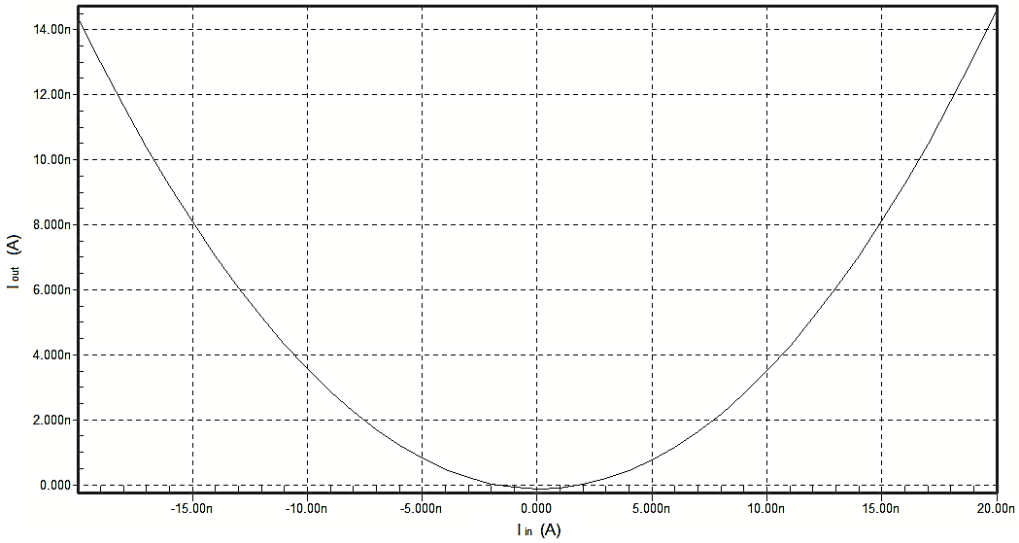


Figure 3.4: Squaring DC transfer curve.

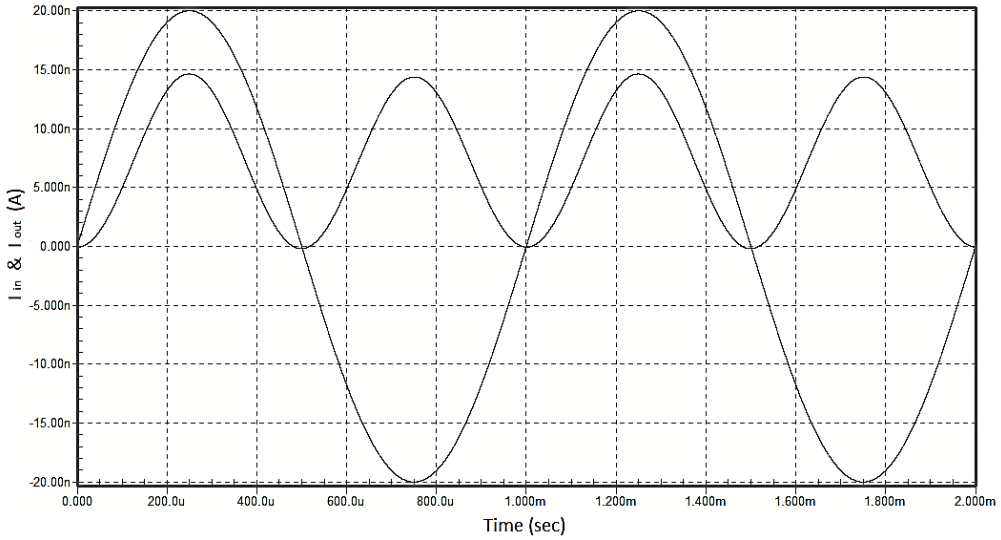


Figure 3.5: Simulation result for squaring function.

Simulation result when using the proposed circuit as a two quadrant divider to divide a DC signal by a triangular signal is shown in Figure 3.6. Also, Figure 3.7 shows the result of dividing a sinusoidal signal by a triangular signal.

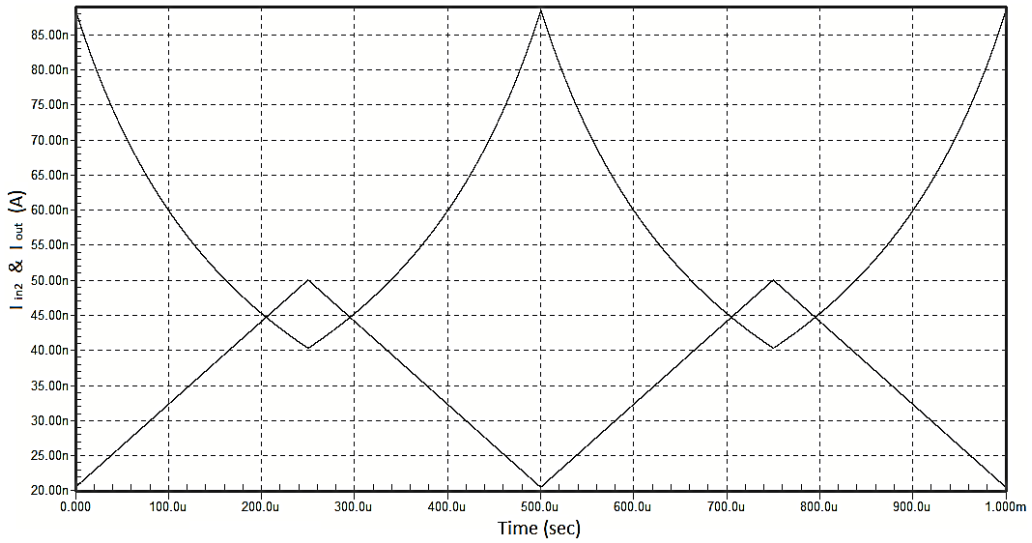


Figure 3.6: Simulation result of the divide function.

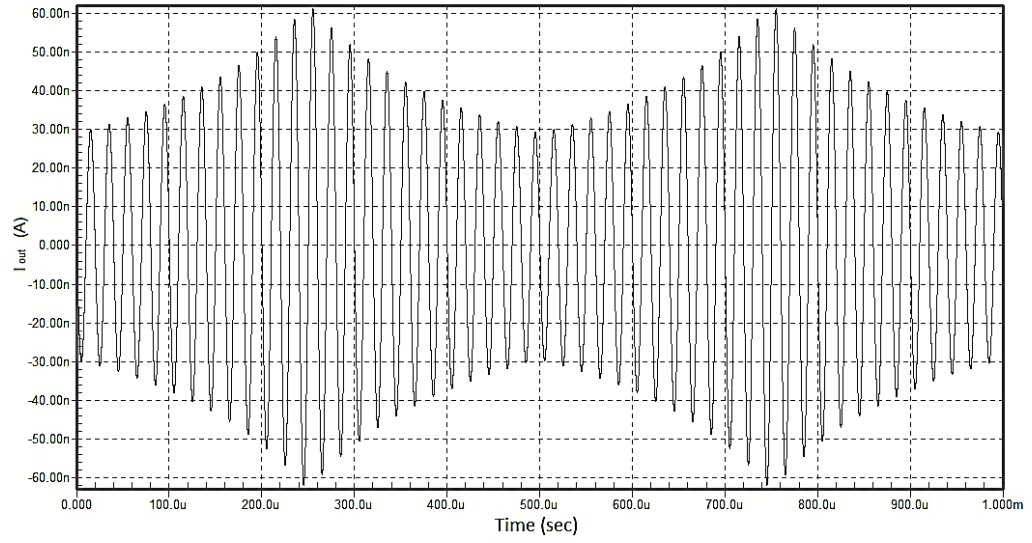


Figure 3.7: Simulation result of the divide function.

Simulation for frequency response was carried out and the result is shown in Figure 3.8. It is clear from the plot that that the -3dB frequency is around 1MHz. The Total Harmonics

Distortion (THD) of the proposed circuit (when configured as an amplifier) was calculated by applying a sine wave signal with frequency of 1kHz and then calculating the ratio of the power of the 1000 harmonics to the power of the fundamental frequency. The THD came to be 0.17%. Simulation result also shows linearity error of around 0.5%.

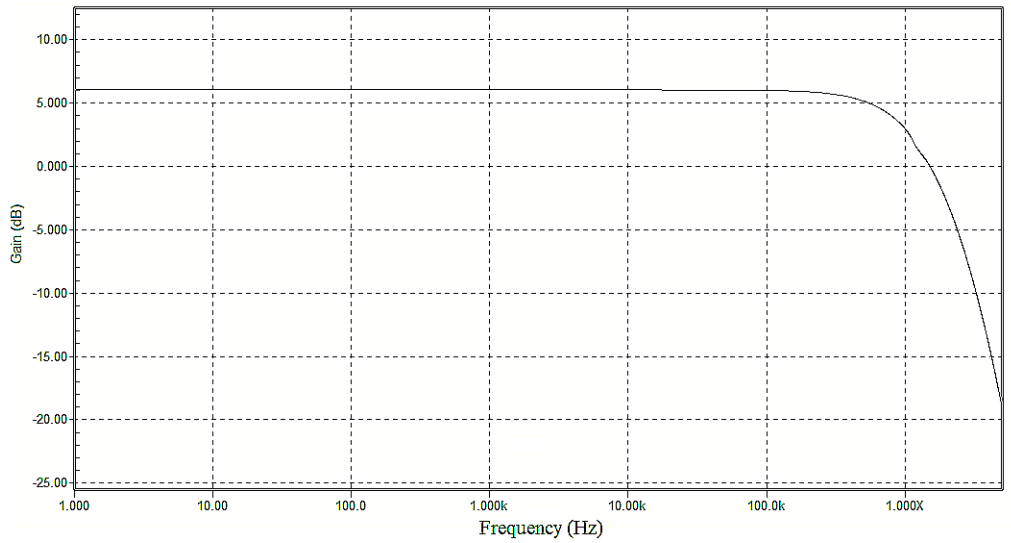
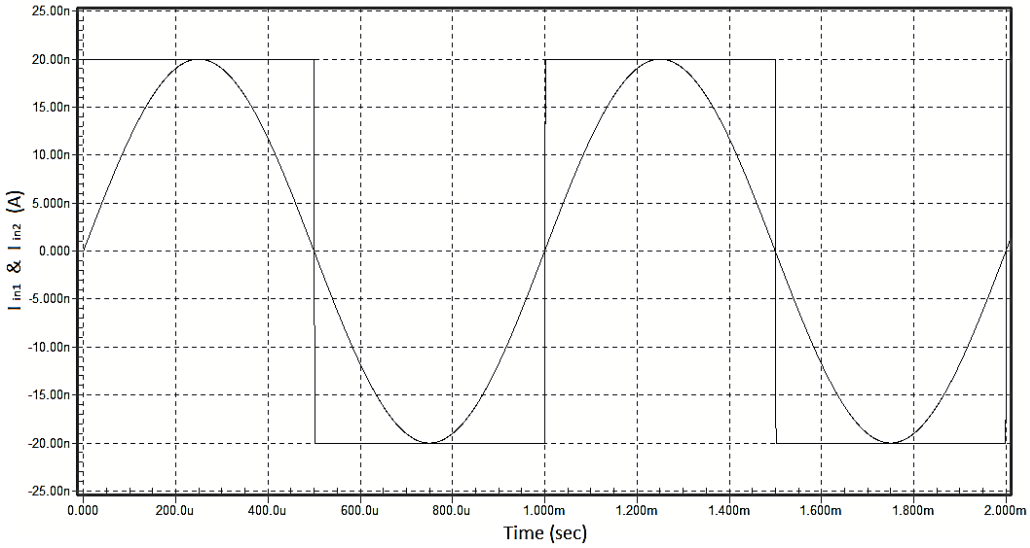
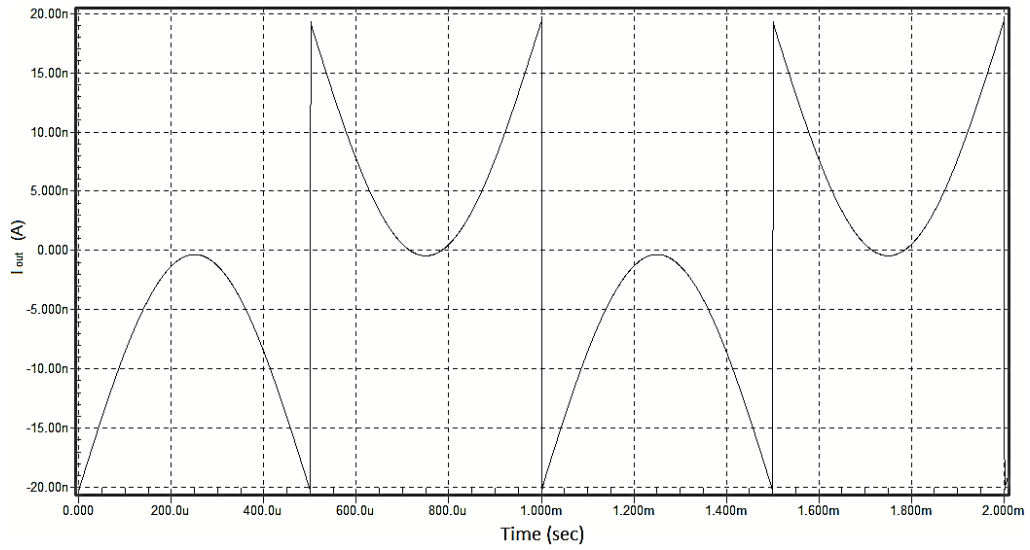


Figure 3.8: Frequency response of the proposed multi-finction circuit.

Figure 3.9 (a) and (b) shows the input and output current signals respectively when using the circuit as a current-mode differential amplifier. It is clear that the circuit is subtracting the square signal from the sinusoidal one.



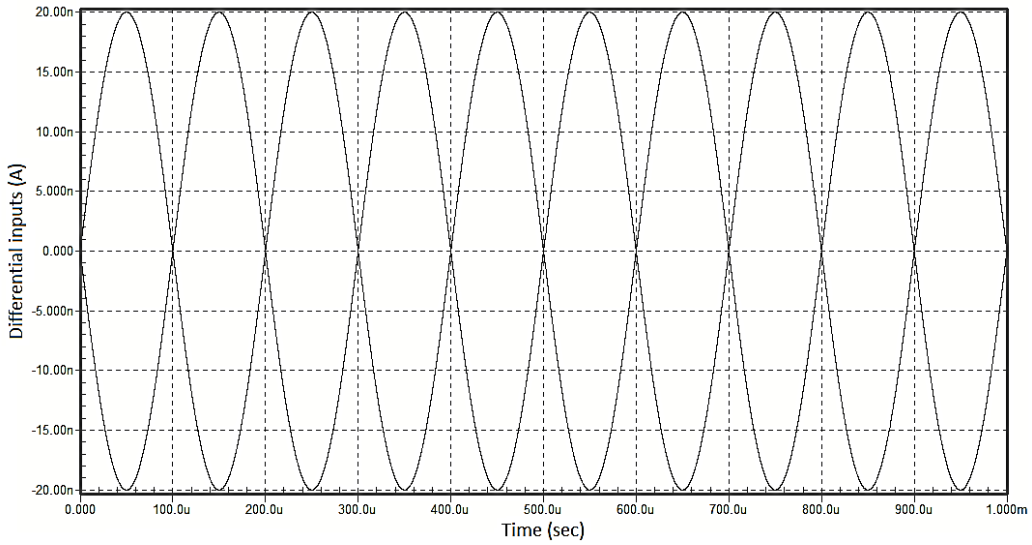
(a)



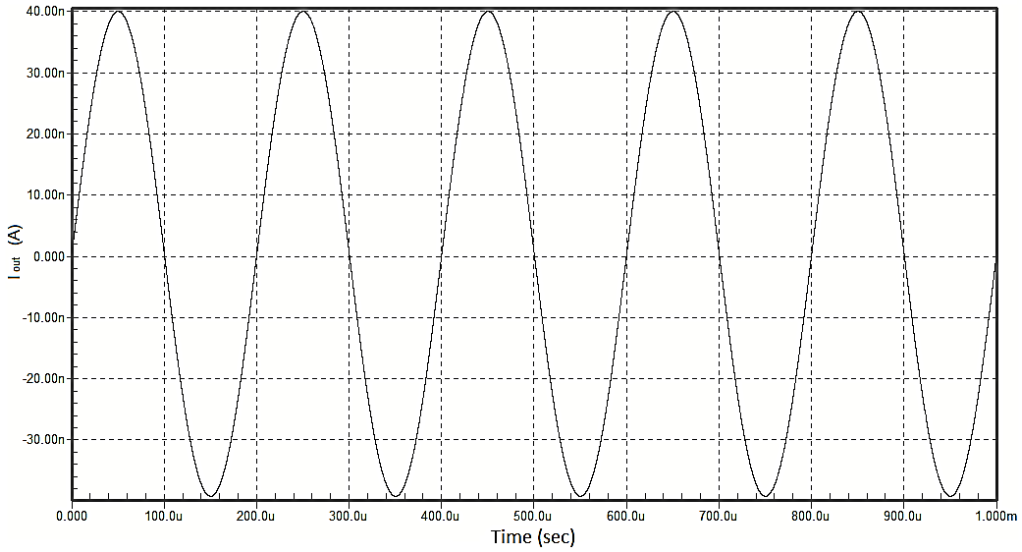
(b)

Figure 3.9: Simulation results for differential amplifier (a) input signal (b) output signal.

The circuit was simulated for a differential-input single-output current amplifier. The differential input and output signals are shown in Figure 3.10 (a) and (b) respectively.



(a)



(b)

Figure 3.10: Simulation result for differential input single output amplifier (a) differential input signals (b) output signal.

Figure 3.11 shows the simulation result for the differential-input single-output current amplifier when I_{Gain1} is varied from 70nA to 30nA. It is clear that the gain of the output changes accordingly.

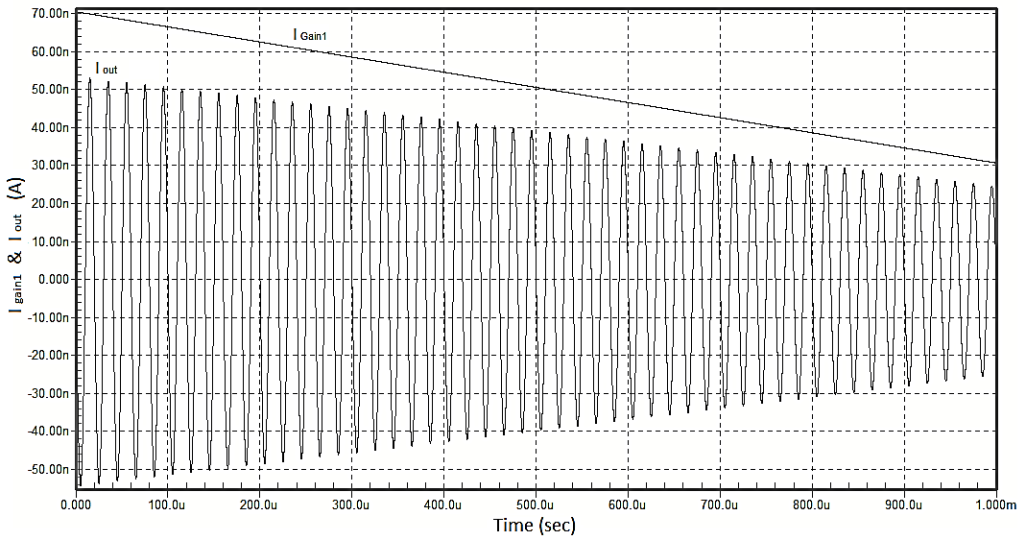


Figure 3.11: The result of changing the gain when using the circuit as a differential-input-single-output current amplifier.

Figure 3.12 shows the simulation result when using the proposed circuit as a controllable gain current amplifier. The input is a sinusoidal signal and the gain is controlled by varying I_{Gain1} from 70nA to 30nA.

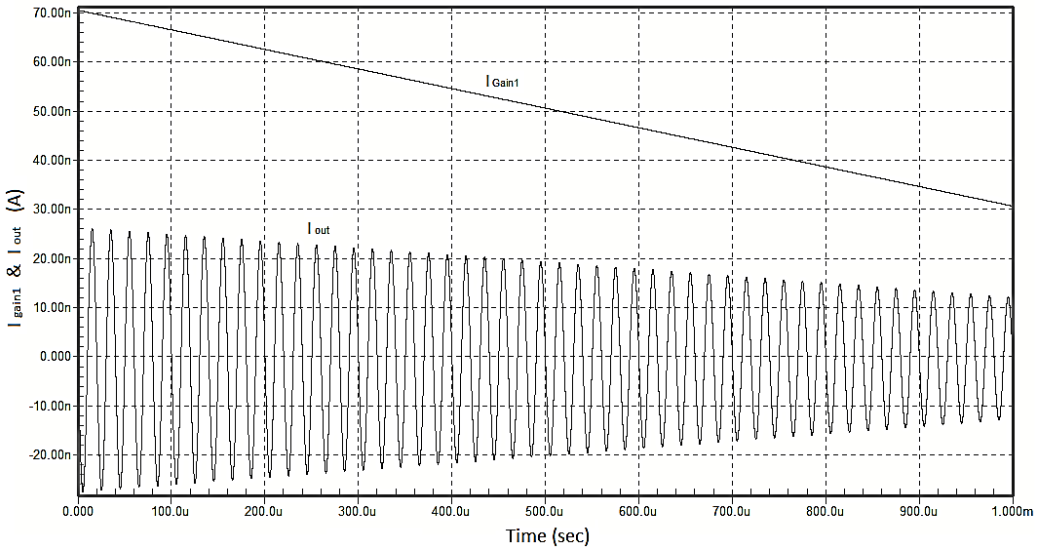


Figure 3.12: The result of changing the gain when using the circuit as a controllable gain current amplifier.

3. 3 Mismatch Analysis

The transistors forming the translinear loop are assumed to be perfectly matched. However, there is nothing perfect in this life and hence, the effects of having mismatch in transistors forming the transliear loop must be studied. Two mismatch cases are discussed below, MOSFETs threshold voltage, and channel length. Referring to equation (3.5), it is a good idea to study the effect of mismatch between M_1 and M_3 and the mismatch between M_2 and M_5.

3.3.1 Threshold voltage mismatch

Referring to equation (1.7), it is clear that the drain current of a MOSFET transistor in subthreshold region is very sensitive to the variation in threshold voltage. Hence, threshold voltage mismatch is discussed below.

(i) Mismatch between M_1, and M_3

Let the threshold voltages for M_1 and M_3 be as given in equations (3.13) and (3.14) respectively.

$$V_{Th1} = V_{Th} + \Delta V_{Th} \tag{3.13}$$

$$V_{Th3} = V_{Th} - \Delta V_{Th} \tag{3.14}$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Then, referring to equation (1.8), equation (3.5) will be as follows:

$$I_{out} = (I_2 - I_5)\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_1 / \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_3\right\}$$

$$I_{out} = (I_2 - I_5)\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG1}-V_{Th}-\Delta V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{SG3}-V_{Th}+\Delta V_{Th}}{nV_T}\right)}\right\}$$

$$I_{out} = (I_2 - I_5)\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG1}-V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{SG3}-V_{Th}}{nV_T}\right)}\right\} e^{\frac{-2\Delta V_{Th}}{nV_T}}$$

$$I_{out} = (I_2 - I_5)\frac{I_1}{I_3}e^{\frac{-2\Delta V_{Th}}{nV_T}} \quad (3.15)$$

It is clear from equation (3.15) that having a mismatch in threshold voltage of M_1 and M_3, the output current will be affected by $e^{\frac{-2\Delta V_{Th}}{nV_T}}$. This error is constant and can be considered as a gain error.

(ii) Mismatch between M_2, and M_5

Let the threshold voltages for M_2 and M_5 be as shown in equations (3.16) and (3.17) respectively.

$$V_{Th2} = V_{Th} + \Delta V_{Th} \quad (3.16)$$

$$V_{Th5} = V_{Th} - \Delta V_{Th} \quad (3.17)$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Then, referring to equation (1.8), equation (3.5) will be as follows:

$$I_{out} = \frac{I_1}{I_3}\left\{\left(\frac{W}{L}I_{D0}e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_2 - \left(\frac{W}{L}I_{D0}e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_5\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{\frac{W}{L}I_{D0}e^{\left(\frac{V_{SG2}-V_{Th}-\Delta V_{Th}}{nV_T}\right)} - \frac{W}{L}I_{D0}e^{\left(\frac{V_{SG5}-V_{Th}+\Delta V_{Th}}{nV_T}\right)}\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{\frac{W}{L}I_{D0}e^{\left(\frac{V_{SG2}-V_{Th}}{nV_T}\right)}e^{\frac{-\Delta V_{Th}}{nV_T}} - \frac{W}{L}I_{D0}e^{\left(\frac{V_{SG5}-V_{Th}}{nV_T}\right)}e^{\frac{\Delta V_{Th}}{nV_T}}\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{I_2e^{\frac{-\Delta V_{Th}}{nV_T}} - I_5e^{\frac{\Delta V_{Th}}{nV_T}}\right\} = \frac{I_1}{I_3}\left\{I_2E - \frac{I_5}{E}\right\} \quad (3.18)$$

Where $E = e^{\frac{-\Delta V_{Th}}{nV_T}}$.

It is clear from equation (3.18) that having a mismatch in threshold voltage between M_2 and M_5 will cause some linearity errors. The first operand (I_2) will be multiplied by a constant

(E) where the other operand (I_5) will be multiplied by the inverse of that constant. The error can only be minimized if the threshold voltage variation is minimized. And since threshold voltage variation is smaller for PMOS transistors than for NMOS transistors [6], it is advisable to design the circuit using PMOS transistors. Hence, the proposed circuit is designed using PMOS transistors.

3.3.2 Channel length mismatch

The fabrication process is not perfect and there must be some mismatch between the transistors dimensions. Hence, channel length mismatch is discussed below.

(i) Mismatch between M_1, and M_3

Let the channel length of M_1 and M_3 be as shown in equations (3.19) and (3.20) respectively.

$$L_1 = L + \Delta L \tag{3.19}$$

$$L_3 = L - \Delta L \tag{3.20}$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Then, referring to equation (1.8), equation (3.5) will be as follows:

$$I_{out} = (I_2 - I_5)\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_1 / \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_3\right\}$$

$$I_{out} = (I_2 - I_5)\left\{\frac{W}{L+\Delta L} I_{D0} e^{\left(\frac{V_{SG1}-V_{Th}}{nV_T}\right)} / \frac{W}{L-\Delta L} I_{D0} e^{\left(\frac{V_{SG3}-V_{Th}}{nV_T}\right)}\right\}$$

$$I_{out} = (I_2 - I_5)\left\{\frac{1-\frac{\Delta L}{L}}{1+\frac{\Delta L}{L}}\left[\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG1}-V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{SG3}-V_{Th}}{nV_T}\right)}\right]\right\}$$

$$I_{out} = \left(\frac{L-\Delta L}{L+\Delta L}\right)(I_2 - I_5)\frac{I_1}{I_3} \tag{3.21}$$

It is clear from equation (3.21) that having a mismatch in channel length between M_1 and M_3, the output will be affected by a factor of $\left(\frac{L-\Delta L}{L+\Delta L}\right)$.This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

(ii) Mismatch between M_2, and M_5

Assuming that there is a mismatch in channel length of M_2 and M_5 such that:

$$L_2 = L + \Delta L \tag{3.22}$$

$$L_5 = L - \Delta L \tag{3.23}$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Then, referring to equation (1.8), equation (3.5) will be written as follows:

$$I_{out} = \frac{I_1}{I_3}\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_2 - \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{SG}-V_{Th}}{nV_T}\right)}\right)_5\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{\frac{W}{L+\Delta L} I_{D0} e^{\left(\frac{V_{SG2}-V_{Th}}{nV_T}\right)} - \frac{W}{L-\Delta L} I_{D0} e^{\left(\frac{V_{SG5}-V_{Th}}{nV_T}\right)}\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{\frac{W}{\left(1+\frac{\Delta L}{L}\right)L} I_{D0} e^{\left(\frac{V_{SG2}-V_{Th}}{nV_T}\right)} - \frac{W}{\left(1-\frac{\Delta L}{L}\right)L} I_{D0} e^{\left(\frac{V_{SG5}-V_{Th}}{nV_T}\right)}\right\}$$

$$I_{out} = \frac{I_1}{I_3}\left\{\left(\frac{1}{1+\frac{\Delta L}{L}}\right) I_2 - \left(\frac{1}{1-\frac{\Delta L}{L}}\right) I_5\right\} \tag{3.24}$$

It is clear from equation (3.24) that having a mismatch in channel length between M_2 and M_5, will cause some linearity errors. This error can be minimized if the circuit is designed using relatively large channel length.

Monte Carlo analysis was carried out to confirm the mismatch analysis. The length of M_1 and M_3 were assumed to have Gaussian distribution with mean of 5μm and standard deviation of

0.02. Running Monte Carlo analysis for 10 iterations yields the DC transfer curves shown in Figure 3.13. Repeating the same steps again but for the lengths of M_2 and M_5, the resulted DC curves are shown in Figure 3.14. From the two figures, it is clear that the error resulted from mismatch between M_2 and M_5 is more severe than the error resulted from the mismatch between M_1 and M_3. That is because the error associated with M_2 and M_5 is linearity error whereas the error associated with M_1 and M_3 is gain error.

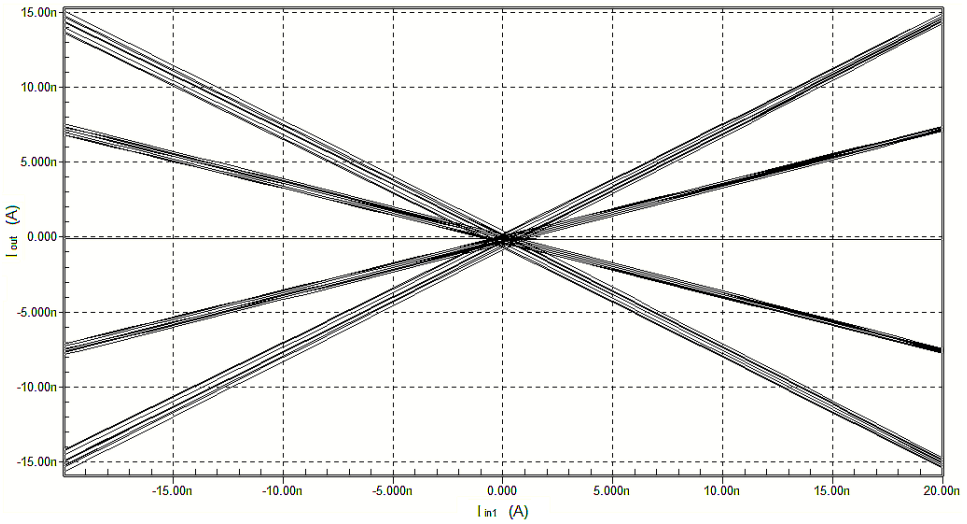


Figure 3.13: Multiplier DC transfer curve when there is a mismatch between the lengths of M_1 and M_3.

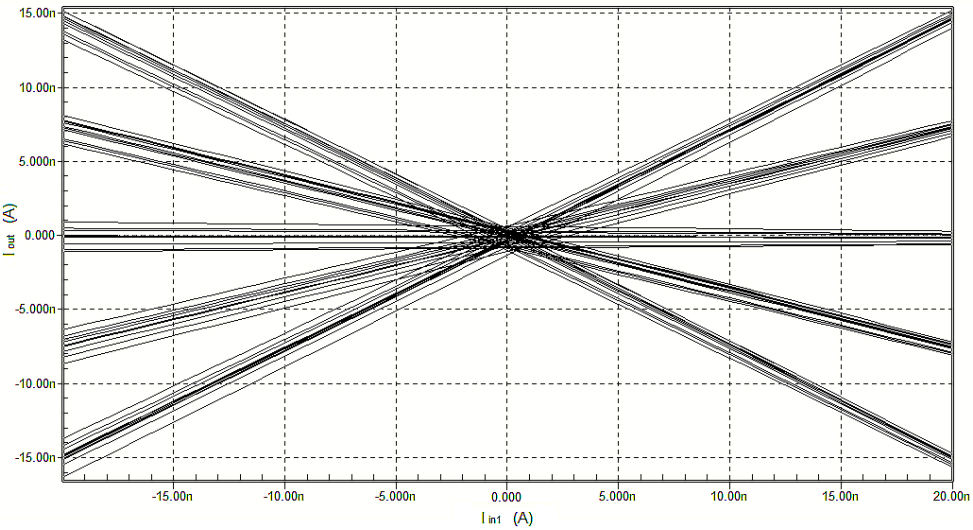


Figure 3.14: Multiplier DC transfer curve when there is a mismatch between the lengths of M_2 and M_5.

The performance of the proposed design was compared with previously published work and is summarized in Table 4. It is clear from the table that the proposed design has a better performance in terms power consumption, linearity error, and THD, and the number of functions it can implement compared to most of the published works. Also, its bandwidth is better than two of the published works. It is worth mentioning that the proposed circuit implements many functions with less number of transistors compared to other designs.

Table 4: Performance comparison.

Reference	**[5] Simulation**	**[21] Experimental**	**[19] Simulation**	**[22] Simulation**	**This work Simulation**
Year	2007	2005	2011	2013	2013
Power Supply	2V	2V	1V	±0.75V	±0.75V
Technology	0.35µm	0.35µm	0.18µm	0.35µm	0.35µm
Bandwidth	<10MHz*	200kHz	768kHz	2.3MHz	1MHz
THD	<1%	0.90%	1.30%	0.7%	0.17%
Linearity error	2.8%	5%	0.88%	0.3%	0.5%
Power Consumption	9µW	5.5µW	1.12µW	2.3µW	1.4µW
Functions	Multiply and divide	Multiply	Multiply	Multiply, divide, squaring, and inverse.	Multiply, divide, and three different types of amplifiers

* See section 2.1.1 and Figure 2.2.

3. 4 Layout and Post Layout Simulation

The circuit layout was designed using Tanner L-Edit tool. The layout is shown in Figure 3.15 below. The layout dimensions are 80.5µm by 48.5µm. The post layout DC transfer curves are shown in Figure 3.16 below.

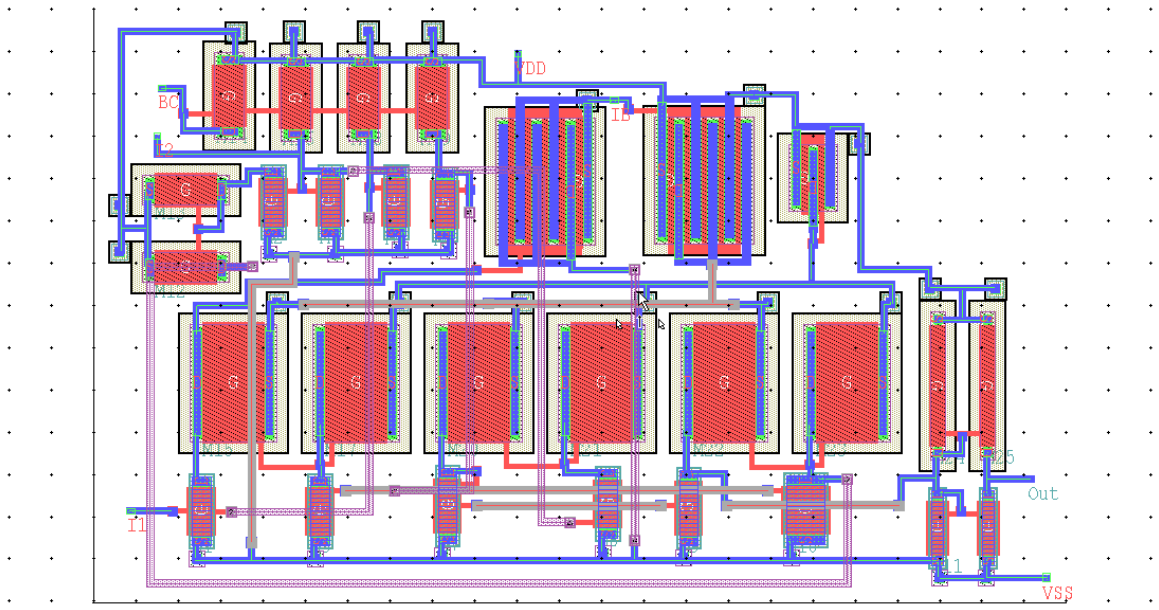


Figure 3.15: Layout design of the proposed multi-functions circuit.

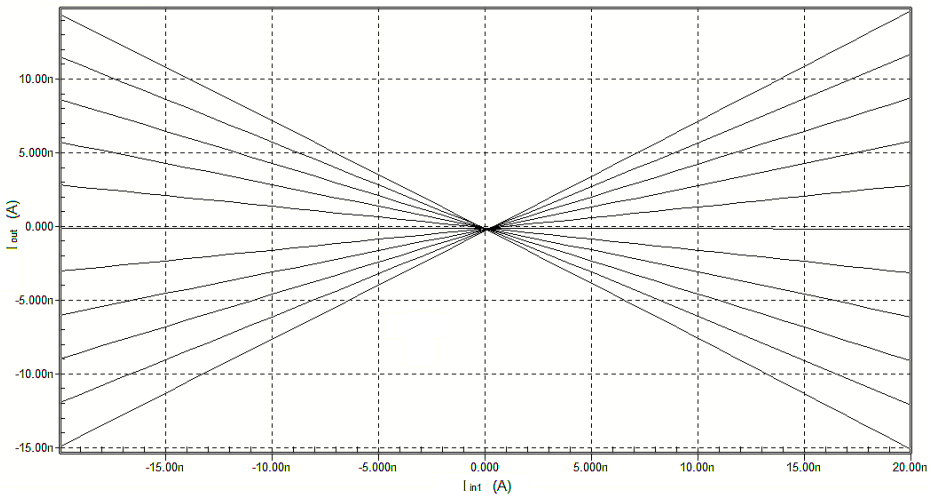


Figure 3.16: Post layout DC transfer curves.

CHAPTER 4

NEW CMOS CURRENT-MODE SQUARE ROOTING CIRCUIT USING MOSFET IN SUBTHRESHOLD

In this chapter, a controllable-gain square rooting circuit based on CMOS transistors operating in subthreshold is proposed. The proposed circuit has the controllable gain advantage over the work in [26] discussed in section 2. 3.

4. 1 Proposed circuit

The proposed circuit shown in Figure 4.1 consists of six transistors M_1 to M_6 forming a translinear loop. All of these transistors are working in subthreshold region. Appling KVL to the translinear loop yields the following:

$$V_{GS1} + V_{GS2} + V_{GS3} = V_{GS4} + V_{GS5} + V_{GS6} \quad (4.1)$$

Assuming all the transistors forming the translinear loops are matched and using equation (1.8), it is easy to show that:

$$I_1 I_2 I_3 = I_4 I_5 I_6 \quad (4.2)$$

Where, I_i is the drain current for the transistor M_i.

With reference to Figure 4.1, it is clear that $I_4 = I_6$. Then, equation (4.2) can be rewritten as:

$$I_4{}^2 = \frac{I_1 I_2 I_3}{I_5} \quad (4.3)$$

Or $$I_4 = \sqrt{\frac{I_1 I_2 I_3}{I_5}} \quad (4.4)$$

The output current is the mirror of I_4 mirrored by M_7, M_a, and M_b. The purpose of current mirror in the output is to provide large output impedance. The output current is given by:

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} = K\sqrt{I_1} \qquad (4.5)$$

Where $K = \sqrt{\frac{I_2 I_3}{I_5}}$

It is clear that equation (4.5) implements the square rooting function and the output current can be controlled by K.

The main advantage of the proposed circuit over most of square rooting circuits reported in the literature is gain controllability. Also, the proposed circuit can be used to compute the geometric mean between two signals (I_1 and I_2) with controllable gain using I_3 and I_5. Moreover, it can compute the square root of the inverse of signal (I_5). Another possible usage of the proposed circuit is a controllable gain amplifier if the input signal is fed to I_1 and I_2 where I_3 and I_5 control the gain.

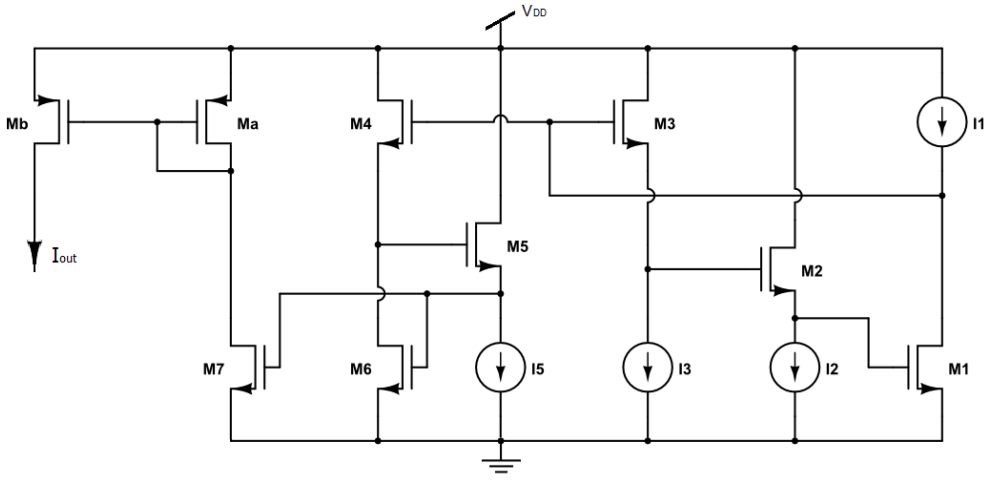


Figure 4.1: Circuit diagram of the proposed square rooting circuit.

4. 2 Simulation Results

The proposed circuit was simulated using Tanner T-Spice with 0.18µm CMOS process technology. The circuit operates from 1V DC supply. The transistors aspect ratios used for simulation are shown in Table 5. The currents I_2, I_3, and I_5 were set to 30nA and the current I_1 was swept from 0 to 500nA. Simulated and calculated results for the DC characteristics of the proposed circuit are shown in Figure 4.2. The maximum relative error was calculated to be about 2%.

Table 5 Transistors aspect ratios of the proposed square rooting circuit.

Transistors	M_a and M_b	$M_1 - M_7$
W/L (µm/µm)	1.2 / 6	7 / 0.5

Simulation of the DC characteristics of the controllable gain square rooting circuit was carried out for different values of I_2 while keeping I_3 and I_5 the same. Simulation results shown in Figure 4.3 confirm the gain controllability of the circuit. The maximum power consumption was calculated to be 0.6µW.

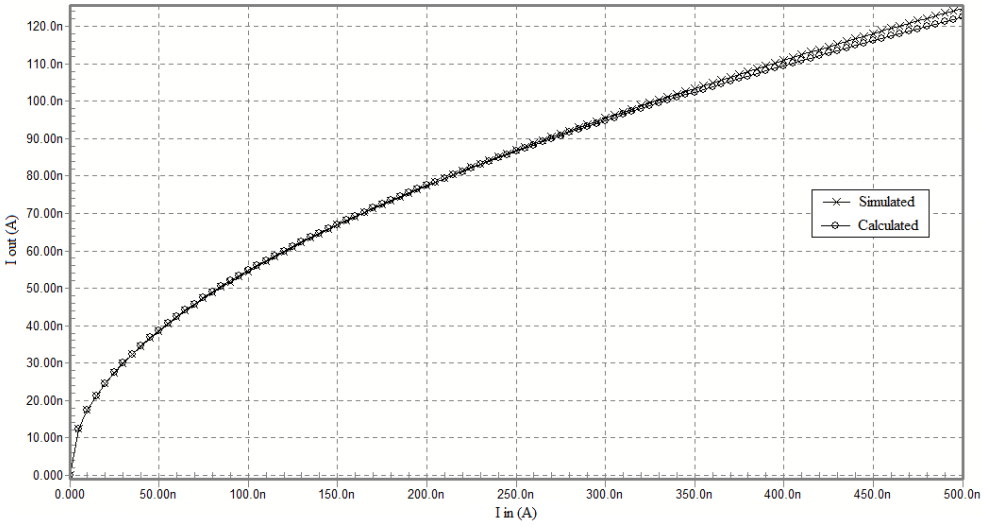


Figure 4.2: DC characteristic for simulated and calculated output current.

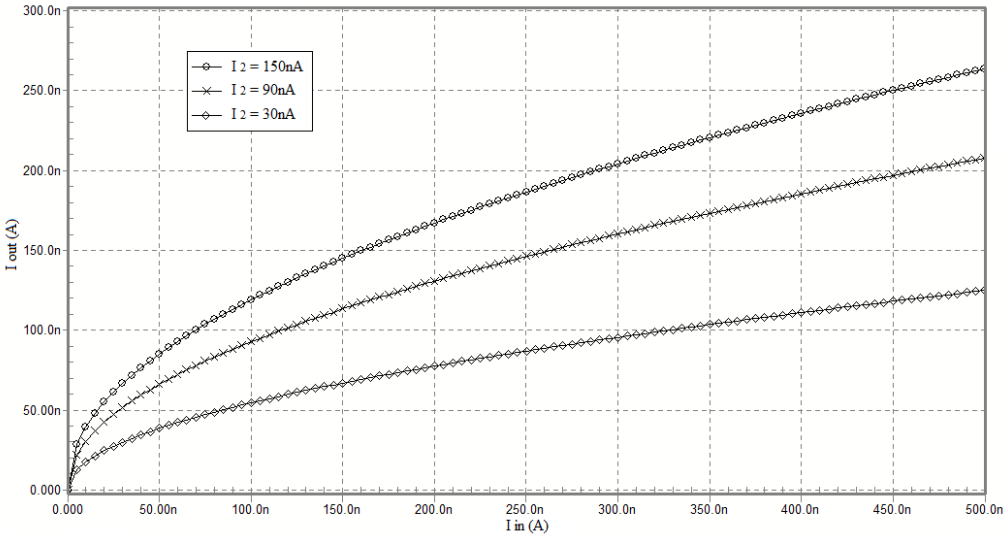


Figure 4.3: DC characteristic for different gains.

Figure 4.4 shows the output current when the input signal is a triangular signal with frequency of 20 kHz. It is clear that the output is proportional to the square root of the input. The proposed circuit has a bandwidth of 1.25 MHz as shown in Figure 4.5.

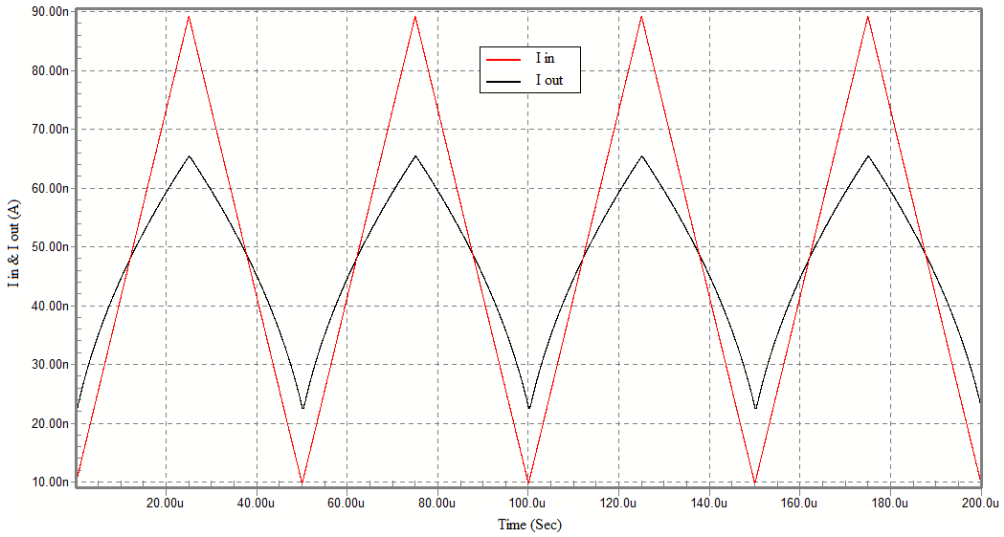


Figure 4.4: Transient response of the proposed square rooting circuit.

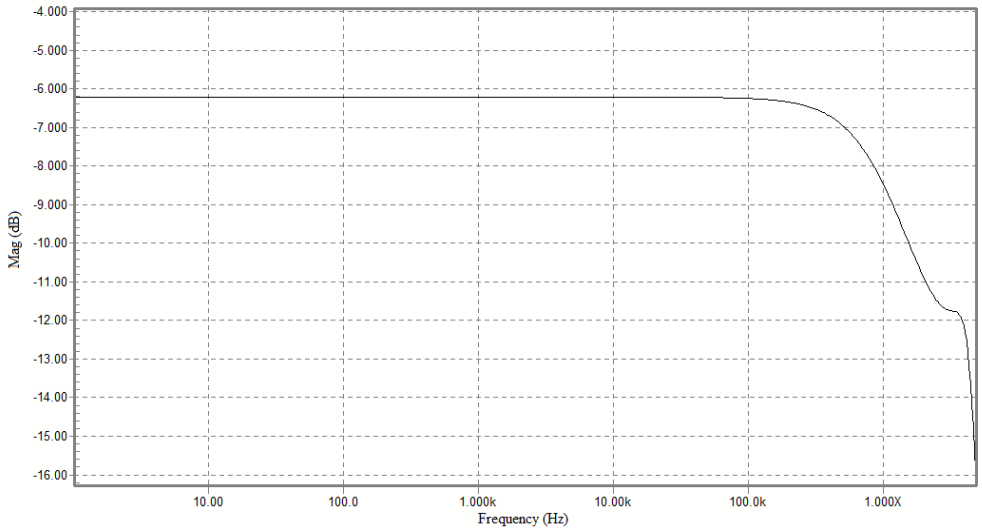


Figure 4.5: Frequency response of the proposed square rooting circuit.

4. 3 Mismatch Analysis

The transistors forming the translinear loop are assumed to be perfectly matched. However, there is nothing perfect in this life and hence, the effects of having mismatch in in the transliear loop must be studied. Two mismatch cases are discussed below, MOSFETs threshold voltage, and channel length. Referring to equation (4.5), it is a good idea to study the effect of mismatch between M_1 and M_2 and the mismatch between M_3 and M_5.

4.3.1 Threshold voltage mismatch

Referring to equation (1.7), it is clear that the drain current of a MOSFET transistor in subthreshold region is very sensitive to variation in the threshold voltage. Hence, threshold voltage mismatch is discussed below.

(i) Mismatch between M_1, and M_2

Let the threshold voltages for M_1 and M_2 be as shown in equations (4.6) and (4.7) respectively.

$$V_{Th1} = V_{Th} + \Delta V_{Th} \tag{4.6}$$

$$V_{Th2} = V_{Th} - \Delta V_{Th} \tag{4.7}$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Referring to equation (1.8), equation (4.5) will be as follows:

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_1 \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_2\right\}}$$

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS1}-V_{Th}-\Delta V_{Th}}{nV_T}\right)} \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS2}-V_{Th}+\Delta V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS1}-V_{Th}}{nV_T}\right)} \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS2}-V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} \tag{4.8}$$

It is clear from equation (4.8) that the circuit is insensitive to threshold voltage mismatch of M_1 and M_2. However, if the mismatch between threshold voltages for M_1 and M_2 were as follows:

$$V_{Th1} = V_{Th} + \Delta V_{Th} \tag{4.9}$$

$$V_{Th2} = V_{Th} + \Delta V_{Th} \tag{4.10}$$

The output current will be:

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} e^{\frac{-\Delta V_{Th}}{nV_T}} \tag{4.11}$$

Thus, if the threshold voltage of M_1 and M_2 are different than the other transistors, this will cause a gain error of $e^{\frac{-\Delta V_{Th}}{nV_T}}$.

(ii) Mismatch between M_3, and M_5

Let the threshold voltages for M_3 and M_5 be as shown in equations (4.12) and (4.13) respectively.

$$V_{Th3} = V_{Th} + \Delta V_{Th} \tag{4.12}$$

$$V_{Th5} = V_{Th} - \Delta V_{Th} \tag{4.13}$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Then, referring to equation (1.8), equation (4.5) will be written as:

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_3 / \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_5\right\}}$$

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS3}-V_{Th}-\Delta V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS5}-V_{Th}+\Delta V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS3}-V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS5}-V_{Th}}{nV_T}\right)}\right\} e^{\frac{-2\Delta V_{Th}}{nV_T}}}$$

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} e^{\frac{-\Delta V_{Th}}{nV_T}} \tag{4.14}$$

It is clear from equation (4.14) that having a mismatch in threshold voltage of M_3 and M_5, the output will be scaled by $e^{\frac{-\Delta V_{Th}}{nV_T}}$ .This error is constant and can be considered as a gain error.

4.3.2 Channel length mismatch

The fabrication process is not perfect and there must be some mismatch between the transistors dimensions. Hence, channel length mismatch is discussed below.

(i) Mismatch between M_1, and M_2

Let the channel length of M_1 and M_2 be as shown in equations (4.15) and (4.16)

respectively.

$$L_1 = L + \Delta L \tag{4.15}$$

$$L_2 = L - \Delta L \tag{4.16}$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Referring to equation (1.8), equation (4.5) will be as follows:

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_1 \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_2\right\}}$$

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\frac{W}{L+\Delta L} I_{D0} e^{\left(\frac{V_{GS1}-V_{Th}}{nV_T}\right)} \frac{W}{L-\Delta L} I_{D0} e^{\left(\frac{V_{GS2}-V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\frac{W}{L(1+\frac{\Delta L}{L})} I_{D0} e^{\left(\frac{V_{GS1}-V_{Th}}{nV_T}\right)} \frac{W}{L(1-\frac{\Delta L}{L})} I_{D0} e^{\left(\frac{V_{GS2}-V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{\frac{I_3}{I_5}} \sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS1}-V_{Th}}{nV_T}\right)} \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS2}-V_{Th}}{nV_T}\right)}\right\} \frac{L^2}{(L^2-\Delta L^2)}}$$

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}} \sqrt{\frac{L^2}{(L^2-\Delta L^2)}} \tag{4.17}$$

It is clear from equation (4.17) that having a mismatch in channel length between M_1 and M_2, the output will be scaled by $\sqrt{\frac{L^2}{(L^2-\Delta L^2)}}$. This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

(ii) Mismatch between M_3, and M_5

Assuming that there is a mismatch in channel length of M_3 and M_5 such that:

$$L_3 = L + \Delta L \tag{4.18}$$

$$L_5 = L - \Delta L \tag{4.19}$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Referring to equation (1.8), equation (4.5) will be written as follows:

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_3 / \left(\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)}\right)_5\right\}}$$

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\frac{W}{L+\Delta L} I_{D0} e^{\left(\frac{V_{GS3}-V_{Th}}{nV_T}\right)} / \frac{W}{L-\Delta L} I_{D0} e^{\left(\frac{V_{GS5}-V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\frac{W}{L(1+\frac{\Delta L}{L})} I_{D0} e^{\left(\frac{V_{GS3}-V_{Th}}{nV_T}\right)} / \frac{W}{L(1-\frac{\Delta L}{L})} I_{D0} e^{\left(\frac{V_{GS5}-V_{Th}}{nV_T}\right)}\right\}}$$

$$I_{out} = \sqrt{I_1 I_2}\sqrt{\left\{\frac{W}{L} I_{D0} e^{\left(\frac{V_{GS3}-V_{Th}}{nV_T}\right)} / \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS5}-V_{Th}}{nV_T}\right)}\right\}\frac{(L-\Delta L)}{(L+\Delta L)}}$$

$$I_{out} = \sqrt{\frac{I_1 I_2 I_3}{I_5}}\sqrt{\frac{(L-\Delta L)}{(L+\Delta L)}} \tag{4.20}$$

It is clear from equation (4.20) that having a mismatch in channel length between M_3 and M_5, the output will be scaled by $\sqrt{\frac{(L-\Delta L)}{(L+\Delta L)}}$ .This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

Monte Carlo analysis was carried out to confirm the mismatch analysis. Running Monte Carlo analysis for 100 iterations using the statistical model of 0.18µm CMOS technology yields the the DC transfer curves shown in Figure 4.6 below. From the figure, the maximum error was

calculated and it is equal to 3.1%.

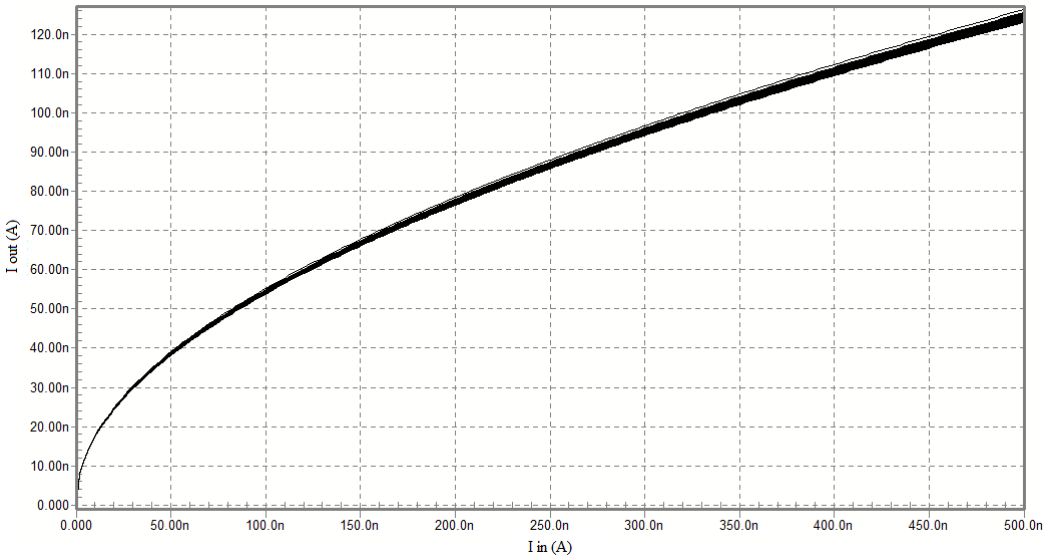


Figure 4.6: DC transfer curves resulted from running Monte Carlo analysis for 100 iterations.

Table 6 below compares the performance of the proposed circuit to the work reported in [26]. It is clear from the table that the proposed circuit has better performance in terms of bandwidth and power consumption. It is important to note that the work in [26] utilized a very large resistor to increase the dynamic range and decrease the error. Otherwise, the dynamic range would be limited to 250nA and the error would increase. Also, the gain controllability of the circuit in [26] is very limited.

Table 6: Comparison between the proposed controllable gain square rooting circuit and the circuit in [26].

Reference	**[26]**	**This work**
Year	2009	2014
Power Supply	0.6V	1V
Technology	0.18µm	0.18µm
Bandwidth	1MHz	1.25MHz
Dynamic Range	250nA to 1µA*	500nA
error	-	2%
Power Consumption	<1µW	0.6µW

* 250nA dynamic range when the circuit operates as in Figure 2.5 and 1µA when a large resistor is used [26].

CHAPTER 5

A NEW MULTI-INPUT ANALOG MULTIPLIER

Many of the multipliers and dividers reported in the literature are of two inputs only. However, sometimes it is necessary to have a multi input multiplier especially in analog signal processing [28]. A trivial way of having such a circuit is to use several two-input multiplier in series as shown in Figure 5.1 below [28]. However, this method is not preferable since the error produced by the first multiplier is propagating throughout the series and hence, degrading the accuracy of the circuit. In [28] the proposed multi-input multiplier uses log-antilog approach. Another approach is the use of the transliear principle. If six MOSFETs or more operating in subthreshold form a translinear loop, then a multi-input multiplier can be achieved. In this chapter, a new multi-input multiplier using MOS transistors operating in subthreshold is presented and discussed.

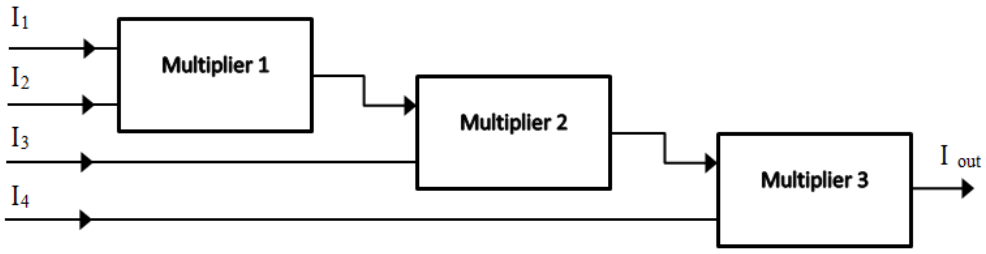


Figure 5.1: Trivial way of implementing multi-input multiplier [28].

5.1 Proposed circuit

The proposed circuit is shown in Figure 5.2. It consists of eight transistors that form one translinear loop. It is very clear from the figure that the translinear loop is formed by the transistors M_1- M_8. Also, it is clear that the transistors M_4, and M_6 have the same drain current.

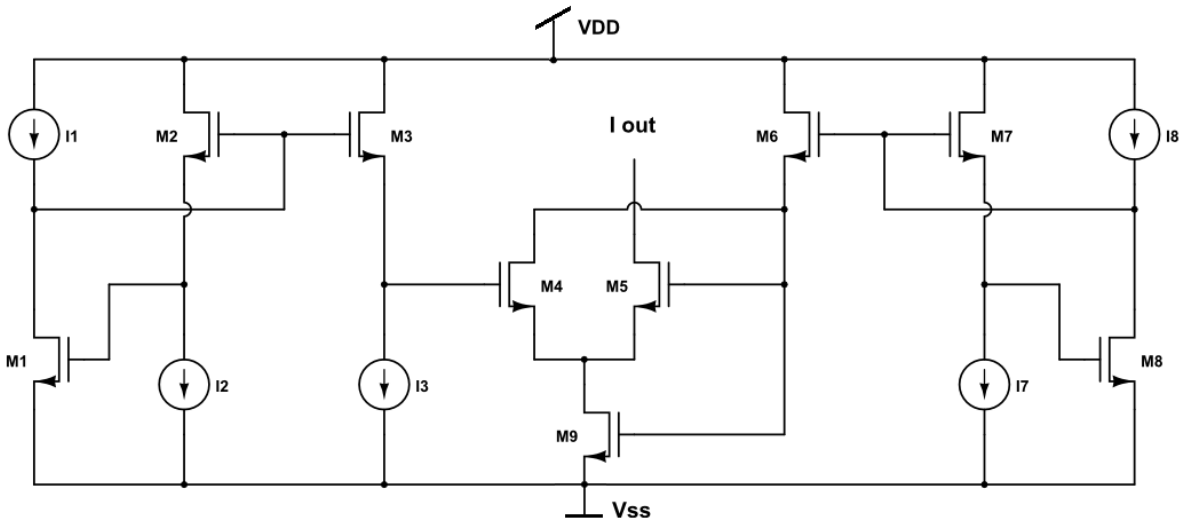


Figure 5.2: Proposed multi-input analog multiplier.

Appling KVL to the translinear loop yields the following equation:

$$V_{GS1} + V_{GS2} + V_{GS5} + V_{GS6} = V_{GS3} + V_{GS4} + V_{GS7} + V_{GS8} \quad (5.1)$$

Since all the transistors forming the translinear loops are matched and working in subthreshold region. Then, substituting equation (1.8) back into equation (5.1), yields:

$$I_1 I_2 I_5 I_6 = I_3 I_4 I_7 I_8 \quad (5.2)$$

Where, I_i is the drain current for the transistor M_i.

Since $I_4 = I_6$, equation (5.2) becomes:

$$I_1 I_2 I_5 = I_3 I_7 I_8 \quad (5.3)$$

Let I_5 be the output current of the circuit. Then equation (5.3) can be written as:

$$I_{out} = I_5 = \frac{I_3 I_7 I_8}{I_1 I_2} \quad (5.4)$$

It is clear from equation (5.4) that the circuit can be used as multi-input multiplier. It also can be used to divide a signal by the product of two signals. Moreover, it can be used to divide the product of two signals by the product of another two signals. Also, it can be used to compute the cubic of a signal by applying the same input to I_3, I_7 and I_8 while I_1 and I_2 control the gain.

5.2 Simulation Results

Tanner T-spice with 0.18µm CMOS technology is used to confirm the functionality of the circuit shown in Figure 5.2. Table 7 shows the aspect ratios for all transistors used in the simulation. The circuit operates from ±0.75V DC supply. The three input currents (I_3, I_7 and I_8) were swept from 20nA to 80nA. Simulation result shown in Figure 5.3 confirms the functionality of the multi-input multiplier. In Figure 5.3, the current I_3 is the x-axis, the current I_7 has three values (20nA, 50nA, and 80nA), and the current I_8 has only two values (20nA, and 80nA). The percentage of relative error is shown in Figure 5.4. it is clear from the figure that the error increases with the increase in the input currents. Although the maximum error looks relatively large, it is expected to be lower than the error if the trivial approach was used. The maximum power consumption of the proposed circuit is around 1µW.

Table 7: Transistors aspect ratio of the proposed multi-input multiplier.

Transistor	$M_1 - M_8$	M_9
W(µm)/L(µm)	14/1	10/2

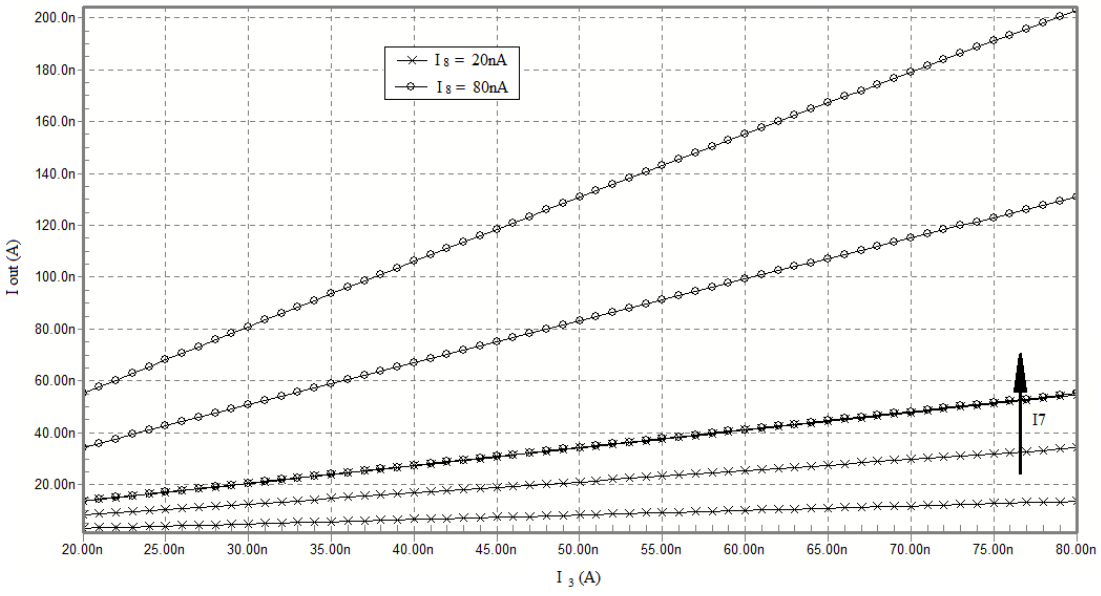


Figure 5.3: Multi-input multiplier DC transfer curves.

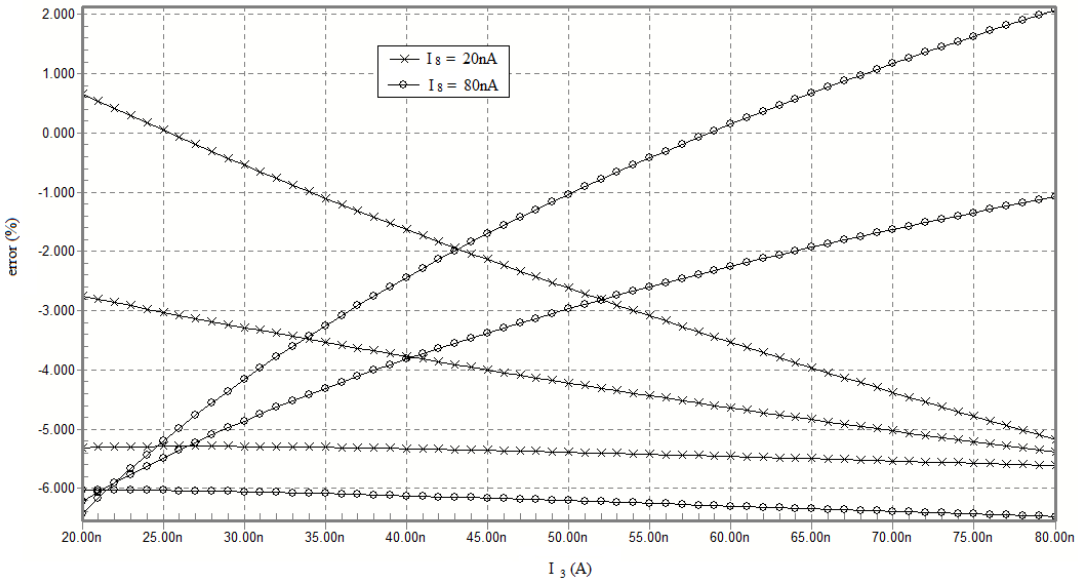
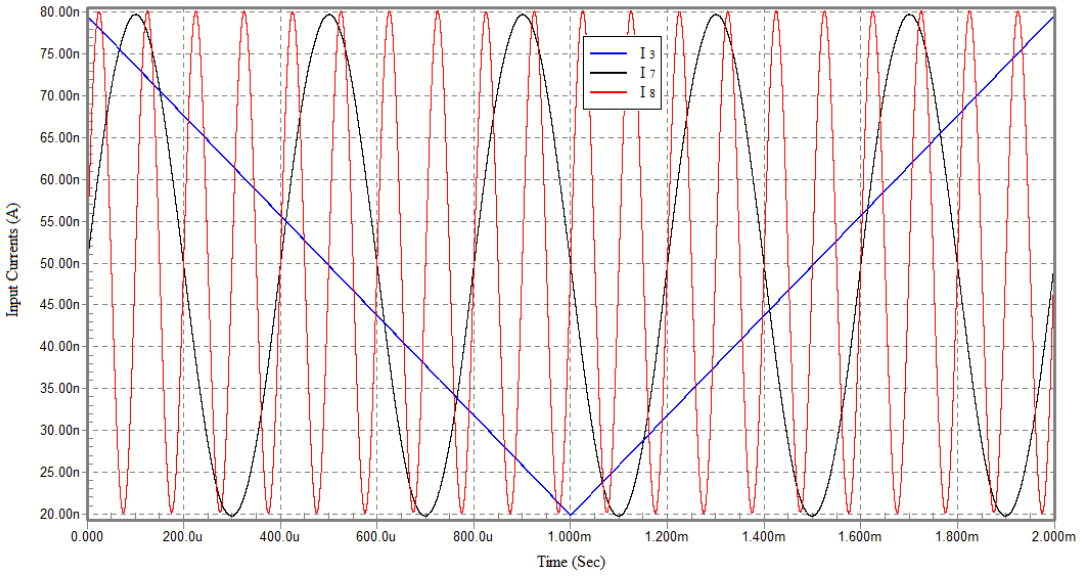
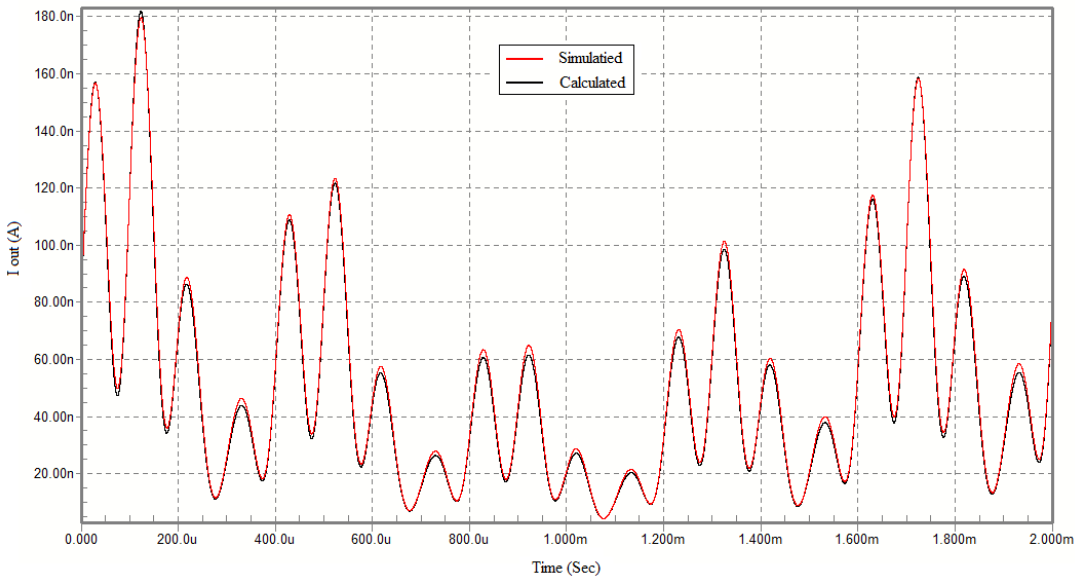


Figure 5.4: Multi-input multiplier error.

Figure 5.5 (b) shows the simulation result of multiplying three current signals that are shown in Figure 5.5 (a).



(a)



(b)

Figure 5.5: Transient response for the multi-input multiplier. (a) input currents. (b) output current.

Simulation for frequency response was carried out and the result is shown in Figure 5.6. It is clear from the plot that that the -3dB frequency is around 520 kHz. The circuit has relatively small bandwidth compared to other proposed multiplier. This means that it is suitable for low frequency applications such as biomedical applications. That is because most of the signals measured from the human body are of low frequencies.

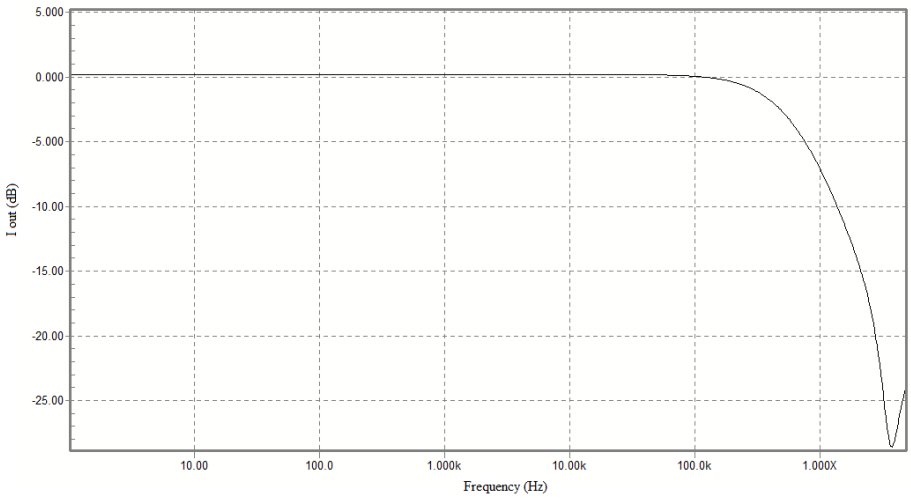


Figure 5.6: Frequency response for the multi-input multiplier.

5.3 Mismatch Analysis

The transistors forming the translinear loop are assumed to be perfectly matched. However, there is nothing perfect in this life and hence, the effects of having mismatch in in the transliear loop must be studied. Two mismatch cases are discussed below, MOSFETs threshold voltage, and channel length. Referring to equation (5.4), it is a good idea to study the effect of mismatch between M_3 and M_1, the mismatch between M_7 and M_8 and the mismatch between M_1 and M_2.

5.3.1 Threshold voltage mismatch

Referring to equation (1.7), it is clear that the drain current of a MOSFET transistor in subthreshold region is very sensitive to variation the in threshold voltage. Hence, threshold voltage mismatch is discussed below.

(i) Mismatch between M_3, and M_1

Let the threshold voltages for M_3 and M_1 be as shown in equations (5.5) and (5.6) respectively.

$$V_{Th3} = V_{Th} + \Delta V_{Th} \tag{5.5}$$

$$V_{Th1} = V_{Th} - \Delta V_{Th} \tag{5.6}$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Then, following the same procedure done in the previous two chapters, it can be shown that the output current will be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} e^{\frac{-2\Delta V_{Th}}{nV_T}} \tag{5.7}$$

Thus, having a mismatch in the threshold voltage of M_1 and M_3 will scale the output

current by a factor of $e^{\frac{-2\Delta V_{Th}}{nV_T}}$. This error is constant and can be considered as a gain error.

(ii) Mismatch between M_7, and M_8

Let the threshold voltages for M_7 and M_8 be as shown in equations (5.8) and (5.9) respectively.

$$V_{Th7} = V_{Th} + \Delta V_{Th} \quad (5.8)$$

$$V_{Th8} = V_{Th} - \Delta V_{Th} \quad (5.9)$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Then, following the same procedure, it can be shown that the circuit is insensitive to threshold voltage mismatch of M_7 and M_8. However, if the mismatch between threshold voltages for M_7 and M_8 were as follows:

$$V_{Th7} = V_{Th} + \Delta V_{Th} \quad (5.10)$$

$$V_{Th8} = V_{Th} + \Delta V_{Th} \quad (5.11)$$

Then, the output current will be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} e^{\frac{-2\Delta V_{Th}}{nV_T}} \quad (5.12)$$

Thus, if the threshold voltages of M_7 and M_8 are different than the other transistors, this will cause gain error of $e^{\frac{-2\Delta V_{Th}}{nV_T}}$.

(iii) Mismatch between M_1, and M_2

Let the threshold voltages for M_1 and M_2 be as shown in equations (5.13) and (5.14) respectively.

$$V_{Th1} = V_{Th} + \Delta V_{Th} \quad (5.13)$$

$$V_{Th2} = V_{Th} - \Delta V_{Th} \quad (5.14)$$

Where V_{Th} is the threshold voltage for the rest of transistors forming the translinear loops. Again, following the same procedure, it can be shown that the circuit is insensitive to threshold voltage mismatch of M_1 and M_2. However, if the mismatch between threshold voltages for M_1 and M_2 were as follows:

$$V_{Th1} = V_{Th} + \Delta V_{Th} \quad (5.15)$$

$$V_{Th2} = V_{Th} + \Delta V_{Th} \quad (5.16)$$

Then, the output current will be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} e^{\frac{2\Delta V_{Th}}{nV_T}} \quad (5.17)$$

It is clear from equation (5.17) that if the threshold voltage of M_1 and M_2 is different from the other transistors, this will cause some gain error of $e^{\frac{2\Delta V_{Th}}{nV_T}}$.

5.3.2 Channel length mismatch

The fabrication process is not perfect and there must be some mismatch between the transistors dimensions. Hence, channel length mismatch is discussed below.

(i) Mismatch between M_3, and M_1

Assuming that there is a mismatch in channel length of M_3 and M_1 such that:

$$L_3 = L + \Delta L \quad (5.18)$$

$$L_1 = L - \Delta L \quad (5.19)$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Then, repeating the same procedure done before, the output current can be found to be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} \frac{(L-\Delta L)}{(L+\Delta L)} \quad (5.20)$$

It is clear from equation (5.20) that having a mismatch in channel length between M_3 and M_1, the output will be affected by $\frac{(L-\Delta L)}{(L+\Delta L)}$ .This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

(ii) Mismatch between M_7, and M_8

Let the channel length of M_7 and M_8 be as shown in equations (5.21) and (5.22) respectively.

$$L_7 = L + \Delta L \quad (5.21)$$

$$L_8 = L - \Delta L \quad (5.22)$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Then, following the same procedure done previously, it can be shown that the output current will be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} \frac{L^2}{(L^2-\Delta L^2)} \quad (5.23)$$

It is clear from equation (5.23) that having a mismatch in channel length between M_7 and M_8, the output will be affected by $\frac{L^2}{(L^2-\Delta L^2)}$ .This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

(iii) Mismatch between M_1, and M_2

Let the channel length of M_1 and M_2 be as shown in equations (5.24) and (5.25) respectively.

$$L_1 = L + \Delta L \quad (5.24)$$

$$L_2 = L - \Delta L \quad (5.25)$$

Where L is the channel length for the rest of the transistors forming the translinear loops. Again, following the procedure done before, the output current can be found to be as:

$$I_{out} = \frac{I_3 I_7 I_8}{I_1 I_2} \frac{L^2 - \Delta L^2}{L^2} \quad (5.26)$$

It is clear from equation (5.26) that having a mismatch in channel length between M_1 and M_2, the output will be affected by $\frac{L^2 - \Delta L^2}{L^2}$ .This error is constant and can be considered as a gain error. This error can be minimized if the circuit is designed using relatively large channel length.

Monte Carlo analysis was carried out to confirm the mismatch analysis. Running Monte Carlo analysis for 100 iterations using the statistical model of 0.18µm CMOS technology yields the the DC transfer curves shown in figure below. From the figure, the maximum error was calculated and it is equal to 10% when all the input currents are equal to 80nA.

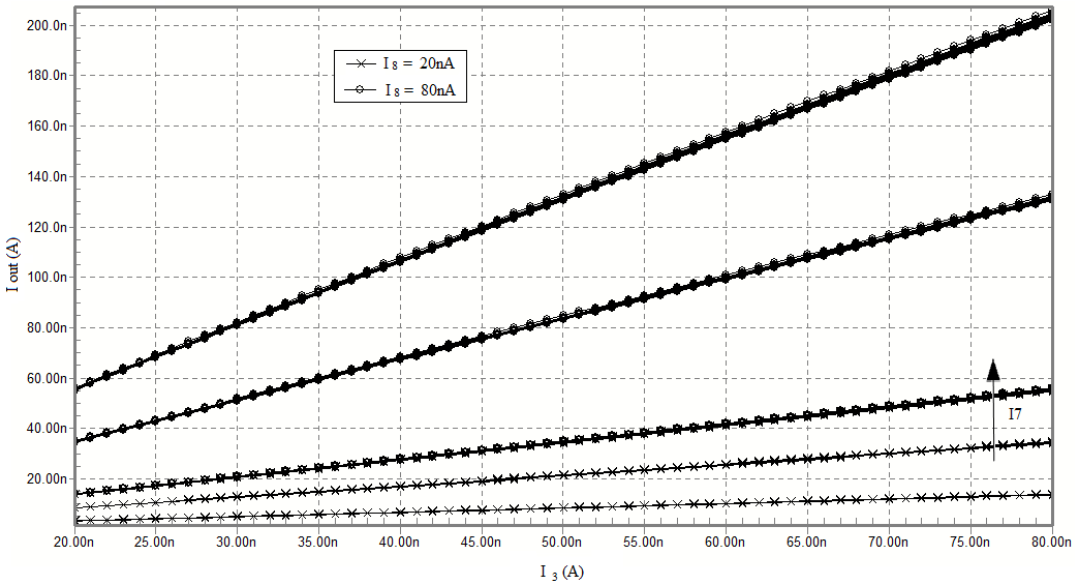


Figure 5.7: Multi-input multiplier DC transfer curves resulted from running Monte Carlo analysis for 100 iterations.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this thesis, three new different circuits were designed. Namely, analog multi-function circuit, controllable gain square rooting circuit, and multi-input multiplier. Tanner tool was used to confirm the functionality of the proposed circuits. Mismatch analysis was carried out for these circuits. Compared to previously published works, the analog multi-function circuit shows better performance in terms of power consumption, linearity error, and THD over most of the published works. The controllable gain square rooting circuit shows better performance in terms of bandwidth and power consumption.

6.2 Future Work

There is nothing perfect. There is always a room for improvement. Thus, the following points can be considered as an extension to this work:

- Fabricating the designed circuits and testing them to prove the simulation results and to compare the experimental results with other published works.
- Researching for techniques to integrate more analog functions in a single circuit.
- Developing technique to increase the dynamic range of the CMOS circuits working in subthreshold region.

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