International Journal of Engineering & Technology
CENTRE OF PROFESSIONAL RESEARCH PUBLICATIONS
ISSN 2049-3444

International Journal of Engineering and Technology Volume 2 No. 8, August, 2012

Design of Analog VLSI Architecture for DCT

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ABSTRACT

When implementing real-time DSP algorithms on digital circuits, the system is always constrained by limited speed, accuracy and round off noise. These limitations must be taken into account for the design and implementation stages. Doubling the dynamic rate of the analog DCT is expensive, whereas in digital DCT an addition of 1 bit in data path is adequate. This paper proposes a novel approach of analog CMOS implementation technique for Digital Signal Processing (DSP) algorithms to reduce the area and power requirement in the existing Digital CMOS implementations. Discrete Cosine Transform (DCT) with signed coefficients have been designed and implemented in this paper. The problems of digital DCTs viz., quantization error, round-off noise, high power consumption and large area are overcome by the proposed implementation. It can be used to develop the architecture design of DFT, DST and DHT.

Keywords: *Sample and Hold, Discrete Cosine Transform, Discrete Fourier Transform, Discrete Sine Transform, Discrete Hartley Transform*

1. INTRODUCTION

Signal Processing is an area that deals with analysis and operation of signals. It can be broadly classified as Analog and Digital Signal processing. For digital signal processing, the real time analog signals are converted to digital, processed and converted back to analog before given to real world. One of the important tools of digital signal processing algorithms is DCT.This transform is very useful in signal processing on image, speech, video, communication, biomedical signals etc. Power consumption is proportional to signal frequency. In digital architecture, power consumption is more.Rond-off noise occurs when converting a signal from analog to digital.

In the proposed method, the A to D conversion is replaced by opamp SAH circuit. The sample is multiplied with DCT coefficient in opamp amplifier and added using opamp adder. Since analog to digital conversion is absent, Round-off noise is also eliminated.

2. THEORY

DCT is a frequency transform used in still and moving video compression due to its decorrelation property. For the data sequence x(n),n=0,1,…N,DCT is given by X(K),K=0,1,….N-1. DCT can be expressed as:

$$X(K) = e(k)\sum_{n=0}^{N-1} x(n)\cos\left[\frac{(2n+1)\pi k}{2N}\right] \quad K=0,1,\ldots N-1. \qquad (1)$$

$$e(k) = \begin{cases} 1/\sqrt{2}, & \text{if } k=0 \\ 1, & \text{otherwise} \end{cases} \qquad (2)$$

DCT is an orthogonal transform. It is effective due to its symmetry and simplicity. First coefficient is the average of all and it is called the DC coefficient. The remaining coefficients are called the AC coefficients. The basic block of DCT is (Multiply and Accumulate) MAC.

The digital DCT will work on only digital signals. It needs ADC and DAC to convert analog signal for its processing. The modules of digital DCT are Multiplier and Adder.

The matrix form of DCT can be given by

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} c4 & c4 & c4 & c4 & c4 & c4 & c4 & c4 \\ c1 & c3 & c5 & c7 & c9 & c11 & c13 & c15 \\ c2 & c6 & c10 & c14 & c18 & c22 & c26 & c30 \\ c3 & c9 & c15 & c21 & c27 & c1 & c7 & c13 \\ c4 & c12 & c20 & c28 & c4 & c12 & c20 & c28 \\ c5 & c15 & c25 & c3 & c13 & c23 & c1 & c11 \\ c6 & c18 & c30 & c10 & c22 & c2 & c14 & c26 \\ c7 & c21 & c3 & c17 & c31 & c13 & c27 & c9 \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(5) \\ x(6) \\ x(7) \\ x(8) \end{bmatrix}$$

Where $c_i=\cos(i\pi/16)$. (3)

Using trigonometric properties, DCT architecture is modified in a systematic way that is simpler to implement.

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} c4 & c4 & c4 & c4 & c4 & c4 & c4 & c4 \\ c1 & c3 & c5 & c7 & -c7 & -c5 & -c3 & -c1 \\ c2 & c6 & -c6 & -c2 & -c2 & -c6 & c6 & c2 \\ c3 & -c7 & -c1 & -c5 & c5 & c1 & c7 & -c3 \\ c4 & -c4 & -c4 & c4 & c4 & -c4 & -c4 & c4 \\ c5 & -c1 & c7 & c3 & -c3 & -c7 & c1 & -c5 \\ c6 & -c2 & c2 & -c6 & -c6 & c2 & -c2 & c6 \\ c7 & -c5 & c3 & -c1 & c1 & -c3 & c5 & -c7 \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(4) \\ x(5) \\ x(6) \\ x(7) \end{bmatrix}$$

The digital multipliers and adders are used to do the multiplication and summation of all. The partial products are generated by logic AND gate and added by digital adders to produce the final product. The DCT output is obtained by matrix multiplication of its co-efficient matrix and input array. So the product of multiplication is accumulated to produce the DCT output.

The Schematic of digital multiplier is shown with AND, adder blocks.

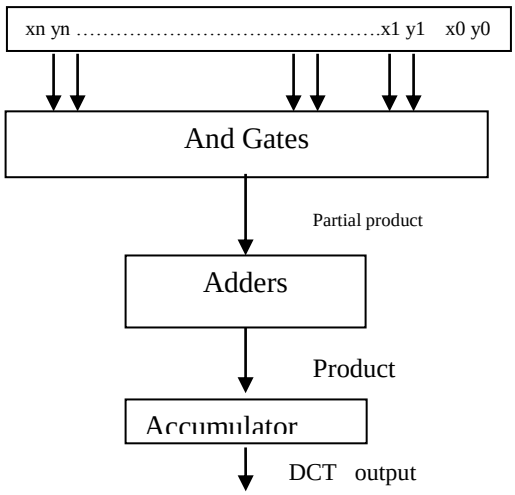


Fig.1.Schematic of Digital Multiplier circuit

The CMOS Circuit of two input AND is used to generate the partial product of digital multiplier.

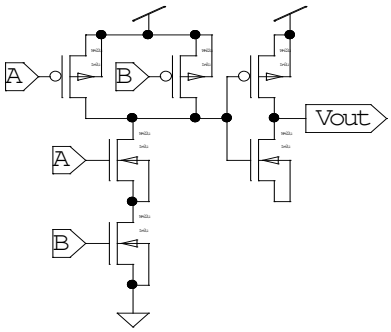


Fig.2.CMOS Switch-Level circuit of AND Gate

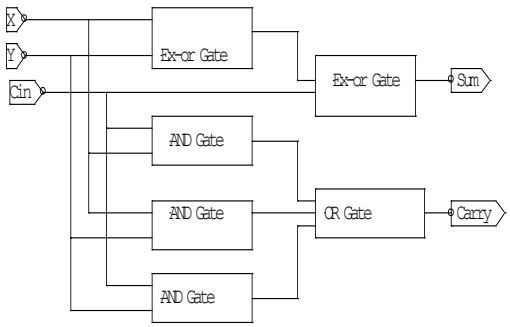


Fig.3.Schematic Diagram of Digital Adder

The EXOR gate and AND gate is used to form the digital adder circuit.

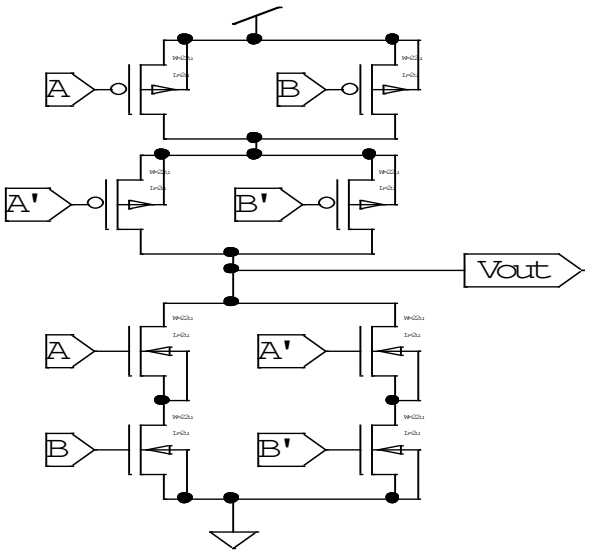


Fig.4.CMOS Switch-Level circuit of EXOR Gate

The D-latch is used to buffer the input and fed to the MAC unit after each clock. The schematic block diagram of D-latch consists of inverter, AND blocks.

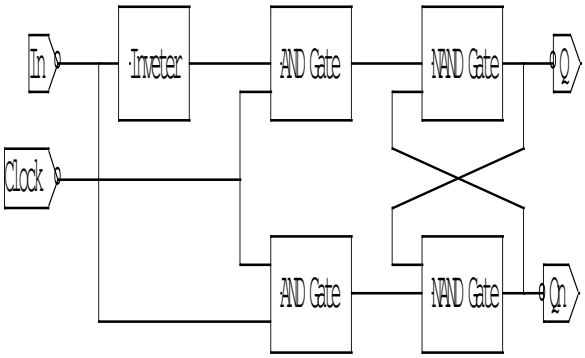


Fig.5.Schematic block diagram of D-latch

The CMOS switch level circuit for inverter is used to negate the input. The Digital DCT architecture is obtained by cascading the MAC units. The analog DCT architecture of using switched capacitors also operates on general DCT expression where input samples are multiplied by all the DCT coefficients simultaneously using capacitor array. The multiplied values are then switched parallel with the help of a cross-point switch, to different integrators to perform multiplication and accumulation.

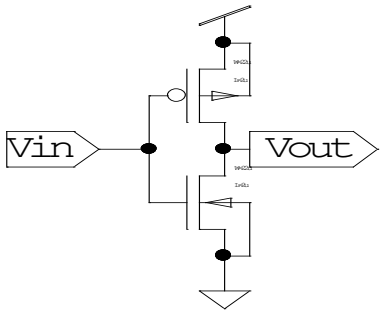
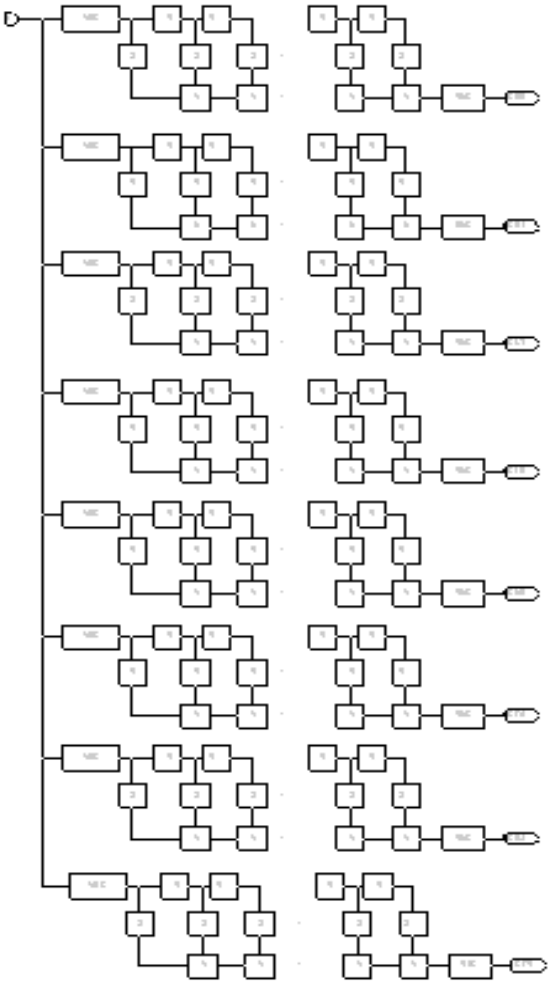


Fig.6. CMOS Switch-Level circuit of Inverter



Block Diagram of Digital DCT

3. THE PROPOSED ARCHITECTURE

The proposed Analog DCT consists of three major blocks

- Multiplier cell
- Adder cell
- Sample and Hold

The proposed design will reduce size, power consumption and increases processing speed. The round-off noise effect is eliminated.

The DCT architecture has high speed sampling unit, multiplier for multiplying the weights with the input signal and a summing unit to sum all the values. It uses OPAMP in the design of multiplier, adder and Sample and Hold circuit.

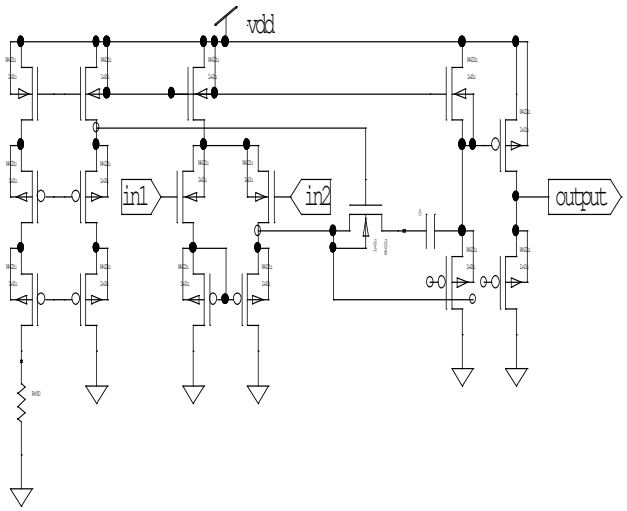


Fig.7.CMOS Switch Level Circuit of opamp

The proposed architecture is designed with CMOS device.

Sample and Hold Cell

The analog sample and hold circuit can replace the delay element of digital FIR filter .It is important in data converter system design. A MOS transistor holds and releases mobile charges when it is on and off respectively.

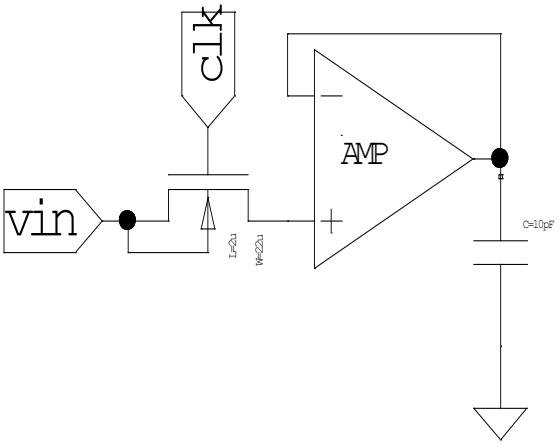


Fig.8.Schematic of Opamp sample and hold circuit

When clk is high, the MOS switch is on which inturn allows Vout to track Vin.When clk is low, the MOS switch is off. So capacitor will keep vout equal to the value of vin at the instance. The simple sample and hold results with charge injection and clock feed through. To overcome this drawback, modified opamp is used.

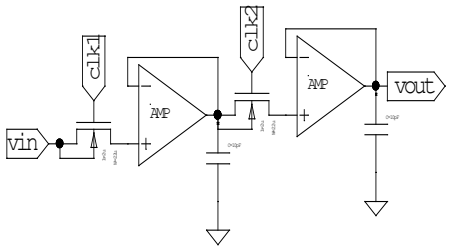


Fig.9.Schematic of Opamp sample and hold circuit

Multiplier Cell

Design of multiplier is a hard task.Opamp based multiplier is used .It uses the Opamp amplifier for multiplying the input and coefficient. The coefficient is set as the gain of amplifier and input is given to the opamp.

Output=input*gain (4)

The input is multiplied by gain value between 0.0 to 0.999 and output is produced. This forms the analog multiplier which reduces power, size and round-off noise. The analog multiplication is carried out using digital algorithm. The multiplier is designed with inverting amplifier. It satisfies negative coefficient multiplication.

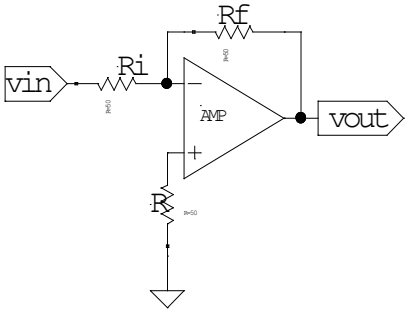


Fig.10. Schematic of opamp inverting Amplifier

The current I_1 through R_i is I_1=Vin/ R_i. (5)

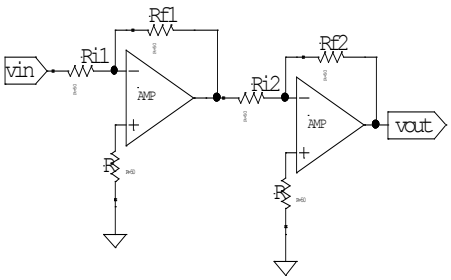
Since opamp draws no current all the current flowing through R_i must flow through R_f .The output voltage, out=-$I_1 R_f$=-Vin

(R_f /R_i). (6)

The gain of the amplifier is

A_{CL}=Vout/Vin=- R_f /R_i. (7)

If positive coefficient should be multiplied the output is given to an inverting amplifier with unity gain.



Schematic of Analog Multiplier cell

The Gain of multiplier A=- R_f /R_i. (8)
The output is given by Vout=A*Vin. (9)

For unity gain, R_i = R_f. So second opamp should have R_{i2} = R_{f2}.

Adder Cell

An opamp adder is used for analog signal addition. A summer circuit that gives non-inverting sum is the non-inverting summer.

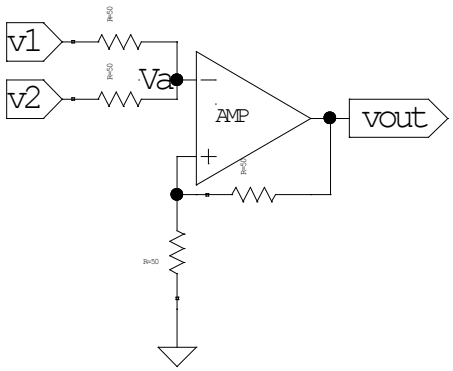


Fig.11.Schematic of Analog Adder cell

Let V_a be the voltage at input terminal. The nodal equation at node 'a' is given by

((V1-Va)/R1)+((V2-Va)/R2)=0 (10)

From which

Va={(V1/R1)+(V2/R2)}/{(1/R1)+(1/R2)} (11)

which is a non-inverted weighted sum of inputs.

The output Vout=V1+V2. (12)

Analog Architecture for DCT

The 8-point DCT architecture is designed with SAH, Multiplier and adder cell. Analog input is given directly to the sample and

hold circuit .the sampled signal is given to multiplier cell to get multiplied with the DCT coefficient. the output of multiplier is given to the adder and finally analog output is obtained.

For 8-point DCT,

$$X(K) = e(k)\sum_{n=0}^{N-1} x(n)\cos\left[\frac{(2n+1)\pi k}{2N}\right] \quad K=0, 1,\ldots 7. \qquad (13)$$

$$e(k) = \begin{cases} \frac{1}{\sqrt{2}}, & \text{if } k=0 \\ 1, & otherwise \end{cases} \qquad (14)$$

The architecture is designed using the matrix form.

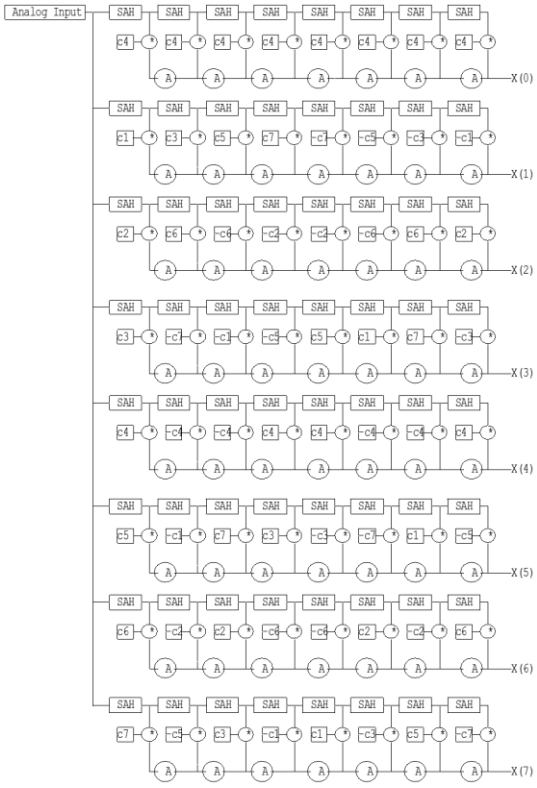


Fig.12.Schematic of Analog Architecture for DCT

The analog DCT architecture is advantageous than digital DCT in terms of reduced hardware, reduced power consumption and reduced cost.No round-off noise.

The proposed analog DCT architecture is advantageous than existing analog DCT using dynamic switched capacitors which results in leakage of charge. Now the switched capacitors are also eliminated which will increase accuracy, reduced power consumption, reduced cost and reduced hardware.

4. RESULTS

The circuits are simulated using Tanner spice and summarized. From the results, it is clear that the proposed system is efficient. The number of transistors in the circuit is deciding the circuit size.

Table 1: Comparison of Multipliers

Module	No.of transistors In numbers	Power Consumption in mW
Operational Amplifier	8	0.00273
Sample and Hold Circuit	11	1.01795
Module	No.of transistors In numbers	Power Consumption in mW
Digital Multiplier	4060	103.6731
Analog Multiplier	32	5.08

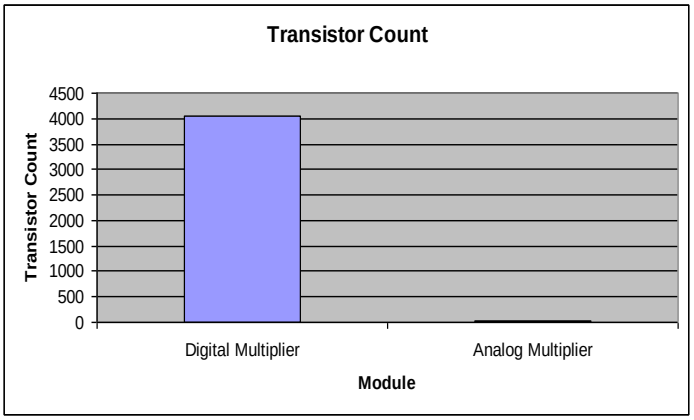


Fig.13.Comparison of Transistor Count

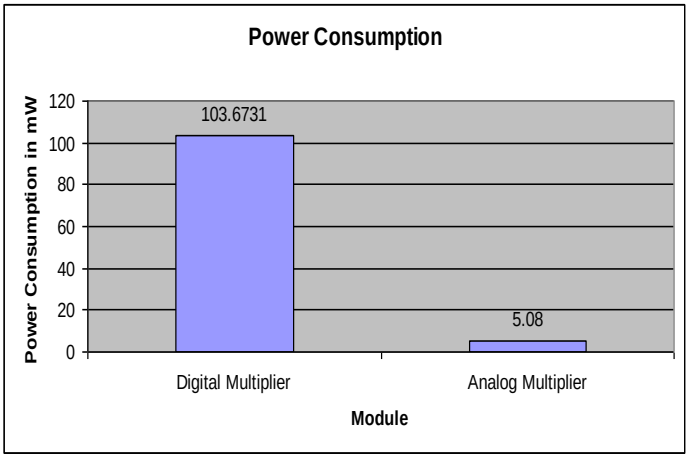


Fig.14.Comparison of Power Consumption

Table 2:Comparison of Adders.

Module	No.of transistors In numbers	Power Consumption in mW
Digital Adder	4060	103.6731
Analog Adder	32	5.08

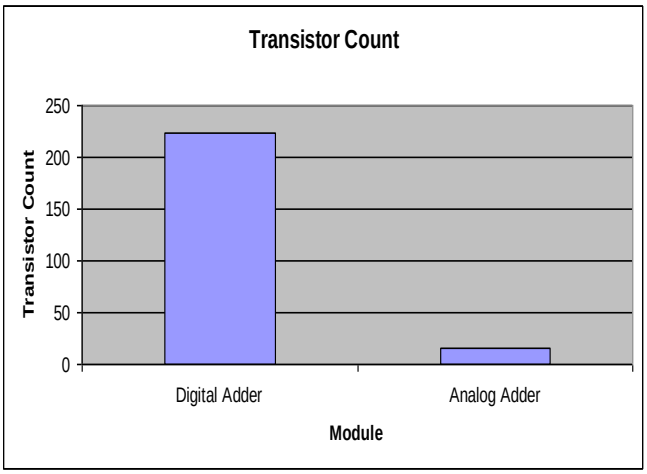


Fig.15.Comparison of Transistor count

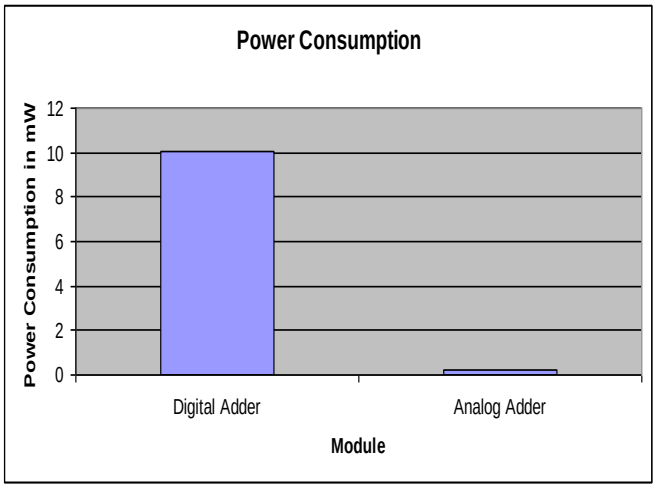


Fig.16.Comparison of Power Consumption

Table 3:Comparison of DCT Architectures

Module	No.of transistors In numbers	Power Consumption in W
Digital DCT	278784	7.440
Analog DCT	3648	1.058

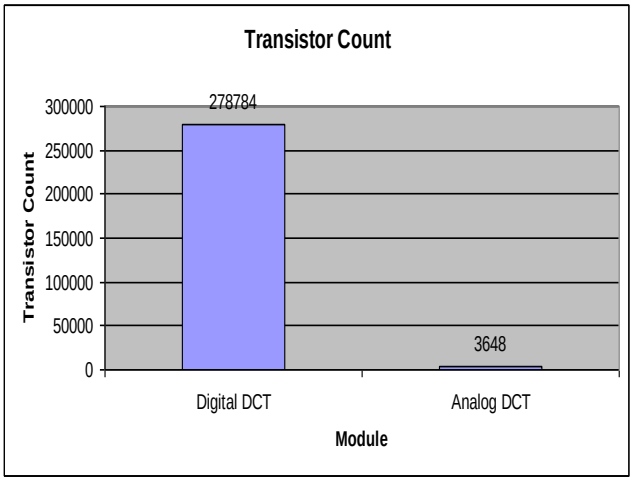


Fig.17.Comparison of Transistor Count

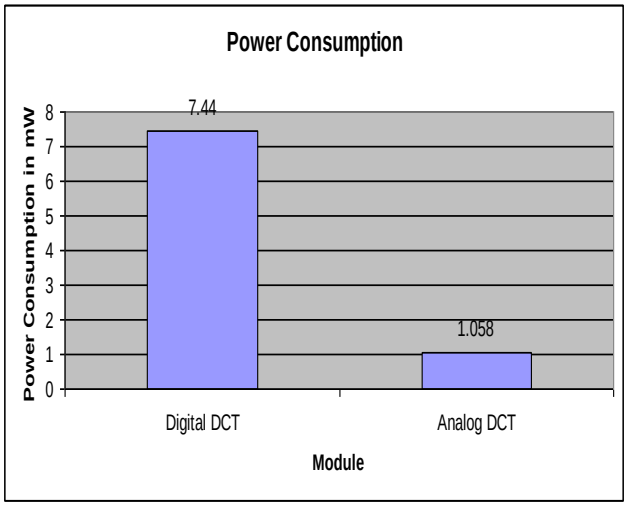


Fig.18.Comparison of Power Consumption

The result shows that Analog DCT architecture requires only 1.3% of the transistor count of Digital DCT architecture and the power is reduced 7 times than Digital DCT. Analog modules for DCT have been designed using HP1.2 µm CMOS technology at 5V. The operation is verified using TSPICE. The proposed analog CMOS implementation of DCT takes 1.058. W of power over 7.440W and 3648 numbers of transistors over 278784 numbers of transistors in the digital implementation respectively. The proposed analog architecture occupies less area, low power and high speed than existing digital system.

5. CONCLUSION

The analog VLSI architecture for DCT is designed and verified.The proposed architecture is advantageous than digital DCT and existing analog DCT architectures. The area and power is compared for the analog and digital modules .In Analog architecture, the area is reduced 76 times and power is reduced 7 times when compared to Digital Architecture. It is

concluded that proposed analog architecture for DCT is better than existing digital DCT and existing analog DCT architectures in terms of area and power. The speed of the architecture can be further increased by using high speed opamp in the module designs.

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