

The Digital Readout System for the CMS Electromagnetic Calorimeter

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Abstract

The readout system for the CMS ECAL detector [1], comprised of 80'000 PbWO₄ crystals, consists of two distinct parts; the on-detector Very-Front-End (VFE) electronics [2,3] and the Upper-Level Readout and Trigger system which is purely digital. The two parts are connected by a large number of optical links; one high-speed link per channel (~80'000) for the readout and two slow links per set of ten channels to distribute clock and control information to the on-detector electronics. This paper will concentrate on the Upper-Level electronics.

1. INTRODUCTION

The Upper-Level digital Readout and Trigger system of CMS ECAL consists of around 60 9-U VME crates, each serving up to 1700 readout channels corresponding to, in the barrel case, 68 trigger towers. This gives for the barrel one crate per supermodule. For the end cap, where the tower mapping is less uniform, the crate mapping will be slightly different. Fig.1 shows an overview of the CMS ECAL readout system.

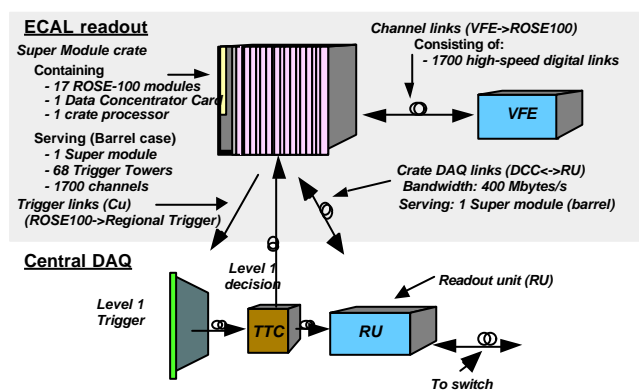


Fig. 1. The CMS ECAL readout system

Each crate contains 17 100-channel readout modules (ROSE100), one Data Concentrator module (DCC) and one standard VME CPU card.

The system provides the necessary control information for the VFE electronics over two 40 Mb/s optical links per group of ten crystals, i.e. a detector submodule. The modules receive the data over one optical link per crystal at an 800 Mb/s sustained rate. It provides information to the regional trigger on the energy, shower profile and time assignment per trigger tower and stores the data during the first level trigger latency. In case of a positive LVL1

decision, the corresponding data is transferred to the DAQ system. In addition, it provides means to assure the synchronisation and integrity of the data, both internally and with respect to the LHC bunch-crossings. The system provides all monitoring and test facilities required to assure proper functionality of the hardware. Also, it performs a local acquisition of monitoring data, such as signals from the light monitoring system, test pulses injected into the VFE electronics, crystal temperatures, monitoring of the APD bias currents, etc.

2. THE ROSE100 MODULE

The ROSE100 readout module, see Fig. 2, is the main component of the ECAL readout and trigger primitives generation. It is implemented as a VME 9-U module and contains all the functionality required to control, read and provide trigger information from four 5x5 crystal Trigger Towers, i.e. a total of 100 channels. Physically, the module consists of a motherboard containing all common circuitry, such as Board Controller, VME interface, etc. and four daughter boards, called Tower boards, with all functionality's required for one Trigger Tower.

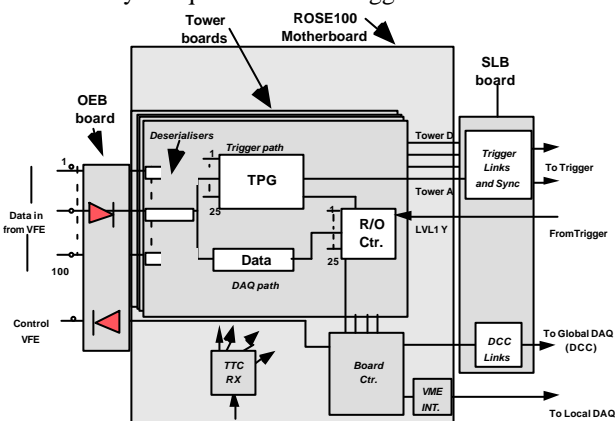


Fig. 2 The ROSE100 module

Furthermore, each ROSE100 has, in the transition board area, two link interface boards. One board is called Opto-Electro-Board (OEB) and contains the opto-electro interfaces for the links from-to the on-detector Very-Front-End (VFE) electronics (120 fibres). The other one, called the Sync-Link-Board (SLB), contains two fast copper (Gb/s) links to the Level-1 local trigger crate as well as one bi-directional fast copper (Gb/s) link to the DCC.

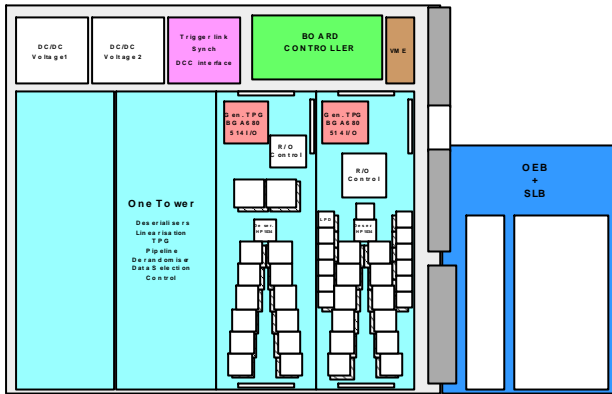


Fig. 3. Preliminary layout of the module

Figure 3 shows the preliminary layout of the module including the transition boards.

2.1 Opto-Electro-Board

The OEB contains one hundred 800 Mbit/s optical receivers carrying the data from the individual crystals as well as 20 optical transmitters, two per group of the 10 crystal detector submodule, one distributing the 40 MHz sampling clock and one carrying, in serial form, the parameters required by the VFE. The 12 fibres for one submodule are assembled into one fibre bundle.

Currently, the Siemens Paroli receiver is used but for the final production a more cost-effective solution will be sought. The outputs from the Paroli receivers are LVDS compatible signals which are routed as strip lines through an impedance controlled connector and distributed to the Tower boards. Tests have shown that the 800 Mbit/s signals can be safely distributed over the motherboard.

The clock and data to the VFE, generated by the Board controller, are routed as differential PECL signals through the same connector and currently the HP HFBR-1119T transmitters are used.

A laser safety interlock system is implemented to assure that, in case of fibre disconnect or break, all the transmitters belonging to a submodule bundle are shut off. The principle is to monitor two crystal fibres per bundle and, as soon as no activity is detected, the clock and data sent down to the VFE is shut down. When the VFE detects absence of the clock it shuts down all the transmitters belonging to that bundle. The time to shut down the entire loop is in the order of a few μ s (defined by the fibre loop length)

2.2 The Tower Board

Each of the Tower Boards contains the complete DAQ and Trigger path for 25 channels. The crystal data from the OEB arrives as LVDS signals and are applied to the deserialiser block (HP low-power G-link receivers). Thereafter, the data is compensated for differences in time-of-flight and length of fibres, linearised and applied to the Trigger Primitives Generator (TPG) where the tower

energy, Bunch Crossing Identification and, eventually, the Isolation bit is generated (see 2.2.2). Simultaneously, the data is stored in a digital pipeline of programmable length during the LVL1 trigger latency.

Information about crystal temperature, APD leakage current is sent, by the VFE, over the same path as the data and this information is also stored in the pipelines but do not participate in trigger decisions.

2.2.1 DAQ path

In case of a positive LVL1 decision the corresponding set of consecutive samples, a time frame, is extracted and stored in one of the derandomisers. The derandomiser area consists of a memory with 256 word. The number of derandomisers and their length can be programmed within this area up to a maximum number of 32 derandomising buffers.

The special data from the VFE is identified at the input stage of the Tower board. It is stored in the pipeline and an internal trigger is generated in order to extract the data from the pipeline. This information is extracted from the normal data blocks and sent through the local DAQ path (see 2.4.1)

A Readout Controller builds, for each LVL1 Yes, a tower data block containing the information from the 25 channels and adds the trigger primitives information corresponding to that event. A first step in the data reduction, zero skipping, is done at this level (see 4.)

2.2.2 Trigger path

The TPG must, for each bunch crossing, calculate the trigger primitives and in case of a positive time identification provide the local LVL1 trigger with information about Tower energy, time origin and, if appropriate, tag the primitives with the information that an isolated electron was found.

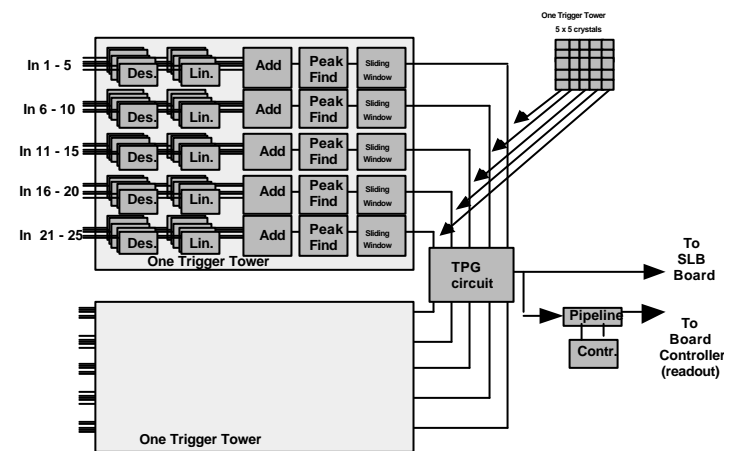


Fig. 4 The Trigger path

The data from the 5 crystals in a phi rows are summed and a peak finding/bunch crossing identification is made. The five strip sums are summed in two ways; all five to generate a total tower energy information and, for the

isolation criteria, two-by-two. The four two-by-two sums are compared and the largest one is compared to the total sum. If the two-strip sum is larger than a defined fraction of the total tower sum (programmable) an isolated electron has been found and the isolation bit is set.

The total tower sum is applied to a look-up table where it is converted to an 8-bit non-linear representation.

The primitives from two trigger towers are combined and sent, via the SLB, to the local LVL1 trigger process.

The algorithm described above is according to the current understanding. However, the algorithm is implemented in FPGAs thus allowing future changes.

2.3 Sync-Link-Board

This board is the interface between the ROSE100 and the external functions. It contains the link and synchronisation for the trigger information and the bi-directional link to the DCC module.

The trigger primitives from all towers in ECAL must be lined up in time at the outputs from all SLBs. To assure this the board contains an accumulator where the presence of information vs. machine clocks is histogrammed and compared to the BC0-signal from the TTC system. If the output is correctly timed, i.e. all latencies being compensated for, the histogram should reflect the LHC timing. Fig. 5 shows the content of the accumulator for different timings.

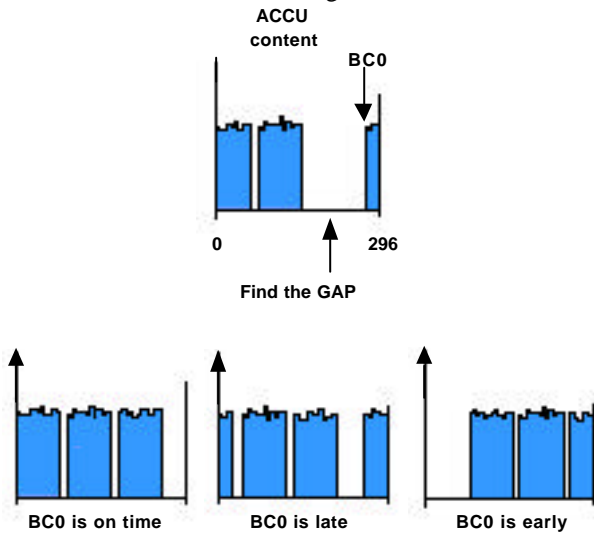


Fig. 5 Principle of trigger primitives synchronisation.

The link to the local LVL1 process is a high-speed (1 Gbit/s) copper link and the choice of the final hardware will be done together with the trigger project.

Data to/from the DCC will be transferred over bi-directional LVDS connections.

2.4 ROSE100 Motherboard

All common function blocks, e.g. Board Controller, VME interface and TTCRx, are implemented on the Mother board.

2.4.1 Board Controller

The Board Controller supervises all functions in the ROSE100 module. One of the main functions is to separate the data going, via the DCC, to the central DAQ system and data that is to be sent to the local CPU in the crate. The first path is called the Global DAQ and the latter the Local DAQ.

It builds the complete Global DAQ data block and checks for inconsistencies, such as wrong event or BC identifiers, separates the information about temperature, leakage current, etc. and sends it via the Local DAQ path.

When the VFE sends this special information the data is recognised before entering the pipeline and the Board Controller is informed that it should, with the proper delay, provide an internal trigger to the Tower boards.

The controller is also responsible for the dispatching, over the internal serial bus, of the set-up information to the various function blocks. It also, over the same bus, executes continuously various monitoring tasks.

It is built around two FPGAs and two dual port memories, one for the Global path and one for the Local path.

2.4.2 VME interface

A standard chip-set from Cypress™, the CYC7C960, is the heart of the implementation of this function. The interface is slave-only and supports all VME64 functions

2.4.3 TTCRx

A single TTC opto-electro interface is centrally placed in the in the crate and a twisted pair is distributed to each one of the ROSE100 modules. Each module has a TTCRx chip which provides the clock, trigger and event number with the proper delays.

3. DATA CONCENTRATOR CARD

The Data Concentrator Card (DCC), see Fig. 6, assembles the event data from the ROSE100 modules including the corresponding trigger primitives.

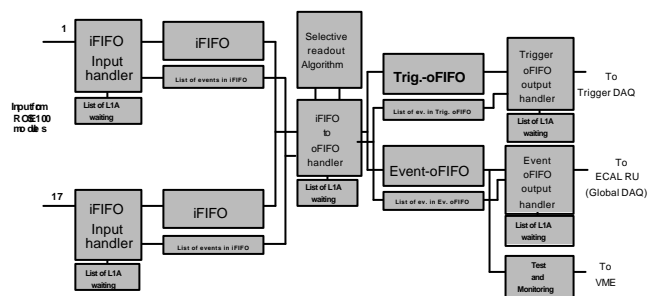


Fig. 6. The DCC Module

The Trigger primitives data is stripped off from the data block and sent to both the Selective Readout Algorithm function and the Trigger output FIFO. A data reduction is performed, using the Trigger Tower information as described below.

In the barrel case a complete supermodule data block is created and, upon request from the Readout Unit (RU) in the central DAQ system, pushed up through the RU to the event building switch network.

The Trigger Primitives information, stored in the Trigger output FIFO, is sent to the Trigger readout system where it is combined with the rest of the information from the trigger system.

A VME interface is provided to allow set-up as well as test and monitoring of the DCC functions.

If the CSRP (see 4) is implemented the DCC provides to the CSRP the information about the seed regions and gets back a map of channels to be read. This information is derived from the Trigger primitives. The links required for this option are not shown in the figure.

4 SELECTIVE READOUT

During high-luminosity LHC operation, physics triggers arrive in CMS at an average rate of up to 100kHz. The background physics interactions occur at a much higher rate. An average of 17 minimum bias events occurs per bunch-crossing, i.e. at a 40 MHz sustained rate. In order to isolate the front-end signals, which are in-time with the triggered bunch-crossing, the pulse shapes are digitised over a duration of several consecutive crossings, before and after the trigger, and stored in a time frame for analysis. The length of the time frame expands the data volume of the calorimeter to 2.4 MB/trigger. To reduce the data size down to 120kB/trigger in blocks of 2kB, as required by the central CMS DAQ system, a readout architecture incorporating data reduction algorithms was specially designed for this purpose.

A first step in this reduction is a zero skip operation performed at the Tower board level. The energy is estimated from the stored time frame and the frame is kept only if the estimated energy is above a defined threshold.

A more refined reduction is then done. The baseline for this data reduction architecture is to use the information extracted for the Level-1 trigger process and to execute the reduction, per crate, in the DCC module. Another possibility, currently under investigation, is to implement a dedicated Centralised Selective Readout Processor (CSRP) in order to facilitate the information exchange across the hardware boundaries. The DCCs will identify the seed regions and communicate them to the CSRP where a map is created of the channels to be read. This information is returned to the DCCs where the selective readout is performed.

5. CONCLUSION

The ECAL Upper Level Readout and Trigger system has been extensively prototyped over the last years. A first prototype readout system was built for the 1997 test beam period and during this year a ROSE50 module has been produced with all the functionality's required for the final system. It will be used to verify all functional blocks and allows a continuous evolution of the hardware implementation up to the point where the final production starts. This helps to avoid the problem with obsolete hardware already at the time of production as the current evolution of technologies is extremely fast.

A set of "stripped down" ROSE100 modules are currently under preparation for the different test systems required for the production of the individual ECAL components. Also, a 1700-channel system for the precalibration of the ECAL Supermodules is in the implementation phase.

6. REFERENCES

- [1]. ECAL TDR CERN/LHCC 97-33 15 Dec. 1997
- [2]. J.-P. Walder, Analog Signal Processing for the CMS Electromagnetic Calorimeter, LEB Rome Sept. 1998, CERN/LHCC/98-36 30 Oct. 1998 pp 218.
- [3]. P. Denes, Digitization and Data Transmission for the CMS Electromagnetic Calorimeter, LEB Rome Sept. 1998, CERN/LHCC/98-36 30 Oct. 1998 pp 223