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READOUT SYSTEM TEST BENCHES

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The list of institutions and signatures is not yet finalized. Contacts inside and outside the laboratory are in progress and, given the open structure of the project, additional participations are expected.

Abstract

We propose to develop and exploit versatile multi-purpose *Personal Computer-based Test Benches* to support the evaluation and design of the basic elements required for digital front-end readout and data transmission systems for an LHC experiment. These test benches will have modular hardware facilities for the operation of new readout system components under realistic conditions, and will implement advanced modern software engineering concepts. They will support components such as fast ADCs, hybrid fibre-optic transceivers, and the prototype VLSI systolic array and data-flow processors currently being developed in national research laboratories and by the emerging European HDTV industry. These efforts would also lay the foundations for projects involving the development of custom-designed VLSI circuits.

* Spokesman

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Introduction

Experiments at multi-TeV super colliders pose a tremendous challenge to the designers of the detectors, signal-processing and trigger systems. The increased complexity of the apparatus, and the extensive use of digital techniques in the measurement chain and in the selection devices, calls for a substantial investment in modern hardware and software technology.

In order to be ready to specify and implement a readout system for the next generation of experiments, it is necessary to associate with the current detector R&D programme a vigorous effort to acquire and exploit the most advanced laboratory and industry developments in the fields of digital processing, data communications and software tools. This proposal concerns hardware and software test bench facilities for laboratory and detector R&D applications, the architectural study and the implementation of high speed front-end and data communication prototypes.

Readout front-end overview

At LHC energy the high luminosity required by the low cross section of the interesting physical channels results in an unprecedented high collision frequency requiring event reduction factors several orders of magnitude higher than in current experiments. The machine bunch crossing separation of 15 ns is comparable to the signal propagation time through the detector elements. This imposes tight constraints on the readout architecture, which has to operate across the whole detector with a timing and control system comparable to that of a modern supercomputer.

The 'standard' readout model of a general-purpose experiment at a super collider has been described several times [1]. At present this architecture is only a tentative crude extrapolation of the parameters and the techniques used in experiments at the CERN SppS and the FNAL Tevatron. Without a precise specification of the scope and configuration of the apparatus we are not at present able to propose a real data acquisition system for LHC.

In the following we underline the items and the techniques which we consider common to any implementation and which appear most important for research and development work in preparation for an experiment at the LHC.

Front-end and first level trigger

In the current philosophy the first trigger level consists of local units logically mapped onto the detector elements or onto groups of them. Their main task is to identify candidates for kinematical objects, e.g. an isolated electron, an energy cluster or a muon. (Only measurement of the missing energy requires a global system and its feasibility depends on the apparatus and the machine luminosity). In general, the selection criteria are based on *pattern recognition* of 2 or 3 dimensional clusters in calorimeter or position detectors and track segments in muon chambers, cutting below thresholds on weighted energy sums and segment angles. At this level central tracking may not be affordable. The requirement of zero dead time and the high bunch crossing rate (67 MHz) determine the main characteristics of this stage of the readout; namely each detector signal has to be *pipelined* in a digital or analog way for the duration of the trigger system maximum latency (1-10 μs) and the trigger processing units must be ready to process events each bunch crossing period (15 ns). These characteristics suggest digital trigger architectures based on *systolic processors* or very fast *pipelined data-driven* systems with basic functions like *lookup tables, multiplier accumulators* and *control logic* with *contiguous cell communication.*

Digital and analog pipeline

The *analog to digital conversion* and the *pipeline* technique are other major issues. The signal digitization can occur before, during or after the first level. This choice is not yet completely clear and it will depend on the specific detector, the dynamic range, the power requirement and the engineering of the apparatus. Calorimeters require a large dynamic range (≈15 bits) and 9 to 10 bits of resolution [2] and they produce analog pulses overlapping several bunch crossings. Recent industrial developments in the field of VLSI circuits for HDTV (High Definition Television) indicate the possibility of prompt digital treatment of the signals during the pipeline phase, complementing the analog shaping with a *pipeline digital signal processor* that provides the physical parameter evaluation simultaneously.

Subsequent trigger levels

After the first level trigger the data of the selected event must be formatted and saved into local memories together with the related trigger information. The next steps in the readout are concerned with the refinement of the measurements of the objects previously found and with the calculation of kinematical parameters such as effective masses, transverse momenta and correlations between different detectors. Pattern recognition may still be needed for those detectors that were not taken into account at the first level. At this stage the readout is essentially *data-driven* and it can proceed asynchronously; the size of the local buffers and the data communication bandwidth will determine the deadtime. Several architectures can be envisaged as a function of the adopted

data access scheme. For example general-purpose processor farms will require very *high speed links* and *multi-port memories* while parallel systems will need local *selective data access* complemented with a global communication network.

The final stages of readout will consist of the full event record building, the event analysis and the mass storage. While general-purpose computers and standard networks developed by industry will supply the necessary computing power and communication facilities, the *standard buses*, the *event builder* and the *overall control system* will require ad-hoc study.

Independent of the specific experimental apparatus, it is generally acknowledged that the front-end electronics constitutes one of the most critical parts of an LHC detector readout system. The development of readout system test benches supporting the evaluation of *pipeline digital signal processing, data-driven processors and fast data communication links* is considered essential as a first step in acquiring the hardware and software expertise needed for an LHC experiment.

High speed readout systems

Readout architectures for LHC experiments will be required to support very high system bandwidths, comparable to those of modern supercomputers. For emerging applications such as HDTV, European industry is at present actively developing appropriate advanced basic components, like fast analog-to-digital converters and pipelined digital signal processors, as well as high-speed systems for image processing, digital video-tape recording and data transmission.

The evaluation of these complex devices and of efficient system architectures for detector readout can be achieved by the creation of versatile 'test benches' comprising personal computers and workstations closely linked with modular electronic systems and equipped with powerful interactive software. We propose to develop such test benches for application in our own studies and those of other proposed R&D projects.

To make maximum use of the collaborating laboratories' existing expertise and hardware investments, the modular electronics will initially be based on the VMEbus, complemented by special intermodule data links supporting transfer rates exceeding 100 Mbytes/sec. Available Macintosh computers will be used, supplemented by a number of Sun workstations which are required to support certain manufacturers' device and system simulation packages.

Basic hardware and software components to be developed
Memory modules for fast signal generation and retrieval *High-speed A/D converters* *Analog and digital pipelines* *Digital signal processors* *VLSI systolic array and data-flow video processors* *Enhanced computer interfaces* *High-speed data links and recorders* *UNIX-based environment with special data presentation facilities* *Simulation and development systems* *Application packages specific to the evaluations to be performed*

Different combinations of the above elements and tools would allow the configuration of a series of test benches optimized for various front-end, data transmission and trigger applications. They could thus be exploited by other project groups engaged in different aspects of LHC detector R&D. The proposed test benches would allow the detailed evaluation of architectures based on the devices currently being produced by European industry and national research laboratories, and lay the foundations for possible future projects involving custom VLSI development.

Hardware outline

Although existing standard buses do not meet the highest speed requirements, they do permit the desired modularity. We intend to use the VMEbus as the hardware support for our set of modules and to implement a high-speed intermodule link protocol for the high bandwidth simulation channel. The functions of some possible VMEbus modules are indicated below. Of course this list is not exhaustive and it is to be expected that other modules will be defined during the evolution of the project.

Fast Dual-port Memory - FDPM

This module provides the interface between any high speed (up to 133 MHz) front-end or data communication device under test and the evaluation and monitor system based on VME. The memory is implemented using high-speed CMOS and is organized in one or more banks with dual access from the VMEbus and the user port. The user port (8/16 bits) is driven by a simple protocol with burst mode capability under the control of an external clock. The module will be the basic I/O data generator and retriever. For short distances it will provide an electrical parallel (8/16 data bits) link to interconnect the other modules. For

relatively long distances (e.g. 100 m) the parallel link is converted (by other modules) into an optical link with a different protocol. Easy optical interconnection is an important target of this project.

In the test bench the dual-port memory plays the roles of data acquisition unit and digital pattern generator to feed digital signal processors or fast DACs. The latter combination permits the generation of analog signals or high speed pulses representing typical detector outputs. The high precision analog signals will be used to test various integrated ADCs, wideband detector front-end amplifiers, analog pipeline circuits, or other hybrid detector front-end devices.

Digital patterns will be used to exercise, in real time, cluster algorithms using digital or video signal processors or any other systolic array or data-driven processing architecture suitable for the solution of the complex trigger requirements.

Timing Unit - TU

Timing and synchronization are facilities common to all front-end electronics and are largely independent of the specific detector. The timing unit module has to distribute the machine bunch crossing frequency and the trigger timing for local front-end electronics. The module consists of a local clock with external signal phase-locking and a set of programmable delays with sub-nanosecond resolution for trigger and control signal fanout. Signal distribution by optical means is also to be considered.

Test Pulse Generator - TPG

The evaluation of analog to digital conversion and digital signal analysis procedures needs a versatile pulse generator which simulates the signal shapes expected from the detector. This module, in conjunction with the output of a fast dual-port memory, and equipped with fast DAC and specialized filters, provides the basic signal source for general ADC and front-end evaluation.

Analog to Digital Converter - ADC

Several implementations of this module are expected using the most advanced developments of the technology. The fast dual-port memory is used as the data acquisition interface.

Analog Pipeline - APIPE

The CERN-developed capacitor switch analog memory [3] together with the pipeline ADC conversion will be integrated in a module for performance evaluation.

Digital Pipeline - DPIPE

The digital pipeline is a common technique in drift chamber image readout. For an LHC calorimeter channel with a prompt analog to digital conversion, the pipeline is composed of a synchronous (all events) and an asynchronous (selected events) buffer. The data chain may also contain some digital processing. Memory delay lines and systolic digital signal processors [4] developed for HDTV can be used to implement these functions.

Data-driven Units - DSP and VSP

Very high speed (125 MHz) programmable data-driven array processors, (e.g. DAVIS [5]) designed for video signal processing are under development by the television industry and prototypes should be available in the near future. These components, integrated in a readout chain, can provide many of the functions needed at the first level of the trigger. This data-driven unit is one of a set of modules providing basic data flow functions.

Look-up Tables - LUT

Data conversion and pattern recognition trigger modules based on look-up tables, content addressable memories and programmable logic.

Protocol Adapter - PAD

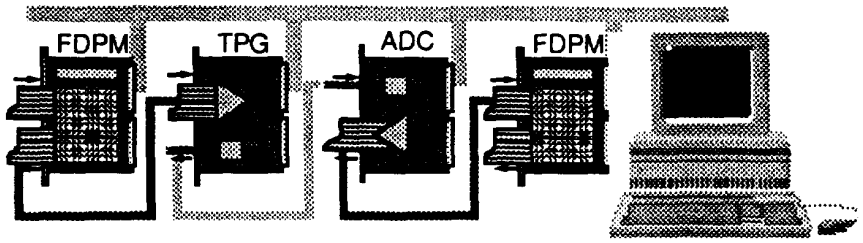
The protocol adapter module interfaces the fast dual-port memory to a serial or parallel data communication link. Several versions of the module are envisaged in order to build test benches for fast electrical and optical links and interfaces with standard buses.

Record Builder - REB

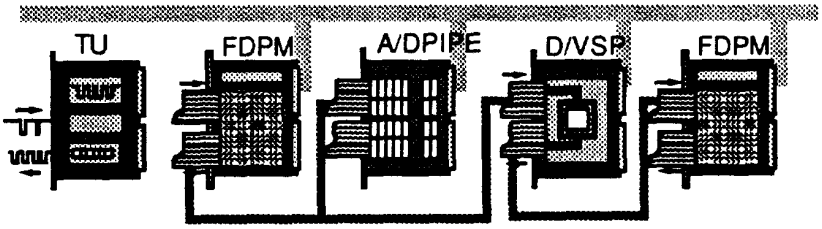
The record builder module is a data driver with multi-memory access. It provides the sparse data collection and the data communication between different readout stages.

The combination of the above modules will allow several configurations such as the following:

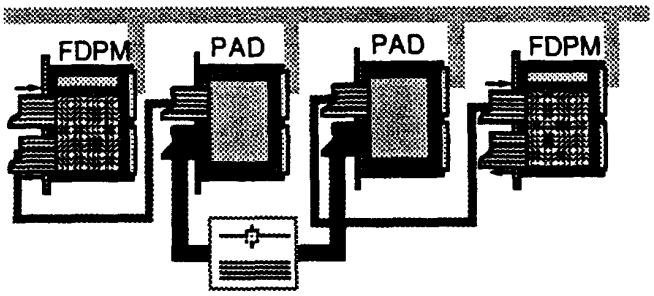
An ADC evaluation system:



An analog/digital pipeline and trigger system:



A data transmission test system:



Software outline

In the HEP community it was common practice to separate the different software activities around an experiment. In particular, online and offline groups were distinct, working on different computers with different operating systems, and even writing programs in different programming languages. This made migration of code across such groups very difficult and people tended to stay with a fixed activity. However, the increasing size and complexity of the more recent HEP experiments has clearly shown the need for full integration of all software in such an experiment. The boundary between offline and online software has

become less clear, although the problems of different operating systems and programming languages have remained.

In the era of future accelerators and experiments, these problems can only be solved by applying new concepts in both computing hardware and software. The ever-growing complexity requires the application of standards wherever possible. To make these new technologies affordable in terms of effort, cost and development time, industry products should be used extensively.

Currently, there is a strong trend towards standardization of operating systems, initiated by computer users in order to preserve software investment and to ease transition from one computer architecture to another. Productivity of programmers and users is also an important issue. POSIX has already published a number of standards with others to follow. Both UI (UNIX International) and OSF (Open Software Foundation), which together represent most major computer manufacturers, have already agreed to comply, now or in the near future, with these POSIX standards. Therefore, to fully benefit from developments in industry, other research institutes and universities, UNIX-like operating systems will have to be used. Despite the lack of realtime features, UNIX offers many appealing aspects such as a standard command interface, multitasking, virtual memory support and memory protection, networking and many useful standard tools and procedures. But probably the greatest advantage is its availability across many computer platforms, including the most recent RISC-based machines.

To cope with the required realtime capabilities, different solutions can be envisaged, ranging from realtime tasks embedded into standard UNIX to separate hardware processors loosely coupled to a UNIX system. There also exist realtime operating systems, which emulate UNIX functions and keep the "look and feel" of the UNIX command interface and tools. POSIX is also considering the addition of realtime features to its proposed standards.

We plan to use X-Window as the basic protocol for the user interface.

The X-Window System (X for short) is an industry-standard software package that allows programmers to develop portable graphical user interfaces. One of the most important features of X is its unique device-independent architecture. X allows programs to display windows containing text and graphics on any hardware that supports the X protocol without modifying, recompiling, or relinking the application. This device independence, along with X's position as an industry standard, allows X-based applications to function in a heterogeneous environment consisting of mainframes, workstations, and personal computers of different origin. X is available on most UNIX systems and also on many personal computers.

The basic X window system does not provide user interface components such as button, menus, or dialog boxes often found in other window systems. Most applications depend on higher level libraries built on top of the basic X protocol

to provide these components (XView, Motif, InterViews...). Using these libraries the test environment can be specified in text editable scripts.

In contrast with the past, it is foreseen that simulation will play a major role in the next generation of experiments. Simulation intervenes at several levels:
- gate-level simulation is needed to help design hardware components - it is already an essential tool in VLSI design.
- behavioral simulation will be of great help for defining and fine-tuning the architecture of readout systems and of complex software. It should be used up to the actual data-taking phase to forecast the effects of varying experimental conditions (background, triggers...) on e.g. the deadtime.
- simulation packages are part of the development kits available from the industry together with complex programmable chips (e.g. VSP).

Object oriented techniques for programming should boost the productivity and ease maintenance significantly by allowing the development of modular programs in an easy and natural way.

Several external institutes will participate in the development of the hardware modules. In order to work in a common framework and to easily integrate these modules in readout architectures, we propose to create a software development environment which will provide well defined tools to :

- Develop programs for testing the functionality of individual modules as well as different readout architectures using combinations of these modules.
- Develop and evaluate algorithms for all processing elements.
- Integrate industrial development packages.

Basic components :

- An interactive visual interface editor to allow user interfaces (dialogs, panels, plots, ...) to be prototyped rapidly and to define associated actions.
- Mathematical, statistical and signal processing packages.
- Support tools and libraries for remote system development and debugging (memory display, load/save, configuration and control scripts, cross compiler, linker, debugger, simulator ...).
- Data and status display tools.
- Simulation and algorithm design tools.

Many of these items are of general interest for the scientific community. Several of them are available or under development in industry and inside the laboratory. We intend to extract maximum benefit from available products and to collaborate with the related software activities of other proposals.

Conclusion

This project, while developing the basic tools for the creation of test benches, would stimulate the contribution of hardware and software expertise from all interested groups inside and outside the laboratory. Its main aims are :

- To develop a versatile modular personal computer-based test bench system to support the development, both within this project and in related studies, of front-end and trigger electronics for future LHC experiments.

- To exploit the test benches to study alternative front-end architectures and evaluate advanced components such as systolic array video signal processors being developed by industry and national laboratories. To evaluate other readout system elements such as signal pipelines, data-driven structures, record building and data transmission techniques.

- To lay the foundations for the specification and design of VLSI circuit implementations.

- To acquire expertise in the domain of open operating systems and software tools in order to drive the project design, to develop packages for the test of specific prototypes and to create the basic modules for future readout systems.

- To gain experience in the use of modern software techniques such as object-oriented programming, code generators, user interfaces and process simulators.

CERN budget request

The budget required from CERN is 760 kSF over the first two years. In addition we intend to recuperate the basic VME equipment, personal computers and MacVEE systems from the UA1 experiment. The other institutions are expected to finance their own equipment and the development of the modules designed under their responsibility. The production of modules for complete test benches will be the responsibilities of each institution with appropriate exchanges.

Basic boards development and production		150
Industry prototypes and evaluation packages		150
Test bench workstations and interfaces		80
Software packages and licences		80
Consumables		80
Cooperants and technical students		120
Travel and training		100
	Total	760

We stress the importance of including in the project a substantial component of young applied physicists and engineers in order to develop new collaborations with advanced technology institutes and to seed the future generations of data acquisition implementors. The request for travel and training is justified by the need for exchanges with industry and other national laboratories.

Sharing of responsibilities and collaboration with other projects

Some of us are already involved in other R&D projects at CERN and some of the test bench development work will be oriented to these applications. General software tools will be developed in collaboration with complementary proposals [6, 7].

The design and production of the prototypes will be shared among the collaboration in a way that will be detailed once the proposal is approved. At present Helsinki is already strongly committed to the development of hybrid and compact multi-optical fibre links.

The principal CERN tasks are the coordination of the design work and most of the software development. Documentation and software packages will be available to other interested projects on completion.

Project schedule

1991	*Basic VME modules design and development (FDPM, TU, ADC, DSG, APIPE, DPIPE)* *Software development system* *Hybrid optical link study* *ADC evaluation test bench* *Simulation and DSP algorithm study* *Video Signal Processor evaluation with simulator*
1992	*DSP and data communication test benches* *Hybrid optical link production* *Software development system* *Development of complete front-end for detector application*
1993	*Next project phase:* *ASIC specification and prototype production*

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