

# A HIGH REPETITION RATE ULTRA FAST HYBRID SWITCH MODULE FOR PROJECT X MEBT CHOPPER \*

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## Abstract

In order to serve several experiments simultaneously, the Project X requires a programmable chopping system to deflect bunches from the initially 162.5MHz CW H-beam. A helical 200 Ohm deflector is proposed, which needs a  $\pm 500V$  variable pulse length driver with  $\sim 2$  ns rise/fall time at an average repetition rate of 33 MHz. The SLAC Hybrid MOSFET/driver Switch Module (HSM) has demonstrated 1ns switching of 1 kV into a 30 Ohm load during 6 MHz burst operation. This paper presents the development and preliminary testing results of a new HSM, which is optimized for the Project X chopper driver parameters.

## I. INTRODUCTION

Project X [1] needs to simultaneously serve several experiments with different bunch structures. A programmable chopping system is needed to deflect unwanted bunches (90%) from the 162.5 MHz CW H-beam in an arbitrary pattern. A variable pulse length driver with  $\sim 2$ ns rise/fall time is needed by a proposed 200 Ohm helical deflector. The driver needs to provide  $\pm 500$  V flat top pulses with minimal flat top duration of 1.4 ns. The average switching frequency of the driver is 33 MHz. No commercially available solid state switches can switch at these parameters.

A Hybrid MOSFET/driver Switch Module (HSM) was designed at the SLAC National Accelerator Laboratory using advanced packaging techniques [2], which demonstrated 1.4 ns switching with a 1 kV drain-source voltage and a 30 Ohm load in 6 MHz burst operation. These results showed potential of power MOSFETs in ultra-fast switching applications.

This paper introduces a new HSM design, which was optimized for the Project X chopper driver parameters. Preliminary results obtained with the HSM are presented.

## II. DESIGN

### A. Power dissipation analysis and MOSFET selecting

The existing HSM was optimized for low average frequency burst operation while the Project X chopper driver requires high frequency high duty cycle operation. In this operation mode, one major concern is power dissipation.

MOSFETs in switching operation have three types of power losses: conduction loss, switching loss and capacitive loss (or  $C_{oss}$  loss).

The conduction loss is the loss due to resistive heating when current flow through the MOSFET:

$$P_{Conduction} = \frac{V_{ds}^2}{(R_{load} + R_{dson})} \cdot R_{dson} \cdot Duty\ Factor$$

Here  $V_{ds}$  is the applied drain-source voltage;  $R_{dson}$  is the on-state resistance of the MOSFET;  $R_{load}$  is the load resistance.

The only variable in this formula is  $R_{dson}$ . Previous research of HSM [3] shows MOSFET in ultrafast switching may not be fully saturated. As a result,  $R_{dson}$  can be as high as 4 times the datasheet value. The modified  $R_{dson}$  was used in Table 1 to calculate conduction loss.

The switching loss is the loss caused by the product of switch current and voltage when the MOSFET switches between on-state and off-state. Assuming linear change of drain current during switching, switching loss can be calculated using the following formula.

$$P_{Switching} = \frac{V_{ds}^2 T_{switching} f}{R_{load} + R_{dson}} \cdot \left( \frac{1}{2} - \frac{R_{load}}{3(R_{load} + R_{dson})} \right)$$

Here  $T_{switching}$  is switching time (2 ns was used in calculation);  $f$  is average switching frequency.

The capacitive loss, or  $C_{oss}$  loss, is due to the parasitic drain capacitance ( $C_{oss}$ ).

$$P_{Coss} = (C_{oss} + C_{load}) \cdot V_{ds}^2 \cdot f / 2$$

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Here  $C_{oss}$  is MOSFET output capacitance;  $C_{load}$  is the sum of all external capacitors connected to the drain of the MOSFET.

The  $C_{oss}$  of a MOSFET varies with drain-source voltage and the relation is highly nonlinear. The  $C_{oss}$  value in the datasheet (typically measured at  $V_{ds} = 25V$  and  $V_{gs} = 0V$ ) was used in the loss calculation.

Table 1 shows selected electrical characteristics of some MOSFETs and estimated power losses.

**Table 1.** Selected electrical characteristics of power MOSFETs and power loss estimation

Items		APT1201R2 (1kV HSM)	FQP2N60C (NMOS)	FB1P40 (PMOS)
$V_{dss}(V)$		1200	600	500
$R_{dson}(\Omega)$		1.2	4.7	10.5
$I_D(A)$		12	2	1.5
$C_{oss}(pF)$		365	20	40
Rise time (ns)		18	25	25
Fall time (ns)		21	28	30
Die size(mm <sup>2</sup> )		6.9x10.6	2.6x2.0	2.4x2.4
Loss @ 400V 33MHz (W)	Conduction	1.7	50	92
	Switching	12.7	26	28
	Capacitive	4100	144	288
	Total	4114.4	220	407

APT1201R2 is the MOSFET used in previous HSMs (1kV HSM). The estimated losses for operation at Project X parameters, dominated by capacitive losses, are unacceptably high, >4 kW. In order to reduce the capacitive loss, a MOSFET with smaller  $C_{oss}$  must be used, which means a smaller die and higher on resistance.

A very limited number of power MOSFETs are readily available in die-form and all of these would have very large power dissipation at the Project X chopper driver parameters. On the other hand, almost all packaged MOSFETs are available in die form with a minimum order quantity of one wafer (or 2000-3000 devices) with a long lead time (3-6 months). So dies decapsulated from package MOSFETs were used in the prototype HSM.

MOSFETs from multiple manufactures were investigated. Among which, FQP2N60C (NMOS) and FB1P40 (PMOS) (Table 1) from Fairchild Semiconductor were selected because they have the lowest estimated total loss among all the devices investigated.

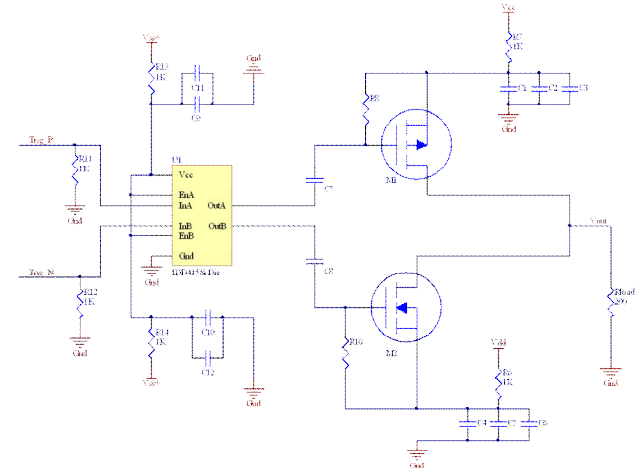
A commercial MOSFET driver from IXYS was used for the first prototype. The IXDD415 has a minimal pulse width of 6 ns and can work at 45MHz CW conditions with proper cooling. This driver is appropriate for initial test of the average power handling capacity and switching speed. The output current of this dual-driver is 15A for each driver, which should be enough to switch the

selected MOSFETs in 1-2ns. However, the minimum pulse width of the driver will limit the minimum output pulse width for the reason discussed in the next section.

## B. Circuit topology selection

A new topology is needed for the HSM since the one used in previous HSM has two major problems: The first problem is turn off time. The turn off time of the old HSM is determined by the RC recharging time of the MOSFET ( $R_{load} * C_{oss}$ ). With a 200 Ohm load, the output capacitance must be less than 4.5 pF in order to get a 2ns turn off time. No power MOSFET has such a small  $C_{oss}$ . The other problem is that the pulse length cannot be easily changed.

A totem pole configuration using complementary MOSFETs (Fig. 1) was selected for the new HSM. The turn on time of the HSM is determined by the PMOS and turn off time by the NMOS, which will not be affected by the load impedance. In this configuration, varying the delay between the triggers of the NMOS and the PMOS can easily change the output pulse length. But the delay cannot be smaller than the minimal pulse length of the driver (6ns), or shoot-through will occur; which will generate extra loss and may damage the power MOSFETs.

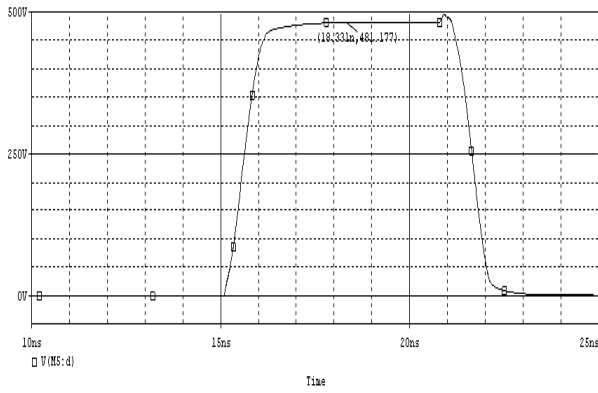


**Figure 1.** Circuit diagram of the totem pole HSM.

## C. Simulation

The design was simulated using PSPICE to validate the switching performance and power loss estimation. The MOSFET models from the manufacturer were used with the parasitic inductors and resistors removed to simulate flip chip assembly. Ideal voltage sources were used as MOSFET gate drivers.

The simulation result is shown in Fig. 2. The HSM shows a rise time of 0.86ns and fall time of 0.79ns. The energy loss per pulse was derived from the simulation. Multiplying those numbers by average switching frequency (33MHz) gives a loss of 102W and 142 W for NMOS and PMOS respectively.



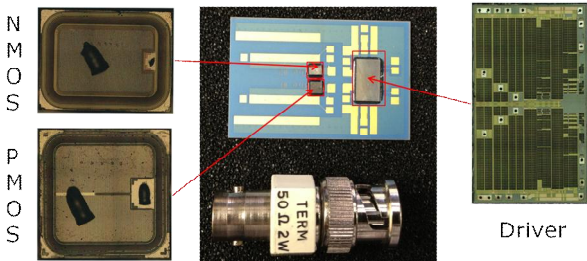
**Figure 2.** Voltage waveform of the load in the PSPICE simulation. The rise time and falling time is 0.86ns and 0.79ns respectively. The peak voltage is 480V for 500 V drain-source voltage.

### III. PRELIMINARY RESULTS

#### A. HSM fabrication

The NMOS, PMOS and gate driver were decapsulated and assembled on an Aluminum Nitride (AlN) PCB. Fig. 3 shows photos of the dies and the assembled PCB.

The decapsulated ICs were visually inspected for defects before assembly. The surfaces of those dies were generally clean, with minor residue from the Al bonding wires. Unlike the epoxy flip chip method used for the ILC HSM [2], a reflow process was used so that the board is suitable for high temperature operation.



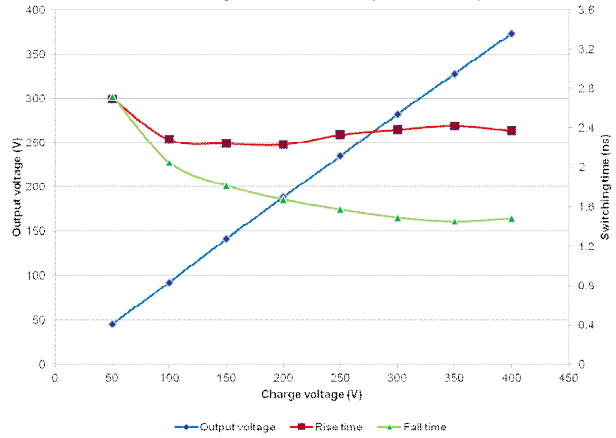
**Figure 3.** Photos of the dies and the PCB after flip chip assembly. Residue of the Al bonding wires (the black objects on the dies) can be found on all dies.

#### B. Test setup and results

The HSM was tested for single shot switching, pulse length variation, and burst operation. The cooling system was under development and the HSM will be tested for average power in the near future.

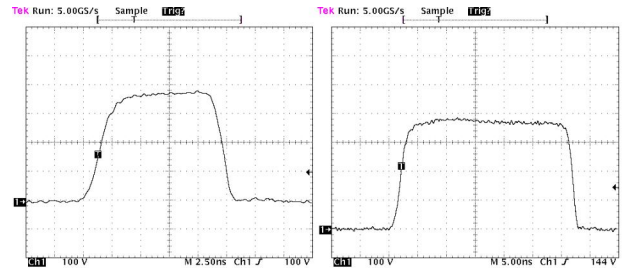
The switching performance of the HSM was tested under different drain-source voltages. The results are shown in Fig. 4. The HSM produced a 373 V output voltage amplitude with 400V drain-source voltage, which implies the PMOS has a  $\sim 12.5$  Ohm  $R_{dson}$ . The output voltage amplitude increases linearly with  $V_{ds}$ , which implies that  $R_{dson}$  does not change with output current.

The switching speed of the PMOS and NMOS were 2.4ns and 1.5ns respectively at 400V  $V_{ds}$ .



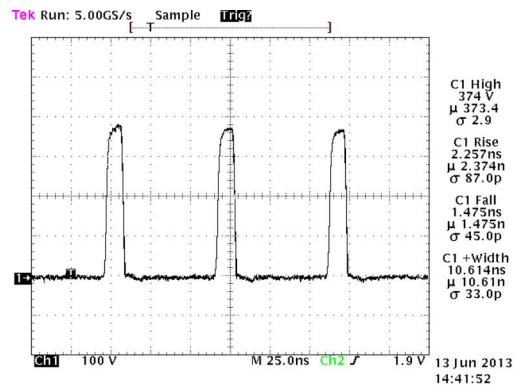
**Figure 4.** Switch performance of the HSM with a 200 Ohm load.

Varying the delays between PMOS and NMOS triggers changes the output pulse length. Fig. 5 shows output pulses of two different lengths: 10 ns on the left and 30 ns on the right. As discussed in the previous section, the HSM was not tested at high voltage for shorter than 10ns to avoid shoot through.



**Figure 5.** Output waveforms with different pulse lengths; 10 ns on the left and 30 ns on the right.

Burst operation was also tested, no distortion of the output waveforms was observed. Due to the limitation of the trigger generator, the burst rate is only 14 MHz. With better equipment, the system will be tested at the required 162.5 MHz burst operation.



**Figure 6.** Output waveform at 14MHz burst operation.

#### **IV. SUMMARY**

A high repetition rate Hybrid MOSFET/driver Switching Module (HSM) has been designed for the Project X chopper driver. Preliminary test shows the module can switch 400 V into 200 Ohm load with a rise time of 2.4 ns and fall time of 1.5ns. The output pulse length can be tuned to a minimum length of 10ns. No distortion or degradation of switching performance was observed in 14MHz burst operation. The HSM will be tested for average power handling once the cooling system is installed.

#### **V. REFERENCES**

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- [2] T. Tang, C. Burkhart, "Improved Hybrid MOSFET/driver Switching Module for Pulsed Power Applications", in Proc. 18th IEEE International Pulsed Power Conference, 2011, pp. 1365.
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