CMOS Integrated Power Amplifiers for RF Reconfigurable and Digital Transmitters

by

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ABSTRACT

This dissertation focuses on three different efficiency enhancement methods that are applicable to handset applications. These proposed designs are based on three critical requirements for handset application: 1) Small form factor, 2) CMOS compatibility, and 3) high power handling. The three presented methodologies are listed below:

1) A transformer based power combiner architecture for out-phasing transmitters

2) A current steering DAC-based average power tracking circuit for on-chip power amplifiers (PA)

3) A CMOS-based driver stage for GaN-based switched mode power amplifiers applicable to fully digital transmitters

This thesis highlights the trends in wireless handsets, the motivates the need for fully-integrated CMOS power amplifier solutions, and presents the three novel techniques for reconfigurable and digital CMOS-based PAs. Chapter 3, presents the transformer based power combiner for out-phasing transmitters. The simulation results reveal that this technique is able to shrink the power combiner area, which is one of the largest parts of the transmitter, by about 50% and as a result, enhances the output power density by 3dB.

The average power tracking technique (APT) integrated with an on-chip CMOS-based power amplifier is explained in Chapter 4. This system is able to achieve up to 32dBm saturated output power with a linear power gain of 20dB in a 45nm CMOS SOI process. The maximum efficiency improvement is about $\Delta\eta=15\%$ compared to the same PA without APT. Measurement results show that the proposed method is able to amplify

an enhanced-EDGE modulated input signal with a data rate of 70.83kb/sec and generate

more than 27dBm of average output power with EVM<5%.

Although small form factor, high battery life time, and high volume integration

motivate the need for fully digital CMOS transmitters, the output power generated by this

type of transmitter is not high enough to satisfy the communication standards. As a result,

compound materials such as GaN or GaAs are usually being used in handset applications

to increase the output power. Chapter 5 focuses on analysis and design of two CMOS

based driver architectures (cascode and house of cards) for driving a GaN power

amplifier. The presented results show that the drivers are able to generate ΔV_{out}=5V,

which is required by the compound transistor, and operate up to 2GHz. Since the CMOS

driver is expected to drive an off-chip capacitive load, the interface components, such as

bond wires, and decoupling and pad capacitors, play a critical role in the output transient

response. Therefore, extensive analysis and simulation results have been done on the

interface circuits to investigate their effects on RF transmitter performance. The

presented results show that the maximum operating frequency when the driver is

connected to a 4pF capacitive load is about 2GHz, which is perfectly matched with the

reported values in prior literature.

DEDICATION

To my kind father, beloved mother, and dear brother.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

1.1   Wireless Handset Hardware Trends

The number of cell phone users has already surpassed the world's population and is expected to reach over 8 billion by 2020, as shown in Fig. 1-1. Furthermore, the number of mobile broadband subscriptions (256kb/s or greater) is continuously increasing over time and becoming more diverse across different areas (Fig. 1-2). With the exponentially growing market for wireless mobile communication, optimizing the performance of the cellphone device, such as processing speed, video quality, memory capacity, power dissipation, linearity, sensitivity and physical size, is critical to the single-user experience as well as to the advancement of wireless technology and overall energy efficiency.
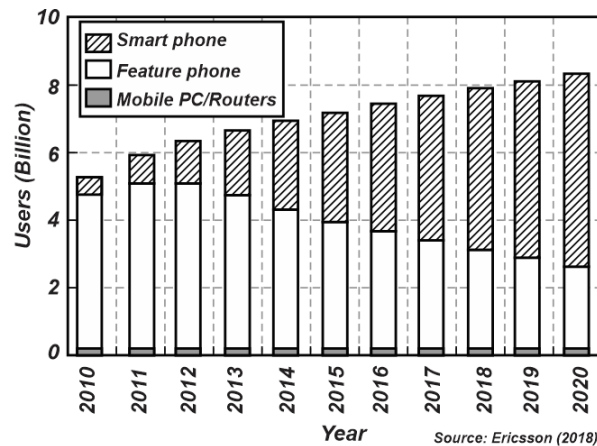
Fig. 1-1, Number of cell-phone users over time

Fig. 1-3a shows a usage breakdown for the different applications on a general smart phone in the United States for an adult in a single day. As can be seen in Fig. 1-3b, the cellular phone is connected to the wireless network over half the time to support the

typical applications. This wireless connection is done through Wi-Fi, Bluetooth or the cellular network using protocol such 4G, LTE. Therefore, to reduce overall power consumption in the handset and increase its battery lifetime, there is a strong need to minimize the wireless transceiver's power consumption.
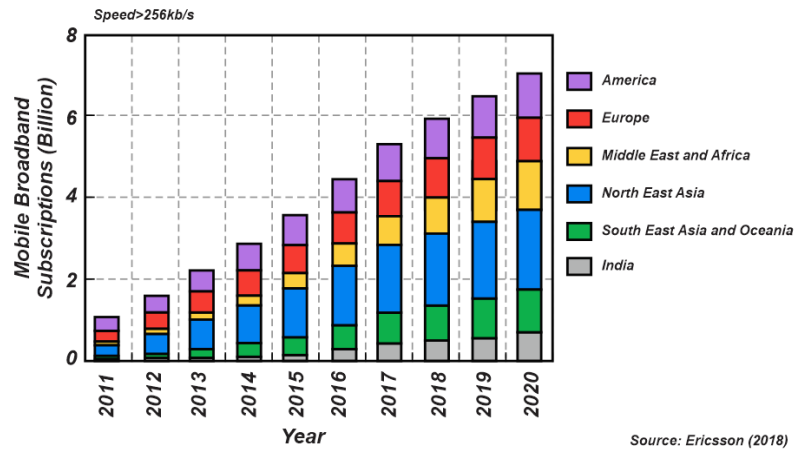
Fig. 1-2, Number of cell-phone users over time for different regions

a)

b)
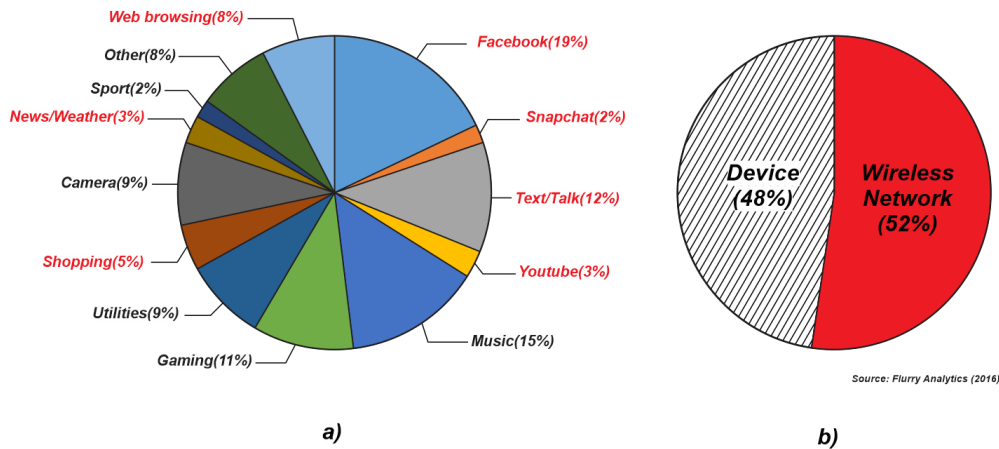
Fig. 1-3, a) Percentage of smart phone usage, b) Comparison between the wireless and device usage

Fig. 1-4 a, b show the power dissipation breakdown of a sample low power receiver (RX) and transmitter (TX) that has been designed in a 40nm CMOS process to meet the IEEE 802.11a and IEEE 802.11h standard requirements with operating frequency from 755MHz to 928MHz [1]. The total power consumption of the RX and TX are P_{RX}=4.43mW and P_{TX}=7.2mW respectively. It is quite clear that although the phase

locked loop circuit consumes most of the power in the RX section (P_{PLL}=1.55mW), the other stages such as the low noise amplifier (LNA) and the mixers consume approximately the same amount of power.

Unlike the receiver section, the power dissipation in the transmitter has quite a different pattern. As shown in Fig. 1-4b, most of the energy in the transmitter (almost 53%) is dissipated by the power amplifier (about 86% of the energy dissipated by the entire receiver). This unequal power distribution between the PA and the other blocks in the TX section illustrates the importance of PA energy optimization.
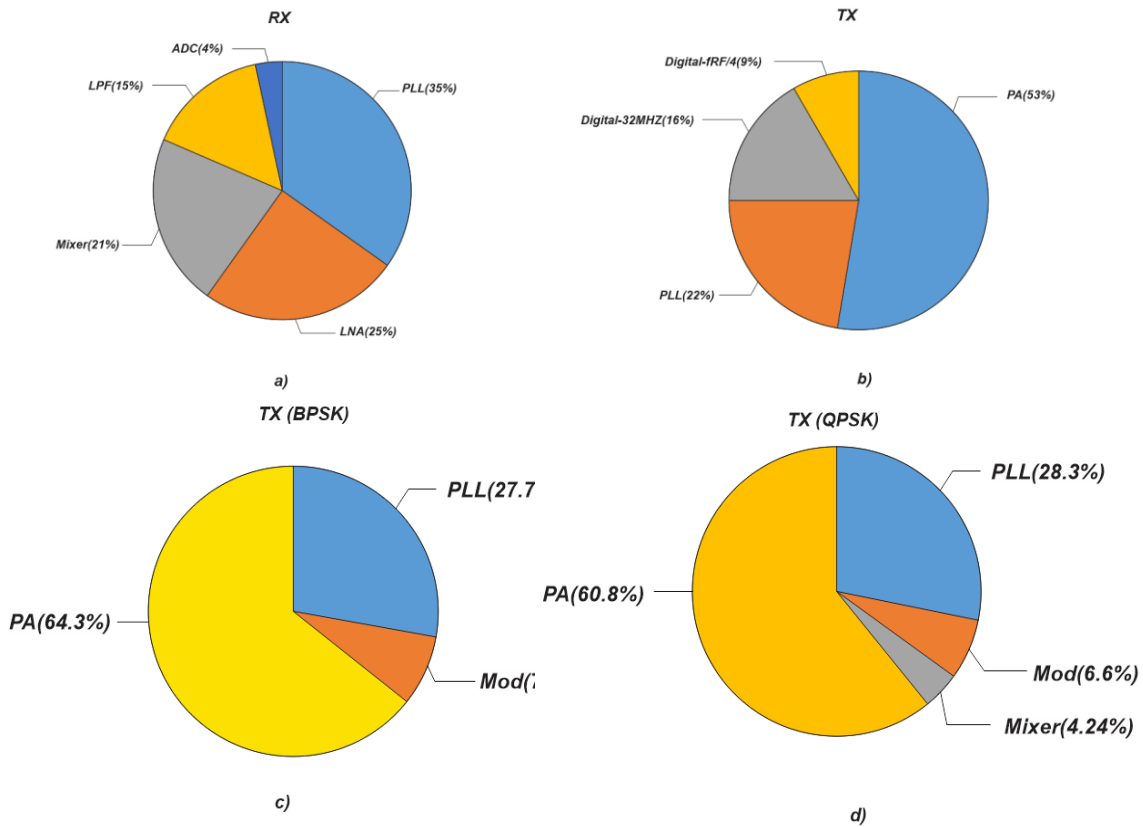
Fig. 1-4, Power consumption comparison in different blocks in a low power CMOS transceiver at 755-928MHz a) Receiver section, b) Transmitter section, Power consumption comparison in different blocks in a low power CMOS transceiver at 84-87GHz (Since the transmitter is fully digital, the PLL block has been utilized as the mixer and therefore, no power dissipation is assigned to the mixer block) c) TX with BPSK modulation, d) QPSK modulation

Since 5G communications and beyond is moving toward millimeter wave frequencies for transmission, Fig. 1-4 c, d show the power dissipation breakdown of a low power transmitter at the W-band (84-87GHz) for BPSK and QPSK modulations in a 65nm CMOS process [2]. The PA again dissipates a significant portion of the power consumption (more than 60%), and this example also demonstrates the need for increasing efficiency in millimeter wave power amplifiers. The work of this thesis presents efficiency-enhancement methodologies for CMOS power amplifiers and pre-drivers.

1.2   Challenges of PA Design for Cellular Applications

In recent years, the demand for high speed communication has grown significantly, with 100 times data rate increase within a 10-year span. This significant expansion is illustrated in Fig. 1-5, which plots the data rate trend for three main communication networks (short links, LAN and cellular). Fig. 1-6 shows the percentage utilization of the new generation communication standards (LTE and 5G), demonstrating that LTE is popular among the total wireless users in the US and 5G is expected to become operational in 2019.
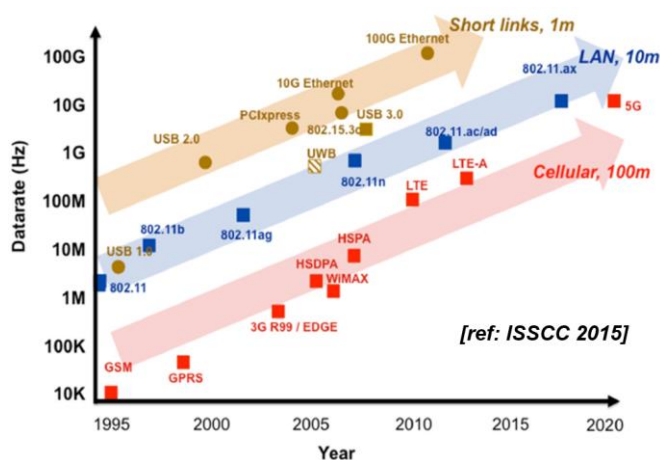
Fig. 1-5, Wireless standard trend over time

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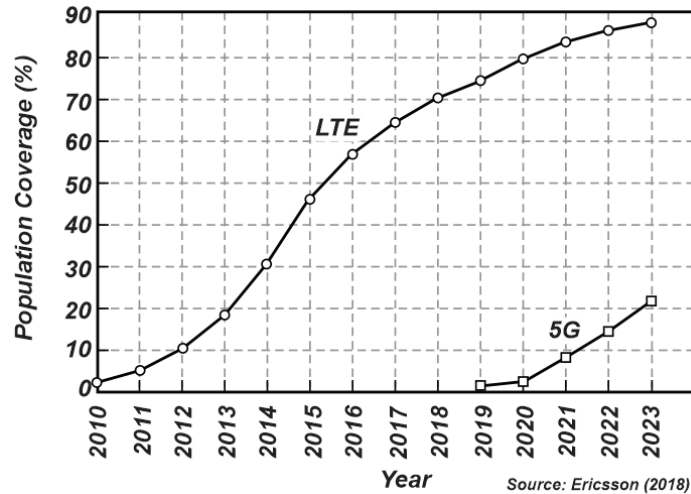
Fig. 1-6, LTE and 5G standard trend over time

One of the main solutions to increase the data bit rate in cellular networks is to utilize digital communication standards such as GSM, WCDMA and LTE [3]. In order to satisfy the required data rate, these communication protocols use advanced digital modulation techniques such as OOK, PSK, QPSK, 16QAM and OFDM. Due to the fact that these techniques modulate the signal in amplitude and phase domains, the transmitted RF signal continuously varies in output power. The average transmitted output power is mainly set based on the distance between the cell phone (handset) and the base station tower. Whereas the peak power with respect to the average power will depend upon the wireless modulation scheme.

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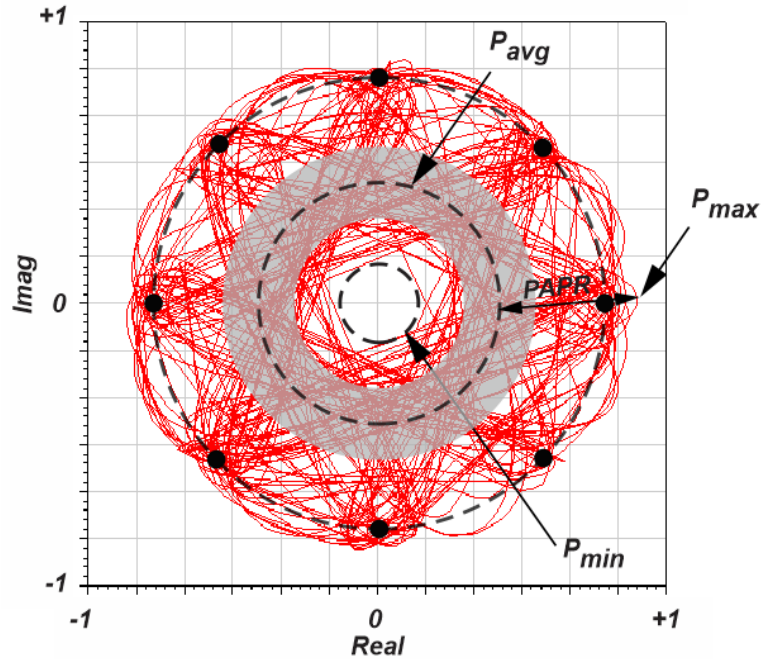
Fig. 1-7, Movement of the π/4 QPSK on the constellation diagram

The ratio between the maximum (peak) output power and the average power is defined as peak to average power ratio (PAPR). PAPR is a critical parameter in wireless telecommunications because higher PAPR typically correlates to higher linearity requirements and power consumption in a wireless transceiver. Fig. 1-7 shows the movement of the output signal vector on the constellation diagram over time for π/4 QPSK modulation. This example illustrates that the maximum output power (P_{max}) does not happen very often, and most of the time the output power level is below the P_{max}. In order to characterize the power distribution of a wireless modulation scheme (standard) over time, the probability density function (pdf) of the transmitted output signal is used. Fig. 1-8 a-d show the pdf of different digital communication standards. As can be seen, the peak of the pdf moves towards the left for more advanced schemes such as OFDM, which means high PAPR value in recent wireless systems. Fig. 1-8e summarizes the PAPR values for the most common digital standards [4]. There is a significant need to

develop high efficiency power amplifiers that process these high PAPR signals for

supporting future-generation communications standards.
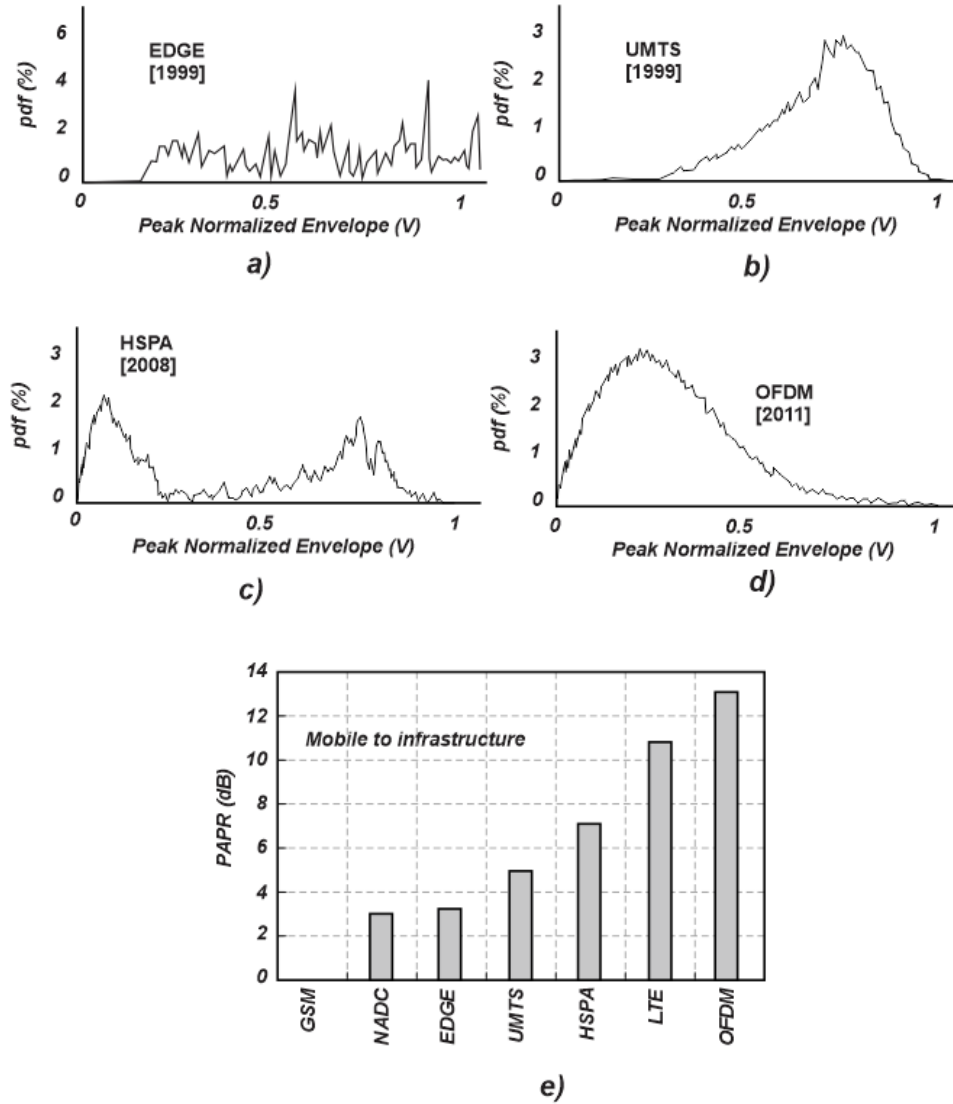
Fig. 1-8, Probability density function of common communication standards a) EDGE, b) UMTS, c) HSPA, OFDM, e) comparison between the PAPR values of common standards

1.3 Silicon CMOS versus Other Compound Materials

Traditionally, compound devices such as SiGe and GaAs have been utilized for

high power generation in handset applications because of their superior device

performances, including high break down voltage capability, high unity gain frequency

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(f_T), low substrate loss, low source path resistance to ground, high thermal conductivity through the substrate, and low loss metallization (thick metal layers). Fig. 1-9 compares most of the important parameters in the compound devices to the silicon process.
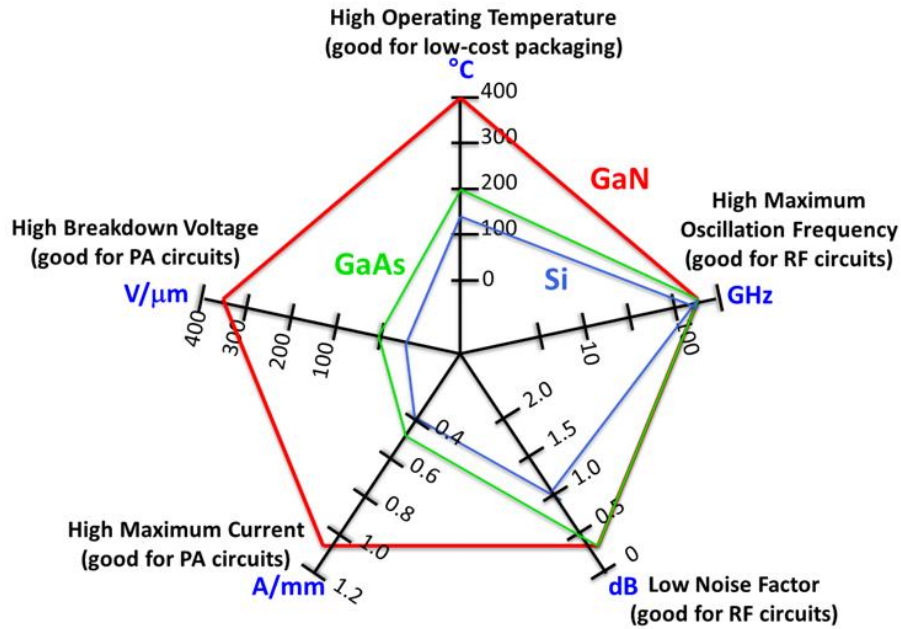
Fig. 1-9,Properties comparison between Silicon, Gallium-Arsenide and Gallium-Nitride materials

Although the compound processes show benefits over silicon technology in some aspects, there are several advantages associated with silicon IC processes that motivate designers to use this technology over the compound processes. These important aspects are listed below:

1) Low yield loss of silicon integrated circuits compared to the compound materials

2) High component-count integration of silicon devices

3) Silicon's low cost final price [5]

4) Capability for integrating the digital processing unit and the PA on the same substrate

5) Available high speed CMOS architectures

Since silicon-based architectures have high yield compared to compound processes, designers prefer to use silicon technology when integrating a large numbers of transistors. When compared with GaN, the cost of silicon-based products is much lower because GaN requires higher purity silicon/SiC substrate material, is implemented on smaller wafer size, and has significantly lower yield. Fig. 1-10 compares CMOS process technology with two of the most common compound processes (GaAs and SiGe) in terms of number of products and applications [5]. Fig. 1-10 demonstrates that the CMOS based RF modules are more cost effective compared to other compound materials.
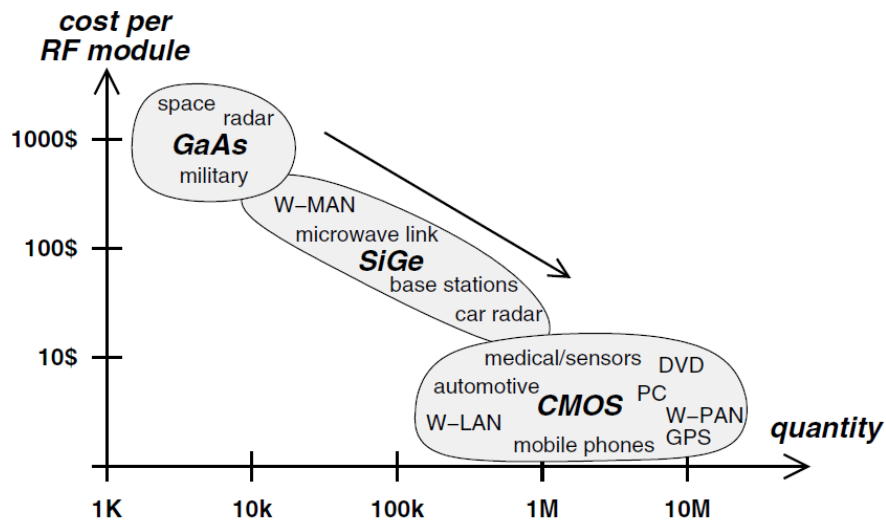
Fig. 1-10, Cost versus quantity comparison between different materials

Furthermore, the number of integrated transistors in GaAs and GaN compound technologies has typically been limited to less than 40 devices per die. But, the CMOS process provides the capability of fabricating millions of transistors on the same substrate. As a result, CMOS processes are the most promising option for high volume fabrication. Recently, novel techniques have been proposed to design highly efficient CMOS PAs at high frequencies [6], therefore enabling integration of the digital signal

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processor with the high-frequency wireless transmitter (PA). Fig. 1-11 compares CMOS with SiGe and GaAs [5] in terms of frequency (speed) and performance (power and efficiency). Although the compound transistors intrinsically provide high performance, new circuit and system level techniques in CMOS are enabling higher power levels and pushing the performance of CMOS to compare with that of SiGe and GaAs.
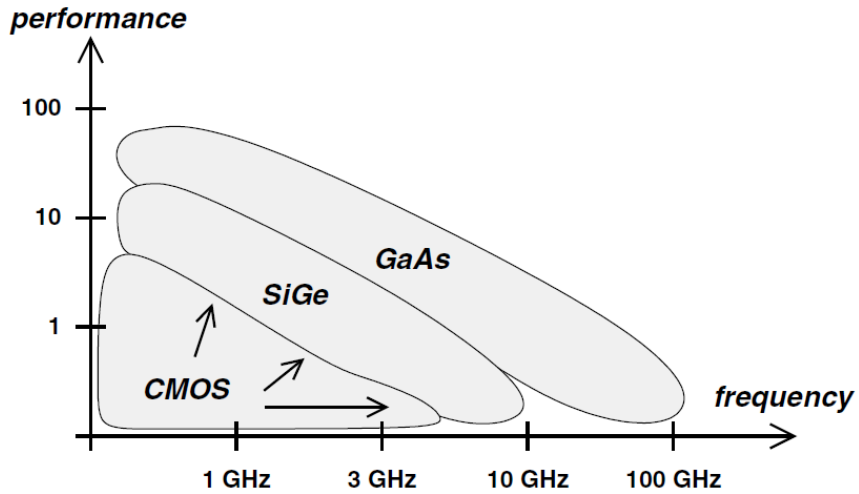
Fig. 1-11, Performance (speed, power and efficiency) versus frequency comparison between the most common materials

1.4   Thesis Objectives

The availability and popularity of mobile handsets has been discussed, and it has been shown that the reliability and cost of wireless modules motivates the desire for using CMOS PAs instead of compound materials.

The main purpose of this dissertation is to investigate and analyze small form factor CMOS based efficiency enhancement techniques for high PAPR signals that are applicable to handset applications. This research proposes three different efficiency enhancement methods: 1) average power tracking (APT) using a current steering DAC, 2) implementation of a digital driver for a GaN power amplifier and 3) small form factor transformer based power combiner for out-phasing transmitters.

This dissertation organized as follows: Chapter 2 reviews the background and prior works for efficiency enhancement techniques in handsets. Chapter 3 explains the out-phasing efficiency enhancement method and proposes an implementation technique for a small form factor power combiner that is suitable for CMOS integration. In chapter 4, the APT technique will be discussed and the proposed current steering DAC based efficiency improvement technique will be explained. Chapter 5, introduces a CMOS-based driver (digital power amplifier) that is suitable for fully digital transmitters and all the challenges associated with the implementation will be analyzed and discussed.

CHAPTER 2

BACKGROUND AND PRIOR ART

This chapter reviews the most popular techniques that have been utilized to

enhance the efficiency of the PA block, focusing on the techniques that are applicable to

CMOS PAs for handset applications. These techniques include PAPR reduction [7-9],

Dynamic range control [4], Doherty [10], envelope elimination and restoration (EER)

[11], envelope tracking (ET) [12] and Out-phasing [13].

2.1   The Importance of PA Efficiency Improvement

As mentioned in Chapter 1, the utilization of advanced digital modulation

techniques in new communication standards increases the PAPR of the output signal. In

order to understand the degradation effect of high PAPR on the PA performance, Fig. 2-1

plots the pdf of the OFDM (PAPR≈13dB) signal on top of the efficiency versus

normalized output voltage for different classes of linear PAs.
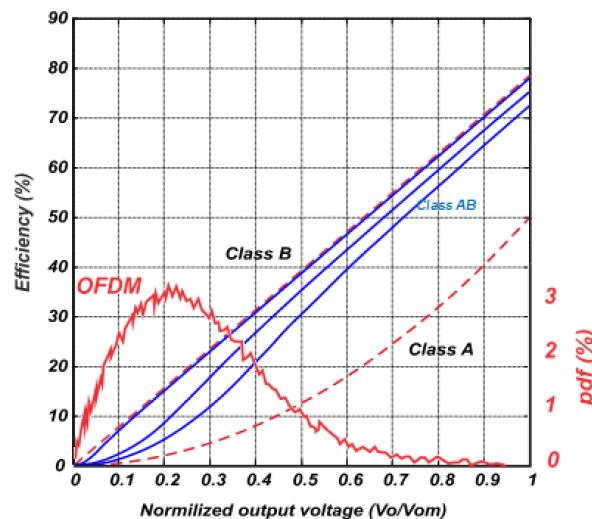
Fig. 2-1, Linear PA efficiencies as a function of normalized output voltage for different classes of operation
as well as the pdf of the OFDM signal

From the pdf of Fig. 2-1, it is apparent that the OFDM signal spends the majority of its time at voltage levels where linear PAs are highly inefficient. Although moving from class "A" toward class "AB" and "B" improves the PA efficiency, the best effective efficiency is still less than 20% (a value that does not satisfy most of the cell-phone transmitter requirement). Therefore, there is a trade-off between the linearity and efficiency of the PAs. Class "A" PA, which is the most linear type of PA, has the lowest efficiency among the class "AB, B" counterpart. In order to improve the low efficiency of the PAs at high PBO levels several system and circuit level techniques have been proposed.

2.2   PAPR Reduction Techniques

The efficiency of the PA reduces significantly when the output power of the PA is highly backed off from the maximum available output power. This degradation in efficiency affects the overall transmitter efficiency when it processes a digital signal with high PAPR value. In [7-9], some techniques have been presented to reduce the PAPR value of the OFDM signal. The principle of this technique is based on analyzing the modulated signal statistically over time and checking how often the signal has a high PAPR value. If the high PAPR value occurs very infrequently, then the signal pre-distortion techniques such as peak windowing can be applied on the modulated signal to reduce the PAPR value. It has been shown in [7] that the PAPR of about 4dB can be achieved with this technique for an arbitrary number of subscribers at the cost of a slight increase in bit error rate (BER). In [8] it has been shown that by increasing the number of channels in the OFDM system, the probability of high PAPR reduces. Mainly, the PAPR reduction techniques can be organized into two different categories: 1) Signal scrambling

techniques (ex. partial transmission sequence (PTS)), 2) signal distortion techniques (ex. Clipping) [9].

2.3 Dynamic Range Control

It is required that the signal applied to the PA does not have a zero envelope (zero power) value. Otherwise, the phase of the input signal has discontinuity and as a result, the transmitted signal becomes highly nonlinear [4]. Under this condition, the PA must be highly linear, especially at zero magnitude. Implementing the PA with a wide range of linearity requires high power dissipation and eventually degrades the overall efficiency of the transmitter. Since the zero envelope value means passing through the origin of the constellation diagram of the modulated input signal, traditionally a technique, called constellation rotation, has been proposed [4]. In this method, two similar constellation diagrams are put on top of each other with some phase rotation between them. By assigning one symbol to one of these constellations and the adjacent one to the other constellation the origin transition will be prevented. The other technique that prevents origin crossing is to set an offset of about half of the symbol time between the in-phase (I) and quadrature (Q) signals [4]. As an example, two of the most common digital modulations that are $\pi/4$-QPSK (used in NADC, TETRA and Bluetooth) and $3\pi/16$-8PSK (used in EDGE) are shown in Fig. 2-2 a, b respectively.
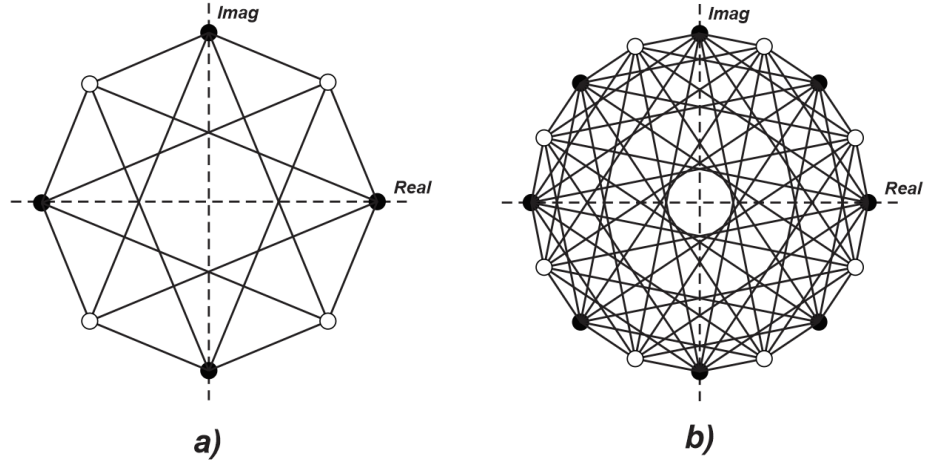
Fig. 2-2, a) The constellation of π/4 QPSK, b) 3π/16-8PSK

2.4 Doherty Power Amplifier

This type of efficiency enhancement technique, which is proposed in [10] for the first time, is based on load modulation. The basic concept, the architecture and the efficiency of this amplifier are shown in Fig. 2-3. The linear amplifiers are modeled with current sources and the load is set to $R_L/2$. When the input power is at high backed off power, the I_2 current source is zero and all the output current is provided by the I_1. When the input power is close to the maximum power, the I_2 starts to conduct and provides some portion of the output current. If at the full input driver power level these two currents are equal, the Doherty amplifier is called symmetric. Otherwise, it is called asymmetric Doherty PA. The effective input impedances seen from each current source are:

$$Z_1 = \frac{R_L}{2}(1 + \frac{I_2}{I_1}) \tag{2-1}$$

$$Z_2 = \frac{R_L}{2}(1 + \frac{I_1}{I_2}) \tag{2-2}$$

When $I_2=0$, $Z_1=R_L/2$ and the impedance seen by the I_2 current source $Z_2=\infty$ and when both current sources generate the same amount of current ($I_2=I_1$) they see similar

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impedances ($Z_1=Z_2=R_L$). It is quite clear that the I_2 current source changes the impedance that the I_1 current source sees or in another word, I_2 modulates the impedance that the I_1 sees (load modulation). By placing the quarter wave length transmission lines, increasing the I_2 reduces the impedance seen by I_1 current source. Since there are two points within the I_2 transition (from zero to the maximum) that provide the optimum impedance required by the I_1 (carrier amplifier) the overall efficiency curve has two peak points. Note that since in this analysis the maximum available currents are equal, the back off peak efficiency point is 6dB lower than the peak at the full output power. This simple analysis reveals that the symmetric Doherty amplifier improves the efficiency at 6dB PBO. Adjusting the I_2 current value into a larger levels, moves the PBO efficiency improvement point to the lower output power levels (higher PAPR values) and vice versa.
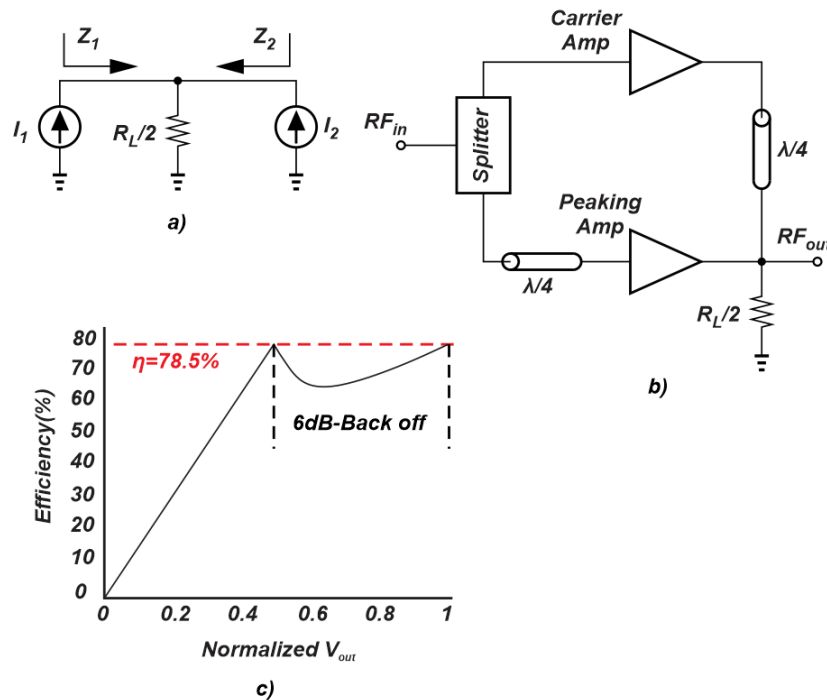
Fig. 2-3, a) Doherty load modulation basic idea, b) Doherty PA architecture, c) Doherty PA efficiency versus normalized output power

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Although the Doherty PA architecture improves the efficiency of the overall PA, since it requires transmission lines for impedance transformation, at low operating frequency this architecture is quite bulky. Therefore, the Doherty PA is not area efficient for handset mobile phones. This is why the Doherty PAs are commonly used only in base stations. In [14, 15], it has been shown that by implementing the transmission lines via lumped components, the size of the Doherty PA can be optimized for the mobile applications. Reference [16] provides a great review of the most recent Doherty PAs improvement.

2.5 Envelope Elimination and Restoration (EER)

Envelope Elimination and Restoration (EER) was introduced in [11] for the first time and is shown in Fig. 2-4. This technique splits the input RF signal into phase and amplitude via an envelope detector and a limiter. Since the phase information signal has a constant envelope this signal can be processed by a non-linear amplifier such as class-C PA. As shown, the envelope of the input signal (V_{Env}) amplifies by an amplifier and modulates the supply node of the main non-linear PA. Since the output of the non-linear PA is a direct function of the supply voltage [12], varying the supply node of the main PA with the envelope information, modulates the amplified version of the phase signal (the input to the PA). As a result, at the output node, the amplified version of the input signal delivers to the load impedance.
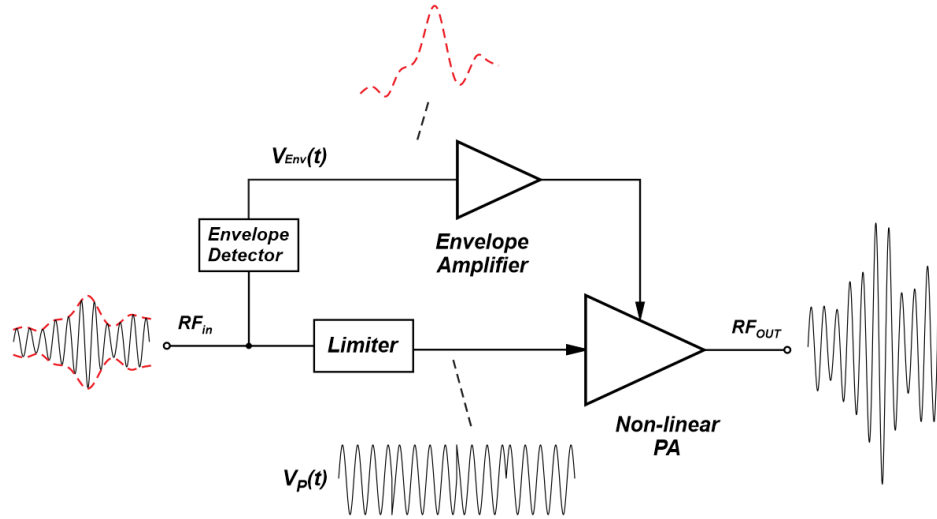
Fig. 2-4, Envelope elimination and restoration circuit diagram

One of the major disadvantages of this type of amplifier is the envelope tracking

and amplification. Since the envelope of the signal is a non-linear function of the main

input RF signal ($V_{env} = \sqrt{I^2 + Q^2}$), where I and Q are the in-phase and quadrature

components of the input signal, the bandwidth of the envelope signal is 3-4 times wider

than the bandwidth of the input signal. As a result, the envelope path, especially the

envelope amplifier, needs to be wide band. Enhancing the bandwidth of the envelope

amplifier increases the power dissipation of this block, which affects the overall

efficiency of the transmitter.

2.6   Envelope Tracking (ET)

The idea behind the envelope tracking PA, which is show in Fig. 2-5, is similar to

the EER method. The main difference between these two methods is the type of amplifier

in the transmitter. Unlike the EER, which uses non-linear PA, ET amplifier utilizes a

linear mode PA since it processes the amplitude and phase of the input signal at the same

time [4, 12]. In this technique the supply modulator changes the supply voltage of the PA

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instantaneously with the input signal envelope. As a result, the DC power dissipation of the PA reduces when low output power level is required.
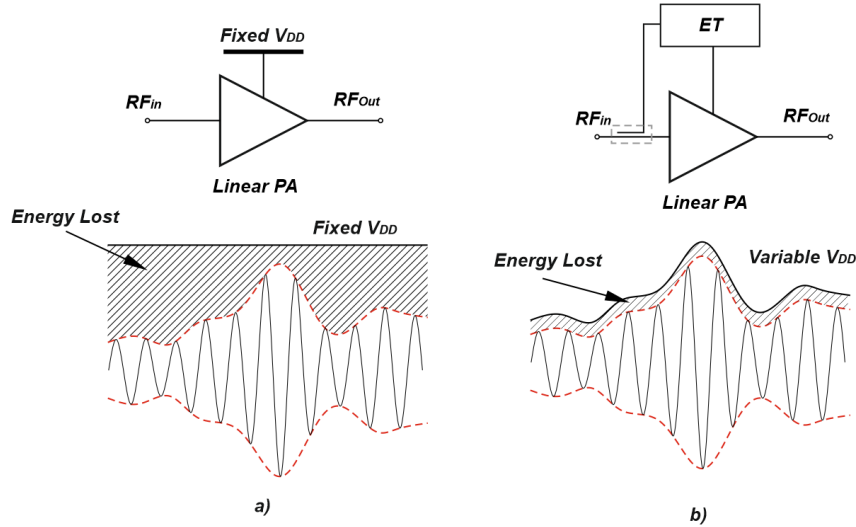
Fig. 2-5, Conventional constant supply voltage PA, variable supply voltage amplifier

Because of the maximum RF output power is a strong function of the supply voltage and the DC power dissipation is a function of transistor DC current:

$$P_{Out-max} = \frac{1}{2} \frac{(V_{DD} - V_K)^2}{R_{opt}}$$

(2-3)

$$P_{DC} = V_{DD} \times I_{DC}$$

(2-4)

where V_K is the transistor knee voltage and R_{opt} is the PA required optimum impedance, when low output power is required, in order to keep the efficiency high, the P_{DC} reduces by decreasing the V_{DD} value.

In order to modulate the supply voltage, multiple techniques have been proposed. In [17], a low drop-out (LDO) has been utilized as the supply modulator. However, due to the fact that the bandwidth of the envelope signal is 5-6 times wider than the bandwidth of the original input signal, the regulator must be quite fast to track the envelope properly. Implementing a high speed regulator makes the supply modulator

quite power hungry and reduces the overall efficiency of the transmitter. In addition, as stated in [18] the efficiency of the regulators are not high enough for high PAPR signals and as a result, utilizing the stand alone LDO or a DC-DC converter in advanced modulated RF signal is not a suitable option [19]. In [20] a class-S modulator, which is a switching supply regulator, has been used to modulate the PA supply voltage. Nevertheless, in order to reduce the ripples, high switching frequency must be utilized that increases the switching loss of the design and as a result, it degrades the overall efficiency of the transmitter. In [21-26], by combining the linear and switching supply regulators the high and low frequency signal generation is separated between the linear and switching regulators and therefore a highly efficient supply modulator has been made.

Although the ET technique increases the efficiency of the transmitter, since the envelope and the RF input signal pass through two different paths (regulator and the main PA), and the delay between them is not equal, they might experience some misalignment, delay at the main PA. In [27] it has been shown that if there is any difference/mismatch between these two paths, the amplified output spectrum is not symmetric.

In order to increase the output power in the cellular applications it is common to use compound devices such as GaN, GaAs and HBT. However, the ET modulator is commonly implemented in CMOS substrate. The difference between the materials in these two sections, lead to different processes, voltage and temperature variation that affects the overall performance. In [28] a full CMOS ET PA has been presented for 10MHz, 16-QAM and LTE application. But the supply modulator and the PA are separate chips.

2.7   Linear Amplification Using Non-linear Component (LINC)

In this technique that is presented in [13] for the first time and is shown in Fig. 2-6, non-linear circuits such as saturated or switched mode PAs have been utilized to generate the output signal. The input RF signal separates into two constant envelope signals to drive the PAs. The signal separator block basically modulates the amplitude information of the input signal into two phase modulated signals ($S_{u, p}$). Since the PAs do not need to process a variable envelope signal, they do not need to be linear. As a result, non-linear PAs that are inherently highly efficient can be utilized instead.
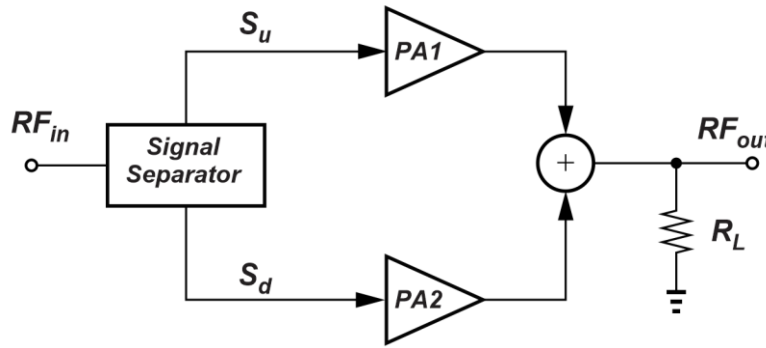
Fig. 2-6, Out-phasing amplifier system architecture

Since the PA process only the phase modulated signal, this type of implementation is known as out-phasing (OP) PA. As mentioned in [29], most challenges in the OP amplifier design are the implementation of the output power combiner and low achievable dynamic range (DR). In [30] it has been shown that DR=60dB requires the phase accuracy of about $0.1°$, which is quite difficult to achieve. In the next chapter, extensive analysis on this type of amplifier will be provided.

2.8   RF DAC-based PAs

This type of PA that is shown in Fig. 2-7 provides the ability of integrating the digital processor as well as the PA on the same chip. As reported in [31-34] the RF DACs

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are able to operate at a wide range of frequency from RF (≈1GHz) mm-wave (≈60GHz) and output power (up to 29.1dBm). Since the RF DAC structures are done in digital domain, they are inherently more efficient than the other types of aforementioned PAs. In addition, the digital implementation capability of the RF DACs make them a good candidate to operate on the same Si substrate along with the digital processing units. As a result, it is expected that this type of PA is the best candidate for the next generation of communication systems.
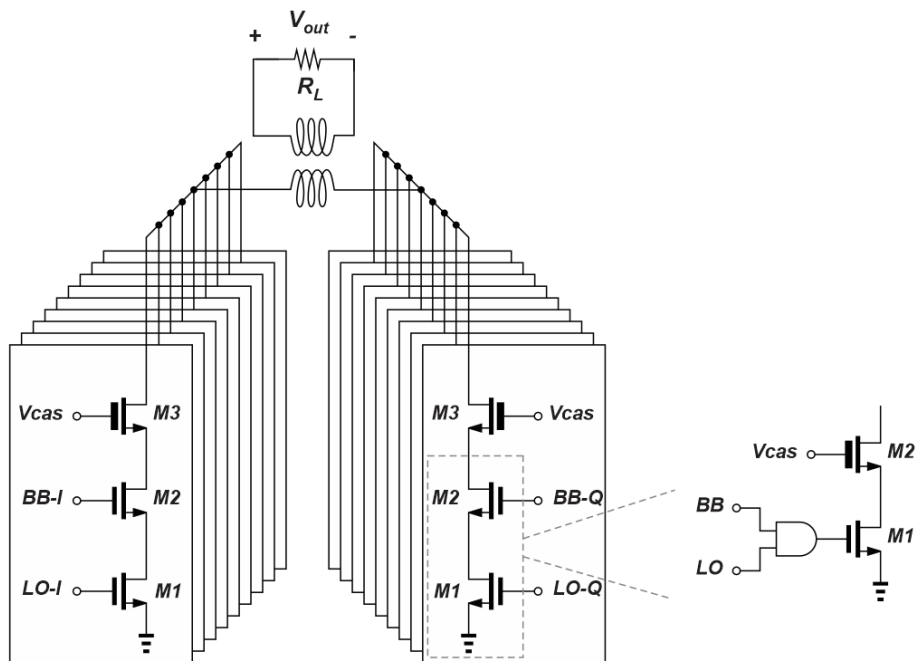
Fig. 2-7, RF-DAC overall circuit diagram

CHAPTER 3

OUT-PHASING PA

This chapter analyzes the out-phasing architecture in more detail and discusses the main challenges and solutions. A new method of power combining, which is typically the bottleneck to implementing out-phasing PAs, is presented. The proposed method is capable of reducing the physical area of the overall circuit by about 50%.

3.1 Introduction

The out-phasing amplification generates two signals with constant amplitude and differential phase (with respect to each other). The relative phase between these two signals is then used to generate the desired variable amplitude RF signal. The equations below shows the relationships between the desired output signal and required relative phase.

$$y(t) = A(t)\cos(\omega t + \varphi) \qquad (3\text{-}1)$$

$$V_1 = 1/2\, V_0 \cos(\omega t + \varphi + \theta) \qquad (3\text{-}2)$$

$$V_2 = 1/2\, V_0 \cos(\omega t + \varphi - \theta) \qquad (3\text{-}3)$$

$$y(t) = V_1 + V_2, \theta = \cos^{-1}(A(t)/V_0) \qquad (3\text{-}4)$$

In order to clarify this concept, the out of phased signals are shown as phasors in Fig. 3-1. In two extreme cases when $V_{1,2}$ are in-phase with each other the output power is at maximum and when $V_{1,2}$ have 180° phase shift with respect to each other, the output power level is minimum (theoretically zero power).
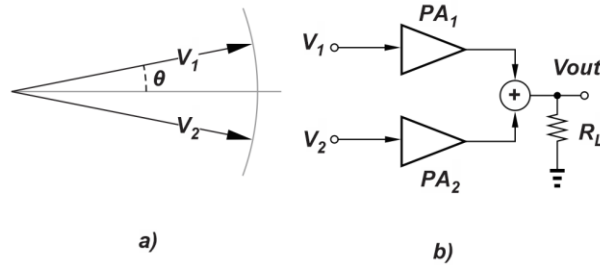
Fig. 3-1, a) Out-phasing vectors, b)out-phasing system diagram

Since the input signals do not carry any amplitude information, switched mode power amplifiers can be utilized to process the inputs ($V_{1,2}$). Because the output power level of the switched mode PAs is a direct function of the supply voltage (V_{DD}), this type of amplifier can be modeled as voltage source instead of a power source (a voltage source in series with an impedance) [35].

3.2   Power Combiner

One of the most important parts of the out-phasing amplifiers is the power combiner. Unlike in-phase power combining, a Wilkinson power combiner as shown in Fig. 3-2a is not an efficient method when the signals are out of phase. Because this type of combiner has a nulling impedance ($2Z_0$) to provide 50Ω termination at all terminals, when the signals are out of phase this resistance acts as a load to the input sources, hence increasing the power dissipation and reducing the overall PA efficiency [29, 36].Therefore, out-phasing combiners require alternative architectures. The most common type of combiner for the out-phasing transmitters is shown in Fig. 3-2b.

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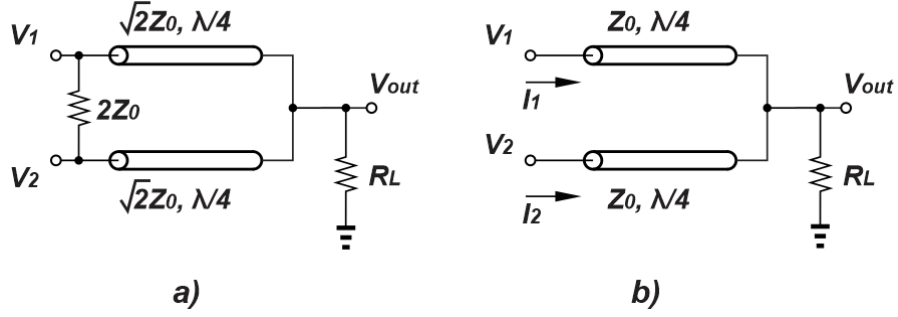
Fig. 3-2, a) Isolated power combiner (Wilkinson), b) non-isolated power combiner

This combiner is implemented by removing the nulling impedance in Wilkinson power combiners and modifying the characteristic impedance of the transmission lines (T-lines) [29, 36-38].

One of the challenges associated with this type of combiner is that unlike a Wilkinson power combiner, the input impedances are not fixed and vary as a function of out-phasing angle. The ABCD matrix and the relationships between the input current and voltage at the input ports of the combiner are calculated as:

$$ABCD = \begin{bmatrix} cos\beta L & jZ_o sin\beta L \\ j/Z_o\, sin\beta L & cos\beta L \end{bmatrix} \qquad (3\text{-}5)$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ j/Z_o & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \qquad (3\text{-}6)$$

$$\begin{bmatrix} V_o e^{j\theta} \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ j/Z_o & 0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_1' \end{bmatrix}$$

$$\qquad (3\text{-}7)$$

$$\begin{bmatrix} V_o e^{-j\theta} \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ j/Z_o & 0 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_2' \end{bmatrix}$$

where Z_o is the T-line characteristic impedance, $I_{1,\,2}$ are the currents injecting from the input voltage sources and $I'_{1,2}$ are the currents coming out of the T-lines.

$$I_1' = V_o e^{j\theta}, I_2' = V_o e^{-j\theta} \qquad (3\text{-}8)$$

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$$V_{out} = R_L(I_1' + I_2') = \frac{2R_L V_o \cos\theta}{jZ_o} \tag{3-9}$$

$$I_{1,2} = j/Z_o V_{out} = \frac{2R_L V_o \cos\theta}{Z_o^2} \tag{3-10}$$

$$Y_{eff1} = \frac{I_1}{V_1} = \frac{2R_L V_o \cos\theta}{Z_o^2(\cos\theta + j\sin\theta)}$$

$$Y_{eff2} = \frac{I_2}{V_2} = \frac{2R_L V_o \cos\theta}{Z_o^2(\cos\theta - j\sin\theta)}$$

$$Y_{eff1} = \frac{2R_L}{Z_o^2}\cos^2\theta - j\frac{R_L}{Z_o^2}\sin 2\theta \tag{3-11}$$

$$Y_{eff2} = \frac{2R_L}{Z_o^2}\cos^2\theta + j\frac{R_L}{Z_o^2}\sin 2\theta$$

$$P_{out} = \frac{2V_o^2 \cos^2\theta}{Z_o^2/R_L} \tag{3-12}$$

$$Y_{eff1-Comp} = \frac{2R_L}{Z_o^2}\cos^2\theta - j\frac{R_L}{Z_o^2}\sin 2\theta + j\omega C \tag{3-13}$$

$$Y_{eff2-Comp} = \frac{2R_L}{Z_o^2}\cos^2\theta + j\frac{R_L}{Z_o^2}\sin 2\theta + \frac{1}{j\omega L} \tag{3-14}$$

As can be seen, the output power has a direct relationship with the out-phasing angle. It is quite clear that the real parts of the effective input admittances are the same and as a result, the real power generated by the PAs are the same. But, PAs also see imaginary components and therefore, some reactive power generates and degrades the efficiency of the overall system. In order to improve the efficiency, the imaginary terms must be removed from the input admittances. A common method of doing this is to put compensation components (capacitor and inductor) in parallel with the input ports. Fig. 3-3a shows the implementation of the out-phasing compensation. Since impedance compensation happens at a specific out-phasing angle, the effective input admittances

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cross the real axis (on the smith chart) twice. Fig. 3-3b shows the variation of the effective input admittances as a function of the out-phasing angle on the smith chart. Since the required capacitor and inductor admittance values to cancel the imaginary parts are frequency dependent, the compensation is sensitive to the frequency. This figure shows the simulation result of the effective input impedances at the input of the combiner at 2.4GHz. In this simulation the L_c=4.9nH, C_c=0.9pF.
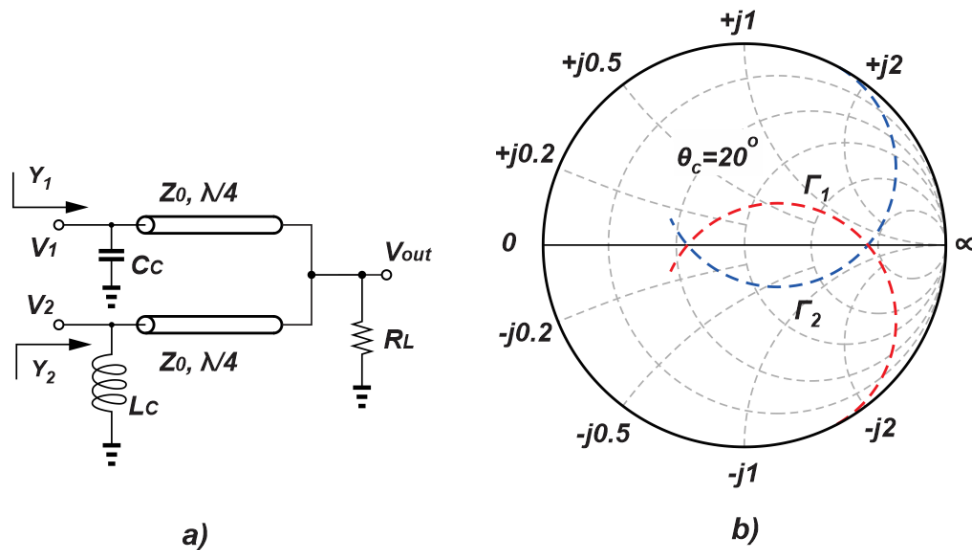
Fig. 3-3, a) Out-phasing non-isolating power combiner, b) effective reflection coefficients at ports $V_{1,2}$

Although implementing the out-phasing PA is quite straight forward, using T-line structures at cellular frequencies (2.4-5GHz) requires board level implementation since implementing the T-lines requires a large area (L=λ/4). Therefore, another more integrated method of combining is required to realize small form-factor PAs.

3.3 Power Combining Using Transformers

Since the out-phasing technique is based on summing the voltages, transformers can be utilized. Unlike the T-lines, transformer-based combiners relax the physical implementation limitation in cellular frequency. As explained in [39] and shown in Fig.

3-4, transformer-based combiners cover a wide range of frequency from sub GHz up to

mm-wave applications. Fig. 3-5 shows two of the most common circuit diagrams of

combiner implementation using transformers.
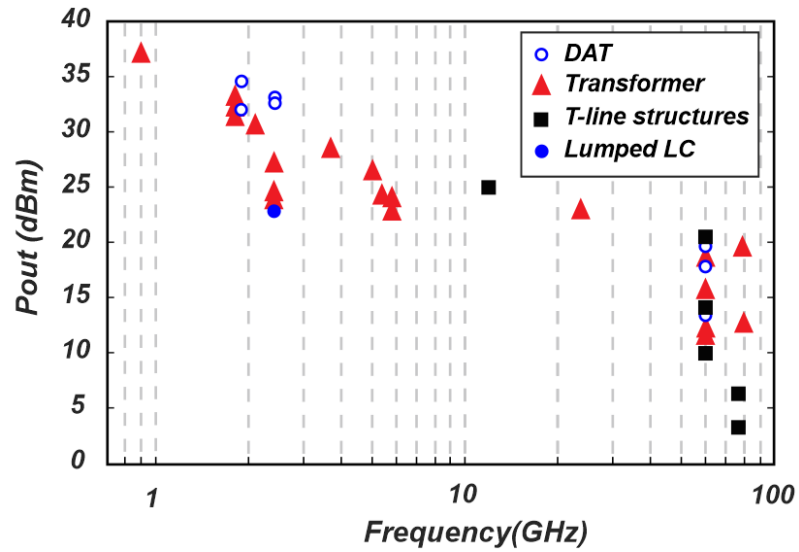
Fig. 3-4, Output power versus frequency for most common power combiners
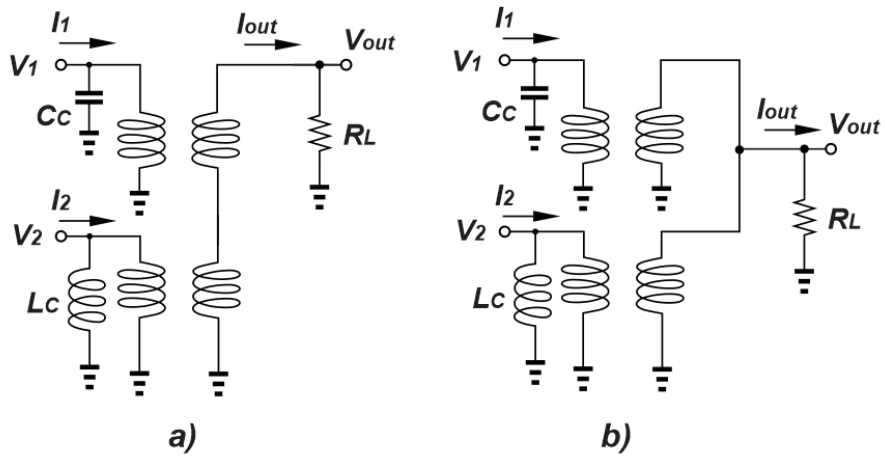
Fig. 3-5, a) Series architecture of transformer combiner, b) parallel architecture of transformer combiner

Considering the 1:1 transformer ratio for simplicity in Fig. 3-5a, the output

voltage and effective input impedance with and without the compensation components

can be written as:

$$V_{out} = V_1 + V_2 = 2V_o cos\theta \qquad (3\text{-}15)$$

$$I_{out} = V_{out}/R_L = \frac{2V_o cos\theta}{R_L} = I_{1,2} \qquad (3\text{-}16)$$

$$Y_{eff1} = I_1/V_1 = \frac{2}{R_L}\left(cos^2\theta - j\frac{1}{2}sin2\theta\right) \qquad (3\text{-}17)$$

$$Y_{eff2} = I_2/V_2 = \frac{2}{R_L}\left(cos^2\theta + j\frac{1}{2}sin2\theta\right) \qquad (3\text{-}18)$$

$$Y_{eff1-Comp} = I_1/V_1 = \frac{2}{R_L}\left(cos^2\theta - j\frac{1}{2}sin2\theta\right) + j\omega C \qquad (3\text{-}19)$$

$$Y_{eff2-Comp} = I_2/V_2 = \frac{2}{R_L}\left(cos^2\theta + j\frac{1}{2}sin2\theta\right) + \frac{1}{j\omega L} \qquad (3\text{-}20)$$

where $I_{1,2}$ are the input currents coming from the voltage sources and I_{out} is the load current. As can be seen, the effective input admittances seen by the input sources have imaginary parts and in order to enhance the overall efficiency, the parallel capacitor and inductor must be placed at the input of the primary coils of the transformers.

Due to the inductive nature of the actual transformers, in practical implementation only capacitors are being used to provide compensation. In [40], a transformer-based out-phasing transmitter at 5.9GHz has been implemented that consumes only 0.8mm^2 of area. This implementation achieved 22.2dBm of output power and almost 35% of drain efficiency.

In [41, 42], it has been shown that instead of implementing the actual transformer, bond wires can be utilized to mimic the behavior of the transformer to save the area. This structure is shown in Fig. 3-6. Nevertheless, the coupling factor in this case highly depends on the shape of the bondwires and the positions of them with respect to each other. As a result, this type of implementation is quite sensitive compared to the on-chip integration of the transformers.
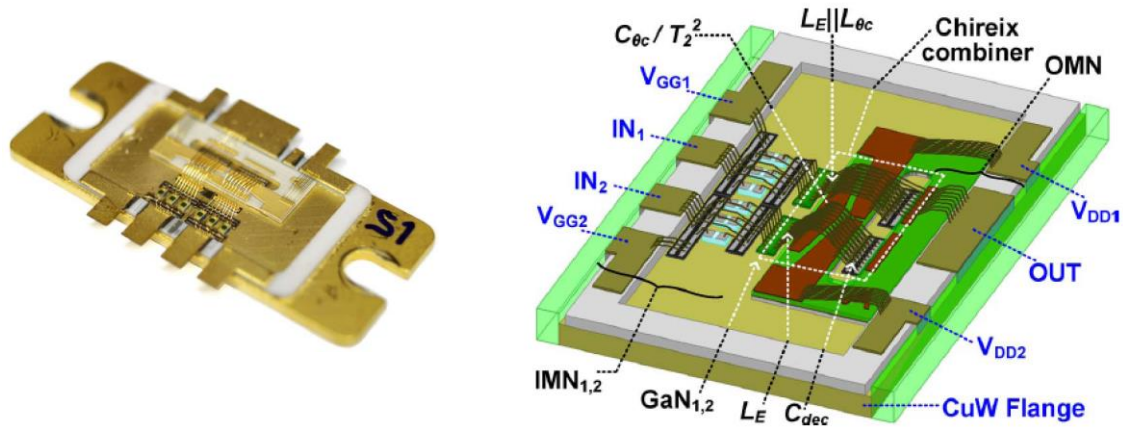
Fig. 3-6, Power combiner implementation using the package bondwires

Instead of combing the RF signals in voltage domain, transformers can be arranged such that the signals add in current domain [6, 43]. Fig. 3-7 shows the circuit diagram of this architecture. Unlike voltage combining, adding the signals in current domain can reduce the area significantly since the transformer coils can be placed in parallel with each other by stacking them on top of one another. However, due to the CMOS process limitations such as number of available routing layers and the maximum thickness of each metal layer, creating more than 2 transformers is not practical.
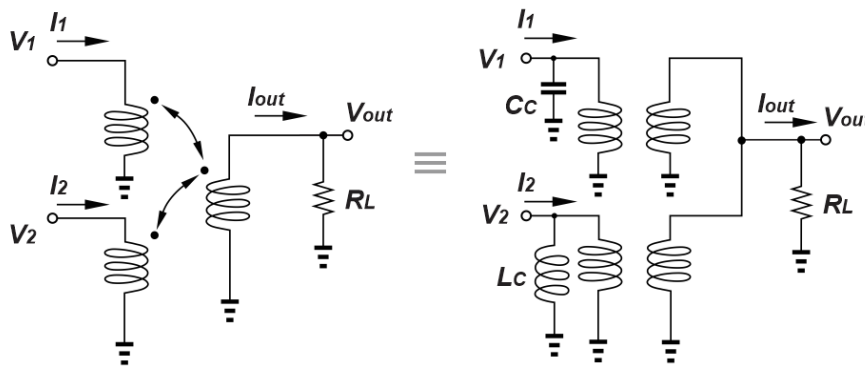
Fig. 3-7, Parallel architecture of transformer combiner

Although combining the powers in current domain is quite efficient in terms of area, this method of integration is applicable only to in-phase combining. As shown in

Fig. 3-7, the transformers' basic equations enforce the output voltage (V_{out}) to be in-phase with the signals at the primary coils (A requirement that does not satisfy the out-phasing nature since at the inputs the signals have different phases). Therefore, the parallel combining is not a practical solution in out-phasing systems.

3.4   Proposed Power Combining Technique

In order to take advantage of the current and voltage combining properties, the transformer implementation that is proposed in [43] has been used. Utilizing the series-parallel configuration conventionally has been proposed only for in-phase power combining and it shows some benefits over series and parallel combining such as: low form factor (almost 50%), less sensitivity in the efficiency (compare to pure series or parallel implementation) and high mutual coupling between the adjacent primary coils that enhances the efficiency. In order to visualize the structure of this combiner, Fig. 3-8 illustrates the layout view of the transformers.
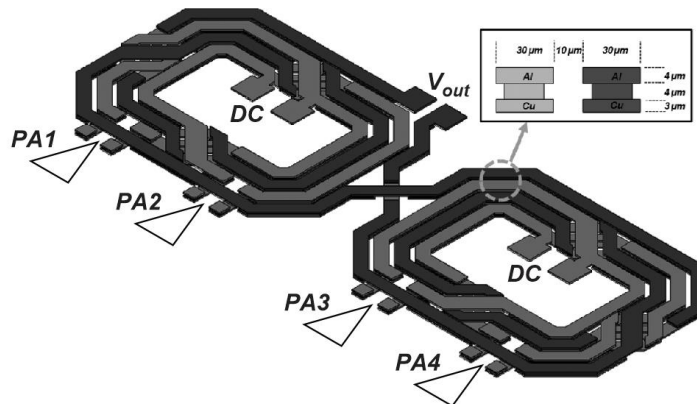
Fig. 3-8, Parallel-series combiner layout architecture

In this implementation most of the routing is done on the top most metal layer (Al) to reduce the routing resistance. Fig. 3-9 compares the efficiencies of the series, parallel and the proposed PSCT. As illustrated, the efficiency of the PSCT is between the other types of combiner. Another important parameter that is commonly being used in

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transformer comparison is the power transmission ratio (PTR). This parameter indicates how efficiently the transformer is incorporated with parallel PA cores but does not reflect the efficiency of the transformer [43].

$$PTR = M\eta(1 - |\Gamma|) \tag{3-21}$$

where M is the number of transformers in parallel with each other, η is the efficiency of each transformer and Γ is the reflection coefficient at the input terminal.
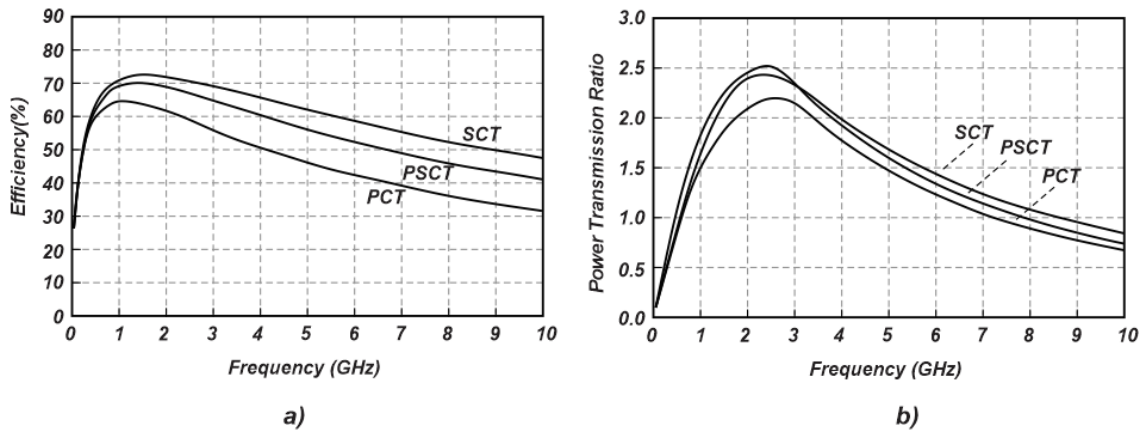
Fig. 3-9, a) Efficiency comparison between SCT, PCT and PSCT, b) power transmission ratio comparison between SCT, PCT and PSCT

Due to the advantages of the PSCT over the other conventional transformer combiners, this research proposes to use this combiner in the out-phasing transmitter. This configuration is illustrated in Fig. 3-10a. Since most of the CMOS processes provide 2 thick metal layers, only two transformers have been placed at each input port (M=2). Because the input signals at each port are in phase with each other, parallel combining is practical. Finally, in order to sum the out-phased signals, series combining has been utilized at the secondaries of the transformers. The simulation result, which is done at 5GHz with L_c=5nH and C_c=200fF with R_L=50Ω and shown in Fig. 3-10b, reveals that the input effective reflection coefficients seen from each input port behave similarly to the conventional out-phasing structure and cross the real axis on the smith chart twice. Note

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that for this simulation the compensation angle is set to $\theta_c=20°$, which is a common value

in most of the communication applications.
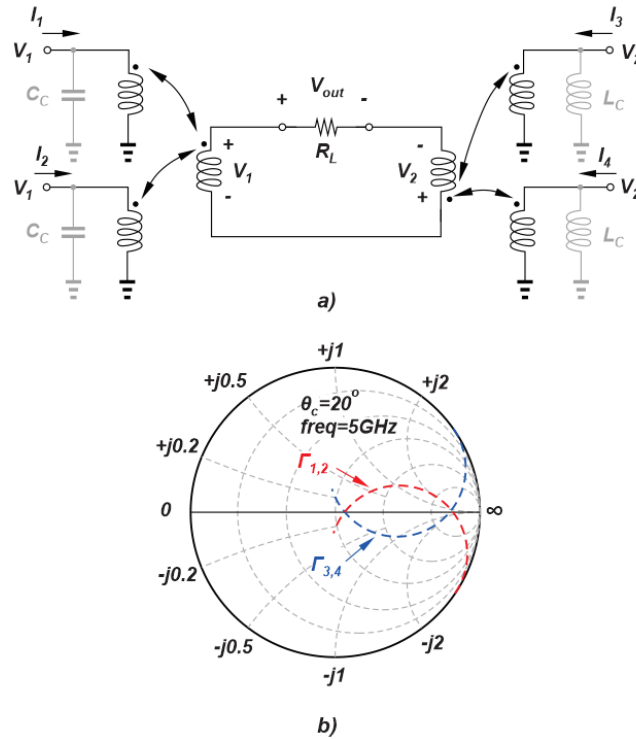
Fig. 3-10, a) circuit diagram of the PSCT for out-phasing architecture, b) the effective reflection coefficient at the input ports of the combiner (compensation at 20°)

Since two transformers have been placed at the input ports instead of one, 3dB

more power can be achieved with this arrangement. In addition, compared to the putting

of 4 transformers in series with each other, the proposed configuration consumes 50%

less area than the conventional implementation methods.

3.5 Out-phasing Transmitter Challenges

One of the main issues associated with the out-phasing transmitters reveals when

a low output power level is desired at the output. Since it is quite difficult to generate two

out-phased vectors to cancel out each other completely, the dynamic range (DR) of the

system is limited by the phase accuracy of the transmitter. In [30] it has been shown that

in order to meet 60dB of DR, the phase error should be controlled by 0.1º that requires

10-bit DAC resolution, which of course has a quite challenging implementation.

In order to increase the DR of the system and generate low output power levels

easily, [29, 37, 38] proposed combining the linear amplification and out-phasing

techniques, which is called mixed-mode out-phasing. When the output power level is

close to the maximum, out-phasing technique is being used to enhance the efficiency and

when low output power level is of interest, the linear amplification is used to reduce the

output power. As a result, instead of using pure switched mode PAs such as class E and

E^{-1}, saturated linear PAs must be utilized. Fig. 3-11 graphically shows how this technique

operates.
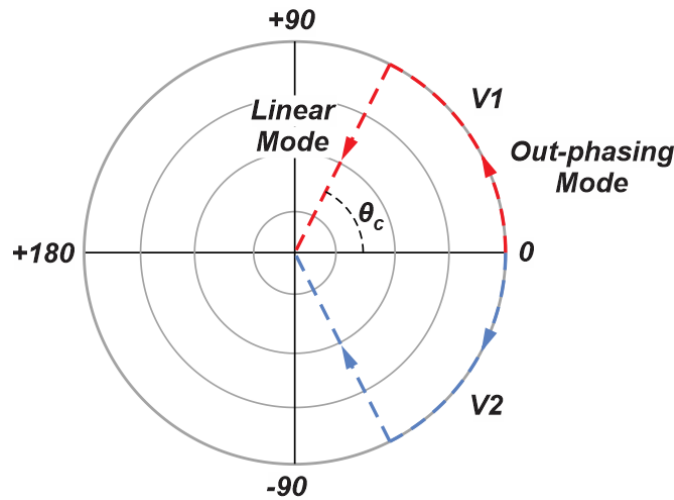
Fig. 3-11, Mixed mode (out-phasing and linear) vector description

The other critical challenge that the out-phasing amplifier has is the amount of

power generated by the PAs at low output power levels. Since the power generated by the

switched mode PAs are fixed, if low output power level is required, the energy generated

by the PAs should dissipate somehow (one PA acts as a load of the other PA), which is

completely in oppisition of the efficiency enhancement idea.

3.6   State of the Art Analysis

Although combining two out-phased signals improves the overall efficiency of the power amplifier, in [44], a new power combining technique in the out-phasing TX has been proposed, which is called 4-way out-phasing, and is based on generating 4 vectors instead of 2 vectors. Fig. 3-12a conceptually illustrates the concept of 4-way out-phasing. As shown in Fig. 3-12b it is quite clear that the variation of the effective input impedances of the 4-way out-phasing is less than the conventional 2-way out-phasing on the smith chart. The 4-way out-phasing technique, by keeping the effective reflection coefficients close to the horizontal axis, reduces the total reactive power generation. Therefore, the overall efficiency of the out-phasing PA increases. In order to compare the performance of these two types of out-phasing PAs the power factor (PF) has been used that is defined as:

$$K_p = \frac{Re(Y_{eff})}{|Y_{eff}|} \tag{3-22}$$
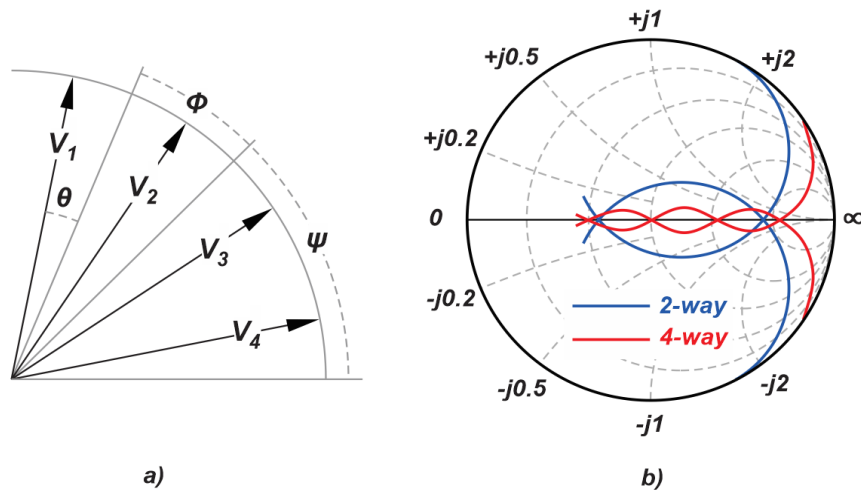
Fig. 3-12, a) 4-way outphasing vector diagram, b) comparison between the conventional 2-way and 4-way effective reflection coefficients

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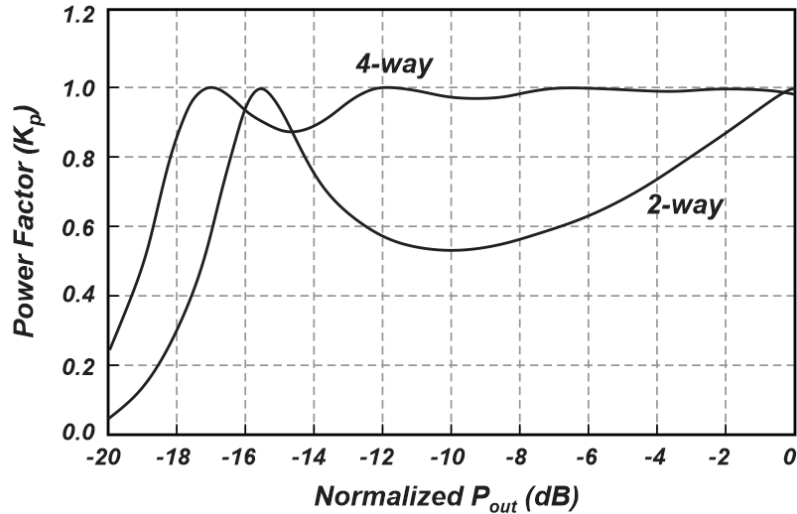
Fig. 3-13, Comparison between the power factors (K_p) of 2-way and 4-way out-phasing

As shown in Fig. 3-13, the PF of the 2-way and 4-way out-phasing touches the

$K_p=1$ twice and 4 times respectively. Also, it is quite clear that the 4-way out-phasing,

compared to the conventional 2-way, reduces the power factor variation significantly. In

[45-48] multiple methods of implementation of 4-way out-phasing such as lumped

component, T-line with lumped component and T-line utilizing radial stubs have been

proposed. Although implementing the 4-way out-phasing PA improves the efficiency of

the transmitter, it has two main challenges: 1) generating the phase between the vectors

and 2) shrinking the size of the combiner.

The phase difference between the out-phased vectors must be set accurately.

Otherwise, the desired performance deviates from the desired values. In [44] the reverse

implementation of the output combiner has been used as the input signal separator.

Nevertheless, it increases the size of the overall transmitter board and makes it quite area

inefficient. In order to reduce the size of the signal separator, [49, 50] proposed a

technique to generate the 4 out-phased vectors with accurate phase difference. This

technique is based on implementing the non-linear network whose impedance is a function of the input voltage value.

Implementing the power combiner via the methods presented in [45-48] makes the design quite bulky and completely area inefficient, especially for CMOS fabrications in telecommunication frequency. Reference [39] investigated the transformer-based implementation of the 4-way out-phasing. By considering the out-phasing vectors as:

$$V_1 = V_0 e^{+j\varphi} e^{+j\theta} \tag{3-23}$$

$$V_2 = V_0 e^{+j\varphi} e^{-j\theta} \tag{3-24}$$

$$V_3 = V_0 e^{-j\varphi} e^{+j\theta} \tag{3-25}$$

$$V_4 = V_0 e^{-j\varphi} e^{-j\theta} \tag{3-26}$$

where V_0 is the fixed output vector, it can be seen that the output voltage is the summation of all of these vectors ($V_{out} = \sum_{i=1}^{4} V_i$). This summation can be simply implemented via series combination of 4 transformers as shown in Fig. 3-14.
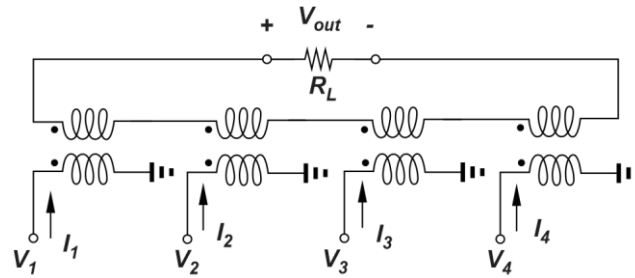
Fig. 3-14, Series transformer combiner implementation for 4-way out-phasing

Although the series combination of the transformers can make the desired output vector, the effective input impedances/admittances must satisfy the PA outputs. As an example, the input admittances of the first and second ports are calculated:

$$Y_1 = \begin{cases} Re = \dfrac{4}{R_L}\left(cos^2\varphi cos^2\theta - \dfrac{1}{4}sin2\varphi sin2\theta\right) \\ Im = \dfrac{-4}{R_L}\left(\dfrac{1}{2}cos^2\varphi sin2\theta + \dfrac{1}{2}sin2\varphi cos^2\theta\right) \end{cases} \quad (3\text{-}27)$$

$$Y_2 = \begin{cases} Re = \dfrac{4}{R_L}\left(cos^2\varphi cos^2\theta + \dfrac{1}{4}sin2\varphi sin2\theta\right) \\ Im = \dfrac{-4}{R_L}\left(\dfrac{1}{2}sin2\varphi cos^2\theta - \dfrac{1}{2}cos^2\varphi sin2\theta\right) \end{cases} \quad (3\text{-}28)$$

where R_L is the output load of the combiner. As shown in this equation and mentioned in

[39], in order to generate an equal amount of power at each PA port, the real parts of the

admittances should be equal. In addition, the stability requirement forces the real parts to

be positive at each PA output terminal for all output power levels. These criterion limit

the out-phasing angle selection and as mentioned in [39] the summation of the out-

phasing angles ($\varphi+\theta$) must be less than $\pi/2$ in order to keep the resistive input

admittances positive. Therefore, in order to design the output combiner for the out-

phasing transmitter not only the output vector must be set correctly, the combiner

structure must be compatible with the PA requirements.

3.7   Conclusion

In this chapter, one of the PA efficiency enhancement techniques has been

introduced and analyzed. It has been shown that the transformer based power combiner is

one of the most popular ways of combining, especially in CMOS processes. A new

implementation technique has been introduced to increase the output power level by the

factor of 2 and reduce the area by the same amount. The state of the art implementation is

explained and showed that the conventional transformer power combiner is not a

promising implementation for 4-way power combiner.

CHAPTER 4

AVERAGE POWER TRACKING

4.1   Introduction

The importance of amplifier design in CMOS process is well discussed in [51-53]. In this chapter, a new method of efficiency enhancement technique that uses average power tracking (APT) is proposed. In addition, the proposed technique has been implemented via a custom made metal-semiconductor field effect transistor (MESFET) to generate watt-level output power in CMOS processes. Furthermore, unlike the conventional envelope tracking technique that utilizes the CMOC process for implementing the supply regulator and GaN, GaAs or HBT devices as the PA, both the power amplifier and supply modulator are integrated on the same substrate.

4.2   Average Power Tracking vs. Envelope Tracking

As we know, the power dissipation of the PA is a function of average current pulls from the supply multiplied by the V_{DD} and the RF power generated by the PA is a function of the fundamental current at the drain of the transistor. As an example, a linear PA that is biased in class B and is shown in Fig. 4-1 has been analyzed. Because the transistor gate in this class of operation is biased at the threshold voltage, any voltage that exceeds the threshold voltage at the gate of the transistor turns it on and generates current at the drain. By considering the sample wave forms shown in Fig. 4-2, the average and fundamental currents can be calculated as:
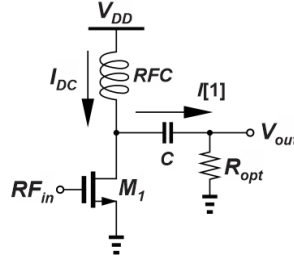
Fig. 4-1, A sample PA circuit diagram
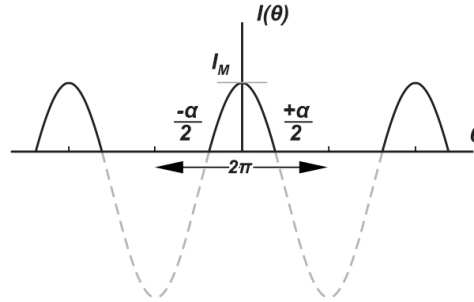
Fig. 4-2, A sample semi-sinusoidal wave form

$$I(\theta) = I_P \cos\theta + I_{DC}, I(0) = I_m, \left(\frac{\alpha}{2}\right) = 0 \tag{4-1}$$

$$I(\theta) = \frac{I_m}{1 - \cos\frac{\alpha}{2}}(\cos\theta - \cos\frac{\alpha}{2}) \tag{4-2}$$

$$I_{DC} = \frac{I_m}{2\pi(1 - \cos\alpha/2)}(2\sin\alpha/2 - \alpha\cos\alpha/2) \tag{4-3}$$

$$I[1] = \frac{I_m}{\pi(1 - \cos\alpha/2)}(\alpha/2 - \frac{1}{2}\sin\alpha) \tag{4-4}$$

$$@ \alpha = \pi, \qquad I_{DC} = \frac{I_m}{\pi}, \quad I[1] = \frac{I_m}{2} \tag{4-5}$$

$$P_{DC} = V_{DD} \times I_{DC} = \frac{V_{DD} \times I_m}{\pi} \tag{4-6}$$

$$P[1] = \frac{1}{2}R_{opt}I^2[1] \tag{4-7}$$

where I_P is the peak value of the sine wave, I_{DC} is the DC level of the sine wave current,

I_m is the maximum of the output current, θ is the angular frequency and R_{opt} is the

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optimum impedance the PA requires to generate the maximum power. This impedance can be easily calculated by dividing the maximum voltage variation on the drain of the transistor by the maximum drain current variation. This analysis is shown graphically in Fig. 4-3b.
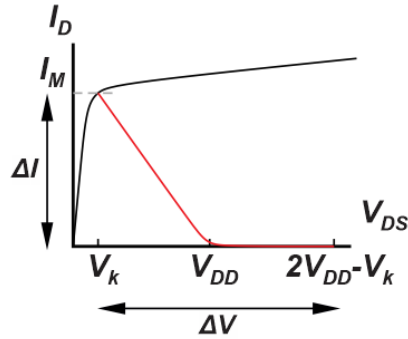
Fig. 4-3, Variation of I_D and V_{DS} of the transistor

By considering the I-V characteristic shown in Fig. 4-3, the output power and efficiency of the PA can be calculated as:

$$R_{opt} \sim \frac{2V_{DD}}{I_m} \tag{4-8}$$

$$P[1] = \frac{1}{2}\frac{2V_{DD}}{I_m}\left(\frac{I_m}{2}\right)^2 \tag{4-9}$$

$$Eff = \frac{P[1]}{P_{DC}} \sim \frac{\pi}{4} = 78\% \tag{4-10}$$

This simple analysis reveals that in order to increase the efficiency of the PA, the average current pulling from the supply must be as low as possible, while maintaining the fundamental output power high enough, according to the specifications required by the RF standard. On the other hand, since the DC power dissipation of the PA is a function of supply voltage, reducing the supply voltage when the required output power is not at the maximum enhances the overall efficiency of the PA. This technique is shown graphically in Fig. 4-4.

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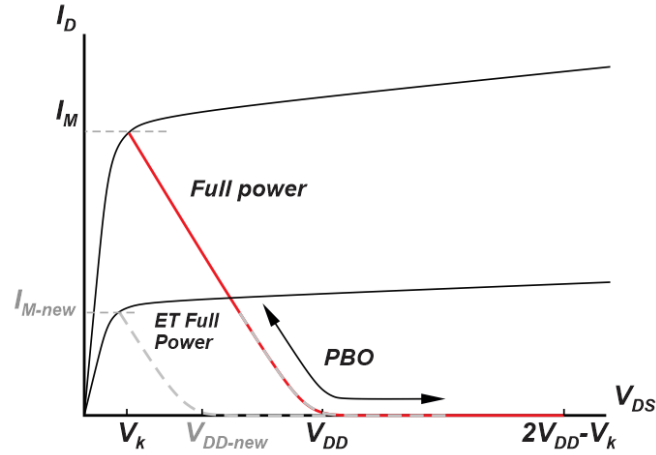
Fig. 4-4, Full power I_D-V_{DS} movement at full power, power back off (PBO) and when ET is applied

When the maximum output power is desired (red curve), the supply voltage is set to the maximum to generate the maximum power. However, when the output power is at lower values (dashed gray curve), there is no need to keep the supply voltage at the previous value and it can reduce to lower values while maintaining the same R_{opt} for the PA. Although this analysis has been done only for the Class-B PA, it can be applied to any standalone linear PAs.

Since the output power level changes over time, the supply regulator must operate fast enough to provide the required value. Also, since the envelope of the signal $A(t) = \sqrt{I^2(t) + Q^2(t)}$ is a non-linear function of the input signal the regulator must respond quickly in order to provide the correct supply voltage value. If there is any phase difference between the actual RF input and the envelope information, additional non-ideality will add to the output signal that degrades the quality (adding AM-AM and AM-PM distortion) of the output signal [27].

Because real time envelope tracking requires high speed in the control circuitry and consumes significant amount of power, another type of tracking, which is called average power tracking (APT), is being used [54-57]. In this technique, the average of the

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input RF signal is tracked, and the supply voltage varies based on that. In order to have a better sense of how this technique works, Fig. 4-5 shows the behavior of the supply voltage for three possible options.
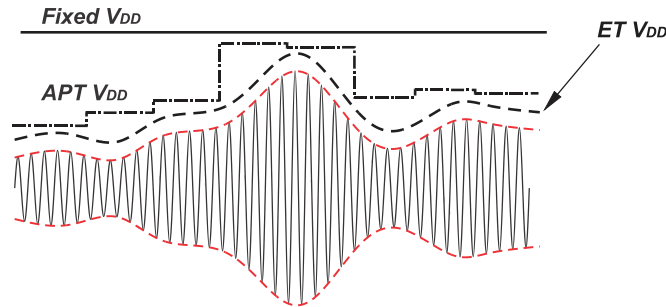
Fig. 4-5, Comparison between the fixed supply voltage, average power tracking and envelope tracking

As can be seen, the signal variation (speed) of APT is between the fixed V_{DD} and ET V_{DD} options. As a result, the circuit complexity of the APT is more relaxed compared to the ET method from the speed perspective requirement. The comparison between the power dissipations of ET and PAT in the form of thermal dissipation are shown in Fig. 4-6. It is quite clear that in ET less heat is generated on the PA compared to the APT, while the Tracker in ET has higher temperature compared to APT.
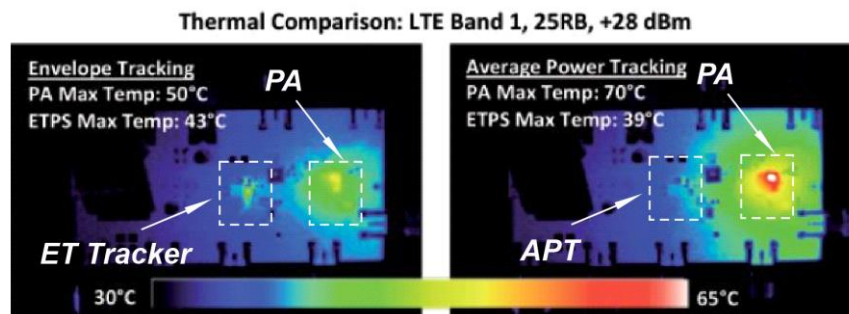
Fig. 4-6, Comparison between the thermal generation of envelope tracking and average power tracking

4.3 Proposed Technique and Design

Since the nominal voltage level in advanced CMOS technologies is going toward sub 1V, while at the same time the required output power level for handset applications is

fixed (27dBm to 33dBm), implementing the voltage supply regulator under this condition is quite challenging. Therefore, a novel idea to implement the APT in current domain has been proposed. Fig. 4-7 compares the conventional and the proposed methods.
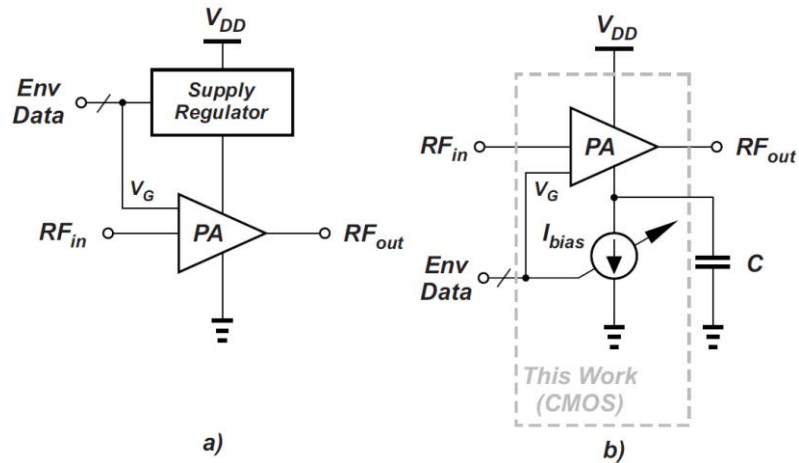
Fig. 4-7, a) conventional envelope tracking technique, b) the proposed power tracking architecture

As can be seen, unlike the conventional ET method, the envelope information in the proposed technique (Fig. 4-7b) is used to adjust the DC current level of the main power amplifier. Since the CMOS process does not have any limitation on the current level, the proposed method can be applied in any CMOS technology. In addition, since the tracker is not connected to high voltage levels, no voltage protection such as cascoding or utilizing thick gate oxide transistors are required.

As a proof of concept, this design has been implemented in the 45nm CMOS SOI process with V_{DD}=0.9V. As shown in Fig. 4-8, the adjustable current source (in Fig. 4-7b) is implemented via a 4-bit current steering digital to analog converter (DAC). The DAC is controlled by 4 control bits to generate 16 different states. Based on the previous measurement results [58, 59], the maximum DC current that the PA requires for proper operation is I_Q=500mA. As a result, the DAC has been designed to provide I_D=0.5A.

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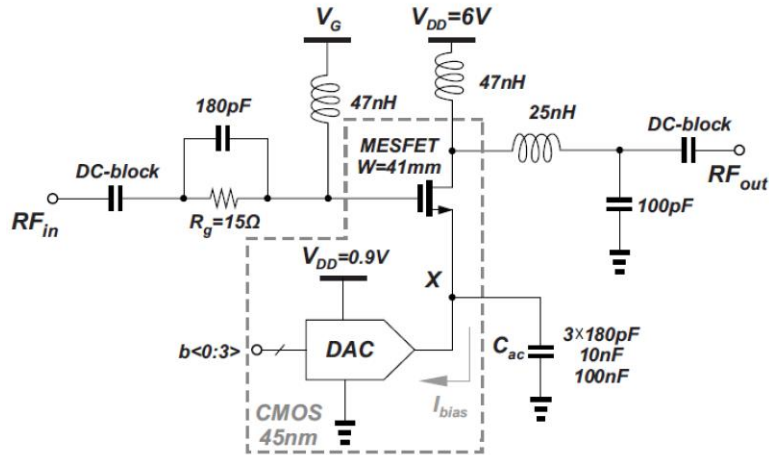
Fig. 4-8, Proposed architecture circuit diagram

The structure of the DAC is shown in Fig. 4-9. The DAC consists of multiple current mirror stages to increase the current level gradually. In order to have control over the main current generator, instead of implementing the bandgap reference (BGR) on the chip, an external biasing resistance is placed off-chip. Since the I_Q=500mA is required, each of the branches in the last stage needs to provide 1/16 of the total current (I_{branch}=26mA). The current in each branch is controlled by a NMOS switch. To control the switches with only 4 input control bits, a 4 to16 bit encoder has been designed.
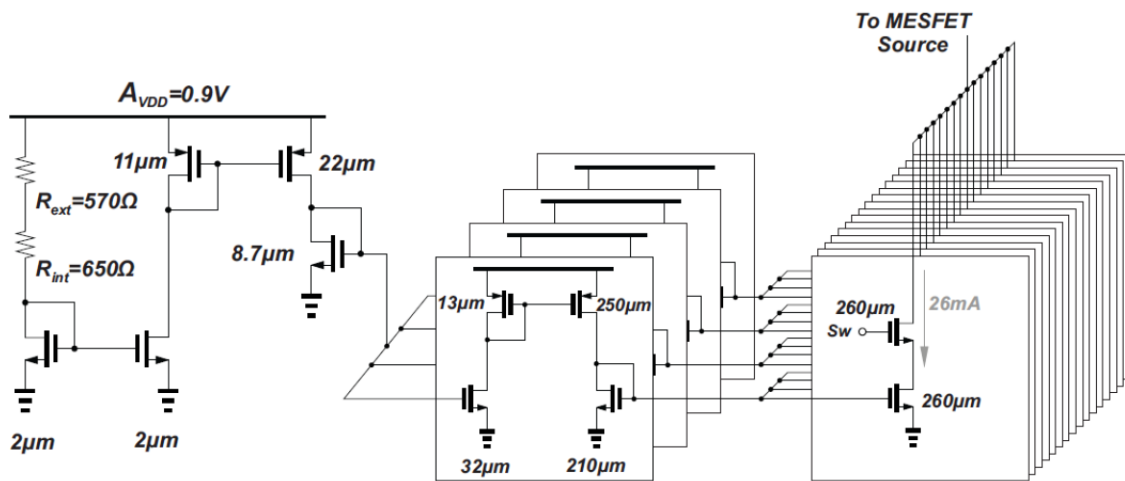
Fig. 4-9, The digital to analog converter (DAC) circuit diagram

Since providing high output power level requires high output current as well as voltage swing, the PA main transistor must be able to tolerate high voltage levels (in the order of 6-7V) in order to provide wall-level output power. Because the main purpose of this design is not to use power combining techniques, such as the transformer based combiner [39, 60], a custom made silicon-based transistor that can tolerate up to 12V in CMOS SOI process has been utilized.

4.4 Metal-Semiconductor Field Effect Transistor (MESFET)

Unlike the metal oxide semiconductor field effect transistors (MOSFETs), metal-semiconductor field effect transistors (MESFETs) do not have the oxide layer underneath the gate polysilicon. Therefore, all the limitations associated with this oxide layer, such as parasitic capacitances and break down voltages, are removed. As a result, the maximum allowable voltage across the gate-drain and gate-source is higher than a MOSFET counterpart. Fig. 4-10 shows the structure of the MESFET transistor [58, 59, 61-63].
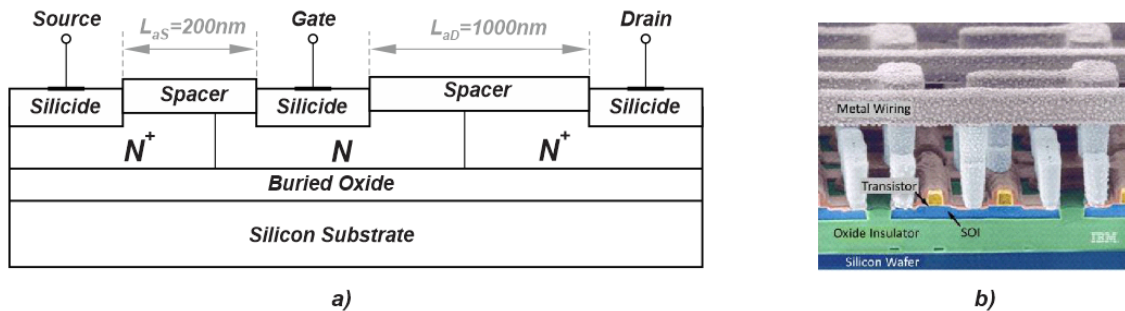
Fig. 4-10, a) MESFET transistor device configuration b) 3D view of the actual device

As can be seen, there is no oxide layer underneath the gate and there is direct contact between the metal on the gate and the semiconductor. The direct connection between the gate metal and the semiconductor creates a Schottky diode on the gate of the transistor. In Fig. 4-10a the L_{aS} and L_{aD} are the distances between the gate and source and

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drain terminals respectively. These two parameters determine the important parameters of

the transistor, such as the break down voltage (V_{BR}) and the cross over frequency (f_t). In

[58], it has been shown that by increasing the L_{aS} and L_{aD} the break down voltage

increases and the f_t decreases. Table. 4-1 shows the performance of a MESFET transistor

for different L_{as} and L_{aD}.

Table. 4-1, Properties of the MESFET under different gate-drain and gate-source distances

Parameter	L_{aS} and L_{aD} = 500nm	L_{aS} and L_{aD} = 1000nm	L_{aS} and L_{aD} = 2000nm
Gate oxide	No Gate Oxide	No Gate Oxide	No Gate Oxide
L_g (nm)	200	200	200
L_{aS}/L_{aD} (nm)	500	1000	2000
W_{finger} (µm)	15	15	15
V_{BD} (V)	15	21	28
f_T (GHz)	24	17.5	9
f_{MAX} (GHz)	35	25	20
V_T (V)	-0.5	-0.5	-0.5

The I_D-V_{DS} plot of the transistor is shown in Fig. 4-11. As can be seen, the

maximum tolerable voltage on the drain is about 17V, which is quite larger than the

maximum available nominal voltage in the 45nm CMOS SOI process ($V_{DD\text{-}nom}$=0.9V). It

must be noted that unlike MOSFET transistors that have hard break down, MESFET

shows soft breakdown behavior at high drain voltage values (the current increases

gradually at high V_d values instead of sharp behavior).

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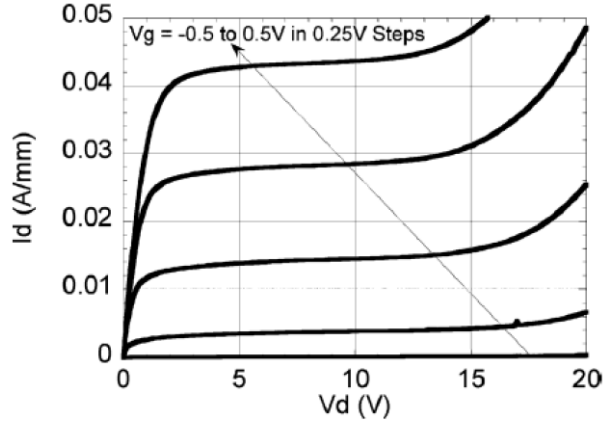
Fig. 4-11, Current density versus V_{DS} of the minimum size MESFET transistor

Fig. 4-12 shows the RF modeling of the MESFET transistor [64]. As shown, the diodes model the leakage current between the gate-drain and gate to source. R_g, R_d, R_s model the resistance on the gate track, drain and source respectively. Similarly, the L_g, L_d and L_s model the bond wire inductances in these three terminals.
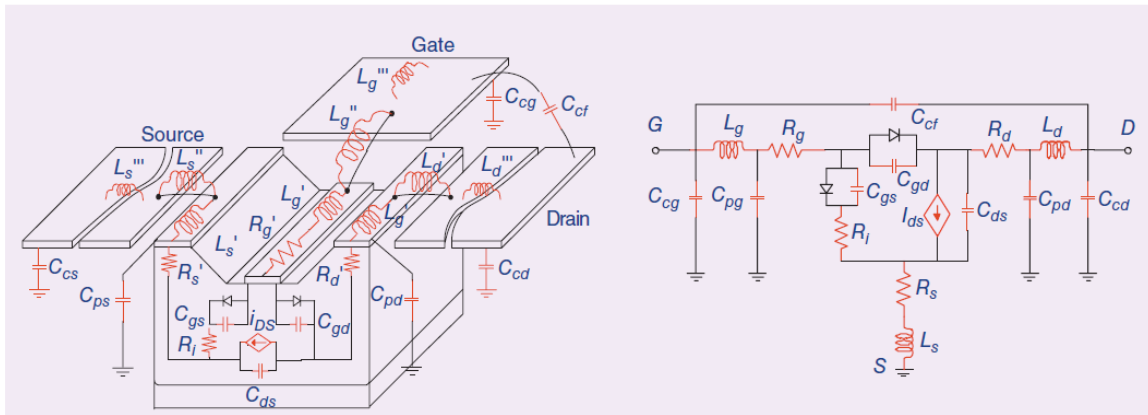
Fig. 4-12, MESFET parasitic modeling and circuit model

The size of the transistor is set based on the required output power. Since watt level output power is of interest in this design, the size of the transistor is set to W_{tot}=41mm based on [58]. Fig. 4-13 shows the implementation diagram of the MESFET transistor in the SOI CMOS process. As shown in Fig. 4-13, the gate contacts are placed at the first metallization layer (m_1 layer) on the N-well substrate. Fig. 4-14 shows the

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entire stack up in the 45nm CMOS SOI process. As shown in Fig. 4-14, there are 11 metallization layers available in this process. In this transistor, the distance between the gate and source is equal to the gate length ($L_{aS}=L_{ag}=200$nm) and the distance between the drain and gate is set to $L_{aD}=1000$nm. Under this condition, the I_D-V_{DS} of the transistor is shown in Fig. 4-15.
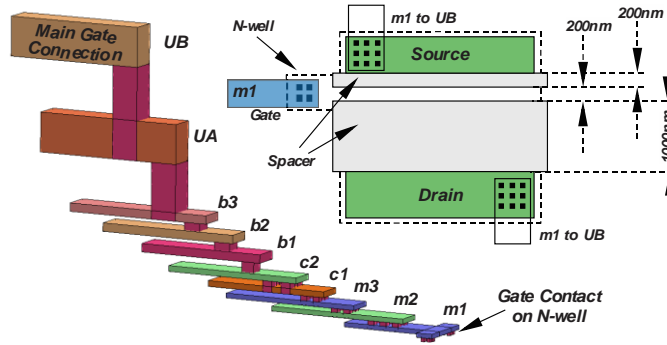
Fig. 4-13, Metallization diagram on the gate connections and the fabrication of the MESFET
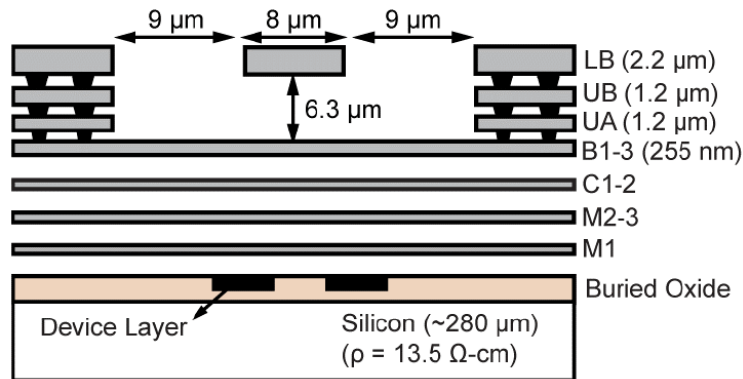
Fig. 4-14, Metal stack up in the 45nm CMOS SOI process
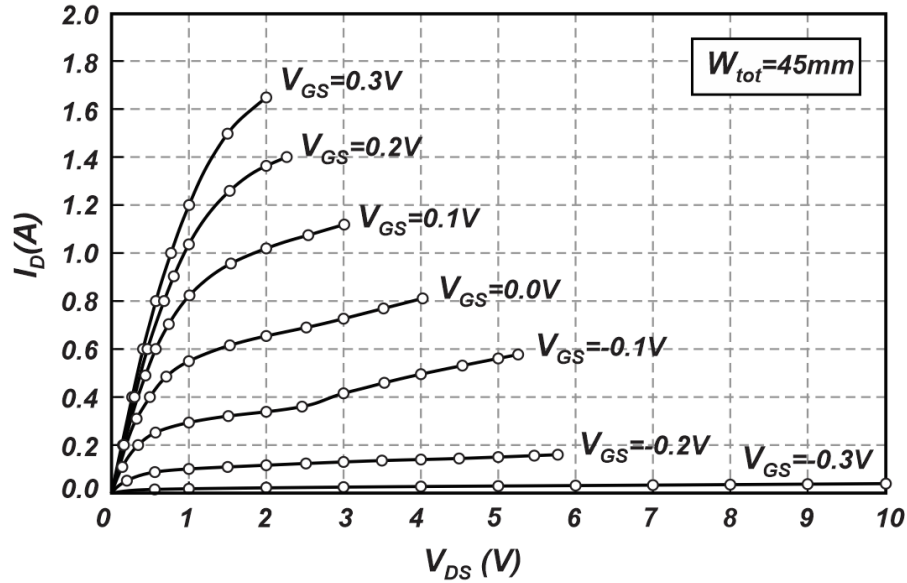
Fig. 4-15, Measured I_D-V_{DS} of the MESFET device (W=45mm)

As can be seen, the device is successfully able to tolerate voltages up to 5-6V, which is high enough to generate watt-level output power. Note that in Fig. 4-15 the tester is limited by the power and that is why some parts of the curves are truncated. Also, since the drain and source terminals are connected to each other through an N-well, the threshold voltage is negative in this device.

One of the critical parameters that must be considered, especially in CMOS SOI process, is the thermal dissipation. Since the buried oxide in the SOI process acts as an isolator, it reflects the heat back to the top as shown in Fig. 4-16a. The generated heat reduces the threshold voltage and increases the current and eventually creates a positive feedback loop that makes the circuit unstable. In [65] a technique to release the heat in the SOI process is proposed. In this technique, which is shown in Fig. 4-16b, c, several tie downs have been used that act as a thermal conductor and create a path from the top to the back of the die and release the heat.
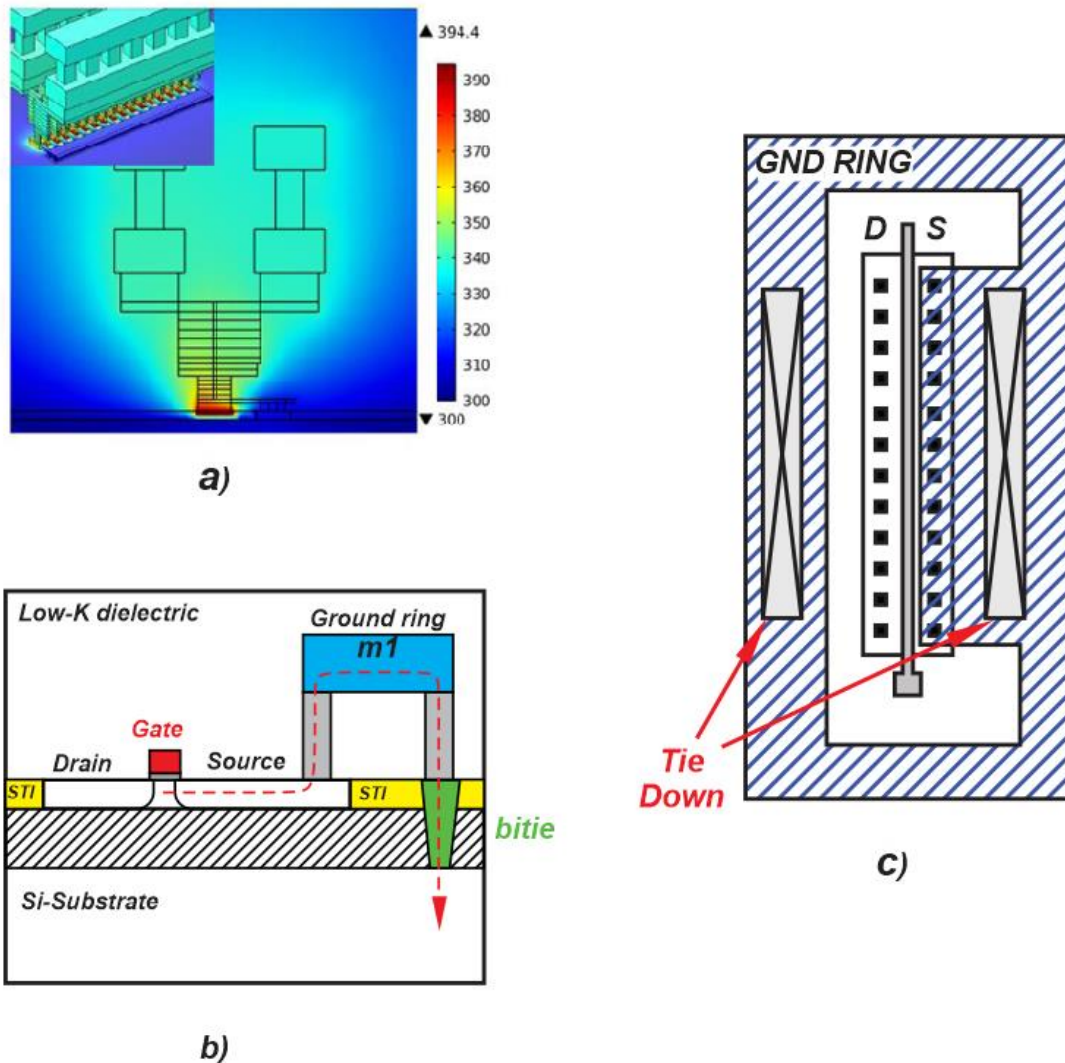
Fig. 4-16, a) Thermal issues in the SOI process, b, c) the methods to release the temperature

Since the plan in this project is to attach the die to the die stand on the PCB via super glue (based on the previous designs and experiences [58, 59, 66-68]), instead of utilizing tie downs that make the design quite complex, simply a fan is used to cool the die when the PA is set to generate high output power.

In order to make the heat release easier for this design, the die stand is connected to the back of the PCB (standard PCB thickness is H=31mils=0.787mm) with vias that are filled with a thermally conductive material (CB100) with the thermal conductivity of TC=3.5W/mK.

4.5 Implementation

The PA architecture has been implemented via the MESFET (W_{tot}=41mm) and the DAC structure shown in Fig. 4-8. In order to make the on-chip track resistance small, multiple paths with several vias between them have been utilized on the top most metallization layer. Fig. 4-17 shows the implementation of the tracks on the die.
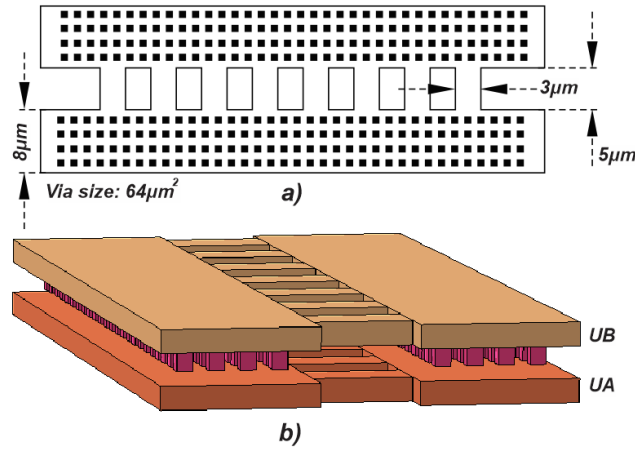
Fig. 4-17, Low impedance routing structure

Because the current that the DAC generates (500mA) should spread evenly between the MESFET pads, an H-shape structure as shown in Fig. 4-18 has been used. The slot structure at each rack has been used to reduce the resistance of the track.
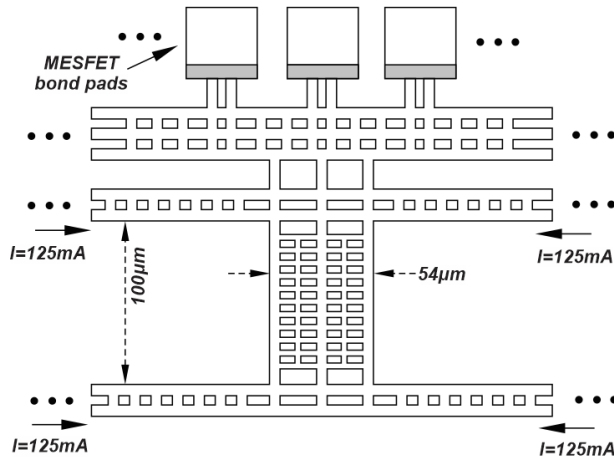
Fig. 4-18, The H-shape routing from the DAC to the MESFET

Since the MESFET gates are distributed over all the length of the MESFET transistor, the gate pads are modified such that there is no connection between the top most metal layers and the bottom layers. Fig. 4-19 shows the modified gate pads.
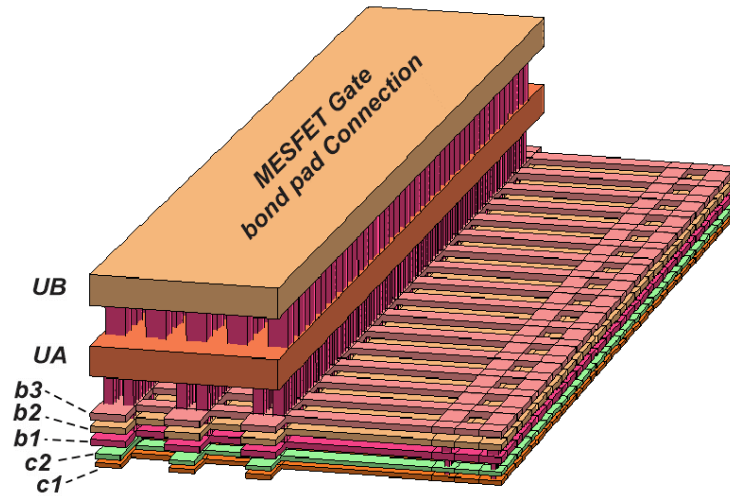
Fig. 4-19, The gate metallization routing on the custom made bond pads

Although the width of all the high current tracks are set such that they provide low resistance, the DAC current profile is deviated from the ideal behavior. Fig. 4-20 shows the behavior of the DAC current at different DAC binary states.
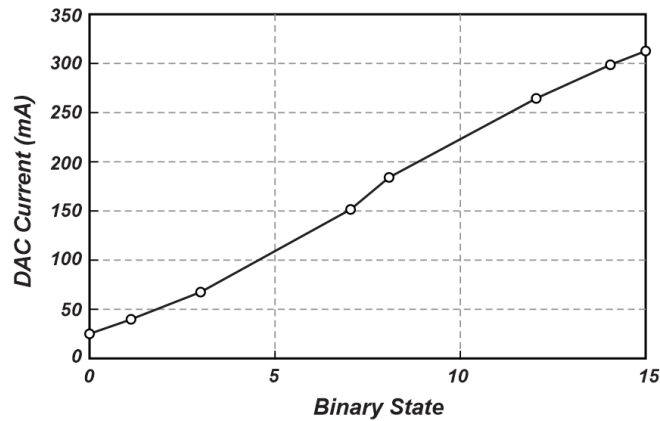
Fig. 4-20, The DAC output current level as a function of the input binary state

As can be seen, at low DAC state values, the DAC generates approximately the expected values (31mA). However, the maximum available current is deviated from the

desired value at high output current levels. The main reason for this deviation is the voltage drop on the gate-source of the transistor that is negligible at low current levels but is quite obvious at high current levels. Fig. 4-21 shows the reason of the voltage drop on the gate-source terminals for the current mirrors.
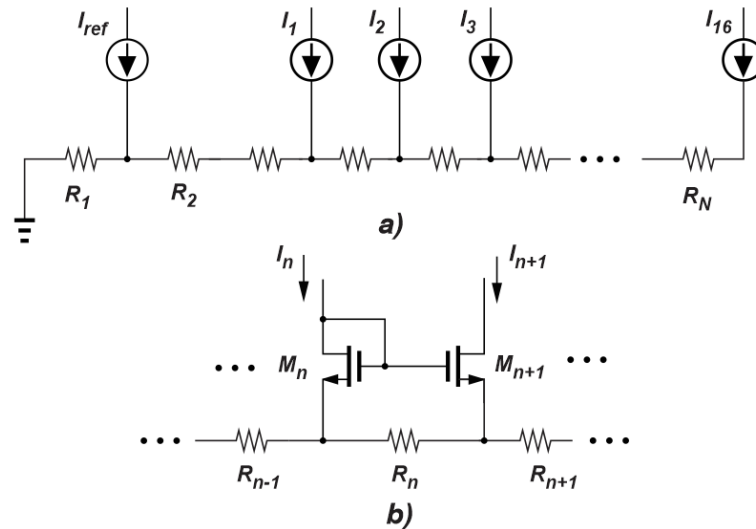
Fig. 4-21, a) Metal routing distributed parasitic resistance, b) The effect of parasitic distributed resistance on the current mirror voltage value

Since the V_{GS} of M_n must be equal to the V_{GS} of M_{n+1} plus the voltage drop across the R_n, at high current levels, the $V_{GS-M(n+1)}$ is less than the desired value and the current at the I_{n+1} branch is therefore less than the required value.

Since the main PA transistor needs to be in a common source (CS) configuration to provide the maximum amplification, a good AC ground must be provided at the source of the transistor. To provide access to the source pads of the MESFET, they are connected to a large pad on the PCB via bond wires as illustrated in Fig. 4-22. The AC ground at this pad is provided by placing $3\times180pF$ capacitors from this node to the main ground of the circuit. As shown in Fig. 4-22, because the MESFET source pads have different distances from the AC ground pad on the PCB, the bond wires that connect

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these pads to the AC ground pad on the PCB have different lengths. Fig. 4-23 shows the circuit diagram after placing all the bond wires.
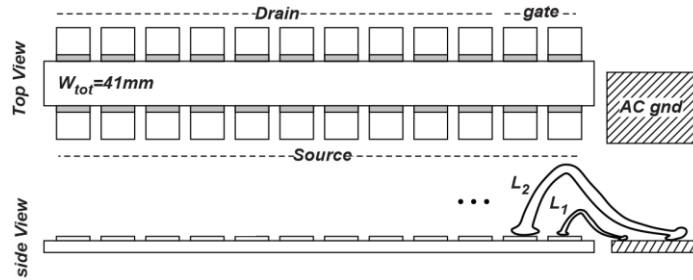
Fig. 4-22, The pad arrangement around the MESFET as well as the AC ground connection

In order to provide an AC ground at the source of the MESFET, the AC ground capacitors, C_{ac}, should resonate with the equivalent bond wire inductance at the operating frequency, ω_0. Although the LC resonance provides the ac ground at the node "X" at ω_0, the circuit behavior at the frequencies lower and higher than the operating frequency is also critical. Fig. 4-24 illustrates the circuit condition at different frequencies. As can be seen, the load that the node "X" sees varies with frequency. At low frequency, the bond wire contributes low impedance and therefore the load at this node becomes pure capacitive (C_{ac}).
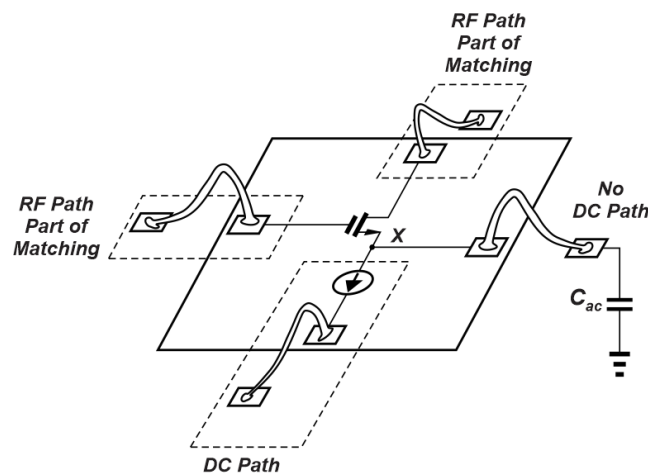
Fig. 4-23, Providing ac ground at the source of the MESFET
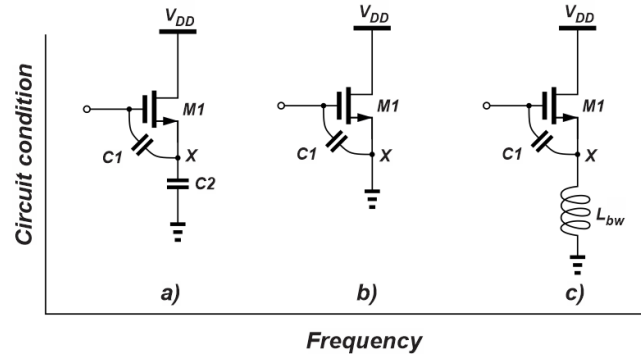
Fig. 4-24, PA condition at different frequencies a) low frequency, b) desired frequency, c) high frequency

By considering the capacitive degenerated CS stage shown in Fig. 4-25, the input impedance of the circuit can be calculated as:

$$Z_{in} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2} \tag{4-11}$$

where C_1 is gate to source capacitance, C_2 is the AC ground capacitance, g_m is the transistor transconductance and ω is the angular frequency. As can be seen, the real part of the impedance seen from the gate of the transistor (input resistance) is negative. Therefore, the circuit shown in Fig. 4-23 is prone to instability and oscillation at low frequency [53]. As a matter of fact the circuit shown in Fig. 4-25 is the basic architecture of the Clapp oscillator [3]. In general, creating negative resistance, regardless of the frequency, is the main reason for the oscillation in any types of oscillator [69-71].
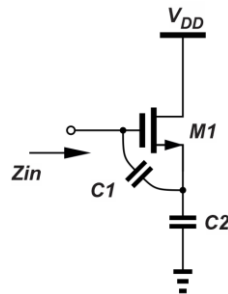
Fig. 4-25, Capacitive feedback configuration in the proposed structure

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In order to make the overall input resistance positive, an extra on-board resistance is placed in series with the gate of the transistor (R_g=15Ω). Due to the fact that the input resistance seen from the gate of the transistor is a reverse function of the capacitance at the source, the AC ground capacitors are increased to reduce the negative input resistance at low frequency. Considering a fixed value for the overall source bond wire inductance, increasing the AC ground capacitor reduces the resonance frequency between the bond wire and the AC ground capacitors and therefore the operating frequency of the circuit is reduced (f_0=70MHz).

At high frequency, the bond wire inductance becomes dominant and makes the load at node "X" pure inductive as illustrated in Fig. 4-24c. The input resistance seen from the gate terminal in this case is $R_{in} = (g_m/C_1)L_{bw}$, which is positive and does not lead to any oscillation in the circuit. Therefore, inductive degeneration that happens at the high frequency does not degrade the circuit performance in terms of stability.

At the output port (drain of the transistor) a matching network that consists of 25nH and 100pF (L-match network) is placed to provide the optimum impedance required by the MESFET (R_{opt}≈18Ω) and maximize the output power. The DC blocks at the input and the output of the circuit are placed to block the DC path from the supply sources to the source and load ports.

The die photograph of this design is shown in Fig. 4-26. As mentioned on the die photo, the total active area of this circuit is about 1.74mm^2 and the MESFET consumes almost 0.41mm^2 (24% of the total area).
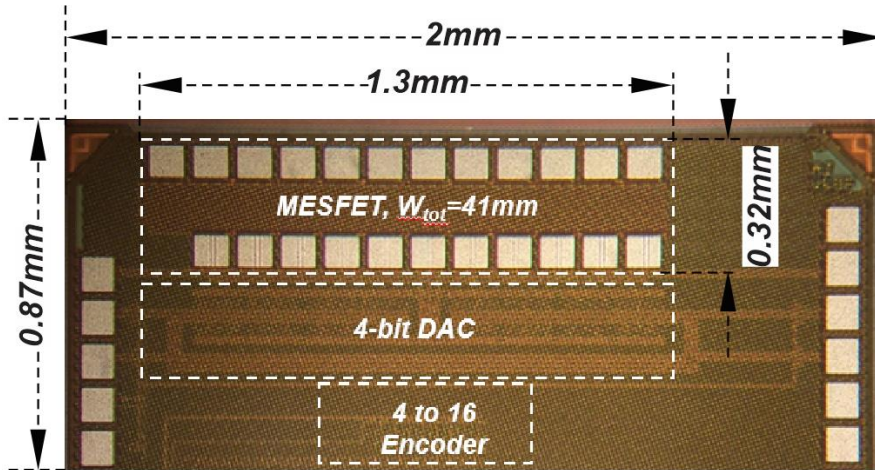
Fig. 4-26, DAC MESFET die photograph

4.6   Measurement Results

In order to measure the performance of the circuit, a 2-layer PCB with FR4 material with the board thickness of H=31mils=0.787mm has been designed. Fig. 4-27 shows the PCB circuit implementation of the board. As shown in Fig. 4-27 the board consumes 6.2×5.5cm^2. In order to provide a clean supply voltage a series of decoupling capacitor that consists of 4 different capacitors (C=10pF, 100pF, 1nF, 100nF) have been placed in parallel with the bias voltages at the gate and the drain of the transistor. The decoupled voltages then applied to the gate and drain of the MESFET transistor via L_{RFC}=47nH. The state of the DAC is set via a dip switch on the board. In order to ensure the DAC has an initial state, all the inputs are pulled down via R_{PD}=3.75kΩ. To provide any further modifications on the RF board, the top and bottom layers of the PCB are exposed without any solder mask.
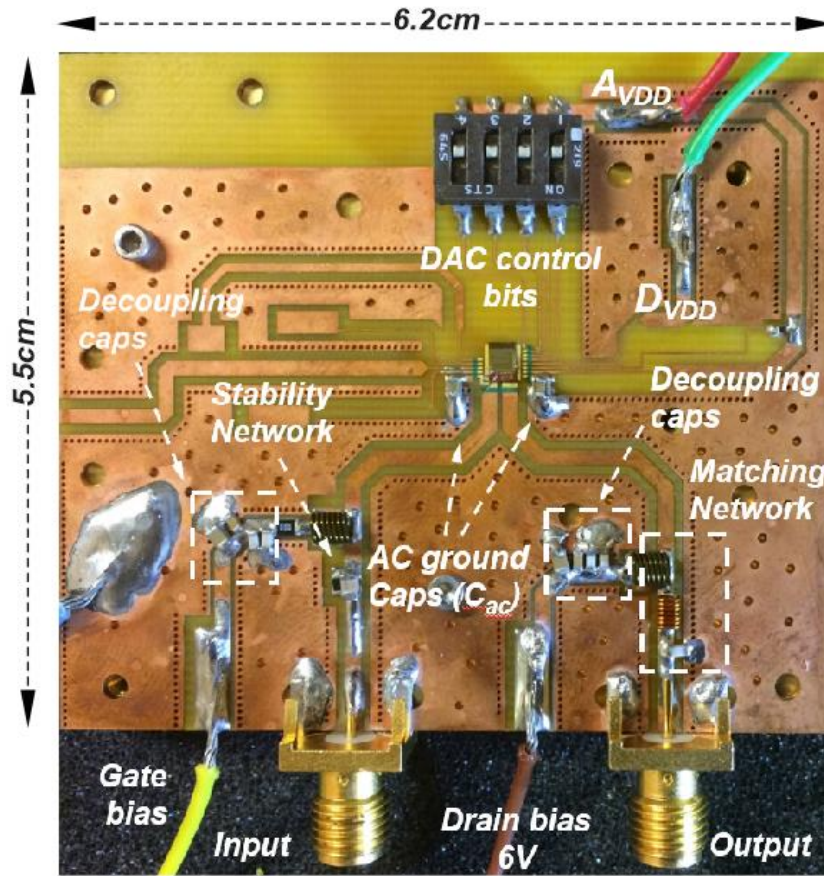
Fig. 4-27, The evaluation PCB configuration

Since in this project the Chip on board technique has been utilized, a close view of the die on the PCB is shown in Fig. 4-28. As can be seen, the bond wires from the source of the MESFET to the AC ground pad on the PCB have different shapes and lengths. Additionally, in order to save area, the AC ground capacitors are place on top of each other. Since there is a high risk of damaging the die in the assembly process due to the charge injection from the soldering iron, all the assembly process after mounting the die is done with the pick and place tool equipment.
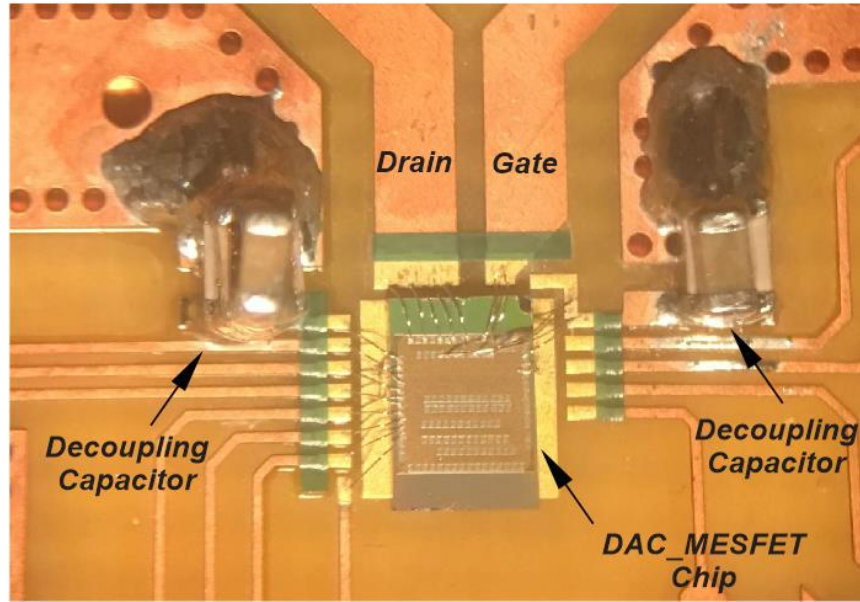
Fig. 4-28, Wire bonded die photograph on the PCB

The measurement setup of this circuit is shown in Fig. 4-29. Each supply input is connected to a separate power supply in order to monitor the current consumption of each section separately. The 4-bit DAC is connected to the 0.9V supply and the DAC control bit digital circuitry (4 to 16 bit encoder) is connected to the same potential but to a separate power supply source. Since the MESFET has negative threshold voltage, the initial gate voltage is set to -0.7V to ensure the transistor's gate channel is close. The main drain potential starts from 0V and gradually rises to the desired value (0 to 6V).

In order to characterize the PA performance (finding the optimum input and output impedance) the input and output ports are connected to the impedance tuners as shown in Fig. 4-29. Fig. 4-30 shows the small signal S-parameters measurement results as well as the μ-factor (stability parameter) of the circuit over frequency. As can be seen, the PA shows reasonable (~-10dB) input and output reflection coefficients between 40MHz and 100MHz. The small signal gain is about 20dB and the revers isolation is below -20dB over all the frequency range. Because in this architecture the PA current

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changes instead of the drain voltage, at each current level the MESFET transistor has different small signal parameters and as a result, the PA has different S-parameters at each biasing condition. This S-parameter shown in Fig. 4-30,Fig. 4-31 have measured when V_{DD}=6V, V_{Gate}=150mV and I_D=307mA. Under this condition, the μ-factor is greater than 1 that shows that the circuit is unconditionally stable. The S-parameter of the system from 10MHz to 200MHz is shown on the smith chart in Fig. 4-31.
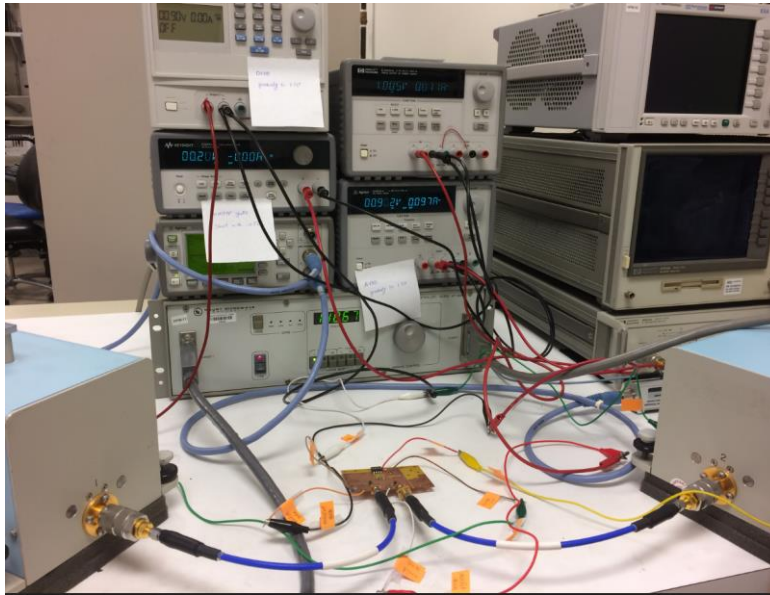
Fig. 4-29, Measurement setup
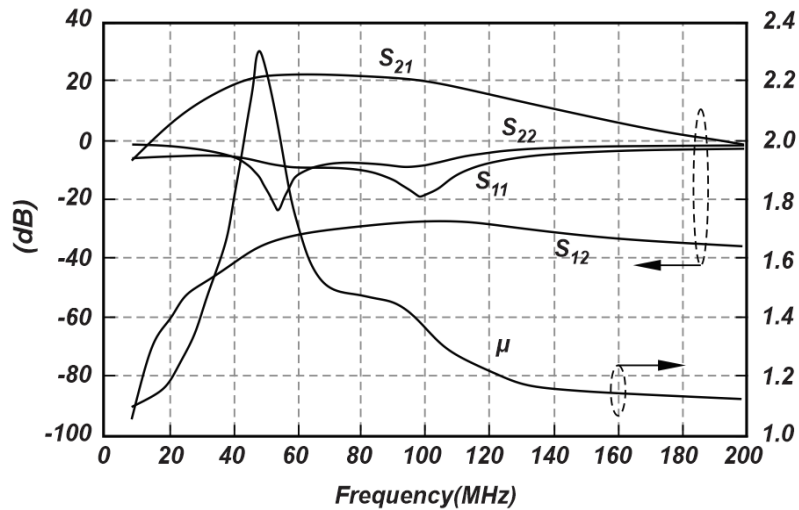
Fig. 4-30, S-parameter measurement result as well as the stability factor over frequency

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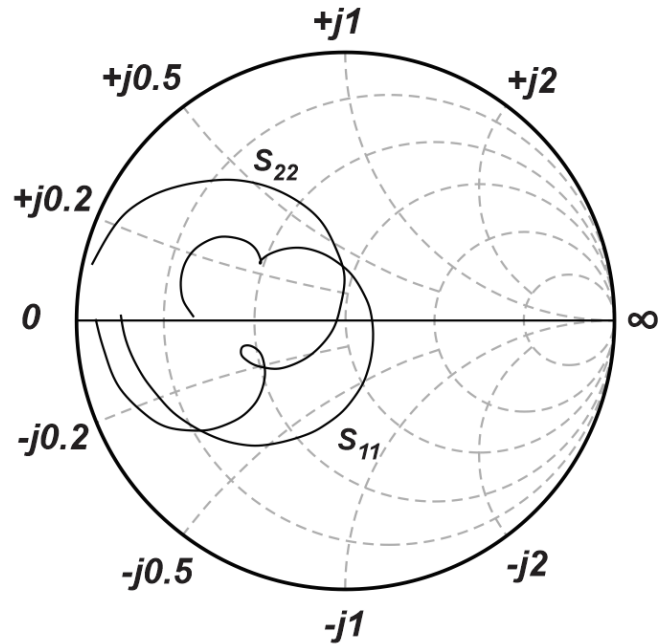
Fig. 4-31, Input and output reflection coefficients

The input output relationship of the PA is shown in Fig. 4-32. As can be seen, the

relationship between the input and output power follows the similar trend as in an stand-

alone PA. By increasing the quiescent current (DAC current) the saturated output power

increases and at the maximum DC current level (I_D=500mA) the output power is 32dBm,

which is equal to the maximum achievable power when the MESFET is placed in the

stand-alone PA configuration [58].
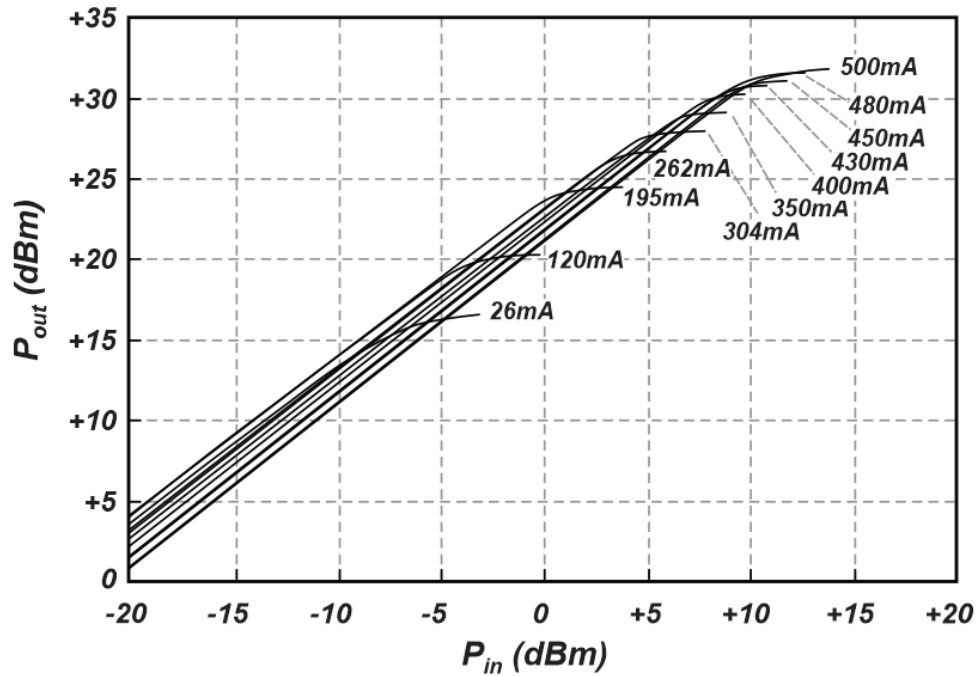
Fig. 4-32, Input-output relationship of the proposed technique

The power gain of the PA is shown in Fig. 4-33. As can be seen the power gain varies between $G_p=21$dB and $G_p=24$dB. This variation in gain ($\Delta G_p \approx 3$dB) is due to change in the transconductance of the PA with the current. At low current levels, the transconductance value is small and by increasing the I_{DAC} it increases as well. However, if the current passes a specific value ($I_D=200$mA in this case) the power gain reduces. The main reason for this phenomenon is the optimum impedance required by the PA. Since the variation in the DAC current changes the specification of the transistor such as: g_m, C_{gs}, C_{DS} and r_o, the optimum impedance that the PA required for the maximum power gain varies. Therefore, the power gain has an optimum at only one specific current level. The variation of the power gain versus the DAC current level is shown in Fig. 4-34.
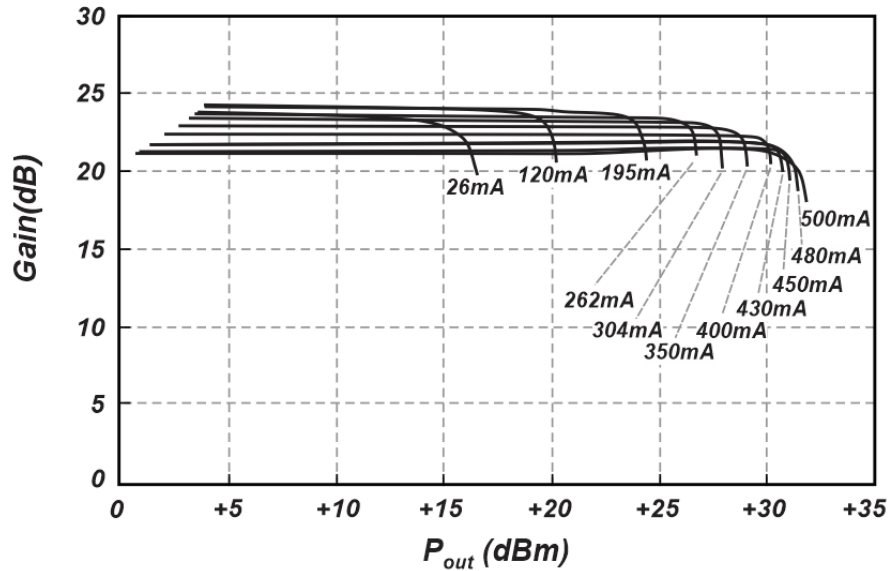
Fig. 4-33, Power gain as a function of output power for different DAC current levels
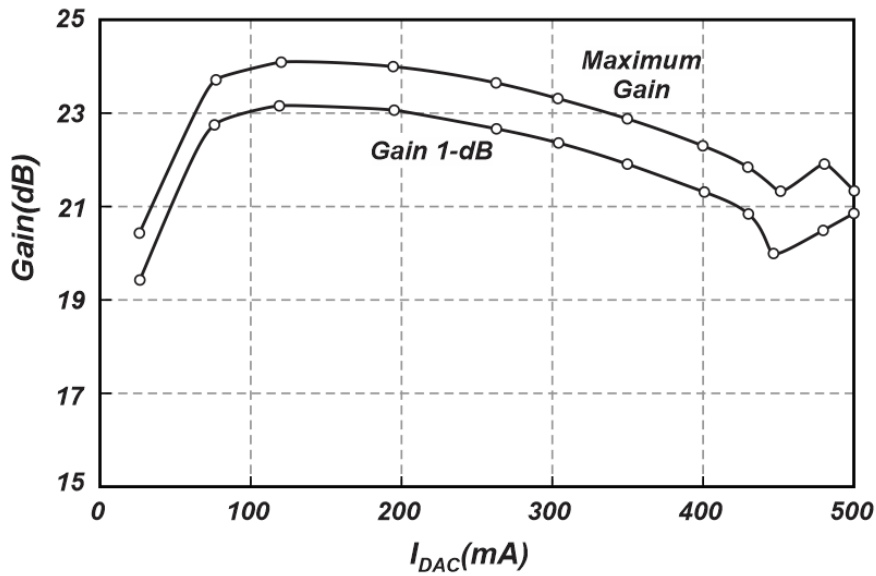
Fig. 4-34, Maximum gain and gain at the 1-dB compression point as a function of DAC current

The efficiency versus output power for different quiescent current level is shown in Fig. 4-35. It is quite clear that at high DAC current values, which corresponds to the high output power levels, the maximum efficiency is higher than when the current is set to lower levels. When the PA current is set to I_D=500mA, the maximum efficiency is about 45% that corresponds to the Class-A of operation and perfectly matches with the

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theory analysis [12]. At low current levels because the PA dissipates less DC power, the peak efficiency is more than when higher current levels is used. As a result, at low current values, higher efficiency can be achieved.
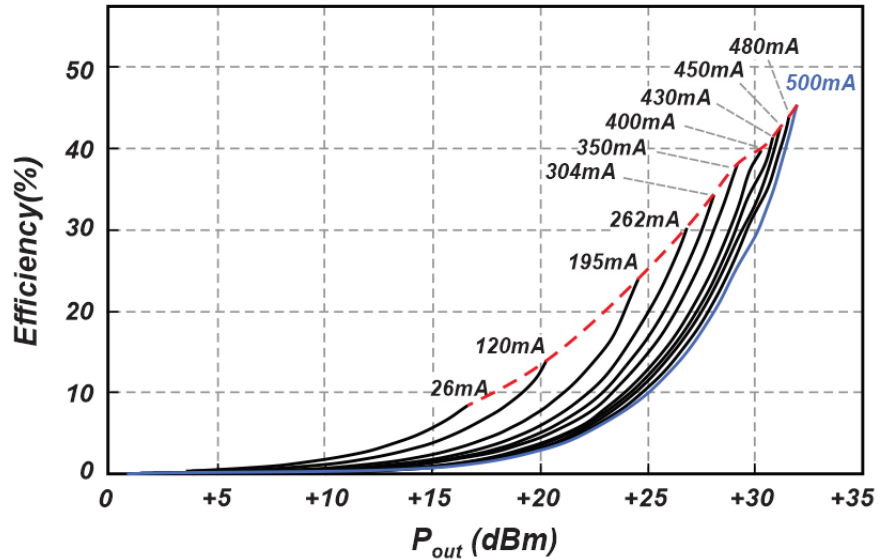
Fig. 4-35, Efficiency versus output power for different DAC current level

The red dotted line in Fig. 4-35 shows the optimum efficiency track for this circuit. If the quiescent current is set based on the required output power level, the efficiency value moves on this line. Note that similar to the conventional envelope tracking method, the proposed efficiency enhancement technique can improve the PA efficiency by almost 10-15% compared to when the PA is biased at the maximum voltage and current level [23].

Because the gain of the PA is quite high ($G \approx 20dB$) the power added efficiency (PAE) is quite close to the drain efficiency (η_D). Also, the dissipated power in the DAC biasing circuit has been included in the entire power consumption calculation.

The linearity of the PA is measured using the output third order intercept point (OIP3) parameter. This parameter is plotted in Fig. 4-36 as a function of the DAC output

current. As shown in Fig. 4-36, by increasing the current level the OIP3 increases that

shows PA becomes more linear. Since I_{DAC} controls the PA's class of operation, the

current level has a direct effect on the linearity of the overall PA. By increasing the DAC

current level, the PA moves from class-AB toward class-A of operation and the linearity

enhances. However, after almost I_D=200mA, by increasing the PA quiescent current the

linearity does not improve significantly.
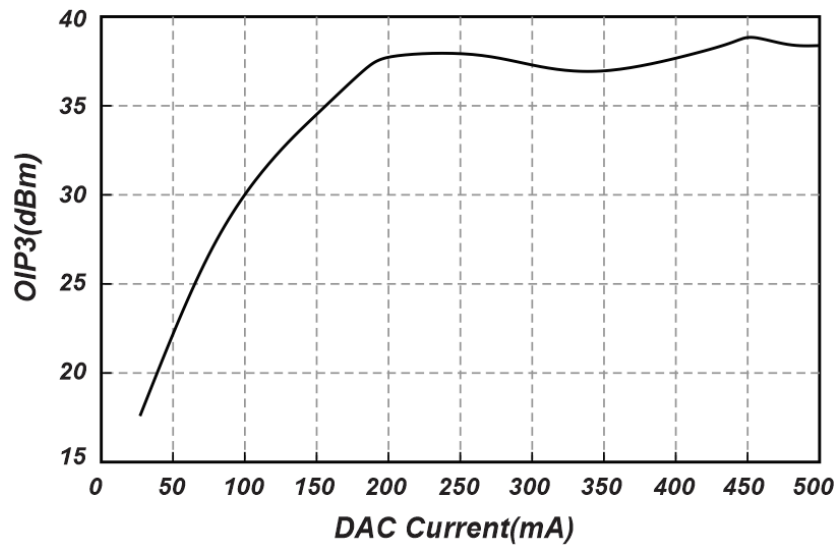
Fig. 4-36, The output intercept variation as a function of DAC current level

To keep the voltage across the DAC at 900mV, the gate voltage of the transistor

must be set according to the input signal power level. Fig. 4-37 illustrates the voltage

values on the gate of the MESFET transistor as a function of DAC current level. It is

quite clear that by increasing the DAC current, the source of the MESFET reduces and

therefore higher gate voltage is required to keep this voltage fixed.
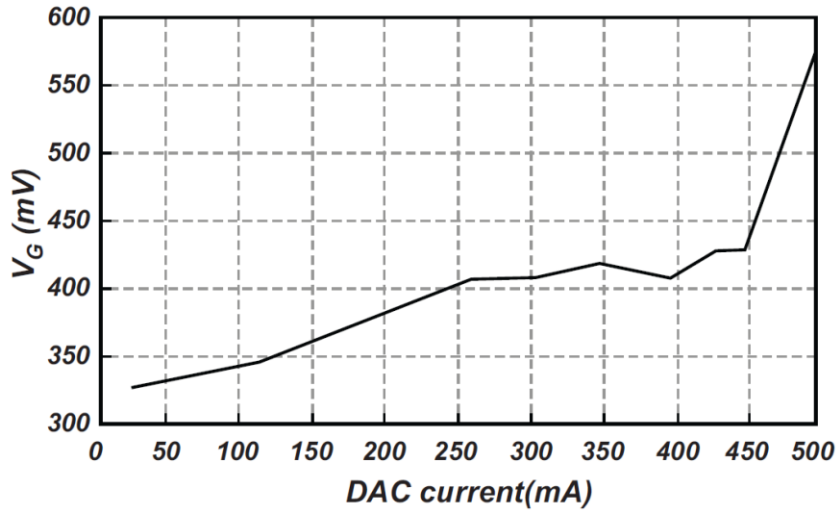
Fig. 4-37, Required voltage on the MESFET gate for proper operation

In order to check the performance of the PA when the actual modulated signal is applied to the circuit, an enhanced data rates for GSM evolution (EDGE) signal with the data rate of 70.83kb/sec has been applied to the PA. Fig. 4-38 shows the efficiency of the PA when the modulated signal is fed at the input port. Similar to the single tone measurement, by reducing the current of the PA the efficiency increases. The red dotted line on the graph shows the border that EVM=5% (a requirement needs by the EDGE standard). Since 6dB peak to average power ratio (PAPR) has been considered as the criterion, the minimum PA quiescent current is set to I_D=262mA. Fig. 4-39 shows the output signal spectrum of the PA when the PA current is set to I_D=500mA. The average output power can be easily calculated as $P_{avg-out}$=27.9dBm within 200kHz of bandwidth. The first, second and third channel leakage ratios are $ACPR_1$=-16.4dBc, $ACPR_2$=-56.9dBc and $ACPR_3$=-71.6dBc. Fig. 4-40 shows the measured output constellation and Fig. 4-41 shows the output spectral density of the PA.
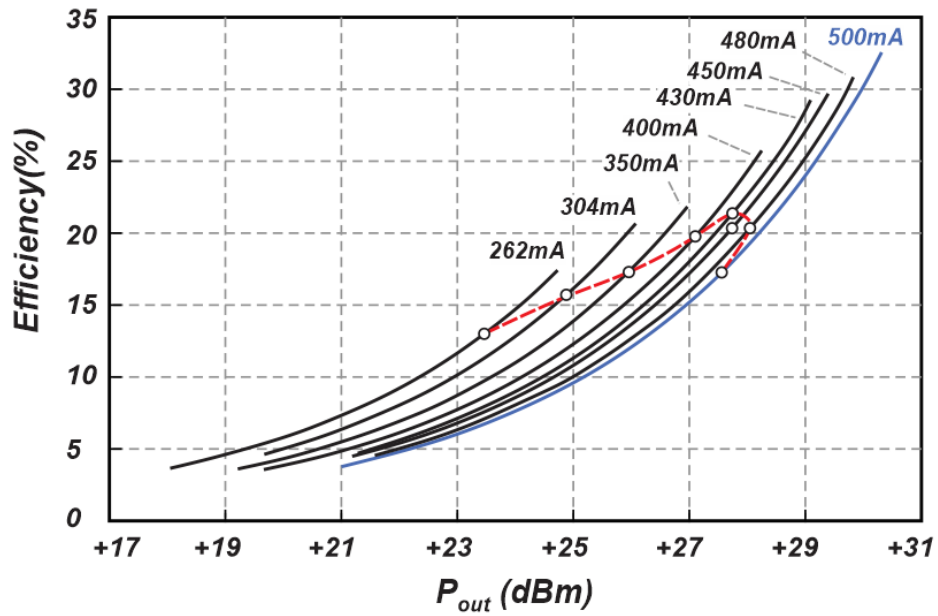
Fig. 4-38, Efficiency of the modulate waveform as a function of output power for different DAC current levels
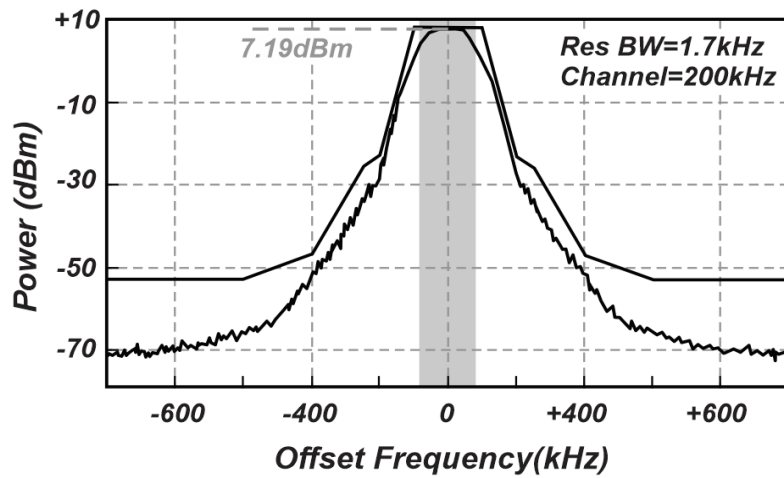
Fig. 4-39, Output spectrum of the EDGE signal
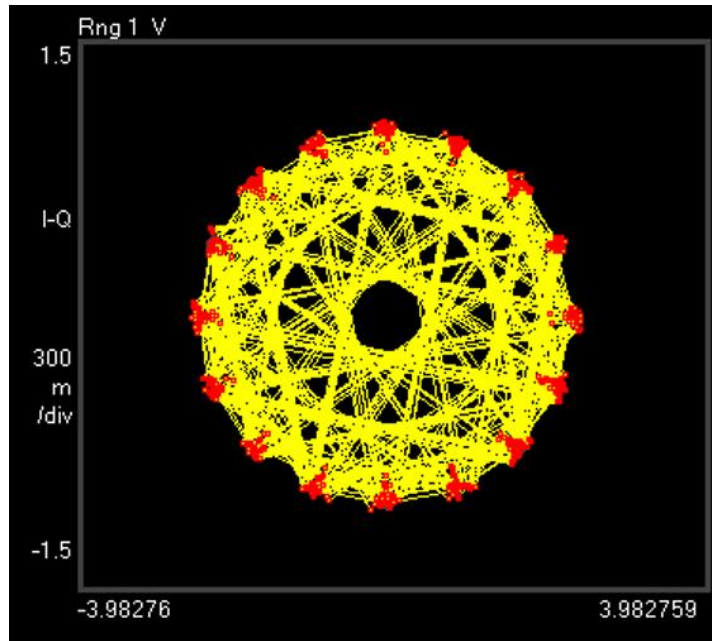
Fig. 4-40, Output voltage variation over time on the modulated signal constellation
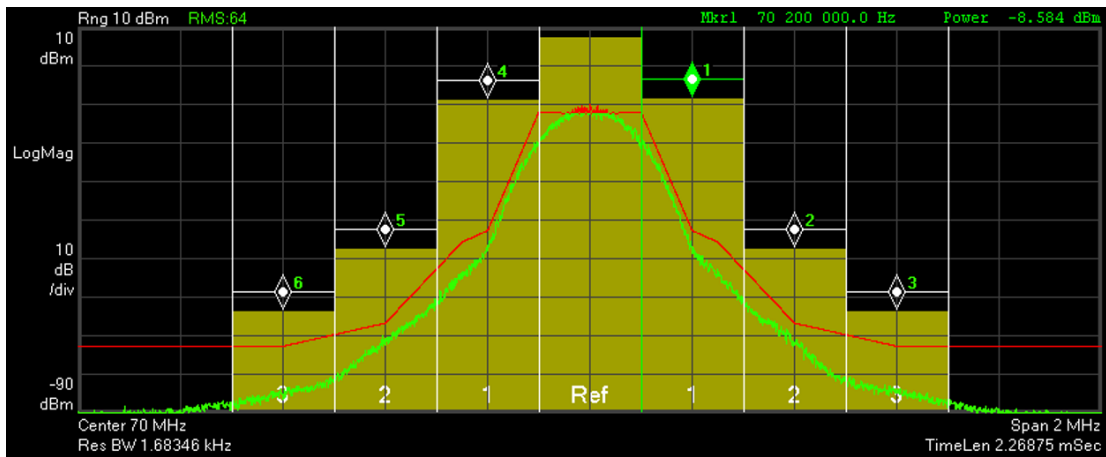
Fig. 4-41, The snap shot of the output modulated signal

4.7   MESFET-MESFET architecture

In order to increase the voltage handling capability, instead of utilizing the variable current source with a DAC, another MESFET transistor has been used at the source of the main transistor. This configuration is shown in Fig. 4-42. The bias signal (V_{bias}) is used to control the biasing current in the main transistor path (I_{bias}). In order to compare the performance of this implementation and the previously presented current steering DAC based structure, the rest of the components in the circuit are unchanged.
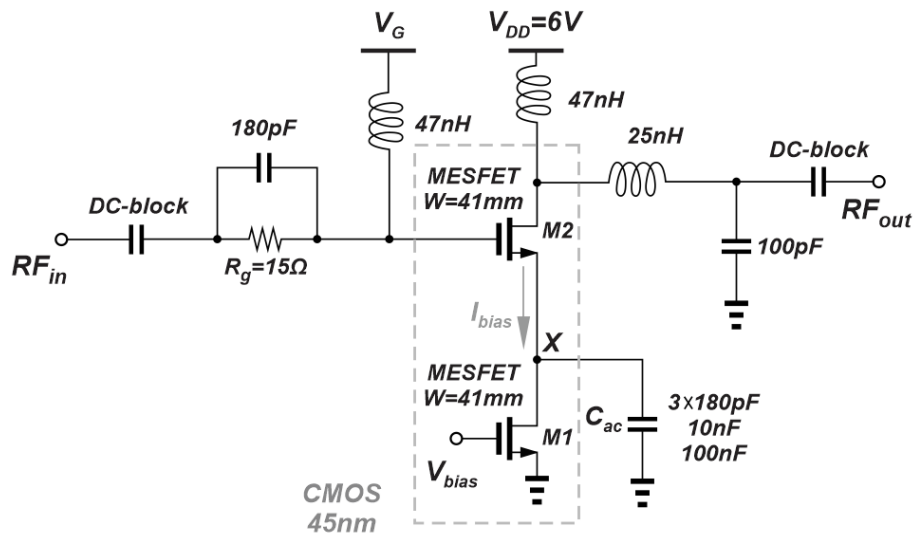
Fig. 4-42, The MESFET-MESFET circuit architecture

The photograph of the die is shown in Fig. 4-43. As shown, the same size MESFET, which is called MESFET bias, is used as the current tracker and the main transistor, which is called MESFET PA, is used as the PA device. The drains of the MESFET bias are connected directly to the source pads of the MESFET PA with wide tracks in order to reduce the resistance between them. Although the middle pads (drain pads of the MESFET bias) have not used, in order to keep the consistency in the design, the two transistors are left exactly identical.

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The source pads of the MESFET PA are then used to provide AC ground. Similar to the previous implementation, the C_{ac} consists of 5 capacitors with different sizes to ensure complete ground at the source of the MESFET PA across all the frequency range. Fig. 4-44 shows the evaluation board configuration that is used in this measurement.
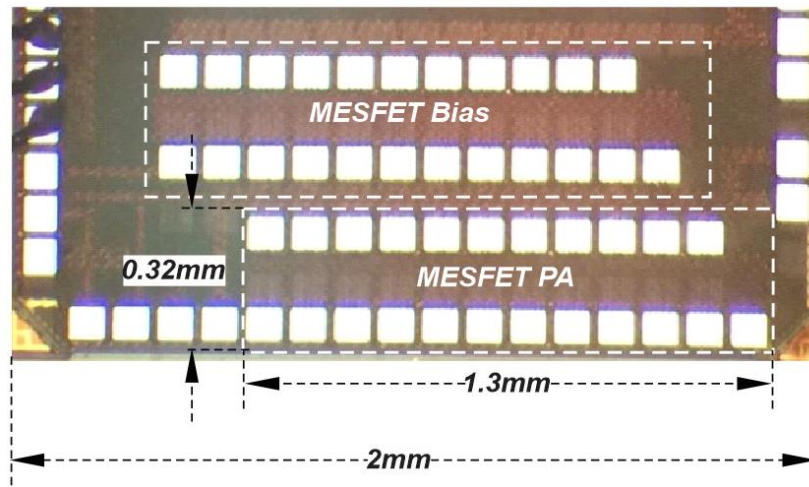
Fig. 4-43, The MESFET-MESFET chip photograph
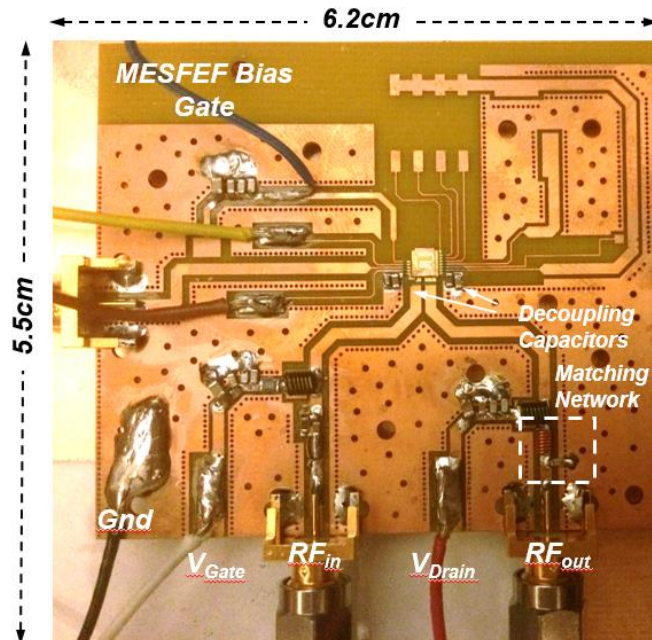
Fig. 4-44, The evaluation board of MESFET-MESFET architecture

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At first, DC measurement has been done on this circuit to ensure that the circuit has a stable steady state. Fig. 4-45 shows the I_D-V_{GS} of the circuit for different drain values. As shown in Fig. 4-45, by increasing the V_{GS} of M_1 the output current increases in a polynomial manner, which is quite similar to the theoretical analysis of the transistor. It is quite clear that the bias current when the supply voltage is set to V_{DD}=3V does not follow the polynomial trend and bends at about V_{GS}=-230mV. The reason for this bending is that the biasing transistor (M_1 in Fig. 4-42) enters the triode region. Since the MESFET transistor has a negative threshold voltage, the gate potential on M_2 must be high enough to keep the biasing transistor (M_1) in saturation. Otherwise, the biasing MESFET does not performs as a current source.
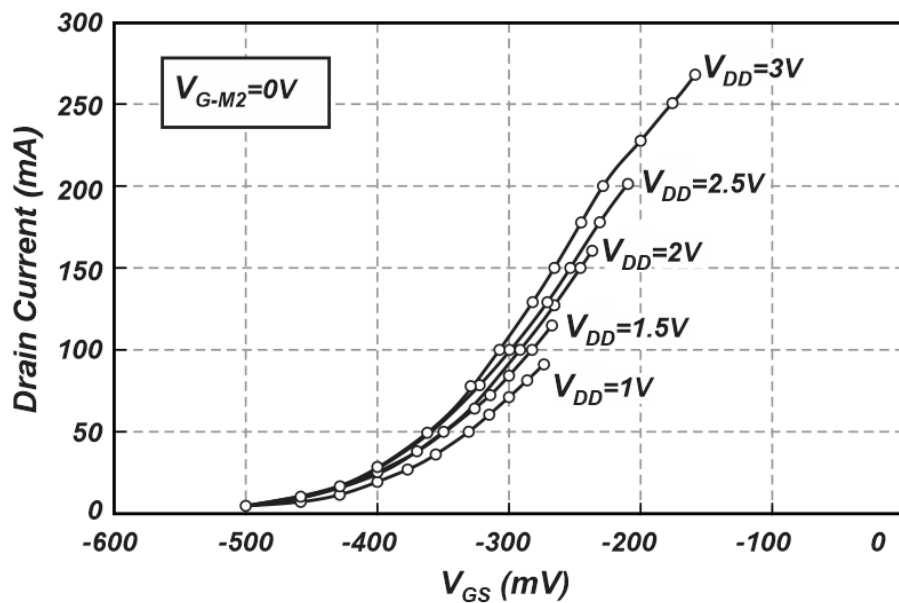
Fig. 4-45, I_D-V_{GS} of the MESFET-MESFET structure

In order to see the performance of the circuit when the biasing transistor is in saturation for all the input bias voltages, at the constant supply voltage (V_{DD}=3V) the V_{GS} of M_1 is changed for three different values of gate voltage on M_2. As can be seen in Fig. 4-46, at high gate voltage values, the curves follow the polynomial behavior and clearly

shows that M_1 is in saturation region. The maximum drain current achieved in this configuration before the transistor shows unstable behavior is about I_D=300mA. It has been observed that by increasing the V_{GS-M1} more than -260mV, the drain current increases quite fast and reaches the maximum allowable on the supply voltage. Therefore, the current has been kept below I_D=300mA.
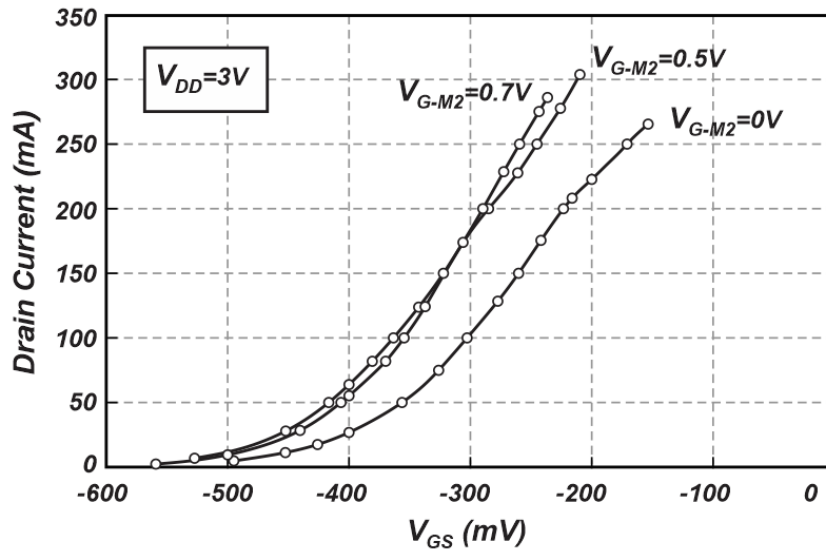
Fig. 4-46, I_D-V_{GS} of the MESFET-MESFET structure

Fig. 4-47 shows the behavior of the mid node (node "X" in Fig. 4-42) as a function of V_{GS} of the M_1. It is quite clear that the relationship between the voltage of the gate of M_2 and mid node "X" is quite linear (similar to the source follower circuit) and confirms the correct operation of the circuit.
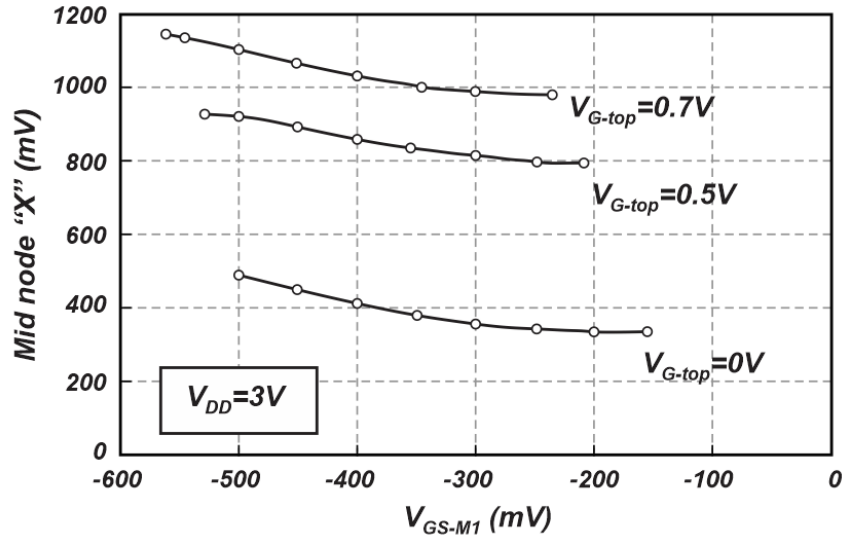
Fig. 4-47, The mid node "X" variation as a function of V_{GS} of the bottom MESFET for different gate voltage values

4.8 MESFET leakage current challenge

One of the critical parameters that must be considered in this type of implementation is the biasing stability. Since the MESFET transistor does not have the gate oxide, the metal-semiconductor contact on the gate terminal forms a Schottky diode. Fig. 4-48a conceptually shows the diode between the gate, drain and source terminals. The values of the leakage current (unwanted current in the gate terminal) highly depends on the area of the transistor, terminals' potential and temperature. Fig. 4-49 shows the gate leakage current measurement result for two different supply voltages.
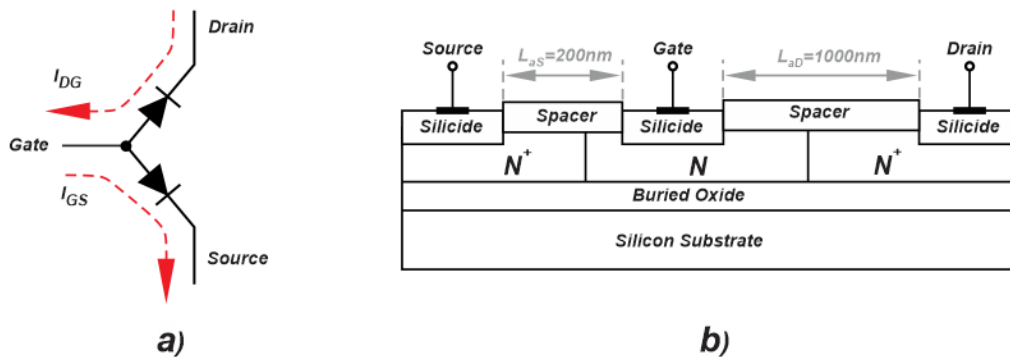
Fig. 4-48, a) The MESFET Schottky diode model, b) MESFET transistor architecture
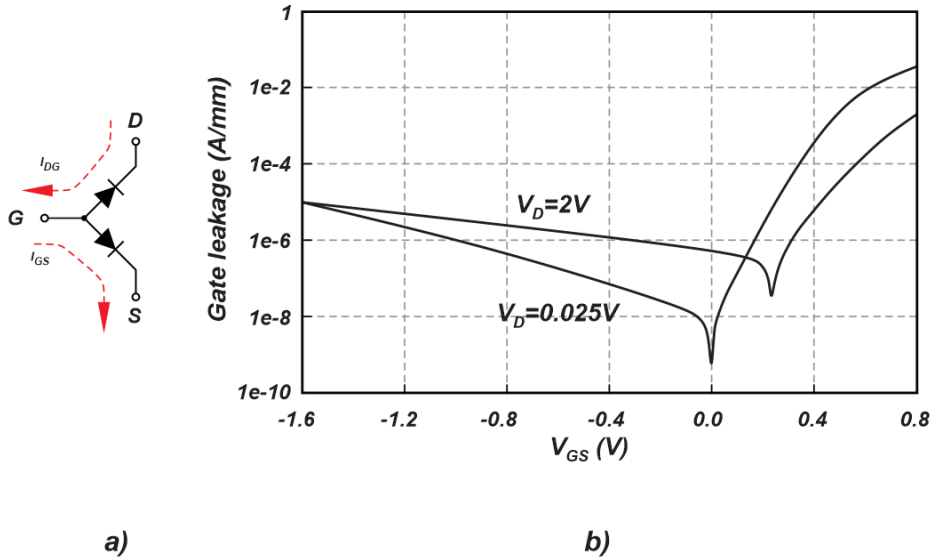
Fig. 4-49, a) diode model of the MESFET transistor, b) Gate leakage current density

The gate leakage current can be analyzed for two different cases: 1) low drain

voltage levels (≈0V) and V_S=0V, 2) high drain voltage value (2V) and V_S=0V.

Case 1 (V_D≈0V, V_S=0V):

When the gate voltage is lower than the threshold voltage (ex. V_G=-1.6V) the

diode between the gate to drain and gate to source are reverse biased (V_{DG}=V_{SG}=1.6V).

At this situation, two diodes are in reverse biased condition and the summation of those

currents come out of the gate terminal. By increasing the gate voltage the V_{GS} becomes

close to 0V and the gate-source diode starts to conduct in the forward direction. When the

forward current of the gate-source diode is equal to the reverse current comes out of the

gate-drain terminal, the total gate leakage current is zero and causes the notch on the gate

leakage current shown in Fig. 4-49b. By increasing the gate voltage to higher values

(V_{GS}>0V), the forward current associated with the gate-source diode, the current

increases exponentially.

Case 2 (V_D≈2V, V_S=0V):

Due to the fact that at deep reverse bias condition, the diode's leakage current is a weak function of the reverse voltage, at log gate voltage values (V_{GS}=-1.6V) the same amount of leakage current comes out of the gate terminal. By increasing the gate voltage the gate-source diode starts to conduct forward current (V_{GS} slightly higher than 0V). Because the gate-drain voltage is still in the reverse condition, higher V_{GS} value is required to compensate the reverse leakage current that comes from the gate-drain diode. As a result, the notch on the curve (V_{DD}=2V) is placed at higher V_{GS} values.

Since the threshold voltage of the MESFET is about -0.5V to -0.6V, most of the time the transistor is biased at the point where the gate leakage current comes out of the gate terminal. Considering the stability requirement, a resistance in series with the gate is required to prevent the unwanted oscillations. As an example this configuration is show in Fig. 4-50. Since the transistor's width is large (W=41mm), the leakage current is quite high at high supply voltages ($I_{leakage}$≈2mA). Because the gate leakage current comes out of the gate terminal, the intrinsic gate-source voltage (V_{gsi}) is higher than the external bias on the gate terminal (V_{bias}), $V_{gsi}=V_{bias}+R \times I_{Leakage}$). Enhancing the gate-source voltage eventually increases the transistor's drain current. Higher drain current increases the power dissipation across the drain and source terminals and enhances the temperature of the device.

As mentioned in [72-74], the reverse leakage current of a diode is a strong function of the temperature. By increasing the temperature, the reverse leakage current increases and enhances the intrinsic gate-source voltage of the transistor (V_{gsi}) and as a result the drain current of the transistor increases. This mechanism continues until the drain current limits by the power supply.

The other mechanism that enhances the current level is the dependency of the threshold voltage and the temperature. As presented in [75], the threshold voltage has negative temperature coefficient. As a result, the transistor's power dissipation reduces the threshold voltage. Threshold voltage reduction leads to higher transistor's drain current and increases the power dissipation across the drain-source terminals of the transistor and this positive feedback loop continues for ever.

The dependency of the diode leakage current and the transistor's threshold voltage on the temperature leads to an endless vicious circle and increases the transistor's drain current. Since high resistance in the gate path increases the intrinsic gate-source voltage of the transistor, this resistor (R_g in Fig. 4-50) should not set to very high value. In the initial measurement this resistor is set to $R_g=39\Omega$ that leads to $I_{D-max}=300mA$. In order to increase the drain current to higher values ($I_D=500mA$), lower resistor must be utilized.
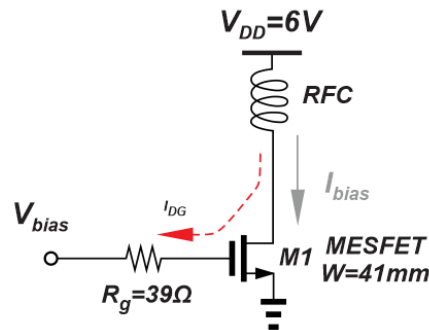
Fig. 4-50, The gate stability resistance placement

4.9 Conclusion

In this chapter we introduced a novel method for implementing the average power tracking. The proposed technique enables the implementation of the tracker and the PA on the same CMOS process. The MESFET transistor is introduced as a candidate for

generating wall-level output power. The proposed technique shows a similar behavior to the conventional envelope tracking methods. Unlike the conventional ET techniques the tracker experiences much less voltage variation, since the proposed method is designed based on the current steering DAC that is implemented at the source of the main PA transistor. The proposed technique shows better than $\eta_D=43\%$ efficiency and higher than $G_P=20dB$ of power gain when tested with a continuous wave (CW) signal. The entire PA tested with the 70.83kb/sec EDGE signal with 200kHz of bandwidth and shows better than EVM=5% while transmitting $P_{out}=27dBm$ average power.

CHAPTER 5

FULLY DIGITAL TRANSMITTER

5.1   Introduction

In this chapter we focus on the design and implementation of CMOS drivers that

are applicable to fully digital transmitters. A system level description of the fully digital

transmitter will be presented and a review of all available drivers are given. Finally, two

of the main candidates for this implementation will be introduced. Simulation results of

the drivers will be shown and the required PCB for the measurement is explained

5.2   System level description

Undoubtedly, digital circuits and systems have several benefits over the analog

counter parts such as: less prone to the environmental noise than analog circuits, ability

of operation with low voltage levels without performance degradation, programmability,

encryption ability and the ability of saving data. As a result, implementing all the

communication transceiver in the digital domain is of interest.

Due to the fact that the digital signals cannot propagate through the space, at the

end of the transmitter chain the signal must be converted into analog domain. A common

method of implementation is shown in Fig. 5-1. Since the envelope of the input signal to

the PA varies according to the input signal, the amplification requires a linear PA.

Because utilizing a linear mode PA degrades the efficiency of the overall transmitter [12],

in order to enhance the efficiency, in this project a switched mode PA has been utilized.
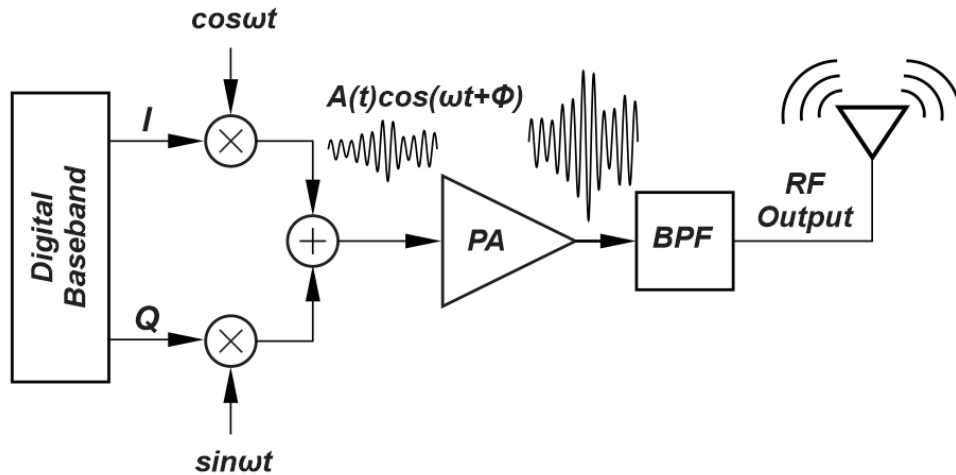
Fig. 5-1, Conventional transmitter architecture

A digital transmitter architecture that is used in this project is shown in Fig. 5-2. In this architecture, unlike the conventional linear transmitter architectures that use in-phase (I) and quadrature (Q) base band signals, amplitude and phase of the input signal are being used. Since the amplitude of the base band signal is not high enough to turn on and off the transistor in the switched mode power amplifier, a digital driver block is required to enhance the input signal voltage amplitude.
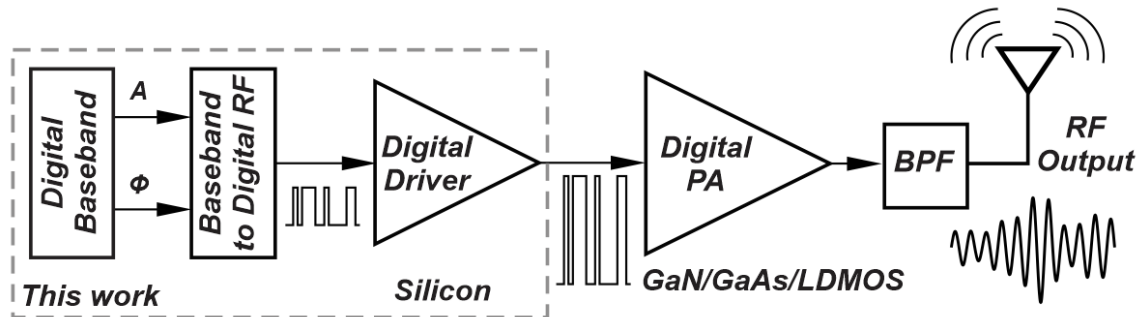
Fig. 5-2, Overall digital transmitter architecture

As can be seen in Fig. 5-2, the information is modulated on the amplitude and phase of the carrier signal. The amplitude modulation is done by generating a pulse width modulation (PWM) signal and phase modulation is implemented by changing the

position of the pulses with respect to each other. In this project the amplitude modulation has been implemented using two different methods: 1) Base band PWM (BB PWM) and 2) RF PWM. These two different types of amplitude modulations are illustrated in Fig. 5-3. In the BBPWM, the amplitude is defined based on the number of pulses in a time unit while in the RF PWM counterpart, the duty cycle of the signal is changed while the number of pulses in a time unit (time frame) is fixed.
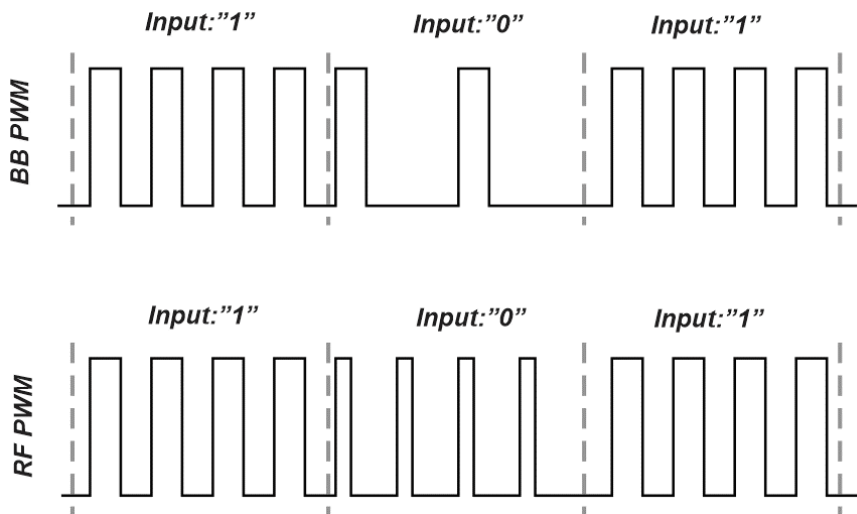
Fig. 5-3, Base band and RF PWM signal wave forms

The entire amplitude and phase modulations are implemented in digital domain using a low supply voltage value (V_{DD}=0.9V) to reduce the digital power dissipation ($P_{diss} = 1/2\, C_L V_{DD}^2 f$). Since the voltage swing at the output of the modulator is not strong enough to turn on and off the main PA switching transistor and interface circuit (driver) is required to enhance the signal amplitude. As reported in [62, 76-78], designing adaptive systems could improve the performance of the whole transceiver, which is undoubtedly achievable in digital implementation.

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5.3   Driver architectures

There are different architectures proposed in the literature regarding how to generate high output voltage swing using low voltage processes [79-90]. In [79-83], an extended drain MOSFET (EDMOS) transistors have been utilized to enhance the maximum tolerable voltage across the output transistors. In [91] it has been shows that the breakdown voltage of this type of transistor in 65nm is about $V_{BR}=10V$. As a result, EDMOS devices are quite practical to generate high output voltage swings. Fig. 5-4a, b show the structure and the symbol of the EDMOS transistor. As can be seen, the drain of the transistor is separated from the gate terminal with an N-Well layer. Because the oxer layer at the drain side of the transistor (high voltage side) is thicker than the oxer layer over the channel, the gate-drain oxide break down does not limit the operation of the circuit. Due to the resistance associated with the N-Well layer in the EDMOS structure, a resistor (R_d is placed in series with the drain terminal). As an example, the R_{DS-ON} of an EDMOS in the 180nm process is about $60m\Omega/mm^2$ [92]. Although increasing the output voltage swing by utilizing EDMOST transistor seems to be a promising method, fabricating a custom made transistor in a regular CMOS process requires a separate transistor design that makes the design quite complicated and time consuming. As a result, in this project this type of implement has not been considered.
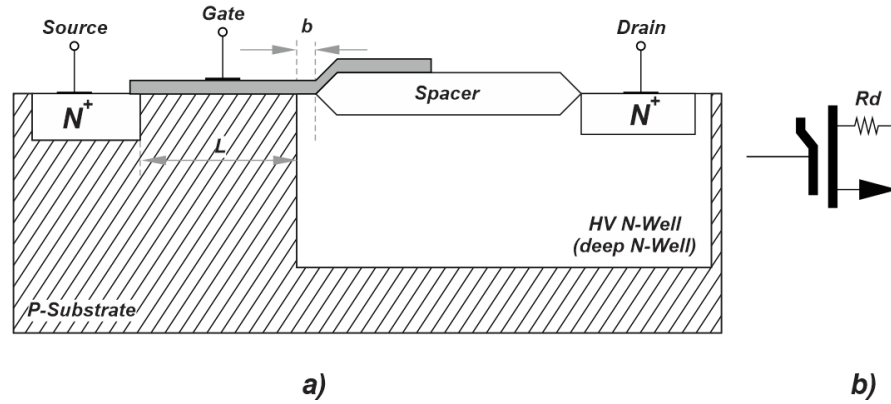
Fig. 5-4, EDMOS transistor a) device structure, b) transistor symbol

In [93], a cascode structure has been used in order to tolerate high supply voltage value by spreading this voltage among the drain-source terminals of the transistors. The entire cascode structure has been used as a stand-alone PA to drive a $R_L=50\Omega$ load impedance. Although this architecture can tolerate up to $V_{DD}=6.5V$, the gate terminals of the cascode transistors need separate bias circuitry. This architecture is shown in Fig. 5-5. The input and output matching networks have been implemented with the T-lines to the 50Ω load. The maximum delivered output power and efficiency at f=1.9GHz are $P_{out}=29.4dBm$ and PAE=41.4%.
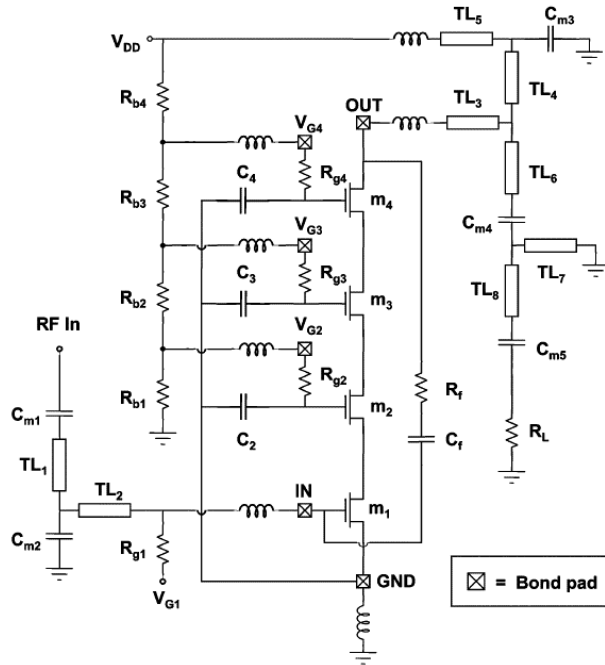
Fig. 5-5, The cascode driver architecture with external biasing on the gates

In [85-88], a new cascode architecture has been proposed that that uses on-chip resistive ladder to generate the gate voltages. This architecture, which is shown in Fig. 5-6, has been implemented in 45nm SMOS SOI and achieved P_{out}=24.3dBm, PAE=14.6% with R_L=50Ω at f=45GHz with V_{DD}=5.1V. A new architecture to generate high output voltage, which is named as house of cards (HoC) architecture is proposed in [89, 90]. This architecture is shown in Fig. 5-7. As illustrated in Fig. 5-7, the transistors at the top and bottom edges are used to connect the output load to the maximum and minimum voltages available in the circuit. This design has been implemented in 65nm bulk CMOS process at 720MHz for a R_L=50Ω. In this project, in order to verify and compare the performances of the drivers, the cascode and house of cards designs have implemented on the same chip.
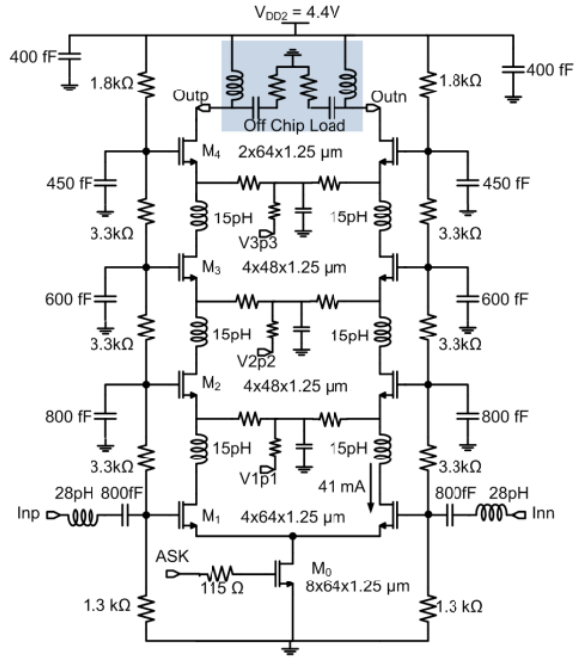
Fig. 5-6, The differential cascode structure
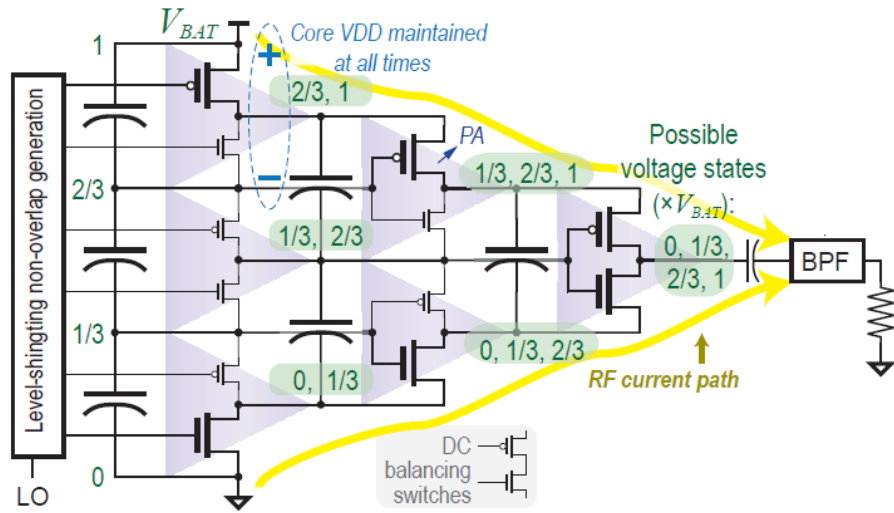
Fig. 5-7, The house of cards architecture

5.4   House of Cards (HoC) analysis and design

The main HoC circuit diagram is shown in Fig. 5-8. The modulated signal connects to the input buffer in order to enhance the driving capability to the HoC architecture. Since the main supply splits among 4 different stages, the supply voltage of this buffer is set to $V_{DD}=1.25V$, which is ¼ of the main supply voltage ($V_{DD}=5V$). The size of the input buffer is set such that it is able to drive 1pF load with about $T_{r,f}\approx12ps$ ($W_{tot}=288\mu m$). This figure shows the ideal and post extracted simulation results of this block. As can be seen the buffer enhances the rise and fall time of the input signal ($T_{r,f}$ input$=20ps$).
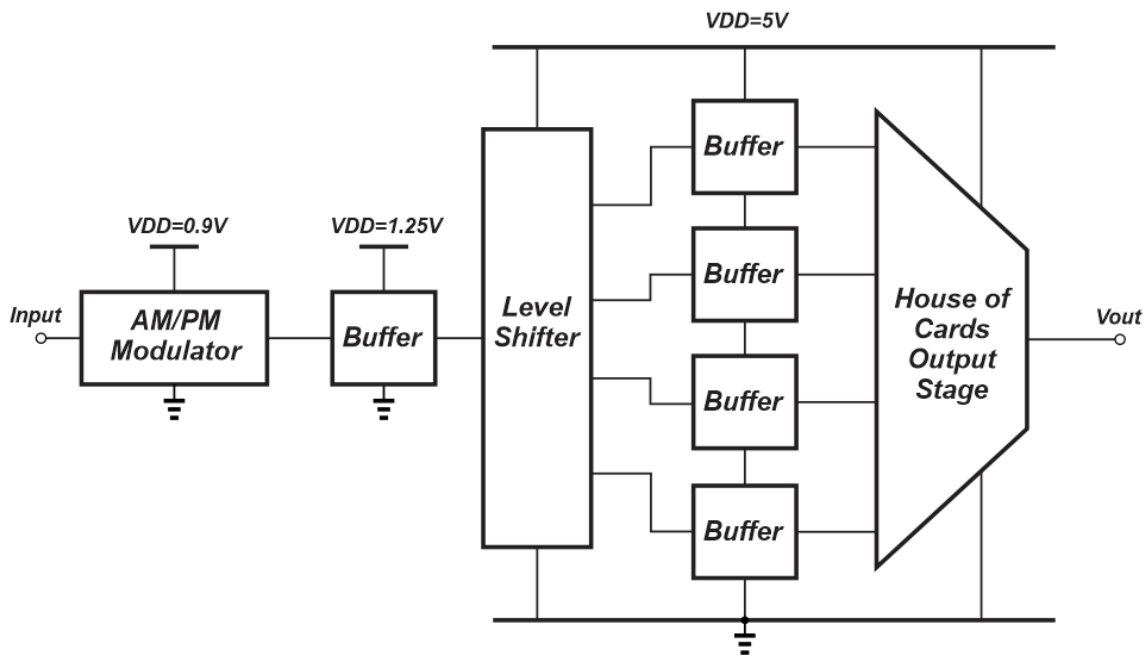
Fig. 5-8, The full house of cards architecture

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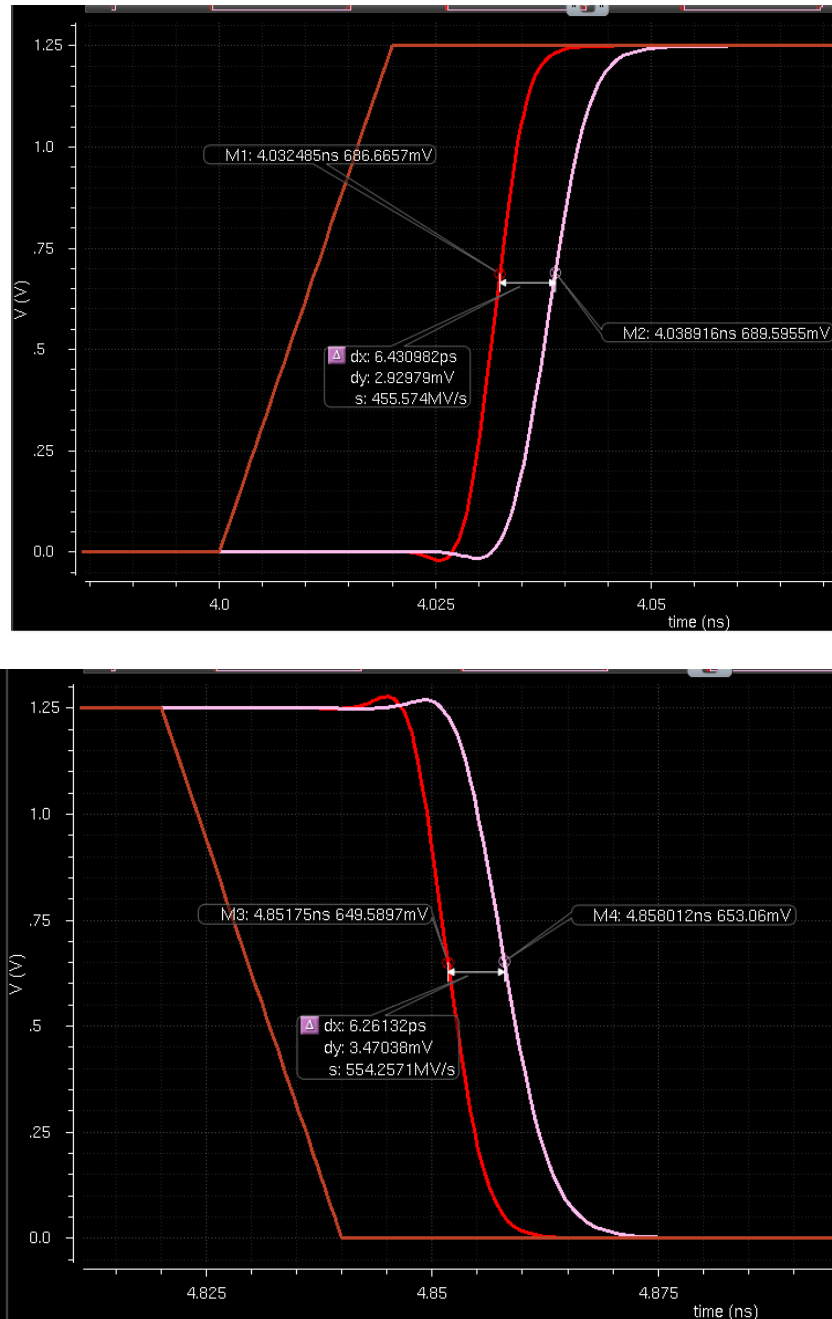
Fig. 5-9, The ideal and post extracted transient response of the input buffer stage

As shown in Fig. 5-8, the HoC structure requires a level shifter block. Different

types of level shifters (LSH) have been proposed in the literature [94-98]. In [94] a new

LSH architecture has been proposed in HV CMOS process with V_{DD}=10V that generates

3.5V output voltage swing between 6.5V and 10V. This architecture relies on a memory

based structure in order to keep the output voltage at a constant value for an arbitrary

about of time. However, since some of the transistors in this architecture need to tolerate

high voltage across their drain-source terminals, in this architecture EDMOS transistors

have been used. Additionally, the maximum voltage achieved in this design does not

exceed the maximum allowable voltage in the process. Furthermore, the output response

speed is in the range of nano-second that is not suitable for this project. The required

speed in this design (in the range of $T_{r,f}=20$ to 50ps) prevents using the structures

proposed in [95-98]. Therefore, in this design, in order to reduce the difficulties

associated with the active LSH, a passive level shifter counterpart has been used [99].

Fig. 5-10 shows the architecture of this level shifter.
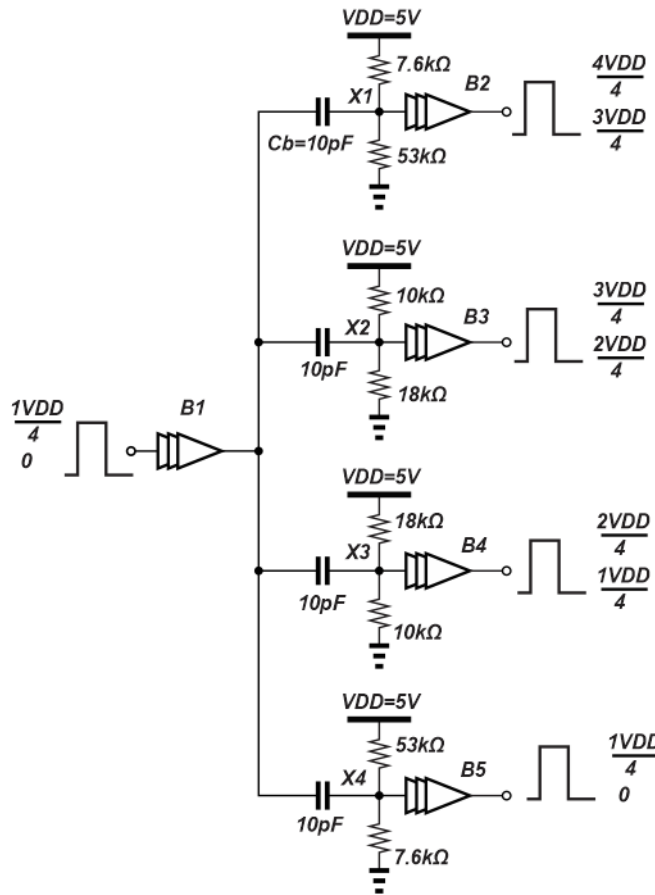
Fig. 5-10, The second stage buffer

The resistors dividers are set such that the DC voltage level at the input of the buffer stages have a correct swing around the level shifted values shown as rectangular signals at the output of the buffers. Also, in order to minimize the DC power dissipation, the resistors are set to large values. Another design parameter is the series capacitors (C_b shown in Fig. 5-10). The value of the coupling capacitors is set based on the input capacitance of the next stage (buffers). Since the input capacitance of the next stage buffer is about $C_X \approx 200fF$ (in Fig. 5-11), the coupling capacitor values must be set such that the voltage drop across them is negligible compared to the input signal ($V_{in}=1.25V$). As a result, the coupling capacitors are set to $C_b=10pF$. $\Delta V_X = \Delta V_{in} \frac{Cb}{Cb+Cin} = 1.25 \times$

$\frac{10pF}{10pF+0.2pF} = 1.22V$, which is high enough to turn on and off the next buffer stage.
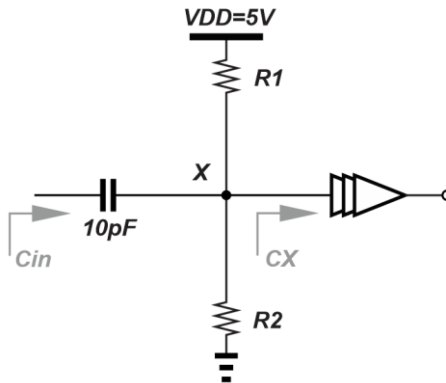
Fig. 5-11, The integrated level shifter and input capacitance of the next stage

Since each buffer stages (B_2-B_5) needs to generate a rectangular output signal around a level shifted supply value, a capacitive voltage divider is placed across each of the buffers. Fig. 5-12 shows the schematic of this architecture. The capacitor values are set such that the buffers are capable of driving the next stage (first stage of the HoC structure). Additionally, in order to ensure the voltages across all the capacitors are equal, R=14kΩ resistors are placed in parallel with each of the local decoupling capacitors. The

simulation results of this stage is shown in Fig. 5-13 through Fig. 5-15 for 500MHz,

1GHz and 2GHz input signal and as can be seen the level shifter operates correctly.
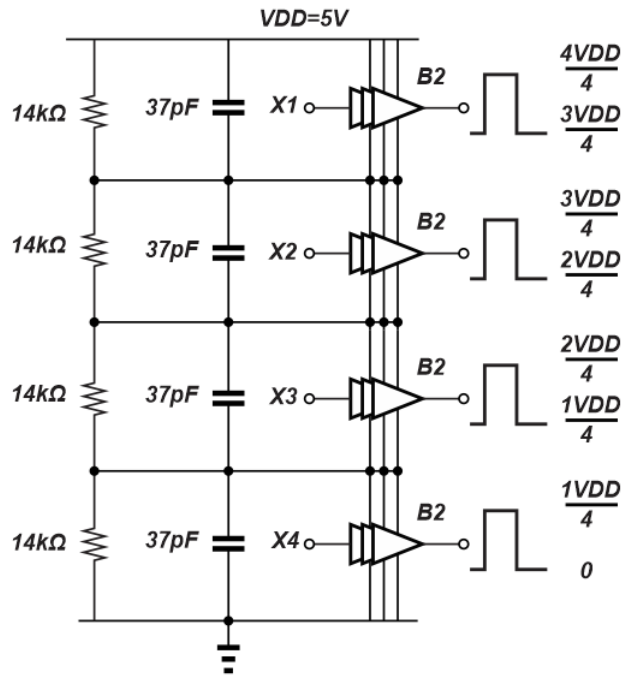
Fig. 5-12, The four cascoded buffer stages
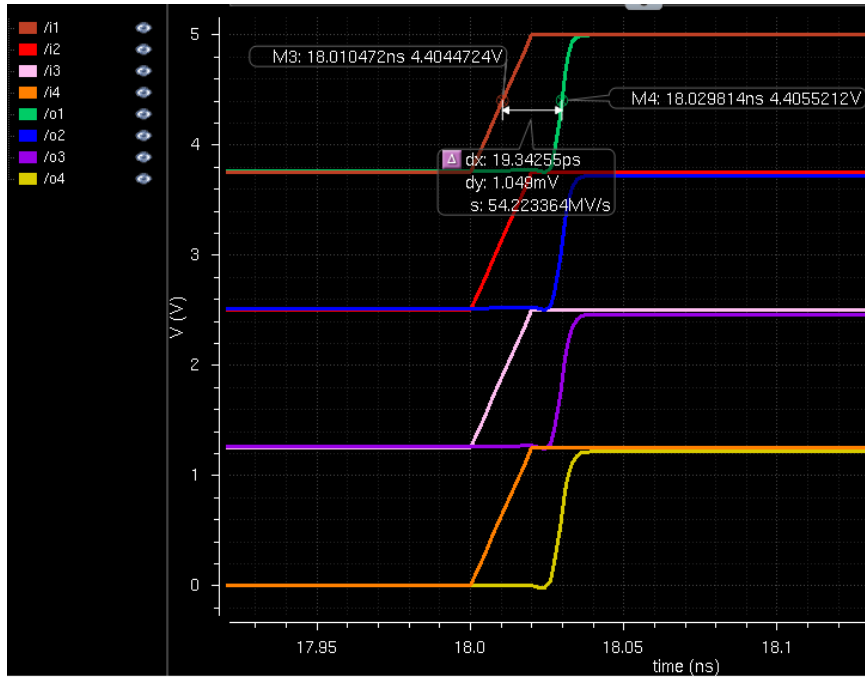
Fig. 5-13, Simulation results of cascode buffer stages
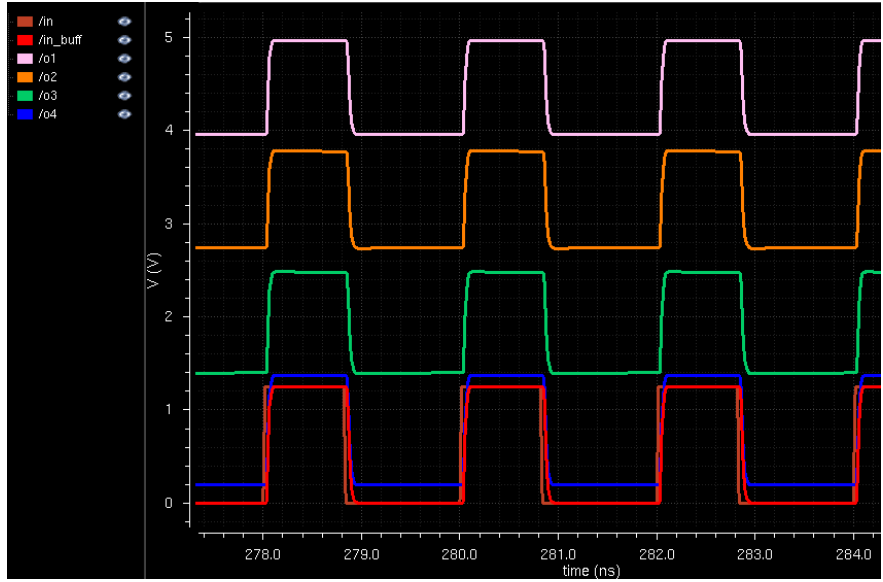
Fig. 5-14, The level shifter simulation results at 500MHz
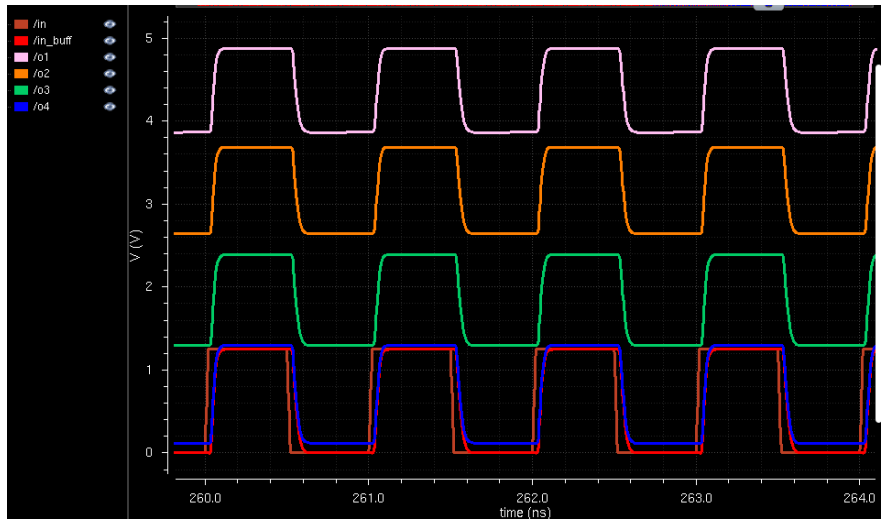
Fig. 5-15, The level shifter simulation results at 1GHz
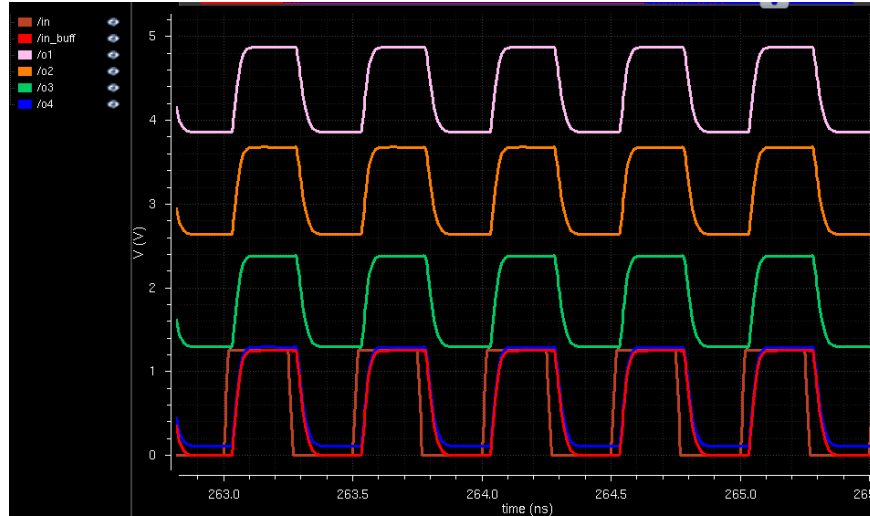
Fig. 5-16, The level shifter simulation results at 2GHz

The HoC circuit is shown in Fig. 5-17. The fixed voltage values at the middle of the HoC structure are made via capacitive dividers similar to the LSH stage (C_{divier}=6.7pF, R=100Ω). Each of the unit blocks, which is shown with the shaded dashed area, operates as an inverter and connects the local supply and ground (source node of the PMOS and NMOS transistors) to the local output node. As a result, each of the local inverter blocks only operates within the V_{DD}/4 supply voltage range and they are safe in terms of maximum tolerable voltage. The sizes of the transistors are set such that the R_{DS} of the transistors is small enough (R_{DS}≈100mΩ) to maximize the speed of the driver as well as increase the drive capability of the stage (maximum output current). Across each of the local inverters there is a local decoupling capacitor in order to compensate any phase mismatch between the signals ($C_{dec-local}$=2.4pF).
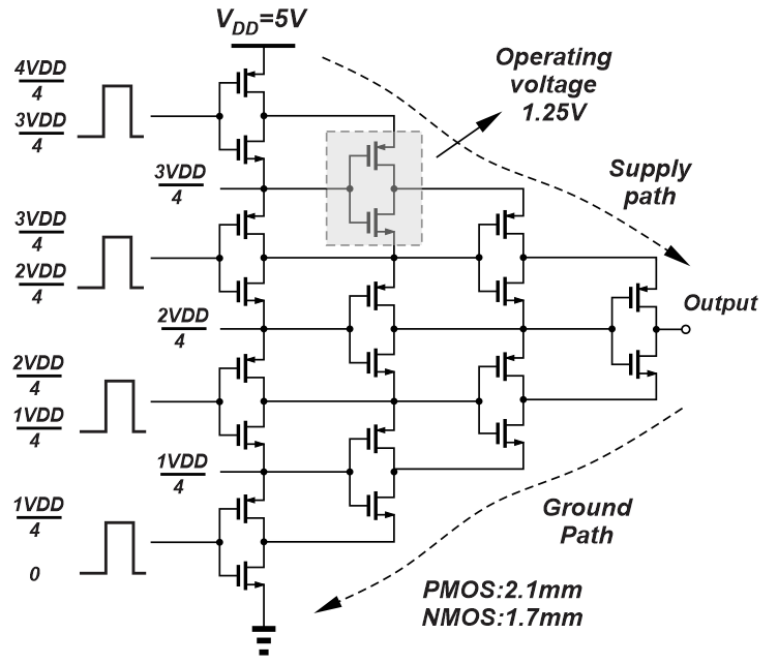
Fig. 5-17, The main house of cards structure

The operation of this system is shown in Fig. 5-18 and Fig. 5-19. When the input signal is at logic low, all the NMOS transistors are at the OFF state and the PMOS transistors are at the ON state. In this situation, the PMOS transistors at the top edge of the structure connects the output node to the supply voltage. Note that the entire structure acts as an inverter circuit and when the input signal is at logic low state, the output node is at the logic high. The next state is when the input signal is at logic high. In this situation, all the NMOS transistors are at the ON state and the PMOS transistors are OFF. Therefore, similar to the previous state, the NMOS transistors at the bottom edge of the circuit connect the output node to the ground. Fig. 5-20, Fig. 5-21 show the simulation results of the full circuit at 1GHz and 2GHz input signal frequency when the circuit is loaded with 5pF load. It is quite clear that the output signal has ΔV_{out}=5V swing and the rise and fall time of the output signal is $T_{r,f}$≈20ps.
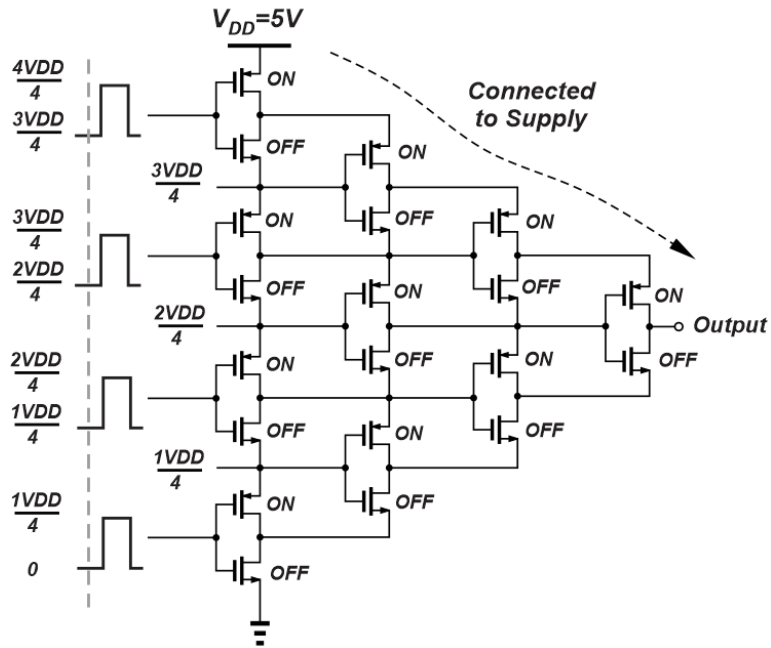
Fig. 5-18, The house of cards transistor states when the output is connected to high value
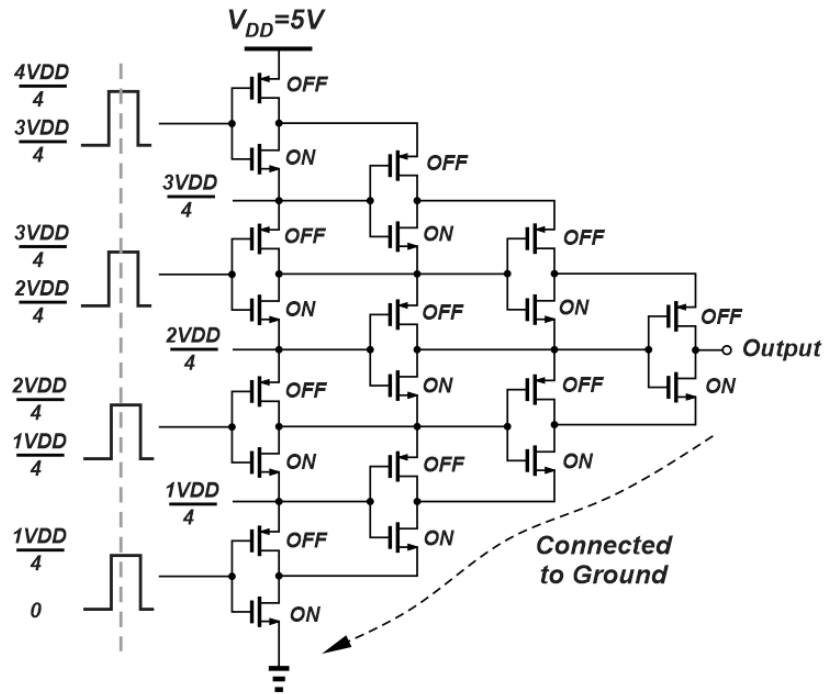
Fig. 5-19, The house of cards transistor states when the output is connected to low value

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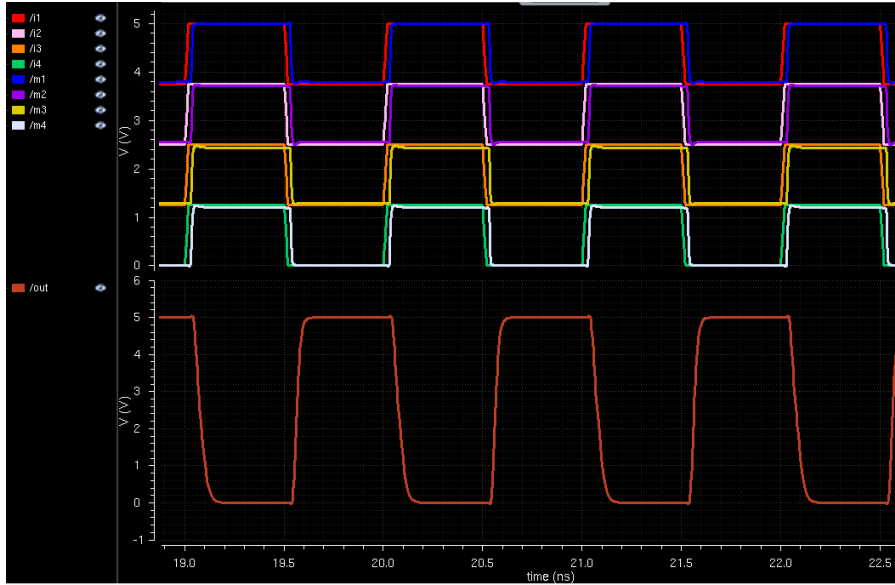
Fig. 5-20, The house of cards output simulation at 1GHz
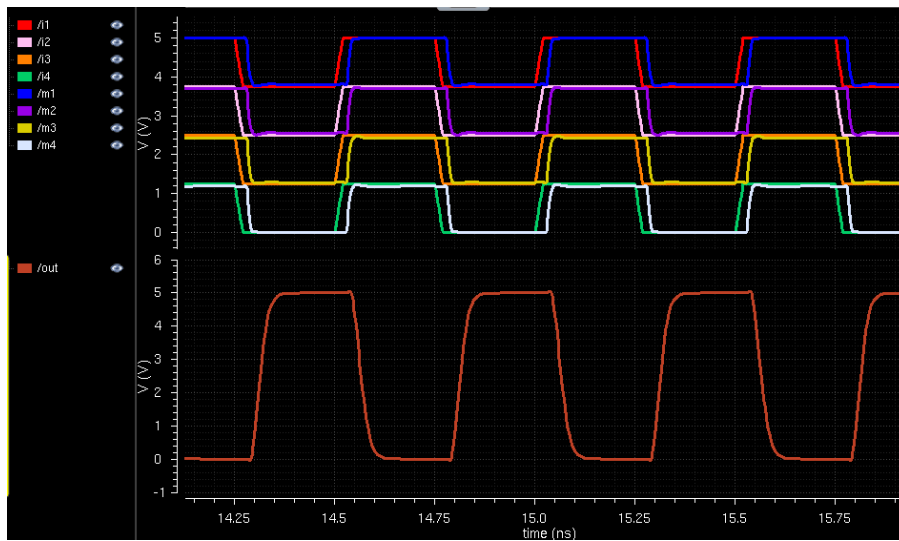
Fig. 5-21, The house of cards output simulation at 2GHz

In order to ensure the safe operation for all the transistors in the circuit, Fig. 5-22 shows the voltages across all the transistor's terminals in the circuit. As can be seen, all the voltages are below 2V, which is the breakdown voltage of the transistors in this process.
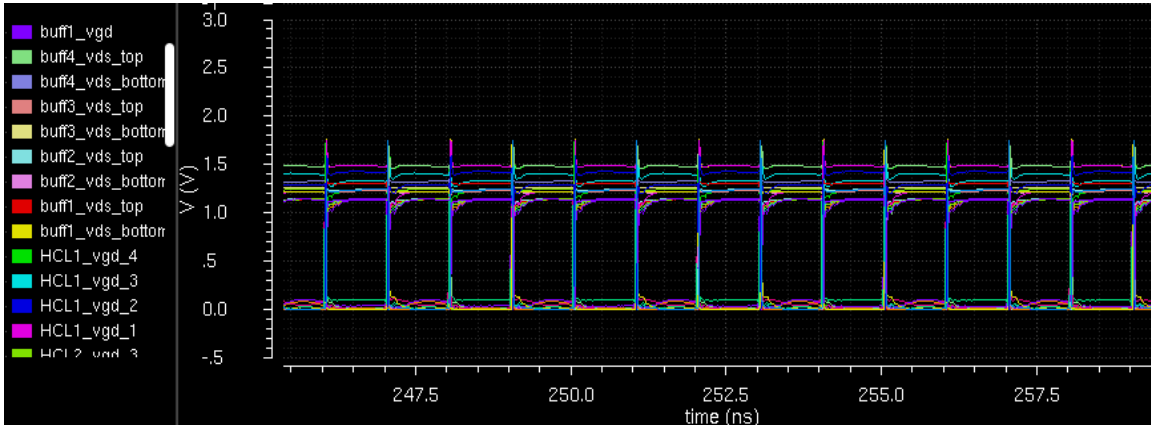
Fig. 5-22, The transistor's terminals voltage

To ensure the safe operation of the transistors in this process, a DC measurement has been done on a single device. Fig. 5-23 shows the I_D-V_{DS} as well as I_G-V_{DS} of the device when the device is at the off state ($V_G=0$). As can be seen, the subthreshold current that passes through the drain increases by increasing the drain voltage. A similar trend is observed for the gate current. Note that in this measurement the minimum size transistor has been used and the transistor length is set to $L_{min}=112nm$.
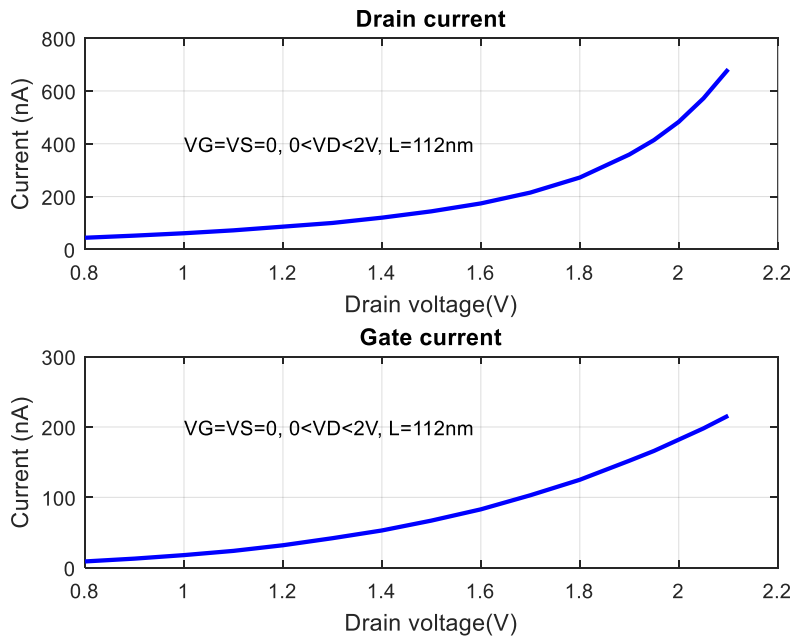
Fig. 5-23, CMOS SOI transistor drain and gate current as a function of the drain voltage ($V_G=0V$)

Fig. 5-24 shows the DC measurement of the transistor when the gate is biased at V_G=0.5V. It is quite clear that by increasing the V_{DS} the drain and gate currents increases similar to when the device is biased at sub-threshold. The ranges that the drain current increases when it is biased at V_G=0.5V is greater than the sub-threshold voltage. Therefore, this measurement clearly shows that the gate-drain oxide break-down is the main concern in 45nm CMOS SOI process. Note that this measurement repeated multiple times to ensure after each measurement the device is safe and operational.
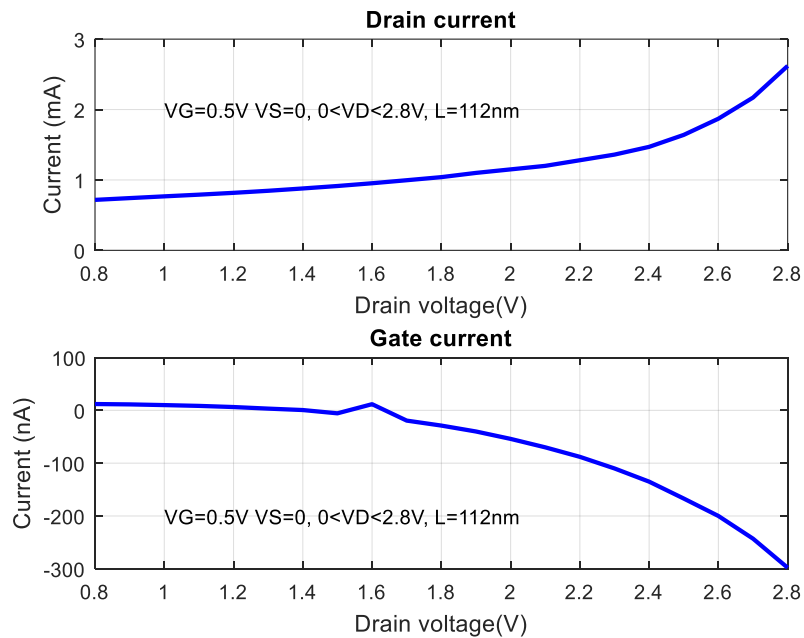
Fig. 5-24, CMOS SOI transistor drain and gate current as a function of the drain voltage (V_G=0.5V)

Since the RFPWM signal, which is in charge of generating amplitude modulation, changes the duty cycle of the signal, the driver performance must be checked at different duty cycle values. Fig. 5-25 shows the output signal at 50%, 40%, 30%, 20%. It is quite clear that the output voltage of the driver covers the full desired range of ΔV_{out}=5V and operational at all the duty cycles.
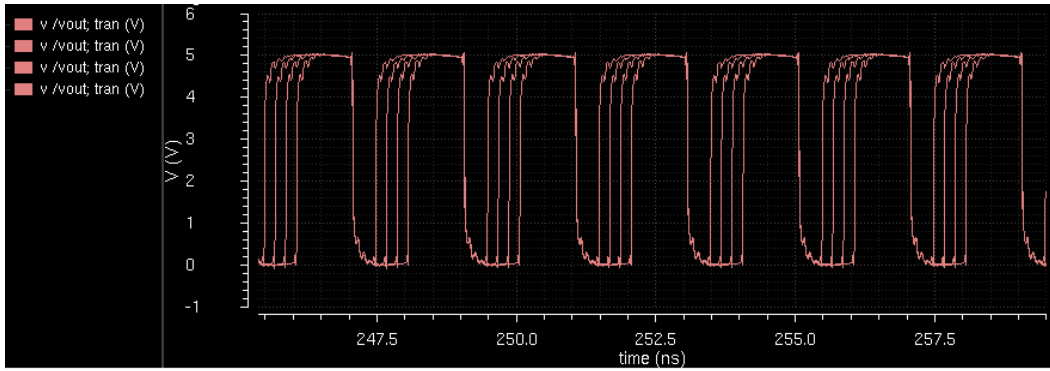
Fig. 5-25, The simulation reslts of the HoC structure for different input signal duty cycle

Since the transistor (CGH60015D) transient model is not available in the PDK, the input impedance of the transistor has been modeled by lumped components in such a way to mimic the same transient behavior as in the ADS transistor model. Fig. 5-26 shows the simulation setups that used for simulating the GaN transistor model and circuit models. The simulation results, which are illustrated in Fig. 5-27, reflect a close relationships between the actual GaN transistor and the lumped component model. Therefore, the lumped component model has been used in all the cadence simulations.
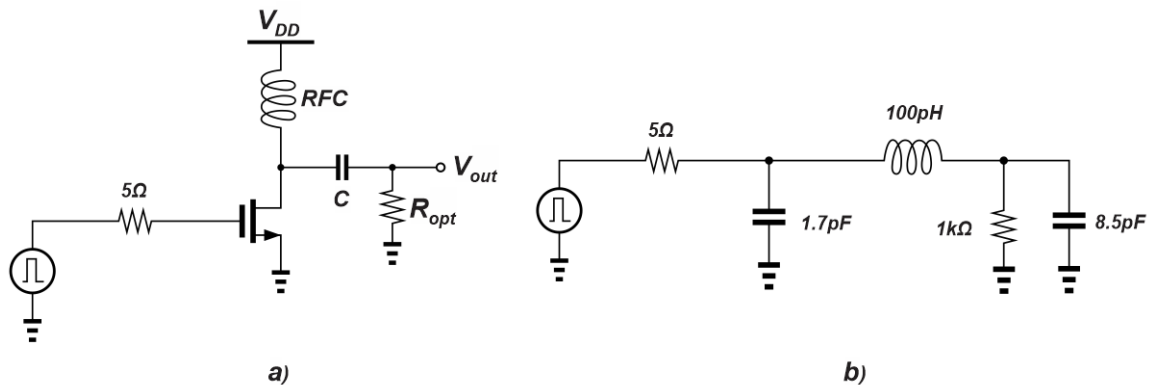
Fig. 5-26, GaN transistor modeling for transient simulation

There are two different methods to connect the CMOS driver to the GaN transistor that are shown in Fig. 5-28. The two transistors can connect directly to each other (die to die connection) or through the interface network on the PCB. Since the GaN

transistor is a depletion mode device, the DC voltage range that it requires is different from the DC value that the driver can generate (2.5V in this case). As a result, the DC level of the GaN transistor must be set separately. Therefore, an interface network has been placed between the driver and the GaN that is shown in Fig. 5-29. The simulation results of the voltage across the input node of the GaN device for different duty cycles (50%, 40%, 30%, 20%) are shown in Fig. 5-30. As can be seen, the gate of the GaN transistor experiences a suitable voltage to act as a switch.
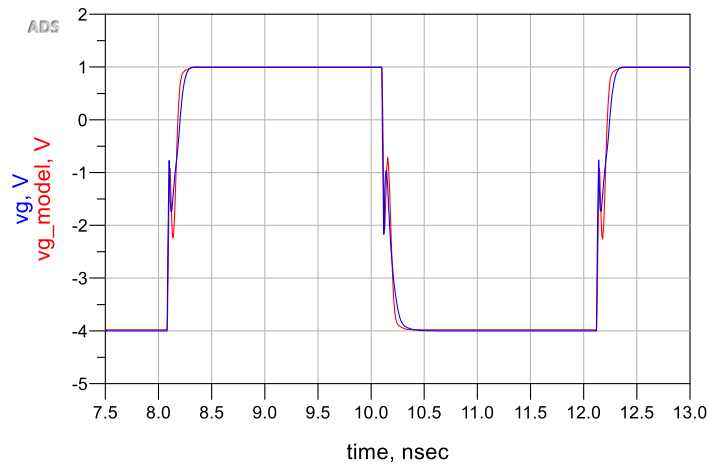
Fig. 5-27, The transient simulation of the actual GaN and the circuit model
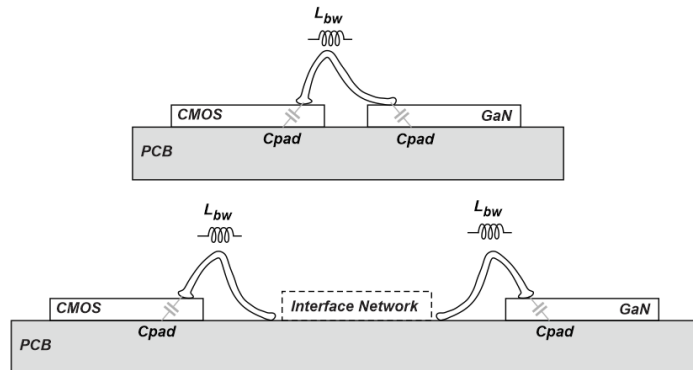
Fig. 5-28, The interface option for CMOS-GaN connection

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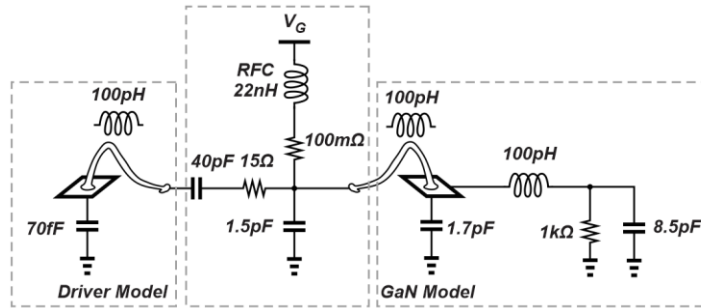
Fig. 5-29, The lumped component model used in the simulation
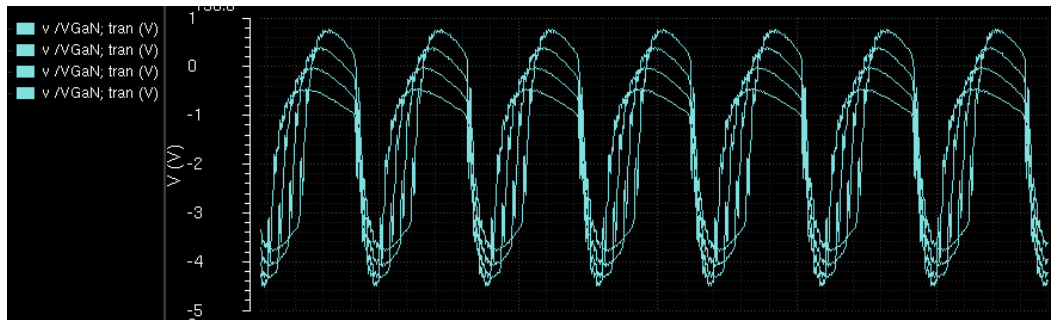
Fig. 5-30, The transient response of the signal at the GaN input node

Note that by changing the duty cycle of the input signal the DC value at the input node of the GaN transistor changes. This variation is due to the DC value variation in the Fourier transform of the signal. By analyzing the rectangular wave shown in Fig. 5-31with the duty cycle of "a", the DC value of the signal can be easily calculated. As can be seen, the DC value has a direct relationship with the duty cycle. As an example, a 50% duty cycle 5V signal has a DC value of 2.5V and if the duty cycle reduces to 20%, the DC value reduces to 1V. As a result, in order to maintain a correct DC operating point of the GaN transistor, the gate voltage must be adjusted according to the input signal duty cycle or the duty cycle should be limited, which degrades the data rate of the transmitter.

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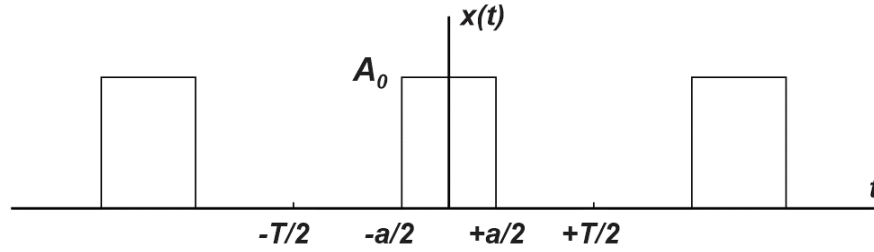
Fig. 5-31, A sample rectangular wave form for duty cycle analysis

$$a_n = \frac{2}{T}\int_{-T/2}^{+T/2} A_0 dt = \frac{2}{T}\int_{-a/2}^{+a/2} A_0 dt = \frac{2aA_0}{T} \tag{5-1}$$

$$DC = \frac{a_0}{2} = \frac{aA_0}{T} \tag{5-2}$$

5.5 Cascode analysis and design

In order to compare the performances of the driver, the cascode structure that proposed in [85-88] has been implemented. The cascode structure is shown in Fig. 5-32. This architecture acts similar to an inverter and connects the output node to the ground or the supply (V_{DD}=5V in this case). The resistors R_{1-7} are used to set the DC voltage levels at the gates of the transistors. The capacitors $C_{1,6}$ are used to connect the buffered input signal to the gates of the input transistors $M_{1,6}$. The rest of the capacitors shown in Fig. 5-32 (M_{2-5}) are placed in order to set the voltage swing on the gates of the transistor in order to keep the terminal voltages below the break down voltage in this process (V_{BR}=2V). When the input signal is high, the M_1 turns on while M_6 is off and vice versa. Similar transistor sizes have been used as in HoC structure to compare the performances of these two structures.

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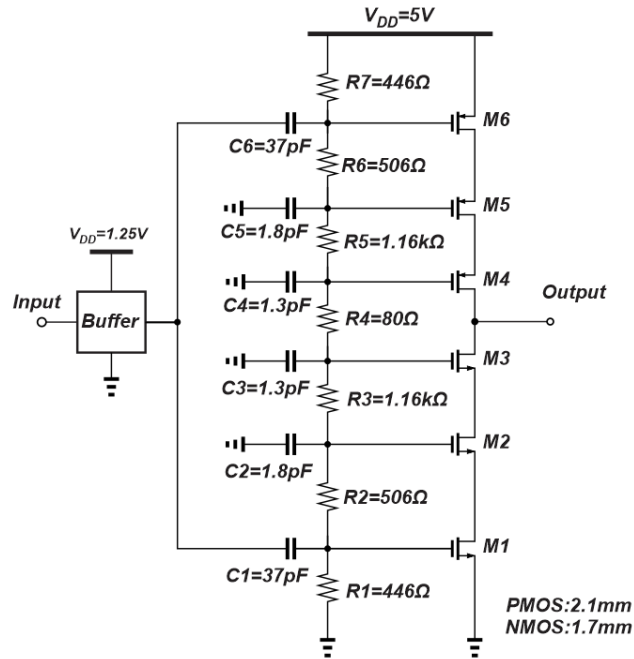
Fig. 5-32, The cascode driver architecture

Compared to the HoC, the level shifter in the cascode structure has been made via the RC ladder and as a result, the cascode structure has a quite simpler structure. Fig. 5-33 shows the input and output transient simulation results of the circuit. As can be seen, the circuit has a voltage swings from 0 to 5V and rise and fall time of about $T_{r,f}=20ps$. Fig. 5-34 compares the power dissipation of these two structures. It is quite clear that the HoC dissipates more power than the cascode structure and it is mostly because more digital blocks are included in this structure. The chip photograph of this design is shown in Fig. 5-35. The HoC consumes $0.48mm^2$ and the cascode structure consumes $0.13mm^2$. It is quite obvious that the Cascode structure consumes less than 1/3 of the HoC area. The entire chip has been fabricated on a $2\times2mm^2$ die with the $90\times90\mu m^2$ pad size.
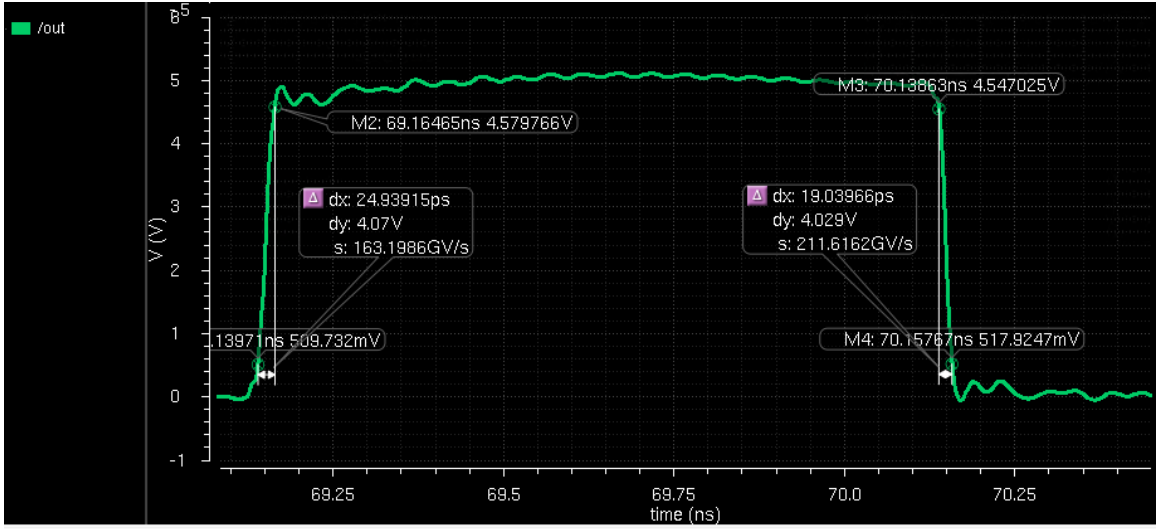
Fig. 5-33, The cascode transient simulation result
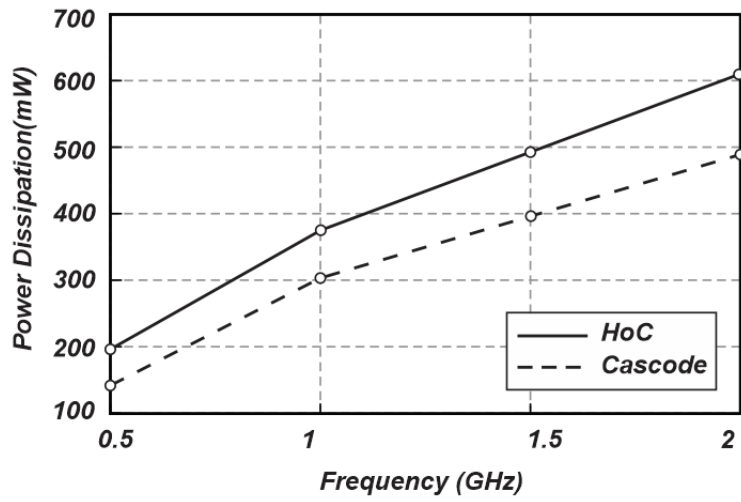
Fig. 5-34, Power dissipation comparison between the cascode and HoC architecture
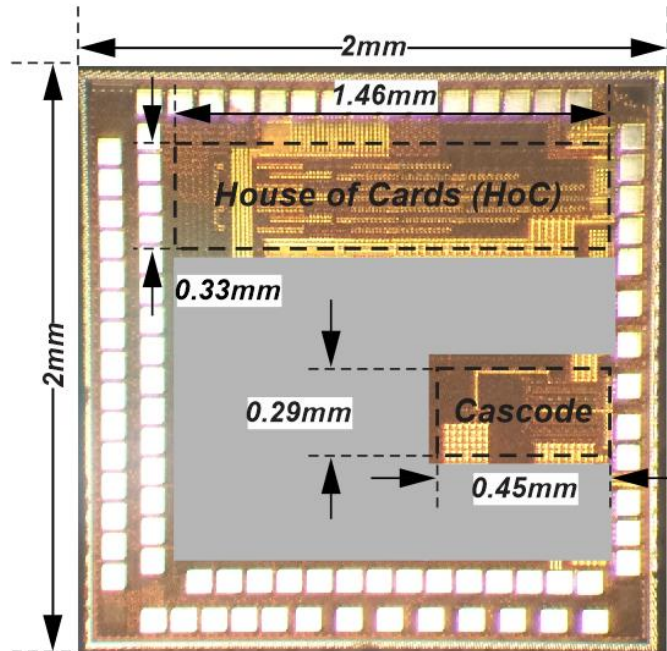
Fig. 5-35, The driver stages chip micrograph

Note that since in this process no serial to parallel interface (SPI) was available, parallel programming has been utilized and because of that high number of pads have been used. Since the die size is not high enough to cover the entire pads in one row, staggered pads have been utilized at the left and bottom sides of the die. In order to reduce the supply bondwire inductance and resistance, 10 bond wires are assigned for the supply (5V) and ground, and 4 bond wires have been used for low supply voltage (1.25V).

5.6   Interface Discussion

Before illustrating the simulation results of the interface circuit, the main difference between driving on-chip and off-chip capacitive loads must be studied. Fig. 5-36 shows a conventional inverter with an on-chip capacitive load (C_{load}). The input signal, supply voltage and ground are connected to the chip via bond wires (sometimes multiple bond wires place in parallel with each other). By considering the ground node on

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the PCB as the reference ground, the input signal generates a well-defined rectangular wave at the node "in". But the circuits on the chip has a different reference potential as the ground and supply (GND_{onchip}). As a result, in order to correctly measure the performance of the on-chip design, the circuit must be measured with respect to the on-chip ground potential especially when the frequency of operation is high and the bondwires change the performance of the generated signal on the die.
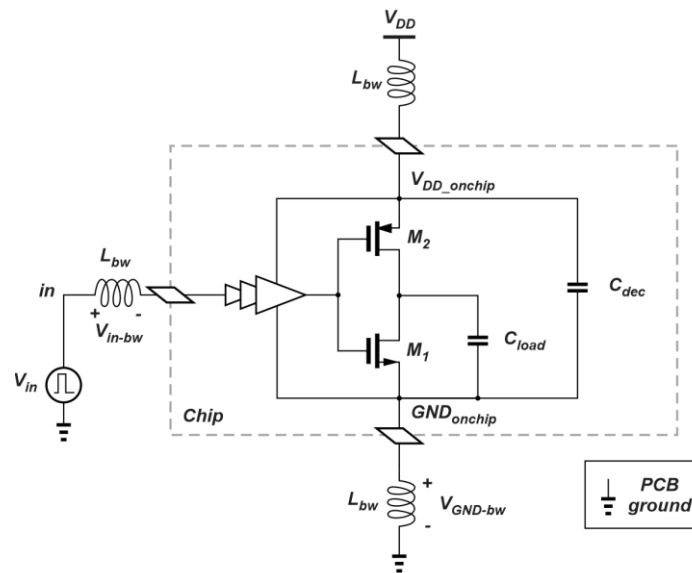
Fig. 5-36, A basic inverter circuit diagram including all the chip connection and decoupling capacitor with on-chip load

The other critical challenge that requires proper addressing in most of the digital circuitry is the switching currents to charge and discharge the load capacitance. Fig. 5-37a, b show the current's path and direction during charging and discharging process. During the charging process the PMOS transistor is on and the NMOS transistor is in the off state. As a result, the decoupling capacitor is placed in parallel with the load capacitor and shares charges with it until the same potential appears across them. During the discharging period, the NMOS transistor shorts two ends of the load capacitor and discharges it until there is no charge across the load capacitor. It is important to note that

as shown in Fig. 5-37, the decoupling capacitor provides current only during the charging process and it does not play any role during the discharge process. Since the decoupling capacitor is placed between the main supply and ground potential nodes, the DC voltage across it is set to V_{DD} through the bond wires.
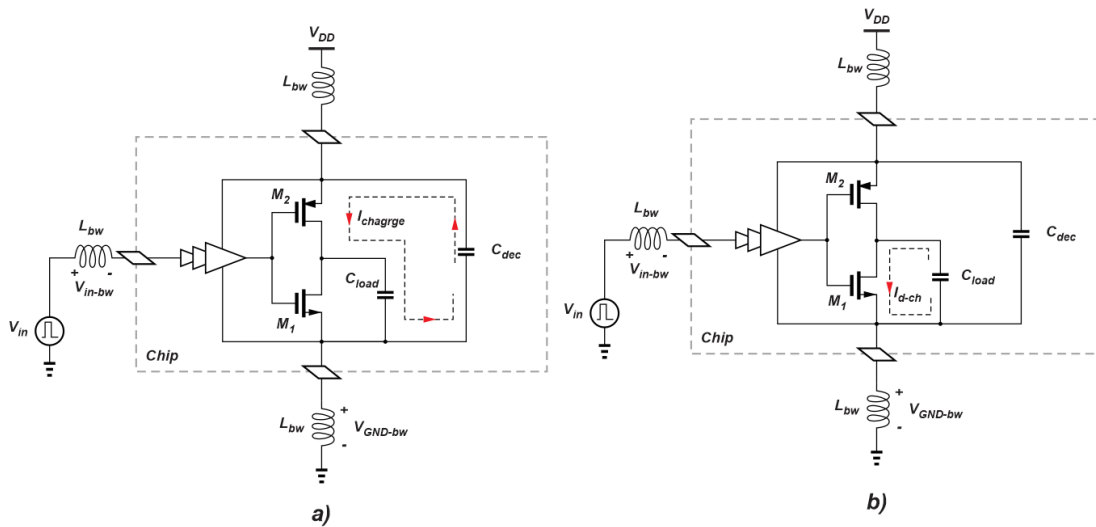
Fig. 5-37, The inverter transient current direction during a) charging and b) discharging process

This simple analysis reveals that the bond wires have no effect on charging and discharging of the output capacitor as long as the load is placed on the chip. It must be noted that the decoupling capacitor must be quite larger than the output load capacitor in order to have a proper operation (the charge sharing between these two capacitor should not change the voltage across the decoupling capacitor).

When the load is placed outside of the chip, similar to what is shown in Fig. 5-38, the voltage of the output load must be calculated/measured with respect to the PCB ground instead of the chip ground. Fig. 5-39a, b show the charging and discharging current's path when the load is placed off-chip.
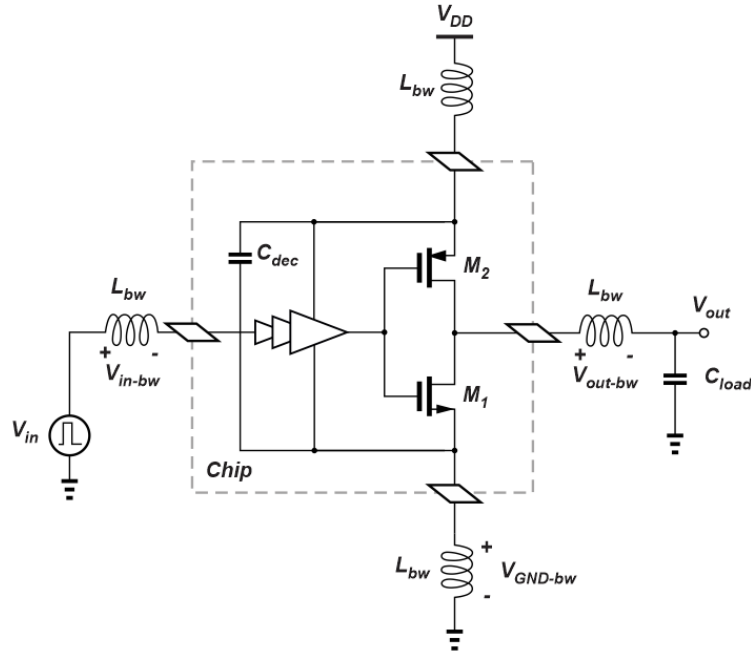
Fig. 5-38, A basic inverter circuit diagram including all the chip connection and decoupling capacitor with off-chip load
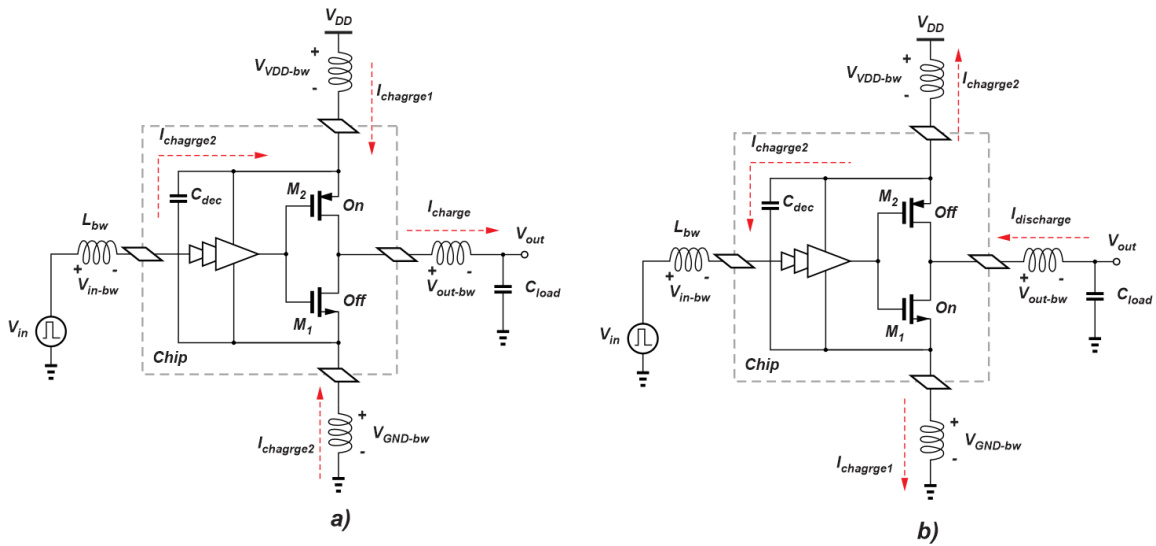
Fig. 5-39, The inverter transient current direction during a) charging and b) discharging process

During the charging process M_2 is on and M_1 is off. Some portion of the charging current that passes through the output capacitor (I_{charge}) comes from the supply bond wires ($I_{charge1}$) and some portion comes from the decoupling capacitor ($I_{charge2}$). Since the M_1 is off during this process, $I_{charge2}$ passes through the ground bond wire because the

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current should close the loop from the outside of the chip. Similar procedure happens during the discharging but with different current direction, which is shown in Fig. 5-39b.

There are three main challenges associated with this way of loading: 1) The output capacitor and the bond wires (load, supply and ground) create an LC network and if there is no damping element (ex. resistor) in this LC circuit, any excitations on the network leads to a never ending oscillation and prevents the circuit to respond correctly 2) the overshoots associated with the oscillations exceed the maximum allowable voltage across the transistors and break the gate oxide of the transistors 3) pulling a rectangular shape currents from the bond wires (supply and ground) create voltage across them and leads to a large Ldi/dt that can damage the transistors' gate oxide or punch through the drain and source terminals.

A simple way to resolve all of these issues is to place a damping element (a resistor in series with the load capacitance) in the circuit to prevent the oscillations. The series resistor changes the circuit behavior from an LC network into an RLC network and damps the unwanted oscillations. Although this resistor protects the transistor from breaking down, by damping the oscillations, it degrades the efficiency of the driver stage by dissipating some of the driver energy. In addition, the value of the resistor determines the speed of the driver since it sets the settling time of the RLC network.

Since the output load capacitance is actually the input capacitance seen from the GaN device (mostly the C_{GS}), placing a resistor in series with it is not practical when die to die wire bonding is required. As a result, both dies must be placed on the PCB and the damping resistor should be inserted between the dies. In case of die to die bonding, the

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only damping resistance in the circuit is the GaN transistor gate resistance and it determines the maximum speed.

Since the purpose of the design is to drive a capacitive load, the interface plays an important role in the transient performance. In order to analyze the effect of interface on the driver performance (speed) a simplified version of the CMOS driver has been simulated. Fig. 5-40 shows the driver model that has been utilized in this analysis. The driver stage is modeled with two switches ($SW_{1,2}$ with R_{on}=100mΩ, R_{off}=1MΩ), C_{dec}=150pF is used as the decoupling capacitor on chip, the supply is connected to the V_{DD}=5V through a 200pH bond wire inductance and 2Ω resistor (damping resistor at the supply) and 50pH bond wire inductance to the ground. Since only the variation of the output signal is of interest, a 30pF coupling capacitor has been placed in series with the driver output to block the DC path to the GaN transistor's model. A 70fF capacitor models the 90µm ×90µm pad capacitance on the CMOS chip. Since the ground potential on the chip is created via the ground bond wires (short bond wires), the pad capacitance is connected between the output node and the on-chip ground.
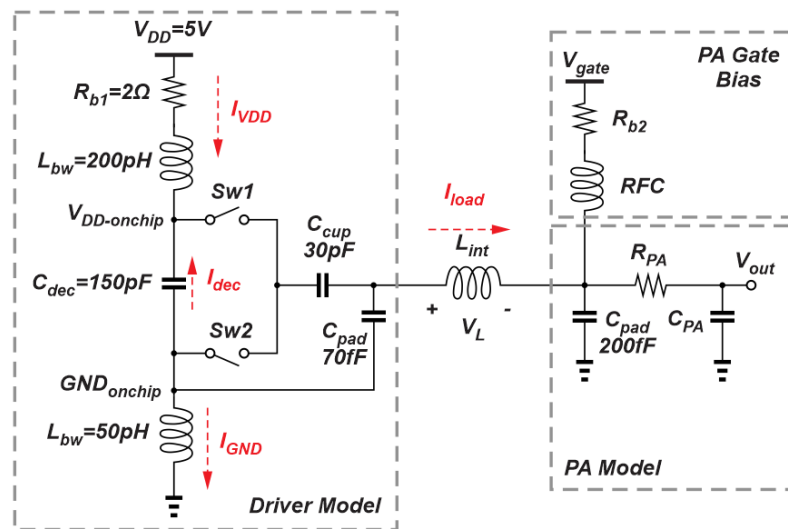
Fig. 5-40, A circuit implementation of a driver stage connected to a general switched mode PA

The output of the driver is then connected to the PA circuit (shown as PA model Fig. 5-40) via an interface bond wire (L_{int}). In order to provide the ability of setting the DC voltage level on the gate of the PA separately, the PA input is connected to the bias voltage (V_{gate}) through an RF chock (ideal RFC). The pad capacitance of the PA circuit is set to 200fF (an approximate value) and the PA is modeled with a series combination of a resistor and a capacitor (C_{PA}=3pF and R_{PA}=3Ω). C_{PA} is set based on the C_{GS} value of the transistor and the R_{PA} value is set based on the resistances on the gate paths of the GaN transistor. Note that if no resistance is placed in series with the output capacitance, the input pulse causes the output node to resonate forever. As a result, the GaN input resistance plays an important role in this analysis. Furthermore, if there is no resistor is placed in the supply path (in series with the supply bond wire), the supply and ground bond wires create an LC network with the decoupling capacitor and the entire circuit starts to resonate. Therefore, a 2Ω resistor is placed in this path and included in the circuit model. Fig. 5-41 shows the transient response of the output voltage as well as the voltage drop across the load bond wire (L_{int} in Fig. 5-40). It is quite clear that the output voltage has 5V voltage swing and satisfies the GaN transistor input voltage requirement. However, the overshoot appears on this node is about 2V (almost equal to the break down voltage of the CMOS devices) and can damage the devices. The voltage across the output bond wire is also quite large (almost 4V) and might damage the transistors. Fig. 5-42 shows the on-chip supply and ground potentials on the chip within the same time frame. As can be seen, the voltage variation on the on-chip ground node is more than 1V (the nominal voltage in 45nm CMOS SOI) and can affect the performance of the driver as well as the other digital section of the transmitter significantly. In order to prevent the

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high voltage across the integrated circuits, conventional ESD protection circuits or the architecture proposed in [100] can be used.
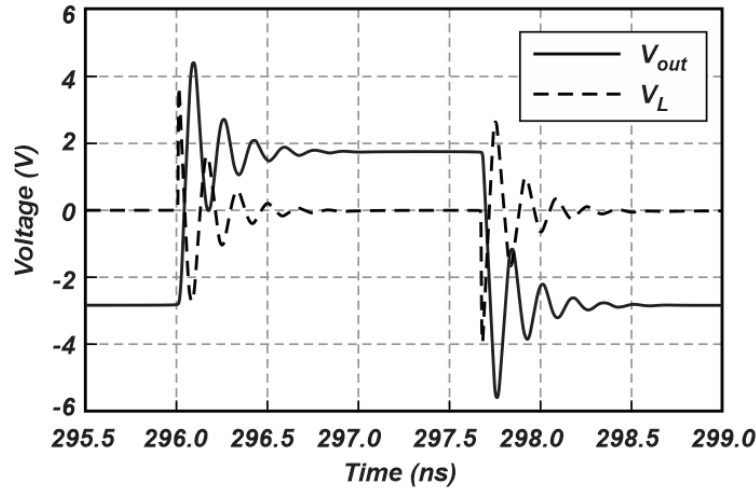
Fig. 5-41, Transient simulation result of the output voltage and the voltage across the output bond wire
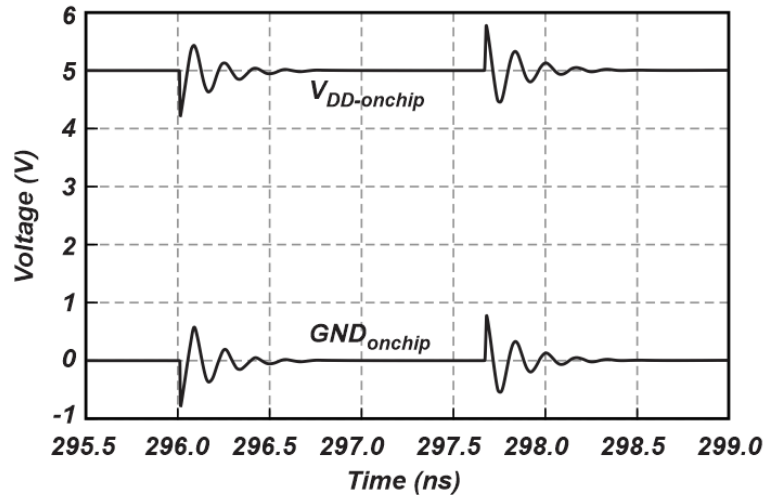
Fig. 5-42, Transient simulation result of on-chip supply and ground

Fig. 5-43 shows the transient current simulation in all the main branches. As can be seen, when the load is pulling current, the current passes through the decoupling capacitor and the ground bond wires. The same situation happens during the discharge process and most of the current passes through the decoupling capacitor and ground bond wires. The reason that most of the current passes through the ground bond wire is that the

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ground inductance values are much lower than the supply bond wires. Because the ground connections are made via quite short bond wires to the PCB substrate. Note that although the current passes through the supply bond wire is less than the ground bond wire ($I_{vdd} \approx 1/4 \ I_{GND}$), the amount of voltage appears across the supply and ground bond wires are the same. Under the condition shown in Fig. 5-40, Fig. 5-44 shows the maximum operating frequency of the driver for two different load capacitors (3pF and 4pF). Note that in this simulation, 20% settling time criterion has been considered.
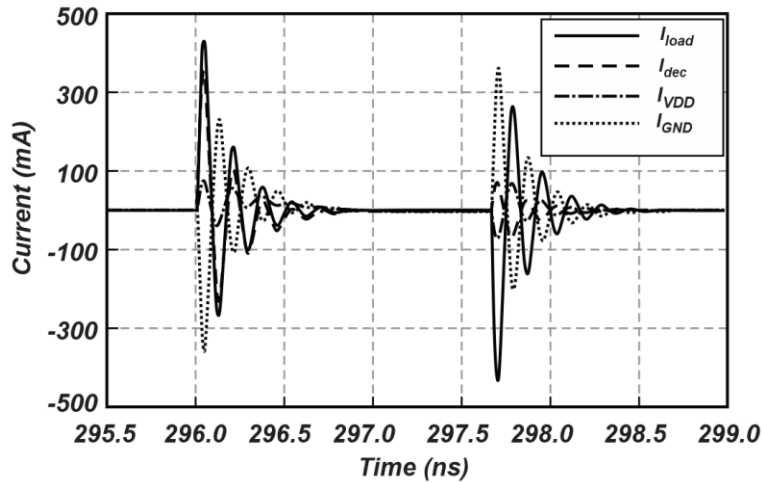
Fig. 5-43, Transient simulation result of the current that passes through the load, decoupling, supply and ground
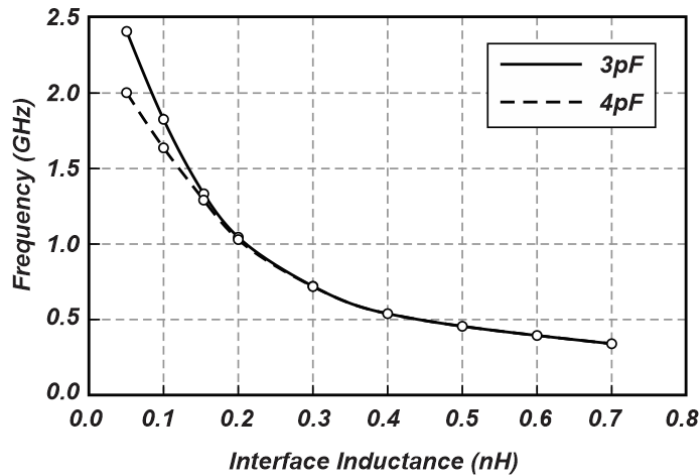
Fig. 5-44, Maximum frequency of operation as a function of load interface inductance for two different load capacitance

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When the interface bond wire is small, the circuit acts similar to the capacitive charging and discharging and as a result, higher frequency of operation is achieved [101]. When the interface bond wire inductance is high, the output node requires a long time to settle down and as a result the maximum operating frequency reduces. The exponential behavior of the circuit is explained well by considering the fact that the time constant of the RLC network has a direct relationship with the inductance ($\tau = 2L/R$) and by increasing the inductance, the time constant increases. As a result, the settling time increases and the maximum operating frequency decreases.

5.7   Board design

5.7.1   RF Track design

In order to test the performance of the circuit a PCB has been designed. Since the expected frequency of operation is limited to 2-3GHz, the FR4 material has been utilized and standard copper material has been used for the routings. The properties of the board material as well as the copper are given in Table. 5-1. In order to have a cost effective design and also have a reasonable RF line thickness, 2-layer board option has been selected.

Table. 5-1, The board specifications

Parameter	Value
Dielectric Constant (ε_r)	4.7 at 500MHz and 4.34 at 1GHz
Dissipation tangent (TanD)	0.017
Board Thickness	31mils (0.787mm)
Conductivity (σ)	5.95×10^7 (S/m)
Resistivity (ρ)	1.68×10^{-8} (Ωm)
Metal thickness (T)	1oz, 1.4 mil (35µm)

Due to the fact that the board requires to be connected to the spectrum analyzer for the measurement purposes, 50Ω tracks have been designed on the board. To enhance the bandwidth of the tracks and also provide isolation between them the coplanar wave guide (CPWG) has been used. The ability of placing matching network (using standard 0603 package component) in parallel with the RF tracks determines the Gap between the RF tracks (G=38.5mil=0.979mm). By using the calculated gap value, the width of the line for a Z_0=50Ω is W=54.46mil=1.38mm. Note that this line width should match the edge mount SMA connector (D=36mil=0.91mm) as well as the pad size of the SMD

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component (P=14mil=0.35mm). Fig. 5-45 shows the simulation result of the 50Ω tracks. As shown, the track characteristic impedance is well matched to 50Ω and the worst case insertion loss for an L=1.7"=42.6mm line at 10GHz is 1.2dB.
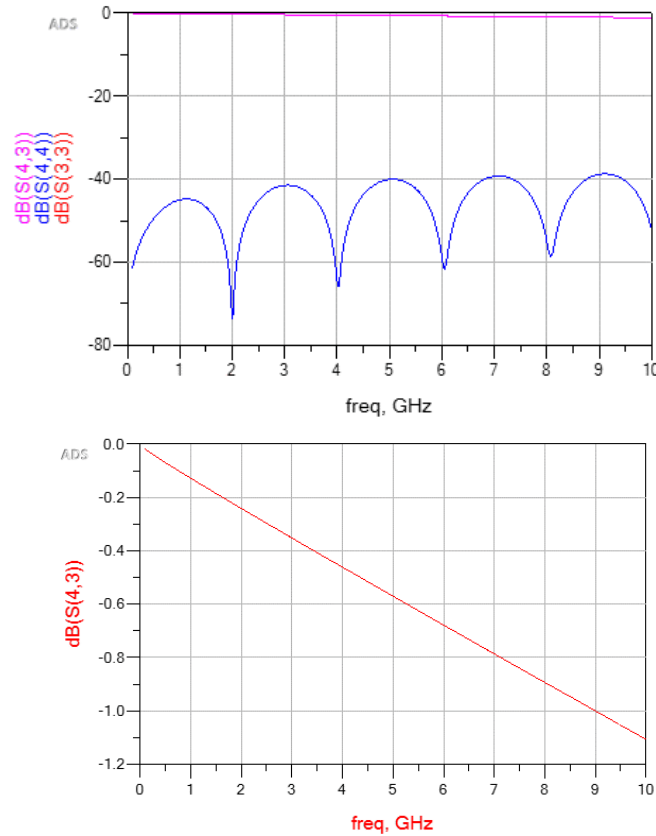
Fig. 5-45, The input return loss as well as the insertion loss of the RF-tracks

Fig. 5-46 shows the RF tracks on the PCB. As shown, all the RF lines are exposed with no color on them in order not to change the line characteristics and provide the SMD component placement ability. Additionally, all the RF lines are isolated from each other via ground planes on top and bottom of the board in order to reduce the cross talk and electromagnetic interference (EMI). Furthermore, the RF lines are designed to have the same length in order not to degrade the phase specification of the signal (L=1976mil).
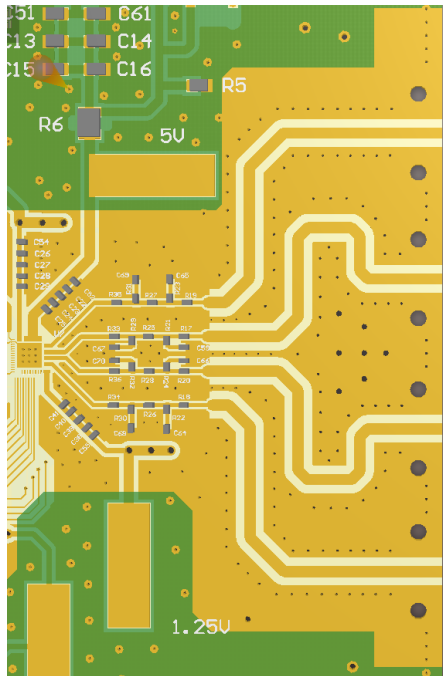
Fig. 5-46, The RF track section on the PCB

The 50Ω RF lines are connected to a network (as a matching network) in case any matching network is required during the measurement process. This network is designed such that it provides a 3rd order filtering on the signal if it is necessary. The matching network is connected to the die flag via W=20mil=0.508mm and G=10mil=0.254mm line. This physical dimensions on the T-line leads to $Z_0=63\Omega$ (S_{11}=-18dB), which is low enough not to degrade the overall output reflection coefficient significantly. The RF lines and PCB is designed highly symmetric in order to prevent the mismatch in the circuit that leads to phase distortion.

5.7.2   Die Flag Design

Due to the fact that some parts of the die needs to have staggered bond pads, similar arrangement must be set on the PCB in order to provide correct connection. Fig. 5-47 shows the pad configuration on the PCB. The main pad underneath the die is 3mm×3mm that is wide enough for the 2mm×2mm die (500µm gap at each side for down

bonding). The pad sizes at the left and bottom side of the circuit is set to 125µm×300µm that is suitable for wire bonding and the distance between them is set to 150µm. The distance between the staggered pads is set to 430µm based on the wirebonding requirement. The vias underneath the die are located such that the die covers all of them in order not to have any issue with the down bonding. In [102] a new technique to minimize the bond wire length has been proposed that is shown in Fig. 5-48. As shown, in order to reduce the length of the bond wire (reducing the inductance associated with them), the PCB has been placed in a trench inside the first layer of the PCB. Although this kind of chip-on-board implementation reduces the bond wire lengths, creating the trench inside the PCB makes the board fabrication quite expensive. As a result, in this design, the conventional die attachment has been used.
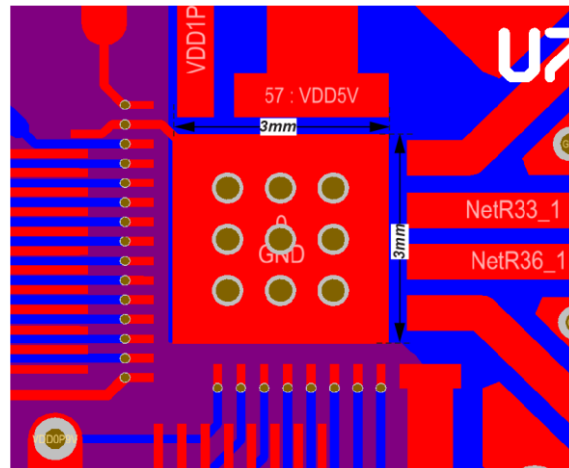
Fig. 5-47, Dimension of the die flag on the PCB
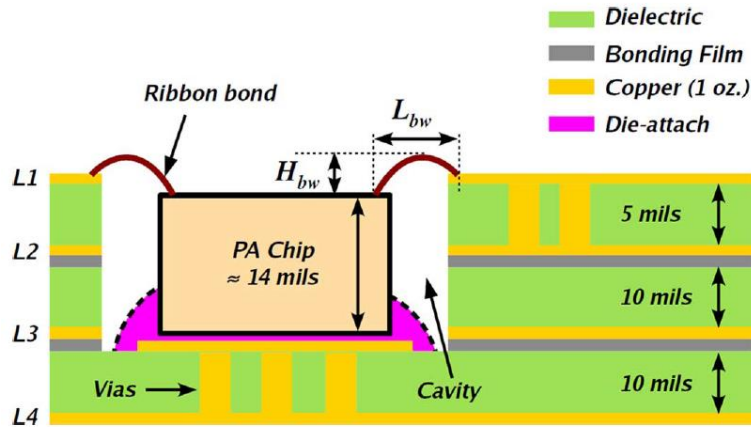
Fig. 5-48, The die attach configuration used in [102]

The wire bonding diagram of the die is shown in Fig. 5-49,Fig. 5-50. As shown in Fig. 5-49, at the top of the die, there is no staggered wire bonding and there are direct bond pad to bond pad connection. But the bottom side of the die has staggered bond pads and two rows of bond pads on the PCB have been used for these connections. In order to prevent the short circuit between the bond wires, the bottom row of the bond pads have moved to the left.
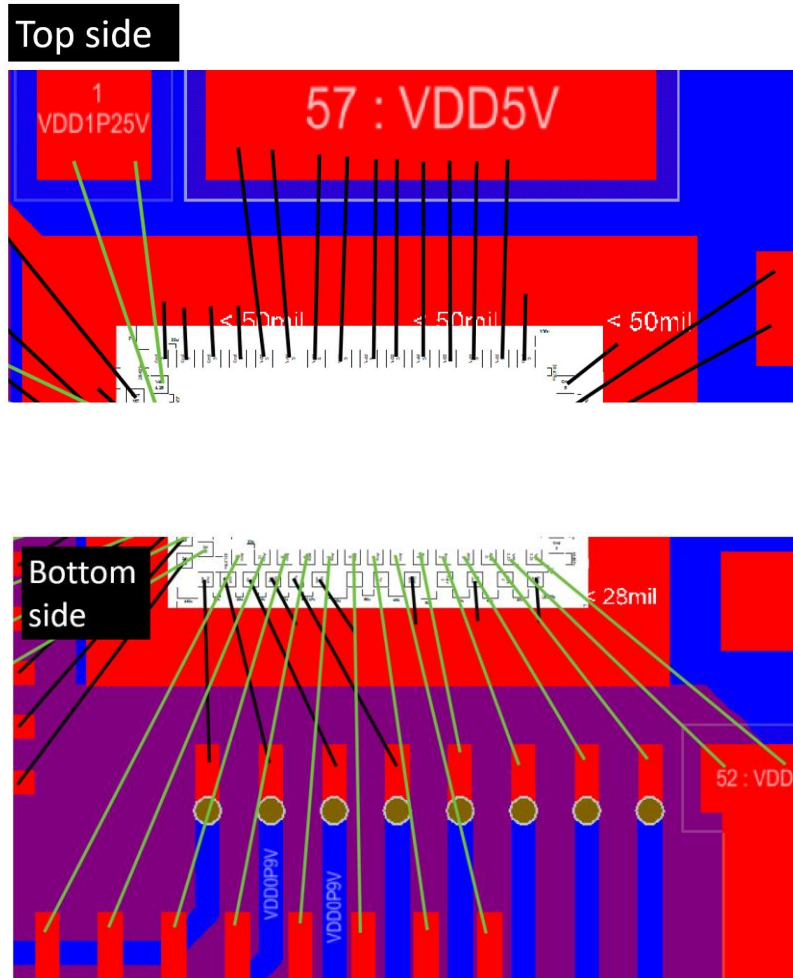
Fig. 5-49, The bonding diagram on the top and bottom of the PCB

Similar to the top side, the right side of the die has no staggered wire bonding and therefore, a simple diagram has been drawn for this section. However, the left side has staggered bond pads and two columns of bond pads on the PCB have been used for these connections. Since the programming frequency is at low frequency (in MHz range), no EM simulations have been done on the tracks and the vias.
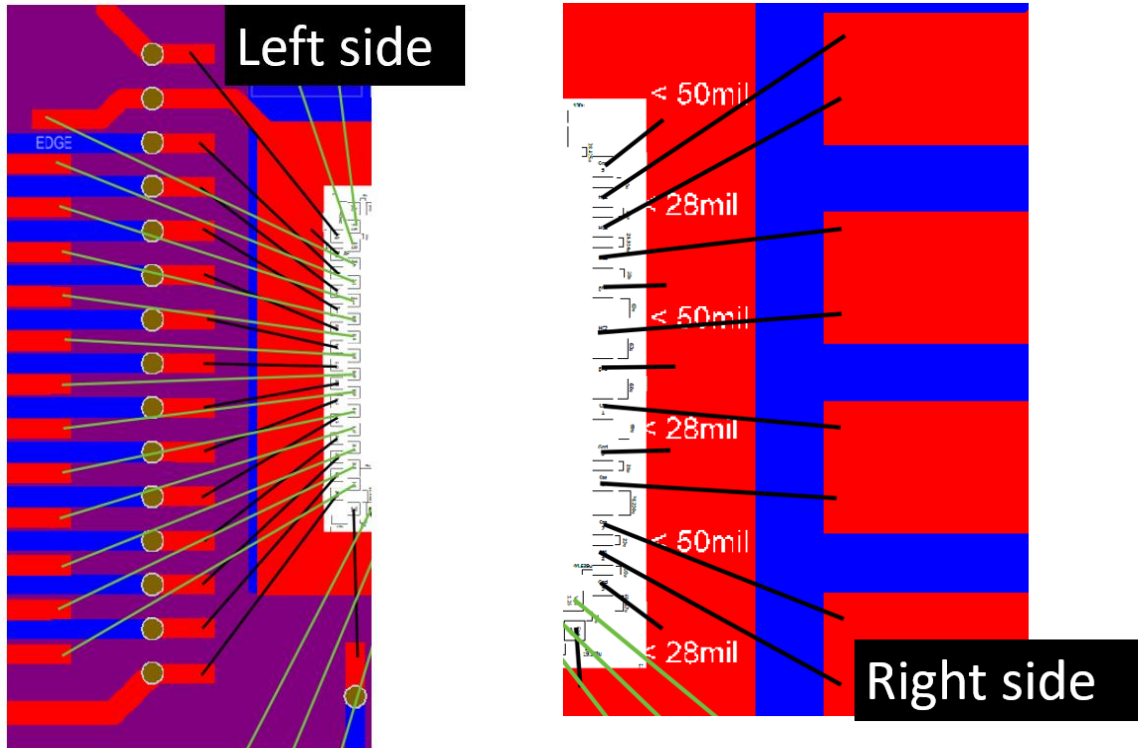
Fig. 5-50, The bonding diagram at the left and right side of the die

The clock signal of the digital programming that carries the edge information requires more isolation than the other data signals (amplitude and phase control signals). Therefore, more shielding has been applied on the "EDGE" signal. This track is shown in Fig. 5-51.
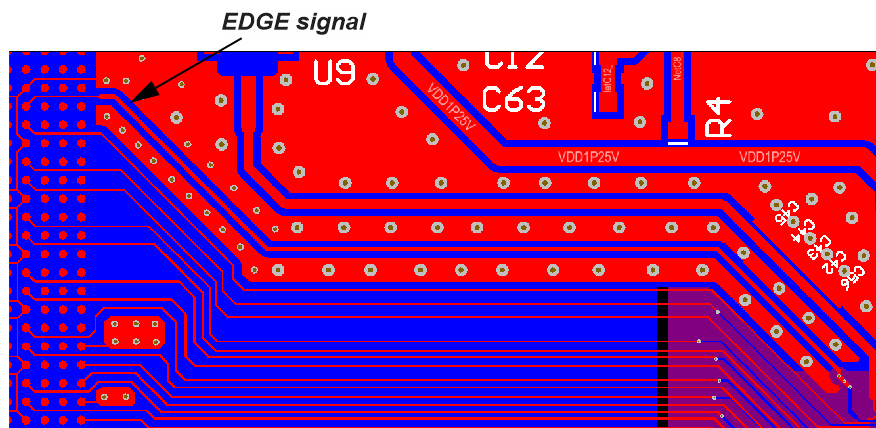
Fig. 5-51, The isolation around clock edge signal

5.7.3 Programmer connection

In order to generate the amplitude and phase modulated signal, a frequency synthesizer block has been implemented on the die. To generate the desired output signal with the correct amplitude and phase information, this block needs to be programmed via a digital programmer. In this design, the "KCU105" evaluation board has been used as an FPGA programmer. The FPGA connects to the PCB through a 400pin connector (ASP-134486-01 from Samtec). The orientation of this connector on the PCB is set such that the PCB and the FPGA evaluation board can be connected easily.

5.7.4 Full board configuration

The full board configuration is shown in Fig. 5-52,Fig. 5-53. As shown, the board size is about 14.4cm×13cm. The Die flag, interface network and the RF tracks are exposed in case there is any component assembly is required. In order to protect the chip, all the supplies are planned to raise gradually from zero to the desired values. As a result, adjustable regulators have been chosen. The main supply on the PCB is set to $V_{DD}=6V$, which is high enough to bias the regulators.
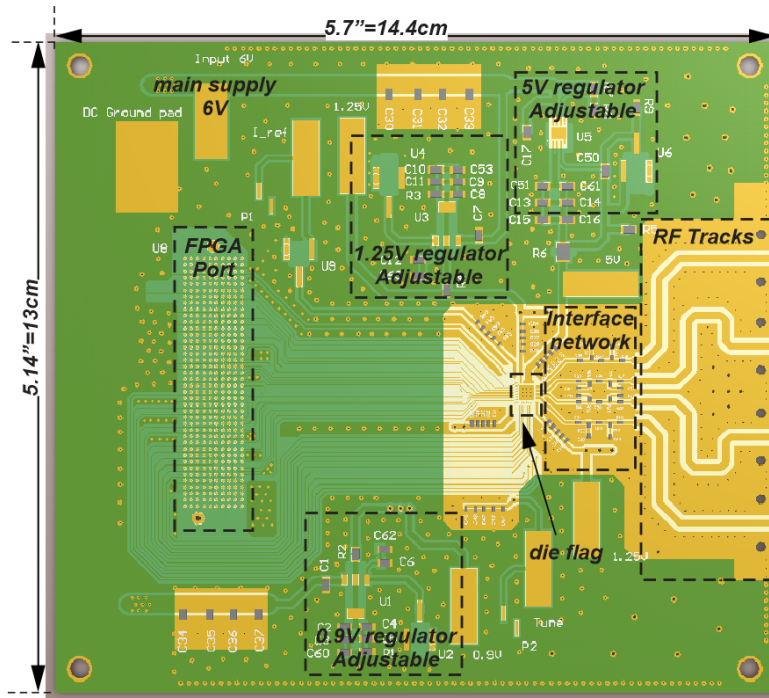
Fig. 5-52, The whole board configuration (Top view)
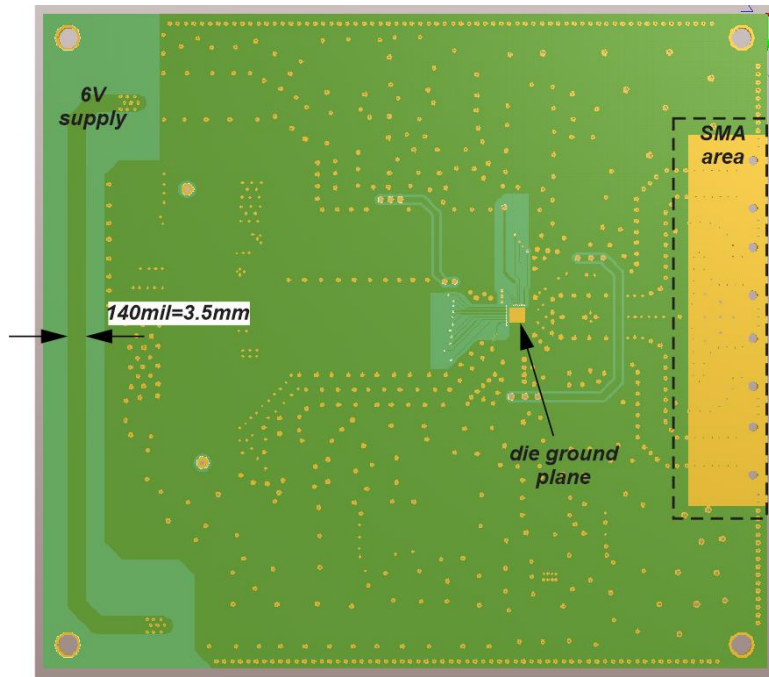
Fig. 5-53, The whole board configuration (Bottom view)

The main bias line (6V) and the output of the regulators are decoupled to the

ground with multiple range capacitors in order to remove all the unwanted signals and

noises. Also, more rooms for extra decoupling capacitor assembly has been considered in case the supply signal is not clean enough and more filtering is required. On the RF line section, the top and bottom side of the board are left exposed in order to mount the SMA connector. To reduce the EMI and cross talk between the RF lines they are all well isolated via ground planning and ground vias. Additionally, the edge of the board is totally isolated by placing ground vias around the board that connect the top and bottom of the board to eachother. The main bias line is thick enough to minimize the voltage drop across it (W=140mil=3.5mm). To reduce the noise on the supply bias line, it extended to the back of the circuit in order to be isolated from the digital programmer tracks. The connection between the top and bottom layers is done with 9 vias (for each connection) instead of one large via in order to reduce the inductance. Fig. 5-54 shows the variation of the via inductance as a function of via hole size.
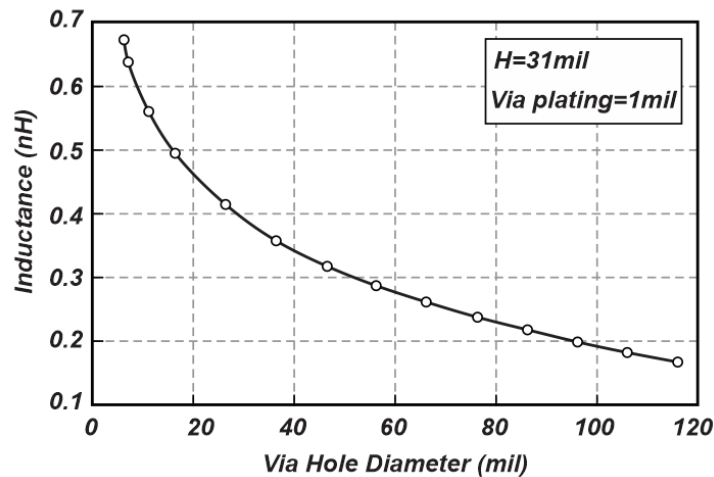
Fig. 5-54, The inductance of a via as a function of hole diameter

As shown in Fig. 5-54, increasing the via hole size, reduces the via inductance. Since the relationship between the via inductance and the via hole size is not linear, in order to reduce the inductance between the top and bottom layers, multiple vias have been placed in parallel with each other (on the main bias line). The minimum size via that

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has been used in this project (allowed by the manufacturer) has the diameter of 6mil corresponds to about L=0.63nH.

Since isolating the digital parallel programmer by placing the ground planes around the lines makes the board quite area inefficient, the distance between the digital tracks are set to three times the width (3×7mil=0.5mm). Note that the programming frequency is in the MHz range ($\approx$50-70MHz), and as a result, the cross talk does not have a significant degradation effect on this part of the circuit.

Unfortunately, the board cannot be placed on the brass block because some of the programming signals are routed at the back side of the board and they pass through the conductive vias that are exposed. Fabricating a multi-layer board makes the design quite expensive. Similarly, covering the vias enhances the board cost by almost 30-40%. As a result, the board will be placed on the board spacers using the holes placed on the board corners.

5.8   Application

In order to check the practicality of the driver stages, the cascode architecture has been selected to be implemented in a complete digital transmitter because it is quite area efficient. The digital transmitter architecture is shown in Fig. 5-55. As shown, in this architecture, 7 cascode driver stages are placed in parallel with each other to form a high power output stage and the input signal to each stage comes from a phase modulator block and the output signals combine with each other with a capacitive combiner block. Since the output signal of each deriver stage alters from ground potential (0V) to V_{DD}, the cascode stages can be considered as switches and the transmitter architecture can be simplified as in Fig. 5-56.
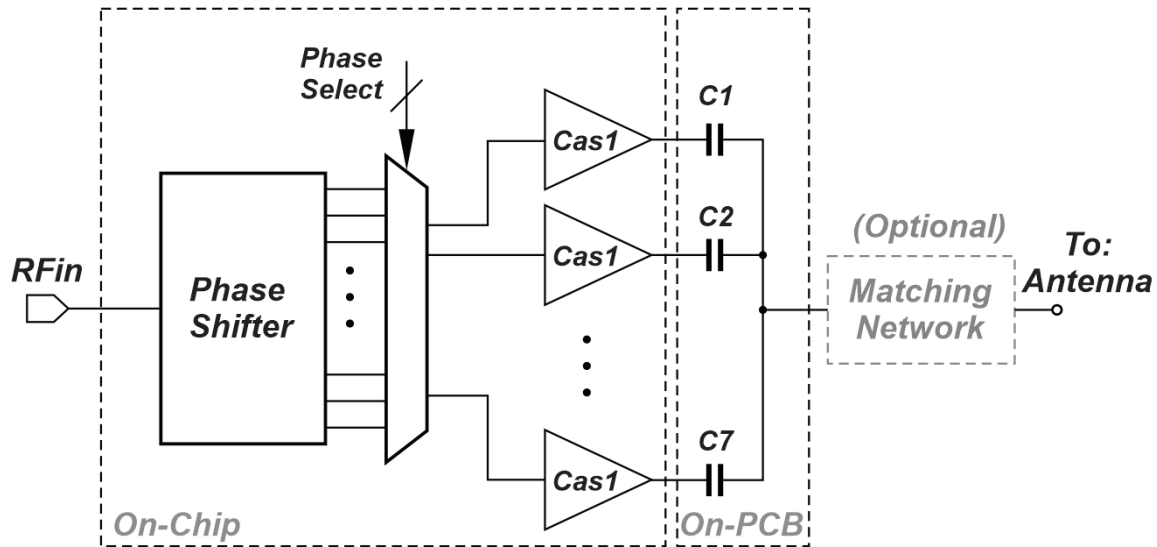
Fig. 5-55, Fully digital transmitter architecture
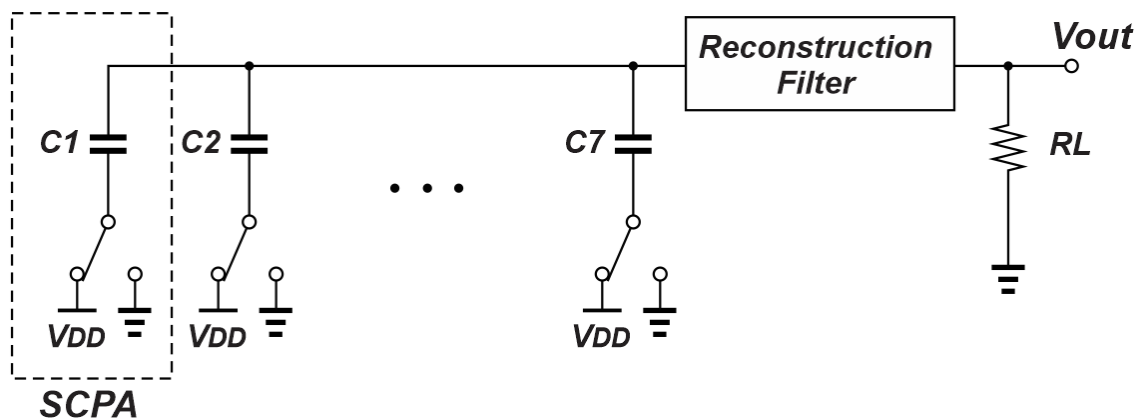
Fig. 5-56, Simplified model of the switched capacitor transmitter architecture

As shown, each driver stage is modeled by a switch and a capacitor, which can be called as a switched capacitor power amplifier (SCPA). In order to generate the output voltage, the combined signal passes through a reconstruction filter. It must be noted that the capacitor values do not need to be necessarily equal and can be weighted in order to make any combination of the output signals generated by the output stages (drivers).[103].

One of the main challenges in the conventional digital transmitters is the limited bandwidth [104-106]. The critical factor that limits the transmitter's bandwidth is the output generated harmonics. In order to expand the bandwidth of the transmitter, the proposed architecture performs harmonic cancellation technique.[107]. Fig. 5-57, graphically explains the harmonic cancellation (HC) idea. As shown, since the bandwidth of the transmitter is quite wide, filtering the harmonics, creates notches in the system bandwidth and prevents the operation at those particular frequencies. As a result, filtering the harmonics is not a practical method for wideband systems. In order to manipulate the signal powers at the harmonics, multiple signals with different phases are combined with each other. This type of combination is the expanded version of conventional out-phasing power combining.
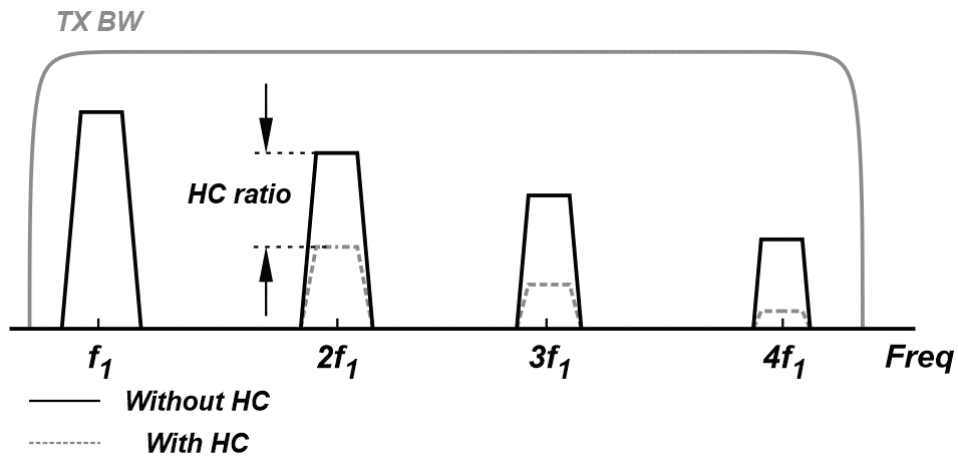
Fig. 5-57, Conceptual explanation of harmonic cancellation (HC) technique

Unlike conventional analog phase modulators that use LC-VCOs to generate sinusoidal signal at the output [69], in order to have a better control on the output phase, a ring oscillator architecture has been utilized. The basic idea of poly phase combining technique is shown in Fig. 5-58. As shown, the phase of the input signals (fundamentals) are not equal. The fundamental, second and third harmonic signals can be written as:

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$$V[1]_{1-5} = A_1 cos(\omega t + \varphi_{1-5})$$ (5-3)

$$V[2]_{1-5} = A_2 cos(2\omega t + 2\varphi_{1-5})$$ (5-4)

$$V[3]_{1-5} = A_3 cos(3\omega t + 3\varphi_{1-5})$$ (5-5)
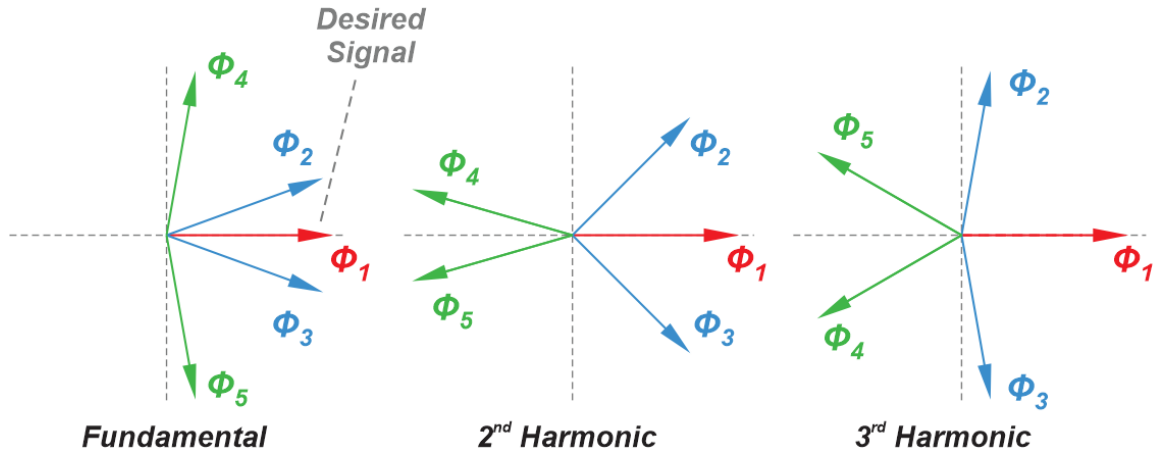
Fig. 5-58, Poly phase harmonic cancellation method description

since the phase of the second and third harmonics are multiples of the phase of the fundamental signals, by arranging the vectors in a particular order, the vector sum at the second and third harmonics can cancel out each other and therefore, these harmonics can be reduced significantly when they add to each other.

The proposed phase modulator has been designed to meet the specification of the 3GPP standard and as a result, in order to enhance the output power, cascode architecture has been utilized. The circuit diagram of the cascode is shown in Fig. 5-59. In order to bias the gates of the transistors, a resistive ladder is designed between the supply and ground rails. To reduce the DC power dissipation, the values of the resistors in this path are increased (I_{DC}=78µA). The sizes of the transistors are set to reduce the drain-source resistance and increase the rise and fall time of the driver stage (50-300ps depends on the supply voltage and frequency). The capacitors at the gates of the transistors are placed to limit the voltage swing at the gates in order to prevent the breakdown across the junctions

(V_{BR}=2V in this process). Two buffer stages are placed at the input of the cascode structure to decrease the fanout, as well as to enhance the voltage swing from the nominal 900mV up to 1.25V. This increased voltage allows the level shifter to provide adequate swing to fully turn on each transistor. It must be noted that the sizes of the input capacitors (4pF) are set in order to reduce the minimum applicable switching frequency (f_{min}=5MHz). The phase modulator and the driver stages are separated by a driver stage that operates with V_{DD}=1.25V. The design has been fabricated in CMOS 45nm RF process with the supply voltage of V_{DD}=0.9V. The fabricated chip is shown in Fig. 5-60 a. As shown, seven driver stages (called PAs) are placed on the chip along with the phase modulator and input/output (IO) circuitry. The main reasons for fabricating seven PAs is to enhance the output power and smoothen the phase variation. The entire chip consumes 2mm×2.5mm area including all the pads and ESD protection circuits.
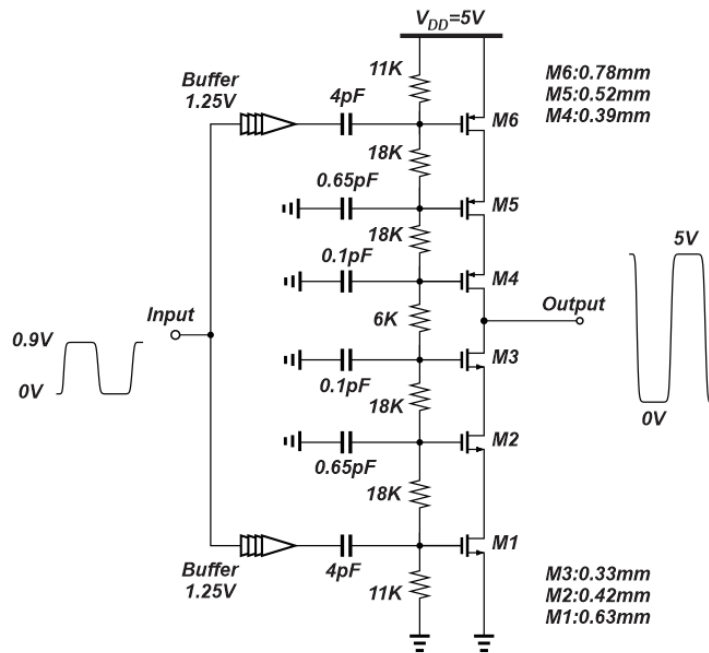
Fig. 5-59, Cascode architecture, optimized for the phase modulator
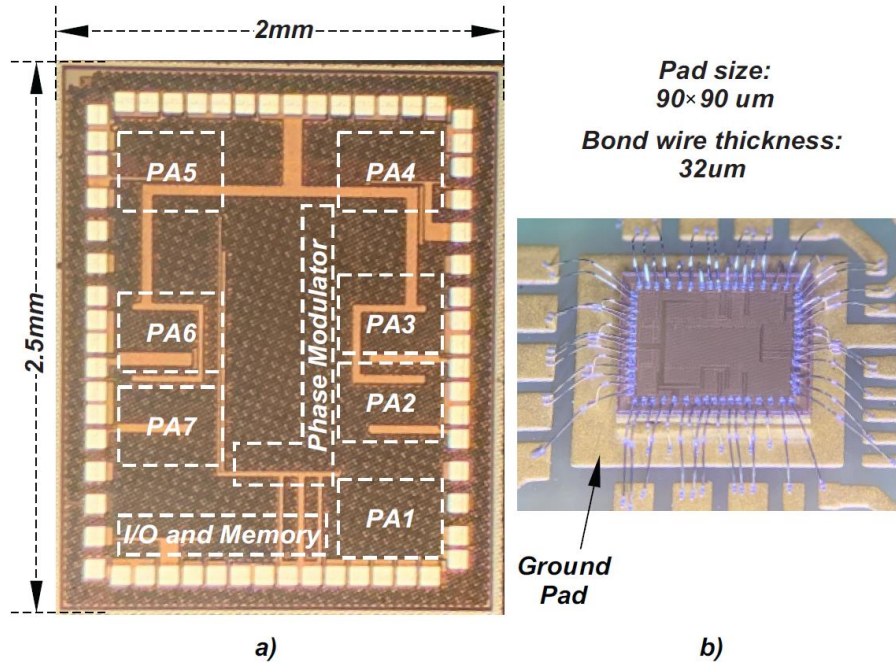
Fig. 5-60, a) Chip photograph of the polyphaser harmonic cancellation transmitter, b) wire-bonded chip to the PCB

In order to reduce the effect of the parasitics of the interface, the chip is directly mounted on the PCB (chi-on board process) and connected to the signal tracks by bond wired as shown in Fig. 5-60 b. In order to shorten the length of the ground bond wires, the area underneath the IC is set as a ground plane. The diameter of the bond wires is about 32μm and the maximum length is limited to L_{max}=1mm that corresponds to about 1nH of inductance. In order to minimize the bond wire inductances in series with the output ports, each PA is connected by 3 bond wires to the PCB tracks. Additionally, the 5V supply and the ground are connected to the die by 10 bond wires (each) to reduce any inductive parasitics in series with these paths. The bonding map of this architecture is shown in Fig. 5-61. As shown, the chip is placed at the middle of the die stand, which is well connected to the ground via multiple holes at the back side. In order to reduce the length of the ground bond wires, each side of the die stand is extended by 500μm in each side to have enough room for ground bonding. Since the chip is mounted on the PCB, to

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enable the correct wire bonding, all the pads are covered with soft wire bondable gold material.
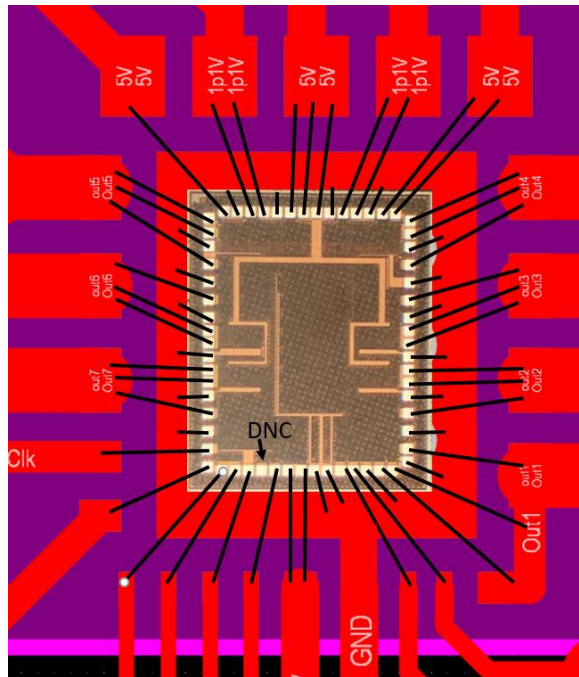
Fig. 5-61, Bonding map of the proposed switched capacitor driver IC

The configuration of the PCB is shown in Fig. 5-62. In order to minimize the PCB manufacturing price, a 2-layer PCB with FR-4 material has been designed with wire bondable gold cover for wire bonding capability. As shown, the board size is 8cm×12cm and there are 3 voltage regulators on it to provide voltages for the phase modulator (0.9V), inter-stage buffer (1.25), and output driver stage (5V). Eight driver output tracks are isolated from each other via ground planes around them. In order to combine the signals generated by the driver stages, the capability of connecting the output tracks to each other by capacitors is provided.
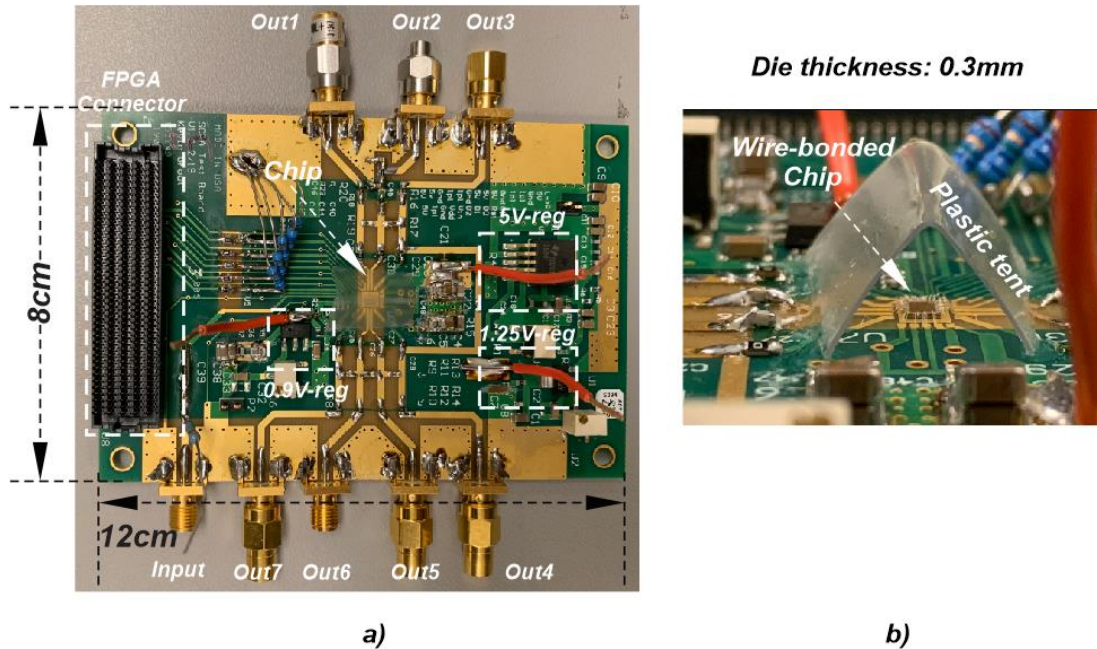
Fig. 5-62, a) PCB configuration, b) plastic cap is placed on top of the die for protection

5.9   Measurement Results

The HoC architecture is fabricated in 45nm CMOS SOI process with nominal

supply voltage of 0.9V and the cascode driver is fabricated in 45nm RF CMOS SOI with

the similar nominal supply voltage. In the first measurement, the HoC architecture

activated and fed with an internally generated pulse width modulated (PWM) signal, with

a random sequence. The spectrum at the output of the driver stage is shown in Fig. 5-63.

The transient response of the HoC stage is also shown in Fig. 5-64. As shown, the output

voltage provides about ΔV_{out}=4V signal swing that matches the total supply voltage

across the chip. In order to verify the switching speed, Fig. 5-65 illustrates the falling

edge of the output transient response. As shown the fall time, which is approximately

equal to the rise time, is about t_{fall}=0.5ns that corresponds to $f_{switching}$=1GHz. It must be

noted that since the maximum speed of the oscilloscope is 1GHz, capturing the switching

speed more than 1GHz is not feasible in the lab. This set of measurement reveals that the

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HoC stage is successfully able to generate output signals up to $V_{out}=5V$, which is high

enough for wide range of applications such as GaN based switched mode power

amplifiers.
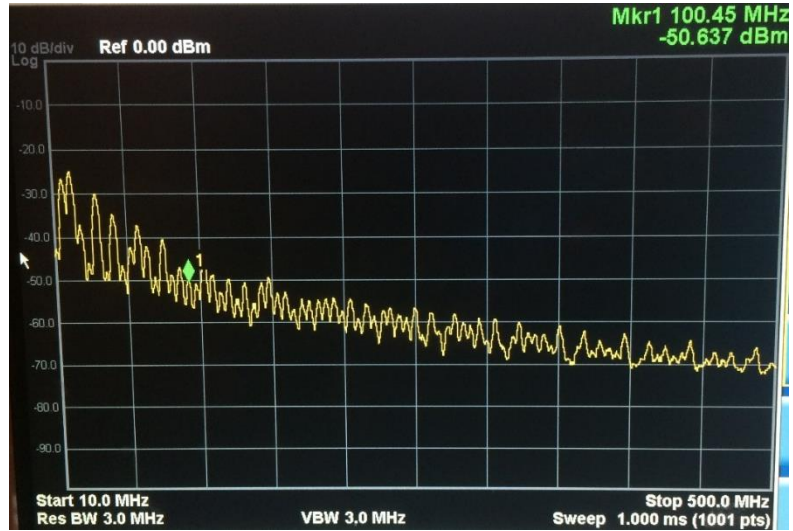
Fig. 5-63, The spectrum of the randomly generated PWM signal (after 20dB attenuation)

Fig. 5-64, Transient response of the HoC driver stage (after 20dB attenuation)
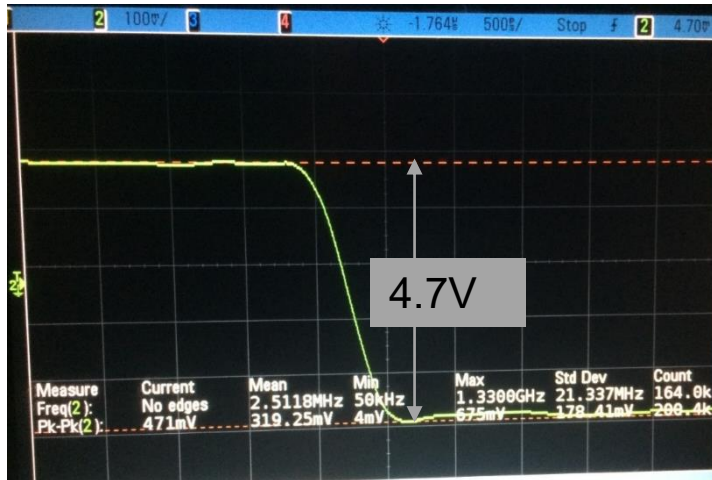
Fig. 5-65, Transient response of the HoC stage (switching speed)

The measurement setup of the cascode architecture is shown in Fig. 5-66. As illustrated, the "KCU105" FPGA is used for programming the phase modulator block in the chip. The input to the board is the reference clock that comes from a vector signal generator. Since the required clock signal needs to have a DC-offset with respect to the ground potential on the PCB (reference ground), the required DC value (Vdd/2) is fed to this track by a large size resistor (1MΩ).
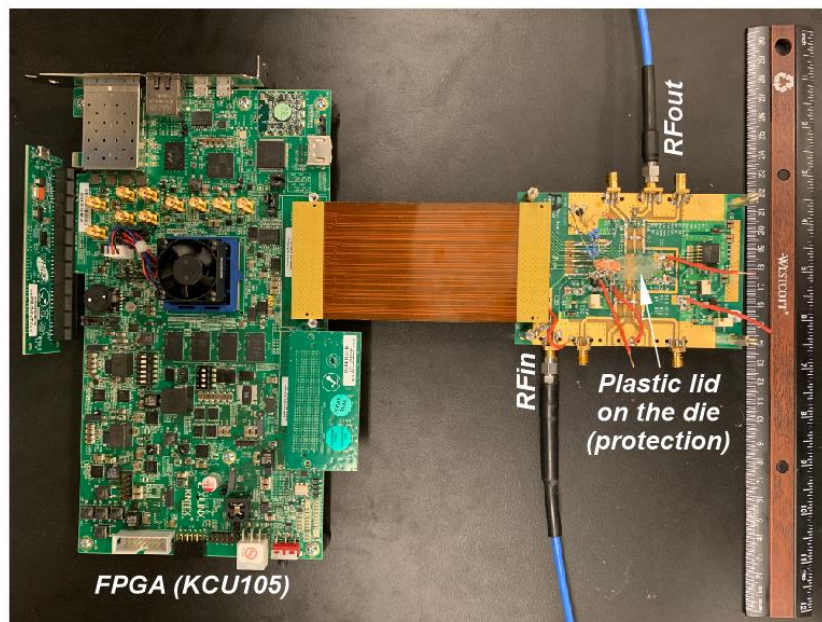
Fig. 5-66, Cascode measurement setup

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The transient response of one of the driver stages is shown in Fig. 5-67. In order to protect the driver stage at this level, the supply voltage is set to V_{dd}=4V and as shown, the output signal tracks the supply voltage. Fig. 5-68 shows the rise and fall transient of the output waveform. As shown the maximum captured signal at the output is about f_{sw}=1GHz, which is limited by the oscilloscope capability.

Fig. 5-67, Transient response of one of the cascode driver stages
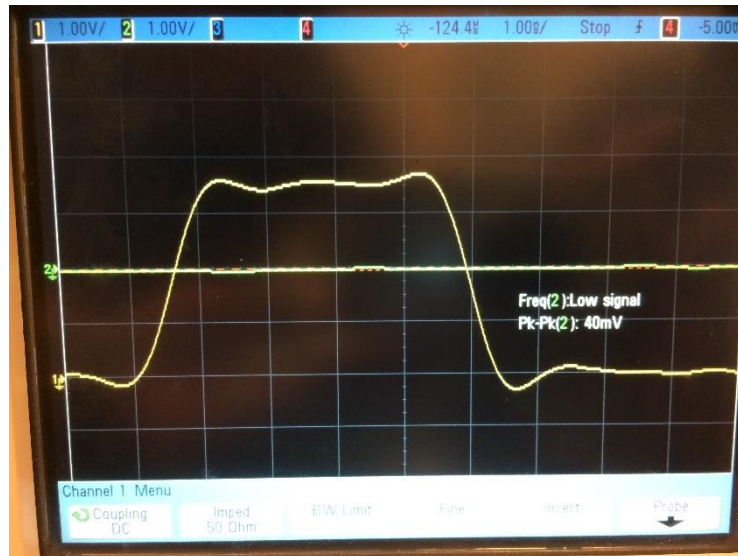
Fig. 5-68, Transient response of one of the cascode driver stages (zoomed version)

In order to estimate the maximum tolerable voltage across the cascode architecture, the supply voltage increased until the cascode stage is not functional. The maximum tolerable voltage for the chip is measured as $V_{absolute}$=7V. Fig. 5-69 illustrates the chip micrograph after applying 7V across the cascode stages. As shown, the black marked on the chip (exactly at the locations of the cascode stages), indicate that the driver is totally damaged and it is not functional anymore.
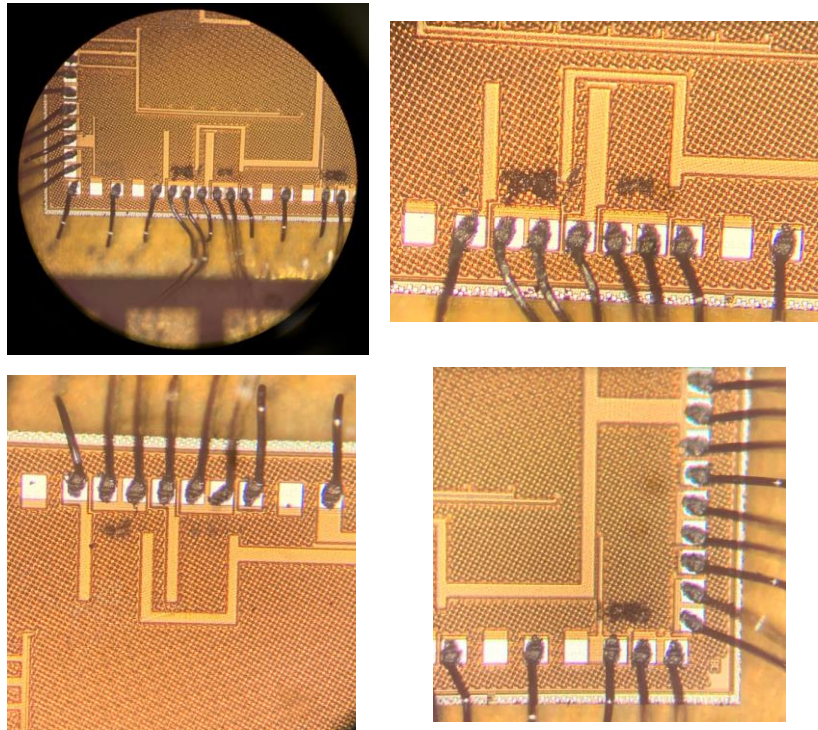
Fig. 5-69, The chip micrograph after applying 7V on the chip

Fig. 5-70 illustrates the maximum achievable output power for versus input signal frequency for different supply voltage levels. As can be seen, the maximum achievable output power is about P_{out}=29dBm, which is quite significant compared to the state of the art reported results. Since the cascode stage has a fixed rise and fall time, by increasing the supply voltage, more time is required to reach to the final value, by increasing the input signal frequency (clock signal), less power can be delivered to the output load

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(R_L=50Ω). It must be noted that the effect of the bond wires and tracks on the PCB is also included in the measurement of the output power. The efficiency of the transmitter module is shown in Fig. 5-71. Since the switching power dissipation is a square function of the supply voltage, by increasing the supply voltage the efficiency of the transmitter module reduces. As shown, the maximum achievable efficiency is about 45%, which is quite considerable compared to the state of the art results.
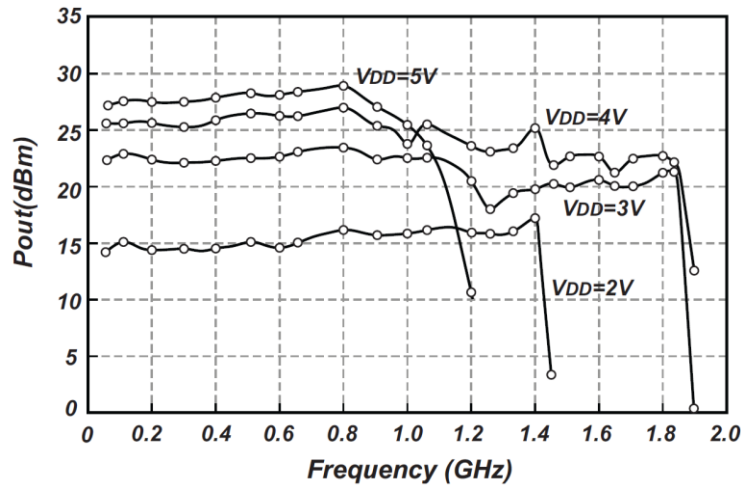
Fig. 5-70, Output power as a function of switching frequency for different supply voltage levels
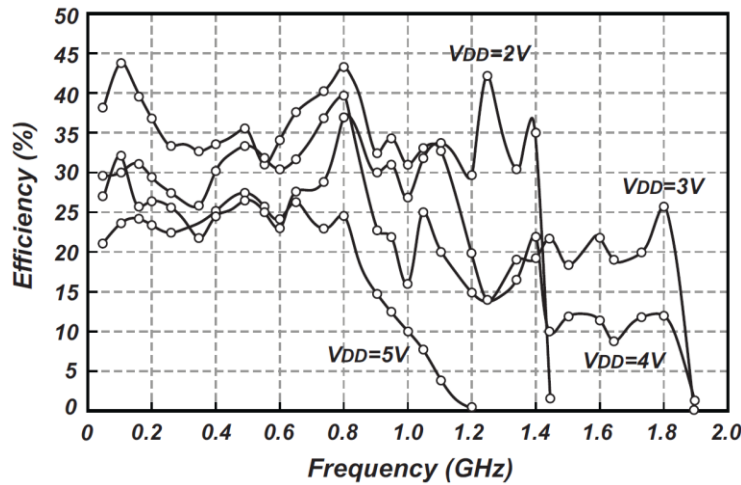
Fig. 5-71, The efficiency of the transmitter module

Fig. 5-72 shows the maximum achievable harmonic cancellation versus frequency. As shown, the applied harmonic cancellation met the 3GPPstandard limit up

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to 1.1GHz. Since the transmitter is designed to operate for GSM standard, the harmonic

cancellation measured up to about 1.1GHz.
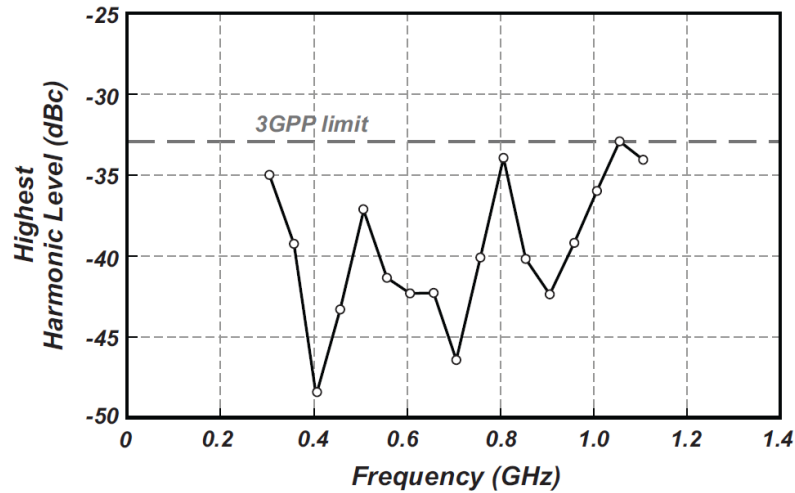
Fig. 5-72, The highest harmonic cancellation level as a function of frequency

In order to verify the system performance, the input is excited with a GSM signal.

The output constellation of the transmitter is shown in Fig. 5-73. The minimum measured

error vector magnitude (EVM) of the transmitter with 200 kHz signal bandwidth at

900MHz carrier frequency is 0.966%, magnitude and phase errors are 0.544% and 0.531°

respectively. Fig. 5-74 shows the behavior of the output signal EVM as a function of

frequency. Since my increasing the frequency the time that the driver stage requires to

settle down reduces, the EVM of the output signal increases with the frequency. Fig. 5-75

illustrates the output spectrum of the transmitter block when the channel bandwidth is

Ch_{BW}=200kHz and carrier frequency f_c=900MHz. As shown, the transmitter stage is

linear enough to pass and passes the GSM spectrum without any significant distortion. It

must be noted that this measured results is captured without any digital pre-distortion at

the input signal.

200kHz, GSM signal at 900MHz

EVM=966m%
Mag Err=544m%rms
Phase Err=531mdeg
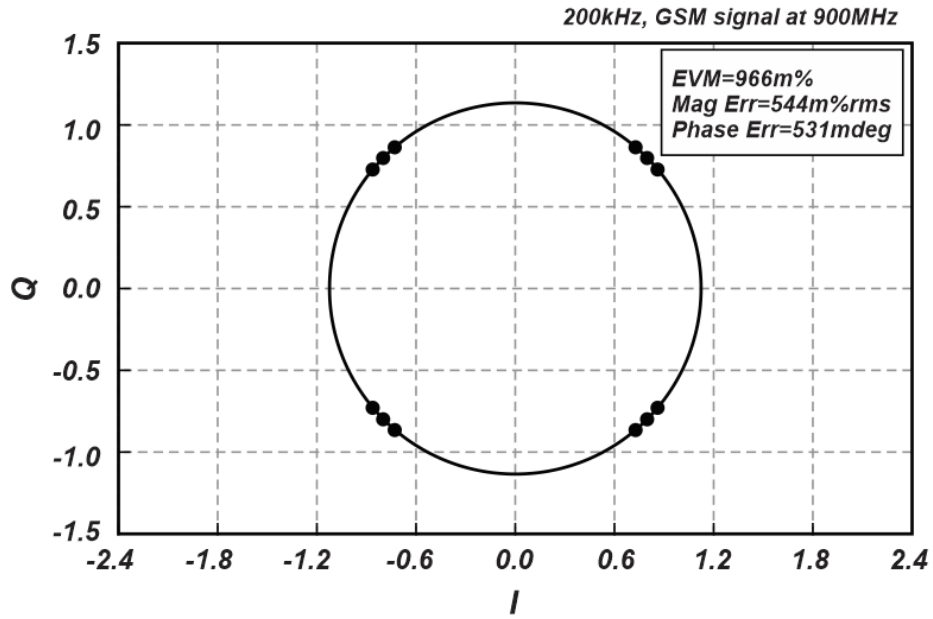
Fig. 5-73, Output constellation of the transmitter when excited by a GSM signal
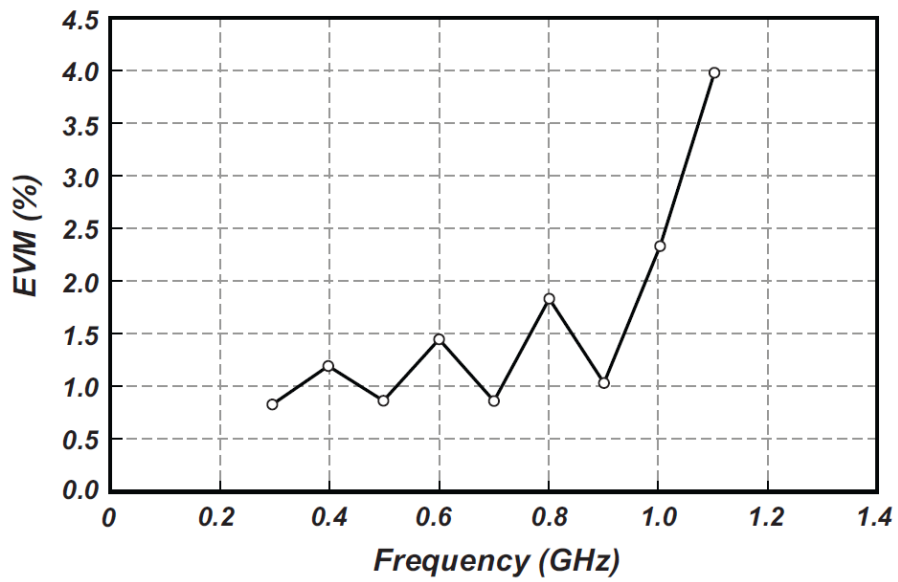
Fig. 5-74, error vector magnitude of the GSM signal as a function of frequency
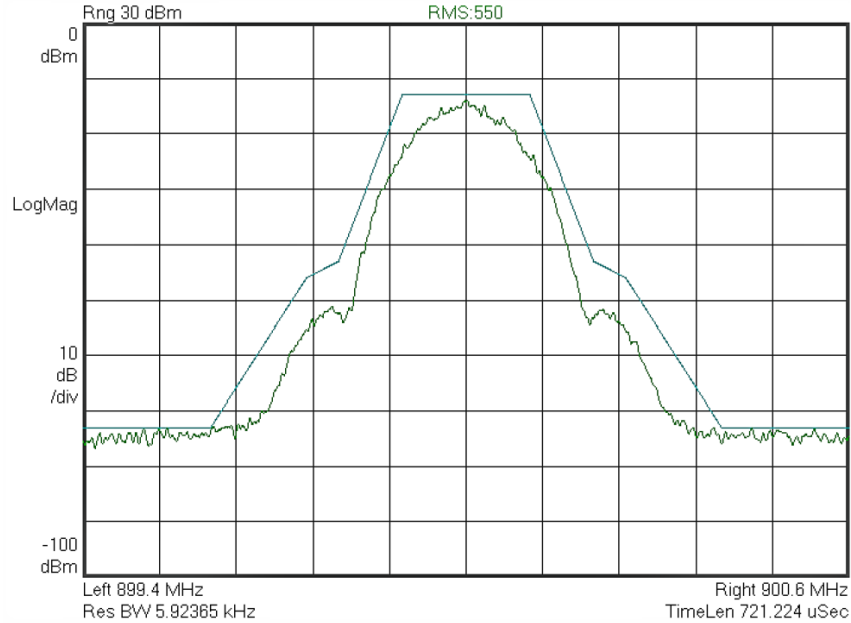
Fig. 5-75, The output spectrum of the transmitter (Channel BW=200kHz and carrier frequency=900MHz)

In order to verify the maximum capability of the digital transmitter, the system is excited with a wideband GSM input signal (Ch$_{BW}$=1MHz) with a carrier frequency of f$_c$=900MHz . Fig. 5-76 shows the output spectrum of the transmitter. As shown, the output spectrum successfully passed the standard spectral mask with no digital pre-distortion. These measurements clearly show that the proposed transmitter architecture as well as the driver stage do not affect the linearity of the system. Table. 5-2 compares the proposed transmitter architecture with the state of the art designs. As reported in the paper, since the proposed architecture utilizes high power cascode driver stages, the maximum achievable output power is significantly higher that the state of the art designs. Also, the linearity (in terms of EVM) at 900MHz is less than all the reported values while the harmonic cancellation (HC) value is -40dBc.

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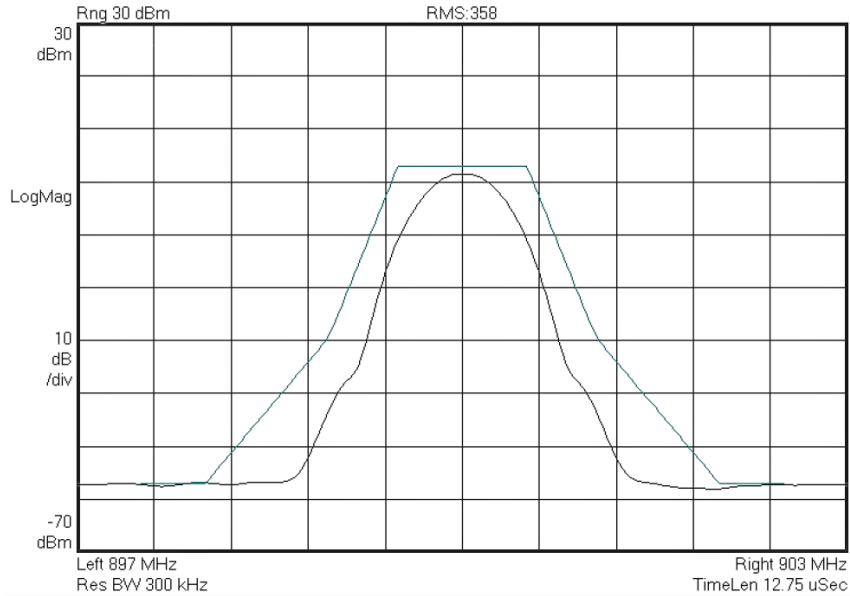
Fig. 5-76, The output spectrum of the transmitter (Channel BW=1MHz and carrier frequency=900MHz)

Table. 5-2, Comparison table between the proposed transmitter architecture and the state of the art designs

	[107]	[108]	[105]	[109]	This Work
Technology (nm)	40	90	40	40	45
Topology	Polyphase (SCPA)	Multilevel / Transformer	Duty Correction	Duty Correction	Polyphase SCPA
Supply voltage (V)	1.1	1.2	1	1, 3	1, 5
$P_{out-max}$ (dBm)	8.9	5.3	1.2	0	29
Active Area (mm^2)	0.13	0.2	0.3	1.1	0.67
Frequency (MHz)	850-1200	906-924	2400	2400	300-1100
HC_{max} (dBc)	-30	-37	-50	-46	-40[*]
EVM(%)	NA	2.5	5.2	NA	1
Maximum η_{Drain}(%)	43	62	39	9[**]	43
Bandwidth(MHz)	0.1	1	1	NA	1

*Averaged across the entire frequency range
**System efficiency

5.10 Conclusion

In this chapter a new approach for digital transmitter implementation has been shown and different CMOS based driver architectures have analyzed. The implementation and design of the cascode and house of cards architectures have been reviewed. It is shown that the main challenge in high voltage CMOS based drivers is the protection of the unction and oxide break down voltage of the transistors. In order to protect the oxide breakdown of the transistors, the aforementioned architectures are promising techniques. In addition, it is shown that the interface connection between the CMOS driver stage and the load (a 50Ω termination or the impedance seen from the input of a GaN based switched mode PA) limits the maximum switching frequency of the CMOS architecture. The main reason for this problem is introduced as the return paths from the load to the driver stage. Particularly, the bond wires create an LC network with the parasitic capacitors in the circuit and degrade the settling time of the output signal.

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