Survey of Photonic and Plasmonic Interconnect Technologies for Intra-Datacenter and High-Performance Computing Communications

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***Abstract*— Large scale Data Centers (DC) and High Performance Computing (HPC) systems require more and more computing power at higher energy efficiency. They are already consuming megawatts of power, and a linear extrapolation of trends reveals that they may eventually lead to unrealistic power consumption scenarios in order to satisfy future requirements (e.g. Exascale computing). Conventional CMOS-based electronic interconnects are not expected to keep up with the envisioned future board-to-board and chip-to-chip (within multi-chip-modules) interconnect requirements because of bandwidth-density and power-consumption limitations. However, low-power and high-speed optics-based interconnects are emerging as alternatives for DC and HPC communications; they offer unique opportunities for continued energy-efficiency and bandwidth-density improvements, although cost is a challenge at the shortest length scales. Plasmonics-based interconnects on the other hand, due to their extremely small size, offer another interesting solution for further scaling operational speed and energy efficiency. At the device-level, CMOS compatibility is also an important issue, since ultimately photonics or plasmonics will have to be co-integrated with electronics. In this paper, we survey the available literature and compare the aforementioned interconnect technologies, with respect to their suitability for high-speed and energy-efficient on-chip and off-chip communications. This work refers to relatively short links with potential applications in the following interconnect distance hierarchy: local group of racks, board to board, module to module, chip to chip and on chip connections. We compare different interconnect device modules, including low-energy output devices (such as lasers, modulators and LEDs), photodetectors, passive devices (i.e. waveguides and couplers) and electrical circuitry (such as laserdiode drivers, modulator drivers, transimpedance and limiting amplifiers). We show that photonic technologies have the potential to meet the requirements for selected HPC and DC applications in a shorter term. We also present that plasmonic interconnect modules could offer ultra-compact active areas, leading to high integration bandwidth densities, and low device capacitances allowing for ultra-high bandwidth operation that would satisfy the application requirements further into the future.**

***Index Terms*— Complementary Metal Oxide Semiconductor (CMOS), Data Centers (DC), High Performance Computing (HPC), International Technology Roadmap for Semiconductor (ITRS), Nanophotonics, Network on Chip (NoC), Plasmonics, Optical Printed Circuit Boards (OPCBs), Silicon Photonics (SiPh), Silicon On Insulator (SOI), Surface Plasmon Polariton (SPP), System in Package (SIP).**

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I. Introduction

HIGH Performance Computing (HPC) and Data Center (DC) communications, covering quite different scales, have increasingly higher bandwidth demands and at the same time require lower and lower power consumptions [1-3]. As the energy dissipation for handling information has risen to environmentally significant levels [1, 4], we are not able to continue handling the exponential growth in information traffic without the use of new technologies that significantly reduce the energy per bit communicated.

A standard nomenclature on an interconnect distance hierarchy from DC-interconnection, to intra-DC connectivity all the way to on-chip interconnection, is shown in Table 1 [5-7]. The different levels of this hierarchy are addressed by various market players and technology solutions, since they have quite different requirements. For most of these interconnection levels, one of the most critical parameters in measuring the performance of a HPC or DC interconnect is, the energy efficiency (measured in pJ/bit or mW/Gbps). An equally critical metric for assessing these interconnections is the cost per bit ($/Gbit). Additionally, the bandwidth density

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(Gbps/mm or Gbps/mm^2) is another important factor for system design [8]. Table 1 illustrates the interconnection hierarchy in the computing system for typical dimensions and targeted energy and cost budget to stay competitive against electronic counterparts [7].

TABLE 1
ENERGY AND COST TARGETS FOR OPTICAL INTERCONNECTIONS

	Distance	Energy per bit	Target Cost
Inter-DCN	1–100 km	<10 pJ/b	<$1000
Rack-to-rack	1 m–2 km	<1 pJ/b	<$100
Board-to-board	0.3–1 m	<1 pJ/b	<$10
Module-to-module	5–30 cm	<0.5 pJ/b	<$5
Chip-to-chip	1–5 cm	<0.1 pJ/b	<$1
Core-to-core	<1 cm	<0.01 pJ/b	<$0.01

The aforementioned interconnect bandwidth requirements are actually showing a tremendous growth trend owning to a large part to the exponential increase of computer performance expectations. Figure 1 presents the processing power, in floating-point operations per second (flops), of the most powerful computer (N=1), the average of the top 500 (N=500) and sum of the top 500 (Sum) over time. For example, IBM's "Roadrunner" achieved 1.026 petaflops in 2008 to become the world's first TOP500 Linpack sustained 1.0 petaflops system. A linear extrapolation of that system could be considered as an indication of the power and cost expectations of the projected first Exaflop system (circa 2020). It is worth noting that today's HPC systems already consume several megawatts of power and in the near future, when they are expected to reach Exascale performance, their target power should be kept below 20 MW power [7, 9]. To meet this target, the ratio of HPC performance in GFlops to the total system power dissipation in watts, must increase by a factor 25. Specifically, the performance development in GFlops, in HPC systems can be derived by extrapolating the past growth. A growth of a factor of about 10 every 4 years can be found, as seen in Figure 1 [10]. However, the corresponding power increase factor that can be accommodated is just a factor 2 for the same time, while the system cost increases only by a factor of 1.5 [11]. Reference [12] forecasts similar trends on HPC requirements, i.e. that the performance will increase by a factor 8, the power dissipation per bit will decrease by a factor 3, and the size will decrease by a factor 2, within a 3 year period. These computers comprise of many-core, multi-processor systems. Given that these cores communicate with each other at speeds of several tens of gigabits per second, interconnect systems should be able to handle speeds of terabits per second [13]. Likewise, for server-to-server communication, where thousands of processors need to communicate very fast, one will need multi-terabit-per-second class interconnections [13].

To some extent this interconnect traffic can be handled by electrical interconnects. Although electronic links might remain dominant for some short-reach chip-to-chip or on chip communications, the inevitable high channel losses of the copper wires, pin-count constraints, and crosstalk would significantly limit the energy efficiency and bandwidth. Furthermore, high-speed electrical interconnections require a specific and precise impedance matching, which needs a fixed hardware configuration. Conversely, optical interconnects exhibit low loss at high symbol rates, have high distance insensitivity, and are immune to electromagnetic interference. They do not need sensitive impedance matching and therefore, allow more open architectures. Thus, optical technology can potentially play a crucial role in decreasing the power consumption in future interconnects, while supporting the required speed and performance [14, 15]. IBM's projections based on the aforementioned trends [16, 17] suggest that energy efficiency values below 1 pJ/bit at cost below $0.10/Gbps will be feasible. ST-Microelectonics has issued projections as well, which follow a similar trend [18, 19]. Future directions based on such trends, have also been considered by other vendors, who have shaped their strategy and implementation plans accordingly.

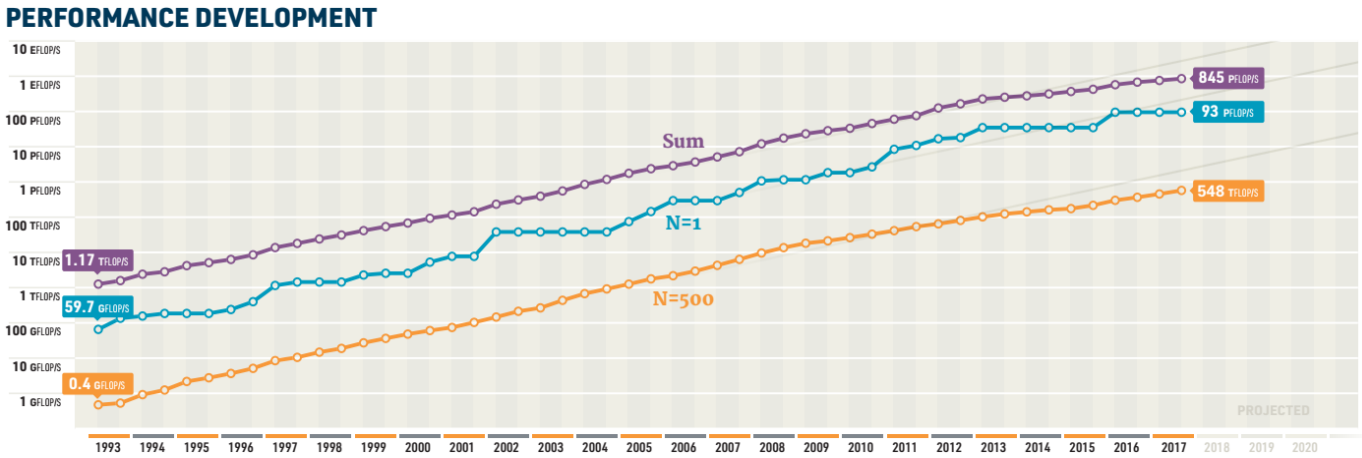

Fig. 1. The processing power (flops) of the most powerful computer (N=1), the average of the top 500 (N=500) and sum of the top 500 (Sum) with time (E. Strohmaier, TOP500, November 2017 [10])

Optical interconnects have thus come in the focus of research as being an enabling technology for intra-datacenter interconnections and Exascale high-performance computers. A critical question then relates to the proper optical interconnect technology among the competing options. Different approaches are considered, related with: (a) the choice of the integration method (e.g. hybrid or monolithic) and packaging process, as well as with (b) the choice of the network on chip (NoC) architecture:

1) Current integration approaches are either monolithic, where optical devices and transistors are all included on the same die [20-22], or heterogeneous, where photonics and electronics are developed on separate chips, and connected with each other via a bonding technique [23, 24]. The first one provides a promising cost and energy-efficient integration solution and the second one a more flexible approach due to the decoupling of electronic and photonic devices fabrication. While heterogeneous integration decouples photonics and electronics fabrication, the necessary multi-chip (TSV/microbump) packaging adds parasitic capacitance limiting performance and energy efficiency. Monolithic integration, on the other hand, simplifies packaging and enables tighter device-to-circuit proximity to lower parasitics. However, some critical limitations related to this approach are that it does not decouple CMOS electronics and photonics scaling roadmaps and that it faces wafer processing challenges combining these two technologies (electronics and photonics). However, today hybrid integration technologies is the most efficient and commonly used approach due to two facts. First, laser light generation still cannot be realized efficiently in silicon as it is an indirect semiconductor material. Therefore, in most cases direct semiconductor materials like AlGaAs or InGaAs are used for light sources. Second, also for photodiodes operating at telecom wavelengths mostly different semiconductor materials than silicon need to be used since silicon photodiodes are sensitive only below the bandgap, corresponding to below ~1100nm.
2) Concerning the Network-on-Chip (NoC) architecture, in this architecture multicore processors are interconnected on the same chip, and their performance is mainly determined by the combined capabilities of the multicore processors, which are running at moderate speeds. Currently, traditional 2D mesh electronic NoC interconnect many-core processes. They are favored for their high scalability and small footprint, but they have buffer bypassing limitations that could be overcome by optical NoC (ONoC) architectures. Yet, in photonic implemented NoC architectures there are several challenges that need to be overcome, such as efficient buffering, header processing, or the unavailability of efficient on-chip light sources. Along these lines, many all-optical NoC schemes have been proposed [25-30].

The main focus of this survey is to review all recent advancements on photonic and plasmonic short distance interconnections, as well as to outline the associated challenges and future perspectives of this area. This work refers to the following interconnect distance hierarchy: local group of racks, board to board, module to module, chip to chip and on chip connections.

In the following sections, we make a detailed comparison among all technologies, mainly on the grounds of energy efficiency and bandwidth performance. Our work is structured as follows: Section II presents a qualitative review of short reach interconnects including conventional electronic CMOS interconnects, photonic technology based interconnects and plasmonics, while Section III exhibits an overall quantitative analysis and evaluation of all these interconnect technologies. In section IV, a similar quantitative comparison is implemented (in terms of energy efficiency) with a focus on specific interconnect device modules. In this section, we compare different interconnect device modules, including low-energy output devices (such as lasers, modulators and LEDs), photodetectors, passive devices (i.e. waveguides and couplers) and electrical circuitry (such as laserdiode drivers, modulator drivers, transimpedance and limiting amplifiers). Finally, in the last section of this survey, we draw some general conclusions.

II. Qualitative Review of Short Distance Interconnects

A. CMOS Conventional Interconnects – ITRS Limitations and Projections

Over the last decades the progress of conventional CMOS electronics has been governed by Moore's Law, stating that the number of transistors on a microprocessor chip will roughly double every two years. This means that more and more transistors and integrated circuits can be placed onto smaller areas. However, in the last years the doubling has started to slow down due to heat dissipation and technology scaling challenges from the large number of transistors and circuits in the small chip area [31].

As the device dimensions such as the gate oxide thickness have been reduced to several atomic layers, tunneling and leakage current become significant. The limit is expected to be reached for gate lengths around 5nm because of increasing leakage currents [32], known as gate leakage limitation[33]. Some solutions to this problem have already been proposed, such as 2D and 3D gates [34] and FinFET gates, as already adopted by major vendors like Intel [28].

In the early stages of integrated transistors, much of the power inside electronic machines was for performing logic operations. Over the last decades, the ever smaller transistors reduced the energy per logic bit considerably [31]. In fact, this power reduction is continuing–though at a slower pace [35]. Conversely, the energy to send information inside electronic machines does not scale down the same way, especially for longer connections. Thus, a significant fraction of the energy dissipated by computing systems is meanwhile used for

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communications [36, 37].

As the interconnect wire length increases, the increased wire capacitance results in a larger interconnect power dissipation. Charging a capacitance to a voltage V results to an energy $(1/2)CV^2$ dissipated in the series resistance through which the capacitor is charged. The same energy is dissipated into the discharging resistance when the capacitor is discharged. Thus, whenever the bit changes state, we dissipate $(1/2)CV^2$, either in the charging resistance or in the discharging resistance. Therefore, one of the goals in the design of efficient CMOS electronic interconnects is to decrease the total capacitance [1] and scale down the operating voltage.

Another important dissipation issue in interconnect systems is the energy required for clocking, data retiming, and time-multiplexing in interconnect links. Energy dissipation for electronic circuitry such as clock and data recovery (CDR) circuits, line coders, and serialization and deserialization (SERDES) circuits (for handling clocking, data retiming, and time-multiplexing issues) is a critical factor affecting the total energy dissipation of interconnects.

In 2007, a market-driven platform power limit of 130 W per die (total power dissipation for processing and communications operations on chip) was acknowledged, and the microprocessor (MPU) frequency roadmap was revised to increase by just 8% per year in order not to exceed this power limit [38]. That clock frequency scaling limitation is highlighted in Figure 2 [38, 39]. It is worth mentioned that today's chip-power limits have been significantly increased reaching values over 200 W [40].

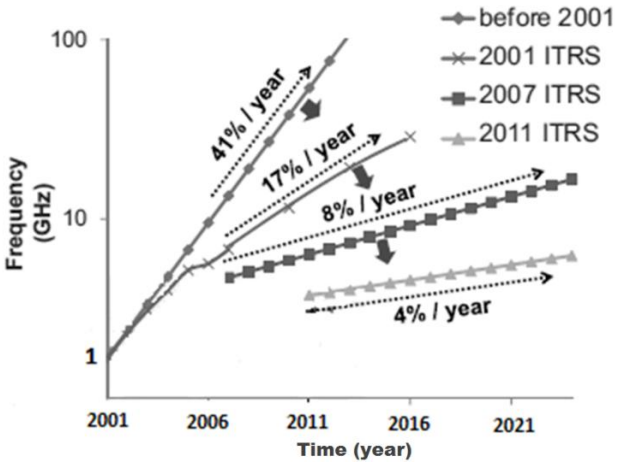

Fig. 2. Historical changes in the ITRS maximum on-chip frequency roadmap [38, 39]

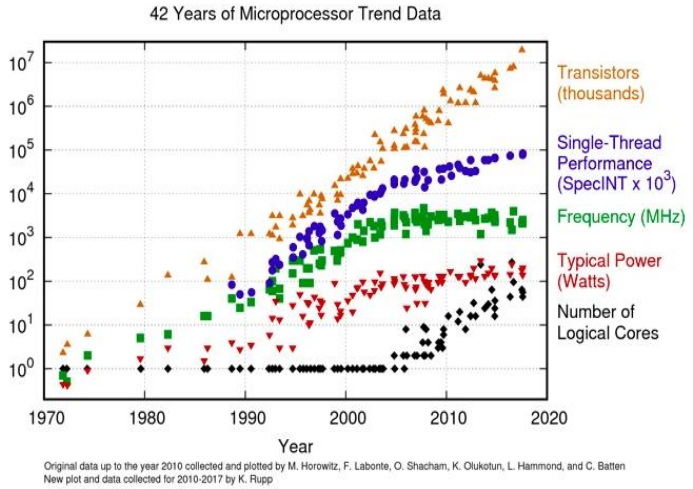

Fig. 3. Evolution of electronic CMOS characteristics over time [41]. Transistor counts (orange triangles) are growing exponentially following Moore's law while performance growth is limited by power consumption. Single thread performance (blue circles) had been increasing by 60% per year until 2005 and slowed down to +20% per year after 2005. The operation frequency (green squares) is also limited due to power restrictions (after 2005).Typical power consumption (red triangles) and number of cores (black rhombuses) are also presented.

Figure 3 shows the evolution of CMOS transistors over time. It summarizes in a single graph the aforementioned limitations that conventional CMOS electronics is facing [38, 42]. We observe that transistor counts are growing exponentially in the diagram following Moore's law while performance growth is limited by power consumption. Single thread performance had been increasing by 60% per year until 2005 and slowed down to +20% per year after 2005. After 2005 also the operation frequency is limited due to power restrictions.

B. Photonic Interconnects at Present and in the Future

Optical interconnect technology has been identified by ITRS and major vendors as an alternative solution to overcome the foreseeable scaling limitations of conventional interconnects. The status and potential of optical based solutions are summarized in the subsequent sections.

Photonic solutions are about to penetrate the lowest levels of the interconnect hierarchy of DC and HPC systems [15, 43, 44]. The current trends foresee that optics will migrate from board levels to the chip level, within the next few years [45, 46]. Fig. 4 shows the structure of a possible Exascale compute node by exploiting photonic devices [43]. As stated in [43], the most critical aspect of the design is providing sufficient memory bandwidth to sustain the processor within an acceptable power budget. This will be achieved by either stacking ~~n~~ear" memory directly on the processor, or locating it within the processor package itself. As the amount of memory that can be connected in this way is limited, additional memory will be provided by memory modules connected to the processor through high-speed optical links.

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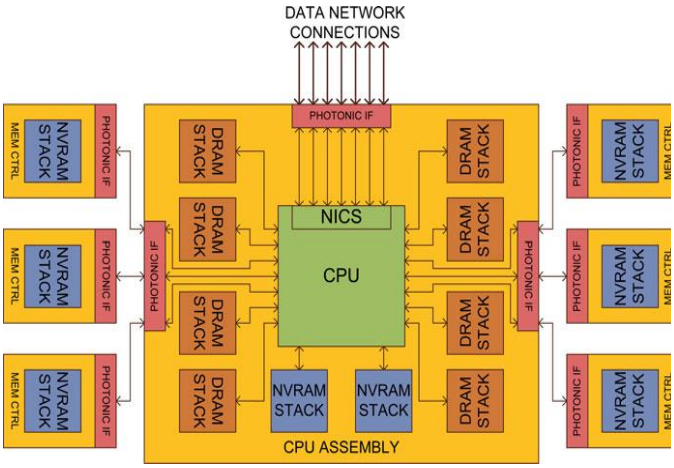

Fig. 4.The structure of a possible Exascale compute node by exploiting photonic devices [43].

Recent research work has been focused on defining the optimal, critical length for certain line rates for which optical interconnects can indeed offer a competitive substitute over the corresponding electronic based ones. It has been stated that the critical length beyond which optical interconnects becomes advantageous over electrical interconnect is approximately one tenth of the chip edge length at the 22 nm technology node (using a chip edge length of 17.6 mm) [47, 48]. Another similar study shows that on-chip electrical interconnects suffer from losses at lengths beyond 200 cm, for the 22 nm node technology and hence it would be better substituted by optical interconnects [49]. For board-to-board systems, when datarates become higher than 20 Gbps, optical interconnects should replace electrical ones since the latter would need power-consuming amplification to be used to compensate for transmission loss [50].

There are two main advantages of optics in reducing energy dissipation in interconnects: a) In optical interconnects there is no charging of electrical lines, and b) optics may eliminate electronic circuitry such as clock and data recovery (CDR) circuits, line coders, and serialization and deserialization (SERDES) circuits. It is known that the charging of electrical wires is the main source of energy dissipation in simple electrical interconnects [51], and that optics can eliminate this through ―quantum impedance conversion" [1]. Another important aspect is that optics has additional features, such as large synchronous zones and large number of physical channels that can potentially eliminate the need for CDR, SERDES and line coding [1]. However, optical interconnects cannot abstain from electronics completely since the processors will be electrical also in near future. Thus, the electrical circuitry is still needed to interconnect the processor I/Os with optical interconnections on-board. This circuitry has to drive the optics and leads to proper matching between the electronic and optic worlds. Nowadays, the optical links are rather static and optimized for peak performance to accommodate the peak data throughput on the link. However, data rates are varying over time due to dynamic user and application behavior. To make these electronics more energy-efficient another approach is to implement adaptivity on the circuit, component and system level to scale the component's performance and power consumption during runtime according to present requirements on the link. If a lower data rate is present on the link, the performance (e.g. bandwidth) of the adaptive component can be reduced and therefore power can be saved. Such an adaptivity can be achieved by either switching a part of the link components completely on and off or by changing their operating points with their biases [52]. It has been shown that both methods can lead to a reduction of power consumption by 80%.

Several photonics based technology solutions could be deployed, as future HPC systems are reaching Exaflop performance. Some of them include the already deployed option of using vertical-cavity surface-emitting lasers (VCSELs) over multi-mode fibers (MMF) or the long-anticipated silicon photonics technology [53, 54]. Market research surveys show that VCSEL-based transceivers on short reach MMF interconnects hold an important portion of the market in optical transceiver sales[55]. Polymer waveguide technology has also been compatible with MMF parallel optical links at board interconnect level and was proposed as a way to reduce the fiber count. On the other hand, silicon nanophotonics is considered one of the most promising technologies, for providing small footprint devices, enormous bandwidth density, low energy operation and CMOS compatibility [13, 54, 56-62]. CMOS-based nanophotonic waveguides on Silicon on Insulator (SOI) usually have low propagation losses ranging from 0.2 to several dB/cm. They can be used as active silicon components for all optical signal processing, along with other materials (III-V, Ge) for achieving low energy interconnections. A lot of research has also been conducted on the incorporation of silicon photonic technology in combination with other technologies, such as polymers, graphene and nitride material, leading to hybrid interconnect schemes with ultrahigh density and speeds [58].

Co-integration of silicon photonic (SiPh) with electronics into a complex circuit, can be achieved via different integration approaches: Front end of line, back end of line backside, 3D and flip chip integration [63]. Next trends for SiPh integration tend to silicon photonic interposer integrated with CMOS logic for the short term, and 3D optical chip stack integration for the long term. Global Foundries and IBM has presented the key challenges and technical results from both 200mm and 300mm facilities for a silicon photonics fabrication process which includes monolithic integration with CMOS [64]. IBM has also developed photonic packaging approaches with the potential for high-throughput fabrication in microelectronics facilities [65]. Samsung has implemented SiPh-based optical to electrical circuit integrated into the DRAM chip, for CPU-DRAM interconnection [66]. Luxtera was the first company to implement a SiPh transceiver integrated circuit (IC, 4 x 10 Gbps) [67-70]. ST-Microelectronics, has heavily invested on SiPh technology and plans to implement an integrated interconnect system on SiPh interposer, with multi wavelength (multi λ) integrated

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nanophotonic lasers that would enable chip to chip DWDM communication [18]. Also Fujitsu implemented an integrated optical Tbps I/O chip based on SiPh which is co-packaged with the CPU chip [71]. Though SiPh has been a niche market, it now is clearly emerging and has the potential to satisfy the requirements of the future market [19].

A critical aspect in short reach interconnects is the limited density of access pins. An advantage of optics is that multiple wavelengths in the form of DWDM only need one access waveguide. Utilizing parallel DWDM the pin density limitation of the existing electrical DRAM interfaces [66-70, 72] could potentially be overcome. To use WDM for short distance interconnects, it is required to utilize micro-/nano-photonic structures. Since a large number of channels are needed, the wavelength separator must be very compact. In [73] an all-solid-state, WDM silicon photonic link for chip-to-chip communications with low energy dissipation (<1.5 pJ/bit) has been presented. A drawback with use of dense WDM techniques in large-scale short distance links is the issue of fabricating or adjusting large numbers of systems with high precision. All these issues make the use of DWDM for short reach interconnects very challenging for the time being [74].

Some other emerging possibilities for short reach interconnects are space-division multiplexing (SDM) and free-space optics (FSO). Although SDM seems to be a very promising approach [5, 75-77], the use of electronic techniques such as MIMO processing for the mitigation of coupling effects between the different information channels [78], results in higher energy dissipations and larger footprints in short reach interconnects. A radical solution for reducing energy per bit while increasing throughput density uses imaging optics to create a massive number of parallel spatial channels for free-space optical (FSO) communication between chips [1, 79]. Transmitting in each channel at a low speed may obviate the need for high-speed receiver and (de)serialization and synchronization circuits, reducing energy consumption substantially. This approach uses a rectangular array of optical inputs and outputs to provide a large number of spatial dimensions. This approach relies on a waveguide-based interposer that maps between the optical inputs and outputs and detectors and modulators (or emitters) located near data registers on the chip.

C. Plasmonics Technology – Where Does It Stand and Where Is It Expected to Contribute?

Plasmonics technology deals with the generation, processing, transmission, sensing and detection of signals at optical frequencies along metallic surfaces [80-82]. It has been widely discussed [83-87], that plasmonics technology is going to bridge the gap between small but slow electronic interconnections and fast but large sized photonic ones. Plasmonic devices can interface with similar speed photonic devices and similar size electronic components. For these reasons, plasmonics may well serve as the missing link between the two device technologies [83].

Surface plasmon polariton (SPP) based circuits, which essentially merge electronics and photonics at the nanoscale, may offer a solution to this photonic-electronic size/speed compatibility problem [84]. SPPs are electromagnetic oscillations that occur at a metal/dielectric interface, when photons interact with the plasma of electrons near the surface of the metal. These oscillations can be confined to very small dimensions- way beyond the diffraction limit. Thin metal films of finite width embedded in a dielectric can be used as plasmonic waveguides. However, the propagation lengths for SPPs typically are limited to some tens of microns by absorption due to dissipation of the SPPs in the metal and due to free-space radiation of SPPs at rough surfaces. There is a tradeoff between propagation length and confinement of light in plasmonic devices. The propagation lengths of highly confined SPPs are so short that they cannot propagate across an entire chip (~1 cm). Weakly confined Dielectric-Loaded Surface Plasmon Polariton (DLSPP) waveguides offer longer propagation lengths and may be considered as a low loss solution [88].

Concerning crosstalk, it has already been pointed out that, with reduced waveguide diameters or higher optical frequencies, SPP waveguides may provide less crosstalk than conventional interconnects, and thus higher interconnect densities. This comes at the price of higher energy loss, of course [89].Another important aspect is that energy per bit of plasmonic interconnects increases exponentially with interconnect length [89].

The key devices of the plasmonic interconnects are the plasmonic Mach-Zehnder modulators such as depicted in Fig. 5 [87]. In this structure an optical signal is inserted by a photonic wire waveguide. In a first section the optical signal is converted into a SPP and simultaneously split up onto two branches. The plasmons are then guided onto two arms that are formed by plasmonic metal-insulator-metal waveguides. The metals on the one hand serve as plasmonic waveguides. On the other hand they are also the electrical contact to apply a voltage. The insulating material in the plasmonic slot waveguide then comprises of a linear-electro optical material.

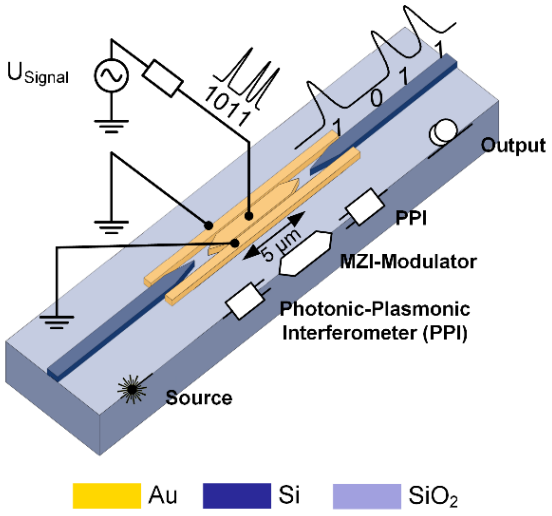

Fig. 5. Configuration of a plasmonic Mach-Zehnder modulator integrated into a silicon strip waveguide [87]

From a comparison among plasmonic and photonic modulators it has been shown that plasmonic modulators have very low capacitance that leads to high performance and low power consumption [90]. Power consumptions of 2.84 fJ/bit have been demonstrated for speeds up to 100 Gbps for plasmonic modulators [91]. Moreover, the area of these modulators is only a small part of the area occupied by photonic modulators- some few μm^2 rather than 1000s of μm^2 to mm^2 [87]. Recently plasmonic modulators were realised with an oxide based electro-optical, providing excellent prospects on the thermal stability of these devices [92]. Also, an all-plasmonic 116 Gbps electro-optical modulator, in which all the elements (the vertical grating couplers, splitters, polarization rotators, and active section with phase shifters) are included in a single metal layer, has been presented in [93].

Plasmonics can be used for detectors as well. Detectors of plasmons that take advantage to enhance the coupling of light into the photodetector, are suggested by ITRS as an alternative technology [94]. One well known plasmonic detector approach is the photodetection with active optical antennas where a highly compact, wavelength-resonant, and polarization-specific light detector, with a spectral response extending to energies well below the semiconductor band edge is utilized [95]. Here, photons coupled into a metallic nanoantenna excite resonant plasmons, which decay into energetic, ~~h~~ot" electrons injected over a potential barrier at the nanoantenna-semiconductor interface, resulting in a photocurrent. Another more recent approach is a photoconductive plasmonic photodetector that features high speed at nanometer scale [96]. The concept is based on the electro-absorption effect in a plasmonic slot-waveguide with amorphous Ge as active material.

In [88, 97, 98], active plasmonics were introduced for WDM switching applications, using the smallest active Dielectric-Loaded Surface Plasmon Polariton (DLSPP) thermo-optic (TO) Mach-Zehnder interferometric switches with successful performance in single-channel 10 Gbps data traffic environments (4x10 aggregated) bringing low-power active plasmonics to practical applications. In [98], the 4x4 Tbps Silicon-Plasmonic router relies on a novel integration concept promoting the use of innovative thermo-optic DLSPP switches integrated with SOI passive photonic components to build a MUX, and electronic processing circuitry. In [85, 99], chip scale interconnection systems based on active and passive plasmonic devices have also been presented. At the transmitter side, chip modules such as plasmonic modulators (phase or amplitude) or nanocavity lasers or LED structures were used as transmitters [87]. At the receiver side, hybrid plasmonic amplifiers with couplers with low losses, and plasmon based photodetectors were used, respectively.

By utilizing a plasmonic modulator and a silicon photonic waveguide, we can combine the benefits of both technologies: long range propagation, and high performance modulation [90]. In order to integrate a hybrid photonic-plasmonic link, an efficient coupling between plasmonic and silicon waveguide must be implemented. In [100-102], new plasmonic MZM array modulators are experimentally demonstrated for the first time, providing compact, ultra-dense, and high-speed interconnections by a multicore fiber (MCF). The key concept is shown in Fig. 6 [102]. It shows a multicore fiber (MCF) interfacing an integrated plasmonic-electronic circuit. A MCF is used as an optical interface to the chip because it allows interconnecting the chip with as much as 40 fiber cores on the footprint of a single fiber. In our case we use a first core to feed in an optical cw signal, we then distribute the signal in the photonic layer to distribute it to an array of modulators. The density of the modulators is only limited by pitch of the MCF or the electronic pads.

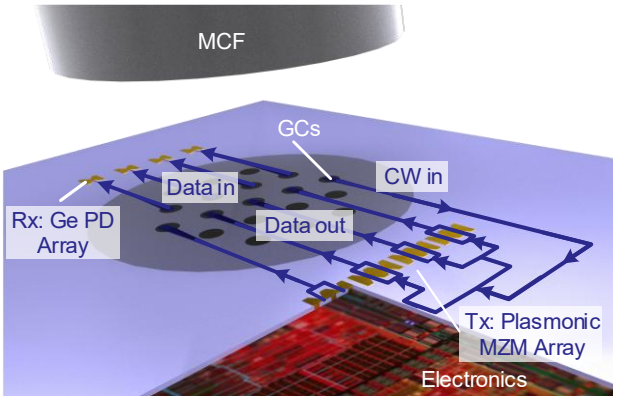

Fig. 6. Compact high-speed optical interconnect scenario: Integrated transceiver consisting of a plasmonic MZM array and a photodiode array. The Tx:, a CW signal of a central laser is coupled to the chip through a multicore fiber (MCF) onto the chip by grating couplers (GCs). The light is then distributed to the integrated plasmonic MZMs to encode a parallel data stream. After encoding, the signals are coupled out via separate cores of the MCF. Rx side: PDs receive the signals stemming from different cores of the MCF. The electronic contacts of the devices may be realized through vias from the bottom of the chip [102].

The bottom line from all relevant studies so far, is that plasmonic technology has a broad range of applications, from passive ones such as couplers, to active ones such as lasers, modulators and switches, and detectors, all of them combined together, to build an energy-efficient interconnect.

D. A Qualitative Comparison

In order to provide a more complete and combined vision of different short-reach interconnect technologies and techniques, Table 2 qualitatively summarizes features and potential solutions with various kinds of interconnects (conventional electronic, photonic and plasmonic).

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TABLE 2
QUALITATIVE COMPARISON OF DIFFERENT INTERCONNECT TECHNOLOGIES.

Interconnect technologies & associated features	Conventional electronic	Photonic	Plasmonic
Energy efficiency	Medium	High	High
Operating speed (GHz)	Medium	High	Highest
Bandwidth density	Medium	High	Highest
Footprint	Small	Medium	Small
Interface	Line driver	Opto-electrical and electro-optical conversion	Opto-electrical and electro-optical conversion + localization of optical field
Need for clock and data recovery (CDR) circuits	High	Medium due to the large synchronous zones (timing precision and stability of optical channels)	
Need for serialization and deserialization (SERDES) circuits	High	Medium due to the large parallelism and the large number of channels (FSO and SDM)	
Need for line coders	High	Medium due to the large parallelism and the large number of channels (FSO and SDM)	

III. Quantitative Analysis and Evaluation of Conventional Electronic, Photonic and Plasmonic Interconnect Technologies

In this section, we compare conventional electronic CMOS, photonic and plasmonic interconnects in terms of energy efficiency, bandwidth and implementation simplicity. Following the work of Miller [1, 51], it is shown that interconnect power is approximately 20% of the total chip power. It is known that interconnects are used to be driven from the server side with bulky and bandwidth-limited copper cables for the very short reach link or more expensive optical interconnects for the longer reach link. In the following sub-section an energy efficiency estimation of optical and electrical interconnects is carried out. The ultimate goal of this comparison is to find the transmission length where optical systems become more power efficient than their electrical counterparts.

A. An Energy Efficiency Analysis of Optical and Electrical Interconnects in Terms of Transmission Length

In terms of energy efficiency, the main difference between electrical and optical interconnects is that the loss of optical waveguides is bandwidth independent, while electrical interconnects are bandwidth limited and electrical propagation lossestypically increase with the data rate (R_{data}). The energy efficiency for electrical interconnects can be written as sum of different contributions:

$$E_{el} = E_{static} + n_{hop}\left[E_{crossbar} + E_{buffer}\right] + (n_{hop}+1)(P_{wg}+P_{Rx})/R_{data} \quad (1)$$

where E_{static} describes the energy efficiency of the terminal equipment. Depending on the transmission link, more than one hop might be needed (n_{hop}). The routing elements consume energy in the crossbar ($E_{crossbar}$) and buffer (E_{buffer}). The energy efficiency also depends on the transmission distance d between the links. Waveguide losses contribute with (P_{wg}) to the overall power consumption. After transmission the receiver needs a minimum powerP_{Rx}. The relative loss depending on the transmission distance$d$and the waveguide losses α_{wg}. The waveguide losses then contribute with

$$P_{wg} = P_{Tx} - P_{Rx} = P_{Tx}\left(1 - e^{-\alpha_{wg}\, d}\right) = P_{Rx}\left(e^{\alpha_{wg}\, d} - 1\right) \quad (2)$$

to the power budget. The total losses thus depend on the power fed into the link. The link power budget, i.e. the waveguide losses and receiver power then is

$$P_{Link} = P_{wg} + P_{Rx} = P_{Rx}\, e^{\alpha_{wg}\, d}. \quad (3)$$

It is convenient to use dB units. With $L_{wg,dB} = 10\left(\alpha_{wg}\, d\right)\log e\ dB$ one can write

$$P_{Link,dBm} = L_{wg,dB} + P_{Rx,dBm} \quad (4)$$

If the distance d becomes long, then the power dissipated due to waveguide losses becomes prohibitively large (waveguide losses increase exponentially) and it is more efficient to increase the hop numbers. Moreover, the dissipated power is much bigger than the power consumed within the terminal equipment (E_{static}).

The energy per bit of an optical interconnect transmitterE_{opt} may be described by two contributions. The energy per bit due to operating the laser (E_{laser}) and the one for data modulation (E_{mod}), both including necessary electrical drivers

$$E_{opt} = E_{laser} + E_{mod}, \quad (5)$$

where it is understood that the energy per bit include the energies for the respective drivers. The losses per bit in the optical waveguide losses do not depend on the data rate (the optical channel has multiple THz of bandwidths.

$$E_{laser} = P_{laser}/R_{data} \quad (6)$$

The required laser power P_{laser} is determined by its minimum optical output power which can be calculated by taking into account the receiver sensitivity P_{rx}, the static loss in the system (e.g. due to coupling, optical TSVs etc.) $P_{loss,static}$ and the loss inside the optical waveguide $L_{wg,,dB}$.

$$P_{laser,dBm} = P_{loss,static,dB} + L_{wg,dB} + P_{Rx,dBm} \quad (7)$$

The theoretical limit for the receiver sensitivity is the shot noise limit. However, for direct-detection unamplified short-range optical systems the thermal noise of the receiver is the more practical choice [103]: The photocurrent $I_p = \frac{\eta q}{h\nu} P_{in}$ is calculated from the optical input power P_{in} taking into account the quantum efficiency η, the charge of an electron q, Planck's constant h and the optical frequency υ. The noise is calculated with the load resistance R_L, the Boltzmann constant k_B, the temperature T and the bandwidth B $\sigma_T^2 = 4k_BTB/R_L$. Assuming white Gaussian noise, the required SNR for a given BER can be calculated. With this SNR, the minimum receive power (receiver sensitivity can be calculated). For example, a data rate of 100 Gb/s (OOK modulation), an optical carrier wavelength of 1550 nm, a quantum efficiency of η=1 at a temperature of 290 K and a SNR of 50 for a BER of 10^{-12} yields a minimum receiver sensitivity of -19.2 dBm. Adding some margin, for the calculations a receiver sensitivity of -10 dBm is chosen.

As for the electrical waveguide, also the relative loss in the optical waveguide is length-dependent but data-rate independent and much lower compared with electrical waveguides at high speeds:

$$L_{wg,o,dB} = \alpha_{wg,o,dB/length}\, d. \quad (8)$$

Taking into account typical numbers for energy-efficient lasers and their drivers (see systems compared in Table 3), at data rates in the Gbps range, the energy consumed in the electro-optical modulation dominates the contributions from the laser operation because of the involved electrical circuits whose energy consumption depends on the data rate (E_{mod}>>E_{laser}) [104].

The improvement of energy-efficient laser sources that are optimized and properly dimensioned for the respective link only has a marginal effect on the energy efficiency of the system. Increasing the energy efficiency of the electro-optical modulation part is more propitious as can be seen in Figure 7. Due to the higher loss of the electrical waveguides, multiple hops are needed which adds power consumption per hop and, consequently, slope that can be seen in Figure 7. Lowering the loss of the waveguide or increasing the hop length of the electrical interconnect would change the slope of the black curve but not the fact that a length exists where optical interconnects outperform electrical ones. For the calculations, an electrical link described in [105] has been used. A 32-nm technology was chosen (E_{static}=0.35 pJ/bit, $E_{crossbar}$=0.36 pJ/bit, E_{buffer}=0.12 pJ/bit, $E_{waveguide}$=0.34 pJ/(bit mm), hop length 1.67 mm). For the optical system, a receiver sensitivity of -10 dBm, a static loss $P_{loss,static}$=2 dB (caused e.g. by optical TSVs [106, 107] as well as coupling loss) and a waveguide attenuation of $\alpha_{waveguide}$=1 dB/cm [108] is used. Due to their lower loss, optical systems operate as single-hop systems. The electrical power consumed by the laser is calculated using the characteristics of optical power vs. laser current and laser current vs. voltage from state-of-the-art devices [109, 110]. This means, the laser power is optimized with respect to the transmission distance d which is currently not supported by all drivers. As mentioned before, the effect of E_{laser} on the results is very small at data rates in the Gbps range. Increasing the laser power by a factor of 10 only decreases the energy efficiency shown in Figure 7 by less than 1 pJ/bit.

As a consequence, there is a break-even length where optical systems become more power efficient than their electrical counterparts. Figure 7 already implies the fact. Depending on available technology, that length varies. In Figure 8, the electrical interconnect is compared with the optical interconnects. The energy efficiency of their modulation stages consisting of electro-optical modulation and driver electronics serves as parameter. The break-even length is shown depending on the data rate. It can be seen that above 10 Gbps the energy efficiency of the modulation stage becomes dominant. Another interesting result is that the break-even length between optical and electrical interconnects drops below 1 mm as soon as the energy efficiency of the modulation stage is better than 1 pJ/bit, which is realistic.

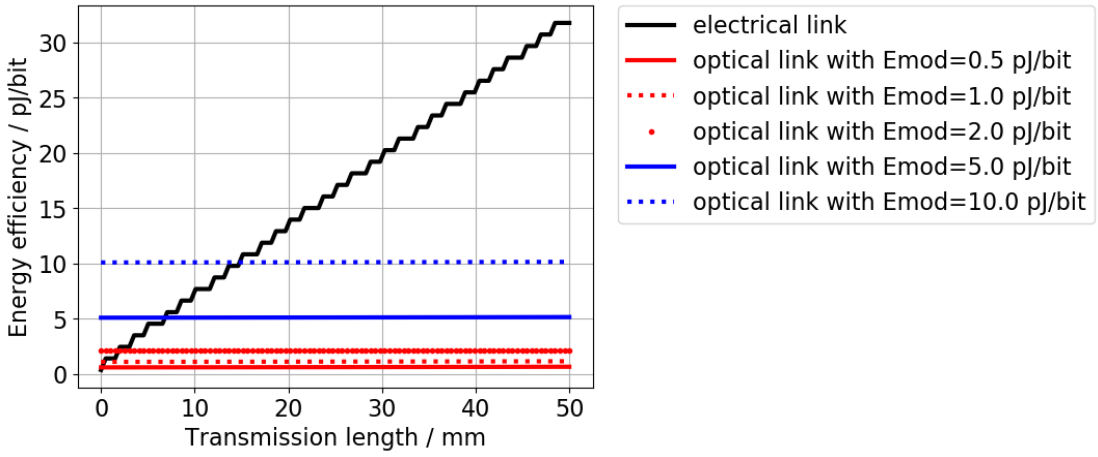

Fig. 7. Energy efficiency of example electrical and optical links with energy efficiency of the electro-optical modulation stage as a parameter.

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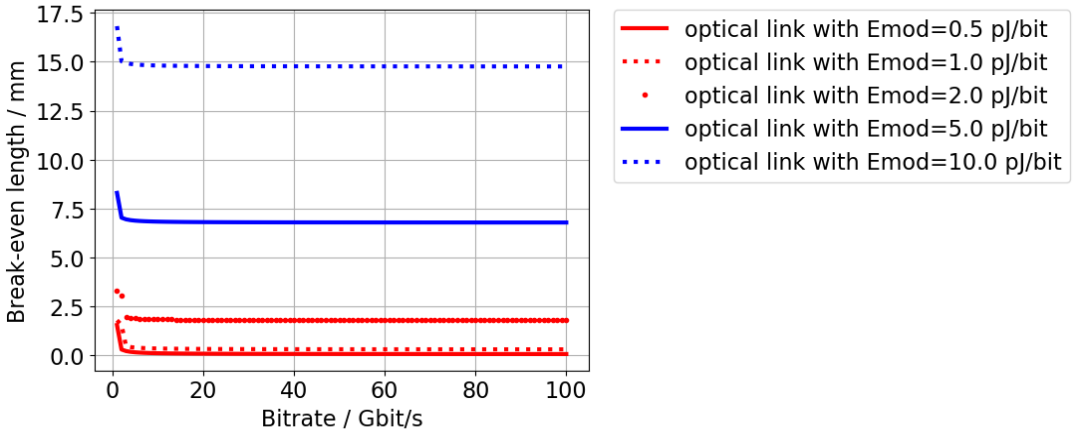

Fig. 8. Bit-rate dependent length where optical interconnects start to outperform an electrical interconnect in terms of energy efficiency with energy-efficiency of electro-optical modulation stage as a parameter.

B. Energy Comparison of State of the Art Electrical, Photonic and Plasmonic Interconnects

Over the last decade, a lot of research has been conducted on chip scale interconnects for improving bandwidth and energy efficiency. Table 3 presents an energy comparison between the different short distance interconnect technologies for the period from 2007 to 2017. In this table only studies with total link energy dissipation results (Tx+Rx power consumption) are included. It is worth mentioned that both commercial and experimental interconnections are presented in the following table. Concerning the conventional CMOS interconnect technology, energy efficiencies from 2 pJ/bit to 15 pJ/bit have been demonstrated over the last few years from vendors like Intel [111] and Altera (Intel Programmable Solutions Group) [112, 113]. Moreover, state of the art data about photonic interconnects are summarized in the following table according to giant industry leaders in the market, such as IBM [114-116] and Fujitsu [117]. Conventional CMOS interconnects, as expected, seems to be a bit behind from their photonic counterparts, in terms of energy dissipation downscaling.

TABLE 3
ENERGY COMPARISON OF DIFFERENT SHORT DISTANCE INTERCONNECT TECHNOLOGIES

Energy/Power consumption	Description	Node techn. (nm)	Link distance	Bit rate/BW	Year	Reference
2 pJ/bit	Electrical Interconnect	90 nm CMOS	0.80 m	6.25 Gbps	2007	[118]
2.8-6.5 pJ/bit	Electrical Interconnect	65 nm CMOS	0.20/0.46 m	5-15 Gbps	2008	[119]
~120 fJ/bit	Silicon photonic interconnect	NA	250 μm	3 Gbps	2009	[120]
3.6 pJ/bit	VCSEL-Based Optical Links	90 nm CMOS	4 m	25 Gbps	2012	[114]
1.37 pJ/bit	VCSEL-Based Optical Links	90 nm CMOS	4 m	15 Gbps	2012	[114]
7 pJ/bit	Electrical Cu-based Interconnect (Altera Stratix V)	28 nm FPGA	0.3 m	28 Gbps	2013	[112, 113]
23.7 pJ/bit	850 nm VCSEL-Based Optical Link	NA	5 m	56.1 Gbps	2013	[115]
1 pJ/bit	VCSEL-Based Optical Link	32 nm SOI CMOS	4 m	25 Gbps	2013	[121]
2.7 pJ/bit	VCSEL-Based Optical Link	32 nm SOI CMOS	4 m	35 Gbps	2013	[121]
26.3 pJ/bit	850 nm VCSEL-based optical link	IBM BiCMOS8HP process	57 m	64 Gbps	2014	[122]
0.2 pJ/bit	Optical link from InGaAs nanoresonators on a silicon substrate	NA	NA	2.5 Gbps	2014	[123]
25.5 pJ/bit	850 nm VCSEL-based Optical Link	130 nm BiCMOS	7 m	71 Gbps	2015	[124]
35 pJ/bit	850 nm VCSEL-Based Optical Link	0.13 μm SiGe BiCMOS	7 m	50 Gbps	2015	[125]
15 pJ/bit	Silicon-photonic link	0.18 μm bulk CMOS	5 m	5 Gbps	2015	[22]
4.9 pJ/bit	Hybrid Integrated Silicon Photonic Transceiver	28 nm CMOS and SOI	NA	25 Gbps	2015	[117]
1.1 pJ/bit (TX) 1.7-2.2 pJ/bit (TX+RX)	1060 nm VCSEL-Based Optical Link	90 nmCMOS	NA	26 Gbps	2015	[116]
1.5 pJ/bit	WDM silicon photonichybrid-integrated solid-state link	3 μm silicon-on-insulator (SOI)	12.4 mm	10 Gbps	2015	[73]
28.5 fJ/bit	LEAP laser for optical interconnects	NA	500 μm	4 Gbps	2015	[126]
11.07 pJ/bit	Silicon Photonic Interconnect	65 nm CMOS	NA	10 Gbps	2016	[127]
~6 pJ/bit	Optical interconnect based onVCSEL (Thunderbolt)	NA	~60 m	25 Gbps	2016	[111]
~15 pJ/bit	Copper link	NA	2 m	20 Gbps	2016	[111]
0.32 pJ/bit (Simulation results)	Surface Plasmonic Polariton Interconnect	65 nmCMOS	NA	25 Gbps	2017	[86]

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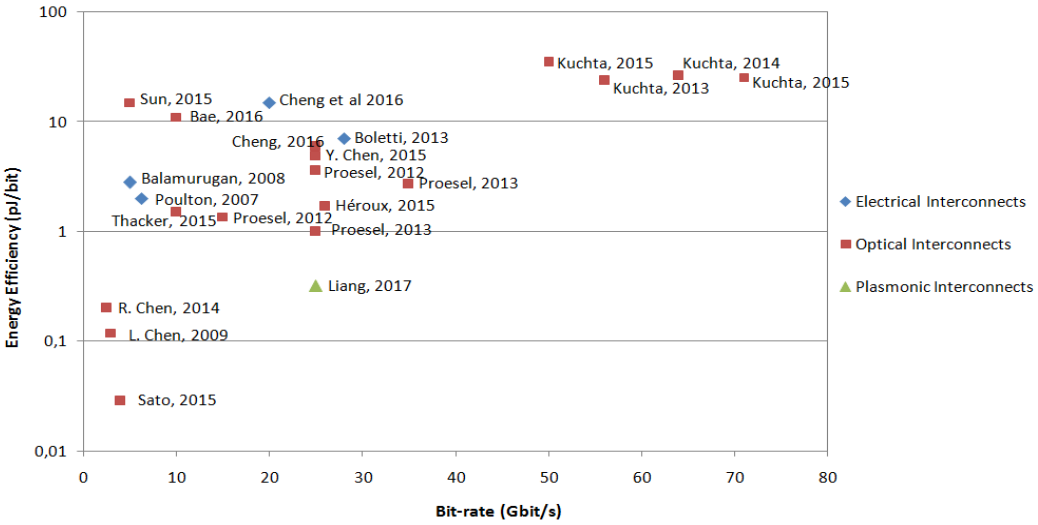

Fig. 9. Total energy dissipation versus bandwidth for conventional electronic, photonic and plasmonic short-reach interconnects (years 2007-2017).

In Table 3, we also include an energy-efficient and low-crosstalk sub-THz surface plasmonic polariton (SPP) interconnect in CMOS [86]. This SPP interconnect has achieved data rate of 25 Gbps with 0.016 pJ/bit/mm energy efficiency at 140 GHz in 65 nm CMOS. Although the results are simulated, they show the great potential of this interconnect technology.

Figure 9 shows the total link energy dissipation of the different interconnect technologies versus bandwidth for the period from 2007 to 2017. As can be seen, photonic and plasmonic interconnect schemes can be much more energy efficient than Cu-based counterparts, providing energies lower than 1 pJ/bit.

IV. On/off-Chip Interconnect Comparison At The Device Level

In this section we attempt to compare in terms of energy efficiency each device module that a typical interconnect consists of (see Figure 10), including low-energy output devices (such as lasers, modulators and LEDs), photodetectors, passive devices (i.e. waveguides and couplers) and electrical circuitry (such as laserdiode drivers, modulator drivers, transimpedance and limiting amplifiers).

Miller [1, 51, 128-130] and other researchers [131-134], have investigated energy targets for the optical interconnect technology in order to become much more competitive than conventional interconnects in future years. Of course these projections and estimations are based on various assumptions for the Byte/FLOP ratio, the I/O chip bandwidth, or the percentage of the interconnect power of the total chip power. Nevertheless, they certainly indicate the trend and the global energy target to be potentially achieved in the future.

For this purpose, we have gathered, the most recent references from the literature, related with energy performance of short distance interconnections, classified at the device level, for both competitive technologies; photonics and plasmonics. Moreover, the maximum operating bit rate is considered, along with active area dimensions for bandwidth (BW) density estimation. We have to state that all references are based on experimental research work.

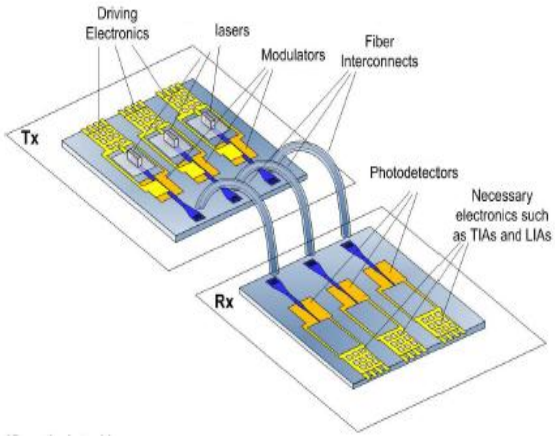

Fig. 10. 2-D typical interconnect structure (Source: Navolchi project [135])

A. Directly Modulated Lasers

Directly modulated lasers are attractive light sources in relatively short-reach data transmissions because of their low power consumption and cost. For a directly modulated laser, optical device energy targets of 10–20 fJ/bit for off-chip, let alone less than ten fJ for on-chip interconnects according to [51], will be hard to achieve. Figure 11 shows the energy cost as a function of laser active region for three different laser technologies. We observe that by reducing the active area, we can effectively reduce the energy cost.

In Table 4 we perform a comprehensive review of all the latest photonic and plasmonic directly modulated sources. As can be seen in this table, VCSELs usually reach a few hundred fJ/bit energies, with the best performance lying at 77 fJ/bit at 25 Gbps [136]. For this reason, despite the fact they are the state of the art transmitters for board-to-board interconnections nowadays, they cannot keep up with future on-chip energy requirements.

TABLE 4
PHOTONIC AND PLASMONIC DIRECTLY MODULATED SOURCES.

Energy/Power consumption	Description	Max. Temperature (°C)	Bit rate/BW	Area	Reference
77 fJ/bit (EDR) 56 fJ/bit (HBR)	850 nm VCSEL	NA	25 Gbps	3.5 μm(oxide-aperture diameter)	[136]
83/117 fJ/bit (EDR) 69/99 fJ/bit (HBR)	850 nm VCSEL	25°C	17/25 Gbps	2 μm (oxide-aperture diameter)	[110, 137]
140fJ/bit(EDR) 107 fJ/bit (HBR)	850 nm VSCEL	25°C	34 Gbps	26 μm (diameter active mesa) 4 μm (oxide-aperture diameter)	[138]
158 fJ/bit(EDR) 108 fJ/bit (HBR)	850 nm VCSEL	25°C	40 Gbps	4 μm (oxide-aperture diameter)	[139]
168 fJ/bit(EDR) 139 fJ/bit (HBR)	980 nm VCSEL	85 °C	35 Gbps	3 μm (oxide-aperture diameter)	[140]
100 fJ/bit(EDR)	980 nm VCSEL	85°C	40 Gbps	5 μm(oxide-aperture diameter)	[141]
431 fJ/bit (EDR) 395 fJ/bit (HBR)	850 nm VCSEL	20°C	40 Gbps	4 μm (oxide-aperture diameter)	[142]
578 fJ/bit (EDR) 477 fJ/bit (HBR)	850 nm VCSEL	85°C	40 Gbps	7 μm(oxide-aperture diameter)	[143]
510 fJ/bit (HBR)	850 nm VCSEL	20°C	57 Gbps	8 μm(oxide-aperture diameter)	[144]
73/95 fJ/bit (HBR)	850 nm VCSEL	20°C	40/50 Gbps	3.5 μm(oxide-aperture diameter)	[145]
320 fJ/bit(EDR)	850 nm VCSEL	25°C	64 Gbps	5 μm (oxide-aperture diameter)	[122]
NA	850 nm VCSEL	28 °C	71 Gbps	5 μm (oxide-aperture diameter)	[124]
245 fJ/bit(EDR)	850 nm VCSEL	25°C	56.1 Gbps	7 μm(oxide-aperture diameter)	[115]
228 fJ/bit(EDR)	850 nm VCSEL	85 °C	41 Gbps	8 μm(oxide-aperture diameter)	[146]
180 fJ/bit(EDR) 140 fJ/bit (HBR)	1060 nm VCSEL	20°C	10 Gbps	NA	[147]
203 fJ/bit(EDR) 177 fJ/bit (HBR)	980 nm VCSEL	85°C	38 Gbps	20 μm (top mesa diameter) 5.5 μm (oxide-aperture diameter)	[148]
302 fJ/bit (HBR)	980 nm VCSEL	25°C	50 Gbps	4.5–5 μm (oxide-aperture diameter)	[149]
287 fJ/bit(EDR) 233 fJ/bit (HBR)	980 nm VCSEL	25°C	35 Gbps	4 μm (oxide-aperture diameter)	[150]
470 fJ/bit(EDR) 330 fJ/bit (HBR)	850 nm VCSEL	25°C	32 Gbps	9 μm (oxide-aperture diameter)	[151]
456 fJ/bit	850 nm VCSEL	85 °C	50 Gbps	5 μm (optical modal diameter)	[152]
171 fJ/bit	DFB laser	20°C	25.8 Gbps	73 μm x 1 μm	[153]
750 fJ/bit	Hybrid III-V (InP)on SOI	NA	NA	5 μm^2	[154]
800 fJ/bit	hybrid III-V on Si	70°C – 80°C	25 Gbps	NA	[155]
500/644 fJ/bit	Hybrid III-V (InP) on Si	25°C/50°C	25.8 Gbps	96 μm^2	[156]
82.5 fJ/bit	Microdisk InP	20 °C	NA	7.5 μm^2	[157]
10 fJ/bit	Metallic cavity semiconductor nanolasers	20 °C	50 Gbps	400 nm diameter	[158]
13 fJ/bit	Photonic crystal nanocavity laser w/wo QD	20 °C	5 GHz	NA	[159]
8.76 fJ/bit or 175.2 μW	InGaAsP/InP BH PhC laser	20 °C	20 Gbps	dimensions: 5.0 x 0.3 x 0.15 μm^3	[160, 161]
4.4 fJ/bit - 44 μW	PhC laser LEAP	25 °C	10 Gbps	2.6 μm × 0.3 μm × 0.15 μm	[162]
5.5 fJ/bit	PhC laser LEAP	20 °C	10 Gbps	2.6 μm × 0.3 μm × 0.15 μm	[163]
10.5 fJ/bit	PhC laser LEAP	25 °C	25 Gbps	2.6 μm × 0.3 μm × 0.15 μm	[126]
0.25 fJ/bit 2.5 μW	Photonic Crystal Nanocavity LED with QD	20 °C	10 GHz	NA	[164-167]
1.15 fJ/bit	El driven Plasmonic nanoLED	NA	0.1 Gbps	80 nm x 4 μm	[168]

*NA-Non Available

EDR: electrical energy-to-data ratio. *HBR*: heat-to-bit rate ratio [110]

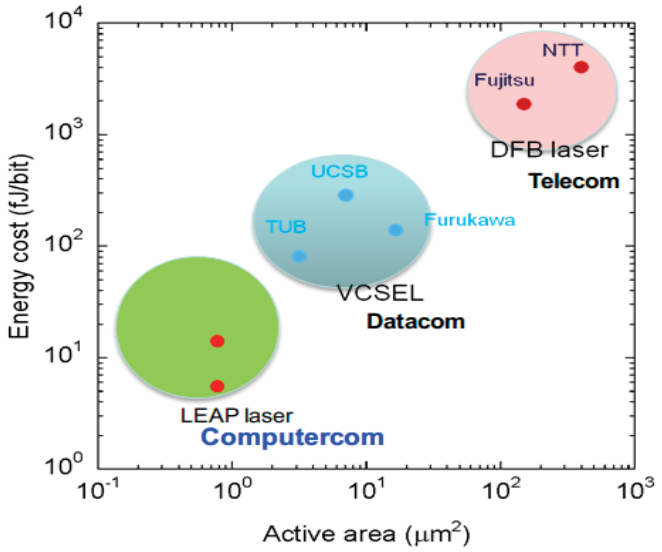

Fig. 11. Energy cost as a function of active region footprint for three different laser technologies (LEAP laser, VCSEL, DFB laser) [169].

DFB laser structures are far less energy efficient with energies at a few pJ/bit, so they are out of the question for the on-chip application addressed here. Some recent research efforts [153, 156] in the field of DFB lasers have shown a better energy performance with a 499 fJ/bit and a 171 fJ/bit respectively but they are still far from the goal of 10 fJ/bit. Photonic crystal nanocavity lasers (or even LEDs), with or without quantum dot gain region for amplification, or silicon nanowire laser structures may stand a chance to be possible on chip transmitters for the future energy requirements, with energies from a few fJ up to 10 fJ/bit, as can be seen in the Table 4. LEAP (lambda-scale embedded active-region photonic-crystal) lasers, are considered the most promising directly modulated transmitter, for meeting future energy requirements. Moreover they can be fabricated with photonic crystal diodes on the same wafer, thus creating on chip optical links consisting of LEAP laser transmitters and photonic crystal (PhC) photodiodes as receivers [170]. Plasmonics may play a key role in the case of directly modulated transmitters, with nanolasers or even nanoLED of metallo-dielectric cavities, consuming power at the microwatt region, but at modest operating rates of up to a few tens of Gbps. In order to compensate the lossy plasmonic material, SPACER technology (Surface Plasmon Amplification by Stimulated Emission of Radiation) on boosting currents and power accordingly, has been adopted [171].

B. External Modulation Sources

By using on chip modulators fed by an external laser source, instead of a directly modulated source, low energies can also be achieved. Unlike lasers, modulators do not have a threshold that could limit the minimum operating energy. However, although the inherent power consumption of those devices is comparably small (fJ/bit range), the main contributors for these components are their electrical drivers needed for the modulation (pJ/bit range). Due to the high voltage requirements of the modulators, their drivers consume much more energy (pJ/bit range) than the VCSEL drivers (fJ/bit range) for the same high speeds. Therefore, nowadays VCSEL-based solutions are still more energy-efficient than the externally modulated ones.

There are two main modulator classes. First, the interferometric Mach-Zehnder modulators (MZMs), that rely on changes of the relative phase of the interfering beams by changing the refractive index, that lead to changes of the output power. Second, electro absorption modulators (EAMs), that rely on changes of the optical absorption in a semiconductor structure. Electro-absorption modulators (EAM) exploit the Franz-Keldysh (FK) effect or the Quantum-Confined Stark (QCS) effect in epitaxially grown GeSi or Ge [172]. Typical MZMs require long arm lengths in order to achieve strong refractive index changes, so they require large footprints. One solution would be the use of other materials with higher refractive index changes, such as electro-optic polymers (EOP) [173]. Electro-optical in-phase and quadrature (IQ) modulators are key elements for spectrally efficient coherent transmission in high-speed telecommunication links and optical interconnects [173]. Plasmonic modulators have also been successfully tested experimentally, achieving high modulation rates, at short device lengths [87, 91, 174, 175]. In addition, low loss plasmonic electro-optic ring modulators with low on-chip optical losses (2.5 dB), high-speed operation (>>100 GHz), and good energy efficiency (12 fJ/bit) have been presented in [176]. Another alternative would be the use of ring resonators in order to enhance the effect of changing the refractive index in only a smaller length of material [177]. ITO and graphene based plasmonic modulators have shown outstanding performances in terms of operational bandwidth and energy efficiency [178, 179] in simulations, but their THz operation remains to be experimentally proven. In [84], a conservative estimation for the modulation bandwidth and energy consumption of a field-effect plasmonic modulator (ITO-filled) [180] has demonstrated values of 500 Gbps and 4 fJ/bit respectively underlining the great potential of this technology.

In Table 5 we perform a comprehensive review of all the latest photonic and plasmonic modulators. Using the data of Table 5, a detailed comparison (with respect to energy efficiency) between the different modulator technologies is implemented in Figures 14, 17.

Figure 12 shows the evolution of the bandwidth over the last 15 years for integrated photonic and plasmonic modulator as well as directly modulated VCSELs [99]. The size of the symbol indicates the required footprint and the shape of the symbol indicates the effect it relays on. It can be seen that photonic modulators have experienced a steady but moderate increase in bandwidth over the years (blue arrow). The plot also shows that newer plasmonic modulators present higher bandwidth performance than photonic counterparts at a much smaller footprint (red arrow).

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TABLE 5
PHOTONIC AND PLASMONIC MODULATORS.

Energy/Power consumption	Description	Bit rate/BW	Area	Reference
640 fJ/bit	SOH electro-optic (EO) polymer MZM	112 Gbps (56 Gbps just below the FEC limit)	1.5 mm x 140 nm	[181]
420 fJ/bit	SOH electro-optic (EO) MZM	40 Gbps	length 250 μm	[182]
18 fJ/bit	SOH electro-optic (EO) MZM	52 Gbps	length 1.5 mm	[183]
19 fJ/bit	SOH electro-optic (EO) modulators	112 Gbps	length 1.5 mm	[184]
94.4 fJ/bit	SOI photonic crystal MZM (EO) polymer	10 Gbps	300 μm x 320 nm	[185, 186]
56 fJ/bit	Node-Matched-Diode Silicon Modulator	25 Gbps	220 nm x 450 nm	[187, 188]
100 fJ/bit (2.5 mW)	Ge FKE EAM	25 Gbps	1.0 μm × 45μm	[189]
60 fJ/bit	Ge Si FKE EAM	28 Gbps	1.0 μm × 55 μm	[190]
50 fJ/bit	Ge Si FKE EAM	1.2 Gbps	30 μm^2	[191]
12.8 fJ/bit	Ge Si FKE EAM	56 Gbps	40 μm ×10 μm	[192]
76.5 fJ/bit	MZI assisted ring modulator	25 Gbps	0.48 mm^2	[193]
50 fJ/bit	Silicon microring	10 Gbps	1000 μm^2	[194]
15 fJ/bit	Silicon microring	66 Gbps	NA	[195]
7.9 fJ/bit	Silicon microring	1 Gbps	20 μm^2	[177]
3 fJ/bit	Silicon microdisk	12.5 Gbps	10 μm^2	[196]
0.9 fJ/bit	Silicon microdisk	25 Gbps	4.8 μm diameter	[197]
0.7 fJ/bit	SOH nanophotonic MZM	12.5 Gbps	1 mm x 160 nm	[198]
0.75 fJ/bit (500 μW)	Ge on Si	3.5 GHz	8 μm^2	[199]
1.1 fJ/bit	GaAs PhC EOM	100 GHz	NA	[200]
70 fJ/bit	POH Mach-Zehnder modulator	40 Gbps	length 29 μm	[201]
25 fJ/bit	All plasmonic EOP	54 Gbps	length 5 μm	[87]
2.84 fJ/bit	POH Mach-Zehnder Modulator	100 Gbps	300 μm × 370 μm	[91]
12 fJ/bit	Plasmonic EO ring modulator	>>100 GHz	NA	[176]
18 fJ/bit	EOP polymer	40 Gbps	length 29 μm	[174]
20 fJ/bit	Plasmonic MZ	72 Gbps	10 μm x 1.5 μm	[202]

*NA-Non Available

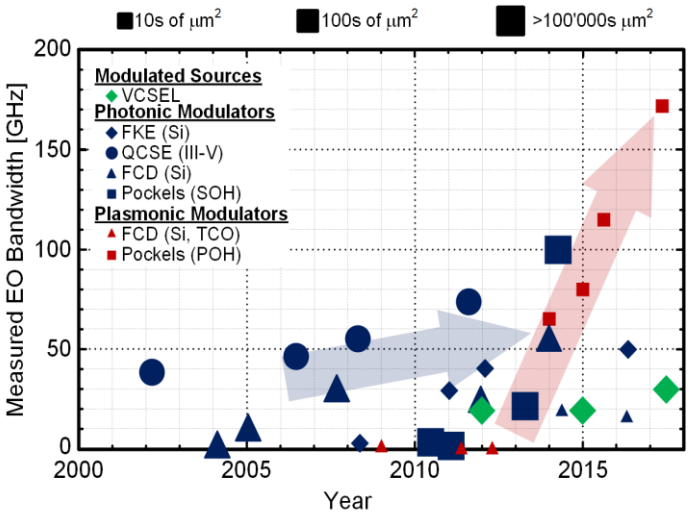

Fig. 12. Bandwidth and footprint of electro–optical integrated modulators (experimental results only) [99].

C. *Photodetectors*

It is known that wishful features for photodetectors are large responsivity, at low dark current and capacitance, and high sensitivity and bandwidth. Although sensitivity is the most important attribute for a photodetector in long distance communications [203], for short distance interconnects the total energy dissipated per bit becomes the most critical factor. Receiver circuits can dissipate, in some cases, the largest portion of energy in a link [14]. For this reason, in order to reduce power consumption overall, one approach is to reduce the total energy dissipation at the receiver side [203].

Photodetector's received optical energy is directly related with transmitter optical output power and the total link loss power budget, which includes total link attenuation, coupling losses and eventually, a power margin. Hence, for 10 fJ/bit transmitted optical energies, the received optical energy would be 1 fJ/bit (1eV photons) in a reasonable optical system allowing for various losses [51, 129]. So we are targeting for photodetectors with total capacitance of a few fF at most, in order to compete as possible receivers for future on chip interconnections.

Typical photodetector structures are P-N, or PIN heterojunctions built by semiconductor materials, such as Si, Ge, and III-V material, and Schottky structures. For low power consumption and high speed circuits, the goal for the detector is to reduce its capacitance by shrinking its size into the nanoscale. A main representative photodetector in the field of silicon photonics is a Ge based detector, built on silicon substrate forming either PIN or APD structures. The latter has better sensitivity than the PIN type detectors, at the expense of higher noise and lower speed though [204, 205]. Furthermore, APDs need very high voltages and accurate voltage control for their operation which are the main limiting factors for an application in practical systems. A lot of research has also been conducted on III-V nano-needle structures [206-208].

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TABLE 6
PHOTONIC AND PLASMONIC DETECTORS.

Bit rate/BW	Description	Capacitance	Responsivity	Bias voltage	Dark current	Energy Consumption	Sensitivity	Area	Ref.
3 Gbps	Ge PD	4 fF	0.8 – 0.9 A/W	-1 V	1.4 μA	33 fJ/bit (PD only)	NA	Length 40 μm	[120]
40 Gbps	Ge PD on Si	2.4 fF	NA	-5 V	4 μA	NA	NA	Length 30 μm	[209]
45 GHz	Ge PD	1 fF	0.8 A/W	-1 V	3 nA	NA	NA	1.3 μm x 4 μm	[210]
28 Gbps	Ge PD	NA	>1.0 A/W	-1 V	~ 3 nA	NA	−15.9 dBm	13.8 μm x 0.5 μm	[211]
> 70 GHz	Ge PD	10.5 fF	1 A/W	-1 V	100 nA	NA	NA	3 μm x 20 μm	[212]
10 Gbps	Ge APD on Si	NA	0.55 A/W	-22 V	~ 10 μA	NA	-28 dBm	Diameter 30 μm	[204]
6.24 GHz	Ge-on-Si APD	NA	54.5 A/W	-31 V	~ 27 μA	NA	−18.3 dBm	1000 nm wide	[205]
12 GHz	APD on Si	4fF	0.03 A/W	-10 V	~ 0.1 nA	NA	NA	5 μm × 5 μm	[213]
25 Gbps	Si–Ge APD	NA	1.05 A/W	-1 V	0.1 nA	NA	-16 dBm	4 μm × 50 μm	[214]
20 Gbps	InGaAs PD	200 fF	0.5 A/W	NA	NA	0.705 pJ/bit (Total Receiver)	−5.8 dBm	250 μm x 250 μm	[215]
10 Gbps	InP /InGaAs PD	0.12 – 0.23 fF	1 A/W	-4 V	40 nA	NA	NA	3.4 μm long	[216]
26 Gbps	InP /InGaAs PD	125 fF	0.85 A/W	NA	NA	NA	NA	32 μm active diameter	[116]
10 GHz	PhC InGaAs PD	1 fF	1 A/W	- 10 V	15 nA	1 fJ/bit (PD only)	−20 dBm	Length 1.7 μm	[217]
25 Gbps	Waveguide PD on Si	30 fF	0.2 A/W	NA	NA	170 fJ/bit (Total Receiver)	-14.9 dBm	NA	[218]
NA	Nanometallic Antenna PD	5 aF	NA	NA	NA	NA	NA	Active volume 0.00072 μm^3	[219]
NA	Au Nanoantenna into GaAs NW	80 aF	NA	NA	NA	NA	NA	12 μm long, diameter 70 nm.	[220]
NA	Nanometallic resonator PD in Ge	NA	1.2 A/W	NA	NA	NA	NA	975 nm wide and 300 nm thick	[221]
40 Gbps	Plasmonic PD	NA	>0.12 A/W	NA	NA	NA	NA	<1 μm^2	[222]

*NA-Non Available

On the other hand, there are the plasmonic-based photodetectors that can be categorized into two types, depending on the way they accept the optical data. In the first detector type, optical data are converted to plasmonic, and the challenge is to match the large photonic mode to a tiny plasmonic one, before it can be absorbed and detected later on. This can be achieved with the use of apertures to confine optical beams and tapered nanometallic waveguides, with incredible performances, concerning energy efficiency. A comparably new approach is the use of optical antennas converting the optical far field into a localized near field. The second detector type is based on plasmonic integrated circuits, and a typical structure is a crossing of a metal and a semiconductor Ge nanowire, to form a Schottky junction. Ge particles absorb incoming optical data, creating electron-hole pairs, which can be, later on, extracted by the plasmon polariton waveguide, allowing for a densely integrated design.

As can be seen from the Table 6, plasmonic detector schemes can be much more energy-efficient than nanophotonic competitors, providing energies at the attojoule levels. Plasmonic detector offers multiple advantages such as high integration densities, low device capacitance allowing for higher bandwidth operation, and ultra-low energies to operate, owing to enhanced light mechanisms with gain induced techniques [222].

D. Passive devices: waveguides and couplers

Table 7 shows photonic (SOI), plasmonic based waveguides and hybrid versions of them along with their attenuation losses. Table 8 shows coupling losses of a conventional coupler, and a coupler used for photonic to plasmonic mode conversion. Plasmonic waveguides show propagation losses in the order of dB/μm, while their photonic counterparts, are in the order of dB/cm. A solution, as mentioned, would be to compensate loss with gain, e.g. by using either nanoparticles (QD with gain), or SPACER mechanism [171], however this would have a significant impact on the overall power efficiency. Still, the maximum interconnection length that can be supported by plasmonic waveguides, before becoming too lossy, is around 100 μm [90], which is too low for supporting chip-level interconnections. Many sublinks would be required in order to reach global spans. A modulator and a detector should be used for each link, with detector of the current link driving the modulator of the next link. Thus the most appropriate link, scenario, is the hybrid link, that consists of high-speed plasmonic modulator in conjunction with energy-efficient conventional photonic waveguides. In [90] it has been shown that hybrid channels are clearly more energy-efficient than pure photonic and plasmonic channels at any length, and become more energy-efficient than electrical from 200 μm which means that they can be used, even for the shortest type of on chip interconnects. The only additional loss they require is the photonic to plasmonic mode conversion coupling and vice versa, which as can be seen in Table 8, is very low, adding only a few dBs more on the total link budget.

TABLE 7
PHOTONIC AND PLASMONIC WAVEGUIDES

Material	Attenuation	Reference
silicon core on insulator (SOI)	0.5 dB/cm	[223]
silicon core on insulator (SOI)	1.4-4.5 dB/cm	[224]
polymer	0.024 dB/cm	[225]
plasmonic(M-I-Si.I-M)	0.28-0.3 dB/µm	[226]
Slot-line	3.0733 dB/µm	[227]
Hybrid plasmonic	0.01-0.22 dB/µm	[227]

TABLE 8
COUPLERS

Description	Coupling loss	Reference
Fiber to Si waveguide	< 1 dB	[228]
photonic to plasmonic mode conversion	1.1 dB	[229]
coupling losses per Si-to-DLSPP interface	2.5 dB	[98]

E. Electrical circuitry

Besides the active and passive optical components in an optical transmission system, various electronic components are required. These components are designed as integrated circuits (IC) using modern semiconductor technologies such as silicon-based CMOS and BiCMOS as well as III-V technologies. While standard CMOS provides low-cost volume fabrication and highly energy-efficient circuits, it needs additional methods to achieve high bandwidth, for instance bandwidth peaking techniques using inductors. Therefore, the chip area becomes very large since common planar inductors are placed in parallel to the semiconductors substrate. Another option is the application of vertical inductors [230]. For integrated vertical inductors the spiral is oriented perpendicularly to the substrate by using several metal layers and vias of the stack. Thus, the inductance per unit of area can be increased significantly. It has been proven that such vertical inductors can be used for inductive peaking in broadband amplifiers [231], where the bandwidth was enhanced by 25%. Furthermore, the big advantage of CMOS is the seamless integration together with digital circuitry and processors to very-large integrated systems like system or network on chip (SoC/NoC). BiCMOS technologies offer higher bandwidths but at the cost of higher power consumption. Similarly, III/V technologies provide even higher bandwidth at even higher power consumption. Therefore, the technology choice is always a trade- off between required bandwidth, energy efficiency, and chip area. However, it has been shown that BiCMOS ICs can achieve a well-balanced performance to meet all those requirements [232].

In an electro-optical transceiver the following analog ICs are present:

1) Laser diode driver (LDD) and modulator driver (MD): At the transmitter side, the LDD and MD drive the laser and modulator for the E/O conversion. They provide the optical components with their bias voltages and currents, thus setting their operating points. Most importantly, the drivers apply the transmitting signal to the laser or modulator for modulation. In this regard, the circuits act also for electrical matching. To achieve sufficient extinction ratio for the modulation, sufficiently high modulation voltages or currents are required. Modern semiconductor technologies suffer from low breakdown voltages of the transistors below 2 V. However, for driving the lasers or electro-optical modulators voltage swings exceeding this breakdown voltage, are often required. Thus, concepts for achieving high voltage swings such as voltage multipliers or breakdown voltage doublers need to be implemented. Especially modulators need very high voltage swings. Therefore, the drivers consume very higher power which can be usually above 1 W. Whereas the modulators themselves consume almost no power since they act as a capacitive load for the drivers.

2) Transimpedance and limiting amplifier (TIA/LA): TIA and LA are receiver amplifiers. The TIA converts the photocurrent from a photodetector into a voltage and amplifies the received signal. The LA further amplifies the voltage signal to logic levels and since it goes to saturation it shapes the signal to steep edges. The receiver amplifier and especially the TIA input stage is the most critical part in the receiver chain since it has to cope with very weak signals. Therefore, the TIA has to be very low-noise to enable a high input sensitivity. On the other, hand sufficient bandwidth is required to mitigate ISI. Therefore, a trade-off between bandwidth and sensitivity has to be found. Furthermore, high linearity is needed in case signal with multiple levels have to be received.

An overview about the state of the art of LDDs, MDs and TIA/LAs is given in Table 9, Table 10 and Table 11.

TABLE 9
SINGLE CHANNEL LASER DIODE DRIVER (LDD) STATE OF THE ART

Technique	Data rate	Power consumption	Active Chip Area w/o pads (Inductors L)	Technology	Ref.
NRZ	25 Gbps	60 mW	0.006 mm^2 (w/o L)	90 nm CMOS	[233]
NRZ	35 Gbps	30 mW	0.002 mm^2 (w/o L)	32 nm SOI CMOS	[121]
NRZ	15 Gbps	28.1 mW (1.9 pJ/bit)	0.04 mm^2	65 nmCMOS	[234]
NRZ	10 Gbps	69.5 mW (6.9 pJ/bit)	0.128 mm^2	65 nmCMOS	[235]
NRZ	26 Gbps	46.9 mW (1.8 pJ/bit)	0.024 mm^2	65 nmCMOS	[236]
NRZ	17 Gbps	60 mW	0.003 mm^2	80 nm CMOS	[237]
NRZ	25 Gbps	60 mW (2.4pJ/bit)	0.09 mm^2	8 HPBiCMOS	[238]
Pre-emphasis	40 Gbps	130 mW	0.06 mm^2 (w/ L)	250 nm BiCMOS	[239]
Pre-emphasis	15 Gbps	30 mW	0.04 mm^2 (w/ L)	65 nm CMOS	[240]
Pre-emphasis	10 Gbps	85 mW	4 mm^2 (w/ L)	130 nm CMOS technology	[241]
Pre-emphasis	48 Gbps	188 mW	0.019 mm^2 (w/ L)	130 nm SiGe BiCMOS technology	[242]
Pre-emphasis	40 Gbps	312 mW	0.5 mm^2	130 nm SiGe	[243]
NRZ(FFE)	71 Gbps	959 mW	1 mm^2 (w/ L)	130 nm BiCMOS	[124, 244]
NRZ (FFE)	42 Gbps	117 mW	0.17 mm^2	14 nm CMOS	[245]
NRZ (FFE)	50 Gbps	190 mW	0.036 mm^2	130 nm SiGe BiCMOS	[246]
PAM4	56 Gbps	39 mW	0.75 mm^2 (w/ L)	65 nm CMOS	[247]
PAM4	56 Gbps	207 mW (3.7 pJ/bit)	0.7344 mm^2	0.25µm InP DHBT Technology	[248]
PAM4	20 Gbps	34.1 mW	0.31 mm^2	90 nm CMOS technology	[249]
PAM4	90 Gbps	177 mW	0.0225 mm^2	130 nm SiGe BiCMOS	[250]

TABLE 10
MODULATOR DRIVER (MD) STATE OF THE ART

Data rate	Differential Gain	Power consumption	Differential Output Voltage Swing	Direct Modulator Integration	Technology	Ref.
10 Gbps	21.6 dB	98 mW	6 V_{pp}	No	65 nm CMOS	[251]
20 Gbps	40 dB	312 mW	3.4 V_{pp}	No	130 nm CMOS	[252]
10 Gbps	n/a	1.25 mW	2 V_{pp}	No	40 nm CMOS	[253]
25 Gbps	n/a	520mW	3.2 V_{pp}	No	65 nm CMOS	[254]
10 Gbps	n/a	98 mW	6 V_{pp}	No	65 nm CMOS	[127]
46 Gbps	n/a	130 mW	2 V_{pp}	No	32 nm CMOS (PAM-4)	[255]
40 Gbps	13 dB	1.35 W	6 V_{pp}	No	0.25 µm BiCMOS	[256]
10 Gbps	40 dB	0.87 W	5.6 V_{pp}	Yes	0.25 µm BiCMOS	[257]
10 Gbps	n/a	58.7 mW	3 V_{pp}	No	0.35 µm BiCMOS	[258]
56 Gbps	n/a	0.45 W	n/a	No	130 nm BiCMOS	[259]
28 Gbps	14.5 dB	2 W	4 V_{pp}	Yes	0.25 µm SiGe:C BiCMOS	[260]
32 Gbps	n/a	0.96 W	3 V_{pp}	Yes	0.25 µm SiGe BiCMOS	[261]
40 Gbps	13.6 dB	1.125 W	2.5 V_{pp}	No	80 GHz SiGe	[262]
11.3 Gbps	n/a	880 mW	6 V_{pp}	No	SiGe bipolar	[263]
224 Gbps	15 dB	3.2 W	2.5 V_{pp}	No	InP bipolar (16QAM)	[264]
100 Gbps	n/a	183 mW	n/a	No	0.25 µm InP DHBT(PAM-4)	[248]
90 GHz	n/a	550 mW	4 V_{pp}	No	130 nm SiGe BiCMOS	[265]

TABLE 11
TIA STATE OF THE ART

BW/ GHz	Gain / dBΩ	Noise / pA/√Hz	P_{DC} / mW	Efficiency / pJ/bit	Chip area / mm^2	Impedance (Ω)	Inductive Peaking	Technology	Ref.
20	398	50	2.2	0.08	N/A	50	Yes	80 nm CMOS	[266]
30	562	20.5	9	0.21	0.29	50	Yes	45 nm CMOS	[267]
31	350	55.7	60	1.35	0.54	54	Yes	180 nm CMOS	[268]
35	280	N/A	270	5.4	0.55	N/A	No	90 GHz BiCMOS	[269]
35	473	11	14	0.28	0.16	100	No	0.13 µm BiCMOS	[270]
45	323	N/A	300	4.67	2.16	N/A	No	105 GHz BiCMOS	[271]
50	140	30	182	2.55	0.92	50	No	200 GHz BiCMOS	[272]
61.6	69.8	19.7	78.1	0.89	0.44	N/A	No	130 nm BiCMOS	[273]

As lasers for direct modulation usually have bandwidths not higher than 20-25 GHz, maximum optical data rates of 30 Gbps can be achieved with NRZ coding. For obtaining higher data rates several techniques such as pre-emphasis or feed-forward equalization (FFE) are implemented in the ICs. This enabled the demonstration of the highest date rate of 71 Gbps with direct VCSEL modulation to date [124]. However, as can be seen the power consumption of the transmitter becomes very high which makes the method unattractive for energy-efficient optical interconnects. An alternative approach is the multilevel modulation scheme which can reach to higher data rates for a given technology, but with even higher power consumptions. PAM4 for optical modulation is mostly demonstrated using HF measurement equipment together with DACs. An issue with PAM4 is that it has lower signal amplitude than NRZ (due to level spacing) and is more susceptible to noise. This needs to be compensated with technologies like FEC, which results in higher power consumption and latency. Although state of the art CMOS implementations show good power efficiency and high modulation speeds, the occupied chip area is rather large since peaking inductors are required. Therefore, those are less suitable for a direct integration with III-V components on silicon.

High-speed modulator drivers with high output voltage swings have been demonstrated mainly in BiCMOS technologies at the expense of a higher power consumption. CMOS MDs show lower power consumption but suffer from much lower bandwidths. However, most of the designs are not directly integrated with the optical modulator.

Various TIAs in different technologies have been published so far. As it can be seen, TIAs can show high bandwidth, high gain and low noise while they are still energy-efficient.

F. Results

The graphs in Figures 13-15, show minimum and maximum energy efficiency values, for each interconnect device module (laser sources, modulators and detectors) separately, specifying their implementation technology as well. Minimum and maximum values can be seen in labels on each column in fJ/bit unit, though they are represented in axes in logarithmic scale for better value fitting.

Concerning directly modulated sources, as can be seen from Figure 13, the best energy performance comes from InP based photonic crystal nanocavity, or LEAP lasers with energies from a few fJ up to 10 fJ/bit, hence capable of meeting future energy requirements. Their energy performance can almost compete with plasmonic nano-LED structures with energies of just a few fJ. VCSELs and hybrid III-V on Si laser structures, are far less energy efficient with energies more or less a few hundred fJ, with the best performance lying at sub hundred fJ and hence they cannot be considered capable of meeting future on-chip energy requirements, though they are state of the art transmitters for board to board interconnections nowadays.

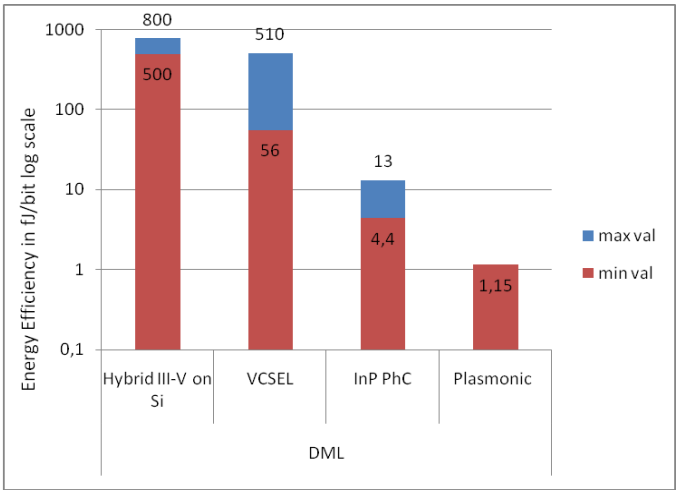

Fig. 13. Energy efficiency of directly modulated sources (data from Table 4)

Regarding modulators, as can be seen from Figure 14, the best energy performance comes from nanoscale silicon photonics based modulators with energy performance ranging from a sub-fJ up to 10 fJ. However, this is not always the case, since, other photonic modulator structure energies usually vary from a few hundred of fJs up to sub hundred fJs, such as hybrid InP on silicon, Ge on silicon, or silicon organic polymer modulator structures. Plasmonic modulators [87, 91, 99, 174, 202] really stand a good energy performance lying from 2.84 to a few tens of fJs, slightly above the best performance of photonic modulators.

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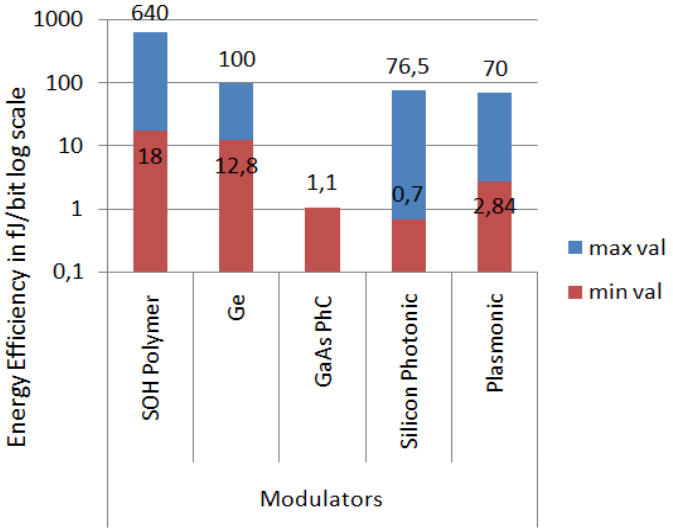

Fig. 14. Energy efficiency of modulators (data from Table 5)

Concerning the receiver side, as one can see from Figure 15, energy performance superiority of a plasmonic photodetectors (integrated Ge, or nanoantenna structures), is crystal clear, compared with a typical Ge photodetector on Si or even enhanced with avalanche mechanism. Plasmonic integrated Ge photodetector total parasitic capacitance lies between 10 and 100 aF, thus giving energies between 10 and 100 aJ, respectively, considering an 1V typical drive swing voltage, which are orders of magnitude less than the aforementioned energies of a typical Ge on Si photodetector.

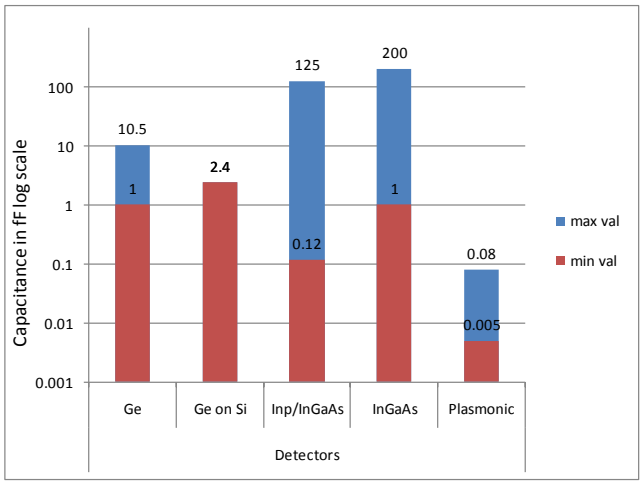

Fig. 15. Capacitance of photodetectors (data from Table 6)

As can be deducted from Figures 13-15, the bottom line is that, with the exception of photodetector energy performance comparison, photonic based chip interconnect modules are considered to be comparable to plasmonic based ones in terms of energy efficiency. However, plasmonic based devices strong point is actually their relatively ultra-small dimensions leading to high integration densities, and with their low device capacitance allowing for ultra-high bandwidth operation. It is then worth it, comparing chip module bandwidth density versus energy efficiency, to observe another point of comparison view among the aforementioned technologies.

Figures 16-18, show energy efficiency versus bandwidth density values, for each interconnect device module (laser sources, modulators and detectors) respectively, specifying their implementation technology as well. We observe that by reducing the active area, we can effectively reduce the energy cost.

Concerning directly modulated sources, as can be seen from Figure 16, the best combined performance comes from InP based photonic crystal nanocavity, and plasmonic nano LED structures. Concerning modulators, as can be seen from Figure 17, the best energy efficiency comes from nano scale silicon photonics. Finally, in Figure 18 it is clearly shown that plasmonic photodetectors are by far the most energy-efficient solution

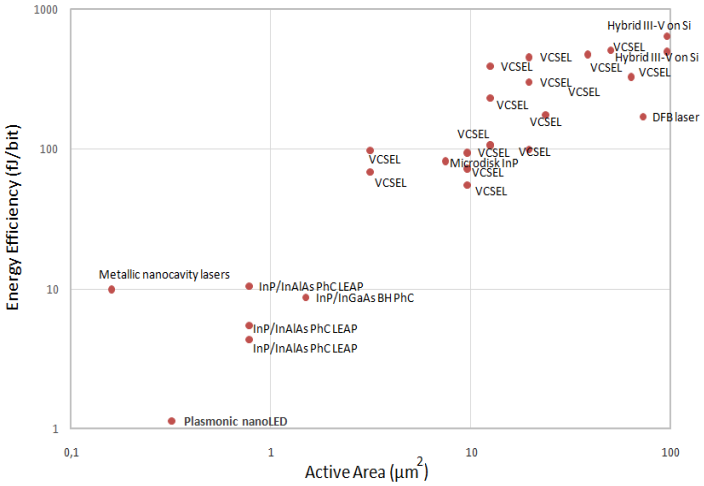

Fig. 16. Active area vs energy efficiency for directly modulated sources (data from Table 4)

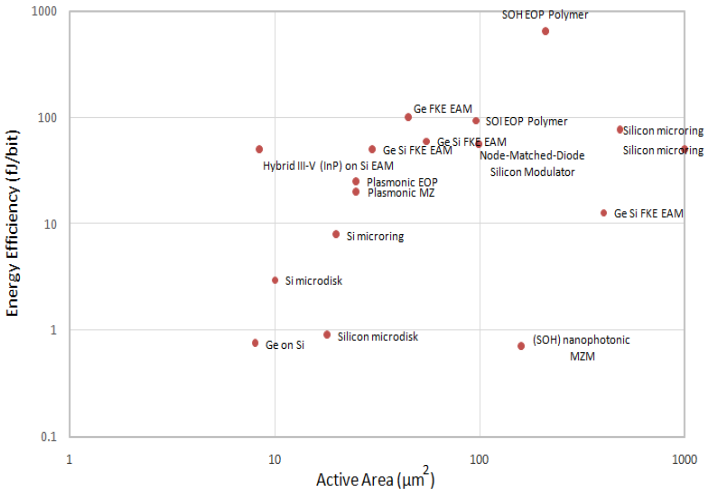

Fig. 17. Active area vs energy efficiency for modulators (data from Table 5)

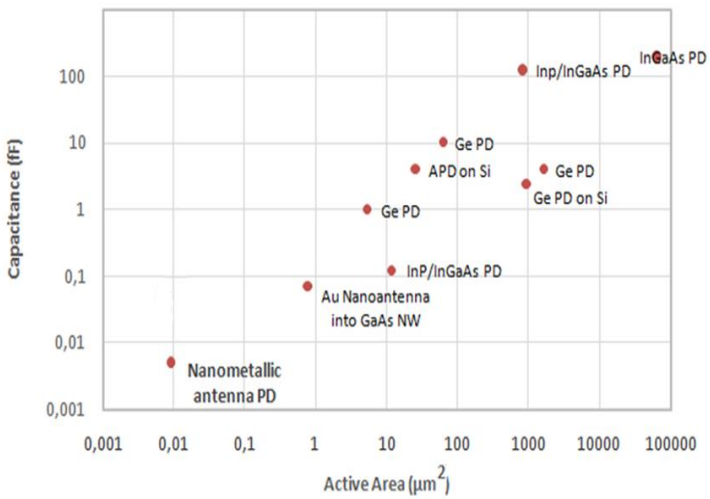

Fig. 18. Active area vs capacitance for photodetectors (data from Table 6)

V. Conclusions

This survey has brought up many critical matters concerning future short-reach interconnections and the possible technologies to realize them. On one side, there are the market trends that anticipate better and better HPC and DC performance scalability, within short term time periods. The resulting scaling trends set tight targets that, although difficult to achieve, the technology vendors will sooner or later have to comply with. On the other side, there are the capabilities of competing interconnect technologies, predecessor ones, such as conventional electrical interconnects, and future promising ones, such as photonic and plasmonic technologies. Along with the proper technology choice, other choices must be made as well, such as integration method (i.e. hybrid or monolithic), packaging process, and NoC architecture.

This paper compares conventional electrical, photonic and plasmonic short distance interconnect technologies in terms of bandwidth density and energy efficiency, based on the latest literature data. These three technologies were also compared at the device level, including output devices, photodetectors, passive devices and electrical circuitry.

At the transmitter side, and specifically concerning direct modulated sources, VCSELs with MMF and/or polymer waveguides is the current state of the art technology, that in the future may be substituted by the most promising silicon photonic technology at nanoscale basis or plasmonic technology. Photonic crystal nanocavity lasers or plasmon nano-LED structures may well be considered as chip transmitters that could meet the future energy bandwidth density requirements. Also, externally modulated lasers, such as silicon micro- and nanoscale photonic modulators, or plasmonic modulators (hybrid or plain) can reach energies, from a sub-fJ up to a few tens of fJ. Thus, they adequately support energy efficient transmission for future on-chip interconnections. Moreover, plasmonic modulator structures can reach ultra-high levels of bandwidth density and, for this reason, may be more suitable for integration purposes than their photonic counterparts.

At the receiver side, in order to have low power consumption and high speed circuits, the ultimate target for the detector is to reduce its capacitance by shrinking its size and thus increasing its bandwidth density. Ge-based detectors built on silicon substrate forming PIN or APD photodetectors can be adequately considered as energy efficient receivers for future interconnect demands. Plasmonic detectors can be even more energy efficient, reaching energies at attojoule levels with capacitance at attofarad levels (one order of magnitude lower than photonics); they have the greatest integration potential due to their superior bandwidth densities.

Based on all these findings, the comparison showed that both photonic and plasmonic technologies can be used for energy-efficient interconnects that could meet future prospects. Additionally, our comparison of bandwidth-density versus energy-efficiency showed that the smaller dimensions and lower capacitances of plasmonic-based devices, compared to photonics-based devices, may ultimately enable higher integration densities and higher bandwidths and lower costs for ultra-short links.

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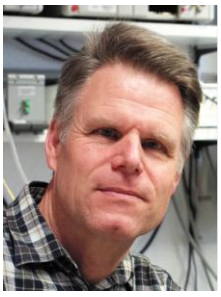

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