DOCTORAL DISSERTATION

学位論文要旨

CHARACTERIZATION AND OPTIMIZATION OF AVALANCHE PHOTODIODES FABRICATED BY STANDARD CMOS PROCESS FOR HIGH-SPEED PHOTORECEIVERS

高速光レシーバの実現に向けた CMOS アバランシェ光検出器の特性評価と最適化

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ABSTRACT

A dissertation presented on the characterization and optimization of avalanche photodiodes fabricated by standard CMOS process (CMOS-APD) for high-speed photoreceivers, beginning with the theory and principle related to photodetector and avalanche photodiodes, followed by characterization, optimization, and wavelength dependence of CMOS-APD, and finally link up with the transimpedance amplifier. nMOS-type and pMOS-type silicon avalanche photodiodes were fabricated by standard 0.18 μm CMOS process, and the current-voltage characteristic and the frequency response of the CMOS-APDs with and without the guard ring structure were measured. CMOS-APDs have features of high avalanche gain below 10 V, wide bandwidth over 5 GHz, and easy integration with electronic circuits. In CMOS-APDs, guard ring structure is introduced for high-speed operation with the role of elimination the slow photo-generated carriers in a deep layer and a substrate. The bandwidth of the CMOS-APD is enhanced with the guard ring structure at a sacrifice of the responsivity. Based on comparison of nMOS-type and pMOS-type APDs, the nMOS-type APD is more suitable for high-speed operation. The bandwidth is enhanced with decreasing the spacing of interdigital electrodes due to decreased carrier transit time and with decreasing the detection area and the PAD size for RF probing due to decreased device capacitance. Thus, an nMOS-type APD with the electrode spacing of 0.84 μm, the detection area of 10 x 10 μm², the PAD size for RF probing of 30 x 30 μm² along with the guard ring structure was fabricated. As a results, the maximum bandwidth of 8.4 GHz at the avalanche gain of about 10 and the gain-bandwidth product of 280 GHz were achieved. Furthermore, the wavelength dependence of the responsivity and the bandwidth of the CMOS-APDs with and without the guard ring structure also revealed. At a wavelength of 520 nm or less, there is no difference in the responsivity and the frequency response because all the illuminated light is absorbed in the p^+-layer and the Nwell due to strong light absorption of Si. On the other hand, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are eliminated by the guard ring structure for the wavelength longer than 520 nm, and then bandwidth

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was remarkably enhanced at the sacrifice of the responsivity. In addition, to achieve high-speed photoreceivers, two types of TIA which are common-source and regulated-cascode TIAs were simulated by utilizing the output of the CMOS-APDs. The figure of merits of gain-bandwidth product was used to find the ideal results of the transimpedance gain and bandwidth performance due to trade-offs between both of them. The common-source TIA produced the transimpedance gain of 22.17 dBΩ, the bandwidth of 21.21 GHz and the gain-bandwidth product of 470.23 THz × dBΩ. Besides that, the simulated results of the regulated-cascode TIA configuration demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth, and 845.35 THz × dBΩ gain-bandwidth product. Both of these TIA results meet the target of this research and further encouraging this successful CMOS-APDs to realize high-speed photoreceivers.

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ABBREVIATION

A - Ampere.

AC - Alternating current.

APD - Avalanche Photodiode.

CD-ROM - Compact Disc Read-Only Memory.

CMOS - Complementary Metal Oxide Semiconductor.

CR - Capacitance-Resistance.

CS - Common-source.

DC - Direct current.

DVD - Digital Versatile Disc.

FOM - Figures of merit.

FTTH - Fiber-to-the-home.

GaAs - Gallium Arsenide

GB - Gain-Bandwidth.

GR - Guard Ring.

Hz - Hertz.

InGaAs - Indium Gallium Arsenide.

InP - Indium Phosphide

I-V - Current-Voltage.

LAN - Local-area networks.

nMOS - N-type Metal Oxide Semiconductor.

PD - Photodiode.

pMOS - P-type Metal Oxide Semiconductor.

RGC - Regulated-cascode.

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SML - Spatial modulated light.

TIA - Transimpedance Amplifier.

V - Voltage

VCSEL - Vertical-cavity surface-emitting lasers.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Rapid emerging technology related to silicon photonics has been motivated to discover more inside its potential to be one of the most valuable findings for future development. With the advantages that exist in silicon, especially in regard to costs, it has encouraged us to make an inquiry in connection with the photoreceiver. Photoreceiver with monolithically integrated photodetectors are attractive and has a great potential of becoming one of the most important communication medium for short-distance optical data transmission for realizing local-area networks (LANs), fiber-to-the-home (FTTH) and board-to-board as well as chip-to-chip high-speed data transmissions [1]–[3]. They also can be used in optical storage systems such as Compact Disc Read-Only Memory (CD-ROM), Digital Versatile Disc (DVD) and Blue-ray Disc because it requires optical interfaces [4]–[6]. The main apparatus for all of this application is photodetector that has the capability to convert the light to electrical signal for further processing.

Although high-speed photodetectors are already commercialized mainly been implemented in III-V technology such as GaAs and InP-InGaAs for long-haul optical communication, the technology is expensive but the cost per user still low due to a large number of users. Therefore, it becomes the highest priority that a low-cost system implements in short-distance communication. This has been boost by the invention of low-cost vertical-cavity surface-emitting lasers (VCSELs) as light sources of transmitters. In order to realize the optical interconnection, it is necessary to integrate optical devices such as light sources, optical waveguides, and photodetectors with electronic circuits. By using CMOS process, it is possible to easily integrate photodetectors and electronic circuits on same Si substrate with low cost because CMOS process is a mature process.

The theory and principle behind the photodetector such as photodetection, quantum efficiency, responsivity, response speed, and etc. are needed to understand

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firmly. During the penetration of incident light onto the photodetector, the photon energy has to be equal or greater than the bandgap energy to excite an electron from the valence band up into the conduction band. When a photon is absorbed, both a minority and majority carrier are generated. Inside the photodetector, both of the carriers should be separated by a depleted semiconductor region with a high electric field. This depletion region has to be thin to reduce the transit time to make sure the photodiode can operate in high-speed operation. However, the depletion layer has to be thick to increase the quantum efficiency where a large portion of the incident light can be absorbed into the photodetector. This contradiction become a trade-off between the response speed and quantum efficiency [7]. Suitable type of the photodetector is needed to fairly tackle this trade-off. In addition, despite carrier transit time, the reason that limiting the bandwidth of the photodetector is a CR time constant. Thus, the appropriate size of the photodetector devices also plays an important role to realize the high-speed response. On the other hand, the photodetector has been familiar to be characterize by using a laser of 850 nm wavelength, but, how about the other wavelength bands such as red (635 nm), green (520 nm) and blue (405 nm) visible light? Some of them are useful for photodetectors such as optical disc as mention before and etc. Therefore, the wavelength dependence of the photodetector should be conducted to further expand its applications.

Furthermore, photodetectors by themselves are generally not sufficient to be integrated with the LSI for optical information processing systems. This is because the output of the photodetector is photocurrent, while the electronic circuit at the subsequent stage is operates with the voltage signal. Additionally, in most cases, the photocurrent produced by the photodetector is quite weak. Therefore, it is essential to have an electronic circuit along with photodetector that produce the output voltage and has electronic amplification ability before it can be used for further processing. Lastly, to realize high-speed photoreceiver by using CMOS process that offer state-of-the-art performance, optimization of each device is necessary.

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1.2 State of the Art

Si photodetectors fabricated by a complementary metal oxide semiconductor (CMOS) process are promising optical devices and various photodiode fabricated by CMOS process such as p-i-n photodiode [2], [8], [9], Silicon-on-insulator (SOI) photodiode PD [10]–[13], spatial modulated light detector (SML) [14]–[19] and avalanche photodiode (APD) [20]–[23] has been developed for optical interconnection applications. There are two desirable indicators to recognize a good photodiode that are consumes high detection efficiency and large bandwidth product. The p-i-n and SOI photodiodes can produce maximum bandwidth near 13 GHz but have the disadvantage of the low detection efficiency. Nevertheless, due to the light penetration depth of Si at 850 nm is more than 10 μm, another problem arises that carriers generated from the bulk Si substrate diffuse slowly and are collected, significantly affecting the response performance and limiting the bandwidth. The emergent of SML photodiodes can provide slow diffusion carriers elimination by the differential structure as reported by [14] with the highest bandwidth is about 4.4 GHz and the responsivity around 0.034 A/μm. However, SML PDs suffer from responsivity degradation because about half of optical input power is blocked as reported by [17], and then they come out a solution by combining the speed advantage of the SML PD and the responsivity advantage of a normal PD so-called speed-enhanced PD, but, unfortunately no bandwidth and responsivity data provided.

Several researchers have implemented a different approach to eliminating the slow diffusion carriers that limiting the speed performance and prevent the lack of responsivity by designing the avalanche photodiode with CMOS compatible (CMOS-APD) [20]–[23]. Avalanche photodiode is a highly sensitive semiconductor electronic device that provide built-in gain so-called avalanche multiplication. By applying higher reverse voltage bias, APDs produce an internal gain effect due to impact ionization. This phenomenon became an advantage for APDs to have higher quantum efficiency. Besides that, guard ring structure [23]–[25] that already implemented in the avalanche photodiode enhanced the avalanche

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effect and provides the maximum avalanche gain. The incorporating of guard ring also gives extra value for APDs due to ability to eliminate the slow diffusion carriers in deep layer and substrate device for higher speed generation.

1.3 Objectives

The development of integrated circuit technology in recent years is remarkable, and the processing speed improves year by year. As we know, the performance of large scale integrated, LSI has been enhanced by down-sizing the LSI. However, due to the down-sizing, resistance in electric wire is increased due to decreasing wire dimension, and capacitance between electric wires is increased due to narrow wire separation. Consequently, the operating speed of the LSI is limited. To enhance the operating speed of the LSI, optical interconnection has been proposed and widely studied. Optical interconnection has no resistance and has no capacitance. Thus, high-speed operation of the LSI is expected. To realize the optical interconnection, optical devices such as lasers, waveguides, photodetectors and LSIs should be integrated in one chip. Therefore, in this research, there have two main objectives that focus on photodetector mainly for avalanche photodiode, which are (1) to characterize and optimize the avalanche photodiodes, and (2) to study the wavelength dependence of the avalanche photodiode. In addition, to realize high-speed photoreceiver by using CMOS process, the avalanche photodiodes should be combined with the transimpedance amplifier. Hence, another objective is to investigate the transimpedance amplifier that can produce high gain and high bandwidth performance by utilizing the output from the optimum avalanche photodiode.

1.4 Thesis Outline

In this Chapter 1, the motivation, state-of-the-art, and objective to represent the whole idea for this thesis was briefly explained. This chapter also reviews the earlier photodiodes designed by other researchers and deliberate the pros and cons between them. Thereafter, the main contribution of this thesis is revealed. In Chapter 2, as the photodetector is the very first building block of the photoreceiver, it is important to review the basic principle regarding photodiodes. After that, the

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selected photodetector for this research that is avalanche photodiode and its respective principle and characteristics are described.

Chapter 3 presents the characterization and optimization of the avalanche photodiode. The characterization of CMOS-APDs is treated first followed by the optimization. Several criteria have been subject to optimize the CMOS-APDs such as electrode spacing, detection area, pad size for RF probing and wavelength. All of the results and discussions are explained here.

After the discussion about avalanche photodiodes are almost complete, the photoreceiver part is deliberated in Chapter 4. In this chapter, the explanation of photoreceiver mainly transimpedance amplifier is conducted first followed by two different types of transimpedance amplifiers with their circuit configuration, principles and simulation results.

Finally, the general conclusions are drawn in Chapter 5. An overview is also given on the main contribution based on the results that have been described in the previous chapters and also in international journals which have been presented. Then, the suggestions or recommendations are made for upcoming research that could continue to improve and advance the performance of this finding.

1.5 Main Contribution

The work presented in this thesis gives the original contribution to the characterization and optimization of avalanche photodiodes which are fabricated by standard CMOS process to realize high-speed photoreceivers. For the first time, the optimization of avalanche photodiode in regards of electrode spacing, detection size, and pads size are acknowledged. The achieved 8.4 GHz bandwidth along with 280 GHz gain-bandwidth product are more than the state-of-the-art commercial PIN photodiodes. Furthermore, in this research, the wavelength dependence of the responsivity and the bandwidth of the CMOS-APDs with and without the guard ring structure shows the guard ring is very beneficial for practical application. The guard ring enhances bandwidth although the responsivity is decreased for wavelength longer than 520 nm. For wavelength shorter than 520 nm, although the

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bandwidth is same regardless of with or without the guard ring, the guard ring is very effective for realizing low dark current.

To keep the amazing results of avalanche photodiodes in line with high demands of the high-speed photoreceivers, the research continued with developing the transimpedance amplifier (TIA). Two types of TIA which are common-source and regulated-cascode have been selected to perform the conversion of small photocurrent from CMOS-APD to voltage signal. The simulation results of the TIAs are very promising for high-speed photoreceivers in regard of CMOS-APDs performance.

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CHAPTER 2

PHOTODETECTOR

This chapter will describe the information needed to easily understand the basic operation of photodiodes followed by the avalanche photodiodes.

After the introduction of photodetector, the principle of a photodiode such as photodetection, absorption coefficient, quantum efficiency, responsivity, response speed, and etc. are explained. Thereafter, the discussion is concentrated on avalanche photodiode which is the main photodiode for this research. It is concern to the avalanche amplification, ionization rate, multiplication factor, and frequency response. Finally, all the key points related to this chapter are summarized.

2.1 Introduction

The main component in photoreceiver's block is a photodetector. Photodetector performed the first task for the photoreceiver which is to convert from the optical signal to the electric form, mainly in current. The photodetector used in this research is a silicon CMOS photodiode, as this is the most inexpensive semiconductor used in electronics. Semiconductor photodetectors depending on the absorption of incident photons with energy more than the semiconductor bandgap energy E_g to generate electron-hole pairs. Apparently, photodetection involves three processes: (1) optical energy absorption and carrier generation, (2) the transportation of photogenerated carriers away from the absorption region, (3) carrier collection and photocurrent generation. The performance of a photodetector can be characterized by a number of figures of merit (FOM) such as responsivity and bandwidth.

2.2 Photodiode Principle

2.2.1 Photodetection

Photodetection occurs when the electrons in the valence band excited by the photon energy which is greater than the material bandgap energy E_g, and then up

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into the conduction band as shown in Figure 2.1. Holes are generated because the electrons are lost from the valence band. The hole and electron each compose a charge carrier. When the electric field is applied to the semiconductor, it causes the holes and electrons to be transported through the material and into an external circuit, yielding a photocurrent. This mechanism so-called the intrinsic band-to-band absorption is the common absorption mechanism in most semiconductor used for photodetection besides free carrier absorption and band-to-impurity absorption as shown in Figure 2.2. However, when the photon energy is smaller than the material bandgap energy E_g, the electrons are not excited to the conduction band.

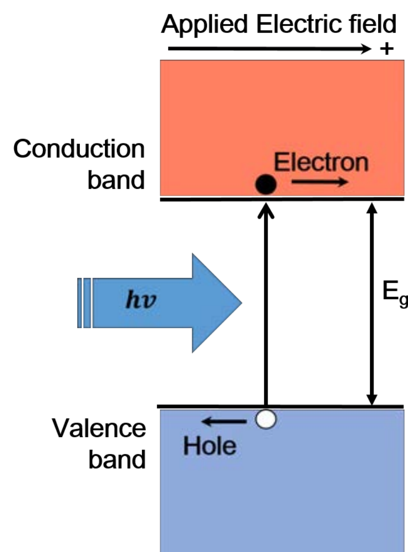

Figure 2.1: Generation of electron-hole pairs by light absorption (Intrinsic band-to-band absorption) [26].

The relationship between the photon energy, E and the wavelength of light are as below:

$$E = \frac{hc}{\lambda} \tag{2.1}$$

where,

E: photon energy

h: Planck's constant

λ: wavelength of light

c: speed of light

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Equation 2.1 shows that the shorter light wavelength has stronger photon energy. In order for electrons in the valence band to be excited and transferred to the conduction band, the photon energy E must be larger than the energy bandgap E_g and the electron hole pairs are generated by the absorption of light. Therefore, excitation does not occur in an environment in which the photon energy is equal to or smaller than the bandgap E_g. Therefore, the conditions for effective excitation of electrons is as follows:

$$E = \frac{hc}{\lambda} \geq E_g \tag{2.2}$$

this yields an allowable wavelength of light

$$\lambda \leq \frac{hc}{E_g} \tag{2.3}$$

or

$$\lambda = \frac{1.24}{E_g(eV)} [\mu m] \tag{2.4}$$

where:

Eg (eV) = bandgap energy in electron–volts.

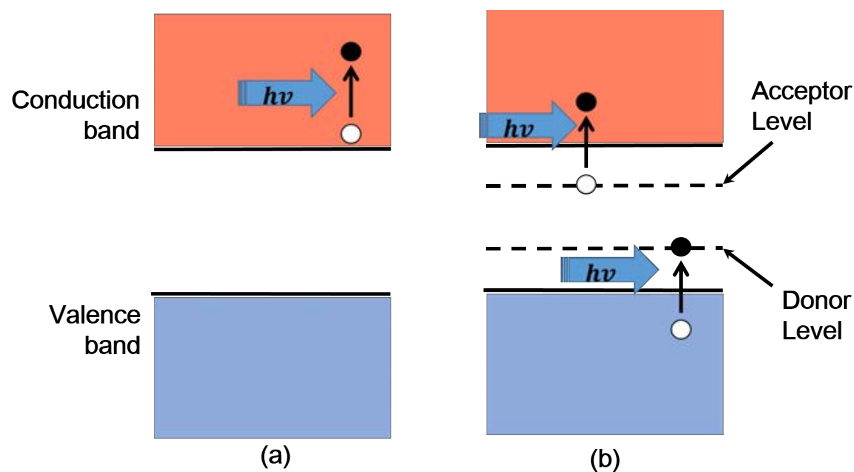

Figure 2.2: Absorption mechanism; (a) Free carrier absorption, and, (b) Band-to-impurity absorption [26].

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In addition, free carrier absorption occurs when the photon energy is absorbed by free carriers in either the conduction or the valence band [26] and corresponds to the 'heating' of the semiconductor material. It is a secondary effect at the near infrared wavelengths used for optical communications. Band–to–impurity absorption is another secondary effect at near infra-red wavelengths. It is used to construct photodetectors responsive at mid infra-red wavelengths as long as 30 µm.

Figure 2.3 shows the band diagram near the pn junction to consider the situation when a reverse voltage V is applied to the pn junction from the outside. When semiconductor is incident with light, electron-hole pairs are generated by light absorption. At this time, the holes in the n-region, which are minority carriers, and the electrons in the p-region are minority carriers, so that those generated at a location distant from the depletion layer diffuse by the diffusion length and then disappear by recombination. On the other hand, carriers generated in the depletion layer and part of carriers generated in the diffusion length region from the depletion layer drift to the n-region and p-region for electrons and holes, respectively. The reverse current by these carriers is the photocurrent I_{ph}.

However, the dark current I_{dark} occurs when the reverse voltage is applied. It is due to the following factors:

(i) Reverse saturation current generated by carrier diffusion,

(ii) Surface leakage current generated from the interface state existing at the interface with air or dissimilar materials,

(iii) Tunnel current flowing through the thin potential barrier of the depletion layer when high voltage applied,

(iv) Current generated by lattice defects in the material.

Based on these four factors, the total current *I* when applying the reverse voltage is,

$$I = -(I_{ph} + I_{dark}) \tag{2.5}$$

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Thus, when a certain reverse voltage V_B is applied, an avalanche breakdown phenomenon occurs where the current increases obviously. This phenomenon will be described later.

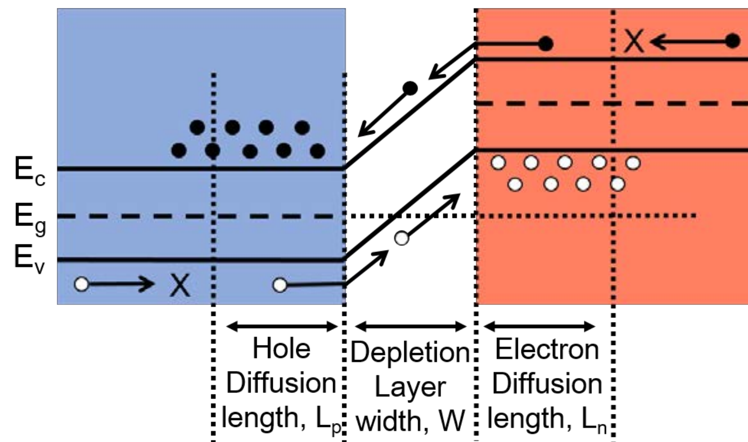

Figure 2.3: Light absorption in pn junction

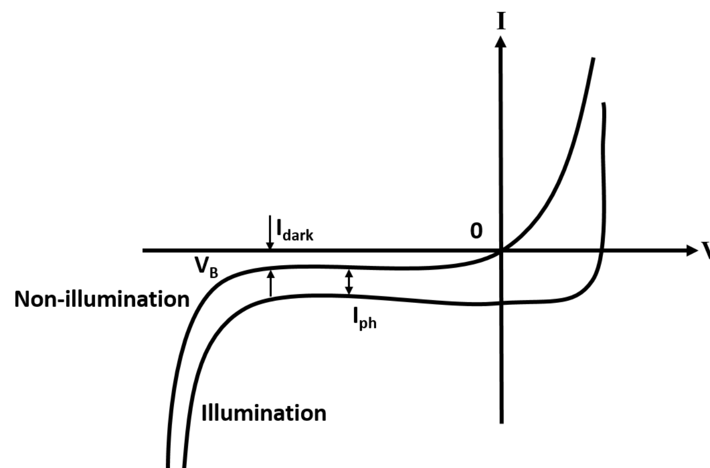

Figure 2.4: Dark current and photocurrent

2.2.2 Absorption Coefficient

As described in the previous section, if light adequate the equation (2.4) when illuminated on the material, the light absorption occurs. An absorption coefficient α_0 indicating the light absorption intensity per unit length is represent the constant for the extended light absorption. Assuming that the incident optical power at the surface is expressed as $P_i(x)$. When light is penetrated on the material, the light absorption $-dP_i(x)$ at the distance dx is expressed as follows:

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$$-dP_i(x) = \alpha_0 P_i(x)dx$$
$$\frac{-dP_i(x)}{dx} = -\alpha_0 P_i(x) \tag{2.6}$$

By integrating both of equations in (2.6) with x after considering the initial condition $P_i(0) = P_{i0}$, it become:

$$P_i(x) = P_{i0}e^{-\alpha_0 x} \tag{2.7}$$

Therefore, the incident optical power distribution in the material is exponentially decreases according to the absorption coefficient α_0. This is shown in Figure 2.5. L_α is the absorption length or the depth that light can enter into the material. Assuming that the incident optical power P_{i0} on the material surface is absorbed into the material, the absorption length L_α from the equation (2.7) is then expressed as,

$$P_{i0}L_\alpha = \int_0^\infty P_{i0}e^{-\alpha_0 x}\,dx$$
$$L_\alpha = \frac{1}{\alpha_0} \tag{2.8}$$

So, L_α becomes the reciprocal of the absorption coefficient α_0. The incident optical power at the absorption length is expressed as,

$$P_i(L_\alpha) = P_{i0}e^{-\alpha_0 x} = \frac{1}{e}P_{i0} \cong 0.37P_{i0} \tag{2.9}$$

Therefore, it decreases about 37% of the incident optical power at the surface. In other words, 63% of light is absorbed to the absorption length. Since the absorption coefficient is generally 10^2 to 10^5 cm^{-1}, the absorption length is 0.1 to 100 µm. Therefore, it is understood that most of light is absorbed in a very shallow material surface.

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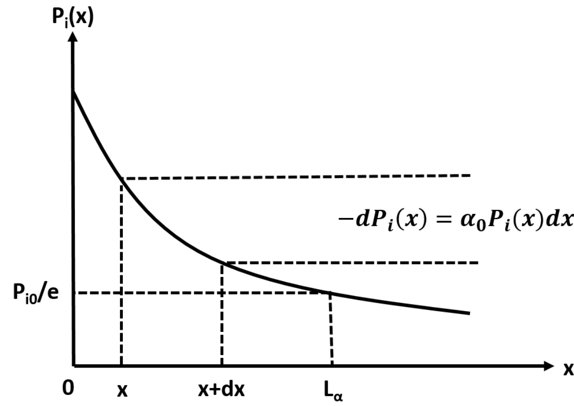

Figure 2.5: Incident optical power distribution in semiconductor.

The absorption coefficient is 0 if the wavelength is not satisfying the equation (2.3). On the other hand, if the wavelength satisfying the equation (2.3), the photon energy hν is close to the energy bandgap E_g. Since the state density of the conduction band as the transition destination of electrons is small, many electrons cannot be shifted from the valence band, therefore the absorption coefficient is low. For shorter wavelength, hν is larger than the bandgap E_g, and electrons can be transferred to the conduction band due to large state density. Therefore, the absorption coefficient increases irrespective to the wavelength.

2.2.3 Quantum Efficiency and Responsivity

Quantum efficiency η is an important parameter for a photodiode that is defined by the probability of a single incident photon on the detector to generate an electron-hole pair [7]. Responsivity *R* is the ratio of the photocurrent to the optical power [7]. Both quantum efficiency η and responsivity *R* are given as performance indicators of the photodetector. Assuming that the photocurrent I_{ph} flows when incident optical power P_i and optical frequency *v* are incident, the quantum efficiency η and the responsivity *R* are defined as follows:

$$\eta \equiv \frac{Number\ of\ carriers\ contributing\ to\ photocurrent}{Number\ of\ incident\ photons} = \frac{I_{ph}/q}{P_i/hv} \quad (2.10)$$

$$R \equiv \frac{Photocurrent\ variation}{Incident\ optical\ power\ variation} = \frac{dI_{ph}(P_i)}{dP_i} \quad (2.11)$$

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The responsivity shows the slope of the photocurrent and incident optical power characteristic. However, in ordinary direct current analysis, the photocurrent and the incident optical power are in a linear relationship as express below,

$$R = \frac{I_{ph}}{P_i} = \frac{q}{hv}\eta \; [A/W] \tag{2.12}$$

From this equation, quantum efficiency and responsivity can be easily converted. However, when a large current flows through the photodetector due to the avalanche amplification effect (to be described later), this equation cannot be used because the photocurrent and the incident optical power have a nonlinear relationship. In theory, if the thickness of the material is sufficiently longer than the absorption length L_α, all the photons are absorbed, and under the ideal situation, a quantum efficiency of 100% can be realized. However, in reality it does not 100% because there are several factors that lower the quantum efficiency as shown below:

(i) reflection from the semiconductor surface
(ii) surface recombination of carriers generated on the crystal surface
(iii) recombination of carriers within the depletion layer
(iv) recombination of carriers generated outside the depletion layer
(v) incomplete absorption
(vi) contact shadowing

The responsivity of a semiconductor will also vary with wavelength [26]. Responsivity increases with wavelength because there are more photons per watt at long wavelengths than at short wavelengths. This leads to the photon energy decreasing with wavelength. Since the amount of photocurrent is determined by the number of photons not the energy of photons, longer wavelengths generate more photocurrent per watt than the short wavelengths.

When light is applied to the semiconductor, only the light absorbed by the depletion layer width W from the depletion layer depth x_n to the depletion layer depth x_p is considered to contribute to the photocurrent. At this time, the internal quantum efficiency η_{in} without considering the reflection at the surface is obtained from the equations (2.6) and (2.9), and represented by,

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$$\eta_{in} = \frac{\alpha_0 \int_{x_n}^{x_p} P_{i0} e^{-\alpha_0 x}\, dx}{\alpha_0 \int_0^{\infty} P_{i0} e^{-\alpha_0 x}\, dx} = e^{-\alpha_0 x_n}(1 - e^{-\alpha_0 W}) \qquad (2.13)$$

Since the absorption coefficient α_0 increases as the wavelength is shorter, $e^{1-e^{-\alpha_0 W}}$ decreases in the equation (2.13), and the internal quantum efficiency decreases.

2.2.4 Response Speed

The response speed of the photodetector is mainly limited by two factors; (1) RC time constant, and (2) carrier transit time. Details explanations of these factors are followed.

2.2.4.1 RC Time Constant

The photodetector absorbs light into the depletion layer which is serves as a current generation source. At the same time, the depletion layer has a junction capacitance C_j and an internal resistance R_i determined by the dark current. If the photodetector is connected to an external circuit such as an amplifier, its load resistance is R_L. The actual photodetector circuit is shown in Figure 2.6 (a) with its equivalent circuit shown in Figure 2.6 (b), and the simplified circuit shown in Figure 2.6 (c).

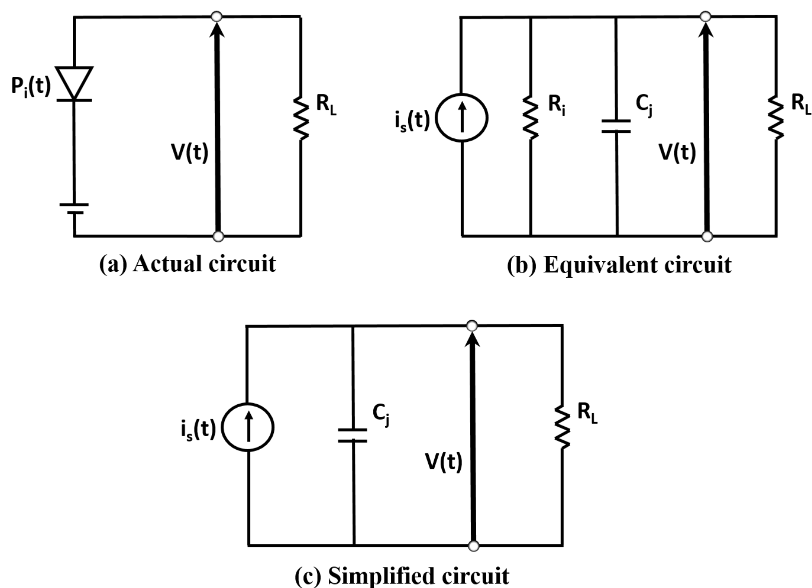

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Figure 2.6: Basic equivalent circuit of photodetector. (a) actual circuit, (b) equivalent circuit, and (c) simplified circuit.

A combination of the internal resistance R_i and the load resistance R_L by the equivalent resistance R_{eq} is expressed as,

$$\frac{1}{R_{eq}} = \frac{1}{R_i} + \frac{1}{R_L} \tag{2.14}$$

Assuming that a sinusoidal or pulsed light enters the photodetector and a photocurrent $i_s(t)$ is generated, the voltage v(t) generated across the resistance R_{eq} becomes

$$C_j \frac{dv(t)}{dt} + \frac{v(t)}{R_{eq}} = i_s(t) \tag{2.15}$$

Then, considering the case where light of sine wave modulation (angular frequency ω) is incident,

$$i_s(t) = i_0 e^{j\omega t} \tag{2.16}$$

Thus, the solution to equation (2.16) is

$$v(t) = \frac{i_0 R_{eq}}{1 + j\omega C_j R_{eq}} \tag{2.17}$$

The voltage amplitude in the low frequency region where $\omega \ll 1/C_j R_{eq}$ is $i_0 R_{eq}$. As a result, the voltage amplitude ratio with respect to the low frequency region in the high frequency region is expressed by the following equation,

$$\left| \frac{1}{1 + j\omega C_j R_{eq}} \right| = \frac{1}{\sqrt{1 + (j\omega C_j R_{eq})^2}} \tag{2.18}$$

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When the frequency at the voltage amplitude ratio with respect to the low frequency region is 1/√2, then, the power becomes 1/2 (-3 dB) and is called as cutoff frequency f_{CR}. It is given by,

$$f_{CR} = \frac{1}{2\pi C_j R_{eq}} \tag{2.19}$$

2.2.4.2 Transit Time

To increase the speed of the photodetector, it is necessary to reduce the junction capacitance C_j from the RC time constant perspective. For that purpose, the width of the depletion layer has to be larger. However, the transit time should be short for high speed response by decreasing the width of the depletion layer. As seen, there is a trade-off between them.

Now, consider a wide depletion layer where incident light is almost absorbed in the depletion layer. When the electric field is turned on, the electrons and holes drift in the opposite direction. This induces a displacement current and reduces the internal electric field, which is cause of saturation in photodetectors. As the electric field in the depletion layer is strong, electrons and holes drift within the depletion layer at the saturation velocity v_{ds}.

Then, consider the traveling speed of carriers in the depletion layer of the pn junction. As shown in Figure 2.7, the sinusoidally modulated light is

$$P_i(t) = P_i e^{j\omega t}$$

If it is incident on the depletion layer, the surface recombination and light absorption in the n-type region are ignored. The photocurrent density $J_s(t)$ at time t is expressed by the number of electrons generated at ($t - x/v_{ds}$) arrive at the depletion layer edge x = 0. By taking a spatial average, it is given by the following equation,

$$J_s(t) = \frac{1}{W}\int_0^W \frac{q}{hv} P_{i0} e^{j\omega\left(t - \frac{x}{v_{ds}}\right)} dx \tag{2.20}$$

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$$= \frac{q}{h\nu} P_{i0} (\frac{1 - e^{(-j\omega t_{tr})}}{j\omega t_{tr}}) e^{j\omega t}$$

$$t_{tr} = \frac{W}{v_{ds}} \quad (2.21)$$

If the frequency modulation is $\omega t_{tr} \ll 1$, the photocurrent density become,

$$J_s(t) = \frac{q}{h\nu} P_{i0} e^{j\omega t} \quad (2.22)$$

Therefore, the photocurrent amplitude ratio in the high-frequency region with respect to the low-frequency region is,

$$\frac{1 - e^{-j\omega t_{tr}}}{j\omega t_{tr}} \quad (2.23)$$

In other words, the photocurrent can follow the modulated optical signal in a range where the traveling time for $\omega t_{tr} \ll 1$ is sufficiently shorter than the modulation period, means that, the width of the depletion layer is narrow. As the transit time becomes almost the same as the modulation period, the phase delay of the photocurrent occurs and the amplitude decreases. The frequency where the amplitude of the photocurrent is $1/\sqrt{2}$ times (-3 dB) and the amplitude of the low frequency region is defined as the cutoff frequency. Also in the pulse response, the rise time τr and the fall time τf of the photocurrent are prolongs by the transit time τtr.

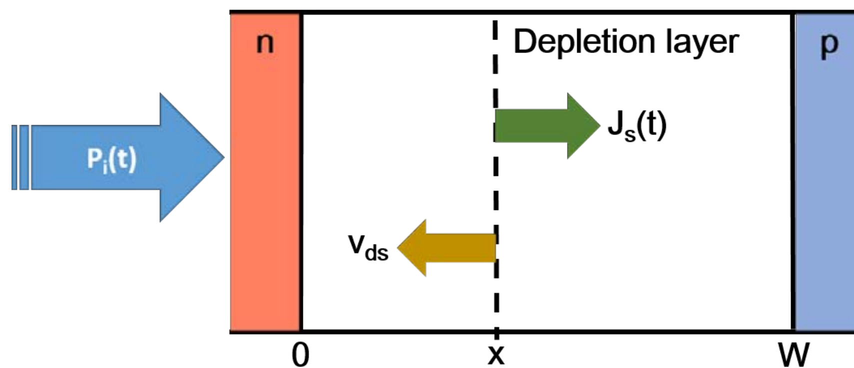

Figure 2.7: Carrier drift in depletion layer

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When the depletion layer width is not sufficiently larger than the light absorption length, minority carriers generated outside the depletion layer will diffuse and enter the depletion layer.

$$\tau_n = L_n^2 D_n$$

$$\tau_p = L_p^2 D_p$$

where,
L: diffusion length,
D: diffusion coefficient

In this case, a time delay due to diffusion of several nanoseconds is further generated. At the time of pulse response, if this diffusion component is present, it becomes a waveform with a trailing tail in the high frequency region, and consequently limit the high speed communication. In the modulation frequency characteristic, this slow component is affected and the modulated output above the mid-range is reduced. Therefore, to achieve high-speed response of the photodetector, it is important to prevent the influence of diffusion carriers generated outside the depletion layer.

2.3 Avalanche Photodiode Principle

APD (Avalanche Photodiode) is a photodetector that has capability to achieve high sensitivity and high bandwidth. It has a function of multiplying electron hole pairs generated by absorption of an optical signal in a depletion layer by utilizing avalanche breakdown. The basic structure of APD is similar to that of ordinary pn junction, but it is optimized to facilitate avalanche breakdown. Usually it is often used in a bias state near the breakdown voltage.

2.3.1 Avalanche Amplification

When a high reverse voltage is applied to the pn junction as shown in Figure 2.8, a strong electric field region is formed in the depletion layer, and the band becomes steep. This strong electric field region is called an avalanche region. When the electric field intensity in the avalanche region exceeds a certain constant

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intensity (about 10^6 V/cm), the carrier multiplication effect occurs according to the following principle:

(i) Carriers generated by light absorption outside the avalanche region enter the avalanche region, or carriers are generated by light absorption in the avalanche region

(ii) Carriers accelerated by the strong electric field in the avalanche region collide with the lattice in the material after transit through the mean free path and the lattice ionizes to generate electron-hole pairs (this phenomenon is called impact ionization)

(iii) Carriers generated by the original carriers and impact ionization are accelerated by the strong electric field and collide with the lattice again to generate electron-hole pairs

As the above flow occurs one by one, the electron-hole pairs multiplied from one photon and this phenomenon so-called avalanche amplification. In that way, even when the incident light is weak, a large photocurrent can be obtained.

The voltage at the time when avalanche amplification begins to enter the infinite region is called an avalanche breakdown voltage V_B. However, when the avalanche breakdown voltage V_B is applied, due to statistical fluctuation of collision such as space charge effect, the multiplication phenomenon is interrupted and the amplification factor becomes finite [20]. Since a large amount of dark current and noise are mixed at the breakdown voltage, APD applied a voltage at just before the breakdown voltage occur.

Typically, a strong electric field that generate the avalanche amplification is only at small portion of the entire APD, therefore, carriers generated in other than the avalanche region are injected into the avalanche region by drift or diffusion, and then contributes to the multiplication phenomenon. A portion intended only for light absorption in a non-avalanche region is called an absorption region. To design the APD, it is necessary to study how to arrange avalanche region and absorption region according to desired characteristics.

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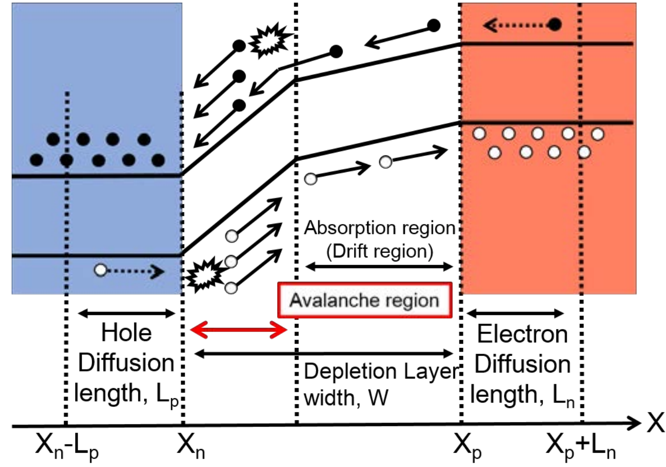

Figure 2.8: Band diagram for avalanche mechanism.

2.3.2 Ionization Rate

The number of electron hole pairs generated by collision ionization when one electron travels within the avalanche region by a unit distance is called electron ionization coefficient α. Similarly, the number of electron-hole pairs generated when one hole travels by a unit distance is called hole ionization coefficient β. In case of Si, the ionization rate is approximated by the following equation.

$$electron: \alpha = 3.80 \times 10^{6} e^{-1.75\times 10^{6}/E}\ [cm^{-1}] \tag{2.24}$$

$$hole: \beta = 2.25 \times 10^{7} e^{-3.26\times 10^{6}/E}\ [cm^{-1}] \tag{2.25}$$

$$ionization\ ratio: k \equiv \frac{\beta}{\alpha} \tag{2.26}$$

The ratio k of electron ionization rate and hole ionization rate is given by the equation (2.26) and is frequently used for APD analysis. In Si, the electron ionization rate is approximately one order of magnitude larger than the hole ionization rate. Depending on the type of carrier contributing to the multiplication effect, the characteristics of the APD are largely different. Among the carriers generated in the absorption region, the electrons that injected into the avalanche region and contribute to the multiplication effect are called “electron-injection-type APD", and for holes are called "hole-injection-type APD" [22]. The difference between these two APDs will described in the Chapter 3.

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2.3.3 DC Characteristics

The multiplication factor of APD is an index to represent how many times the number of carriers generated by photoexcitation has been amplified as compared to the time of non-multiplication. The multiplication factor M is expressed as follows by using the DC photodetection current.

$$M(V) = \frac{I_{ph}(V)}{I_{ph0}} = \frac{I(V) - I_{dark}(V)}{I_0 - I_{dark0}} \tag{2.27}$$

where,

I_{ph}: Photocurrent

I_{ph0}: Photocurrent at non-multiplication

I_{dark}: Dark current

I_{dark0}: Dark current at non-multiplication

I: Total current under illumination

I_0: Total current under illumination at non-multiplication

It is also known that the multiplication factor M can be expressed by the following empirical formula,

$$M = \frac{1}{1 - \left(\frac{V - RI}{V_B}\right)^n} \tag{2.28}$$

where,

RI: voltage drop in the APD internal and external circuits

R: Sum of parasitic resistance and load resistance in PD

V_B: Avalanche breakdown voltage

n: constant

When the avalanche multiplication factor is large, even if the incident optical power is weak, a large current flows, so the voltage drop due to it cannot be ignored. Therefore, the following phenomenon occurs:

(i) Increase the voltage applied from the outside to the APD

(ii) The multiplication factor increases and the photocurrent increases

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(iii) Voltage drop at the parasitic resistance and the load resistance inside the APD reduces the substantial applied voltage to the APD

(iv) The multiplication factor decreases

Due to this phenomenon, assuming that the maximum amplification factor is observed at a certain voltage V, even if a voltage of V or more is applied, a further multiplication factor cannot be obtained.

The voltage drop RI can be expressed by using the multiplication factor M and the sensitivity R_0 at the time of non-multiplication from the equations (2.12) and (2.27).

$$RI = R(I_{ph} + I_{dark}) \cong RI_{ph} = RMI_{ph0} = RM\mathcal{R}_0 P_i \tag{2.29}$$

Therefore, the stronger the incident optical power P_i, the larger the voltage drop, so the maximum multiplication factor decreased. In the vicinity of the avalanche breakdown voltage, the multiplication factor varies significantly depending on the incident optical power even when the same voltage is applied, so the photocurrent and the incident optical power have a nonlinear relationship as shown in Figure 2.9.

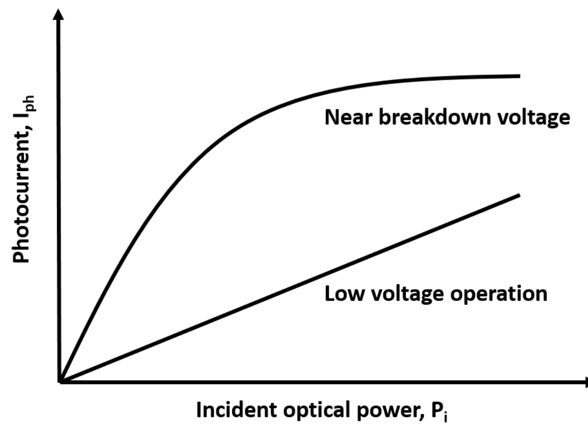

Figure 2.9: Photocurrent - incident optical power characteristics of APD.

When the applied voltage is lower than the avalanche breakdown voltage V_B, the voltage drop inside the APD is often negligible in many cases, and the equation (2.28) can be simplified as follows.

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$$M(V) = \frac{1}{1 - (V/V_B)^n} \quad (2.30)$$

2.3.4 AC Characteristics

In the avalanche operation, unlike the response speed of PD, it has irregular factors that limiting the operation speed of APD. For the carrier transit time, it takes about twice longer than the non-multiplication time in the avalanche operation. This is because, as shown in Figure 2.10, holes generated by ionization collision must travel again in the absorption region after the electrons generated in the absorption region have traveled to the avalanche region. It is considered that a travel time is significantly affects the operation speed because a large number of holes with slow moving speeds are generated in the avalanche region and travel in the absorption region in the reverse direction.

When an avalanche breakdown phenomenon occurs, carriers traveling in the avalanche region lose kinetic energy once by collision ionization. Carriers that originally existed and carriers generated by impact ionization are accelerated by strong electric fields, but they lose their kinetic energy again by the next impact ionization. In this manner, carriers travel in the avalanche region while repeating acceleration and deceleration, so that it takes time to multiply the carriers.

Regarding the frequency characteristic of the APD, the execution time from collision ionization until the next collision ionization occurs is T_{eff}, the frequency characteristic of the multiplication factor can be expressed by the following expression.

$$Electron\ injection\ type\ APD: M_n(\omega) = \frac{M_{n0}}{\sqrt{1 + \omega^2 k M_{n0}^2 T_{eff}^2}} \quad (2.31)$$

$$Hole\ injection\ type\ APD: M_p(\omega) = \frac{M_{p0}}{\sqrt{1 + \omega^2 \left(\frac{1}{k}\right) M_{p0}^2 T_{eff}^2}} \quad (2.32)$$

where,

M_n: Electron multiplication factor

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M_{n0}: Electron DC multiplication factor

M_p: Hole multiplication factor

M_{p0}: Hole DC multiplication factor

Since the cutoff frequency of each APD is $\omega_n = 2\pi f_{nc}$ and $\omega_p = 2\pi f_{pc}$, it can express as,

$$Electron\ injection\ type\ APD: M_n(\omega) = \frac{M_{n0}}{\sqrt{1+\omega^2 k M_{n0}^2 T_{eff}^2}} = \frac{M_{n0}}{\sqrt{2}} \quad (2.33)$$

$$Hole\ injection\ type\ APD: M_p(\omega) = \frac{M_{p0}}{\sqrt{1+\omega^2 \left(\frac{1}{k}\right) M_{p0}^2 T_{eff}^2}} = \frac{M_{p0}}{\sqrt{2}} \quad (2.34)$$

When these equations are used to calculate the GB (Gain-Bandwidth) product, the following equation is obtained,

$$Electron\ injection\ type\ APD: M_{n0} f_{nc} = \frac{1}{2\pi\sqrt{k}T_{eff}} \quad (2.35)$$

$$Hole\ injection\ type\ APD: M_{p0} f_{pc} = \frac{1}{2\pi\sqrt{\frac{1}{k}}T_{eff}} \quad (2.36)$$

From the equations (2.35) and (2.36), it can be seen that the GB product of APD are constant. k in the equation is the ionization ratio defined by equation (2.26). Therefore, $M_{n0}f_{nc} > M_{p0}f_{pc}$, and the electron-injection-type APD has a larger GB product than the hole-injection-type APD.

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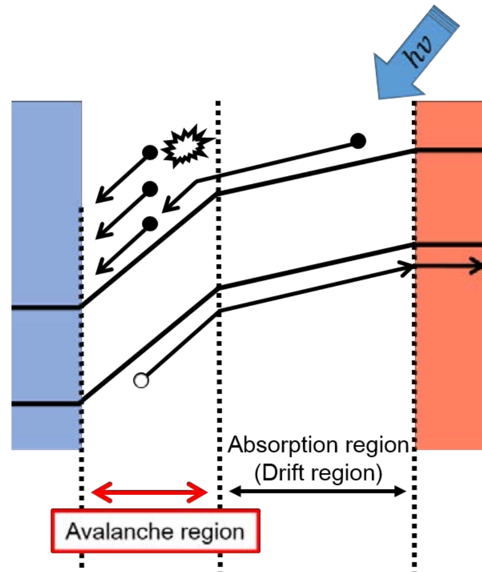

Figure 2.10: Carrier movement in absorption region.

2.4 Summary

As the first task of a photoreceiver is to convert the optical signal to a current, photodetector is treated extensively in this chapter. The theory and principle behind the photodetector such as photodetection, quantum efficiency, responsivity, response speed, and etc. has been described first. The photon energy has to be equal or greater than the bandgap energy to excite an electron from the valence band up into the conduction band. When a photon is absorbed, both a minority and majority carrier are generated. To separate the photogenerated electron-hole pairs in a photodiode, it has a depleted semiconductor region with a high electric field. This depletion region has to be thin to reduce the transit time to make sure the photodiode can operate in high-speed operation. But, the depletion layer has to be thick to increase the quantum efficiency where a large portion of the incident light can be absorbed into the photodiode. This become a trade-off between the response speed and quantum efficiency. One of the solution for this trade-off is by applying avalanche photodiode.

An avalanche photodiode is a main photodetector used in this research, therefore, the theory related to this type of photodiode is explained thoroughly. It is including the avalanche amplification, impact ionization, avalanche multiplication, frequency response and the figures of merit (FOM) of gain-bandwidth product.

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Avalanche photodiodes are high sensitivity and high-speed semiconductor optical sensors. APDs have an internal region where electron multiplication occurs as compared to regular PIN photodiodes. By applying reverse bias voltage, APDs result in high gain in the output signal that ensure a low light levels can be measured at high-speed. The avalanche amplification phenomenon can increase the quantum efficiency for the photodiode. All of this become advantages for the APDs. But, a regular APDs require a high reverse bias for their operation. The bandwidth for APDs are limited by the slow diffusion carriers from the bottom level or substrate of the device. Therefore, an improved designed of APDs that can overcome their disadvantages will be discuss in the next chapter. That kind of APDs will be characterized and optimized to find better APDs with a capability to perform effectively for high-speed photoreceivers.

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CHAPTER 3

AVALANCHE PHOTODIODE

The main contribution for this thesis is to characterize and optimize the avalanche photodiodes fabricated by CMOS process (CMOS-APDs) which is discussed thoroughly in this chapter. First, an introduction for this chapter is explained. It is then followed by the characterization of avalanche photodiode concerning the two types of CMOS-APDs (nMOS-type and pMOS-type) along with two different guard ring structures. The measurement system is also described in order to do the measurement.

After that, the optimization dependence of electrode spacing L_s, detection area S_{DT}, and PAD size for RF probing S_{PAD} are discussed for one of the selected device between two types of CMOS-APDs. Next, another optimization subject that is related to wavelength dependence of the CMOS-APDs are discussed. Last but not least, all of the points is sum up at the end of this chapter.

3.1 Introduction

nMOS-type and pMOS-type silicon avalanche photodiodes (APDs) were fabricated by standard 0.18 μm CMOS process, and the current-voltage characteristic and the frequency response of the APDs with and without the guard ring structure were measured. The role of the guard ring is cancellation of photo-generated carriers in a deep layer and a substrate. The bandwidth of the APD is enhanced with the guard ring structure at a sacrifice of the responsivity. Based on comparison of nMOS-type and pMOS-type APDs, the nMOS-type APD is more suitable for high-speed operation. Thus, by using nMOS-type CMOS-APD as a reference device, the optimization analysis to enhance the CMOS-APD's performance especially for higher bandwidth and lower responsivity can be done. The indication is to decrease the carrier transit time and device capacitance with decreasing the spacing of interdigital electrodes and with decreasing the detection area and the PAD size for RF probing, respectively. Therefore, an nMOS-type CMOS-APD is fabricated along with the optimize size of the electrode spacing, the

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detection area, and the PAD size for RF probing to achieve the optimum CMOS-APD.

Furthermore, the 850 nm wavelength is categorized as a long wavelength that has weak optical absorption of Si. most of the photodetectors are characterized by using a laser of 850 nm wavelength. But, how about the other wavelength behavior such as red (635 nm), green (520 nm) and blue (405 nm) towards CMOS-APD. Therefore, in this research, the wavelength dependence of the CMOS-APD is conducted to further explore their characteristics and also expand the applications of the CMOS-APDs. From previous chapter, the guard ring has an effect for 850 nm wavelength, thus, the effectiveness of the guard ring to the other wavelengths are investigated.

3.2 Characterization of CMOS-APD

3.2.1 Structure

Figure 3.1 shows the photograph of the fabricated CMOS-APD. It has two parts that are the detection area and three PAD for RF probing and DC biasing. The detection area S_{DT} and the PAD size S_{PAD} are S_{DT} = 20 x 20 μm^2 and S_{PAD} = 40 x 40 μm^2, respectively.

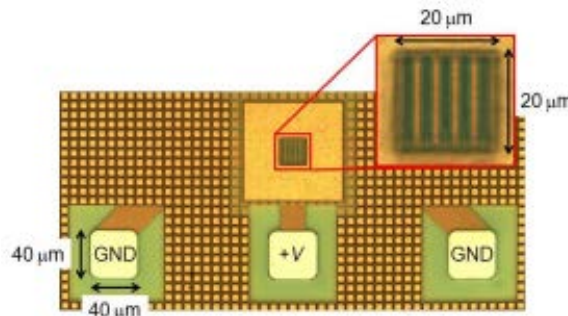

Figure 3.1: Photograph of fabricated CMOS-APD.

Figure 3.2 shows the cross-sectional structure of (a) nMOS-type and (b) pMOS-type CMOS-APDs fabricated by standard 0.18 μm CMOS process without process modifications. The shallow trench isolation (STI) oxides are used as isolation regions between n$^+$-layer and p$^+$-layer. The n$^+$-layer and p$^+$-layer are arranged alternately and then the electrodes are interdigital structure with the electrode spacing, L_s. The light is illuminated from the top of the device.

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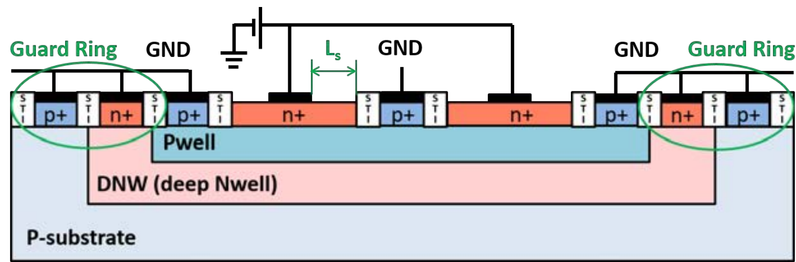
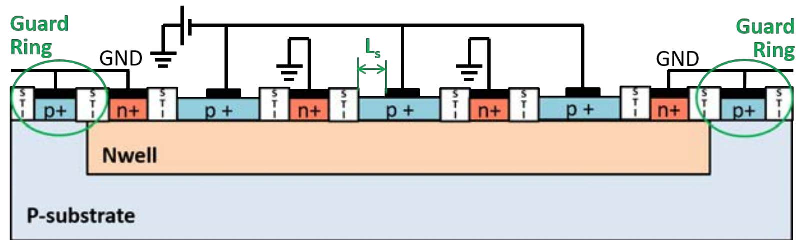


(a) nMOS-type CMOS-APD.



(b) pMOS-type CMOS-APD.

Figure 3.2: Cross-sectional structure of fabricated CMOS-APDs.

From the figure, the difference between CMOS-APD with and without the guard ring (GR) structure is found to be the connection of electrodes of the P-substrate and the DNW to the ground in Figure 3.2 (a), and the connection of electrodes of the P-substrate to the ground in Figure 3.2 (b). If all electrodes are electrically shorted, it represents the existence of the GR. If not, the structure is without the GR structure, and the P-substrate and the DNW are open for the nMOS-type and the P-substrate is open for the pMOS-type.

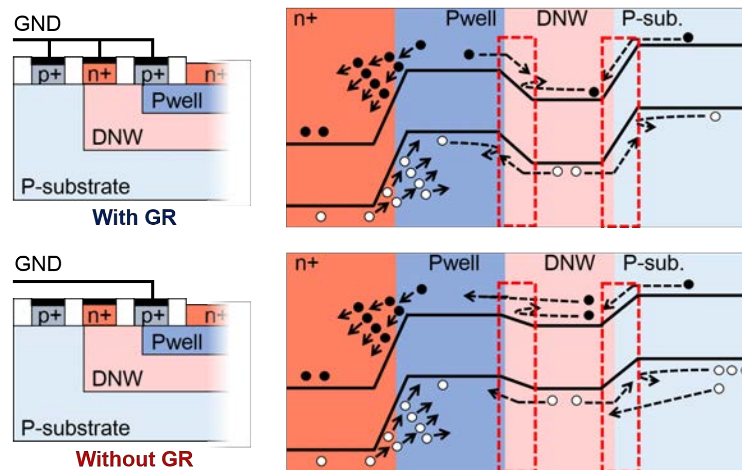


Figure 3.3: Band diagram of the nMOS-type CMOS-APD with and without GR.

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The structure of Figure 3.2 (a) is same with the nMOS structure in a P-substrate and then is referred to as the nMOS-type CMOS-APD. This structure so-called electron-injection-type CMOS-APD as mention in Chapter 2 was also referred in [22]. Figure 3.3 shows the band diagram to easily understand the carrier generation and recombination mechanism of the nMOS-type CMOS-APD. Due to the GR, the photo-generated electrons in the P-substrate and DNW move toward n^+-layers on the DNW because of the built-in potential barrier between the Pwell and the DNW, while photo-generated holes in the P-substrate move toward the p^+-layers on the P-substrate because of the built-in potential barrier between the P-substrate and the DNW, and photo-generated holes in the DNW move toward the p^+-layer on the Pwell. They are recombined and do not contribute to the photocurrent. In the Pwell and the n^+-layer on the Pwell, the photo-generated electrons and holes are drifted towards the n^+-layers and the p^+-layers, respectively. Since the high electric field is applied between the n^+-layers and the Pwell, the photo-generated electrons in the Pwell and the photo-generated holes in the n^+-layer are multiplied due to avalanche mechanism while traveling toward the n^+-layer and the p^+-layer, respectively. As a result, the responsivity is enhanced.

For the nMOS-type CMOS-APD without the GR, the potential barrier heights between the P-substrate and the DNW and between the DNW and the Pwell are undefined and may be low, and then the photo-generated electrons and holes in the P-substrate move toward the n^+-layers and the p^+-layers on the Pwell, respectively. Since the p^+-layers on the P-substrate and the n^+-layers on the DNW are not electrically connected, the photo-generated electrons and holes in the DNW and the P-substrate degrade high-speed operation because the carriers are slow diffusion carriers due to weak electric field.

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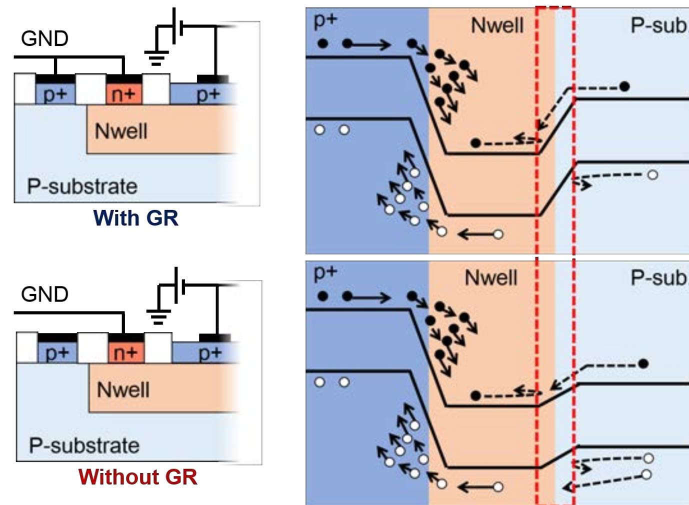

Figure 3.4: Band diagram of the pMOS-type CMOS-APD with and without GR.

The structure of Figure 3.2 (b) is same with the pMOS structure in a P-substrate and is referred to as the pMOS-type CMOS-APD. This structure so-called the hole-injection-type CMOS-APD as mention in Chapter 2 was also referred in [22]. Figure 3.4 shows the band diagram of the pMOS-type CMOS-APD with and without the GR. The photo-generated electrons in the P-substrate move to the n^+-layers on the Nwell and the photo-generated holes move to the p^+-layers on the P-substrate due to the built-in potential barrier between the P-substrate and the Nwell, and they are recombined and do not contribute to the photocurrent. On the other hand, the photo-generated electrons in the Nwell and the p^+-layer on the Nwell drifted towards n^+-layers, and the photo-generated holes in the Nwell drifted towards the p^+-layers on the Nwell, respectively. In this region, a high electric field is applied between p^+-layers and Nwell, and therefore, the photo-generated electrons in the p^+-layer and the photo-generated holes in the Nwell are multiplied due to avalanche mechanism while traveling toward the n^+-layer and the p^+-layer, respectively. As a result, the responsivity is enhanced.

For the pMOS-type CMOS-APD without the GR, the potential barrier height between the P-substrate and the Nwell are undefined and may be low, and then the of photo-generated electrons and holes in the P-substrate move toward the n^+-layers and the p^+-layers on the Nwell, respectively. Since the p^+-layers on the P-substrate are not electrically connected together with the n^+-layers on the Nwell to the ground, the photo-generated electrons and holes in the P-substrate

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degrade high-speed operation because the carriers are slow diffusion carriers due to weak electric field.

3.2.2 Measurement System

Figure 3.5 shows the measurement system used to characterize the CMOS-APD. In the measurement, a laser light from a 10 Gbps vertical cavity surface emitting laser (VCSEL) at 850 nm wavelength was intensity modulated with RF signal from a network analyzer and was illuminated from the top of the device. The light from the VCSEL was illuminated on the detection area of the CMOS-APD by optical fiber which has core diameter of 9 μm. The DC current is measured by an ammeter and the AC current is measured by a network analyzer.

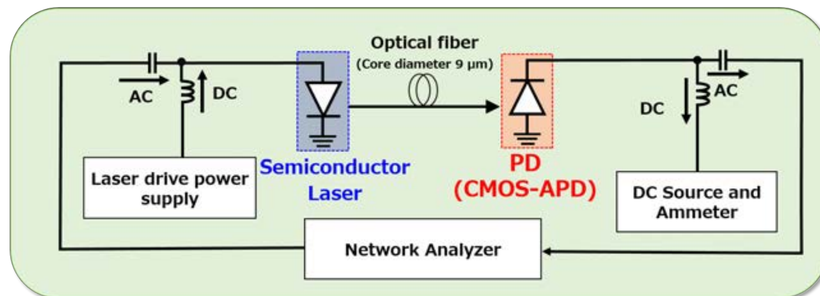

Figure 3.5: Measurement system for CMOS-APD characterization.

The frequency response was measured by using two types of network analyzers; Hewlett Packard 4396A for low frequency range of 100 kHz to 1 GHz, and Agilent Technology E8363B for a high frequency range of 10 MHz to 40 GHz. The frequency response of the VCSEL and RF cables are compensated by using a commercial GaAs PIN photodiode with the nominal bandwidth of 30 GHz (Albis Optoelectronics AG, PQW30A-S).

3.2.3 I-V Characteristics

Figure 3.6 shows the measured Current-Voltage (I-V) characteristics for (a) nMOS-type and (b) pMOS-type CMOS-APDs with and without the GR. The dark current at a low bias is about 10 pA with the GR structure, and the dark current without the GR structure is higher than that with the GR structure. It is because the carriers in the deep layer and the substrate are cancelled due to the GR structure

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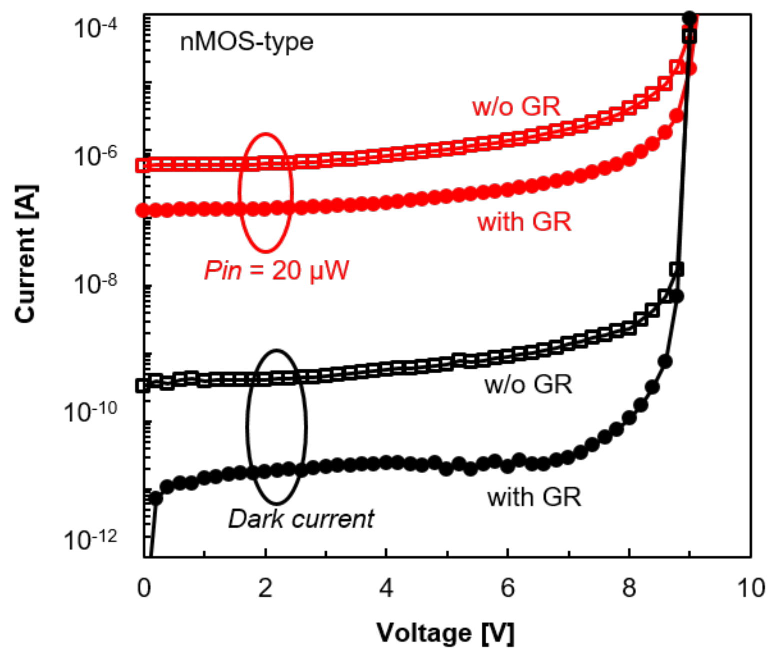
and are not canceled in the CMOS-APD without the GR structure. The breakdown voltage measured when the dark current exceeds 1 μA is about 9.05 V and 8 V for the nMOS-type and pMOS-type, respectively. The breakdown voltage difference for those types may be caused by different doping concentration in the Pwell and the Nwell, which are not disclosed from the manufacturer. Under light illumination at 20 μW, the photocurrent is almost constant for low bias voltage for both types, and it is gradually increased and finally is significantly increased before breakdown voltage due to avalanche amplification.



(a)

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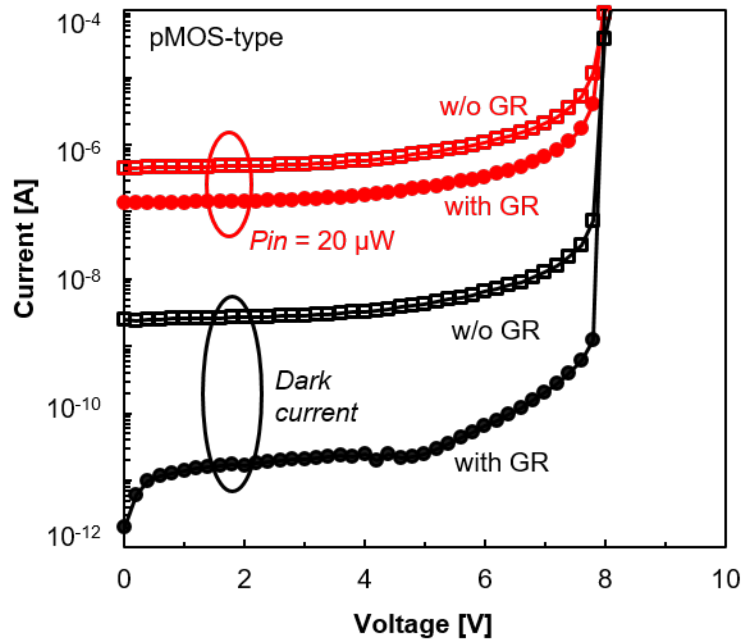

(b)

Figure 3.6: Measured I-V characteristics for (a) nMOS-type and (b) pMOS-type CMOS-APDs with and without the GR.

3.2.4 Responsivity

Figure 3.7 shows the responsivity of the nMOS-type and the pMOS-type CMOS-APDs with and without the GR as a function of the bias voltage. The responsivity rises initially with the bias voltage because of the increase of the depletion width. It is then dramatically increased at a certain voltage due to avalanche amplification, and the responsivity more than 1 A/W is achieved near the breakdown voltage for all the devices. The responsivity of the CMOS-APDs with the GR is lower than that of without the GR because the quantum efficiency is decreased due to cancellation of photo-generated carriers in the deep layer and the P-substrate.

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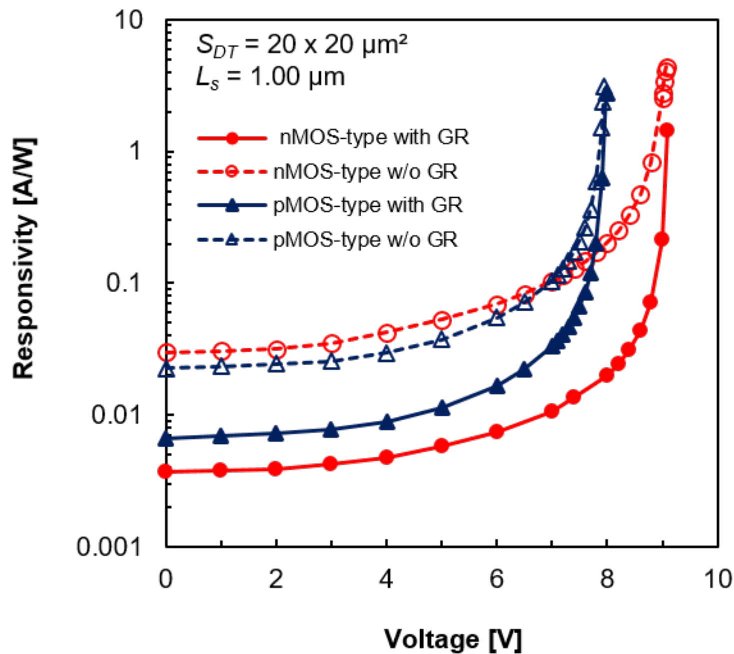

Figure 3.7: The responsivity of nMOS-type and pMOS-type CMOS-APDs with and without the GR as a function of the bias voltage.

3.2.5 Frequency Response

Figure 3.8 shows the frequency response for (a) nMOS-type and (b) pMOS-type CMOS-APD for 8.5 V and 7.5 V bias voltage, respectively, at 850 nm wavelength. The frequency response for the CMOS-APD with the GR is flat until several GHz. On the other hand, the frequency response of the CMOS-APD without the GR shows high signal magnitude for low frequency region and then dropped to the same signal magnitude with the GR structure around 100 MHz. The large signal magnitude of about 15 dB as compared to the CMOS-APD with the GR at low frequency is due to slow diffusion carriers from the deep layer and the P-substrate. The bandwidth of the CMOS-APD with the GR is three orders of magnitude wider as compared to the CMOS-APD without the GR due to cancellation of photo-generated carriers in the deep layer and the P-substrate which are slow diffusion carriers.

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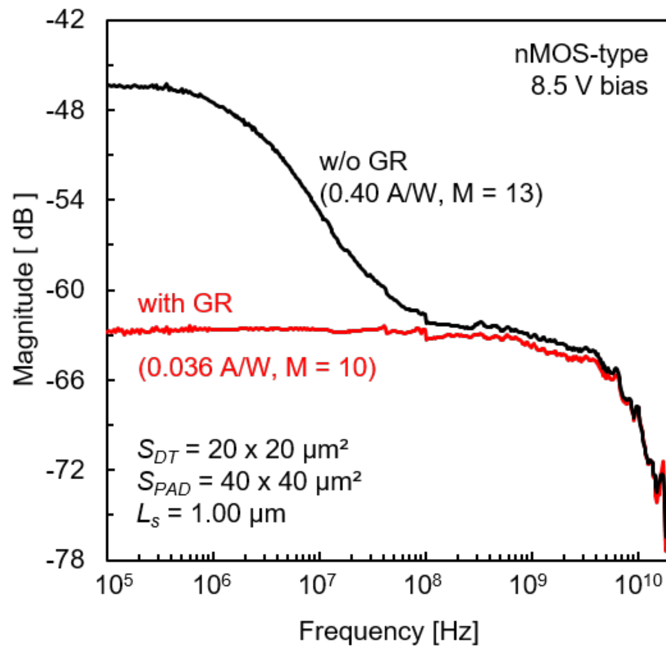
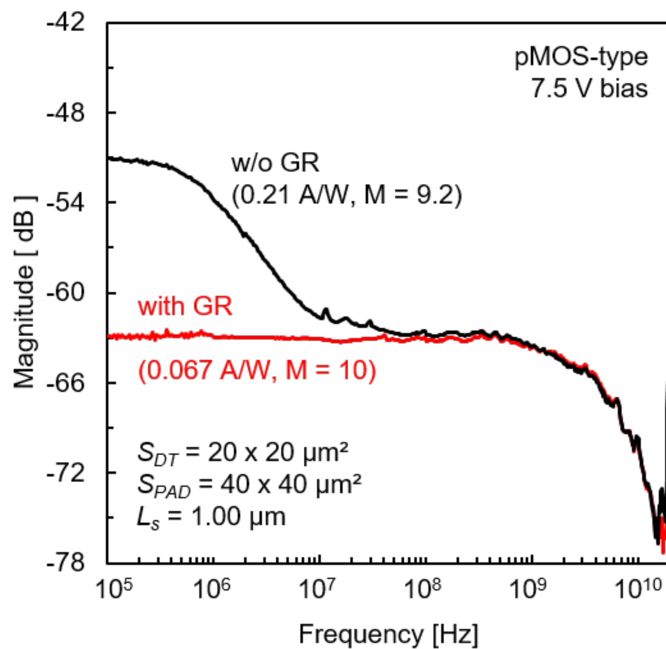


(a)



(b)

Figure 3.8: Frequency response for (a) nMOS-type and (b) pMOS-type CMOS-APD.

The comparison of the frequency response between nMOS-type and pMOS-type CMOS-APDs with the GR is shown in Figure 3.9. From the normalized frequency response, the maximum bandwidth for nMOS-type CMOS-

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APD is 6.77 GHz and is higher than the pMOS-type CMOS-APD of 4.29 GHz. It is due to the quicker avalanche buildup time of electrons compared to the holes, or in other words, the electrons move faster in Pwell rather than holes in Nwell. Therefore, the nMOS-type CMOS-APD with the GR is a suitable candidate for high-speed application. Next, the nMOS-type CMOS-APD will be a subject for CMOS-APD optimization.

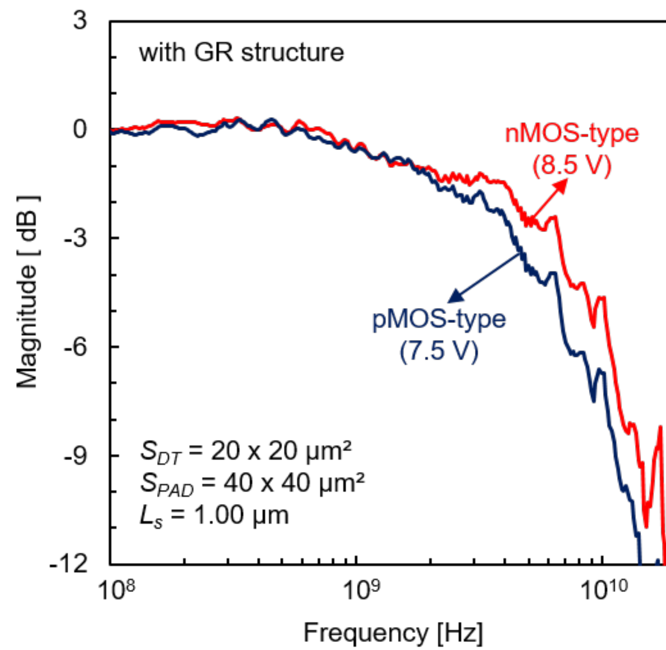

Figure 3.9: The comparison of the frequency response between nMOS-type and pMOS-type CMOS-APDs with the GR.

3.3 Optimization of CMOS-APD

From previous characterization of nMOS- and pMOS-type CMOS-APD, the nMOS-type CMOS-APD with the GR was selected to be optimize due to higher bandwidth performance. Therefore, in this section, details discussion about experimental results on the performance of nMOS-type CMOS-APDs with the GR for various electrode spacing L_s, the detection area S_{DT}, and the PAD size S_{PAD} will be revealed. The idea is that the bandwidth can be improved by reducing the carrier transit time due to decreasing the electrode spacing L_s. Bandwidth enhancement also can be achieved by shrinking the detection area and the PAD size for RF probing due to decreased depletion capacitance and the PAD

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capacitance, respectively. Thus, to incorporate with that idea, the CMOS-APD with several size of the electrode spacing L_s, the detection area S_{DT}, and the PAD size for RF probing S_{PAD} are fabricated as shown in Table 3.1.

Table 3.1: The variation size of the electrode spacing L_s, the detection area S_{DT}, and the PAD size S_{PAD} for size optimization of the fabricated CMOS-APD.

Electrode spacing L_s	**Detection area S_{DT}**	**PAD size S_{PAD}**
0.84 µm	10 x 10 μm^2,	30 x 30 μm^2,
1.00 µm	20 x 20 μm^2	40 x 40 μm^2,
1.52 µm	30 x 30 μm^2	50 x 50 μm^2
2.40 µm	40 x 40 μm^2	60 x 60 μm^2.
4.12 µm	50 x 50 μm^2	70 x 70 μm^2
		100 x 100 μm^2

3.3.1 Electrode Spacing

Figure 3.10 shows the relation between the avalanche gain and the bandwidth of the CMOS-APDs for different electrode spacing L_s. The detection area S_{DT} and the PAD size S_{PAD} are S_{DT} = 20 x 20 μm^2 and S_{PAD} = 40 x 40 μm^2, respectively. The bandwidth is enhanced with decreasing the electrode spacing is maximized when the avalanche gain is about 10 irrespective of the electrode spacing L_s. The maximum bandwidth of 7 GHz is obtained when the avalanche gain is about 10 for the electrode spacing L_s = 0.84 µm. The gain-bandwidth product is the same irrespective of the electrode spacing L_s and is 280 GHz.

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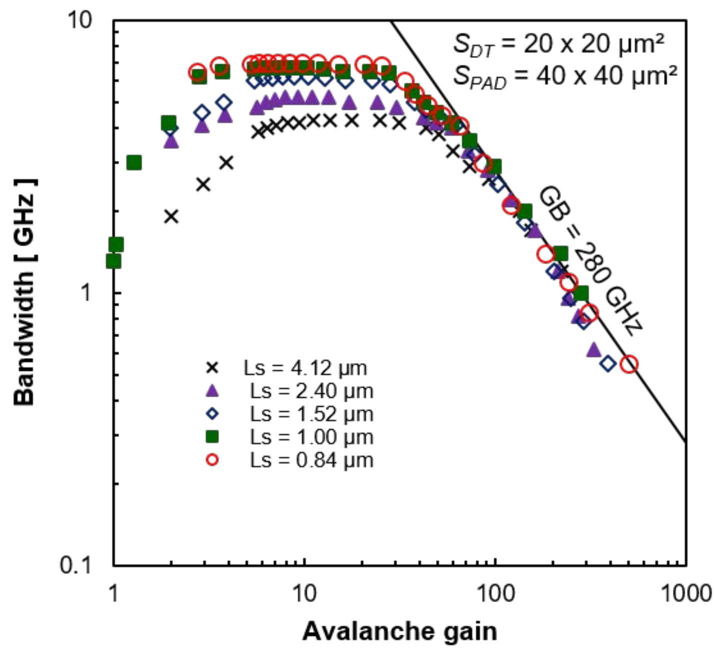

Figure 3.10: The relation between the avalanche gain and the bandwidth of the CMOS-APDs for different electrode spacing L_s.

Figure 3.11 shows the relation between the responsivity and the bandwidth of the CMOS-APDs for different electrode spacing L_s. Since the responsivity depends on the electrode spacing L_s as shown in Figure 3.7, the responsivity-bandwidth product also depends on the electrode spacing L_s, and the value is tabulated in Table 3.2. Commercial fast Si PIN-PD typically has the responsivity of 0.4 ~ 0.5 A/W and the bandwidth of 1 ~ 2 GHz, and the CMOS-APD has wider bandwidth and higher responsivity as compared to commercial Si PIN-PDs at a same bias voltage (below 10 V).

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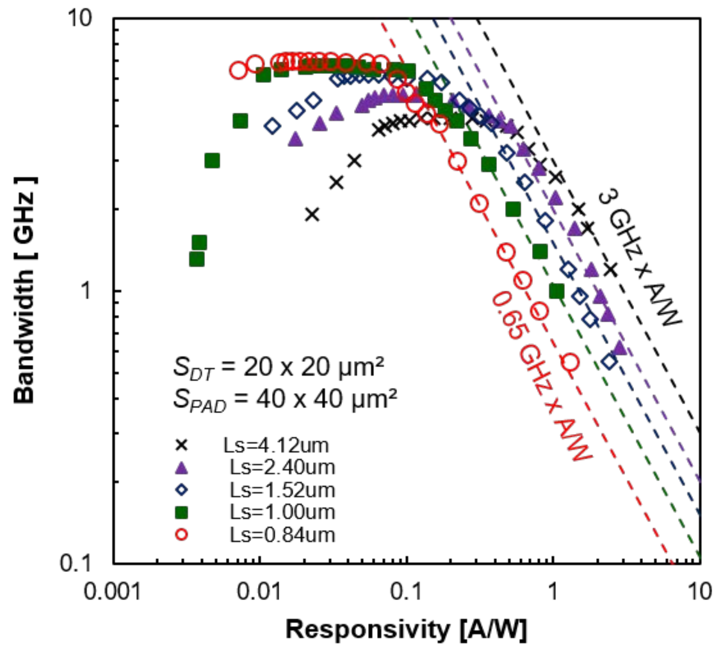

Figure 3.11: The relation between the responsivity and the bandwidth of the CMOS-APDs for different electrode spacing L_s.

Table 3.2: The responsivity-bandwidth product dependence of the electrode spacing L_s.

Electrode spacing L_s (µm)	**Gain-bandwidth product (GHz)**	**Responsivity-bandwidth product (GHz x A/W)**
0.84	280	0.65
1.00	280	1.1
1.52	280	1.5
2.40	280	2.2
4.12	280	3.0

Figure 3.12 shows the relation between the inverse of the maximum bandwidth and the electrode spacing obtained from Figure 3.10. The inverse of the maximum bandwidth is proportional to the electrode spacing Ls, and the maximum bandwidth is estimated to be about 8.4 GHz, which is derived from the electrode spacing L_s = 0 µm.

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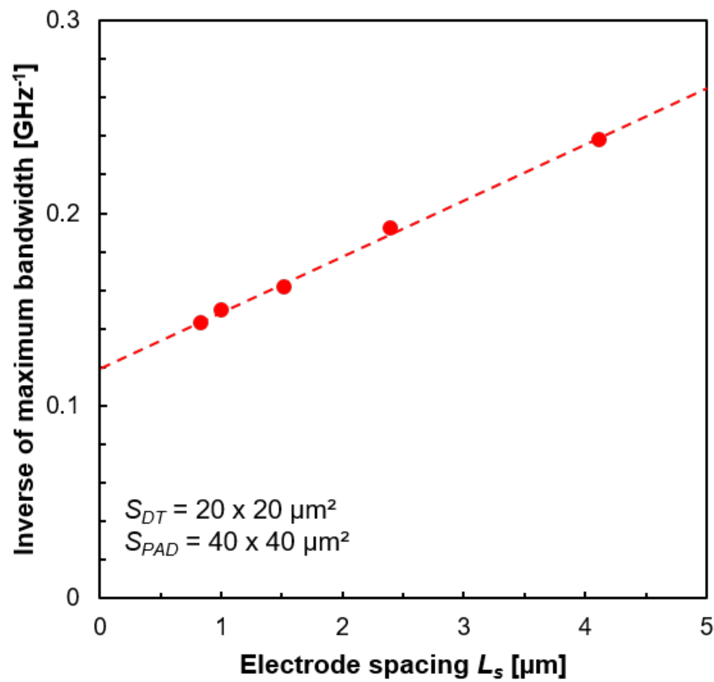

Figure 3.12 The relation between the inverse of the maximum bandwidth and the electrode spacing L_s.

Figure 3.13 shows the device capacitance of the CMOS-APDs at 8.5 V bias voltage against the electrode spacing L_s measured by a LCR meter (Agilent 4284A Precision LCR meter) at 1 MHz. The device capacitance includes depletion capacitance of p-n junctions and the PAD capacitance, and is about 300 fF. The device capacitance is slightly decreased with decreasing the electrode spacing L_s. This is due to decreased total area of the p-n junction between n^+- and Pwell layers because the number of electrodes is increased due to decreased electrode spacing with constant detection area S_{DT}. However, the dependence of the device capacitance on the electrode spacing is very weak, and then the bandwidth enhancement with decreasing the electrode spacing shown in Figure 3.12 is due to decreased carrier transit time owing to electrode spacing narrowing.

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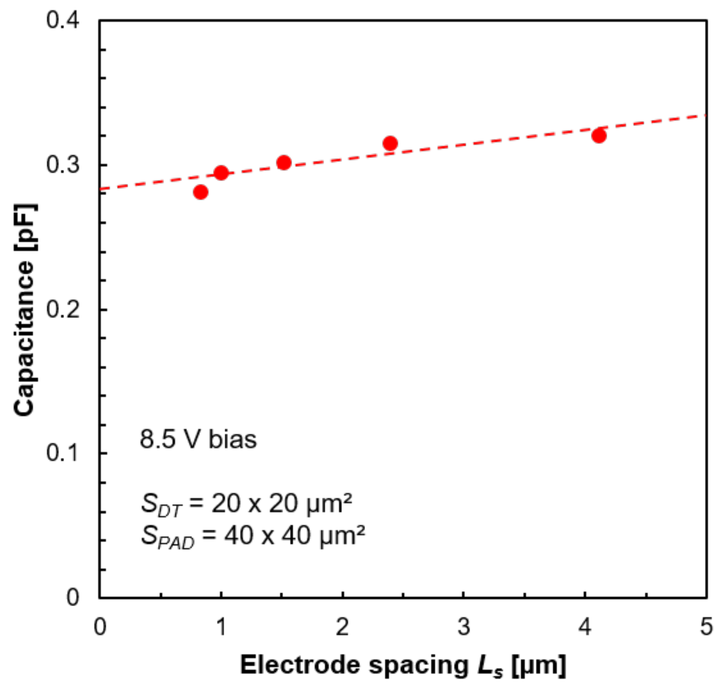

Figure 3.13: The device capacitance of the CMOS-APDs at 8.5 V bias voltage against the electrode spacing L_s.

3.3.2 Detection Area

Figure 3.14 shows the relation between the avalanche gain and the bandwidth for different detection area S_{DT}. The electrode spacing L_s and the PAD size S_{PAD} are L_s = 1.00 μm and S_{PAD} = 40 x 40 μm^2, respectively. The detection area of 10 x 10 μm^2 shows the largest bandwidth of about 8.0 GHz compared to other sizes. It means that, the smaller detection area enhances the bandwidth, however, too-small detection area causes difficulty of light illumination from top of the CMOS-APD.

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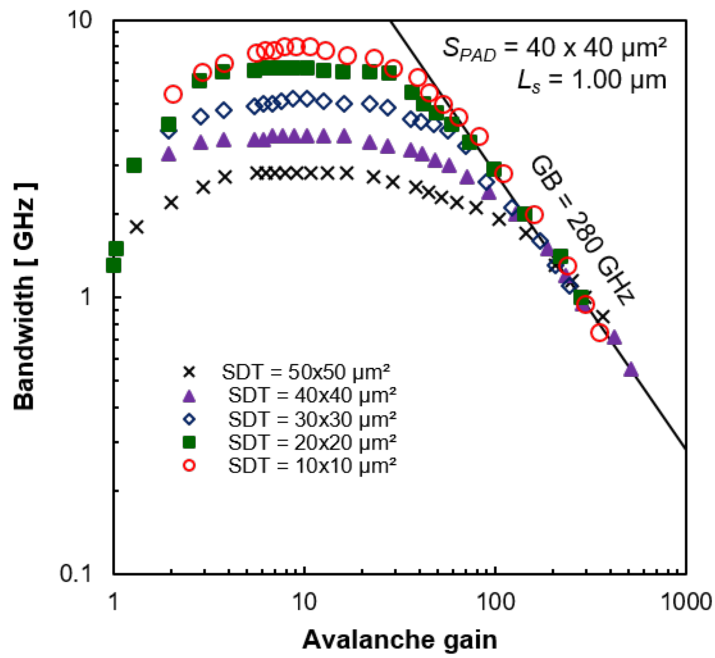

Figure 3.14: The relation between the avalanche gain and the bandwidth for different detection area S_{DT}.

3.3.3 PAD Size

Figure 3.15 shows the relation between the avalanche gain and the bandwidth for different PAD size S_{PAD}. The electrode spacing L_s and the detection area S_{DT} are L_s = 1.00 µm and S_{DT} = 20 x 20 µm^2, respectively. The bandwidth is increased with decreasing the PAD size.

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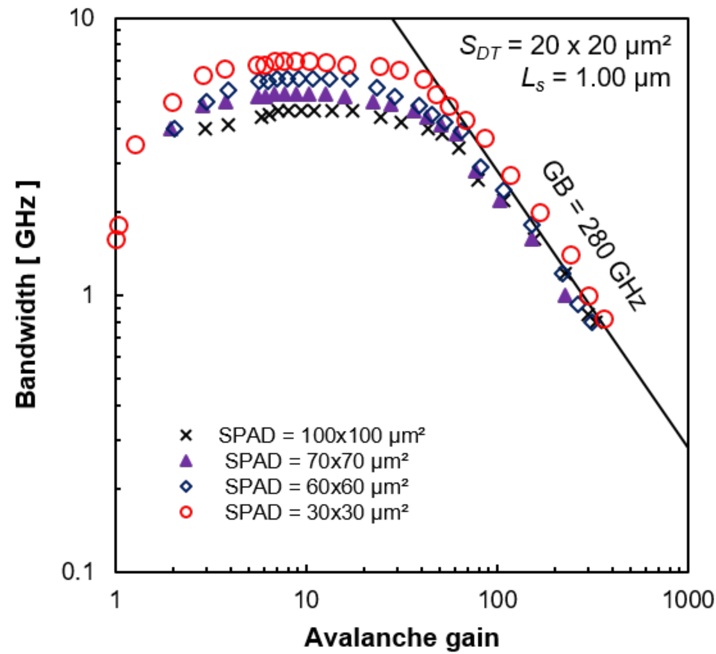

Figure 3.15: The relation between the avalanche gain and the bandwidth for different PAD size S_{PAD}.

3.3.4 The Optimum Size

From Figures 3.10, 3.14, and 3.15, the bandwidth is found to be inversely proportional to the avalanche gain larger than 100, and the gain-bandwidth product (GB) is 280 GHz irrespective of the electrode spacing, the detection area, and the PAD size.

Figure 3.16 shows the relation between the inverse of the maximum bandwidth and the detection area S_{DT} and the PAD size S_{PAD} obtained from Figures 3.14 and 3.15. The open squares are the inverse of the maximum bandwidth against the detection area S_{DT} with the PAD size S_{PAD} = 40 x 40 µm^2, and the closed circles are the inverse of the maximum bandwidth against the PAD size S_{PAD} with the detection area S_{DT} = 20 x 20 µm^2. The inverse of the maximum bandwidth is proportional to both the detection area and the PAD size.

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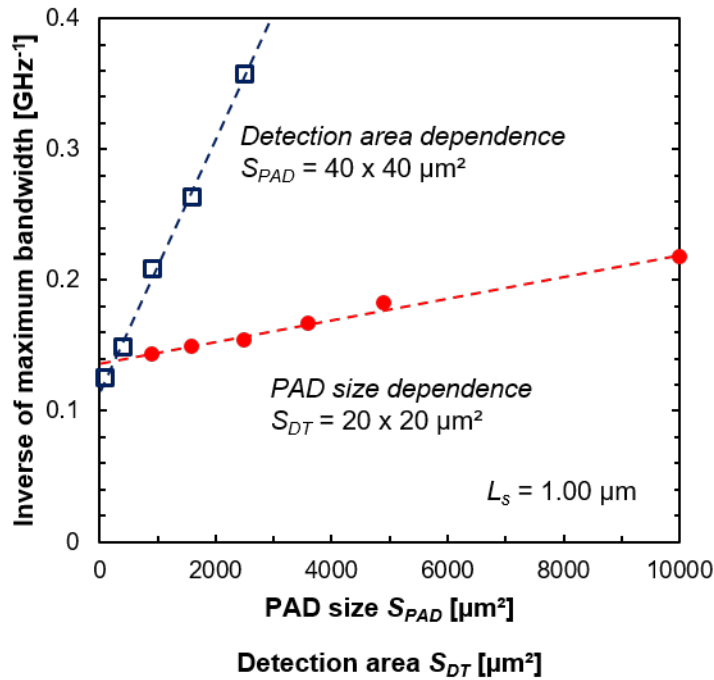

Figure 3.16: The relation between the inverse of the maximum bandwidth and the detection area S_{DT} and the PAD size S_{PAD}.

Figure 3.17 shows the device capacitance of the CMOS-APDs at 8.5 V bias voltage against the detection area S_{DT} and the PAD size S_{PAD} measured by a LCR meter (Agilent 4284A Precision LCR meter) at 1 MHz. The device capacitance is linearly decreased with decreasing the detection area S_{DT} and the PAD size S_{PAD}. The PAD capacitance for S_{PAD} = 40 x 40 µm^2 is estimated to be 100 fF from S_{DT} = 0 µm^2, and the depletion capacitance of the detection area of 20 x 20 µm^2 is estimated to be 244 fF from S_{PAD} = 0 µm^2. The dependence of the device capacitance on the detection area S_{DT} and the PAD size S_{PAD} is almost the same with Figure 3.16. As a result, the bandwidth enhancement with decreasing the detection area and the PAD size shown in Figure 3.16 is due to decreased device capacitance owing to decreased detection area S_{DT} and the PAD size S_{PAD}.

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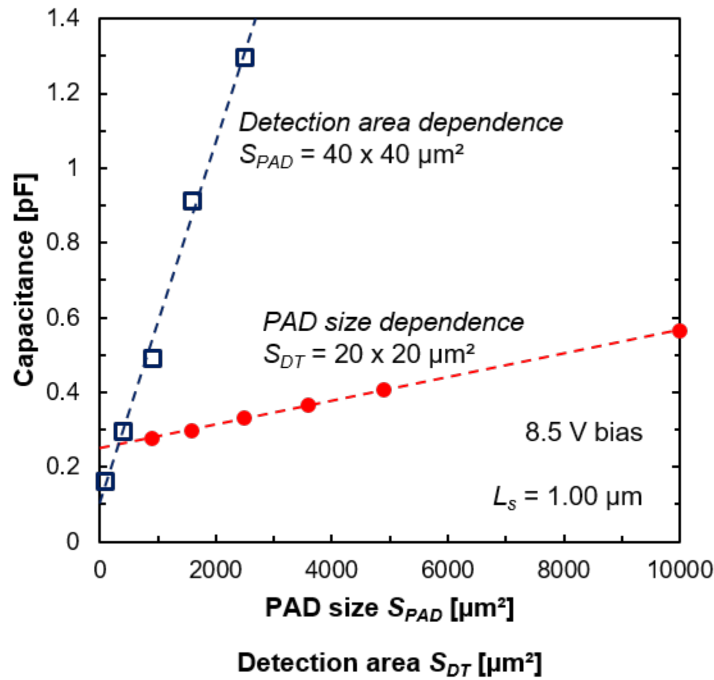

Figure 3.17: The device capacitance of the CMOS-APDs at 8.5 V bias voltage against the detection area S_{DT} and the PAD size S_{PAD}.

Figure 3.18 shows the relation between the device capacitance and the inverse of the maximum bandwidth derived from Figures 3.16 and 3.17. The open squares are the inverse of the maximum bandwidth for different detection area S_{DT} with the PAD size S_{PAD} = 40 x 40 μm^2, and the closed circles are the inverse of the maximum bandwidth for different PAD size S_{PAD} with the detection area S_{DT} = 20 x 20 μm^2. The inverse of the maximum bandwidth is linearly changed with the device capacitance, and then the bandwidth enhancement with decreasing the detection area and the PAD size is due to the decrease of the device capacitance. It is also found that the ultimate bandwidth is estimated to be about 10.7 GHz from the y-intercept. This bandwidth is determined by carrier transit time, and then the bandwidth can be enhanced by decreasing the electrode spacing at the sacrifice of the responsivity because decreased electrode spacing increases the number of electrode and then the effective illuminating area is decreased.

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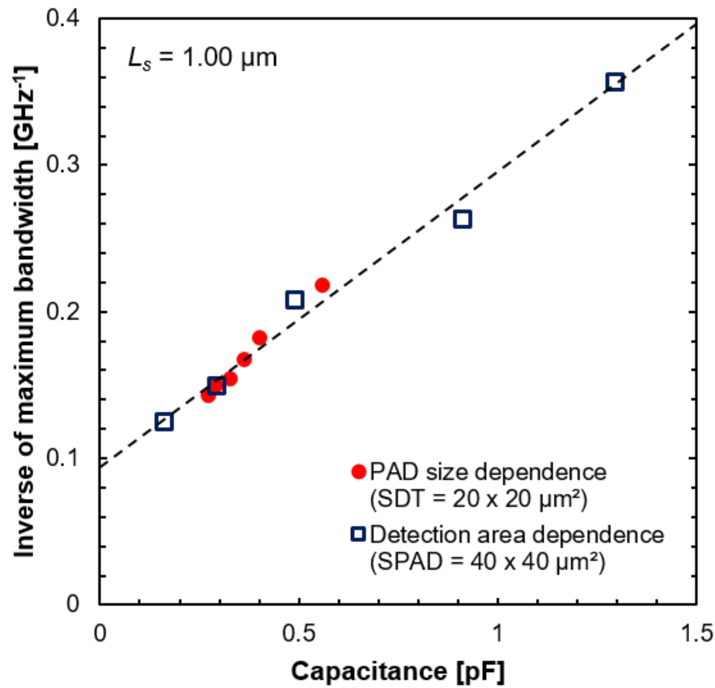

Figure 3.18: The relation between the device capacitance and the inverse of the maximum bandwidth.

Finally, an nMOS-type CMOS-APD is fabricated with the electrode spacing of 0.84 µm, the detection area of 10 x 10 µm^2 and the PAD size for RF probing of 30 x 30 µm^2 along with the guard ring structure for the purpose of high-speed operation. The detection area is determined to effectively illuminate a laser light guided by using a SI-9 optical fiber, and the PAD size is determined to match the tip size of the RF probe. The relation between the avalanche gain and the bandwidth is shown in Figure 3.19. The maximum bandwidth of 8.4 GHz, the gain-bandwidth product of 280 GHz, and the responsivity-bandwidth product of 0.7 GHz x A/W are achieved. The maximum bandwidth is achieved at the avalanche gain of about 10 and the responsivity of about 0.02 A/W.

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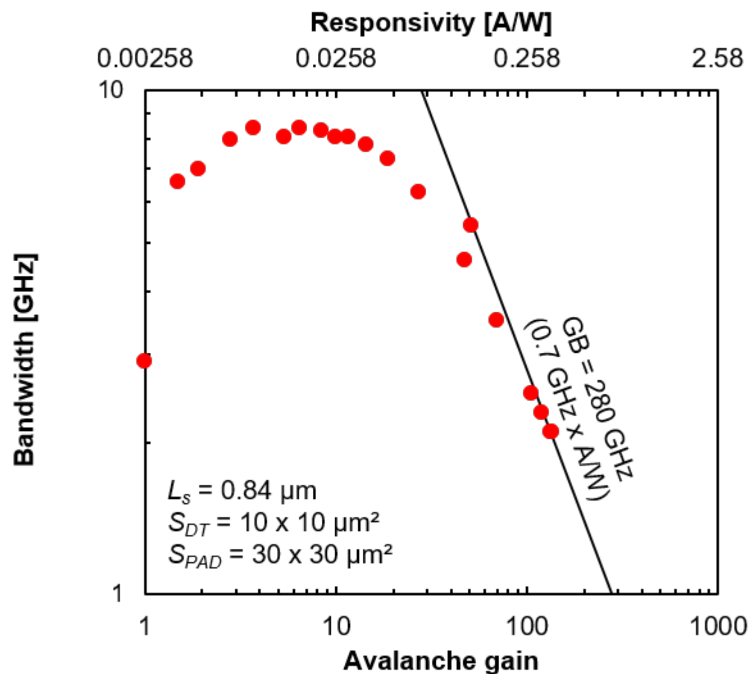

Figure 3.19: The relation between the avalanche gain, the responsivity and the bandwidth for the optimum nMOS-type CMOS-APD with the guard ring.

3.4 Wavelength Dependence

Figure 3.20 shows the cross-sectional structure of a pMOS-type CMOS-APD with the GR included the width of the p^+-layer, n^+-layer, Nwell and electrodes. This structure used to investigate the details experimental results on the wavelength dependence of the I-V characteristics, responsivity, and frequency response. It is because the pMOS-type CMOS-APD structure only have Nwell and P-substrate as compared to nMOS-type CMOS-APD, thus, easily to understand the behavior of each wavelength towards avalanche photodiode. The wavelengths of the input optical signal are 400 nm $\leq \lambda \leq$ 850 nm.

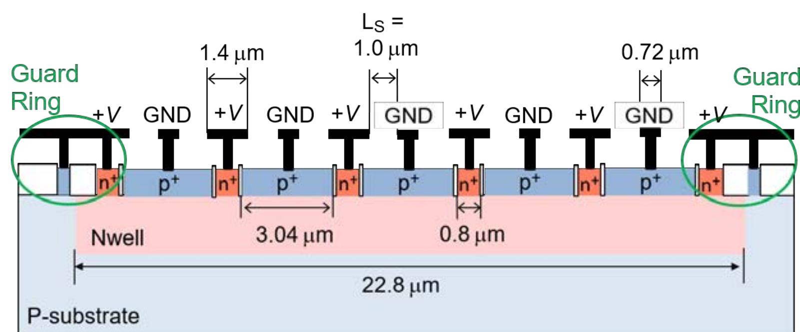

Figure 3.20: Cross-sectional structure of a pMOS-type CMOS-APD.

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3.4.1 I-V Characteristics

Figure 3.21 shows the measured I-V characteristics for with and without the GR structures at wavelengths of 405 nm, 520 nm, 635 nm and 850 nm. At 405 nm wavelength, the I-V characteristics for both with and without the GR structures are almost the same. This is due to strong optical absorption of Si at 405 nm wavelength, and therefore all the incident light is absorbed in the p^+-layer and the Nwell and does not reach the P-substrate. It can be seen that the photocurrent is increased gradually with the bias voltage, and is then significantly increased above 7 V by avalanche amplification. The avalanche gain at 8 V is about 100. At 520 nm wavelength, although the photocurrent of the CMOS-APD with the GR is slightly smaller than of the CMOS-APD without the GR, the difference is insignificant. This is because most of the incident light is absorbed in the p^+-layer and the Nwell and only a few reaches the P-substrate region at 520 nm wavelength. The avalanche gain at 8 V is also about 100.

On the other hand, the difference of the I-V characteristics under illumination at 635 nm wavelength was clearly observed for with and without the GR structures, and the photocurrent of the CMOS-APD with the GR is about half as compared to the CMOS-APD without the GR. This is because the optical absorption of Si at 635 nm wavelength is decreased and a small portion of the incident light reaches the P-substrate region. The electrons and holes photo-generated in the P-substrate move toward the n^+-layer and the p^+-layer, respectively. For the CMOS-APD with the GR, the photo-generated holes are blocked from moving to the Nwell direction by the potential barrier between the Nwell and the P-substrate as shown in Figure 3.4. As the p^+-layer on P-substrate is connected to the n^+-layer on the Nwell, the photo-generated electrons and holes are recombined and do not contribute to the photocurrent. Only electrons and holes photo-generated in the p^+-layer and the Nwell contribute to the photocurrent, and accordingly the photocurrent is decreased. In contrast, large photocurrent is obtained for the CMOS-APD without the GR because the photo-generated electrons and holes in the P-substrate flow to the electrodes through the low potential barrier between the Nwell and the P-substrate as shown in Figure 3.4. The avalanche gain at 8 V is about 100.

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At 850 nm wavelength, the optical absorption of Si is further decreasing, therefore, more carriers are photo-generated in the P-substrate, and then the magnitude of the photocurrent is hugely affected by the mechanisms of the guard ring described above. For this reason, the difference of photocurrent has spread to around 3.3 times between with and without the GR structures. The avalanche gain at 8 V is also about 100.

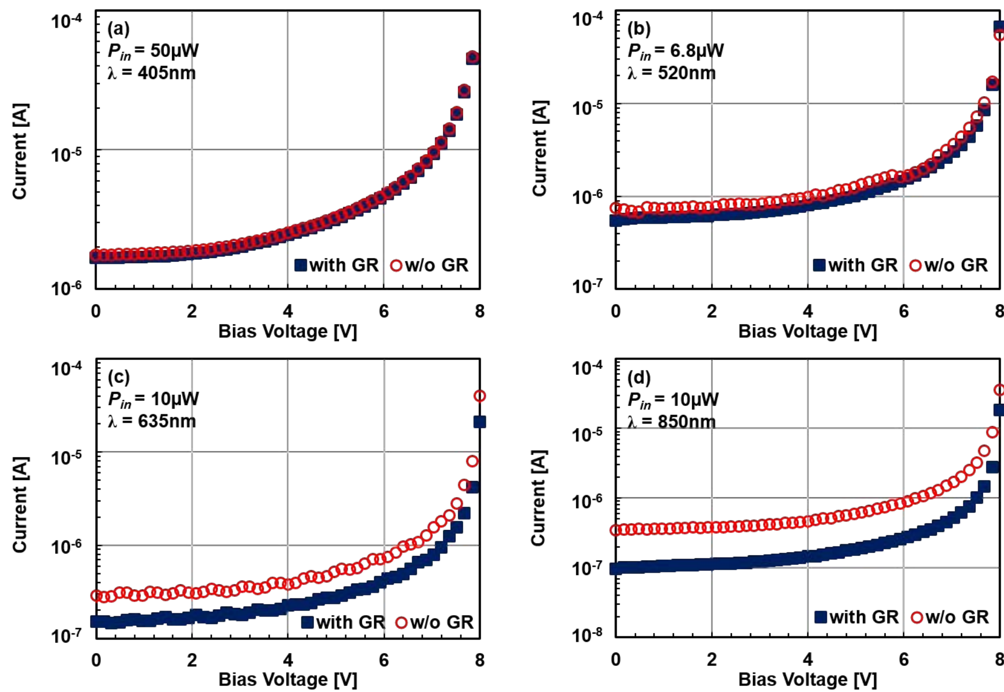

Figure 3.21: Measured I-V characteristics for different wavelengths.

3.4.2 Responsivity

Figure 3.22 shows the wavelength dependence of the responsivity at the bias voltage of 2 V and 7 V, obtained from Figure 3.21. There is no difference in responsivity for both structures at 405 nm wavelength, and the difference increases with increasing the wavelength. At 405 nm wavelength, all the incident light is absorbed in the p^+-layer and the Nwell due to strong optical absorption of Si, and consequently does not reach the P-substrate. As a result, the responsivity is almost same regardless of the guard ring structure. In contrast, due to weak optical absorption of Si at 850 nm wavelength, the incident light can reach the P-substrate region and the GR blocks the photo-generated carriers in the P-substrate, which are slow diffusion carriers, from moving toward the electrodes. Therefore, the

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reduction of responsivity is more severe with the guard ring. The increased responsivity at 7 V is due to avalanche amplification.

The responsivity at 2 V bias (no avalanche gain) for the GR structure at 850 nm wavelength is almost the same with that reported in [23], [27], [28], and the avalanche gain is also almost the same. However, no experimental results of the responsivity for different wavelength have been reported except in [29].

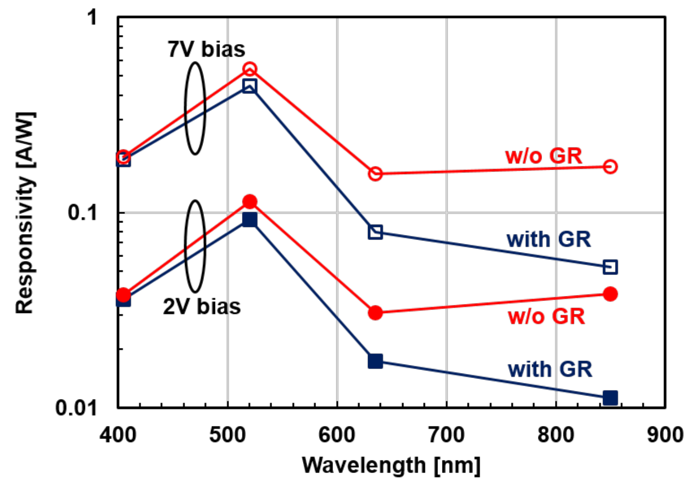

Figure 3.22: Wavelength dependence of the responsivity.

The responsivity R without avalanche gain is given as

$$R = \eta_{ext}\eta_{int}\frac{q}{h\nu} = \eta_{ext}\eta_{int}\frac{q\lambda}{hc} \quad [\text{A/W}] \tag{3.1}$$

where η_{ext} and η_{int} are the external and the internal quantum efficiencies, respectively, q is the electron charge, h is the Planck's constant, h is the frequency of light, c is the speed of light in vacuum, and λ is the wavelength of light. The external quantum efficiency η_{ext} is composed of the ratio of effective illumination area excluding the electrodes and the surface reflection of the device. As is shown in Figure 3.20, total electrode width is 9.2 μm, and then the ratio of effective illumination area is 54% because the detection area is 20 x 20 μm^2. From optical property of intrinsic Si [30], the surface reflectivity R_{Si} depends on wavelength because the refractive index of Si depends on wavelength, and is tabulated in Table 3.3 along with the absorption length of Si, the external quantum efficiency η_{ext}, and

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estimated internal quantum efficiency η_{int} from equation (3.1) and the responsivity at 2 V shown in Figure 3.22. The highest internal quantum efficiency is achieved at 520 nm wavelength. The internal quantum efficiency is slightly decreased with the GR structure at 520 nm wavelength, and then the total thickness of the p^+-layer and the Nwell can be deduced to be slightly shallower than the absorption length of Si at 520 nm wavelength. For 405 nm wavelength, the internal quantum efficiency is decreased as compared with 520 nm wavelength. This is because the illuminated light is absorbed almost in the p^+-layer, and a portion of the photo-generated electrons is recombined with holes in the p^+-layer while traveling toward the n^+-layer. The difference of the internal quantum efficiency due to the guard ring structure is mainly due to measurement error in the photocurrent caused by misalignment of light illumination.

For wavelength longer than 520 nm, the absorption length of Si is increased and then the illuminated light is also absorbed in the P-substrate. A part of the photo-generated carriers is recombined in the P-substrate, and then the internal quantum efficiency is decreased even though without the GR structure. The internal quantum efficiency is also decreased by the GR structure.

Table 3.3: Estimated quantum efficiency of the CMOS-APD.

λ (nm)	R_{Si} (%)	η_{ext} (%)	η_{int} (%)		Absorption length (μm)
			With GR	Without GR	
405	47.6	28.3	38.8	41.0	0.127
520	37.8	33.6	65.4	81.0	1.14
635	34.7	35.3	9.59	17.1	3.17
850	32.5	36.5	4.48	15.3	18.7

3.4.3 Frequency Response

Figure 3.23 shows the measured frequency response for various wavelengths. In this experiments, we focused on the difference of the frequency response due to with or without the GR structure in low frequency region. Since

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the frequency response of the intensity modulated laser light source is not compensated, it is impossible to evaluate the bandwidth of the CMOS-APDs in high frequency region. The decrease in the signal magnitude in high frequency region (more than 100 MHz) is due to decreased modulation efficiency of light sources.

At 405 nm wavelength, there is no difference in the frequency response regardless of the guard ring structure, which is a similar trend to the responsivity characteristics because all the incident light is absorbed in the p^+-layer and the Nwell. At 520 nm wavelength, the signal magnitude of the CMOS-APD without the GR is slightly higher than the CMOS-APD with the GR in low frequency region, and no difference in the signal magnitude is observed for frequency range over 10 MHz. The difference in signal magnitude in low frequency region is related to the slight difference in responsivity at 520 nm wavelength. This is because a small portion of incident light is absorbed in the P-substrate region for 520 nm wavelength as mentioned before, and the carriers photo-generated in the P-substrate are diminished with the the GR. Thus, the signal magnitude is reduced as compared to the CMOS-APD without the GR.

On the other hand, at 635 nm wavelength, the signal magnitude of the CMOS-APD without the GR in low frequency region is obviously higher than the CMOS-APD with the GR. The difference is approximately 6 dB at 100 kHz and is also corresponding to the difference of responsivity at a wavelength of 635 nm in Figure 3.22 which is about 2 times. This is because the carriers photo-generated in the P-substrate reaches the electrodes and contribute to the photocurrent. As the carriers photo-generated in the P-substrate is slow diffusion carriers due to weak electric field, the signal magnitude is reduced in the frequency of several MHz. At 850 nm wavelength, the difference in signal magnitude in low frequency region becomes more apparent, which is about 10 dB at 100 kHz. This difference also corresponds to the difference of responsivity in Figure 3.22, approximately 3 times. There is no difference in the frequency response over 10 MHz regardless of the guard ring structure at 635 nm and 850 nm wavelength. The bandwidth of the CMOS-APD without the GR is about 1 MHz or less, while the bandwidth of the CMOS-APD with the GR is found to be more than 100 MHz, which is limited by

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the modulation bandwidth of laser sources. The bandwidth of more than 1 GHz is expected for the CMOS-APD with the GR because the bandwidth of more than 1 GHz was already achieved for the same CMOS-APD at 830 nm wavelength [22]. The bandwidth is significantly improved by the guard ring because slow diffusion carriers photo-generated in the P-substrate are canceled by the GR structure.

From all the results above mention, CMOS-APD with the GR is very beneficial for practical application. The guard ring enhances bandwidth although the responsivity is decreased for wavelength longer than 520 nm. For wavelength shorter than 520 nm, although the bandwidth is same regardless of the guard ring structure, the guard ring is very effective for realizing low dark current shown in Figure 3.6 (b).

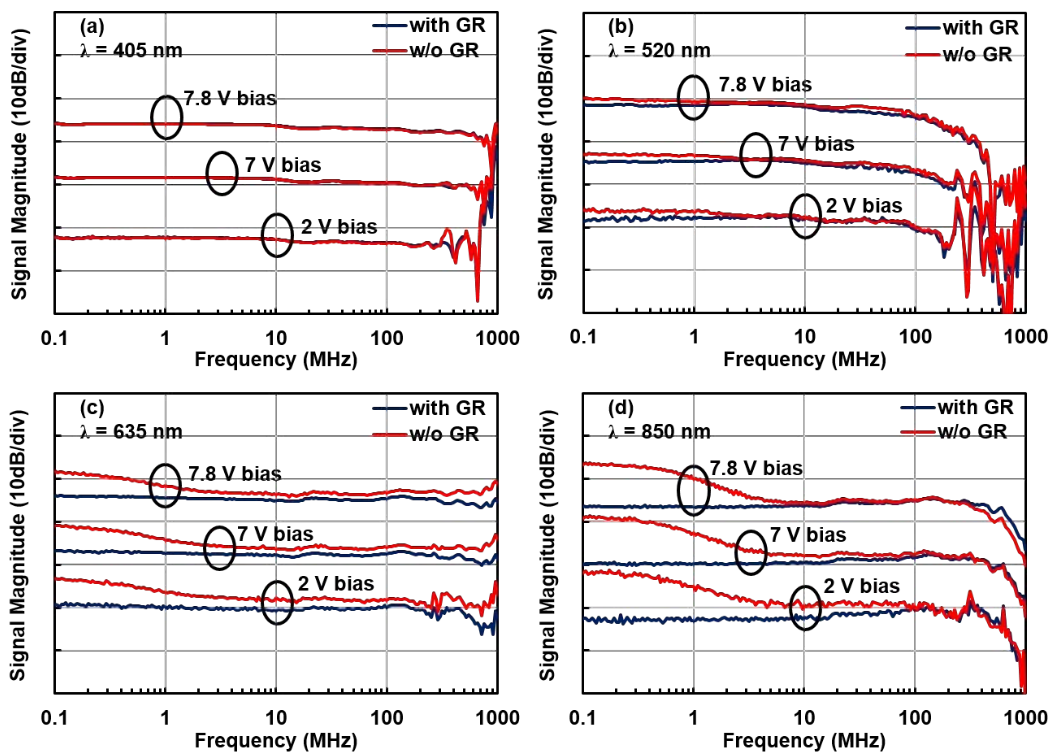

Figure 3.23: Frequency responses for different wavelengths.

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3.5 Summary

nMOS-type and pMOS-type CMOS-APDs with and without guard ring (GR) are fabricated by standard 0.18 μm CMOS process without process modification. The responsivity of the CMOS-APD with the GR is lower than CMOS-APD without the GR because the quantum efficiency is decreased due to elimination of photo-generated carriers in the deep layer and the P-substrate. However, the maximum bandwidth for the CMOS-APD with the GR is wider as compared to the CMOS-APD without the GR due to elimination of photo-generated carriers in the deep layer and the substrate because the carriers are slow diffusion carriers. The nMOS-type CMOS-APD is faster than the pMOS-type CMOS-APD and is suitable for high-speed application. By optimizing the electrode spacing to 0.84 μm, decreasing the detection area and the PAD size for RF probing to 10 x 10 μm^2 and 30 x 30 μm^2, respectively, the maximum bandwidth of a CMOS-APD is enhanced to 8.4 GHz with the gain-bandwidth product of 280 GHz and the responsivity-bandwidth product of 0.7 GHz x A/W.

On the other hand, the wavelength dependence of the responsivity and bandwidth of the CMOS-APDs with and without the GR has been successfully characterized. At a wavelength of 520 nm or less, there is no difference in the responsivity and the frequency response because all the illuminated light is absorbed in the p^+-layer and the Nwell due to strong light absorption of Si. However, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are canceled by the GR structure for the wavelength longer than 520 nm, and then bandwidth was remarkably enhanced at the sacrifice of the responsivity. In terms of low dark current and wide bandwidth performance, the introduction of the GR structure in CMOS-APDs is found to be effective.

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CHAPTER 4

PHOTORECEIVER

All important information of the photodiodes has been treated extensively in previous chapters. In this chapter, the photoreceiver which is the subsequent element of the photodiode is clarified.

First, an introduction for this chapter is explained. The important building block in the photoreceiver is transimpedance amplifier (TIA) that converts small photodiode currents to a voltage, and then the specifications of TIA are described. After that, two different TIA circuit design with the circuit configuration, principle, and their simulation results are discussed. Finally, all the key points related to this chapter are summarized.

4.1 Introduction

Photodiodes by themselves are generally not sufficient to produce directly signals that can be used for optical information processing systems. In most cases, the photocurrent produced by the photodiode is quite weak and require electronic amplification before it can be used for further processing. Therefore, it is essential to have an amplification circuit along with photodiode because the CMOS-APDs have no internal gain. The amplification used in this research is TIA.

Recently, a lot of pre-amplifier especially TIA have been widely researched. Several TIA are designed to improve the performance of bandwidth, gain and, sensitivity. For instance, the common-gate (CG), common-source (CS), common-drain (CD), and regulated cascade (RGC). As usual, to achieve higher bandwidth for example, some parameter should be increases or decreases, but it has a trade-off to another performance such as gain and vice versa. Thus, to realize the photoreceiver which offer state-of-the-art performance, optimization of each device is necessary. In this chapter, we focus on available high-speed TIA which can be integrated with our photodiodes to realize a photoreceiver.

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4.2 TIA

Since the photodiodes produce a small current and the following process attempts in the voltage domain, the current must be converted to voltage. This task can be handle by a transimpedance amplifier TIA, where, the input signal of a TIA is a current and the output signal is a voltage. Figure 4.1 shows the basic schematic of a TIA with the photodiode as its input.

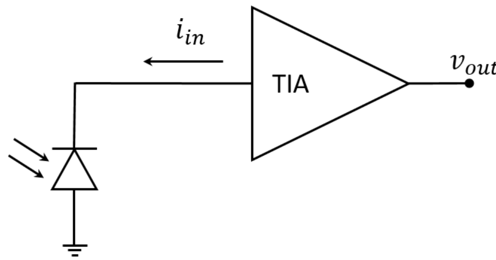

Figure 4.1: The basic schematic of a TIA.

The relationship between both signals is known as transimpedance gain, as shown below.

$$Transimpedance\ gain = \frac{v_{out}}{i_{in}} \tag{4.1}$$

where v_{out} is output voltage and i_{in} is input current. The input current from the photodiode, i_{in} is actually the small photocurrent of the photodiode, i_{pd}. The output unit of TIA is a transimpedance gain, Ω or $dB\Omega$.

TIA has several advantages such as ease of biasing, high bandwidth, low noise, and low input resistance. Besides that, TIA has to be design wisely because it has some tradeoffs between the sensitivity (due to noise), speed (bandwidth) and transimpedance gain. Transimpedance gain is usually equal to the feedback resistor for large open-circuit amplifications [31]. If the output voltage signal is small, post-amplifier is needed to further amplify the signal. The gain is increase with increasing the feedback resistance, but at the same time, the bandwidth of the preamplifier will reduce by increasing the input resistance [31].

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In this research, there are two TIA design which are common-source and regulated-cascode. It is necessary for the TIA circuit satisfy the following conditions; (1) the output signal with sufficient voltage amplitude to make sure the electronic circuit connected to the subsequent stage can be operate, and (2) have fast response in GHz order. To achieve these conditions, the TIA circuit should have a high-speed response compare to the CMOS-APD and low power consumption.

4.3 Common-Source TIA

4.3.1 Principle

Figure 4.2 shows the voltage-current or shunt-shunt feedback topology so-called common-source TIA. This type of feedback was preferred because it can degrade both input resistance and then increase the bandwidth by increasing the input pole magnitude and output impedance, thus it can produce better drive capability. It is also selected because of the ability to achieve high sensitivity and wide bandwidth simultaneously. By referring the common source configuration of TIAs as depicted in Figure 4.2, typically shunt feedback resistance, R_F role is to provide low input impedance. Resistive load, R_L, on the other hand, is usually used to get wider bandwidth response. However, it suffers from direct trade-off between gain and voltage headroom. The achievable transimpedance gain of each stage is reduced by load resistance which is required the headroom at low voltage supplies. Higher scaled of 65 nm or 45 nm CMOS technologies offer NMOS and PMOS devices with high unity gain cut-off frequencies. Consequently, high-speed data communication can get this advantages by using high scale CMOS technologies. However, as the device size of these technologies is scales down, the breakdown voltage of the transistors is also decreases. Thus, low supply voltage is needed for successful operation. Therefore, the trade-off between gain and voltage headroom for common source TIA is become more critical in nano-scale circuit design.

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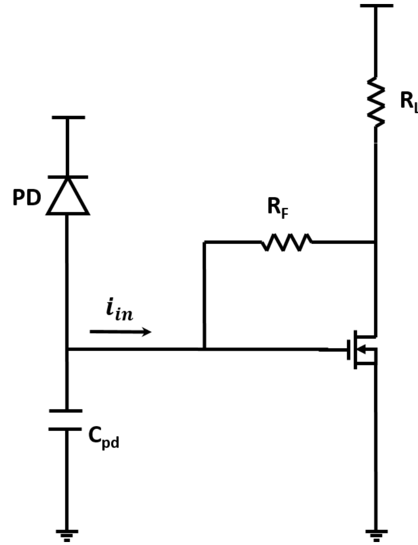

Figure 4.2: Common-source TIA with shunt feedback.

The transimpedance gain and input resistance of a common-source TIA with shunt feedback are (4.2) and (4.3), respectively,

$$Z_{TIA} = \frac{g_m R_F - 1}{g_m R_L + 1} R_L = -R_F \tag{4.2}$$

$$R_{in} = \frac{R_F + R_L}{g_m R_L + 1} \tag{4.3}$$

From (4.2) and (4.3), a trade-off between transimpedance gain and input resistance of common-source TIA occurs. To make the transimpedance gain higher, R_F needs to be increased, but increasing R_F increases the input impedance which yields the reduction of input pole frequency.

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4.3.2 Circuit Configuration

Figure 4.3 shows the schematic diagram of a common-source TIA. In this circuit, the gain can be increased or decreased by changing the resistances R1 and R2 or the gate width W of the MOSFET. Although the gain can be increased by increasing the value of each parameter, but, it is different for each parameter. Therefore, it is necessary to select the parameter properly according to the feature. In addition, it is desirable that the gain is large, but as the gain is increased, the range for linear amplification is possibly narrows and maybe the waveform collapses, so it is important to balance with the input signal current.

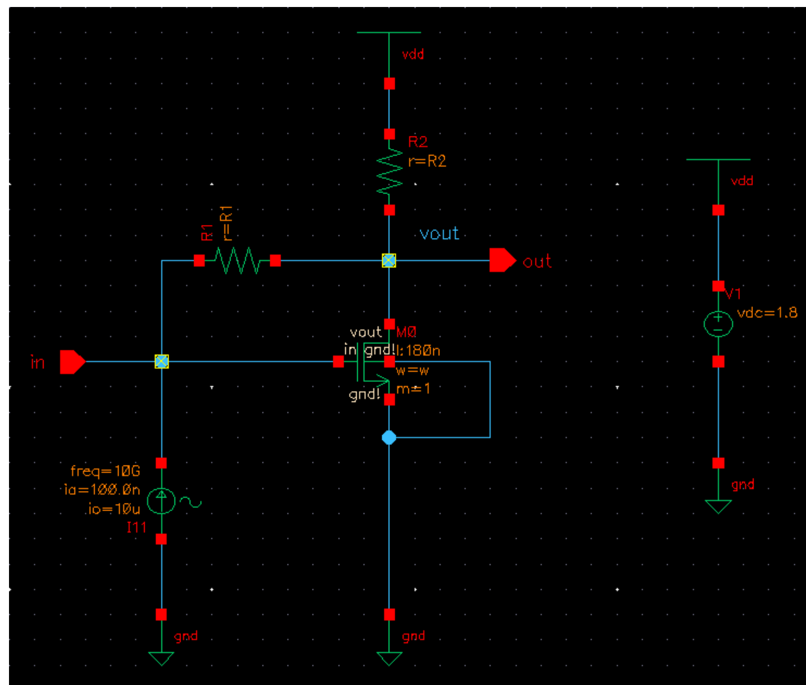

Figure 4.3: Schematic diagram of a common-source TIA.

4.3.3 Simulation Results

At first, DC analysis of the CS is done by varied the parameters of resistances R1 and R2 and the gate width W. The gate length L of the nMOS is 0.18 μm, which is the minimum value in this technology aims for high-speed response. By using 3 types of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and 5 types of W: 0.5 μm, 1 μm, 2 μm, 5 μm, 36 simulations were performed in total. As a results,

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(i) the wider the gate width, the steeper the slope of the IV characteristic, therefore, the gain is increased.
(ii) Gain is also increased if R1 or R2 value increased.
(iii) it is more effective to increase the gain if R2 larger than R1.
(iv) but, if the gain is too high, the linear amplification range becomes narrow, so it is not suitable for the TIA.

In order to investigate whether the simulation is correctly performed, the transient analysis is simulated. Randomly, the simulation was carried out with the resistance value R1 = 10 kΩ, R2 = 10 kΩ, and varied the gate width W to 0.5, 1, 2, 5 µm. Three types of input currents are examined: 0, 25, and 50 µA. As a result, the output current for 0, 25, and 50 µA input current is same with previous DC analysis. Thus, this simulation is in good agreement and can proceeds for frequency response analysis.

To simulate the frequency response, input of the simulation is AC current and the output voltage is in the logarithmic region, then, a -3 dB bandwidth is obtained. To consider which combination that each parameter gives a wider -3 dB bandwidth, the conditions are similar to DC analysis. The resistors R1 and R2 and the gate width W are variables, and the gate length L of the nMOS is fixed to 0.18 µm, which is the minimum value in the process in order to achieve high-speed response. The input signal current was selected as the offset value of 10 µA, which is a region where linear amplification is possible in all parameters. The amplitude was set at 0.1 µA, which was sufficiently small with respect to the offset.

A total of 36 simulations were performed by three values of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and four values of W: 0.5 µm, 1 µm, 2 µm, 5 µm. As results, the resistors that yields the optimum results are R1: 20 kΩ and R2: 50 kΩ. The frequency response for these resistors is shown in Figure 4.4 and all the results related to gain, transimpedance gain, bandwidth and gain-bandwidth product are tabulated in Table 4.1. Typically, the gain-bandwidth product is a figure of merits that can define the optimum design of the particular circuit because gain and bandwidth is trade-off. Therefore, for this common-source TIA, the optimum parameters are R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 µm, that provide the results of

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transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ.

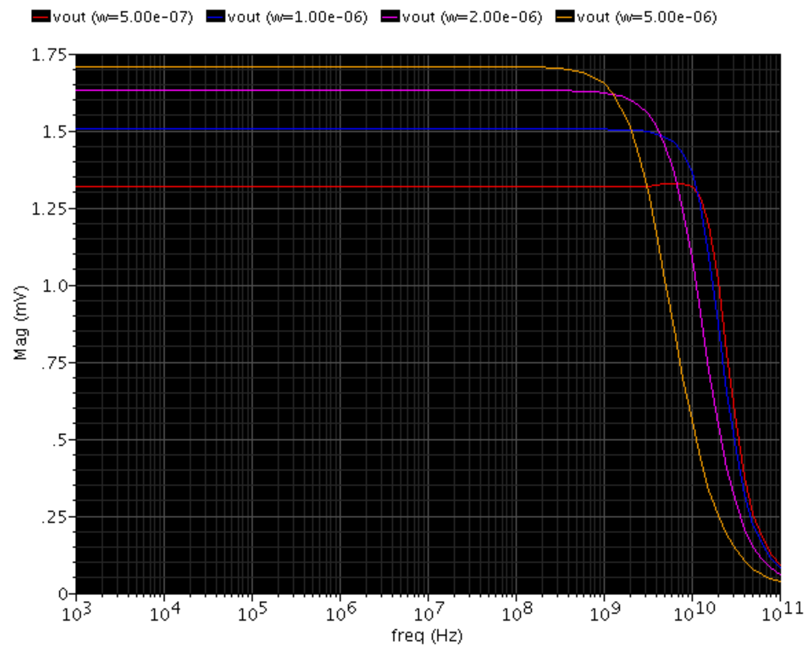

Figure 4.4: Frequency response of the common-source TIA.

Table 4.1: Simulation results for selected parameters of the common-source TIA.

Parameters			Simulation Results			
R1 [kΩ]	R2 [kΩ]	w [um]	Gain [kΩ]	Transimpedance Gain [dBΩ]	BW [GHz]	GB Product [THz × dBΩ]
20	50	0.5	12.84	22.17	21.21	470.23
		1	14.69	23.34	14.63	341.46
		2	15.80	23.97	8.64	207.10
		5	16.89	24.55	3.93	96.48

4.4 Regulated-Cascode TIA

4.4.1 Principle

Figure 4.5 shows the regulated-cascode (RGC) amplifier that is widely used for TIA design in high-speed optical communication. RGC is well known to deliver the high output impedance and wide output voltage range [32]. RGC is actually a modified common gate amplifier, which is the common gate architecture with a local feedback. The common gate amplifier consists of

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transistor M_1 and resistor R_1. The local feedback is produced by transistor M_2 that has connected between the gate and source of M_1.

Resistor R_2 and transistor M_2 forms a common source configuration that gets a small portion of input signal and then produces a voltage at the gate of M_1. At the output of M_1, this signal is amplified and then common gate configuration increases the amplified output of M_1. The effective transconductance of whole architecture is increased by M_2 which benefits to reduce the input resistance to separate the input pole connected with large parasitic capacitance, C_{pd} from the bandwidth determination. The dominant pole of RGC is usually located within the amplifier rather than at the input node as offer by common gate or common source TIAs. The input resistance and transimpedance of RGC are shown in (4.4) and (4.5), respectively [33].

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2}R_2)} \tag{4.4}$$

$$Z_{TIA} = \frac{v_{out}}{i_{in}} = \frac{R_1}{s^2 C_{PD} C_0 R_{in} R_{out} + s(C_{PD} R_{in} + C_0 R_{out}) + 1} \tag{4.5}$$

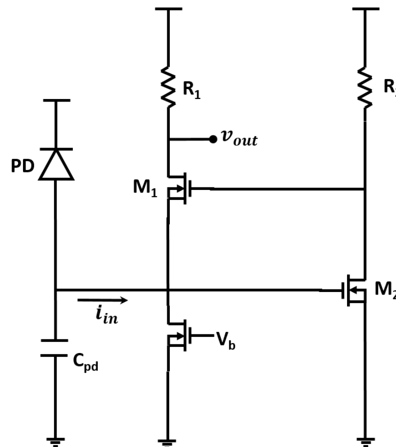

Figure 4.5: Regulated-cascode (RGC)

The RGC TIA has a good potential for optical receiver applications with high gain, low noise, and lower power consumption characteristics.

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4.4.2 Circuit Configuration

Figure 4.6 shows the schematic diagram of a regulated-cascode TIA. In this circuit, the photocurrent is amplified to be a voltage at the drain of M1. The M2 and R3 stage functions as a local feedback to reduce the input impedance by its voltage gain. The input signal used for this circuit is same with previous common-source circuit. The output signal is located between the source of transistor M1 and resistor R2. The input voltage is 1.8 V. The gate length L of all the transistors is 0.18 µm, which is the minimum value in this technology aims for high-speed response.

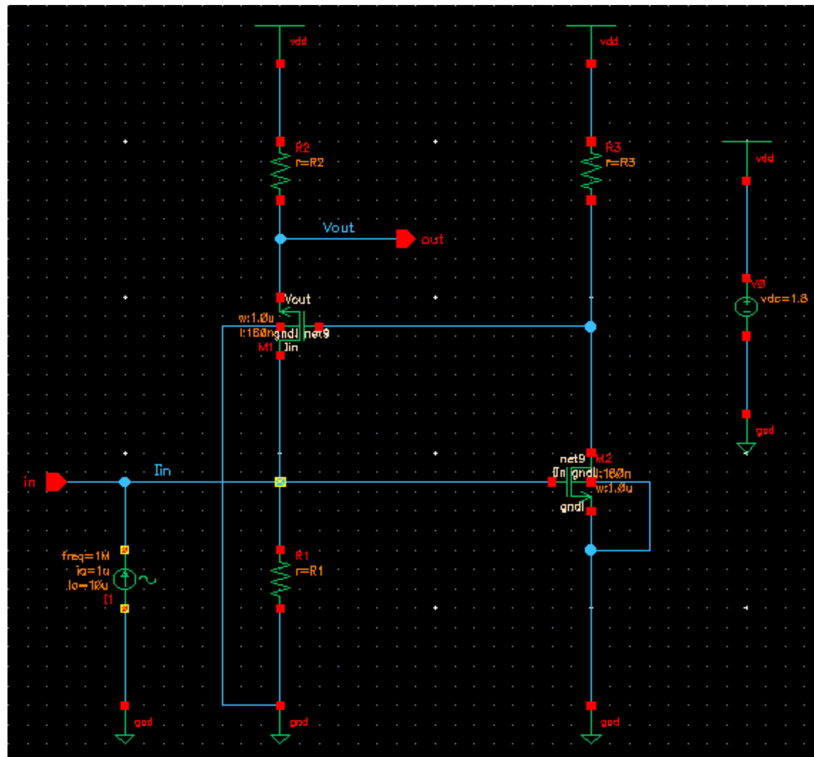

Figure 4.6: Schematic diagram of a regulated-cascode TIA.

4.4.3 Simulation Results

The method used to find the optimum parameters of RGC circuit is quite same with previous common-source circuit analysis. The parameters for this RGC circuit analysis is three types of resistors: R1, R2, and R3. The values are varied for 10 kΩ, 20 kΩ, and 50 kΩ, therefore, a total of 26 simulations were performed. The

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gate length and width for both transistors are 0.18 μm and 1 μm, respectively. The target bandwidth and transimpedance gain for this RGC TIA are > 9GHz and > 54 dBΩ, respectively. Form all 26 simulations, only four combinations meet both requirement and tabulated in Table 4.2. Based on the highest gain-bandwidth product, the optimum parameter values for the combination of resistors R1, R2, and R3 are 20 kΩ, 10 kΩ, and 10 kΩ, respectively. The bandwidth achieve for this RGC TIA is 10.64 GHz and transimpedance gain of 79.45 dBΩ with the gain-bandwidth product of 845.35 THz × dBΩ. The frequency response is shown in Figure 4.7.

Table 4.2: Simulation results for selected parameters of the regulated-cascode TIA.

R1 [kΩ]	R2 [kΩ]	R3 [kΩ]	BW [GHz]	Transimpedance Gain [dBΩ]	GB Product [THz × dBΩ]
10	10	10	9.69	79.25	767.93
		20	9.26	79.42	735.43
20		10	10.64	79.45	845.35
		20	10.45	79.51	830.88

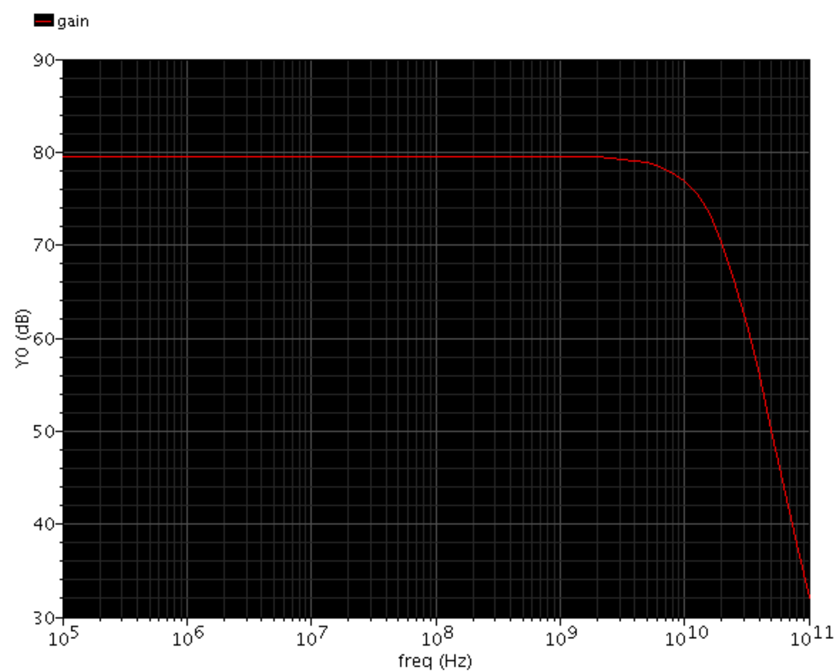

Figure 4.7: Frequency response of a regulated-cascode TIA.

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4.5 Summary

This chapter provides the analysis of TIA which is a subsequent stage after successful designed of CMOS-APD in previous chapter. An overview of the existing transimpedance amplifiers in CMOS technology such as common source and regulated cascade has been described. Their design with pros and cons are also discussed. The main goal of this chapter is to find the optimum parameters for both type of TIA circuits in term of resistances and channel width of the transistor to achieve high transimpedance gain and high bandwidth performance. However, trade-offs between gain and bandwidth are hindrances to attain optimum performance of the TIA. Therefore, the figure of merits of gain-bandwidth product is used to find the ideal results. The common-source TIA provide the good results of transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ via the optimum parameters of R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 µm. On the other hands, the RGC configuration that is a modified common gate amplifier enhances the effective input transconductance and therefore isolates efficiently the large input parasitic capacitance from the bandwidth determination. It also relaxes the effect of the large input capacitance on the high-frequency noise characteristics. The simulated results of the RGC TIA demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth and 845.35 THz × dBΩ gain-bandwidth product for 20 µA input current. Both of the results of common-source and RGC TIA meet the target of this research to realize a high-speed photoreceivers for our successful CMOS-APDs.

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CHAPTER 5

CONCLUSION AND SUGGESTION

5.1 Conclusion

Optical communication has been realized mainly in long-haul communication, and recently board-to-board and chip-to-chip optical interconnection have been actively studied. In order to realize the optical interconnection, it is necessary to integrate optical devices such as light sources, optical waveguides, and photodetectors with electronic circuits. Fast photoreceivers that are integrated photodetector and electronic circuits have been ready in the market, but their cost was too high since they are designed in expensive technology such as InP or InGaAs. However, by using CMOS process, it is possible to easily integrate photodetectors and electronic circuits on same Si substrate with low-cost because CMOS process is mature process.

Avalanche photodiode fabricated by CMOS process (CMOS-APDs) have been developed for optical interconnection applications [21], [28], [34], [35]. CMOS-APDs have high avalanche amplification below 10 V bias. The bandwidth of the CMOS-APD, however, is limited by slow photo-generated carriers from the substrate because all the electrodes are arranged on the surface of the substrate. One solution is to add guard ring (GR) structure in the CMOS-APD. The maximum bandwidth for the CMOS-APD with the GR is wider as compared to the CMOS-APD without the GR due to elimination of photo-generated carriers in the deep layer and the substrate because the carriers are slow diffusion carriers. The nMOS-type CMOS-APD is faster than the pMOS-type CMOS-APD and is suitable for high-speed application. However, the responsivity of the CMOS-APD with the GR is lower than CMOS-APD without the GR because the quantum efficiency is decreased due to elimination of photo-generated carriers in the deep layer and the P-substrate. This become a trade-off between bandwidth performance and responsivity. It means that, several parameters for the CMOS-APD must be carefully selected to achieve balance

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results of the bandwidth and responsivity. It is also important to investigate the figure of merits of responsivity-bandwidth product. By optimizing the electrode spacing to 0.84 μm, decreasing the detection area and the PAD size for RF probing to 10 x 10 μm^2 and 30 x 30 μm^2, respectively, the maximum bandwidth of a CMOS-APD is enhanced to 8.4 GHz with the gain-bandwidth product of 280 GHz and the responsivity-bandwidth product of 0.7 GHz x A/W.

On the other hand, the wavelength dependence of the responsivity and bandwidth of the CMOS-APDs with and without the GR has been successfully characterized. At a wavelength of 520 nm or less, there is no difference in the responsivity and the frequency response because all the illuminated light is absorbed in the p^+-layer and the Nwell due to strong light absorption of Si. However, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are eliminated by the GR structure for the wavelength longer than 520 nm, and then bandwidth was remarkably enhanced at the sacrifice of the responsivity. In terms of low dark current and wide bandwidth performance, the introduction of the GR structure in CMOS-APDs is found to be effective. Therefore, for above mention results, it can conclude that the first two objectives of this research are achieved.

The final objective of this research is to find the optimum parameters for both type of TIA circuits in term of resistances and channel width of the transistor to achieve high transimpedance gain and high bandwidth performance. Nevertheless, trade-offs between gain and bandwidth are difficulties to attain optimum performance of the TIA. Therefore, the figure of merits of gain-bandwidth product has to be investigated to achieve the target results. Two types of TIA that are common-source and regulated-cascode TIA has been selected to convert and amplify the photocurrents from CMOS-APDs to the voltage signal along with transimpedance gain and bandwidth. As a results, common-source TIA produce a transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ by the optimum parameters of R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 μm. On the other hands, the regulated-cascode TIA demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth and 845.35

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THz × dBΩ gain-bandwidth product. Thus, from these results, the final objective for this research is found to be achieved.

5.2 Suggestion

This research has established that the CMOS-APD is a candidate detector for use in high-speed integrated CMOS photoreceivers. The developed CMOS photoreceivers, however, are not optimum and further research on these receivers is required.

Currently, the photoreceivers part only achieve for simulation by HSPICE and Cadence software. It is just one step closer to implement and fabricate the photoreceiver that monolithically incorporate the CMOS-APDs with pre-amplifier such as TIA, post-amplifier and output buffer in one chip. Transimpedance amplifier is an important component in photoreceiver because it was the first device to convert and amplify the photocurrent after absorption of incident optical light by photodetector. The suitable and effective design of transimpedance amplifier results in high performance of a photoreceivers in term of gain, bandwidth, sensitivity, etc.

After successful design and fabricate the photoreceiver, it is then possible to integrate optical devices such as light sources and optical waveguides in order to realize the optical interconnection. On the other hand, other application such as optoelectronics integrated chip (OEIC) can be achieve too.

This is not a complete list of suggestion. There are many more implementations of the CMOS-APD feasible and numerous combinations of CMOS-APDs and photoreceiver circuitry possible.

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PUBLICATION

[1] Zul Atfyi Fauzan Mohammed Napiah, Ryoichi Gyobu, Takuya Hishiki, Takeo Maruyama and Koichi Iiyama, "Characterizing Silicon Avalanche Photodiode Fabricated by Standard 0.18 um CMOS Process for High-speed Operation," *IEICE Transactions on Electronics*, Vol. E99-C, No. 12 December 2016.

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