International Journal of Science Engineering and Advance Technology, IJSEAT, Vol. 5, Issue 1
ISSN 2321-6905
January -2017

International Journal of Science Engineering and Advance Technology

Urdhva Tiryagbhyam Sutra Multiplier Based 32-Bit MAC Design

[1]Bandaru.Divakar , [2]T.Srinivas
[1]Student, [2]Associate Professor
Aditya College of Engineering, Surampalem A.P. India
bdk403@gmail.com, tirumala.sri1@gmail.com

ABSTRACT: The Vedic Multiplier and the Reversible Logic Gates has Designed and actualized in the increase and Accumulate Unit (MAC) and that is appeared in this paper. A Vedic multiplier is composed by utilizing Urdhava Triyagbhayam sutra and the snake configuration is finished by utilizing reversible rationale entryway. Reversible rationales are likewise the crucial necessity for the developing field of Quantum processing. The Vedic multiplier is utilized for the increase unit in order to decrease halfway items and to get elite and lesser territory .The reversible rationale is utilized to get less power. The MAC is composed in Verilog HDL and the recreation is done in Xilinx 14.2 and blend is done utilizing Xilinx. The chip outline for the proposed MAC is likewise completed.

Keywords—Reversible Logic, Urdhava Triyagbhayam, Quantum Computing, Kogge Stone Adder

I.INTRODUCTION

In the gather viper the past MAC yield and the present yield will included and it comprises of Multiplier unit, one snake unit and both will get be consolidated by an amass unit. The significant uses of Multiply-Accumulate (MAC) unit are chip, rationale units and computerized flag processors, since it decides the speed of the general framework [13]. The effective outlines by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are fundamentally executed by persistent use of increase and expansion, the whole speed and execution can be register by the speed of the expansion and augmentation occurring in the framework. For the most part the postponement, for the most part basic deferral, occurs because of the long duplication prepare and the spread postponement is watched as a result of parallel adders in the expansion organize. The fundamental thought of this paper is examination of zone, speed and different parameters of Conventional MAC unit with the Vedic MAC plan.

II.LITERATURE SURVEY

A. MAC Unit

A duplicating capacity can be done in three ways: halfway item Generation (PPG), incomplete item expansion (PPA), and last routine expansion. The two jug necks that ought to be considered are expanding the speed of MAC are halfway item diminishment and aggregator piece. The 32 bit Mac configuration by utilizing Vedic multiplier and reversible rationale door should be possible in two sections. In the first place, multiplier unit, where a customary multiplier is supplanted by Vedic multiplier utilizing Urdhava Triyagbhayam sutra. Duplication is the essential operation of MAC unit [1]. Control utilization, dispersal, region, speed and inactivity are the real issues in the multiplier unit. In this way, to evade them, we go for quick multipliers in different utilizations of DSP, systems administration, and so forth. There are two noteworthy rule that enhance the speed of the MAC units are decreasing the halfway items and due to that collector weight is getting lessened. The fundamental operational squares in advanced framework in which the multiplier decides the basic way and the postponement. The (log2N + 1) halfway items are created by 2N-1 cross results of various widths for N*N. The halfway items are created by Urdhava sutra is by Criss Cross Method. The greatest number of bits in incomplete items will prompt to Critical way.

The second a portion of MAC is Reversible rationale entryway. In present day VLSI, quick exchanging of signs prompts to more power dissemination. Loss of all of data in the calculations that are not reversible is kT*log2 joules of warmth vitality is created, where k is Boltzmann's consistent and T the supreme temperature at which calculation is performed. Lately, reversible rationale capacities has developed and assumed an indispensable part in a few fields, for example, Optical, Nano, Cryptography, and so forth.

III.DESIGN OF MAC ARCHITECTURE:

- The plan of MAC engineering comprises of 3 sub outlines.
- Design of 32×32 piece Vedic multiplier.
- Design of snake utilizing DKG door reversible rationale.
- Design of gatherer which coordinates both multiplier and snake stages.

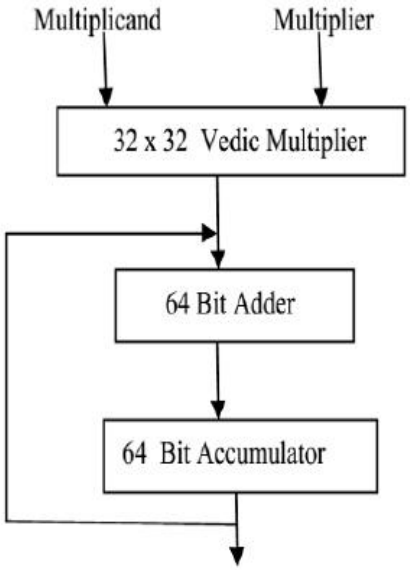


Fig: Modified MAC Architecture.

A.32 x 32 bit Vedic Multiplier:

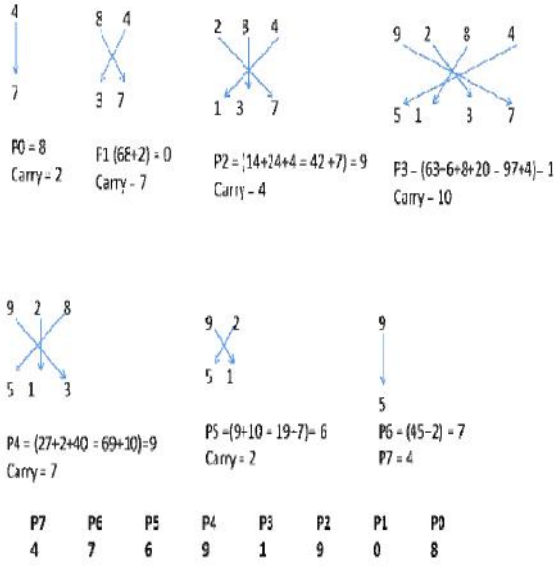
Vedic science is an old arrangement of arithmetic, which was detailed by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). Following an exploration of eight years, he created sixteen scientific formulae from Atharvana Veda[11]. The sutras (adages) secured every single point of Mathematics, for example, Arithmetic, Algebra, Geometry, Trigonometry, differential, vital, and so forth., "Vedic" is gotten from "Veda" which implies the power place of all learning and awesome [2, 3]. The proposed Vedic multiplier depends on the "Urdhava Triyagbhayam" sutra (calculation). These Sutras have been customarily utilized for the increase of two numbers in the decimal number framework.

In this work, we will use comparable methods to tackle the parallel number framework to make the new truism, which will be more perfect for the computerized frameworks. It is a general augmentation recipe relevant to all instances of duplication.

B.Urdhava Triyagbhayam Sutra:

It actually signifies "Vertically and Crosswise". Move operation is a bit much in light of the fact that the fractional item computation will perform it in a solitary stride, which thusly spares time and power. This is the primary preferred standpoint of the Vedic multiplier.

A case for the Urdhva Triyagbhayam sutra is as follows:9284 * 5137



IV.IMPLEMENTATION OF VEDIC MULTIPLIER USING MODEL ARCHITECTURE IN DESIGN:

The accompanying fig. 2 demonstrates the outline of a 16×16 Vedic multiplier utilizing a 8×8 Vedic multiplier and the plan can be actualized utilizing Verilog HDL. Utilizing a 16×16 Vedic multiplier we can plan 32 ×32 Vedic multiplier with convey spare viper as appeared in fig. We have changed the last viper organize with the Kogge stone snake which is more proficient than the Carry spare viper which is appeared in the fig.By utilizing the Vedic multiplier we can accomplish lesser halfway items as the table demonstrates that the multiplier and snake stages for Vedic multiplier for higher piece are lesser when contrasted with the ordinary multiplier. The multiplier configuration has been recreated and combined utilizing Xilinx.

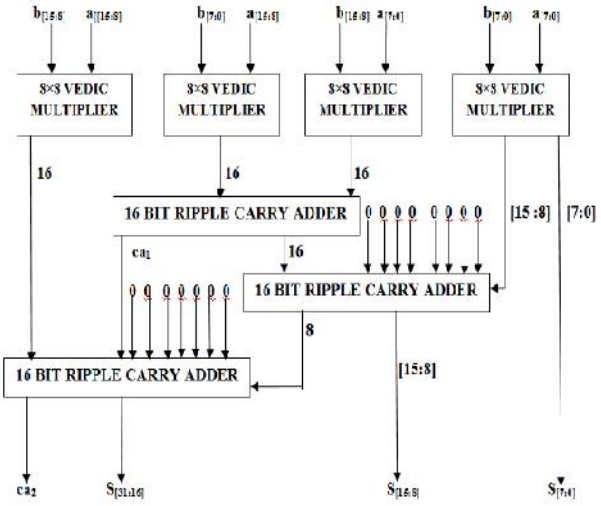


Fig : 16×16 Vedic multiplier using 8×8 Vedic multiplier

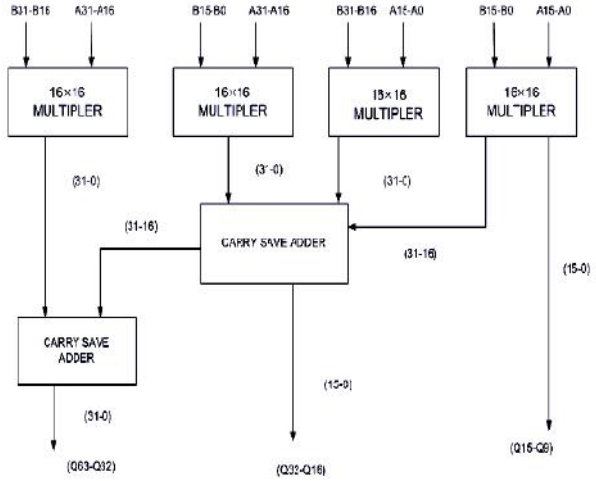


Fig : 32 × 32 Vedic Multiplier with Carry save Adder

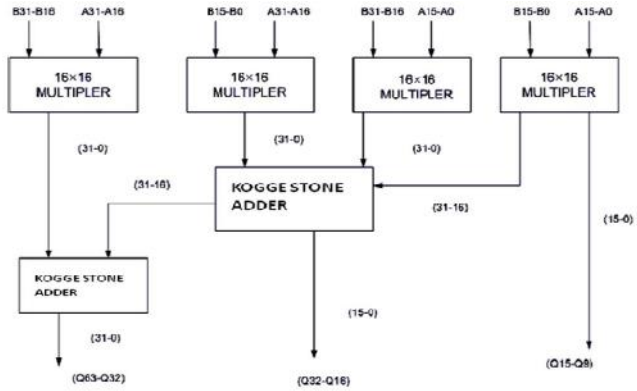


Fig : 32 × 32 Vedic Multiplier with Kogge Stone Adder

IV.KOGGE STONE ADDER:

It's a parallel prefix adder, which is the one of the fastest adder. Carry stages: log2 *n*; The number of cells: n(log2 n-1)+1 ; Maximum fan-out: 2 (extra wiring). So, it will reduce the power consumption as well as the power dissipation.

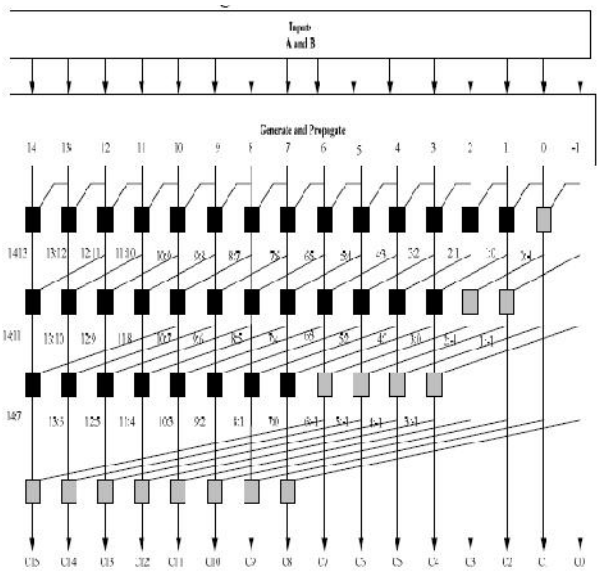


Fig: 16-bit Kogge Stone Adder

V. DESIGN OF ADDER USING REVERSIBLE LOGIC DKG GATE

A. Reversible rationale

Reversible rationale is a remarkable strategy (not the same as other rationale). Loss of data is impractical in here. In this, the quantities of yields are equivalent to the quantity of sources of info.

1. General thought for reversible rationale door

A Boolean capacity is reversible if every incentive in the info set can be mapped with a one of a kind incentive in the yield set. Landauer [18] demonstrated that the use of conventional irreversible circuits prompts to power scattering and Bennet [17] demonstrated that a circuit comprising of just reversible entryways does not disseminate control. In the outline of reversible rationale circuits, the accompanying focuses must be remembered to accomplish a streamlined circuit:

Fan-out is not allowed

Circles or inputs are not allowed
Waste yields must be Minimum
Least postponement
Least quantum cost
Zero vitality dissemination [17]

2. DKG Gate

A 4* 4 reversible DKG entryway [6] that can work independently as a reversible full snake and a reversible full subtractor is demonstrated as follows. On the off chance that info A=0, the DKG entryway acts as a reversible Full viper, and if input A=1 then it acts as a reversible Full subtractor. It has been confirmed that a reversible full-viper circuit requires no less than a few trash yields to make the yield blends one of a kind [5], [6].

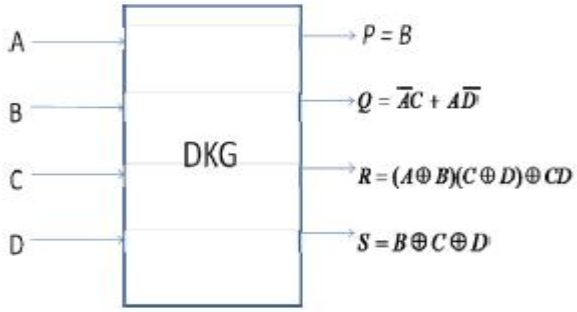


Fig. 6a [6] DKG gate

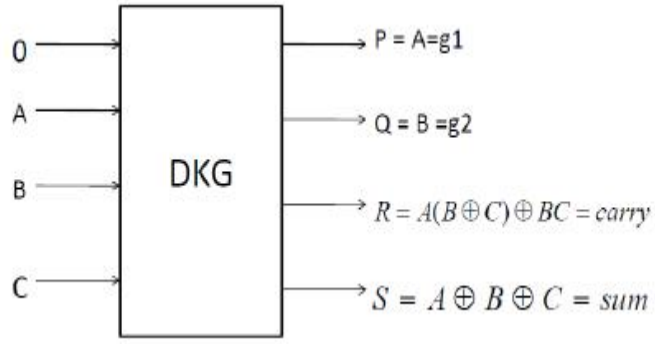


Fig. 6b DKG gate as a Full adder

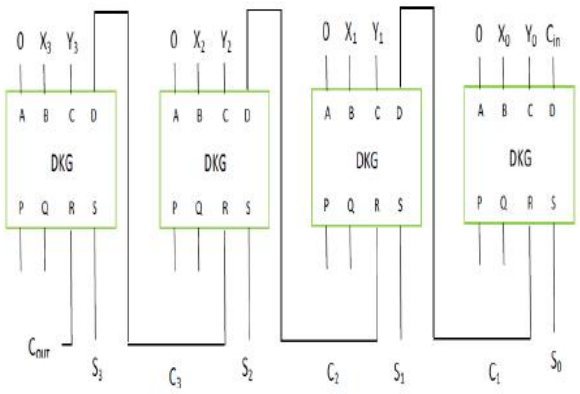


Fig. 6c Parallel adder using DKG gate

VI. ACCUMULATOR STAGE

Aggregator has a critical part in the DSP applications in different ranges and is an extremely essential and basic strategy. The enroll planned in the aggregator is utilized to include the increased numbers. Multiplier, viper and a gatherer are framing the basic establishment for the MAC unit. The traditional MAC unit has a multiplier and multiplicand to do the essential increase and some parallel adders to include the fractional items created in the past stride. To get the last duplication yield we add the halfway item to these outcomes. Vedic Multiplier has advanced to heighten the activity of the MAC Unit. The proposed MAC is contrasted and the ordinary MAC and the outcomes are broke down. The outcomes got utilizing our outline would be wise to execution when contrasted with the pervious MAC plans.

VII.RESULT AND DISCUSSION

The adjusted multiplier utilizing the Kogge Stone Adder is quick and the outline of 32 bit MAC is done in Xilinx. All the amalgamation and reenactment results are performed utilizing Verilog HDL. The union and recreation are performed on Xilinx ISE 14.4. The reenactment results are appeared beneath figures.

Fig.15: RTL schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

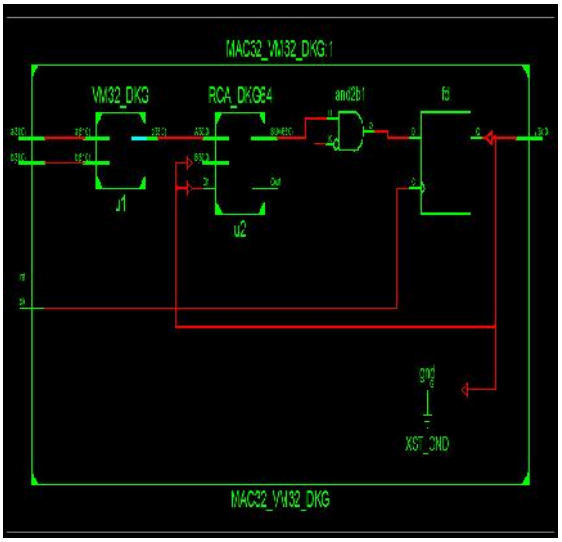


Fig.16: RTL sub schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

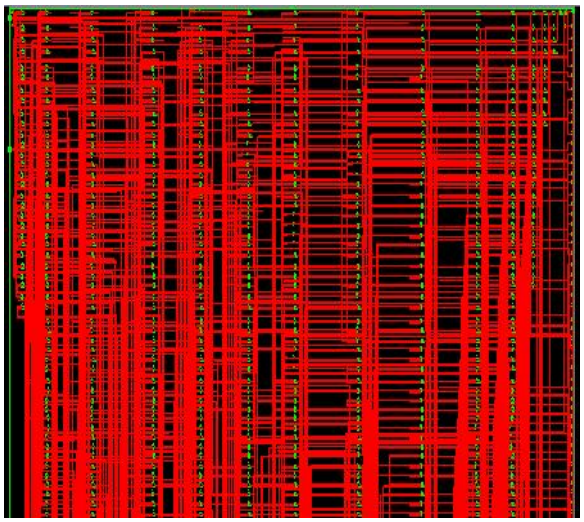


Fig.17: Technology schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

MAC32_VM32_DKG Project Status (07/21/2016 - 16:40:26)			
Project File:	VM_DKG32.xise	Parser Errors:	No Errors
Module Name:	MAC32_VM32_DKG	Implementation State:	Placed and Routed
Target Device:	xc3s500e-4fg320	• Errors:	No Errors
Product Version:	ISE 14.4	• Warnings:	1584 Warnings (1584 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	64	9,312	1%	
Number of 4 input LUTs	3,257	9,312	34%	
Number of occupied Slices	1,771	4,656	38%	
Number of Slices containing only related logic	1,771	1,771	100%	
Number of Slices containing unrelated logic	0	1,771	0%	
Total Number of 4 input LUTs	3,257	9,312	34%	
Number of bonded IOBs	131	232	56%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.61			

Fig.18: Design summary of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

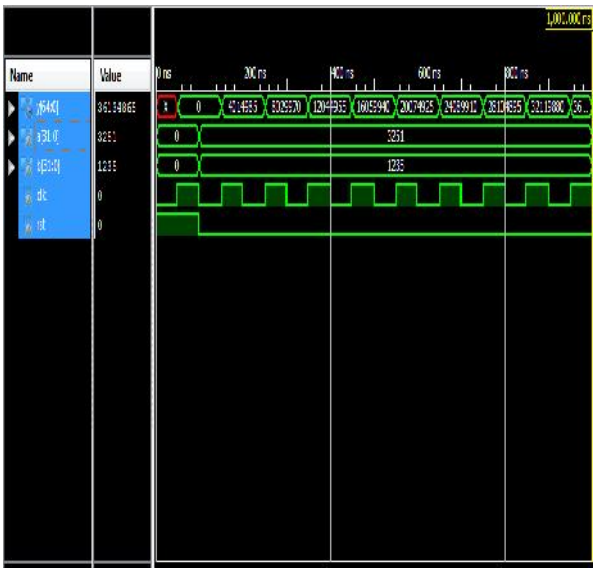


Fig.18: Simulation of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

CONCLUSION AND FUTURE WORK

The outcomes acquired by the plan of Vedic multiplier with 32 bits and reversible rationale are very great. The work displayed depends on 32 – bit MAC unit with Vedic Multipliers. We have composed MAC unit essential building squares and its execution has been broke down for every one of the pieces. Hence, we can state that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible rationale is the best in all perspectives like speed, postponement, territory and intricacy when contrasted with different models which are appeared in table.

Numerous specialists are reconfiguring the structure of MAC unit, which is the fundamental square in various outlines and perspectives particularly utilizing reversible rationale which advances late days. Range Analysis and Correlation straight separating which are the utilizations of change calculation additionally add to the field of correspondence, flag and picture preparing and instrumentation, and some other. Consolidating the Vedic and reversible rationale will prompt to new and proficient accomplishments in creating different fields of Mathematics, science also designing.

REFERENCES

[1] Vaijyanath Kunchigi ,Linganagouda Kulkarni, Subhash Kulkarni 32-bit MAC unit design using Vedic multiplier International Journal of Scientific and Research Publications, Volume3, Issue 2, February 2013

[2] Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, High Speed Energy Efficient ALU design using Vedic multiplication techniques, International Conference on Advances in Computational Tools for Engineering Applications, 2009. ACTEA '09.pp. 600 - 3, Jul 15-17, 2009.
[3] Sree Nivas A and Kayalvizhi N. Article: Implementation of Power Efficient Vedic Multiplier. International Journal of Computer Applications 43(16):21-24, April 2012. Published by Foundation of Computer Science, New York, USA
[4] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, High Speed and Area Efficient Vedic Multiplier, International Conference on Devices, Circuitsand Systems (ICDCS), 2012.
[5] D.P.Vasudevan, P.K.Lala, J.Di and J.P.Parkerson, "Reversiblelogic design with online testability", IEEE Trans. On Instrumentation and Measurement, vol.55., no.2, pp.406-414,
April 2006.
[6] Raghava Garipelly , P.Madhu Kiran , A.Santhosh Kumar A Review on Reversible Logic Gates and their Implementation International Journal of Emerging Technology and Advanced
Engineering Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 3, March 2013.
[7] Wikipedia.org/ mac design
[8] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics, Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, IIT Kharagpur.
[9] Asmita Haveliya, A Novel Design for High Speed Multiplier for Digital Signal Processing Applications (Ancient Indian Vedic mathematics approach), International Journal of Technology and Engineering System (IJTES), Vol.2, No.1, Jan -March, 2011.
[10] Aniruddha Kanhe, Shishir Kumar Das and Ankit Kumar Singh, Design and Implementation of Low Power Multiplier Using Vedic Multiplication Technique, (IJCSC) International Journal of Computer Science and Communication Vol. 3, No. 1, January-June 2012, pp. 131-132 International Journal of Scientific and Research Publications, Volume 3, Issue 2, February 2013 ISSN 2250-315.
[11] www.hinduism.co.za/vedic.htm#Vedic Mathematics.
[12] www.vedicmaths.org/
[13] A. Abdelgawad, Magdy Bayoumi ," High Speed and Area- Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications", IEEE Int. Symp. Circuits Syst. (2007) 3199–3202.
[14] R.Bhaskar, Ganapathi Hegde, P.R.Vaya," An efficient hardware model for RSA Encryption system using Vedic mathematics", International Conference on Communication Technology and
System Design 2011 Procedia Engineering 30 (2012) 124 – 128.
[15] Fatemeh Kashfi, S. Mehdi Fakhraie, Saeed Safari," Designing an ultra-high-speed multiply-accumulate structure", Microelectronics Journal 39 (2008) 1476–1484.
[16] Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, "Vedic mathematics", Motilal Banarsidass Publishers Pvt. Ltd, Delhi, 2009.
[17] C.H. Bennett," Logical reversibility of computation", IBM J. Res. Dev. 17 (1973) 525–532.
[18] R. Landauer, Irreversibility and heat generation in the computational process's, IBM J. Res. Dev. 5 (1961) 183–191.
[19] Ashis Kumer Biswas, Md. Mahmudul Hasan, Ahsan Raja Chowdhury, Hafiz Md. Hasan Babu, "Efficient approaches for designing reversible Binary Coded Decimal adders".