A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces

A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces

Pedro Toledo[1,2,3], Paolo Crovetti[1], Hamilton Klimach[2], Sergio Bampi[2]
[1]Departament of Electronics and Telecommunications (DET), Politecnico di Torino,
[2]Graduate Program in Microelectronics (PGMICRO), Federal University of Rio Grande do Sul,
[3]Corresponding author: pedro.leitecorreia@polito.it

***Abstract*—This paper presents a power-efficient Ultra Low Voltage (ULV) Digital-Based Operational Transconductance Amplifier (DB-OTA), which uses static logic gates and processes digitally the analog input signal. Post-layout simulations in 180nm CMOS technology show that at 300mV supply voltage the circuit consumes just 2nW while driving a capacitive load of 80pF with Total Harmonic Distortion lower than 5% at 100mV input signal swing. The total silicon area is 1,426 μm^2. The maximum energy efficiency supply for the DB-OTA and its scalability to 40nm CMOS technology node are also demonstrated.**

***Index Terms*—Ultra-Low Voltage (ULV), Operational Transconductance Amplifier (OTA), Digital-Based Circuit, Internet of Things (IoT).**

I. Introduction

Ultra-low Voltage (ULV), Ultra-Low-Power (ULP) integrated circuits are necessary in Internet of Things (IoT) nodes to allow energy-autonomous operation from harvesters and/or very small batteries through their whole life [1]. While high energy efficiency is achieved in digital circuits at near-threshold supply voltages (V_{DD}) close to the minimum energy point [2] and by energy-quality scaling [3], the same concepts do not apply to analog interfaces, which are indeed the bottleneck in terms of power, cost and performance [4].

Focusing on Operational Transconductance Amplifiers (OTAs), which are ubiquitous in analog circuits, traditional topologies are power hungry and not amenable to low V_{DD} operation [5], [6], especially due to the degradation of analog performance in nanoscale MOS devices, which are not well suited to analog even at nominal supply.

The above limitations of OTA under low V_{DD} have been addressed at system level and the block level. In the system level approach, the main idea is to either replace or mimic the OTA behavior by different blocks, e.g., ring oscillators [7] or dynamic amplifiers [8]. On the other hand, at block level ULV OTAs using bulk-driven Differential-Pair (DP) [6], internal positive feedback [9] and Common-Mode FeedFoward (CMFF) circuit [10] have been proposed. However, all these solutions are power-hungry and their performance does not improve in aggressively scaled technological nodes.

In this paper, the digital-based differential circuit concept presented in [11] is exploited to design a novel highly energy-efficient ULV OTA, referred to here as Digital-Based Operational Transconductance Amplifier (DB-OTA).

In section II, the circuit operation is briefly reviewed and a design guideline for ULV operation is proposed. Based on the post-layout simulations shown in section III, the DB-OTA just consumes 2nW at $V_{DD} = 300$mV driving a capacitance load (C_{out}) of 80pF with a Total Harmonic Distortion (THD) lower than 5% for 100mV of input signal swing. In the same section III, the DB-OTA scalability is also demonstrated. Finally, in section IV, some concluding remarks are drawn.

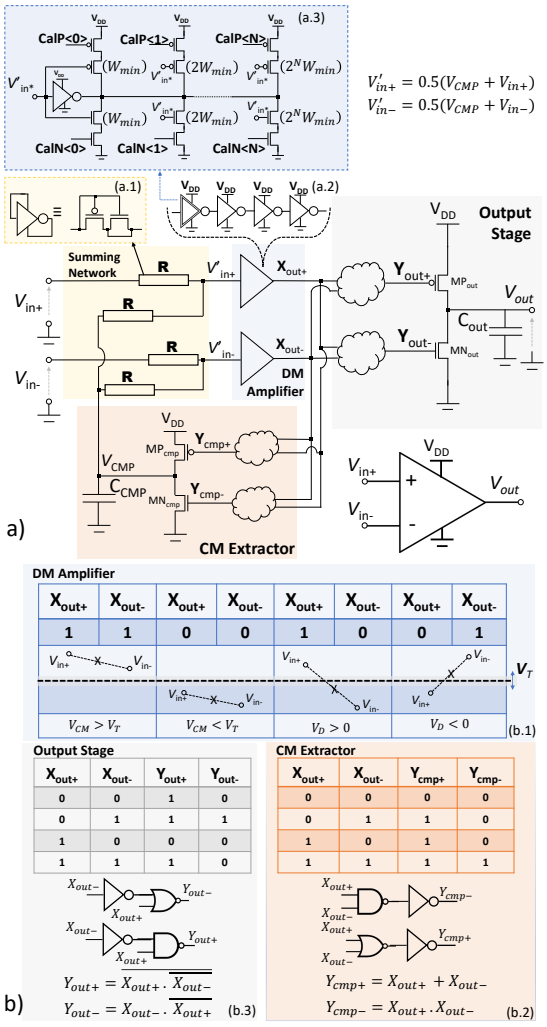

Fig. 1. (a) DB-OTA schematic. N is the number of stages in the calibration inverter chain. (b) Truth tables that rule the DB-OTA operation. V_T is the tripping point of a buffer.

II. ULV DB-OTA Circuit Description and Design

In this section, the operation of a digital-based differential circuit presented in [11] is firstly reviewed and then exploited to design an ULV DB-OTA.

A. Digital-Based Differential Circuit Description

The schematic of the proposed ULV DB-OTA is shown in Fig. 1 (a). The circuit is comprised by the *Differential-Mode (DM) amplifier*, the *Common-Mode (CM) extractor* loop, the *summing network* and the *output stage*, as in [11]. The main goal of this topology is to replace the classical DP stage with digital gates keeping the same functionality, i.e., to amplify the differential input signal $v_{\rm d} = (V_{\rm in+} - V_{\rm in-})$ and to be insensitive to common mode input signal variations $v_{\rm cm} = \frac{(V_{\rm in+}+V_{\rm in-})}{2}$. To reach these goals, the *DM Amplifier*, which is formed by two digital buffers, is used to sense the level of the input voltages w.r.t. the buffers voltage tripping points ($V_{\rm T}$) resulting in four possible logical outputs: $(X_{\rm out+}, X_{\rm out-}) = (0,0),(1,1),(1,0),(0,1)$.

As detailed in Fig. 1 (b.1), when $(X_{\rm out+}, X_{\rm out-}) = (0,1),(1,0)$ the *output stage* is activated and $V_{\rm out}$ is increased/decreased depending on $v_{\rm d}$. Otherwise, when $(X_{\rm out+}, X_{\rm out-}) = (0,0),(1,1)$, the *CM Extractor* is turned on to correct the input CM signal. The truth tables which describe how the *CM Extractor* and the *output stage* work are shown in Fig. 1 (b.2) and (b.3), respectively.

Once it is sensed that the CM input signal must be corrected, the transistor $\rm MN_{cmp}$ ($\rm MP_{cmp}$) is turned on and $C_{\rm CMP}$ is properly discharged (charged) and the generated $V_{\rm CM}$ signal is then subtracted from the input through the *summing network* ($V'_{\rm in+(-)} = 0.5(V_{\rm CMP} + V_{\rm in+(-)})$). On the other hand, after the CM signal compensation, the $v_{\rm d}$ signal can be thus amplified charging or discharging $C_{\rm OUT}$ through the transistors $\rm MP_{out}$ and $\rm MN_{out}$. A detailed analysis of the circuit dynamic can be found in [11].

B. ULV DB-OTA Design

The proposed ULV DB-OTA has been designed in 180nm following digital design criteria. Under this perspective, CMOS static logic is adopted for most the gates in Fig.1. Moreover, as usual in ULP digital design, the power supply voltage is set to the Minimum Energy Point (MEP) [2], which turns out to be about $V_{\rm DD} = 300$mV for the target technology and switching activity.

The strength of the *output stage* is set by considering the maximum capacitive load (80pF in the proposed design) and slew rate requirements, taking into account also that a minimum capacitive load (10pF in the proposed design) is needed in the DB-OTA for low-distortion analog signal reconstruction. The strength of the other gates is consequently designed as cascaded drivers. Minimum-size devices have been used in the *CM extractor* stage and the capacitance $C_{\rm CMP}$ has been set in view of the closed-loop stability requirements [11] and to reduce Total Harmonic Distortion (THD).

Two parts of the circuit deserve a special care due to their analog function, i.e. the *summing network* and the first inverters of the *DM amplifier*: the *summing network* has been implemented using inverter-based pseudo-resistors as voltage dividers. Large area has been adopted in PMOS devices in Fig. 1 (a.1), to achieve a good matching leveraging Pelgrom's law [12].

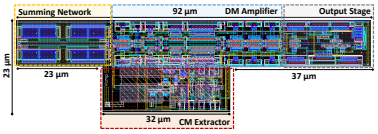

Fig. 2. DB-OTA layout. Total area of 1,426 μm^2.

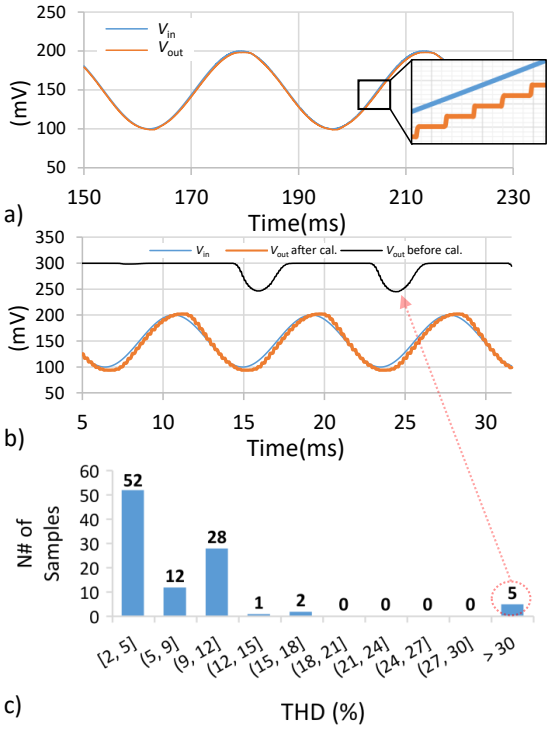

Fig. 3. a) $V_{\rm in}$ and $V_{\rm out}$ for $C_{\rm out} = 80$pF, $V_{\rm amp} = 50$mV and $f_{\rm in} = 30$Hz. b) $V_{\rm in}$, $V_{\rm out}$ before calibration (black) and $V_{\rm out}$ after calibration (red) for $C_{\rm out} = 80$pF, $V_{\rm amp} = 50$mV and $f_{\rm in} = 120$Hz. c) 100 samples MC simulation for DB-OTA THD (%).

For what concerns the *DM amplifier* in Fig. 1 (a.2), mismatch in the buffers $V_{\rm T}$ decides the DB-OTA input offset voltage and it has been mitigated by the calibration network in Fig. 1 (a.3). Such a calibration network includes four auxiliary pull-up (pull-down) branches, having pMOS (nMOS) devices with minimum length and binary weighted minimum width ($W_k = 2^k W_{\rm min}, k = 0\ldots3$) and driven by the same input signal, which can be individually enabled/disabled depending on an 8-bit digital calibration word so that to modify the trip point of the buffer and effectively compensate mismatch. It is worth mentioning that this calibration network is also able to work in low $V_{\rm DD}$.

III. Simulations Results

The proposed DB-OTA has been laid out in 180nm CMOS so that to match the delays of the non-inverting and inverting

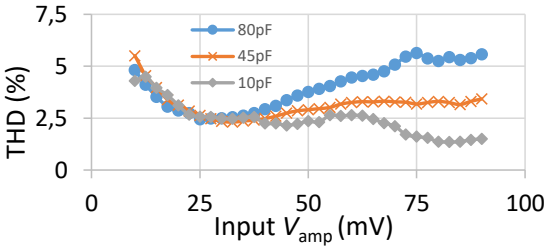

Fig. 4. THD (%) versus V_{amp}

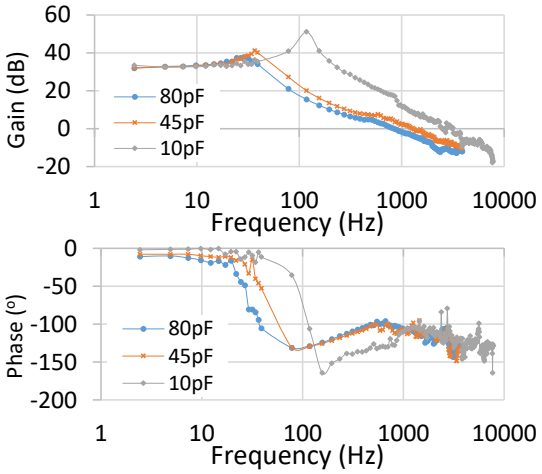

Fig. 5. ULV DB-OTA frequency response.

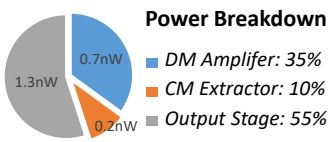

Fig. 6. ULV DB-OTA Power Breakdown

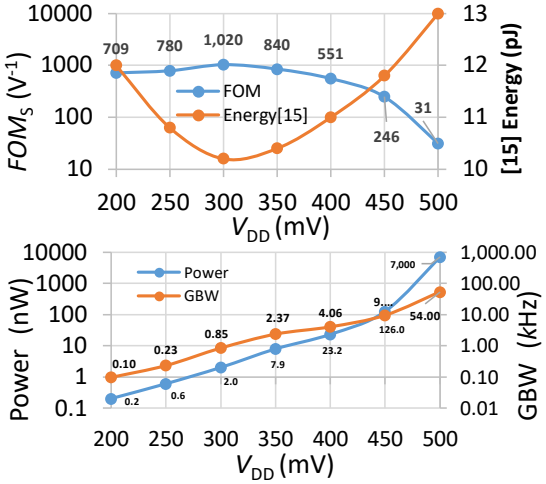

Fig. 7. V_{DD} versus FOM_S, Power and GBW.

signal paths. The layout of the circuit, including the calibration network, occupies just 1,426 μm^2 and it is shown in Fig. 2. The operation and performance of the DB-OTA have been tested by post-layout simulations performed in the voltage follower configuration and is then compared with ULV OTAs presented in recent literature.

A. Post-Layout Simulated Performance

The time-domain input and output waveforms of the proposed DB-OTA at $V_{\rm DD} = 300$mV, with sine wave input at 30Hz frequency, 50mV peak amplitude and $C_{\rm out} = 80$pF capacitive load are reported in Fig.3(a) and reveal the operation of the circuit as an opamp and less than 2% THD and 2nW power consumption. A zoom in the waveform shows the step-wise changes in $v_{\rm out}$ resulting from digital operation. Fig. 4 depicts THD versus $V_{\rm amp}$ for three different $C_{\rm out} = 80, 45, 10$pF keeping $f_{\rm in} = 120$Hz.

1) Frequency Response: The frequency response of the circuit has been tested by time-domain, large-signal simulations, since small signal analysis cannot be adopted in view of the digital operation of the circuit. For this purpose, the DB-OTA has been tested in the voltage follower configuration with 50mV-peak-amplitude sine wave input at different frequencies f_0, and the differential amplification frequency response $A_{\rm d}(f) = \frac{V_{\rm out}(f)}{V_{\rm d}(f)}$ has been estimated in magnitude and phase taking the ratio of the Fast Fourier Transform (FFT) at the fundamental frequency f_0 of the output and of the differential voltage. The DB-OTA frequency response reported in Fig.5 exhibit 35dB DC gain and 0.85, 1.3 and 2.48 kHz Gain Bandwidth Product (GBW) with phase margin 76°, 68.5° and 57° under $C_{\rm out} = 80, 45$ and 10 pF load, respectively.

2) Process Variations and Calibration: The uncalibrated DB-OTA has been tested under process variations for $V_{\rm amp} = 50$mV, $C_{\rm out} = 80$pF and $f_{\rm in} = 120$Hz by Montecarlo (MC) simulations performed on 100 samples and the output THD has been considered to evaluate the signal quality degradation. The histogram of the output THD reported in Fig.3(c) reveals a noticeable number of samples exceeding 10% THD due to the spread of the trip voltages of the *DM amplifier* $\Delta V_{\rm T}$, which leads to high input offset voltage and results in the output saturation, as shown in Fig.3(b). From the same figure, however, the offset can be completely compensated by the proposed calibration network turning the DB-OTA back to work properly.

3) Power Consumption and Figure of Merit (FOM): For all $C_{\rm out}$ values here explored the power consumption was found to be always lower than 2 nW. Fig. 6 shows the DB-OTA power breakdown for $C_{\rm out}$ =80pF, at which it can be seen that 45% of the total power is used to process the input signal while the rest is used to charge $C_{\rm out}$. The energy efficiency of the proposed DB-OTA under low $V_{\rm DD}$ has been also analyzed in Fig. 7 where the power, the GBW and the small signal figure of merit $FOM_{\rm S} = 100\, GBW\, C_{\rm out}(I_{\rm DD})^{-1}$ are plotted at different $V_{\rm DD}$. It is interesting to note that there is a peak for $FOM_{\rm S}$ around $V_{DD} = 300$mV, which coincides with the energy-efficient $V_{\rm DD}$ optimum in digital sub- or near-threshold designs, regarding their most energy efficient $V_{\rm DD}$, i.e., their Minimum Energy

TABLE I
COMPARISON WITH STATE-OF-THE-ART ULTRA-LOW-VOLTAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Performance	[10]$^{+}$	[6]$^{+}$	[13]$^{+}$	[14]$^{+}$	[9]*	[5]* MC-OTA	[5]* FFC-OTA	**This work***	Unit
Technology	65	130	180	350	65	130	130	180	nm
Supply Voltage	0.35	0.25	0.5	0.6	0.3	0.3	0.3	0.3	V
DC Gain	43	60	52	69	60	46.2	49.8	35	dB
GBW	3600	1.88	1,200	11.4	70	2,450	9,100	0.85	kHz
Slew Rate	5600	0.7	2,890	14.6	25	2,400	3,800	0.5	$\frac{V}{ms}$
THD	0.6	0.2	1	0.08	-	-	-	3	%
Phase Margin	56	52.5	-	65	53	52	76	76	^{o}
C_{out}	3	15	20	15	5	2	2	**80**	pF
Power	17,000	18	110,000	550	51	1,800	1,800	**2**	nW
Dia Area	5,000	83,000	26,000	60,000	3,000	-	-	**1,426**	μm^2
FOM_S	19	29	0.11	0.18	2.05	81	303	**1020**	V^{-1}
FOM_L	34.6	14.6	26.27	23.9	73.4	80	140	**600**	-

$^{+}$experimental; *simulation;

Point (MEP). To illustrate, in Fig. 7 the notch filter MEP designed in [15] is also plotted. This result is expected since the DB-OTA processes the analog input information digitally.

B. Comparison with the State of the Art

Based on the post-layout simulation, compared to ULV OTAs proposed in recent literature, whose performance is summarized in Tab. I, the ULV DB-OTA presented here is able to drive the highest C_{out} (x4 lager than [13]) at the lowest power consumption (x9 lower than [6]) and shows itself as the most power-efficient topology for CMOS technology considering FOM_S as a benchmark (x3.35 lager than [5] FFC-OTA). The comparison in terms of both FOM_S and FOM_L is also illustrated in Fig. 8 including the performance of the proposed circuit samples after calibration and reveals that state-of-art performance is achieved even considering process variations. Moreover, the results of preliminary transistor-level simulations performed on the circuit ported to 40nm CMOS are also shown in Fig.8, demonstrating a further improved performance in finer technology, as expected for digital circuits and as not observed in traditional analog OTAs.

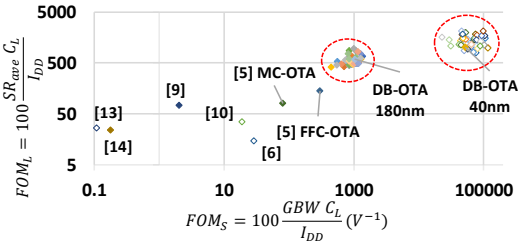

Fig. 8. State-of-art plot for ULV OTA.

IV. CONCLUSION

By processing the analog input signal digitally with static logic gates, the ULV DB-OTA presented here has achieved at $V_{DD} = 300\,\text{mV}$ a $FOM_S = 1020\,\text{V}^{-1}$ consuming only 2 nW and 1,426 μm^2 of silicon area. The DB-OTA maximum energy-efficient point has been demonstrated as well as its scalability. Through this implementation, this work moves forward against the common statement which states that, in general, analog integrated circuits do not take advantage of CMOS technology scaling.

REFERENCES

1 Alioto, M., *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, 1st ed. Springer, 2017.

2 Pinckney, N., Blaauw, D., and Sylvester, D., "Low-Power Near-Threshold Design: Techniques to Improve Energy Efficiency," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 49–57, Spring 2015.

3 Dennard, R. H., "Past Progress and Future Challenges in LSI Technology: From DRAM and Scaling to Ultra-Low-Power CMOS," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 29–38, Spring 2015.

4 Crovetti, P. S., Musolino, F., Aiello, O., Toledo, P., and Rubino, R., "breaking the boundaries between analogue and digital," *Electronics Letters*, vol. 55, no. 12, pp. 672–673, 2019.

5 Lv, L., Zhou, X., Qiao, Z., and Li, Q., "Inverter-Based Subthreshold Amplifier Techniques and Their Application in 0.3-V ΔΣ-Modulators," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1436–1445, May 2019.

6 Ferreira, L. H. C. and Sonkusale, S. R., "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Tran. Circuits Syst. I: Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, June 2014.

7 Drost, B., Talegaonkar, M., and Hanumolu, P. K., "Analog Filter Design Using Ring Oscillator Integrators," *IEEE J. of Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec 2012.

8 Lim, Y. and Flynn, M. P., "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," *IEEE J. of Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct 2015.

9 Veldandi, H. and Shaik, R. A., "A 0.3-V Pseudo-Differential Bulk-Input OTA for Low-Frequency Applications," *Circuits, Systems, and Signal Processing*, vol. 37, no. 12, pp. 5199–5221, Dec 2018.

10 Abdelfattah, O., Roberts, G. W., Shih, I., and Shih, Y., "An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA with Rail-to-Rail Input Range," *IEEE Tran. Circuits Syst. I: Reg. Papers*, vol. 62, no. 10, pp. 2380–2390, Oct 2015.

11 Crovetti, P. S., "A Digital-Based Analog Differential Circuit," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 12, pp. 3107–3116, Dec 2013.

12 Galup-Montoro, C., Schneider, M. C., Klimach, H., and Arnaud, A., "A Compact Model of MOSFET Mismatch for Circuit Design," *IEEE J. of Solid-State Circuits*, vol. 40, no. 8, pp. 1649–1657, Aug 2005.

13 Chatterjee, S., Tsividis, Y., and Kinget, P., "0.5-V Analog Circuit Techniques and their application in OTA and filter design," *IEEE J. of Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec 2005.

14 Ferreira, L. H. C., Pimenta, T. C., and Moreno, R. L., "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 54, no. 10, pp. 843–847, Oct 2007.

15 Rosa, A. L. R., Soares, L. B., Stangherlin, K. H., and Bampi, S., "Designing CMOS for Near-Threshold Minimum-Energy Operation and Extremely Wide V-F Scaling," in *2015 28th Symposium on Integrated Circuits and Systems Design (SBCCI)*, Aug 2015, pp. 1–6.