Fully Synthesizable Low-Area Digital-to-Analog Converter With Graceful Degradation and Dynamic Power-Resolution Scaling

Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling

Orazio Aiello, *Member, IEEE,* Paolo Stefano Crovetti, *Member, IEEE,* Massimo Alioto, *Fellow, IEEE*

***Abstract*— In this paper, a fully synthesizable digital-to-analog converter (DAC) is proposed. Based on a digital standard cell approach, the proposed DAC allows very low design effort, enables digital-like shrinkage across CMOS generations, low area at down-scaled technologies, and operation down to near-threshold voltages. The proposed DAC can operate at supply voltages that are significantly lower and/or at clock frequencies that are significantly greater than the intended design point, at the expense of moderate resolution degradation. In a 12-bit 40-nm testchip, graceful degradation of 0.3bit/100mV is achieved when V_{DD} is over-scaled down to 0.8V, and 1.4bit/100mV when further scaled down to 0.6V.**

The proposed DAC enables dynamic power-resolution tradeoff with 3X (2X) power saving for 1-bit resolution degradation at iso-sample rate (iso-resolution). A 12-bit DAC testchip designed with a fully automated standard cell flow in 40nm consumes 55µW at 27kS/s (9.1µW at 13.5kS/s) at a compact area of 500µm^2 and low voltage of 0.55V.

***Index Terms*— Digital-to-analog converter (DAC), fully synthesizable, graceful degradation, power-resolution scaling**

I. INTRODUCTION

ENERGY-AUTONOMOUS systems for distributed sensing and data acquisition impose stringent constraints on cost, size and power for all on-chip sub-systems [1]-[6]. As main focus of this paper, digital-to-analog converters (DACs) are no exception, as building blocks for sensor readout, on-chip tuning/calibration, reference generation, building blocks for analog-to-digital conversion, audio processing, threshold generation for sensor event detection [7]-[17]. The low-cost requirement demands low design effort, small area, digital-like shrinkage across CMOS generations, design/technology portability, while requiring relatively low bandwidths [7].

Although conventional single-bit sigma-delta (ΣΔ) DACs and pulse-width modulation (PWM) DACs are fully digital, they are not attractive in tightly area- and power-constrained systems. Indeed, they demand power-hungry high-order ΣΔ modulators and digital interpolators at high oversampling clock rates [18]. Also, PWM DACs require area-hungry reconstruction filters with large time constant to suppress image frequencies [18]-[20]. In view of these limits of pure ΣΔ and PWM fully-digital DACs, state-of-the-art low-frequency DACs are mostly based on hybrid architectures, such as high-order multi-bit ΣΔ noise shaper with low (e.g., 32-64X) oversampling ratio and an analog DAC (e.g., current-steering, resistive string) [7]-[14]. Compared to fully-digital DACs, the presence of the analog DAC increases the design effort and limits voltage scaling, being the minimum voltage $V_{DD,min}$ in the 1.8-3.3V range (with few exceptions at 1.2V [21], and 0.8V [12]).

To address the above challenges, the Dyadic Digital Pulse Modulation (DDPM) was recently proposed in [22] by one of the authors, as a low-complexity bitstream generation method that can be used for D/A conversion. The DDPM modulation moves most of the energy of image spectral components to much higher frequencies than PWM, reducing the area of the reconstruction filter by 2^N, being N the resolution [22]. The DDPM modulation does not require interpolation, and has no stability issues thanks to its open-loop architecture.

Existing DACs cannot meet the constraints imposed by tightly area- and power-constrained systems, and do not address the related challenges in terms of resiliency, power-resolution scalability, low-voltage operation, area efficiency and design effort. DAC resiliency against clock frequency and voltage variations is needed to replace power-hungry highly-stable clocks (e.g., quartz crystal) by much less accurate ultra-low power oscillators [2], [5]. Similarly, resiliency against voltage variations permits to withstand large fluctuations in the harvested power and in the voltage of near-exhausted batteries [16], [23], [24], while mitigating or eliminating the need for accurate voltage regulation. Unfortunately, conventional DACs suffer from catastrophic failure when the rated clock frequency $f_{\max}$ is exceeded, or V_{DD} falls below the minimum voltage $V_{DD,min}$ (see Fig. 1). Indeed, operation beyond $f_{\max}$ causes timing violations in digital blocks, and exceeds the bandwidth and the slew rate specifications in analog circuits. Similarly, operation below $V_{DD,min}$ causes timing failures in digital circuits at a given frequency, and pushes transistors out of the intended operating region in analog circuitry. Graceful

Manuscript received Aug. 23, 2018.

Orazio Aiello is with ECE – National University of Singapore (email: *orazio.aiello@nus.edu.sg*), and Politecnico di Torino. Paolo Crovetti is with Politecnico di Torino (email: *paolo.crovetti@polito.it*). Massimo Alioto is with ECE – National University of Singapore (email: *massimo.alioto@nus.edu.sg*).

degradation under V_{DD} and $f_{\max}$ over-scaling has been extensively demonstrated in processors [25]-[26], GPUs [27], digital signal processing [28]-[31], memories [32]-[34], and Networks on Chip [35]. To the best of the authors' knowledge, graceful degradation in DACs was not explored to date. As other limitations, existing DAC architectures do not explicitly allow dynamic power-resolution tradeoff, as opposed to ADCs [3], [36]. Also, low voltage operation down to near-threshold is not allowed in existing DACs [7]-[14], [21].

In this paper, a fully synthesizable Nyquist-rate DAC architecture with graceful resolution degradation at reduced supply and/or increased frequency, and dynamic power-resolution scaling is presented. Its fully-automated standard cell design substantially reduces the design effort and the area compared to conventional analog or hybrid designs, enabling digital-like shrinkage across CMOS generations, low-voltage operation and design/technology portability.

The paper is organized as follows. In Section 0, the basic principle is introduced. A gracefully degradable and power-resolution scalable architecture is described in Section III. Section IV details the testchip design. Measurement results are reported in Section V. Conclusions are drawn in Section VI.

II. Digital-to-Analog Conversion Based on Dyadic Digital Pulse Modulation

The proposed DAC is based on the Dyadic Digital Pulse Modulation (DDPM) [22]. Its N-bit input is an integer number D_{in} in binary representation $(b_{N-1}b_{N-2}\dots 0)$

$$D_{in} = \sum_{i=0}^{N-1} b_i\, 2^i \quad b_i \in \{0,1\}, \tag{1}$$

Which is uniquely associated to a 2^N-bit DDPM sequence $\Sigma_n = [S_N, 0]$, being S_N a bit sequence that is recursively defined as

$$S_i = [S_{i-1}, b_{N-i}, S_{i-1}] \quad \text{for } i = 1 \dots N. \tag{2}$$

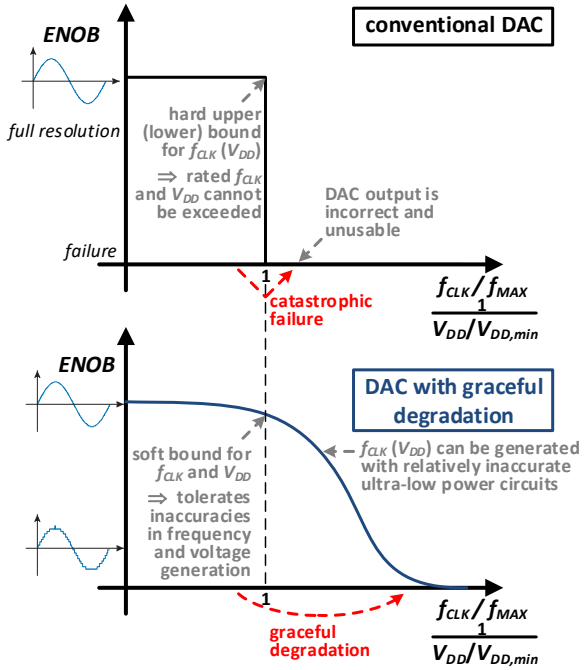

Fig. 1. Catastrophic vs. graceful degradation in digital-to-analog converters.

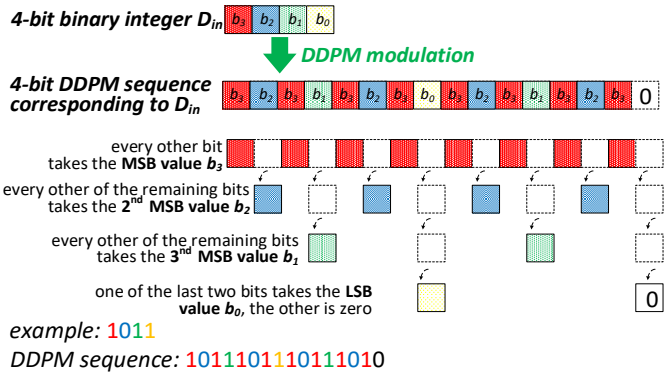

Fig. 2. Example of 4-bit Dyadic Digital Pulse Modulation (DDPM) and related bit sequence associated with a generic integer $D_{in} = b_3b_2b_1b_0$.

In (2), the symbol [,] indicates the bit string concatenation, and S_0 is a void string. As exemplified in Fig. 2, every other bit in the 2^N-bit DDPM sequence takes the value of the most significant bit (MSB) of D_{in} (i.e., DDPM bits occupying odd-numbered positions are assigned to b_{N-1}, e.g. 1, 3, 5…). In the remaining bits, every other bit takes the value of b_{N-2}. The same assignment is recursively applied until two bits are left, of which the former is assigned to the least significant bit b_0 (LSB) of D_{in}, and the latter is forced to zero.

From the above definition, the generic binary digit b_i of D_{in} is contained in the DDPM sequence 2^i times. Hence, each digital b_i contributes to the DDPM sequence with a number 2^i of 1's, if $b_i = 1$ (no 1's, if $b_i = 0$). Thus, the DDPM sequence contains a number $n_{1,DDPM}$ of 1's that is given by $\sum_{i=0}^{N-1} b_i\, 2^i$ (i.e., it is equal to the integer D_{in} itself), and a number of 0's given by $n_{0,DDPM} = 2^N - \sum_{i=0}^{N-1} b_i\, 2^i$. When the DDPM sequence is generated by CMOS logic (i.e., logic levels 0 and V_{DD}) at the clock rate $f_{\text{clk}} = 1/T_{\text{clk}}$, the time-averaged value $V_{out,DC}$ (i.e., the DC value) of the DDPM sequence over a period $T_{\text{sample}} = 2^N T_{\text{clk}}$, is proportional to $n_{1,DDPM}$ and V_{DD}, yielding

$$V_{out,DC} = \frac{V_{DD} \cdot n_{1,DDPM}}{n_{1,DDPM} + n_{0,DDPM}} = V_{DD}\, \frac{\sum_{i=0}^{N-1} b_i 2^i}{2^N}. \tag{3}$$

From (3), the DC voltage of a DDPM sequence generated by CMOS logic is equal to the output voltage of a Nyquist-rate N-bit DAC with sample rate $f_{\text{sample}} = f_{\text{clk}}/2^N$ [8]. The DC voltage $V_{out,DC}$ is extracted from the DDPM sequence by a simple low-pass filter, as in Fig. 3.

The first-order low-pass filter in Fig. 3 represents the reconstruction filter that is invariably cascaded to any DAC. Based on the spectral characteristics of DDPM modulation, its time constant RC is set to make the filter cut-off frequency f_c approximately equal to $f_{sample}/\sqrt{3}$ [22]. This choice suppresses higher-frequency components of the DDPM sequence, yielding an output equivalent to a Nyquist-rate zero-order-hold (ZOH) DAC. The required resistor and capacitor values are typically well aligned with the range of values that can be reasonably integrated on chip. As an example, for f_{sample} in the 100kHz range, the above requirement is met by an RC filter with a capacitor in the 10pF range, and a resistor in the 100kΩ range. Also, the DDPM DAC filter cut-off frequency is 2^N higher than a PWM DAC, thus leading to a substantial

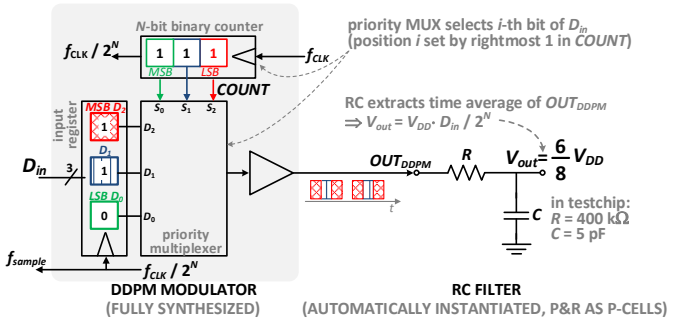

Fig. 3. DDPM DAC architecture, comprising a digital block generating the DDPM sequence and a 1st-order RC filter extracting its DC value.

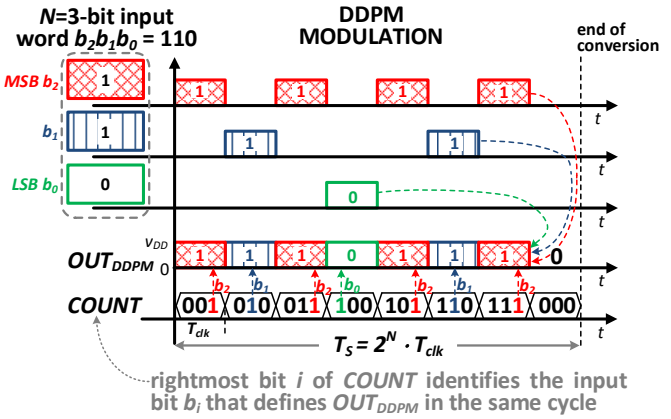

Fig. 4. Example of 3-bit DDPM modulation and analysis of the clock cycle count *COUNT* during a DAC conversion.

area advantage. A detailed spectral analysis and comparison with PWM DACs is presented in the Appendix. DDPM conversion also eliminates the area- and power- hungry digital interpolation for upsampling, compared to ΣΔ DACs [22].

The DDPM modulator in Fig. 3 can be implemented by a priority multiplexer (MUX), whose selection inputs are generated by a modulo-2^N binary counter. This can be seen by analyzing the binary count $COUNT$ of the clock cycle during a conversion. From Fig. 4, $COUNT$ turns out to have its rightmost 1 in the bit position i identifying the input bit b_i that defining the DDPM digital output in the same cycle (with i=0…$N-1$). In the example in Fig. 4, $COUNT = 001$ in the first cycle, whose rightmost bit occurs at position $i = 2$ corresponding to the input bit b_2, which indeed defines OUT_{DDPM} in the same cycle (highlighted in red). In the next cycle, $COUNT$ is 010, whose rightmost bit occurs at position $i = 1$ corresponding to the input bit b_1, which again defines OUT_{DDPM} in the same cycle, and so on. Thus, the DDPM output can be generated by selecting b_i among the input bits through a priority multiplexer driven by a counter, as in Fig. 3.

The DAC architecture in Fig. 3 can be designed with automated standard cell-based design flows at low design effort. As side benefit, this architecture includes only a passive RC filter, eliminating the stringent voltage limitation $V_{DD,min}$ that is otherwise imposed by analog active circuitry.

The above properties of the DDPM modulation do not provide any guarantee of graceful degradation, when V_{DD} is scaled below (f_{clk} is scaled above) the rated value. Indeed, catastrophic degradation in the DAC output generally occurs when voltage/frequency over-scaling determines timing violations in the MSBs first[1], rather the LSBs. Indeed, such violations in the MSB cause errors with the largest weight of 2^{N-1}, as opposed to the weight of 1 in the LSB. Hence, graceful degradation can be achieved by architecting the DDPM modulator in Fig. 3 so that over-scaling triggers timing failures in LSBs first rather than MSBs, as discussed in Section III.

III. A Novel DDPM DAC Architecture with Graceful Degradation and Power-Resolution Tradeoff

A. DDPM Modulator Architecture for Graceful Degradation

As observed in Section II, the critical path of the priority MUX in Fig. 3 needs to be associated with the LSB rather than the MSB of the DDPM output. The next most critical path has to be associated with the bit position next to the LSB, and so on, until the fastest path is associated with the MSB. To this aim, the priority MUX must be arranged as a series of binary decisions starting from the MSB and ending at the LSB, as discussed below.

Since every other bit of OUT_{DDPM} is assigned to the input MSB b_{N-1}, such a sequence can be generated by a MUX, whose selection signal is driven by a toggle flip-flop (T-FF), both highlighted in red in Fig. 5. The MUX allows the alternate selection of either the MSB b_{N-1} in odd-numbered cycles, or another proper digital signal X_{N-1} in even-numbered cycles, where X_{N-1} depends on the remaining input bits $b_{N-2}…b_0$. In even-numbered cycles, the signal X_{N-1} should alternatively take the value of b_{N-2} and of X_{N-2}, as obtained by inserting a MUX with inputs b_{N-2} and X_{N-2}, where X_{N-2} depends on $b_{N-3}…b_0$. Again, the selection signal is generated by a T-FF (highlighted in blue in Fig. 5). Recursively, a MUX is added for each digit b_i of the input, thus leading to N cascaded MUXes in total as shown in Fig. 5. The alternate selection for each digit is assured by the corresponding T-FF driven by the T-FF associated with the immediately more significant digit. The last MUX is fed by the input LSB input and a logical zero, as expected from Fig. 2.

The recursive DDPM architecture in Fig. 5 comprises only N MUXes and T-FFs, leading to a circuit complexity that is linear with the resolution. Interestingly, in the modulator architecture in Fig. 5, the counter in Fig. 3 is implemented by the cascaded T-FFs at no cost. When grouped together, the MUXes in Fig. 5 are equivalent to an N-input priority MUX. Accordingly, the DDPM modulator architecture in Fig. 5 is functionally equivalent to the general architecture in Fig. 3.

The architecture in Fig. 5 enables graceful resolution degradation at reduced V_{DD} and/or increased f_{CLK}. From Fig. 5, the maximum operating frequency $f_{max} = 1/T_{\text{CLK,min}}$ depends on the bit position in the input data as in the following ($T_{\text{CK,min}}$ is the minimum clock cycle preventing setup time violations).

[1] Timing violations typically occur in MSBs first in mainstream architectures of VLSI arithmetic operators (e.g., adders, multipliers, comparators), as they are invariably architected to make the critical path pass through the MSBs.

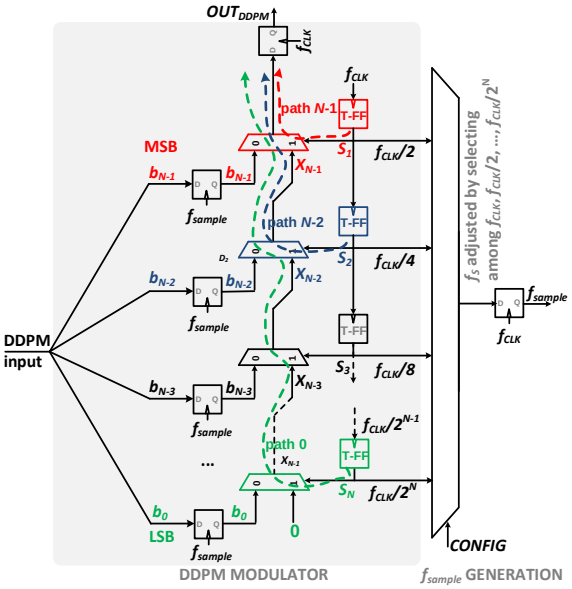

Fig. 5. Gate-level description of the proposed DDPM modulator with graceful degradation. The longest (most critical) paths affect the propagation of the LSBs towards the output, rather than the MSBs.

The critical path associated with the selection of the MSB b_{N-1} is highlighted in red in Fig. 5. From this figure, the minimum clock cycle $T_{CLK,min}$ of this path is set by the sum of the clock-to-Q delay $\tau_{\mathrm{CK-Q,TFF}}$ of the launching T-FF in red, the subsequent MUX delay τ_{MUX}, and the setup time t_{SETUP} of the capturing flip-flop generating the output. Similarly, the critical path associated with the selection of the less significant position b_{N-2} is longer (blue, in Fig. 5). The minimum clock cycle $T_{\mathrm{CLK,min}}$ of this path is set by the sum of the clock-to-Q delay $\tau_{\mathrm{CK-Q,TFF}}$ of the launching T-FF in blue, two subsequent MUX delays τ_{MUX} and the setup time t_{SETUP} of the capturing flip-flop. For less significant input bit positions, $T_{\mathrm{CLK,min}}$ progressively increases by adding further MUX delays, and is maximum for the LSB b_0 (i.e., $T_{\mathrm{CLK,min}} = \tau_{\mathrm{CK-Q,TFF}} + N \cdot \tau_{MUX} + t_{SETUP}$). In general, the minimum clock cycle associated with digit b_i is

$$T_{CLK,min}(i) = \tau_{CK-Q,TFF} + (N-i) \cdot \tau_{MUX} + t_{SETUP}, \quad (4)$$

which monotonically decreases when moving towards more significant bits. Accordingly, the adoption of frequencies beyond (voltages below) the rated frequency f_{max} (minimum voltage $V_{DD,min}$) leads to timing violations that start appearing in the LSBs first (green path in Fig. 5). Further frequency increase (voltage decrease) determines the violation of the immediately shorter paths. Those are associated with progressively more significant bit position, while the timing constraint in (4) is fully met for more significant bits, thus gracefully degrading the resolution as shown in Fig. 1.

B. DDPM Architecture for Power-Resolution Scalability

As additional novel capability, the above DDPM modulator architecture allows for dynamic management of the power-resolution tradeoff, as a lever to reduce power whenever lower resolution is acceptable for the intended application, or the task being executed [3], [36]. To this aim, observe that a 2^N-bit DDPM sequence associated to an input having the last h LSBs equal to zero can be broken into 2^h contiguous 2^{N-h}-bit identical sub-sequences, each being equal to the 2^{N-h}-bit DDPM sequence associated to the same input (see Fig. 6). Hence, when taken as an independent output, such 2^{N-h}-bit subsequence is equal to the DDPM output with resolution scaled down to $(N-h)$ bits, and sample rate increased by 2^h times. Accordingly, an N-bit DDPM modulator with h input LSBs being forced to zero, and the sample rate being increased by a factor of 2^h, can be used as an $(N-h)$-bit DDPM modulator, without any further modification in Fig. 5.

The proposed DDPM architecture can be dynamically reconfigured to operate at any resolution from N down to 1 bit, by simply varying h from 0 to $N-1$. When h is increased, the 2^{N-h} sequence associated with the corresponding sample is shorter than the original 2^N-bit sequence by a factor of 2^h, thus reducing the energy per conversion. Also, to maintain the same sample rate and hence the time taken by the conversion, the clock frequency needs to be reduced by the same factor. In this case, the DAC enables dynamic power-resolution tradeoff at constant sample rate by adjusting h. The power is reduced due to the lower f_{CLK} and the lower energy per conversion, due to the reduced number of cycles per conversion.

As an alternative tradeoff, the clock frequency reduction by 2^h can be accompanied by a sample rate reduction by the same factor, thus again saving power. In turn, the simultaneous reduction in clock frequency and sample rate by 2^h maintains the resolution constant[2] at N bits. In this case, the power consumption is traded off with the sample rate, while keeping the resolution constant. The above clock frequency down-scaling is achieved by adding the multiplexer in Fig. 5 (right-hand side), whose selection signal $CONFIG$ sets the desired down-scaled frequency. Indeed, the cascaded T-FFs effectively implement a frequency divider with input frequency f_{CLK}, output frequency $f_{\mathrm{CLK}}/2$ at the output of the first T-FF (red in Fig. 5), $f_{\mathrm{CLK}}/4$ at the second, and so on. The above mentioned

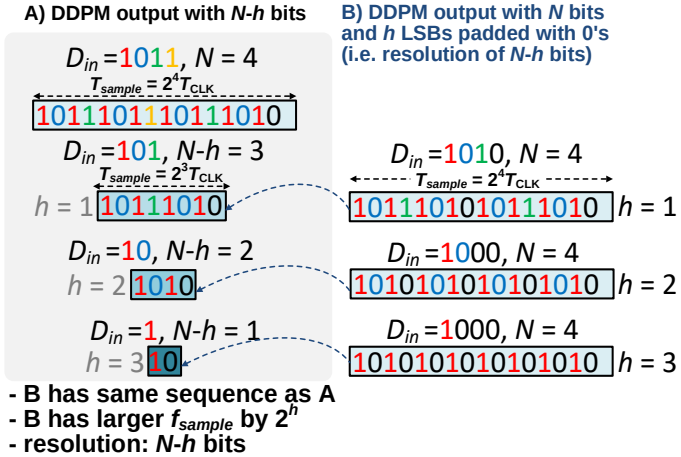

Fig. 6. Example showing that an $(N-h)$-bit DDPM modulator (left side) is equivalent to a 2^N-bit DDPM modulator with h LSBs padded with 0's and T_{sample} reduced by 2^h (right side).

[2] Indeed, the resolution is dictated by the number of clock cycles per conversion, i.e. the ratio of the clock frequency and the sample rate.

linear complexity potentially makes resolution highly scalable, as opposed to the exponential area increase in DAC architectures relying on binary-sized elements. The resolution is hence limited by noise and non-idealities in the shape of the digital pulses, as will be discussed in the next section.

IV. Testchip Design

A testchip implementing a 12-bit DAC based on the proposed architecture was designed with a fully automated digital flow in 40nm. The digital core power domain includes the circuits generating and selecting the divided frequencies in Fig. 5. The micrograph of the test chip is reported in Fig. 7 and its block diagram is shown in Fig. 8. The timing constraints adopted to design the DAC are set to operate at full resolution at nominal voltage, and up to a clock frequency $f_{\max}$=225MHz, which corresponds to a sample rate of $f_{\max}/2^N$=55kS/s for N=12 bits. An on-chip configurable ring oscillator generates the clock.

The first-order reconstruction filter in Fig. 3 was designed by using a 5-pF metal-insulator-metal on-chip capacitor using the available 6 metal layers, and a high-resistivity poly resistor with a resistance of 400kΩ. The DDPM modulator in Fig. 3 is very compact and occupies 500μm^2, as expected from its digital nature and intrinsic simplicity from Fig. 5. The reconstruction filter occupies a silicon area of 1,500μm^2, and its area could be halved by using the entire 10-metal stack, and further reduced by attaching a capacitive load. The resistor and the capacitor were automatically instantiated and routed.

Regarding the DAC non-idealities, (3) was evaluated by implicitly assuming that each pulse in the DDPM sequence is a perfectly square pulse, i.e. the DDPM modulator output is constantly V_{DD} (0V) during 1 (0) pulses. Actually, the asymmetric rise/fall transitions in the output buffer driving the reconstruction filter give rise to non-linearity error. Indeed, for $D_{in} \leq 2^{N-1}$ (i.e., b_{N-1}=0), the analysis of the DDPM output in Fig. 8a shows that an increase in the input code by an LSB always introduces an additional rising-falling edge pair, resulting to nearly the same incremental error at each input code increase, and hence a gain error. However, for $D_{in} > 2^{N-1}$ (i.e., b_{N-1}=1), the increase of the input by an LSB actually reduces the number of rising-falling edge pairs by one, thus leading to a different gain error. This determines a double-slope non-linearity error, i.e. a piecewise-linear DAC characteristic whose

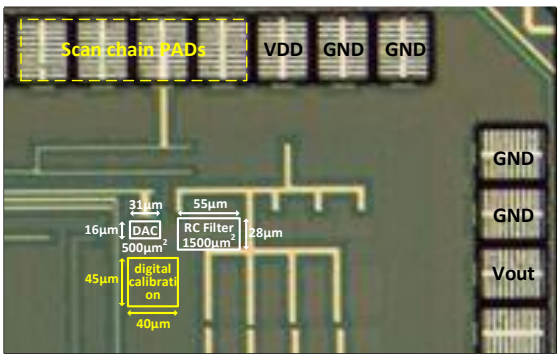

Fig. 7. 12-bit DDPM DAC testchip micrograph.

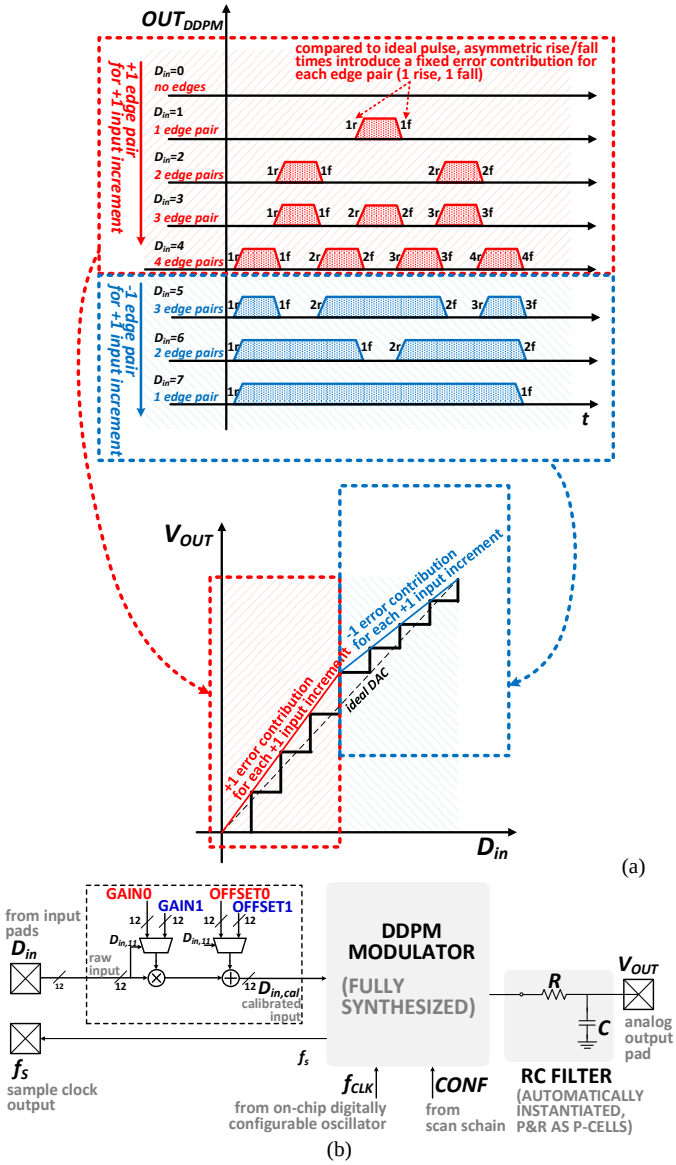

Fig. 8. a) 3-bit example showing the dual-slope gain error, b) digital calibration to suppress such error. Multiplier and adder are easily embedded in the digital block (e.g., Digital Signal Processor) driving the DAC input.

slope changes when crossing the digital input equal to 2^{N-1}.

The above non-ideality can be easily corrected by simply pre-multiplying the input by a proper coefficient that is different for the two code regions. Once the gain is corrected, the two half curves on the left and the right of 2^{N-1} need to be realigned by pre-adding an offset term to the input in the two code regions. Hence, the input pre- calibration generating a calibrated input $D_{\text{in,cal}}$ from the input D_{in} as in Fig. 8b is adopted:

$$D_{\text{in,cal}} = \begin{cases} GAIN0 \cdot D_{\text{in}} + OFF0 & \text{for } D_{in} \leq 2^{N-1} \\ GAIN1 \cdot D_{\text{in}} + OFF1 & \text{for } D_{in} > 2^{N-1} \end{cases} \quad (5)$$

The above coefficients are calibrated based on the preliminary analysis of the uncalibrated static transfer characteristics $V_{out}(D_{in})$. The gain error is first eliminated by correcting the slope of the first half curve so that its average LSB (i.e., $V_{out,0}(2^{N-1})/2^{N-1}$) is equal to the correct value. From (5), this is achieved by setting

$$GAIN0 = \frac{LSB}{\frac{V_{out,0}(2^{N-1})}{2^{N-1}}} \quad (6)$$

where LSB is the targeted LSB value for the calibrated DAC, and $V_{out,0}(2^{N-1})$ is the output voltage before calibration ($GAIN1$ is evaluated analogously). The offset coefficients $OFF0$ and $OFF1$ are then obtained by enforcing continuity of the two half curves around the middle point, leading to

$$OFF0 = 2^{N-1} - GAIN0 \cdot 2^{N-1} \quad (7)$$

with $OFF1$ being evaluated analogously. The amount of calibration required in the tested dice was minor, with a discontinuity of the uncalibrated curve around the middle point being close to one LSB.

In Fig. 8b, the different correction for $D_{in} \leq 2^{N-1}$ and $D_{in} > 2^{N-1}$ as in (5) is performed by a MUX driven by the input MSB. In practical cases, the function in (5) is executed by the microprocessor or Digital Signal Processor driving the DAC, thus not requiring any extra area.

V. Measurement Results

The testchip described in the previous section was first characterized at nominal operating conditions at full resolution, i.e. V_{DD}=1V, f_{CLK}=225MHz, with the DAC output connected to the testing equipment, whose equivalent input impedance is 100GΩ in parallel to 100pF. The test conditions represent a typical application scenario for the proposed DAC, which is driving a capacitive load up to the 100pF range with a full voltage swing from 0 to V_{DD}, without delivering any DC power to the load.

The static and dynamic characterization in nominal conditions are reported in Fig. 9. From this figure, the DNL (INL) is within ±1LSB (±2LSB), and the DAC achieves an SNDR of 70dB for a 1kHz sine input, corresponding to 11.3 effective bits (ENOB). The power consumption is 55µW and the resulting DAC figure of merit (FOM) results to 153dB, where FOM is defined as [9]-[12]

$$FOM = 10\log_{10}\cdot\frac{2^{2\cdot ENOB}\cdot BW}{P} \quad (8)$$

where BW is the bandwidth of the DAC, which is routinely assumed equal to half the Nyquist rate, and P is the power consumption.

The graceful resolution degradation was firstly characterized by measuring the DAC static characteristics, while progressively reducing the supply voltage below the nominal voltage. From Figs. 10a-b, scaling the voltage from 1V down to 0.55V leads to progressively larger errors as expected, with INL being degraded to ±5LSB. As shown in Fig. 11a, voltage over-scaling from 1V down to 0.7V degrades ENOB by 1 bit, with a graceful degradation of 0.3-0.5bit/100mV. At lower voltages close to the near-threshold region, the degradation is expectedly more rapid due to the faster gate delay increase when down-scaling V_{DD}. In particular, the resolution is degraded by 2.6 (3.2) bits at V_{DD} equal to 0.6V (0.55V), with a degradation sensitivity of 1.4ENOB/100mV. Fig. 11b shows the graceful resolution degradation under above-target clock frequencies. The ENOB degradation amounts to 1.5 bits when drastically increasing the clock frequency by 2X, which

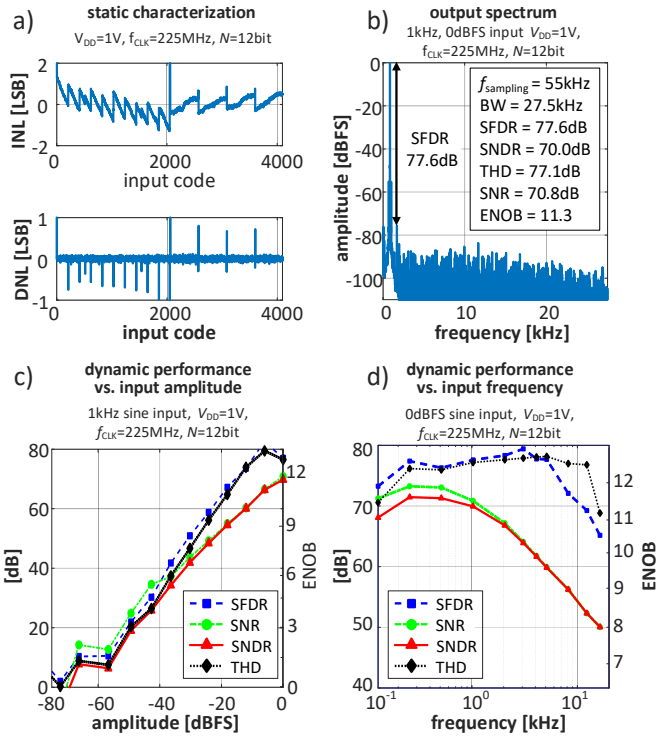

Fig. 9. Characterization of the proposed DAC under nominal conditions at full resolution: a) INL, DNL vs input code, b) output spectrum for full-swing 1-kHz sine wave input, c) SFDR, SNR, SNDR, THD vs. input amplitude (1-kHz sine wave), d) SFDR, SNR, SNDR, THD vs. input frequency (full-swing sine wave).

translates into a clock frequency sensitivity of 0.01bit/MHz above f_{max}. Again, further frequency over-scaling from 2X to 3X leads to more pronounced resolution degradation with clock frequency sensitivity of 0.017 bit/MHz.

Aggressive over-scaling the supply voltage or the clock frequency over the limits in Fig. 11 eventually leads to a catastrophic failure. From the measurements, the most likely cause is the failure of the clock division circuitry, which stops generating the clock correctly beyond a certain point. Nevertheless, the range of frequencies and voltages beyond which failures occur is actually very wide, as shown in Figs. 11a-b, with the voltage being scaled from nominal down to near-threshold, and the frequency being up-scaled by a factor of 2-3X, before failure occurs.

The power-resolution scalability of the proposed DAC was tested by reducing f_{CLK} at iso-sample rate first, and then at iso-resolution, as discussed in Section III.B. The former case is plotted in Fig. 11b (red curve), where 4X f_{CLK} reduction from 225MHz down to 55MHz reduces the power by 6X at the cost of 2-bit resolution degradation (from 12 to 10 bits), while maintaining the same sample rate of 55kS/s. This translates into a power-resolution sensitivity of 3X/bit. The case at iso-resolution is plotted in the same figure (green curve), and shows that 6X power reduction is obtained through 4X reduction in both f_{CLK} and sample rate (i.e., 13.75kS/s), while maintaining the full 12-bit resolution. This translates into a power-sample rate sensitivity of 3X/octave. Such ability to trade off power with either resolution or sample rate offers additional opportunities to reduce power, whenever one of these

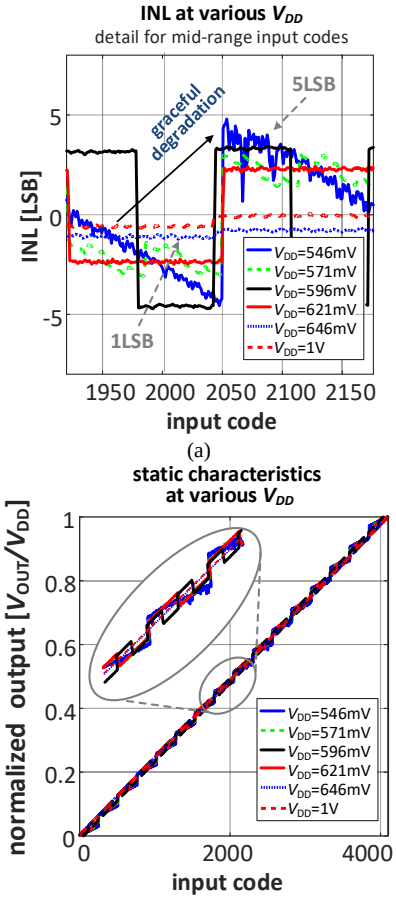

Fig. 10. Static characterization of graceful resolution degradation under over-scaled voltage down to 0.55V: a) static characteristics vs input code at different V_{DD}, b) INL vs input code at different V_{DD}.

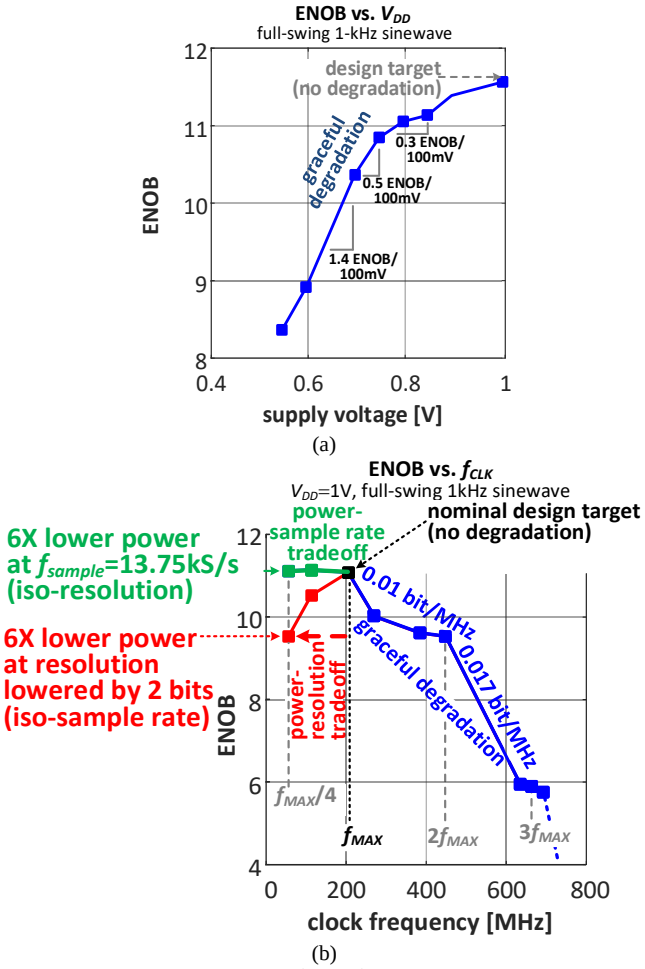

Fig. 11. Dynamic characterization of graceful degradation: resolution under a) V_{DD} over-scaling, b) frequency scaling. The nominal design target is the black square (f_{max}=225MHz, f_{sample}=55kS/s, nominal V_{DD}). In b), graceful resolution with frequency over-scaling (blue curve) and power-resolution tradeoff (red curve) are shown at same 55-kS/s sample rate. Dynamic power-sample rate tradeoff is shown by the green curve at same resolution.

requirements can be relaxed at run time. This capability is quite unique among DACs, as the power consumption of non-fully digital DACs is normally dominated by the analog circuitry, and is independent of the clock frequency (i.e., it cannot be traded off with resolution). Dynamic power-resolution is also very uncommon in fully-digital ΣΔ DACs [37]. Indeed, dynamic scaling of the oversampling ratio would require reconfigurable interpolators that can operate at different rates. Also, the precision of the arithmetic circuits employed in the loop filter (e.g., adders, multipliers) needs to be set for the largest output resolution, limiting the power savings under lower oversampling ratios. On the other hand, a DDPM DAC does not suffer from these limitations, in view of the inherent regularity of DDPM sequences and sub-sequences in Fig. 6.

In Figs. 12a-d, the results obtained in six die samples and under different voltage and temperatures are shown to gain an insight into the consistency of the above results across chips and environmental conditions (such analysis was not performed in prior art in Table I). From Fig. 12a, the graceful resolution degradation at reduced V_{DD} (Fig. 12a) and increased clock frequency (Fig. 12b) is confirmed across dice. A maximum ENOB degradation of 1 bit is observed from sample to sample under the same test conditions. Consistency is also confirmed by Fig. 12c, which plots the RMS static INL versus V_{DD} across five dice. This figure indeed shows that INL is also gracefully degraded across dice. In Fig. 12d, ENOB is shown to have a negligible dependence on the temperature, as less than 0.1-bit resolution variation takes place across the -25°C to 75°C temperature range. The above robustness across dice and temperature is a consequence of the inherently graceful performance degradation in the timing of the DDPM modulator.

The latter allows operation beyond $f_{\max}$ and below $V_{DD,min}$, thus avoiding design pessimism since frequency and voltage deviations cause a moderate resolution reduction. Similar to digital design frameworks for sub-systems with graceful degradation, the proposed DAC allows the designer to focus on the typical corner with very limited or no design margin.

As no gracefully degradable or power-resolution scalable DAC was available for comparison, the proposed DAC was compared to conventional DACs targeting a comparable sample rate range [9]-[12]. From Table I, the proposed DAC enables aggressive voltage scaling down to near-threshold voltages (i.e., 0.55V), as opposed to state-of-the-art DACs that operate at above-1V voltages [9]-[11]. This is explained by the digital

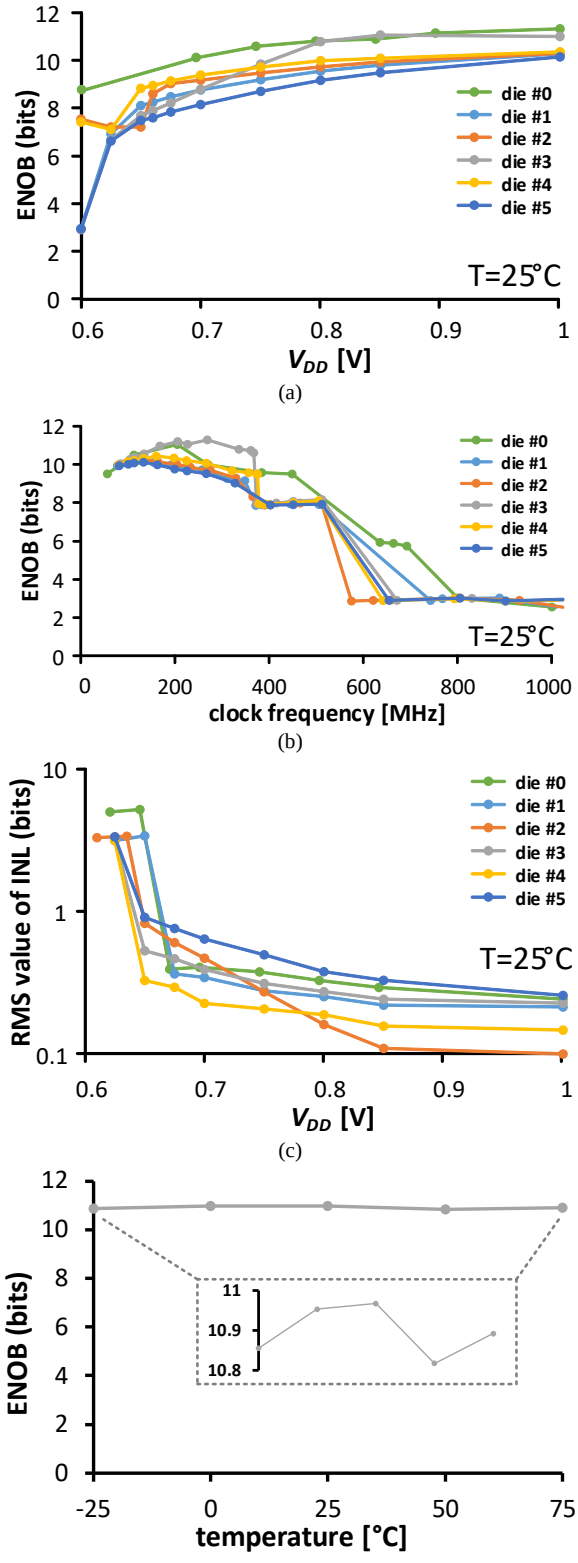

Fig. 12. Characterization across dice: a) ENOB vs. V_{DD}, b) ENOB vs. f_{CLK}, c) RMS INL vs. V_{DD}, d) ENOB vs. temperature. Die #0 was shown in Figs. 11a-b.

nature of the proposed DAC (i.e., it is not based on matched components) and the absence of active analog circuitry and its voltage headroom [7]. This simplifies system integration and voltage generation, while also reducing the power consumption. As an example, operation at 0.55V permits to reduce power by 4X, compared to 1V, following a nearly-quadratic law, as expected in digital circuits.

The proposed DAC has 28-2,800X lower area than [9]-[12], excluding the RC reconstruction filter for fair comparison. Even unfairly including the reconstruction filter area of 1,500μm^2 in the proposed DAC (and not in others), the area advantage is still in the 7-700X range. Such area advantage is explained by the avoidance of interpolators, arithmetic circuits and active analog circuitry needed by ΣΔ DACs, and by the very simple circuitry required by the DDPM modulator in Fig. 3. This area advantage further increases at finer technologies due to its digital architecture, which scales faster than analog counterparts [7].

The power consumption at nominal voltage and frequency is 55μW, which is 1.7X higher than the 9-bit DAC in [11], as expected from the lower resolution of the latter. However, re-configuring the DAC at 4X lower clock frequency, power is reduced to 9.1μW, i.e. 3.6X lower than [11] while still maintaining higher resolution. The resulting FOM ranges from 156dB to 160dB, which outperforms [11]-[12] by up to 20dB,and is worse than [9], [10] by 20dB. In other words, the above advantages in terms of voltage, power, area and design effort are achieved while maintaining a reasonable FOM, as it lies in the middle of the FOM range of comparable prior art. The FOM is also expected to improve at more recent technology generations due to its digital nature, thanks to the lower energy per cycle of the purely-digital DDPM modulator.

VI. Conclusion

A fully synthesizable, power-resolution scalable Nyquist-rate DAC operating down to 0.55V with graceful resolution degradation has been presented. The proposed architecture allows correct operation beyond the rated voltage and frequency, as timing violations appear in LSBs first and then progressively in more significant positions. A 12-bit DAC testchip in 40nm demonstrates resolution degradation under voltage and frequency scaling down to 0.3bit/100mV and 0.01bit/MHz, and an FOM lying in the middle range of prior art (i.e., 153-160dB).

The proposed DAC allows dynamic power-resolution scaling with 3X power reduction for 1-bit degradation, and power-sample rate scaling with 3X power reduction per octave. At system level, additional power benefits can be achieved by leveraging the DAC ability to withstand substantial voltage and frequency variations, thus relaxing the accuracy requirements in voltage and frequency generation. Thanks to its digital nature, the proposed DAC can be designed with very low effort (e.g., in Verilog) and fully-automated digital flows, enabling easy technology and design portability. Being based on standard cells, the DAC also achieves low area (i.e., 500μm^2 in 40nm) and digital-like shrinking across CMOS generations.

Appendix. Spectral Properties of DDPM Streams

The spectral properties of DDPM are summarized and compared with digital PWM (DPWM) in the following. The DDPM binary stream corresponding to a DC input D_{in} can be expressed in terms of its Fourier series as [22]

$$v_{out,D_{in}}(t) = V_{DD} \sum_{k=-\infty}^{+\infty} c_{D_{in},k} e^{2\pi j k f_{sample} t}, \qquad (A.1)$$

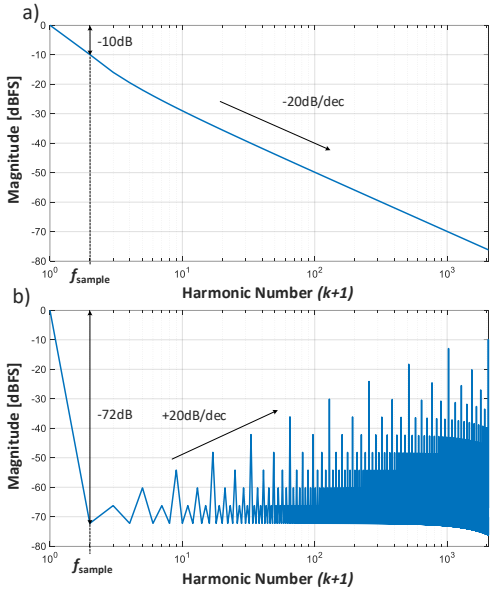

Fig. 13. Envelope of the magnitude spectra of a) PWM streams, b) DDPM streams for $N = 12$bit, showing the different spectral energy distribution.

where the magnitude of the harmonic coefficients $c_{D_{in},k}$ is

$$\left|c_{D_{in},k}\right| = \sum_{i=0}^{N-1} b_i \, 2^{i-N} \sum_{m=0}^{2^{N-i}-1} \delta[k - 2^i m]. \qquad \text{(A.2)}$$

$c_{D_{in},k}$ is non-zero only for harmonics of order $k = 2^i m$, with m being an integer and $i = 0 \ldots N-1$ (dyadic harmonics), and is proportional to 2^i.

As in Fig. 13b for N=12 bits, the peaks in the envelope of the harmonic coefficients increase with the harmonic order k at a 20dB/dec slope. This increasing behavior is opposite compared to DPWM (Fig. 13a), whose k-th harmonic decreases at 20dB/dec slope. Thus, the largest harmonic component to be rejected to retrieve the baseband component of a DDPM signal is at the highest frequency $2^N f_{sample}$, whereas its spectral content at f_{sample} is the lowest in magnitude (-$6N$dB below the DC component). In contrast, DPWM has the largest harmonic at f_{sample}, and just below the DC component (by $1/\pi$, i.e. ~10dB). The above results can be generalized to non-constant inputs, as they follow the same envelope as in Fig. 13b [22].

Thanks to the above properties, the requirements of the reconstruction filter in a DDPM DAC are substantially relaxed compared to DPWM at the same clock frequency and sample rate. For example, assuming a first-order RC reconstruction filter, the cutoff frequency needed to keep the harmonic components in (A.2) below the quantization error is found to be $2^{N+1}/\pi\sqrt{3}$ higher than the DPWM DAC at the same clock frequency and sample rate. This translates into a proportional reduction in the RC filter silicon area, and hence makes DDPM more amenable for low-cost on-chip integration.

TABLE I. COMPARISON WITH STATE-OF-THE-ART DACS WITH COMPARABLE SAMPLE RATE (BEST PERFORMANCE IN BOLD)

	This work			[9]	[10]	[11]	[12]
technology (nm)	40			45	180	350	350
type	DDPM modulation-based			ΣΔ	ΣΔ	switched-current	ΣΔ
area (μm²)	**500**			160,000[a)]	100,000 [a)]	14,000 [a)]	1,440,000 [a)]
area (F^2)	$0.4 \cdot 10^6$			$790 \cdot 10^6$	$3.1 \cdot 10^6$	$0.1 \cdot 10^6$ [b)]	$11 \cdot 10^6$
graceful resolution degradation	**YES**			NO	NO	NO	NO
power-resolution or power-sample rate dynamic tradeoff	**YES**			NO	NO	NO	NO
	nominal	*clock-scaled (iso-sample rate)*	*sample rate-scaled (iso-resolution)*				
resolution (bit)	12	10	12	**18**	N/A	9	16 [d)]
sample rate (kS/s)	55	55	13.75	48 [f)]	40 [f)]	111	48 [f)]
clock frequency (MHz)	225	55	55	3.072	6.25	N/A	3.072
DNL (LSB)	1	1	1	N/A	N/A	**0.8**	N/A
INL (LSB)	±2	±2	±2	N/A	N/A	**±1.6**	N/A
supply voltage (V) (analog/digital)	1/1	**0.7/0.7**	**0.7/0.7**	1.45/1.1	1.8/ N/A	3.3/3.3	0.8/0.8
min. supply voltage (V)	1	**0.55**	**0.55**	1.1	N/A	3.3	0.7
SNDR (dB) @ 1kHz	70	64.2	72	**108** [c)]	103 [c)]	48[d)]	69
SNDR (dB) @ $f_s/2$	50	46	46	N/A	N/A	N/A	N/A
dynamic range (dB)	74	62	74	108 [c)]	115 [c)]	N/A	88
THD (dB)	72.2	74	74	**104.6**	N/A	N/A	N/A
SFDR (dB)	72.5	72.5	74.9	**120**	N/A	N/A	N/A
ENOB	11.3	10.3	11.7	**17.6**	16.8	8[d)]	11.2
power (μW)	55	**9.1**	**9.1**	875	700[e)]	33	2,600
power-resolution scaling at iso-sampling rate	**3X/bit**			N/A	N/A	N/A	N/A
power-sampling rate scaling at iso-resolution	**3X/octave**			N/A	N/A	N/A	N/A
FOM (dB)	153	157	160	**180** [d)]	174[d)]	140 [d)]	140

[a)] As in prior art, area does not include the reconstruction filter (in the proposed DAC, it is the RC circuit in Fig. 3, occupying 1,500μm²). In [12], only the digital sub-system is considered. [b)]Area normalized to F^2 (F = process minimum feature size) is relatively constant across CMOS generations in digital architectures, and increases by slightly less than 2X in analog architectures. Hence, the area of [11] ported to 40nm is expected to translate into substantially larger area than this work, even though its normalized area is lower; [c)]A-weighted; [d)] based on text and figures; [e)] analog power only, [f)] twice the signal bandwidth for oversampled DACs.

ACKNOWLEDGEMENTS

The authors acknowledge the chip fabrication support from Mediatek Singapore, the MOE2014-T2-2-158 grant from the Singapore Ministry of Education, and the grant MSCA-GF ULPIoT:703988 from the EU Commission. The authors also thank Gopalakrishnan Ponnusamy for testing support.

REFERENCES

[1] M. Alioto (Ed.), *Enabling the Internet of Things – from Integrated Circuits to Integrated Systems*, Springer, 2017

[2] G. Chen, M. Fojtik, K. Daeyeon, D. Fick, J. Park, M. Seok, M. T. Chen, Z. Foo, D. Sylvester, D. Blaauw, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," *ISSCC Digest of Technical Papers (ISSCC)*, pp. 288-289, San Francisco (USA), 2010

[3] L. Freyman, D. Fick, M. Alioto, D. Blaauw, D. Sylvester, "A 346μm^2 VCO-based, Reference-Free, Self-Timed Sensor Interface for Cubic-Millimeter Sensor Nodes in 28nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2462-2473, Nov. 2014

[4] J. Richmond, M. John, L. Alarcon, W. Zhou, W. Li, T.-T. Liu, M. Alioto, S. R. Sanders, J. M. Rabaey, "Active RFID: A Perpetual Wireless Communications Platform for Sensors," in Proc. of *ESSCIRC 2012*, pp. 434-437, Bordeaux (France), Sept. 2012

[5] S. Paul, et Al., "A Sub-cm^3 Energy-Harvesting Stacked Wireless Sensor Node Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14-nm Tri-Gate CMOS for Always-ON Always-Sensing Applications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 961-971, April 2017

[6] O. Aiello, P. Crovetti, M. Alioto, "Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation Down to 0.3V," in Proc. of ISCAS 2018, Florence (Italy), May 2018

[7] G. Radulov, P. Quinn, H. Hegt, A. van Roermund, *Smart and Flexible Digital-to-Analog Converters*, Springer, 2011

[8] R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Springer, 2003

[9] L. Risbo, R. Hezar, B. Kelleci, H. Kiper, M. Fares, "A 108dB-DR 120dB-THD and 0.5Vrms output audio DAC with inter-symbol-interference-shaping algorithm in 45nm CMOS," *ISSCC Digest of Technical Papers (ISSCC)*, pp. 484-485, San Francisco (USA), 2011

[10] H. Westerveld, D. Schinkel, E. van Tuijl, "A 115dB-DR audio DAC with−61dBFS out-of-band noise," *ISSCC Digest of Technical Papers (ISSCC)*, San Francisco (CA), 2015

[11] H. S. Kim, J. Y. Jeon, S. W. Lee, J. H. Yang, S. T. Ryu, G. H. Cho, "A 0.014mm^2 9b switched-current DAC for AMOLED mobile display drivers," *ISSCC Dig. of Technical Papers*, pp. 316-318, San Francisco (CA), 2015

[12] K. Lee, et al., "A 0.8 V, 2.6 mW, 88 dB Dual-Channel Audio Delta-Sigma D/A Converter With Headphone Driver," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 916-927, March 2009

[13] S. Su, T. Tsai, P. K. Sharma and M. S. Chen, "A 12 bit 1 GS/s Dual-Rate Hybrid DAC With an 8 GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving > 75 dB SFDR Over the Nyquist Band," *IEEE Journal of Solid-State Circ.*, vol. 50, no. 4, pp. 896-907, April 2015.

[14] Maximum MAX5530/MAX5531 Datasheet [online] – available at *https://datasheets.maximintegrated.com/en/ds/MAX5530-MAX5531.pdf*

[15] J. Genoe, et Al., "Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption," *ISSCC Digest of Technical Papers (ISSCC)*, pp. 488-489, San Francisco (USA), 2014

[16] A. Sinha, A. P. Chandrakasan, "Dynamic Power Management in Wireless Sensor Networks," *IEEE Design & Test of Computers*, vol. 18, no. 2, pp. 62-74, March 2001

[17] M. Cho et al., "A 6×5×4mm3 General Purpose Audio Sensor Node with a 4.7μW Audio Processing IC," in Proc. in *IEEE VLSI Symp.*, 2017

[18] P. Harpe, H. Hegt, A. H. M. van Roermund, *Smart AD and DA Conversion*, Springer, 2011

[19] R. Hezar, L. Risbo, H. Kiper, M. Fares, B. Haroun, G. Burra, G. Gomez, "A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS," *ISSCC Dig. of Tech. Papers*, San Francisco (CA), 2010

[20] T. Rueger, B. Duewer, S. Hodapp, T. Lei, J. Melanson, B. Trotter, "A 110dB ternary PWM current-mode audio DAC with monolithic 2Vrms driver," *ISSCC Dig. of Tech. Papers*, San Francisco (CA), 2004

[21] W. H. Tseng, W. L. Lee, C. Y. Huang, P. C. Chiu, "A 12-bit 104 MS/s SAR ADC in 28 nm CMOS for Digitally-Assisted Wireless Transmitters," in IEEE Jour. of Solid-State Circ., vol. 51, no. 10, pp. 2222-2231, Oct. 2016

[22] P. S. Crovetti, "All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation," *IEEE Trans. on Circuits and Systems I – part I*, vol. 64, no. 3, pp. 573-584, Mar. 2017

[23] O. Aiello, P. Crovetti, L. Lin and M. Alioto, "A pW-Power Hz-Range Oscillator Operating With a 0.3–1.8-V Unregulated Supply," in *IEEE Journal of Solid-State Circuits*, In print.

[24] S. Carreon-Bautista, L. Huang, E. Sanchez-Sinencio, "An Autonomous Energy Harvesting Power Management Unit With Digital Regulation for IoT Applications," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 6, pp. 1457-1474, June 2016

[25] N. Shanbhag et al., "Stochastic computation," in *Design Automation Conference (DAC)*, 2010 47th ACM/IEEE, June 2010, pp. 859–864

[26] A. B. Kahng, S. Kang, R. Kumar, J. Sartori, "Slack Redistribution for Graceful Degradation Under Voltage Overscaling," *2010 15th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, 2010, pp.825-831

[27] M. Cho, et al., "Post-silicon voltage-guard-band reduction in a 22nm graphics execution core using adaptive voltage scaling and dynamic power gating," *ISSCC Digest of Technical Papers (ISSCC)*, San Francisco, CA, 2016, pp. 152-153

[28] S. Zhang, N. R. Shanbhag, "Embedded Algorithmic Noise-Tolerance for signal processing and machine learning systems via data path decomposition," *IEEE Transactions on Signal Processing*, July 2016

[29] A. Orailoglu , "Graceful degradation in synthesis of VLSI ICs," in Proc. of *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 301-311, Austin (TX), Aug. 1998

[30] R. Hegde, N. Shanbhag, "A voltage overscaled low-power digital filter IC," *IEEE Journ. of Solid-State Circ.*, vol. 39, no. 2, pp. 388–391, Feb. 2004

[31] R. Hegde, N. Shanbhag, "Energy-efficient signal processing via algorithmic noise-tolerance," in Low Power Electronics and Design, 1999 Proc. 1999 International Symposium on, Aug 1999, pp. 30–35

[32] F. Frustaci, M. Khayatzadeh, D. Blaauw, D. Sylvester and M. Alioto, "A 32kb SRAM for error-free and error-tolerant applications with dynamic energy-quality management in 28nm CMOS," *ISSCC Digest of Technical Papers (ISSCC)*, San Francisco (CA), 2014, pp. 244-245

[33] F. Frustaci, D. Blaauw, D. Sylvester, M. Alioto, "Approximate SRAMs with Dynamic Energy-Quality Management," *IEEE Trans. on VLSI Systems*, vol. 24, no. 6, pp. 2128-2141, June 2016

[34] H. Lee, S. Cho, B. R. Childers, "Performance of Graceful Degradation for Cache Faults," in Proc. of ISVLSI'07, pp. 409-415, Porto Alegre (Brazil), 2007

[35] A. Kohler, G. Schley, M. Radetzki, "Fault Tolerant Network on Chip Switching With Graceful Performance Degradation," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, no. 6, pp. 883-896, May 2010

[36] M. Yip, A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC," *ISSCC Digest of Technical Papers (ISSCC)*, San Francisco (CA), 2011, pp. 190-191

[37] R. C. C. Cheung, K. P. Pun, S. C. L. Yuen, K. H. Tsoi and P. H. W. Leong, "An FPGA-based re-configurable 24-bit 96kHz sigma-delta audio DAC," Proceedings. 2003 IEEE Int. Conf. on Field-Progr. Technology (FPT), Tokyo, Japan, 2003, pp. 110-117

Orazio Aiello (S'06–M'15) received the B.Sc degree in Electronic Engineering and the M.Sc degree in Microelectronic Engineering from the University of Catania in 2005 and 2008, respectively (both cum laude). In 2013, he received the PhD degree from Politecnico di Torino. In 2008-2009, he worked at the EMC Competence Center of the Istituto Superiore Mario Boella (Turin, Italy). In 2012, he was Visiting PhD Student at Monash University. In 2013 he was part of a joint project with FIAT-Chrysler Automobiles, in 2014 he joined NXP Semiconductors as Mixed Signal IC Designer and EMC expert. In 2015-2016 he was Visiting Fellow at the University of Sydney and University of New South Wales. Since 2015 he has collaborated with the Green IC group at National University of Singapore where he is now a Marie Skłodowska-Curie Individual and Global Fellow (MSCA-IF-GF). His main research interests include the design for reliability of System Basis Chip front-ends in harsh environments, energy-efficient circuit design and mostly-digital sensor interfaces. He is currently leading the ULPIoT project, funded by the European Commission.

Paolo Crovetti (S'00-M'04) was born in Turin, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Turin, Turin, Italy, in 2000 and 2003, respectively.

He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin. He has co-authored more than 50 papers appearing in journals and international conference proceedings. His main research interests are in the fields of analog, mixed-signal, and power integrated circuits. His recent research activities are focused on non-conventional information processing techniques allowing the fully digital implementations of analog functions and on ultra-low-power IC design for Internet of Things (IoT) applications.

Prof. Crovetti is an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS and a Subject Editor of IET Electronics Letters in the area of Circuits and Systems and serves as a regular reviewer for several IEEE journals.

Massimo Alioto (M'01–SM'07-F'16) received the Laurea (MSc) degree in Electronics Engineering and the Ph.D. degree in Electrical Engineering from the University of Catania (Italy) in 1997 and 2001, respectively. He is with the ECE Department, National University of Singapore where he leads the Green IC group and is the Director of the Integrated Circuits and Embedded Systems area. Previously, he held positions at the University of Siena, Intel Labs, University of Michigan Ann Arbor, University of California, Berkeley, and EPFL.

He has authored or co-authored more than 250 publications. One of them is the second most downloaded TCAS-I paper in 2013. He is co-author of three books, including *Enabling the Internet of Things - from Circuits to Systems* (Springer, 2017). His primary research interests include self-powered wireless integrated systems, near-threshold circuits, widely energy-scalable systems, data-driven integrated systems, hardware-level security, among the others.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems, and Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. He is/was Distinguished Lecturer, and member of the Board of Governors of the CASS Society, and Chair of the "VLSI Systems and Applications" Technical Committee. He served as Guest Editor of several IEEE journal special issues (e.g., TCAS-I, TCAS-II, JETCAS) and as Associate Editor. He is/was Technical Program Chair in a number of conferences (e.g., ISCAS 2022, SOCC, ICECS, NEWCAS), and TPC member (ISSCC, ASSCC). Prof. Alioto is an IEEE Fellow.