Modeling and Simulation for Signal and Power Integrity in Mobile Platforms

Tutorial

22nd IEEE Workshop on Signal and Power Integrity
May 22-25, 2018, Brest, France

Modeling and Simulation for Signal and Power Integrity in Mobile Platforms

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Abstract. This tutorial will cover technological, architectural, modeling and simulation challenges for the Signal and Power Integrity of high-end mobile platforms. On one hand, the latest packaging technologies for mobile applications will be discussed, emphasizing their pros and cons in view of current and expected future system requirements. On the other hand, the architectural challenges will be translated into modeling and simulation challenges, that engineers have to face in their daily work for ensuring system-level signal and power quality. Fast simulation approaches based on reduced-order behavioral models for both interconnects and devices will be discussed in detail. Finally, case studies from real mobile applications will be illustrated.

Gianni Signorini is a Staff Engineer in the "Chip-Package-Board" team of Intel Communication and Devices Group (iCDG). He is leading the execution and methodology development for Signal and Power Integrity simulations of Intel Mobile Modem solutions. Gianni received his B.Sc. (2010), M.Sc. (2012) and Ph.D. (2016) in Electronic Engineering from the University of Pisa, Italy. He joined Intel in 2011 and he is based in Munich, Germany.

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Part 1: Signal and Power Integrity Challenges in Mobile System-in-Package and Platforms

- Package/PCB/SiP Technologies
- Signal Integrity Challenges
- Power Integrity Challenges

Detailed list of topics:

- Package/PCB/SiP Technologies (40mins)
  - Limitation of standard Package/PCB (thickness, area, #IOs, …)
  - Wafer-Level vs Flip-chip Packages, #Layers
  - Trend: Integration as PoP, System-in-Package, Modules
  - Integration of Passives, Die-stacking
- Chip-Package-Board Co-Design (5mins)
  - Methodology, Opportunities, Challenges in parallel, concurrent Chip/Package/Board Co-Design
  - EDA Tools, Challenges in 3D-EM simulations of combined Chip/Package/Board

- Signal Integrity Challenges (15mins)
    - Basics
    - High-Speed Interface Trends: PCIe Gen4, Memory LP4/LP4x, MIPI DigRF4
    - EMIB / Hybrid Packages / PoP / InFO-PoP
- Power Integrity Challenges (30mins)
    - Basics
    - Placement/BoM Constraint, Integrated Passives
    - Model availability (non-standard methodology required)
    - Noise coupling in RF interfaces and HSIO PHYs

Part 2: Signal and Power Integrity Modeling and Simulation

- Macromodeling for Passives, Interconnects and Power Delivery Networks
    - Overview of Linear Time-Invariant macromodeling approaches
    - Classical Model Order Reduction
    - Data-driven approaches: rational interpolation and approximation
    - Post-processing: passivity verification and enforcement
    - Parameterization schemes and multivariate modeling
- Macromodels for High-Speed IOs
    - Overview of driver and receiver modeling approaches
    - From transistor-level to behavioral and algorithmic modeling
- Methodologies for Signal Integrity, Power Integrity and RF Simulations
    - State-of-the-art and Recent Advancements
    - Application examples