All-Digital High Resolution D/A Conversion by Dyadic Digital Pulse Modulation

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***Abstract*— In this paper, the limitations of digital-to-analog (D/A) conversion by Digital Pulse Width Modulation (DPWM) are addressed and the novel Dyadic Digital Pulse Modulation (DDPM) technique for all-digital, low cost, high resolution, Nyquist-rate D/A conversion is proposed. Thanks to the spectral characteristics of the new modulation, in particular, the requirements of the filter needed to extract the baseband component of DPWM signals can be significantly released so that to be suitable to inexpensive integration on silicon in analog interfaces for nanoscale integrated systems. After the new DDPM technique and its properties are introduced on a theoretical basis, the implementation of a D/A converter (DAC) based on the proposed modulation is addressed and its performance in terms of noise and linearity is discussed. A 16-bit DDPM-DAC prototype is finally synthesized on a field-programmable gate array (FPGA) and experimentally characterized.**

***Index Terms*— Dyadic Digital Pulse Modulation (DDPM), Digital Pulse-Width Modulation (DPWM), Digital-to-Analog (D/A) Converter (DAC), On-Chip DAC, Mostly Digital Analog Interface, Digital Assisted Analog Interface.**

I. Introduction

THE limitations of present-day nano-scale MOS transistors as analog devices [1] have brought an increasing interest towards mostly-digital (MD) [2-8] and digitally-assisted (DA) [9-12] analog interfaces (AIs) for present day and future integrated systems. Both MD AIs, where analog signal processing is (almost) completely moved to the digital domain and implemented by synthesizable logic (Fig.1a), and DA AIs, where critical calibration, conditioning, configuration and biasing are managed by a digital unit (Fig.1b), very often rely on accurate monitoring and generation of continuous-in-amplitude voltages and currents which require on-chip analog-to-digital (A/D) and digital-to-analog (D/A) conversion.

Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) for MD/DA AIs [13] should be mostly-digital circuits themselves, with a very good static accuracy, intrinsically robust to process variations and mismatch and suitable to be implemented in nanoscale technologies with a minimum overhead in terms of silicon area and power consumption. By contrast, bandwidth and dynamic performance are often not critical [7].

Focusing on DACs, state-of-the-art topologies based on weighted resistances, capacitances or transistor aspect ratios are not attractive, since they strongly rely on device matching and therefore require a large silicon area to achieve a high resolution [14-15]. On the other hand, sigma-delta ($\Sigma\Delta$) DACs [16-19] do not provide an output at a fixed rate, often involve rather complex, area and power intensive, digital hardware and require design efforts to avoid in-band spurious and stability issues related to the closed-loop nonlinear dynamics. Moreover, multi-bit $\Sigma\Delta$ DACs [20] are not fully digital since they require low-resolution (2-5 bit) accurate DACs based on other techniques.

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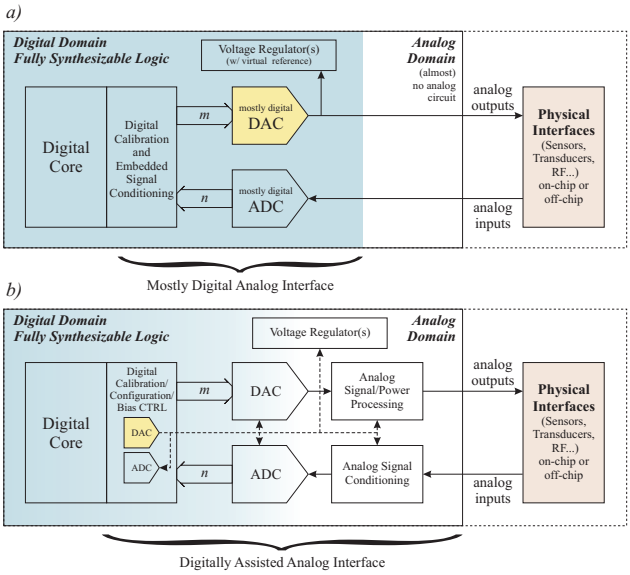

Fig. 1. Target applications of the proposed DAC in a) Mostly Digital [2-8] (MD) and b) Digital-Assisted (DA) [9-12] IC analog interfaces.

In this scenario, digital pulse width modulation (DPWM) could be an interesting option for D/A conversion [21], since it is intrinsically digital, process insensitive and inexpensive. Unfortunately, however, the requirements of the output filter needed to extract the baseband component of a DPWM stream, even for a constant digital input, i.e. in (quasi) static conditions, are very stringent and not compatible with integration.

In this paper, the limitations of DPWM-based D/A conversion are addressed and the new Dyadic Digital Pulse Modulation (DDPM) technique for all-digital, low-cost D/A conversion in MD/DA AIs is proposed. The effectiveness of the novel technique is verified on the basis of theory and experiments performed on a field-programmable gate array (FPGA)-based 16-bit DDPM DAC prototype.

The paper has the following structure: in Section II, the strict trade-off between resolution and output filter requirements, which limits the application of DPWM for high resolution D/A conversion, is revised. The possibility to overcome such limitation is then addressed in Section III, where the novel DDPM technique is proposed and the spectral characteristics of DDPM-modulated signals are analyzed. In Section IV,

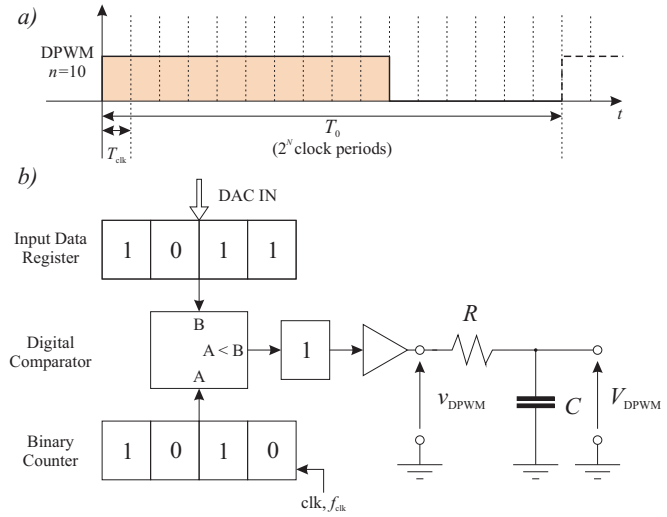

Fig. 2. Digital Pulse Width Modulation (DPWM) for D/A Conversion: a) 4-bit DPWM Waveform, b) Hardware Implementation of a 4-bit DPWM DAC.

the hardware implementation of a DDPM DAC is discussed and its synthesizable VHDL description is provided while, in Section V, the static linearity and noise performance of a DDPM DAC is investigated together with the possibility to compensate systematic errors by digital calibration. In Section VI, an FPGA prototype of a DAC based on the novel technique is then considered and its measured performance is reported. Finally, in Section VII, some concluding remarks are drawn.

II. D/A Conversion by Digital Pulse Width Modulation (DPWM) and its Limitations

The conventional DPWM technique and its limitations as a method for on-chip D/A conversion under (quasi) static conditions, which can be significantly released by the novel DDPM technique proposed in this paper, are shortly revised in this Section.

A. D/A Conversion by Digital Pulse Width Modulation

In a synchronous digital system operated at a clock frequency $f_{\rm clk} = 1/T_{\rm clk}$, where high ("1") and low ("0") logic levels are associated to the constant supply voltage $V_{\rm DD}$ and to the reference voltage (0V), respectively, a voltage proportional to an N-bit binary code n to be converted into analog can be obtained by digital pulse width modulation[1] (DPWM), i.e. taking the DC component of the voltage $v_{{\rm DPWM},n}(t)$ of a digital line, periodically driven with a sequence of 2^N bits consisting of n ones followed by $2^N - n$ zeros, as shown in Fig.2a. Such a sequence can be easily generated by a digital comparator whose inputs are fed by a register storing the input code n and by an N-bit free-running binary counter, as depicted in Fig.2b.

[1]Uniform sampled trailing edge DPWM is considered unless otherwise specified. The considerations on the magnitude spectra under static conditions, however, apply to all DPWM modulations (trailing-edge, leading-edge and double-edge DPWM), which differ from each other only for a time shift under static conditions.

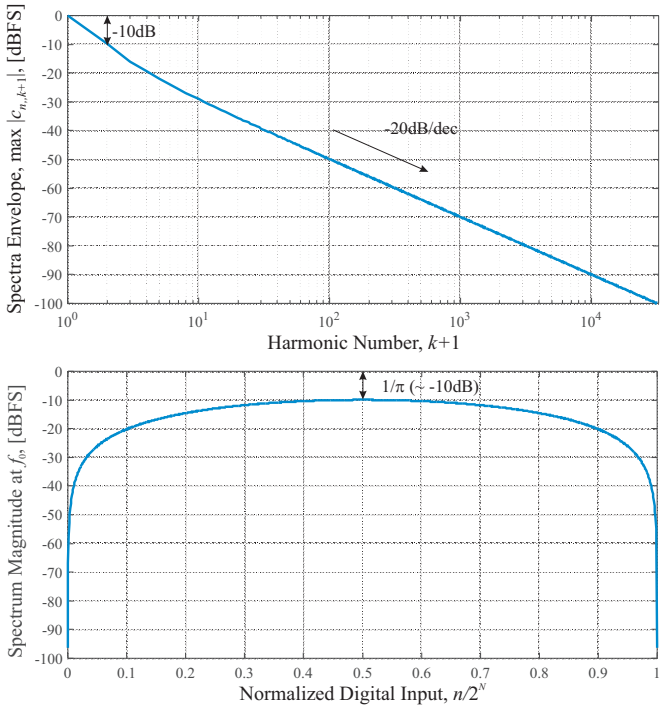

Fig. 3. Digital Pulse Width Modulation (DPWM), $N = 16$ bit resolution: top) envelope of the spectra of the 2^{16} DPWM waveforms for different digital inputs, bottom) amplitude of the spectral component at the fundamental frequency $f_0 = f_{\rm clk}/2^N$ versus normalized digital input $n/2^N$.

The resulting voltage waveform $v_{{\rm DPWM},n}(t)$, in fact, is a square wave with a frequency $f_0 = 1/(2^N T_{\rm clk}) = f_{\rm clk}/2^N$ and a duty cycle $D = n/2^N$, can be expressed for $n \neq 0$ as[2]

$$v_{{\rm DPWM},n}(t) = V_{\rm DD} \sum_{k=-\infty}^{+\infty} \Pi\left(\frac{t}{nT_{\rm clk}} - \frac{1}{2} - \frac{2^N}{n}k\right), \quad (1)$$

where

$$\Pi(x) = \begin{cases} 1 & |x| < \frac{1}{2} \\ \frac{1}{2} & |x| = \frac{1}{2} \\ 0 & |x| > \frac{1}{2} \end{cases},$$

and its spectrum

$$V_{{\rm dpwm},n}(f) = V_{\rm DD} \sum_{k=-\infty}^{+\infty} c_{k,n}\delta\left(f - kf_0\right), \quad (2)$$

where $\delta(\cdot)$ is the Dirac distribution and

$$c_{k,n} = D\,{\rm sinc}(kD){\rm e}^{\jmath\pi kD} = \frac{n}{2^N}\,{\rm sinc}\left(\frac{kn}{2^N}\right){\rm e}^{-\frac{\jmath\pi kn}{2^N}}, \quad (3)$$

in which ${\rm sinc}(x) = \sin(\pi x)/\pi x$, shows a DC component $n/2^N\, V_{\rm DD}$ proportional to the input code n. This component can be extracted by a low pass filter (LPF), as shown in Fig.2b, and taken as the output of a very low cost, fully digital DAC, whose static accuracy and linearity can be excellent being only limited by fluctuations in the clock and in the supply voltage.

Unfortunately, however, the effectiveness of DPWM as a D/A conversion technique is completely impaired by the requirements of the LPF needed to extract the DC component of a DPWM signal, as discussed in what follows.

[2]The same expression can be extended by continuity to the case $n = 0$ (identically null signal). This extension is implicitly assumed in what follows.

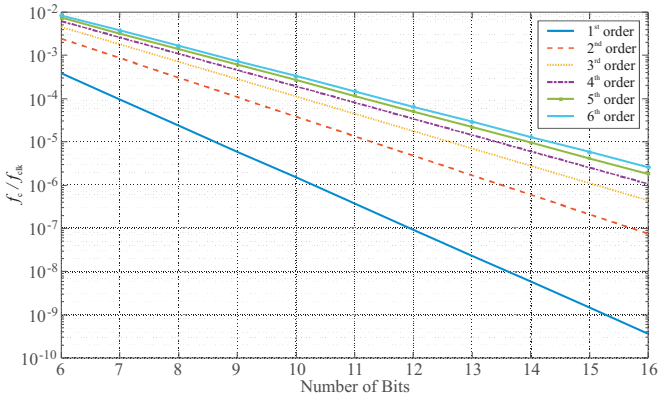

Fig. 4. Clock Frequency/Output Filter Corner Frequency/Resolution tradeoff in a DPWM DAC: output filter corner frequency f_c normalized with respect to the clock frequency f_{clk} versus number of bits, for different filter orders.

B. DPWM DAC Filter Requirements and Trade-offs

To discuss the requirements of the output filter of a DPWM DAC under (quasi) static conditions, from the envelope of the magnitude spectra of the 2^N N-bit DPWM waveforms, defined as

$$\max_{0\le n<2^N} V_{DD}|c_{k,n}| = \max_{0\le n<2^N} \frac{n}{2^N} V_{DD}\,\mathrm{sinc}\left(\frac{kn}{2^N}\right),$$

and reported in Fig.3 for N=16 bits, it can be observed that the largest AC component to be rejected over all DPWM waveforms is at the fundamental frequency f_0 (i.e. for $k=1$) and it is only a factor $\alpha_0 = 1/\pi$, i.e. about 10dB, below the full swing V_{DD}.

To keep the spectral component at the fundamental f_0 below the upper bound of quantization error $\varepsilon = V_{DD}/2^{N+1}$ in the worst case, a LPF with an attenuation[3] α_F at f_0

$$\alpha_F < \frac{\varepsilon}{V_{DD}\alpha_0} = \frac{\pi}{2^{N+1}} \tag{4}$$

is therefore needed. Since higher harmonics of DPWM signals monotonically decrease with frequency, a LPF providing at least the same attenuation α_F at frequencies $f > f_0$ is sufficient to have all the harmonics below the quantization error so that condition (4) can be taken as the specification for the output filter of a DPWM DAC.

Nevertheless, meeting (4) is a real challenge for an IC implementation. For a P-th order LPF with an out-of-band asymptotic attenuation $\alpha(f) = (f_c/f)^P$ increasing with frequency with a slope of $20\cdot P$ dB/dec above the corner frequency f_c (e.g. a Butterworth filter), to meet condition (4), it should be

$$f_c < \sqrt[P]{\alpha_F} f_0 = \sqrt[P]{\pi}\, 2^{-\frac{N+1}{P}} f_0 = \sqrt[P]{\pi}\, 2^{-\frac{N(P+1)+1}{P}} f_{clk}. \tag{5}$$

From (5), for a given clock frequency f_{clk}, the resolution N of a DPWM-based DAC is traded off with the corner frequency f_c, which is also an upper bound of the DAC bandwidth. Given a 100 MHz clock, for instance, a first-order ($P=1$) LPF with a corner frequency of less than 2.4kHz is required to meet condition (5) in an 8-bit DPWM DAC, while a first-order ($P=1$) LPF with a corner frequency of less than 10Hz or a second-order ($P=2$) filter with a corner frequency below 400Hz would be needed for a 12-bit resolution.

If the clock frequency is lower and/or a higher resolution is targeted, the situation is worse and cannot be substantially improved increasing the order of the LPF above $P=2$, as highlighted in Fig.4, where a full picture of the trade-off is given. In practice, for a clock frequency lower than 1 GHz, a fully integrated DPWM DAC with more than a 7-8 bit resolution would require active or passive integrated filters, which are complex and/or analog-intensive and/or requiring large passives, close to or beyond the limits of feasibility.

The tradeoff between clock, LPF requirements and resolution highlighted above completely impairs the potential advantages of DPWM as a technique for on-chip, high-resolution D/A conversion and makes it not competitive with other methods. To address this substantial limitation, which is also felt in the fields of digital audio, power electronics and control, improved DWPM techniques [21-30], e.g. involving modulated DPWM signals [22], taking advantage of pulses with a sub-clock time resolution [23], or based on oversampling and multibit noise shaping [29], have been proposed and also implemented in commercial devices. Nonetheless, such techniques require more complex, expensive and analog-intensive hardware than standard DPWM and are therefore not well suited to MD/DA AIs. An alternative approach is proposed in what follows.

III. The Dyadic Digital Pulse Modulation (DDPM)

In this section, considering that the DPWM sequence in Fig.2a is just one of the $\binom{n}{2^N}$ binary sequences of 2^N bits with n ones and 2^N-n zeros corresponding to a digital stream with a mean value $n/2^N$ V_{DD} proportional to an integer code n, the possibility to exploit other, non-DPWM sequences, better suited to on-chip D/A conversion is explored to overcome the stringent limitations of DPWM discussed so far.

A. Dyadic Sequences

The strict requirements for the output filter of a DPWM DAC are due to the fact that most of the harmonic content of a DPWM signal is concentrated at the fundamental frequency $f_0 = f_{clk}/2^N$, as shown in Fig.3a, which is inversely proportional to the number of quantization intervals 2^N and is therefore very low, close to the baseband and difficult to be rejected. In Fig.3b, it can be observed that the amplitude at the fundamental frequency is maximum for $n = 2^{N-1}$ (i.e. the value associated to the MSB in an N bit binary representation), which is therefore the worst-case input code that dictates the DPWM DAC output filter specification (5).

To release such a stringent requirement, it can be observed that the same input code $n = 2^{N-1}$, which corresponds to a DPWM sequence with an equal number of ones, all clustered in the first part of the DPWM period, and zeros, all in the second part of the period, can be more conveniently associated to the sequence $S_{N-1} = \ldots 10101010\ldots$ including ones

[3]The *attenuation* is here considered as a scaling factor $\alpha \in (0,1)$ and not as its reciprocal. At the same time, in discussions, a value of α close to zero will be considered as a *large attenuation* and a value of α close to one as a *small attenuation*.

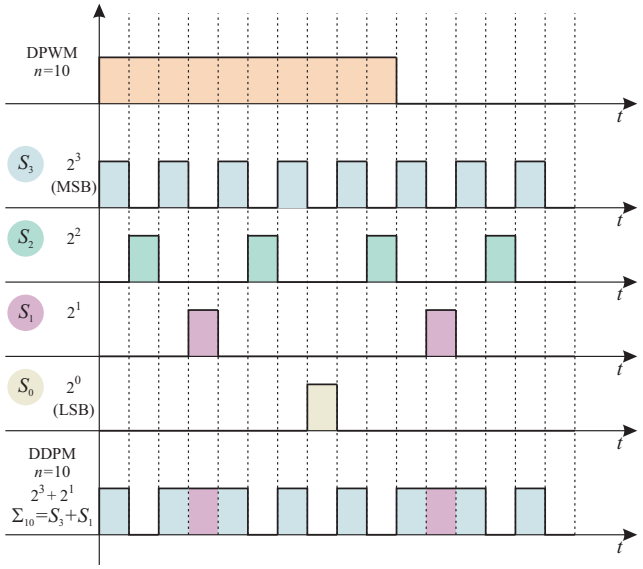

Fig. 5. Dyadic sequences and Dyadic Digital Pulse Modulation (DDPM) waveforms.

interleaved with zeros, as depicted in Fig.5. The resulting waveform, in fact, has the same DC component of the MSB DPWM waveform but, being periodic with period $2T_{\rm clk}$, it does not include any spectral content at f_0 and its AC power is all above $2^{N-1}f_0 = f_{\rm clk}/2$, which is much higher than f_0 in a high-resolution DAC, and is therefore much easier to be suppressed by a low-pass filter.

Similarly, the $n = 2^{N-2}$ input code, which corresponds to the second MSB and requires 1/4 of ones and 3/4 of zeros in a period, can be associated to a sequence $S_{N-2} = \ldots 10001000\ldots$ obtained repeating a pattern of a one followed by three zeros, as depicted in Fig.5. The corresponding waveform, which is actually periodic with a period $4T_{\rm clk}$, again does not show any spectral component at f_0 and its AC power is all above $2^{N-2}f_0 = f_{\rm clk}/4$. It is worth noting that, even though $2^{N-2}f_0$ is lower (one half) than $2^{N-1}f_0$, the second MSB waveform is not more difficult to be filtered than the MSB waveform, since the amplitude of its spectral lines is reduced as well by a factor two.

The same reasoning can be applied recursively down to the LSB, which can be associated to a sequence $S_0 = \ldots 00001000\ldots$ with a single one over 2^N slots, i.e. to a waveform that is periodic with a period $2^N T_{\rm clk}$: this waveform has a spectral component at f_0, indeed, nonetheless it is extremely weak and requires just an attenuation of 1/2 (i.e. $6\,{\rm dB}$) to be rejected below the quantization error level. The sequences S_i introduced above, which include 2^i ones spaced of 2^{N-i} positions, will be indicated as i-th order *dyadic* sequences hereafter.

B. Dyadic Digital Pulse Modulation

It is interesting to observe that dyadic sequences S_n up to the $(N-1)$-th order introduced thus far, which are much easier to be filtered than the DPWM streams with the same mean value, can be arranged in a 2^N-bit frame so that the positions of the "one" pulses belonging to different sequences are non-overlapping, as in Fig.5. Starting from the beginning of the 2^N-bit frame, in fact, every other of the 2^N slots, i.e. 2^{N-1} slots, can be assigned to the (ones of the) MSB sequence S_{N-1}, every other of the 2^{N-1} remaining slots, i.e. 2^{N-2} slots spaced by three slots, can be assigned to the (ones of the) second MSB sequence S_{N-2} and so on, till the LSB, which takes one of the two last available slots.

Following this approach, a set of N 2^N-bit orthogonal dyadic sequences S_i with $i = 0\ldots N-1$, including 2^i ones, is thus defined and any integer $n \in [0, 2^N)$, which can be written in terms of its binary representation as

$$n = \sum_{i=0}^{N-1} b_{i,n} 2^i$$

where $b_{i,n}$ is the i-th binary digit of n, can be uniquely expressed by superposition of orthogonal dyadic sequences as

$$\Sigma_n = \sum_{i=0}^{N-1} b_{i,n} S_i. \tag{6}$$

The sequence Σ_n defined in (6) includes by construction exactly n ones and $2^N - n$ zeros and therefore corresponds to a digital stream with a mean value proportional to n and suitable to be extracted for D/A conversion.

Considering the more favorable spectral properties of dyadic sequences, the association of an integer n to the binary sequence Σ_n defined as in (6), which will be indicated hereafter as *dyadic digital pulse modulation* (DDPM), is proposed in this paper as an alternative to DPWM for high-resolution on-chip D/A conversion. The properties of DDPM signals, both in (quasi) static conditions and for time-varying input codes, are discussed in what follows.

C. DDPM D/A Conversion under Quasi-Static Conditions

The DDPM sequence associated to a constant input code n by (6) corresponds to a digital waveform

$$v_{{\rm DDPM},n}(t) = V_{\rm DD} \sum_{k=-\infty}^{+\infty} x_n(t - 2^N k T_{\rm clk}) \tag{7}$$

where

$$x_n(t) = \sum_{i=0}^{N-1} \sum_{h=0}^{2^i-1} b_{i,n} \Pi\left(\frac{t}{T_{\rm clk}} - 2^{N-i}h - 2^{N-i-1} - \frac{1}{2}\right) \tag{8}$$

with a spectrum

$$V_{{\rm ddpm},n}(f) = V_{\rm DD} \sum_{k=-\infty}^{+\infty} c_{k,n}\, {\rm sinc}\left(\frac{k}{2^N}\right) \delta\left(f - k f_0\right) \tag{9}$$

where $f_0 = 1/T_0 = f_{\rm clk}/2^N$ and

$$c_{k,n} = \sum_{i=0}^{N-1} b_{i,n} 2^{i-N} \sum_{m=0}^{2^{N-i}-1} \delta\left[k - 2^i m\right] {\rm e}^{-\jmath\pi m\left(1+2^{i-N}\right)} \tag{10}$$

where $\delta[\cdot]$ is the Kroenecker function defined as

$$\delta[n] = \begin{cases} 1 & n = 0 \\ 0 & n \neq 0. \end{cases} \tag{11}$$

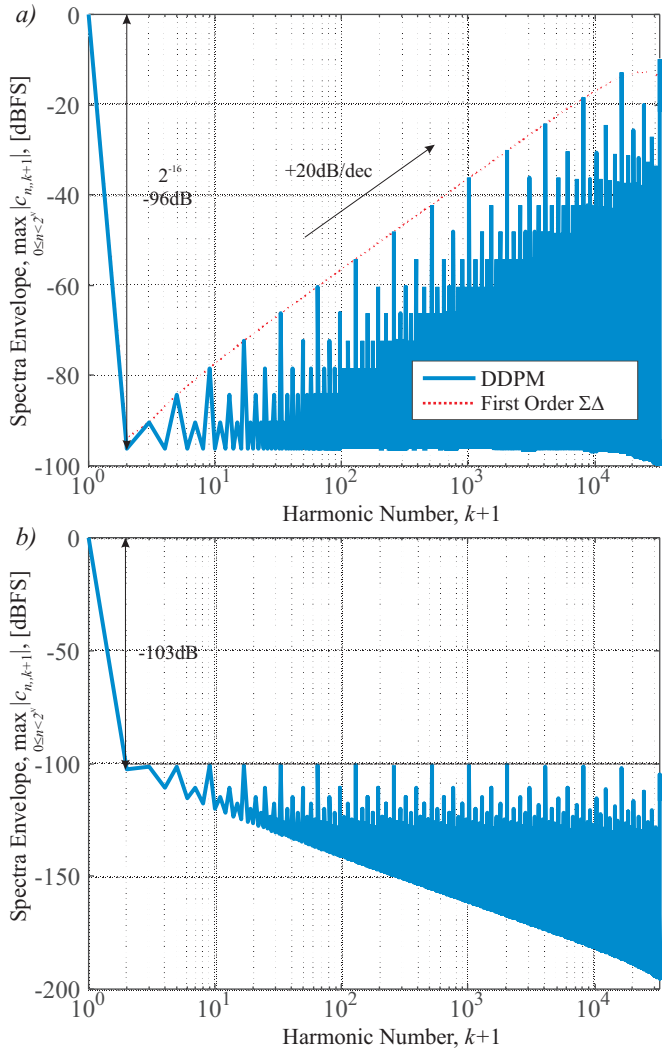

Fig. 6. Dyadic Digital Pulse Modulation, $N = 16$ bit resolution: a) envelope of the spectra of the 2^{16}, 2^{16}-time-slot-long DDPM streams and of the 2^{16}, streams including the output of a single-bit, first-order, digital $\Sigma\Delta$ modulator for a dc input ranging from 0 to $2^{16} - 1$ (first 2^{16} time slots), b) DDPM spectra envelope in a) filtered by the first-order LPF designed following (12).

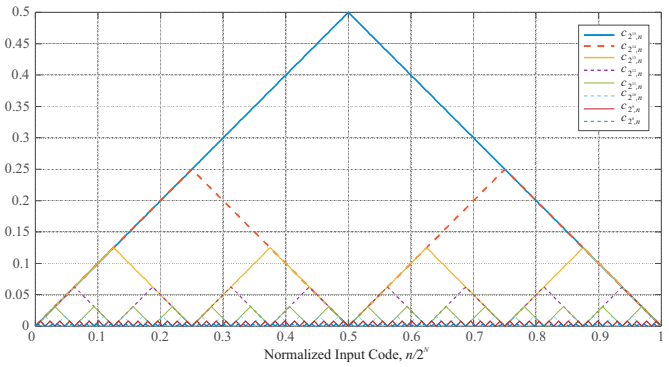

Fig. 7. Dyadic Digital Pulse Modulation (DDPM), Harmonic coefficients $c_{k,n}$ for $k = 2^p$ with $p \in [8, 15]$, versus the normalized input code $\frac{n}{2^N}$ for $N = 16$ bit DDPM waveforms.

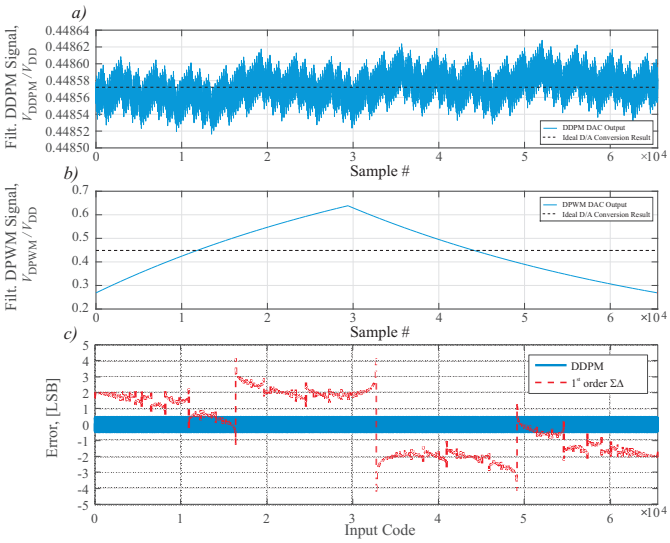

Fig. 8. Comparison of 16-bit DDPM (a) and DPWM (b) waveforms corresponding to the input code $n = 29398$ (0x72D6, normalized decimal value: 0.448577) filtered with a LPF designed following (12) and (c) comparison of the errors in the filtered output voltage sampled at time $2^N T_{\rm clk}$ vs. input code in a 16-bit DDPM DAC and in a first-order $\Sigma\Delta$ DAC with the same LPF.

On the basis of (9), the DC component ($k = 0$) of a DDPM waveform is $n/2^N \ V_{\rm DD}$ as expected and it is therefore suitable to be filtered to perform D/A conversion. Moreover, the contributions to the spectrum of the terms associated to the binary digits b_i, which are spaced by $2^i f_0$ and whose amplitude is scaled by 2^i, can be also noticed.

To discuss the requirements of the LPF needed to extract the DC component of a DDPM waveform for D/A conversion in quasi-static conditions, the envelope of the DDPM magnitude spectra for $0 \le n < 2^N$ is now considered in analogy with what presented in Section II for DPWM waveforms, and is plotted in Fig.6a for $N = 16$. Here, the 2^i-th harmonic components, corresponding to the powers of two $n = 2^i$, whose amplitude is increasing with frequency by 20dB/decade, are clearly visible. Such increasing behavior is opposite to that observed in Fig.3 for DPWM spectra, and can be found in the envelope of the spectra of first-order, single-bit, digital $\Sigma\Delta$ streams[4] [30] for constant inputs ranging from 0 to $2^N - 1$, which is plotted in Fig.6a for comparison. Unlike in $\Sigma\Delta$ streams, however, the spectral content of DDPM waveforms is concentrated for all codes at dominant dyadic harmonics $k = m \cdot 2^{N-h}$, with $m, h \in \mathbb{N}$ for small values of $h > 0$. This can be also noticed in Fig.7, where the dominant harmonic coefficients $c_{k,n}$ for $k = 2^p$ with $p \in [8, 15]$, are plotted versus the input code n.

Looking at Fig.6a, a LPF which attenuates the fundamental at f_0 of only 6dB and with an attenuation increasing with frequency by at least 20dB/dec is sufficient in a DDPM DAC to reject the harmonic content of DDPM signals below the quantization error threshold $\varepsilon = V_{\rm DD}/2^{N+1}$ for any input code n. These requirements are easily met by a first-order

[4]For a fair comparison with DDPM, the spectra of the first-order $\Sigma\Delta$ streams have been evaluated taking the first 2^N clock cycles.

LPF with a voltage transfer function

$$H(f) = \frac{1}{1 + \jmath\frac{f}{f_c}} \quad \text{where} \quad f_c = \frac{f_0}{\sqrt{3}} \tag{12}$$

as shown in Fig.6b, where the envelope of the DDPM spectra considered in Fig.6a and filtered by such a LPF is reported.

Comparing (12) and (5), which summarizes the requirements of a filter for a DPWM DAC, a first-order ($P = 1$) filter, with a corner frequency $2^{N+1}/(\pi\sqrt{3})$ times higher than that needed for a DPWM DAC, is suitable to a DDPM DAC with the same resolution and operated at the same clock frequency: it means that a 16-bit DDPM DAC operated at $f_{\rm clk} = 1\,\text{GHz}$, requires just a simple RC output LPF with a corner frequency of about $10\,\text{kHz}$, which can be implemented by a capacitor of $20\,\text{pF}$ and a resistor of about $1\,\text{M}\Omega$ and can be conveniently integrated on silicon requiring an area of less than $2,000\,\mu\text{m}^2$ in a 40nm CMOS technology.

The same LPF would be completely not effective to reject the AC component of a DPWM signal, as shown in Fig.8a-b, where the time-domain DDPM and DPWM waveforms corresponding to the same input code $n = 29398$ after filtering are shown. A LPF with a corner frequency of $0.4\,\text{Hz}$, i.e. more than 20,000 times lower, not suitable to integration, would be required for a 16-bit DPWM DAC operated at the same clock frequency. Moreover, from Fig.8c, it can be observed that for almost all input codes n, the error in the filtered output of a DDPM DAC, sampled at time $t = 2^N T_{\rm clk}$ from the beginning of the conversion, is significantly less than in a first-order, single-bit $\Sigma\Delta$ DAC with the same LPF designed as in (12).

D. Time Varying DDPM-Modulated Signals

While DDPM-based D/A conversion in quasi-static conditions has been considered thus far, the spectral characteristics of a DDPM modulated signal corresponding to a generic input sequence s_p of positive integers represented on N bits is now considered. With the notations introduced above, such a sequence can be associated to a DDPM waveform

$$v_{\rm s}(t) = \frac{V_{\rm DD}}{2^N} \sum_{m=-\infty}^{+\infty} x_{s_m}(t)\Pi\left(\frac{t}{T_0} - \frac{1}{2} - m\right) \tag{13}$$

where $x_{s_m} = x_n|_{n=s_m}$ and x_n is defined in (8), with a spectrum

$$V_{\rm s}(f) = \sum_{k=-\infty}^{+\infty} C_k\left(fT_0\right) V_{\rm ZOH}\left(fT_0 - k\right) \text{sinc}\left(\frac{k}{2^N}\right) \tag{14}$$

where

$$V_{\rm ZOH}(\xi) = V_{\rm DD}\,\text{sinc}\left(\xi\right) \text{e}^{-\jmath\pi\xi}, \tag{15}$$

$$C_k\left(\xi\right) = \sum_{m=-\infty}^{+\infty} c_{k,s_m} \text{e}^{-\jmath 2\pi\xi m} = \text{DTFT}_m\left\{c_{k,s_m}\right\}(\xi) \tag{16}$$

and $c_{k,s_m} = c_{k,n}|_{n=s_m}$ where $c_{k,n}$ are defined in (10).

It can be observed that the term of the sum in (14) for $k = 0$ is the spectrum of the ideal zero-order hold (ZOH) signal resulting from the conversion of the sequence s_p by an N-bit multilevel DAC [31]. Moreover, the spectral contributions due to the terms of the sum for $k \neq 0$ are centered around frequencies kf_0 and their amplitude is related to the coefficients $c_{k,n}$ defined in (10). Since such coefficients are relevant only for $k \gg 1$, as shown in Fig.7, the spectrum of a DDPM signal is similar to the spectrum of a ZOH signal up to the first multiples of the sampling frequency.

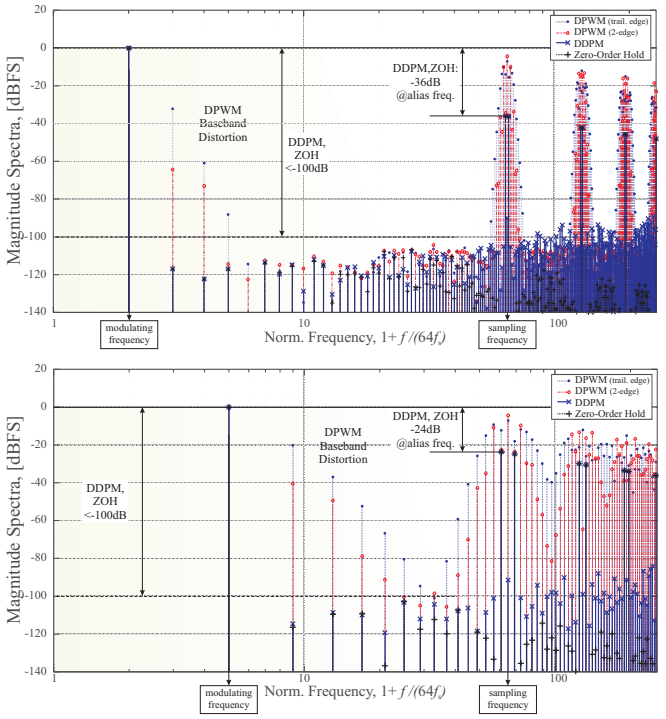

Fig. 9. Comparison of the spectra of $N = 16$ bit DDPM, trailing-edge DPMW, double-edge DPMW, and by zero-order hold (ZOH) modulated sequences corresponding to a full swing sine-wave sequence sampled with 64 (top) and 16 (bottom) samples per period.

To illustrate the spectral properties of a DDPM modulated signal in a special case, a full-swing, uniformly sampled sine wave input sequence quantized over $N = 16$ bits, is now considered. The spectra of the corresponding DDPM-modulated signals sampled at 64 and 16 samples per period are compared in Fig.9 with the spectra of the ZOH, of the trailing-edge DPWM and of the double-edge DPWM signals associated to the same sequence.

It can be appreciated that, unlike DPWM modulations, whose spectral characteristics are analyzed in [28], DDMP does not give rise to baseband signal harmonic distortion and to sideband spectral components and all spurious under the Nyquist frequency are more than 100dB below the fundamental. Moreover, the spectrum of the DDPM signal is similar to that of the ideal ZOH signal up to the first multiples of the sampling frequency f_0, as expected from (14), while its harmonic content increases with frequency as in Fig.6a.

The requirements of the reconstruction filter for a DDPM DAC with time-varying inputs are therefore the same discussed in the literature for an ideal ZOH signal [31] and are less stringent compared with DPWM. In particular, for an N-bit DAC, a P-th order LPF with a corner frequency f_c so that

$$\left|\text{sinc}\left(\frac{f_0 - 2f_c}{f_0}\right)\left(\frac{f_c}{f_0 - 2f_c}\right)^P\right| \simeq \frac{2}{\pi}\left(\frac{f_c}{f_0}\right)^{P+1} < \frac{1}{2^{N+1}}$$

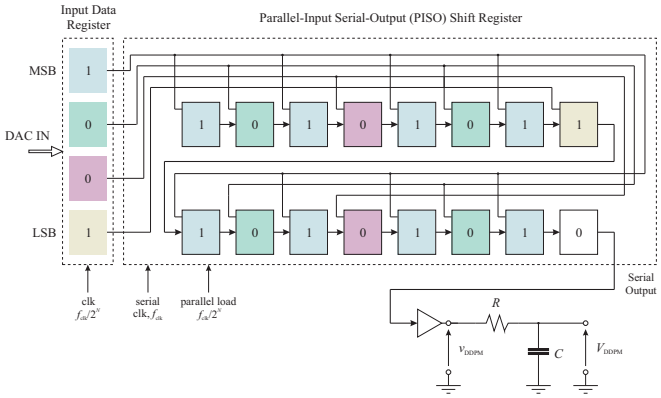

Fig. 10. Implementation of a 4-bit DDPM modulator using a PISO register.

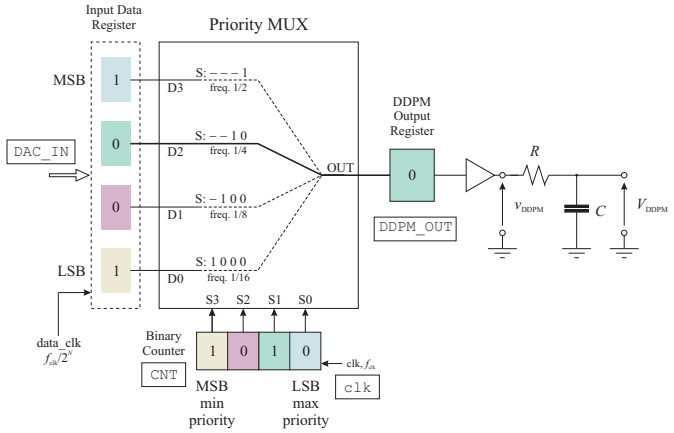

Fig. 11. Implementation of an $N = 4$ bit DDPM modulator based on a priority multiplexer (variables appearing in the VHDL code of Fig.12 are reported in frames.)

is required. In particular given the order P of the filter, its corner frequency should be

$$f_c < \sqrt[P+1]{\pi}\, 2^{-\frac{N+2}{P+1}} f_0. \tag{17}$$

The requirement (17) for $P = 1$ is more stringent than (12) derived under quasi-static conditions since an increased attenuation is needed to reject the ZOH-like spectral components of a DDPM signal at the first alias frequency. Nonetheless, to get accurate 2^N-level-quantized voltages proportional to a sequence of input codes (i.e. to retrieve the ZOH signal in itself, rather than its baseband component), as often needed in MD/DA AIs [7], the output filter of a DDPM DAC can be designed considering the less stringent quasi-static requirement (12) rather than (17).

The reconstruction filter requirements (17) can be further released by oversampling, interpolation, and noise-shaping techniques proposed for DPWM DACs [29]. While these aspects will be addressed in future work, the hardware implementation of a DDPM-based DAC is discussed in the following.

IV. DDPM Modulator Hardware Architecture

The feasibility and the practical value of a DDPM-based integrated DAC is strongly related to the possibility to generate DDPM sequences Σ_n using a simple digital architecture like the DPWM modulator in Fig.2b. To this purpose, the hardware (HW) implementation of a DDPM modulator is now addressed.

Considering how orthogonal dyadic sequences are arranged in a DDPM pattern, a simple DDPM modulator can be implemented by a parallel-input-serial-output (PISO) 2^N bit shift register as shown in Fig.10. The content of the register is loaded from the parallel inputs, which are hardwired to the outputs of the data register according with the DDPM pattern in Fig.5, at the data rate $f_0 = f_{\rm clk}/2^N$ and it is shifted to the serial output at the clock frequency $f_{\rm clk}$. This architecture does not require any combinational logic and is therefore suitable to operate at a very high clock rate. Nonetheless, since a 2^N-bit PISO register is needed, its implementation is impractical and area-consuming for a resolution higher than 5-6 bits.

To address the limitations of the DDPM modulator in Fig.10, a different implementation is proposed in Fig.11. Such

```
process (clk)
variable INDEX : integer := N;
variable DATA  : std_logic_vector(N downto 0);
begin
   if (clk'event AND clk='1')  then
      DATA := DAC_IN(N-1 downto 0) & '0';
      for i in N-1 downto 0 loop
         if CNT(i) = '1' then
            INDEX := i;
         end if;
      end loop;
   DDMP_OUT  <= DATA(N-INDEX);
   CNT <= CNT + '1';
   end if
end process
```

Fig. 12. Simplified VHDL Description of the DDPM Modulator in Fig.11.

an architecture, whose behavior is described in synthesizable behavioral VHDL in Fig.12, is based on a *priority multiplexer* (PMUX), i.e. a combinational network with $2{\cdot}N$ inputs, among which N data inputs $D_{N-1} \cdots D_0$ and N selection inputs $S_{N-1} \cdots S_0$, and one output X, described by the Boolean function

$$X = \sum_{i=0}^{N-1} D_{N-i-1} \cdot S_i \cdot \prod_{k=0}^{i-1} \overline{S_k}, \tag{18}$$

where sums and products are intended as Boolean OR and AND operators, respectively. In such a network, the digital output X takes the value of the bit D_{N-k} of the data input, being k the index of the first "one" in the selection inputs starting from the LSB, i.e. the index for which $S_k = 1$ and $S_i = 0$ for $i < k$, and it is assumed that $k = 0$ if all selection inputs are at zero.

The data inputs of the PMUX are fed by the DAC input data register, which samples the DAC input codes n at a rate $f_{\rm clk}/2^N$, while the selection inputs are connected to a free-running 2^N-bit binary counter operated at the clock frequency $f_{\rm clk}$. Considering such an architecture, every other clock period (i.e. 2^{N-1} times in a full count), $S_0 = 1$ and the output X takes the value D_{N-1} of the MSB of the input data. In the remaining counting periods $S_0 = 0$ and in one

half of the cases (i.e. 2^{N-2} times in a full count), $S_1 = 1$ and the output X takes the value of the second MSB D_{N-2} of the input. Applying the same approach recursively down to the LSB, the output X, which corresponds to the DDPM modulator output, is driven in a full counting period to the logical value of the bit D_i of the input exactly 2^i times, arranged according with the DDPM pattern in Fig.5.

Since, based on (18), a PMUX can be implemented by two-level logic with just $N + 1$ gates with an average fan-in of $(N + 1)/2$, the DDPM modulator in Fig.11 is well suited to be operated at a high frequency compared with $\Sigma\Delta$ DACs [30], which require power and area-consuming N-bit pipeline adders [32] for a high throughput. The DDPM modulator architecture in Fig.11 will be considered hereafter for performance assessment and experimental validation.

V. DDPM DAC Linearity and Noise

While the DDPM technique has been introduced thus far with reference to idealized digital waveforms, the main factors which may limit the static accuracy of an on-chip DDPM DAC - including non-instantaneous high-to-low and low-to-high transitions, power supply fluctuations and nonzero power supply impedance - are discussed in this Section.

A. Finite Switching Time and Double Slope Error

During transitions, the v_{DDPM} voltage waveform is mainly related to parasitics, in particular to the digital line capacitance, to the non-zero output resistance of the driver and to the input slope of the signal that triggers the transition. Depending on such factors, which affect rising and falling edges in a different way, the area of a digital pulse lasting k clock periods (dashed area in Fig.13a), can be expressed as

$$A_{\mathrm{P},k} = \int_0^{kT_{\mathrm{clk}}+t_{\mathrm{fall}}} v_{\mathrm{DDPM}}\mathrm{d}t = kT_{\mathrm{clk}}V_{\mathrm{DD}} + A^+ - A^- \quad (19)$$

and is in general different than the area $kT_{\mathrm{clk}}V_{\mathrm{DD}}$ of a rectangular pulse lasting k clock periods, by the area error $\Delta A = A^+ - A^-$. Such an error affects the mean value of real digital waveforms of a quantity $h\Delta A/T$, being h the number of rising/falling edge pairs (i.e. the number of standalone pulses) in a period T_0, possibly affecting the linearity of D/A conversion. In DPWM DACs, however, the impact of the pulse area error on linearity is small since DPWM waveforms include just one pulse per conversion period ($h = 1$). By contrast, this could be a concern in non-return-to-zero (NRZ) single-bit $\Sigma\Delta$ DACs [19-20] and also in DDPM DACs, where the number h of standalone pulses in a period depends on the input code and can be quite large.

Nonetheless, looking at the DDPM pattern in Fig.5, it can be observed that every other time slot in a period is assigned to the MSB, so that all digital inputs $n \in \left[0, 2^{N-1}\right)$ are associated to DDPM waveforms including n standalone "one" pulses, which are separated from each other by (at least) one MSB slot at zero, like in return-to-zero (RZ) DACs, as shown in Fig.13b. Hence, for any $n \in \left[0, 2^{N-1}\right)$ in a DDPM waveform, being $h = n$, the DDPM DAC static characteristic can be expressed as

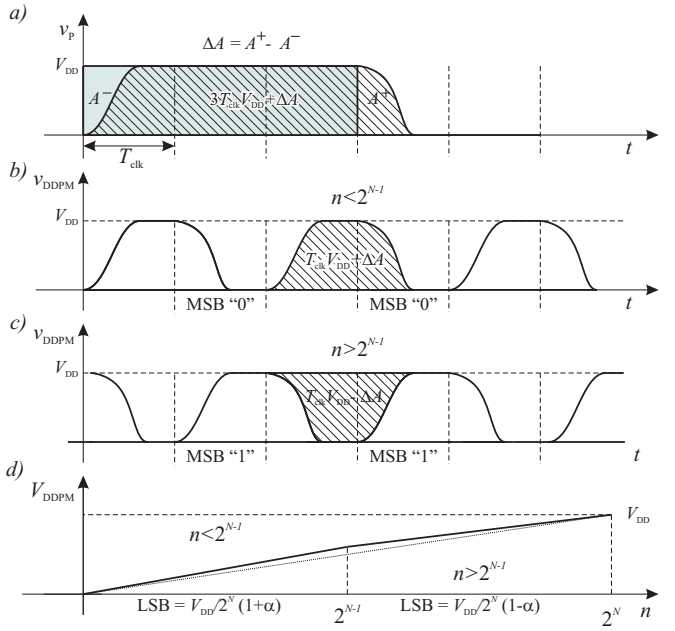

Fig. 13. Double slope error: a) Real vs. Ideal digital pulses: Area Error ΔA definition, b) incremental DDPM pulse (dashed) for $n \in [0, 2^{N-1})$ increasing of one unity, c) incremental DDPM pulse (dashed) for $n \in [2^{N-1}, 2^N)$ increasing of one unity, d) DDPM DAC static characteristic $V_{\mathrm{DDPM}}(n)$ showing double slope error (intentionally emphasized for illustration).

$$V_{\mathrm{DDPM}} = \frac{nV_{\mathrm{DD}}T_{\mathrm{clk}} + n\Delta A}{2^N T_{\mathrm{clk}}} = \frac{n}{2^N}V_{\mathrm{DD}}\,(1+\alpha) \quad (20)$$

and the pulse area error ΔA gives rise to a gain error $\alpha = \Delta A/(V_{\mathrm{DD}}T_{\mathrm{clk}})$ which does not impair the linearity of a DDPM DAC. Moreover, from Fig.13c, it can be observed that for $n \in \left[2^{N-1}, 2^N\right)$, MSB slots are at "one" and any increase by one unit in n corresponds to an additional pulse in the DDPM sequence which fills a gap between two next MSB slots[5], thus canceling a rising/falling edge pair and reducing the actual number of separate pulses by one unit. Considering that $h = 2^{N-1}$ for $n = 2^{N-1}$, for $n \in \left[2^{N-1}, 2^N\right)$ the number of separate pulses is given by $h = 2^N - n$ and

$$V_{\mathrm{DDPM}} = \frac{n}{2^N}V_{\mathrm{DD}}\,(1-\alpha) + \alpha V_{\mathrm{DD}}. \quad (21)$$

As a consequence, also for input codes $n \in \left[2^{N-1}, 2^N\right)$, the pulse area error ΔA considered so far gives rise to a gain and offset error but does not impair the linearity of the DAC. Considering both (20) and (21), however, for $\Delta A \neq 0$ the characteristic of the DAC is piecewise linear, changing its slope in correspondence of $n = 2^{N-1}$. The *double slope error* highlighted so far can be fully compensated by pre-processing the input data. To this purpose, being n the actual value to be converted, the input code n'

$$n' = \begin{cases} \left\lceil \frac{n}{1+\alpha} \right\rfloor & \text{for} \quad 0 \le n < 2^{N-1}(1+\alpha) \\ \left\lceil \frac{n-2^{N-1}\alpha}{1-\alpha} \right\rfloor & \text{for} \quad 2^{N-1}(1+\alpha) \le n < 2^N \end{cases} \quad (22)$$

where $\lceil\cdot\rfloor$ is the rounding operator to the closest integer, should be applied as an input code of the DAC.

[5]In this range, the DDPM DAC can be regarded as a return-to-one DAC.

B. Power Supply Fluctuations

While a constant power supply voltage $V_{\rm DD}$ has been assumed so far, the power supply of digital circuits can be affected by fluctuations due to noise, interference and also to the current absorbed by the same DAC, that is translated into a power supply voltage drop by the nonzero impedance of the PCB and on-chip power network. In order to analyze the effects of power supply variations, it is now assumed that the supply voltage can be expressed as:

$$v_{\rm DD}(t) = V_{\rm DD} + v_{\rm dd}(t) \tag{23}$$

being $V_{\rm DD}$ the nominal DC value of the supply voltage and $v_{\rm dd}(t)$ a time-varying fluctuation related to noise and other unwanted effects. Limiting the analysis, for the sake of simplicity, to a constant input code n (i.e. a periodic DDPM), based on (7) and (9), the error on a DDPM waveform due to power supply fluctuations $v_{\rm dd}(t)$ can be expressed as

$$v_{\rm ddpm}(t) = v_{\rm dd}(t) \sum_{k=-\infty}^{+\infty} x_n(t - 2^N k T_{\rm clk}) \tag{24}$$

and its spectrum

$$V_{{\rm ddpm},n}(f) = \sum_{k=-\infty}^{+\infty} c_{k,n} V_{\rm dd}\left(f - k f_0\right), \tag{25}$$

where $V_{\rm dd}(f)$ is the Fourier Transform of $v_{\rm dd}(t)$, includes a DC component

$$\delta V_{{\rm DDPM},n} = V_{{\rm ddpm},n}(0) = \sum_{k=-\infty}^{+\infty} c_{k,n} V_{\rm dd}\left(k f_0\right) \tag{26}$$

which corrupts the mean value $V_{{\rm DDPM},n}$ associated to the input code n, with an error related to the spectral components of the fluctuations $v_{\rm dd}(t)$ at the harmonics of f_0. Such an error, which can be deterministic or random depending on the nature of $v_{\rm dd}(t)$, will be analyzed in what follows.

C. Deterministic Supply Fluctuations - Multiple Slope Error

Considering power supply fluctuations which are deterministic and periodic with the same period of the DDPM signal, like those due to the voltage drop on the power supply impedance induced by the current absorbed by the DDPM DAC, (25) can be written as

$$\delta V_{{\rm DDPM},n} = V_{{\rm ddpm},n}(0) = \sum_{k=1}^{+\infty} 2\Re\{c_{k,n} V_{\rm dd}\left(k f_0\right)\} \tag{27}$$

being $\Re\{\cdot\}$ the real part operator. Taking into account of the dependance on k and n of the coefficients $c_{n,k}$ illustrated in Fig.7, it can be observed that the more relevant contributions to the sum in (27) are those related to dominant dyadic harmonics $k = m \cdot 2^{N-h}$ with $m, h \in \mathbb{N}$ and small values of $h > 0$ and the magnitude of such contributions is a piecewise linear function of the input code n, showing 2^h triangular oscillations for $0 < n < 2^N$.

As a consequence, the systematic error highlighted in (27) is globally a piecewise linear function of n, where the main slope changes occur in correspondence of input codes n integer multiples of 2^{N-h} for a small $h > 0$ and corrupts the ideal characteristics of a DDPM DAC with a gain error that depends on the input code interval and can be therefore defined as *multiple slope error*, in analogy with the double slope error considered in Section IVa. Such an error can be fully compensated by digital pre-processing, by the same approach illustrated in (22), dividing the input range into $m = 2^p$ sub-ranges, calculating different slope correction factors α_i, $i \in [1, m]$ on the basis of best linear fit of the uncalibrated DAC characteristics over each sub-range, and applying such correction factors to the input code, i.e. applying an input

$$n' = \left\lceil \frac{n - (i-1)\, 2^{N-p} \alpha_{i-1}}{1 + \alpha_i} \right\rceil \quad \text{for} \quad n \in \left[(i-1)\cdot 2^{N-p}, i \cdot 2^{N-p}\right),\ i \in [1, m] \tag{28}$$

being n the actual value to be converted.

D. Random Noise

As far as random supply fluctuations are considered in (26), the standard deviation of noise-induced errors in the output voltage can be expressed as

$$\sigma_{\delta V_{\rm DDPM},n} = \sqrt{\frac{n^2}{2^{2N}} S_{V_{\rm dd}}(0) + \sum_{k=1}^{+\infty} c_{k,n}^2 S_{\rm V_{dd}}\left(k f_0\right)} \tag{29}$$

where $S_{\rm V_{dd}}\left(k f_0\right)$ is the power spectral density (PSD) of supply noise, assumed to be stationary.

In (29) two contributions can be highlighted: the first is related to the low-frequency noise PSD, the second is related to the noise PSD at higher DDPM harmonics. While the first contribution increases with the input code n, the second term, if a constant noise PSD (white noise) is assumed, is dominated by the term including $c_{2^{N-1},n}$, which increases for $n < 2^{N-1}$ and decreases for higher codes, as depicted in Fig.7. As such, according with (29), the overall noise standard deviation is related to the input code and increases with n for $n < 2^{N-1}$, while it remains almost constant for $n > 2^{N-1}$, where the increasing contribution of the first term is balanced by the decreasing contribution of the second.

VI. FPGA Prototype and Experimental Results

To validate the DDPM technique proposed in this paper, a 16-bit DDPM DAC prototype has been synthesized on FPGA and its static performance has been measured. Experimental results will be discussed in this section, after a short introduction on the prototype implementation and on the test setup.

A. FPGA-based DDPM DAC and Test Setup

A 16-bit DDPM modulator based on the architecture in Fig.11 has been synthesised starting from its VHDL description on an Altera Cyclone IV FPGA mounted on the DE2-115 evaluation board, so that to drive a $1.8\,\mathrm{V}$ digital output with a DDPM signal. The synthesised DDPM DAC required only 53 FPGA logic elements (to be compared with 55 logic elements needed for a 16-bit DPWM modulator based on the architecture in Fig.2b), operates at a clock frequency of $100\,\mathrm{MHz}$

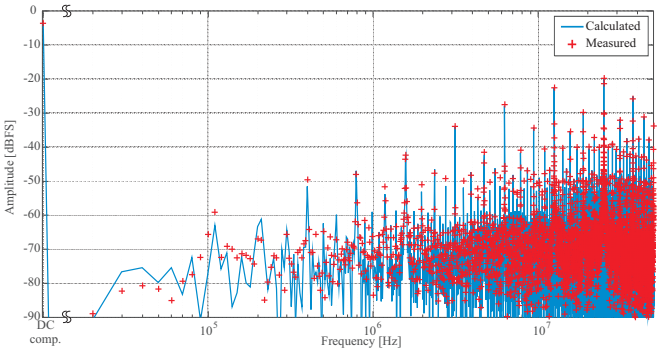

Fig. 14. Spectrum of an unfiltered 16-bit, 100MHz DDPM signal corresponding to the input code $n = 43690$ (0xAAAA), calculated on the basis of 9 (a), and measured, taking the FFT of the output voltage of the FPGA-based prototype acquired by a digital oscilloscope.

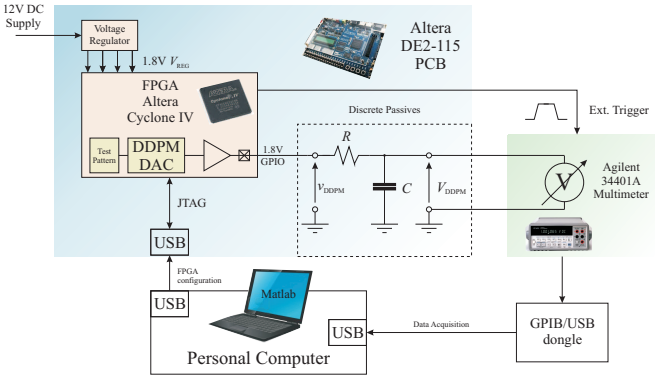

Fig. 15. Experimental test setup used to measure the static conversion characteristic of the DDPM DAC FPGA prototype.

corresponding to a sample rate $f_0 = f_{\rm clk}/2^N = 1.526\,\text{kHz}$ and includes an on-board output RC filter [6] with $R = 180\,\text{k}\Omega$ and $C = 1\,\text{nF}$, designed for a corner frequency of about $880\,\text{Hz}$ in accordance with (12).

The unfiltered output voltage of the FPGA-based DDPM modulator for the input code $n = 43690$ (0xAAAA) has been acquired by a digital oscilloscope and its spectrum, evaluated from the Fast Fourier Transform (FFT) of the acquired waveform is compared in Fig.14 with the DDPM spectrum calculated on the basis of (9).

Moreover, the DAC static characteristic $V_{\rm DDPM}(n)$ has been measured with the test setup in Fig.15. Here, the FPGA, on which the DDPM DAC under test is synthesized, is configured to periodically increment the DAC input code by one unit, from 0x0000 up to 0xFFFF, and to generate a triggering pulse signal every 2s. At each triggering pulse, four samples of the filtered DDPM output of the DAC are measured by a 6.5-digit digital multimeter Agilent 34401A and are forwarded via a general purpose interface bus (GPIB) to a PC running an acquisition procedure developed in the Matlab environment. The measurement of the full DDPM DAC characteristic took about 36 hours.

B. Experimental Results and Discussion

Based on the experimental DDPM DAC transfer characteristics $V_{\rm DDPM}(n)$, the integral nonlinearity error

$$\text{INL}(n) = \frac{V_{\rm DDPM}(n) - \beta\, n - V_{\rm OFF}}{\text{LSB}_{16}}, \qquad (30)$$

where β (ideally $V_{\rm DD}/2^N$) and $V_{\rm OFF}$ (ideally zero) are the coefficients of the best linear fit of the measured data, $\text{LSB}_{16} = V_{\rm DD}/2^{16} = 27\mu\text{V}$ is the least significant bit at 16-bit resolution, and the differential nonlinearity error

$$\text{DNL}(n) = \text{INL}(n+1) - \text{INL}(n) \qquad (31)$$

[6]The clock frequency and of the values of the filter components for the prototype have been chosen considering the PCB implementation (PCB parasitics, external digital drivers, discrete components ...). Different choices (e.g. higher clock frequency and lower filter capacitance and/or resistance) would be surely more appropriate for an on-chip implementation and will be considered in future work.

have been evaluated and are reported in Fig.16 and Fig.17, respectively.

In Fig.16, in particular, both the raw INL characteristic of the converter and the characteristics obtained with the digital compensation of the double-slope and of the multiple-slope errors are shown.

It can be observed that the uncompensated INL shows a triangular shape due to the double slope error, as described in Section IV, and reaches a peak value of about 110 LSBs, corresponding to a gain error $\alpha = 4.48 \cdot 10^{-3}$ in (20) and limiting the effective number of bits (ENOB) of the converter over the whole range to about 8.5. After the digital compensation of the double slope error, performed as in (22), the peak INL is reduced to about 15 LSBs and the ENOB of the converter raises to 12.1. The same INL can be obtained without calibration, using only one half of the input range of the DAC, leading, in this case, to an ENOB of 11.1.

It is interesting to observe that the INL characteristic after the compensation of the double slope error still includes a systematic piecewise linear component, denoting the effect of the multiple slope error discussed in Section IVc. After the compensation of the multiple slope error over $m = 16$ intervals by (28), the measured INL does not include systematic components any more, is less than 2 LSB for almost all codes and an ENOB of 15.4 is obtained. It is worth noting that the quite large uncompensated INL of the FPGA prototype can be related to the fact that a standard digital output, not optimized for symmetric edges, is employed and its operation is affected by a significant capacitive load at PCB level (ESD protections, pads, PCB traces,...). A better performance without compensation is expected in an on-chip implementation.

In Fig.17, the measured DNL of the converter is reported (blue dots) for each input code. It can be observed that almost all measured values are in the $\pm$1LSB range. Moreover, the standard deviation σ of the four samples acquired in sequence for the same input code has been considered to highlight the impact of random noise in this measurement and the $\pm 3\sigma$ bounds are reported in the same figure. Since almost all DNL values lie between the $\pm 3\sigma$ bounds, the results of the measurement are dominated by random noise, being the actual systematic differential nonlinearity of the converter

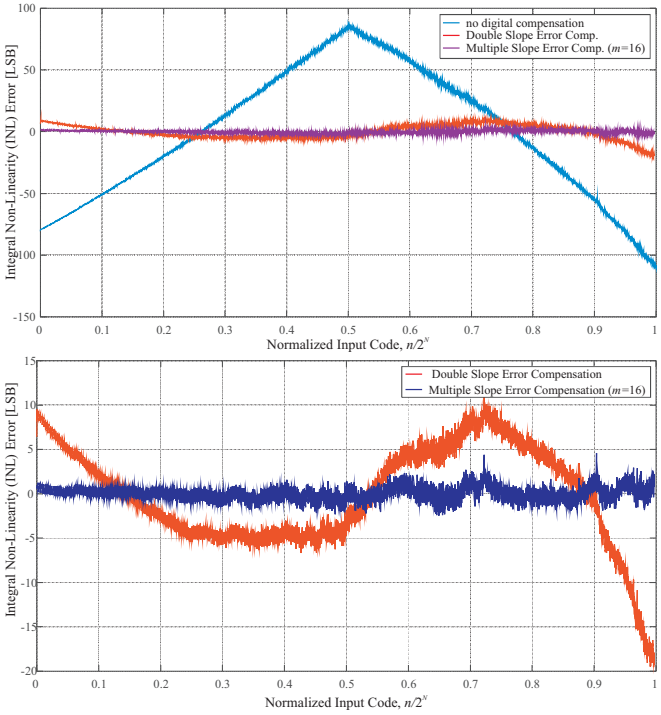

Fig. 16. Integral Nonlinearity Error (INL) expressed in LSB_{16}, for the uncompensated DDPM DAC, with double slope error compensation and with 16-segment multiple slope error compensation. In the bottom figure a detail of the top figure is reported.

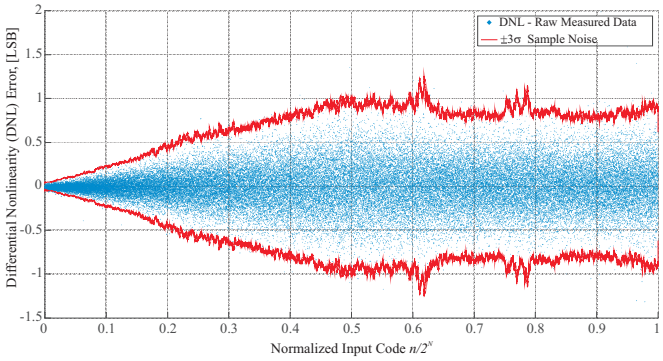

Fig. 17. Measured Differential Nonlinearity Error (DNL) expressed in LSB_{16} of the DDPM DAC.

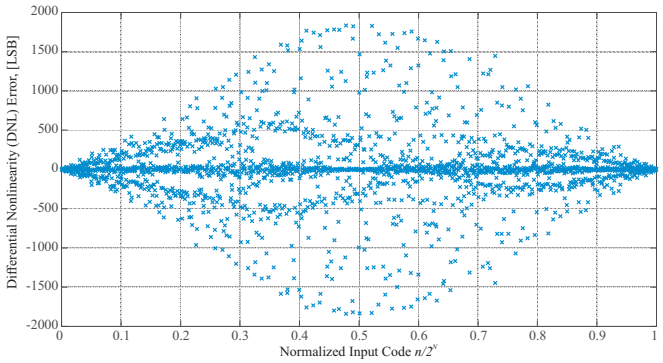

Fig. 18. Measured Differential Nonlinearity (DNL) in LSB_{16}, obtained as in (31), from the measured static characteristic $V_{\mathrm{DPWM}}(n)$ of a 16-bit DPWM DAC with the same output filter of the proposed DDPM DAC.

significantly better.

It can be also observed that the measured standard deviation increases with the input code up to $n = 2^{N-1}$ and remains substantially constant - and equal to about 0.3 LSBs - for higher codes. This is in qualitative agreement with what it is expected for a DDPM DAC in the presence of random noise on its power supply voltage, considering (29) and the following discussion in Section IVd.

C. Comparison with DPWM and state-of-the-art techniques

In order to highlight the effectiveness of the proposed DDPM technique, a 16-bit DPWM modulator, based on the architecture in Fig.2b has been synthesized on the same FPGA and using the same output LPF of the DDPM DAC prototype and its static characteristic $V_{\mathrm{DPWM}}(n)$ has been measured by the same test setup. In Fig.18 the result of the DNL measurement, obtained as in (31), is reported. It can be observed that the error, not properly due to nonlinearity but rather to the large ripple of the DPWM output voltage, not sufficiently filtered and randomly sampled by the multimeter, can be as large as ± 2000 LSBs for the worst-case input codes close to 2^{N-1}. Such a value limits the ENOB to about 4 bits and is in agreement with the discussion in Section II. To obtain approximatively the same performance of the calibrated DDPM DAC reported in Fig.17, an output filter with a corner frequency of $0.04\,\mathrm{Hz}$ (e.g. with $R = 2.7\,\mathrm{M}\Omega$ and $C = 1.8\,\mu\mathrm{F}$) would be required. Using such a filter, however, the DAC would settle to the target 16-bit accuracy in about 6 minutes so that to be impractical not only for a fully integrated, but also for a PCB implementation and its characterization.

The results of the measurements performed on the FPGA prototype and reported so far are summarized in Tab.I and give a clear picture of the advantages of DDPM over DPWM as a high resolution D/A conversion technique suitable to address the requirements of high-resolution, low cost D/A conversion in MD/DA AIs.

VII. Conclusion

In this paper, the novel Dyadic Digital Pulse Modulation (DDPM) technique has been proposed to overcome the limitations - mainly related to the output filter requirements - of digital pulse width modulation (DPWM) as a technique to perform on-chip D/A conversion in present day mostly digital and digital assisted analog interfaces. After the effectiveness of the DDPM approach is analytically demonstrated considering the spectral characteristics of DDPM modulated signals, the implementation of a DDPM modulator has been addressed and a compact DDPM modulator architecture has been proposed and described in VHDL. Moreover, the limitations to the static accuracy of a DDPM-based DAC due to the shape of real digital voltage waveforms and to fluctuations in the power supply voltage have been analyzed, showing how the DDPM technique is particularly well suited to achieve a good linearity. Finally, a prototype of a fully digital DDPM-based DAC has been synthesized on an FPGA and its main static performance have been measured and discussed.

TABLE I
EXPERIMENTAL RESULTS FOR THE DDPM AND DPWM DAC.

Param.	unit	DDPM			DPWM	
calibration segments		1	2	16	N/A	N/A
ENOB	bit	8.5 (11.1†)	12.1	15.4	4	$\simeq 16^{\S}$
INL	±LSB	110	15	< 2	4	-
DNL	±LSB	1	1	1	2,000	-
Logic Elements		53			55	55
Sample Rate	S/s	1,525			1,525	1,525
BW (3dB)	Hz	880			880	0.036
Settl. time	ms	7	9	11	3	$360 \cdot 10^3$
R	kΩ	180			180‡	2,700
C	nF	1			1‡	1,800

† achieved using only one half of the input swing ‡ DPWM DAC implemented using the same RC low pass filter used for the DDPM DAC considered in the first two columns § DPWM DAC with an RC filter designed according with (4) for a 16 bit resolution. Estimated data are reported since the measurement would be impractical.

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