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***Abstract*—This paper presents the physics-based variability analysis of multi-fin double-gate (DG) MOSFETs, representing the core structure of FinFETs for RF applications. The variability of the AC parameters as a function of relevant geometrical and physical parameters, such as the fin width, the fin separation, the source (drain)-gate distance and the doping level is investigated. The analysis exploits a numerically efficient Green's Function technique [1]-[2], extending to the RF case the linearized approach well known from DC variability analysis. The variability of a single fin DG-MOS transistor is compared to a more realistic structure with two fins and raised source/drain contacts, i.e. including both the active part of the FinFET and a significant amount of passive (parasitic) components at the device level. Although presently implemented in a 2D in-house software, the technique can be easily exported to standard 3D TCAD tools, e.g. for tri-gate FinFETs analysis.**

***Index Terms*—FinFET, Variability, Numerical simulations**

I. INTRODUCTION

FinFETs have become the leading devices for CMOS applications, allowing for a higher immunity to short channel effects with respect to their competitors (UTB-SOI). A significant key to the success of FinFETs relies in their 3D structure allowing for completely new scaling features and device architecture. Despite the enormous amount of work dedicated to the fabrication, optimization and modeling of these devices, comparably less effort has been dedicated to their AC characterization and modeling [3], although the interest towards analog RF and microwave applications fosters research in this field. The peculiar 3D structure of the device can obscure the RF advantages brought by the gate length reduction because of a considerable amount of parasitic capacitances and resistances [3] that have a milder effect, or are totally absent, in the standard MOS technologies. Since variability is known to significantly impact the DC device behavior, the same is expected for the AC performance, both at the active device and at the parasitics level. Furthermore the multi-fin structure used for RF FinFETs makes the separation of the device active and passive parts difficult already for the intrinsic device. In fact, some geometrical variations may have a small impact on the DC characteristics but affect the AC variability, e.g. through capacitances. It is therefore mandatory to devise reliable and efficient tools allowing for the evaluation of AC performance variations as a function of the most important physical parameters of the FinFET structure.

For accurate variability estimation, physics-based analysis through TCAD tools is the most important way to link a device performance variation to a physical or geometrical parameter variation ([1], [2] and references therein). Unfortunately, variability analysis through the so-called incremental approach, i.e. repeating the device analysis by changing the parameter within a prescribed range, usually corresponds to a highly intensive numerical effort and is especially difficult for devices with complicated geometries, like multiple fin devices, or with randomly distributed parameter fluctuations. A breakthrough has been the development of Green's Function (GF) based techniques, which rely on linearized model analysis and are hence extremely numerically efficient. Besides being approximated, the GF approach has been proven to be accurate for the DC device variability even for extremely scaled devices [1], [4]. Currently the GF approach is limited to the DC variational analysis, like the one implemented in Synopsys [4]. Recently a methodology extending the GF approach to the AC case has been presented [2], to evaluate the sensitivity of the AC admittance matrix with negligible numerical effort with respect to the ordinary device simulation time. While in [2] only test case structures are reported, in this paper we present preliminary results concerning the RF variability analysis of more realistic DG devices, as the preliminary step towards the complete FinFET variability analysis. A single fin device and a double fin one, including the finger cross-couplings and part of the raised source/drain and gate couplings, are compared. The variation of the AC admittance matrix elements is presented as a function of the fin width, drain extension length, source/drain doping and fin separation. Comparison with the incremental analysis shows that the proposed approach is valid up to 20% of variation of the parameters, hence validating the proposed approach.

II. GREEN'S FUNCTION APPROACH TO AC SENSITIVITY ANALYSIS

In this paper we exploit the physics-based AC sensitivity analysis introduced in [1]-[2]. The starting point is the Large Signal (LS) physics-based model in [5], allowing for Harmonic Balance based multi

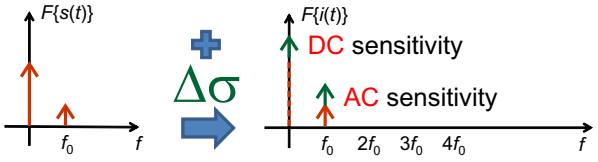

Fig. 1. Schematic representation of the variability modeling approach. $s(t)$ is a terminal applied voltage, $i(t)$ the terminal current, F the Fourier transform.

tone device simulation including efficient GF analysis capability. The physical model is solved with a small amplitude AC tone $V_{j,\mathrm{AC}}$ at frequency f_0 and each terminal j superimposed to DC bias. In principle all the harmonics nf_0 should be included in the simulation spectrum but the AC tone is so small that the analysis can be limited to $n = 0, 1$ (see Fig. 1): hence the extra numerical effort for the system solution is negligible with respect to the simple DC analysis. The solution returns the AC device currents $I_{k,\mathrm{AC}}$ at each terminal k, see Fig. 1, allowing for the direct evaluation of the AC admittance without any need of model linearization:

$$Y_{k,j} = \frac{I_{k,\mathrm{AC}}}{V_{j,\mathrm{AC}}}.$$

The system is then linearized to account for the change $\Delta\sigma$ of any given parameter σ: keeping the voltage sources at the terminals unchanged, the short circuit variation of the current phasor $\Delta I_{k,\mathrm{AC}}$, induced by $\Delta\sigma$, is recovered by the GF technique. Finally, the variation of the admittance matrix elements $\Delta Y_{k,j}$ is simply:

$$\Delta Y_{k,j} = \frac{\Delta I_{k,\mathrm{AC}}}{V_{j,\mathrm{AC}}}. \qquad (1)$$

Notice that the system, both the one with the nominal parameter σ and the one with variations, is solved with simultaneous DC and AC excitations (see Fig. 1): therefore, even though in this paper we will focus on the AC device response, it is worth noticing that the proposed GF approach allows for the simultaneous DC and AC variability analyses.

III. Case Study 1: Single Fin DG Device

The above analysis has been applied to a single fin DG structure, shown in Fig. 2, left, representing a 2D cross section of a tri-gate FinFET. The quantities to be varied are: the fin width (WF), the gate/source(drain) distance (LDE) and the source/drain (S/D) doping (DOP), see Fig. 2 for the exact definition and geometry. These parameters have been selected since they impact in particular the parasitic resistance of the fin, thus playing an important role in determining the RF device performances. With the aim of a possible development of a small-signal high gain or of a low noise amplifier for small-cell applications, the operating frequency has been fixed to 60 GHz and the bias condition is $V_{\mathrm{GS}} = 0.6$ V and $V_{\mathrm{DS}} = 1$ V corresponding to a drain current of 0.4 mA/mm.

In Fig. 3 the real part of the drain-gate element of the admittance matrix is plotted against the percentage

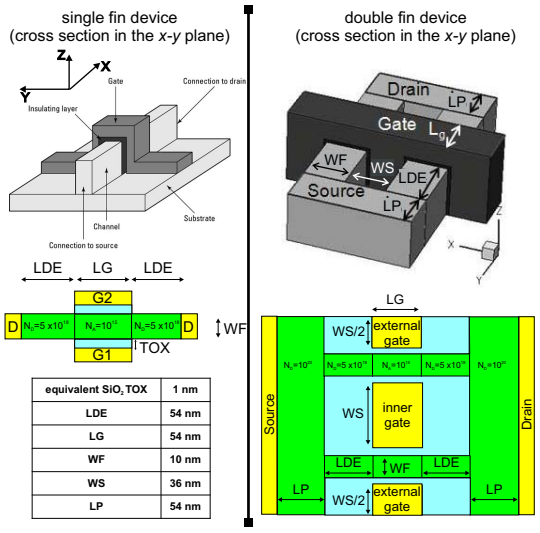

Fig. 2. Single fin DG MOSFET (left) and double fin DG structure (right). Green areas represent Si regions, the light blue SiO_2 and yellow the metal gates.

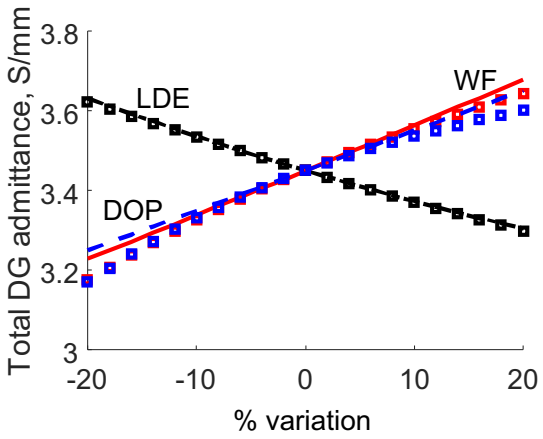

Fig. 3. Real part of the drain-gate admittance for the single fin DG device vs. parameter variations.

parameter variations (this element is of course related to the total transconductance). It is evident that nearly exact tracking of the variations is observed for both DOP and WF: the variation is significant and around 10%, thus suggesting that the parasitic resistance of the S/D region heavily affects the transconductance. Increasing DOP and WF reduces the parasitic resistance: the admittance variation is approximately linearly increasing with these quantities and with nearly the same slope. Of course, the opposite is observed with increasing the S/D-gate separation LDE. Notice that in this figure, and in the following Figs. 5-8, the contributions of the two gates are summed to emulate the FinFET behavior, where the two contacts are effectively shorted. For validation, the results from the GF approach are always reported compared to the much more computationally intensive incremental analysis (symbols in the figures). The accuracy of the GF approach is verified even for parameter variations up to 20% with respect to the nominal values.

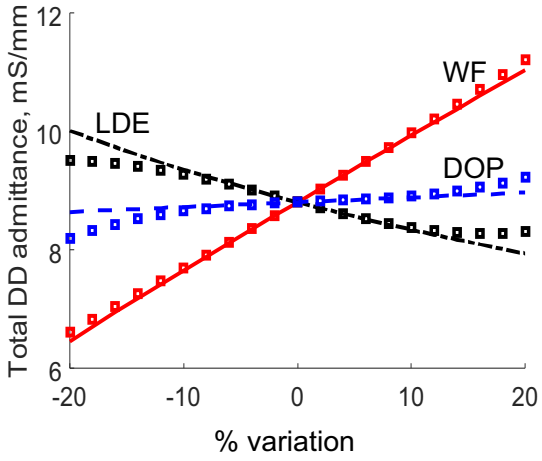

Fig. 4. Real part of the drain-drain admittance for the single fin DG device vs. parameter variations.

Fig. 4 shows the variation of the real part of the drain-drain element of the admittance matrix. Here as well the variation is quite significant. While the general trend is maintained with respect to the DG element, the effect of DOP is highly reduced while the WF effect is dominant. In fact, the dependency of the output conductance on DOP and LDE is just through the parasitic resistances and short channel effects. Remarkably, the DOP dependence is milder. A possible interpretation is that DOP reduces the parasitic resistance but increases the short channel effects: the two effects have opposite influence on the output conductance. Notice that this parameter, despite being quite negligible for digital applications, plays a significant role for analog applications.

Turning to the imaginary parts, Fig. 5 shows the capacitances of the gate-gate (top), gate-drain (middle) and drain-drain (bottom) elements, i.e. the imaginary part divided by the angular frequency. Notice that the percentage variation with respect to the nominal value is lower, limited to a few percent in the case of the gate-gate and gate-drain elements: this is due to the fact that the considered variations impact mainly on the parasitic capacitances which are in any case a small amount with respect to the total capacitance, dominated by the gate oxide. For the total GG capacitance WF and DOP variations are again closely correlated, suggesting that the parasitic source resistance dominates over the intrinsic access resistance, while the DG capacitance is less affected. The output capacitance, see Fig. 5, bottom, despite smaller, is known to be mostly a geometrical capacitance and has the most significant dependence on the parameter variation.

Finally, Fig. 6 shows the cut-off frequency behavior: f_T traces the transconductance variations, but the effect of the gate-gate capacitance makes the f_T spread limited to around 6 GHz in this case. Notice that the single fin device is stripped by most capacitive parasitics, that will be shown in the following, hence the cut-off frequency value is extremely high.

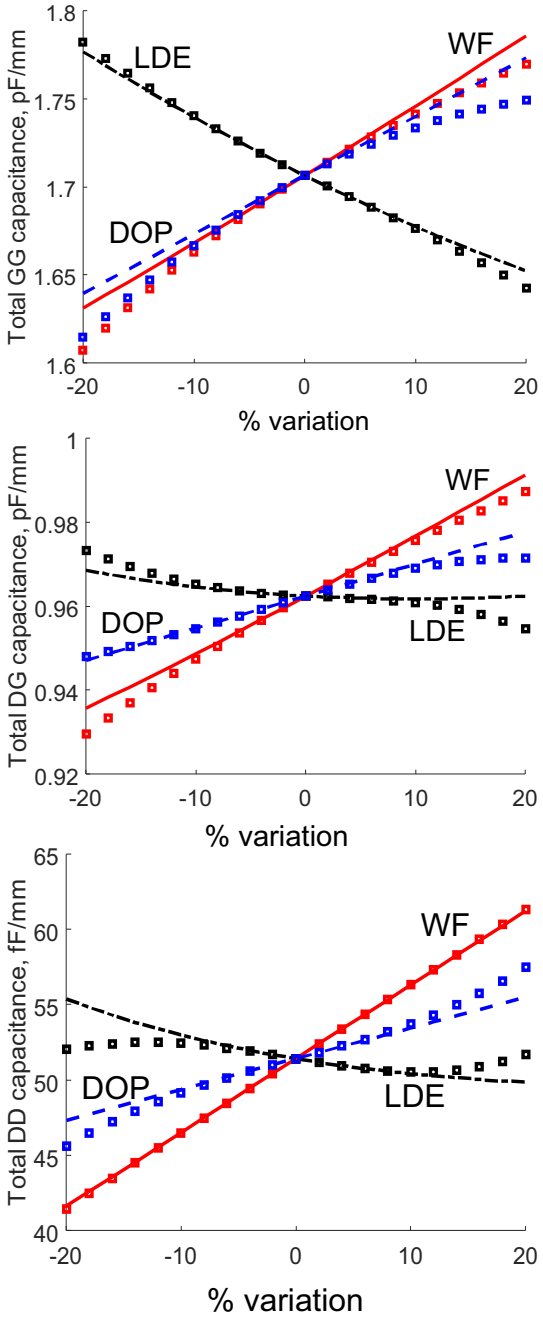

Fig. 5. Total gate-gate (top), drain-gate (middle) and drain-drain (bottom) capacitance of the single fin DG device vs. parameter variations.

IV. Case Study 2: Double Fin DG Device

To better highlight the capability of the proposed approach we consider here a two fin device, with the source and drain contacts joined to emulate the raised S/D contact of a realistic FinFET device, see Fig. 2, right. Here the geometry of the two intrinsic fins is the same as in the previous case. The DC drain current exhibits good scaling with respect to the single fin case, however this structure allows for the investigation of extra parasitics. In the multi-fin case the parasitic network identification through measurement deembeding or conformal mapping is a difficult and

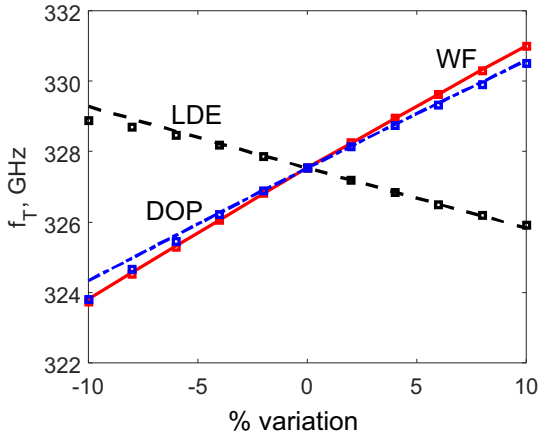

Fig. 6. Cut-off frequency of the single fin DG device vs. parameter variations.

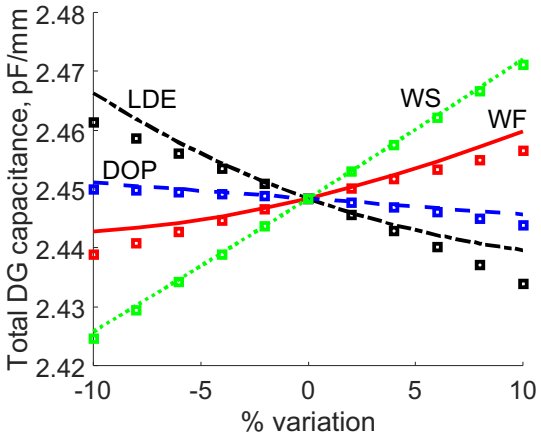

Fig. 7. Drain-gate capacitance of the two-fin DG structure.

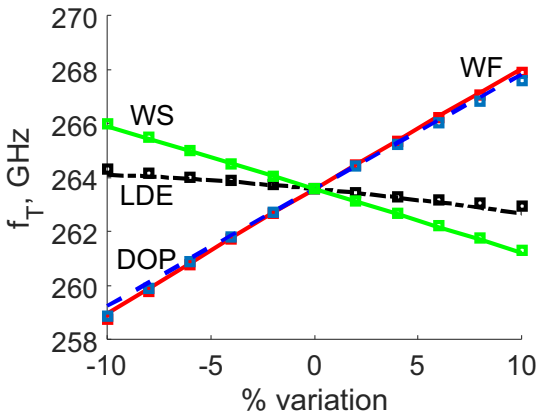

Fig. 8. Cut-off frequency of the two-fin DG device.

cumbersome task [3], [8], while TCAD tools are the ideal environment to simultaneously include all the peculiarities of these devices. In fact, the reduced size of the FinFETs allows for the concomitant simulation of the multiple fins together with the inner portion of their interconnects, as demonstrated e.g in the simulation of whole SRAM cells in DC [6], [7].

Turning to the variability analysis of the device in Fig. 2, besides the variations of WF, LDE and DOP like in the previous case, we address also the fin separation WS. Globally the capacitances of the double fin device are found to be higher than the ones of the stripped single fin case due to the sidewall source and drain regions. Comparing the total gate-gate and gate-drain capacitances of the two-fin DG MOS with the previous stripped device (scaled by an ideal factor of two), a rough estimate of 0.5 pF/mm for each side of the gate (source/drain) can been made: this amount adds to the drain-gate capacitance and double of it (source+drain) to the total gate-gate capacitance. While this is just a crude estimation found by comparison of the two devices, the capacitance found from TCAD is instead accurate. It includes all fringing effects and their (possibly complicated) dependency on the geometry. The same is true for the variation analysis. Here only selected results are shown for brevity. Fig. 7, for example, shows the drain-gate behavior: unlike the case of the stripped device, here the fin width separation WS and LDE play a major role with respect to DOP and WF, hence highlighting the strong influence of the parasitic capacitance. Finally Fig. 8 shows the cut-off frequency as a function of all parameters. Here the effect of WS is found to be close to that of WF and DOP, showing the complicated interconnection of the transconductance variations combined with the total gate capacitance, which increases with WF, WS and DOP and decreases with LDE (not shown for brevity).

V. Conclusions

We have demonstrated an efficient TCAD tool for the FinFETs AC variability analysis. The variability of a single and double fin DG MOSFETs have been presented with focus on the parasitics affecting the RF behavior. The source/drain parasitic resistance variability has a significant impact both on the single fin transconductance and output conductance, and on the gate capacitance. The double fin structure is heavily affected by the extra gate-source (drain) capacitances and the fin width separation becomes the dominant variability source, especially compared to the gate-source (drain) separation. Other possible geometries will be considered in the full paper.

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