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Behavioral Macromodels of Differential Drivers with Pre-Emphasis

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Abstract

This paper addresses the extension of the behavioral modeling via parametric relations to differential drivers with pre-emphasis. These devices are of paramount importance to enable multi-gigabit data transmission over conventional copper interconnects. The proposed models preserve the accuracy and efficiency strenghts of behavioral parametric macromodels for conventional devices. Their operation is demonstrated in a realistic simulation example involving a 3.125 Gb/s commercial driver with pre-emphasis.

1 Introduction

Nowadays, a cost effective solution for the transmission of signals in the Gb/s range relies on the pre-conditioning of signals sent on the usual interconnect data links. Pre-conditioning is aimed at enhancing the high-frequency components of the transmitted signals, in order to compensate for the low-pass distortion effect of interconnects. These techniques arise from communication and signal processing theory and give rise to driver devices with pre-emphasis features as well as to sophisticate solutions based on channel equalization. High-performance differential data links based on these solution have been successfully demonstrated in [1, 2, 3, 4].

On the other hand, the increasing complexity of driver and receiver circuits demands for accurate and efficient models to be used in system-level simulations aimed at the assessment of data link performance and signal integrity effects. In this study, the state-of-the-art Mπlog approach for the behavioral macromodeling of digital devices, discussed in [5, 6, 7, 8] is extended to this class of devices. Macromodels are expressed in terms of suitable nonlinear parametric relations, that can be easily estimated from device port responses and can be readily converted into SPICE-like subcircuits or directly implemented as meta-language descriptions, like VHDL-AMS. Besides, the models are fully compatible with IBIS (Input Output Buffer Information Specification), the standard for the description of digital integrated circuits [9]. IBIS ver. 4.1, within the framework of *multilingual extension*, allows for the inclusion of models in different possible languages, enabling the use of the proposed model in most EDA tools.

2 Device and model structure

This Section illustrates the basic structure of a driver circuit with pre-emphasis and discusses its modeling. We start by considering a generic bit stream defined by a discrete-time sequence $x(k)$, $k = 1, 2, ...$ that must be sent on the interconnect, where $x \in \{0, 1\}$. For enhancing the high frequency components of transmitted signal, a common solution is to apply a FIR (Finite Impulse Response) filtering technique to the original sequence $x(k)$ to obtain a new transmitted sequence $y(k)$. Without loss of generality, the simplest FIR filter with two coefficients writes

$$y(k) = a_1 x(k) + a_2 x(k-1) \qquad (1)$$

whose transfer function in the z-domain is $H(z) = a_1 + a_2 z^{-1}$, and the frequency response turns out to be $H(\omega) = a_1 + a_2 \exp(-j\omega T)$, where T is the pulse width. As an example, Fig. 1 shows $|Y(j\omega)|$ for $x(k) =$"011010", $T = 1$ns, $a_1 = 1$, $a_2 = -\beta$, and two different values of β: $\beta = 0$ (no-emphasis) and $\beta = 0.33$ (33% of emphasis).
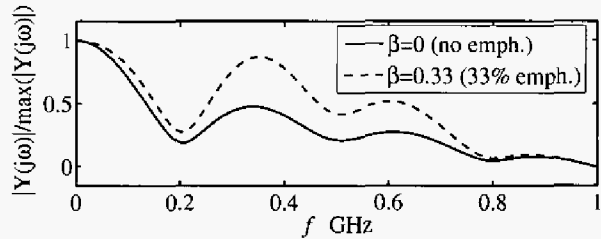

Figure 1: Example spectra of $y(k)$ signal (see text and equation (1)) for no emphasis (solid line) and 33% emphasis (dashed line)

A suitable design of the filter, *i.e.*, the tuning of the filter coefficients a_1, a_2 of (1) leads to the optimal transmitted signal compensating for the frequency attenuation of the interconnect (*i.e.*, the communication channel) and to good quality received signals (a discussion on the tuning of the filter coefficients can be found in [10]).
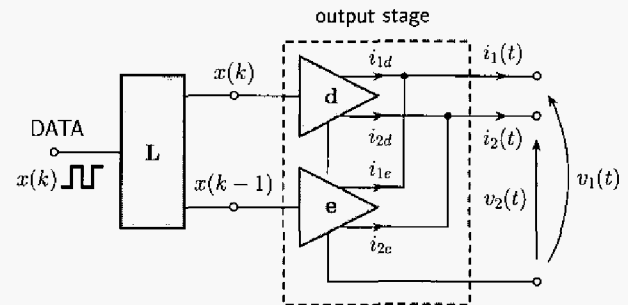

Figure 2: Generic structure of a two-tap differential driver with the main blocks and the relevant electrical variables.

Figure 2 shows the basic structure of a differential driver implementating a FIR filter with two coefficients, with its main blocks and electrical variables. In this structure, d denotes the main driver and e the complementary driver providing the user-tunable degree of emphasis. The analog output currents can be

expressed as sums of the output currents of the two drivers

$$\begin{cases} i_1 &= i_{1d}(t) + i_{1e}(t) \\ i_2 &= i_{2d}(t) + i_{2e}(t) \end{cases} \tag{2}$$

where i_{1d}, i_{2d} and i_{1e}, i_{2e} are the separate contributions of driver d and e, respectively, to the total currents i_1 and i_2. The values of the above currents are decided by the drivers state and strenght. The drivers state is controlled by block L, that processes the input bit sequence $x(k)$ to feed drivers d and e with $x(k)$ and $x(k-1)$, respectively. Each device current, therefore, is proportional to the signal $a_1 x(k) + a_2 x(k-1)$, where a_1 and a_2 are coefficients taking into account the drivers strenghts. This is the mechanism for the analog implementation of the FIR filter of (1).

As an example, Fig. 3 shows the output voltage responses of a driver with the same structure described in the scheme of Fig. 2, producing the bit stream $x(k)$ ="00111000". In each subplot, the vertical dotted lines indicate the intervals defined by the discrete-time k. More details on this class of devices can be fond in [2, 3, 4].
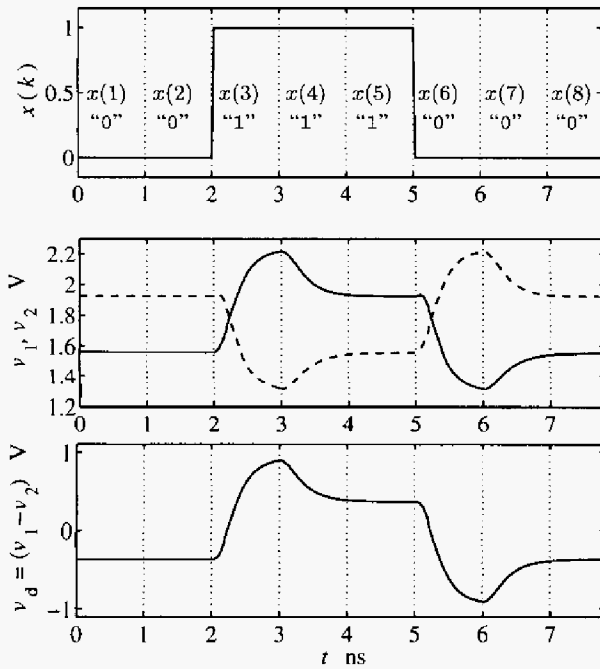

Figure 3: Example port responses of a differential driver like the one illustrated in Fig. 2.

For the structure of Fig. 2, a behavioral macromodel would be a set of nonlinear dynamic relations approximating the output port currents i_1 and i_2 flowing out of the device port terminals. According to (2), i_1 and i_2 are sums of the drivers output currents, and these can be effectively approximated by means of two-piece parametric representations as described in [7, 8]. In such a way, the following model representation for the complete driver of Fig. 2 can be adopted (only current i_1 is discussed here

for the sake of simplicity)

$$i_1 \approx [w_{1dH}(t) i_{1dH} + w_{1dL}(t) i_{1dL}] + \\ [w_{1eH}(t) i_{1eH} + w_{1eL}(t) i_{1eL}] \tag{3}$$

where submodels i_{1dH}, i_{1dL} account for the device d behavior in the fixed high and low state, respectively, and i_{1eH}, i_{1eL} are the corresponding submodels for the driver e. All submodels are nonlinear dynamic parametric relations whose inputs are the port voltage variables $v_1(t)$ and $v_2(t)$. In the previous representation, the other terms are weighting signals accounting for the synchronous delayed state transitions of the two output stages.

The estimation of model (3) amounts to computing the weighting signals and the parameters defining its submodels. This is a direct extension of the procedure discussed in [8] for the case of a standard differential stage like d and e in Fig. 2. However, the estimation of (3) implies the complete and separate access to each of the two drivers composing the output stage. In order to simplify the modeling procedure, the approximations $i_{1eH} = \alpha_{1H} + \alpha_{2H} i_{1dH}$ and $i_{1eL} = \alpha_{1L} + \alpha_{2L} i_{1dL}$ are exploited in equation (3), leading to

$$i_1 \approx [w_{1dH}(t) + \alpha_{1H} + \alpha_{2H} w_{1eH}(t)] i_{1dH} + \\ [w_{1dL}(t) + \alpha_{1L} + \alpha_{2L} w_{1eL}(t)] i_{1dL} \tag{4}$$

that can be rewritten as

$$i_1 \approx w_{1H}(t) i_{1dH}(v_1, v_2, d/dt) + w_{1L}(t) i_{1dL}(v_1, v_2, d/dt). \tag{5}$$

where the new weighting signals w_{1H} and w_{1L} include all the effects of the state transitions of both drivers composing the output stage.

Model representation (5), can be estimated as a standard two-piece representation by means of the Mπlog methodology for differential drivers, as discussed in [7, 8]. Briefly, the estimation procedure amounts to computing the parameters defining its submodels and the weighting signals. Each submodel i_{1dH} and i_{1dL} is the sum of a static part (*i.e.*, a static surface obtained by means of a set of DC experiments) and a dynamic part obtained by matching the response of a parametric model to the reference responses of the driver forced in a fixed high and low logic state, respectively. Once the submodels parameters are estimated, the weighting signals are compuded from the transient responses of the driver performing complete state switchings on a set of reference loads by means of linear inversion of equation (5).

It is worth noting that the above representation was derived for the class of two-tap differential drivers like the one of Fig. 2, implementing a FIR filter with two coefficients. However, representation (5) is more general and holds also for the case of differential drivers implementing FIR filters with a higher number of coefficients.

3 Application Example

In this Section, the proposed modeling approach is demonstrated on a Xilinx Multi-Gigabit serial transceiver used in the

Virtex-II Pro series FPGA. The example transceiver is a differential CML (Current Mode Logic) device operating in the frequency range 622 Mb/s – 3.125 Gb/s that allows a configurable degree of pre-emphasis within the range 10 – 33 %. The internal structure of the output buffer of the example transceiver is the same illustrated in Fig. 2 and a detailed HSPICE transistor-level description, available form the official Xilinx website (www.xilinx.com), is used as the *reference* model hereafter. In all tests carried out in this study, the reference model with a 33% degree of pre-emphasis is used to compute the responses needed for the estimation of macromodel parameters and for model validations. More details on the device and on the usage of the reference model can be found in [12].

For the macromodel estimation, the weighting signals and submodels of (5) are computed through the procedure outlined in the previous Section and the obtained macromodels are implemented as SPICE subcircuits. In all tests carried out in this study, the accuracy of the proposed macromodel has been quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the maximum delay between the reference and the macromodel responses measured for the zero voltage crossing of the differential voltage $v_d = v_1(t) - v_2(t)$. The maximum relative voltage error is computed as the maximum error between the reference and macromodel voltage responses divided by the voltage swing.

As a first validation, devised to highlight the accuracy of the macromodel for loads different from those used in the estimation process, we consider a test setup consisting of the example driver connected to a 50 Ω differential resistor. In the estimation procedure, model parameters were obtained from the transient responses of the driver connected to the transceiver input section, whose internal differential matching resistor is 100 Ω. The driver produces a "001111..." bit stream and three different bit-rates values are considered. For such bit-rates, Fig. 4 shows the comparison of the differential voltage $v_d(t)$ waveforms computed for the macromodel and for the reference model. In this test, the timing error is 5 ps and the maximum relative error turns out to be less than 5%. It is ought to remark that the three macromodels involved in this test differ only for their weighting signals (see (5), which, however, are obtained from a single set of generating coefficients by different juxtaposition in time of their edges. In other words, the proposed macromodels can be considered parametric in the duration of the bit time.

As a second validation, a test setup consisting of two Thevenin sources connected to the output terminals of the example driver is considered. Each Thevenin source consists of the series connection of a $R_S = 50$ Ω resistor and an independent voltage source. In this test, the driver produces a "001111..." bit stream (see the top panel of Fig. 5) and the bit time is set to the unrealistic value of 10 ns in order to allow the driver response to reach steady state values before the starting of each transition. The middle panel of Fig. 5 shows the waveforms of the two voltage sources (labelled as $e_1(t)$ and $e_2(t)$). The two waveforms have non-synchronous transitions in order to excite both the differential and the common mode operation of the de-
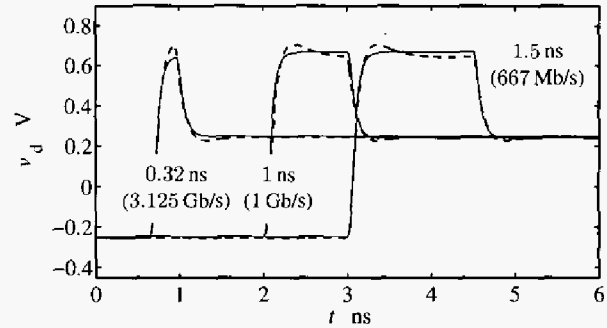

Figure 4: Differential voltage $v_d(t)$ computed for the Example driver producing a bit stream "001111...". The driver is loaded by a 50 Ω resistor and different bit-rates are considered.

vice. Finally, the bottom panel of Fig. 5 shows the reference and macromodel responses of the differential voltage v_d. For this comparison, the same performance figures as in the previous case for the timing and maximum voltage errors are achieved.

Finally, a more realistic simulation test case consisting of the driver connected to a coupled interconnect structure is considered. The interconnect is a lossless transmission line (odd mode impedance $Z_o = 90$ Ω, even mode impedance $Z_e = 50$ Ω, line length 0.30 m) loaded by a 50 Ω differential resistor. The data pattern used for this study is a 256 bit-long sequence with 0.32 ns bit time (3.125 Gb/s). Figure 6 shows the comparison between the reference and the macromodel port voltages $v_1(t)$ and $v_2(t)$ and the differential voltage $v_d(t)$ responses. Also in this situation a good agreement between reference waveforms and predictions is obtained, with timing errors on the order of 5ps and maximum relative voltage errors less than 3 % of voltage swings.

The efficiency gain of the proposed macromodels w.r.t. the original transistor level models depends on two factors: the implementation of the logical block **L** and the complexity of the analog driver devices. Analog implementations of **L**, as in conventional transistor-level models, requires a run-in time delay for proper operation. As an example, the run-in time of the transistor-level model of the device of this study is 150 ns (*i.e.*, approx. 500 clock cycle at 3.125 Gb/s), which considerably increases simulation times. On the contrary, the proposed macromodel automatically includes the role of the logical block into the weighting signals of (5), thus avoiding, even in a SPICE-like implementation, the overhead of the run-in time. The efficiency gain for the analog driver components, instead, compares to that allowed by the Mπ*log* approach for conventional devices, *i.e.*, speed-up factors on the order of 5 ÷ 100 are possible.

4 Conclusions

This paper discusses the development of suitable macromodels of differential drivers with pre-emphasis. The proposed models are mathematical relations expressed in terms of parametric equations that completely hide the internal structure of de-
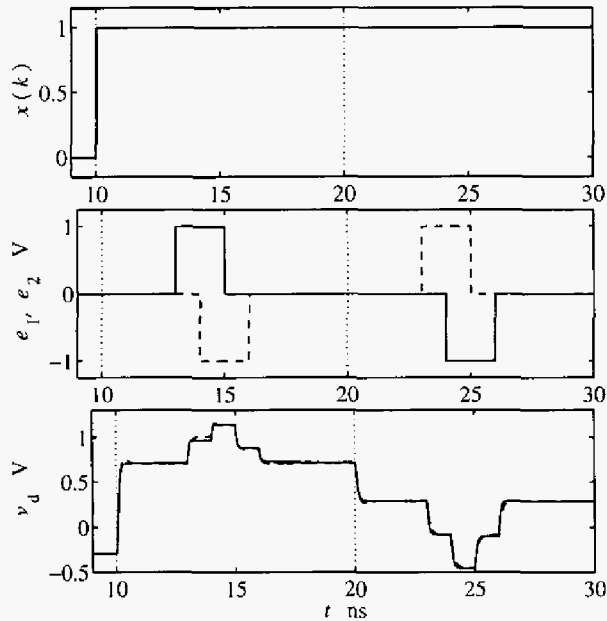
Figure 5: Top panel: driver input signal; middle panel: voltage waveforms $e_1(t)$ (solid line) and $e_2(t)$ (dashed line) of the two thevenin sources stimulating the output port of the driver (see text); bottom panel: comparison between the reference (solid line) and the macromodel (dashed line) response of the differential port voltage $v_d(t)$.

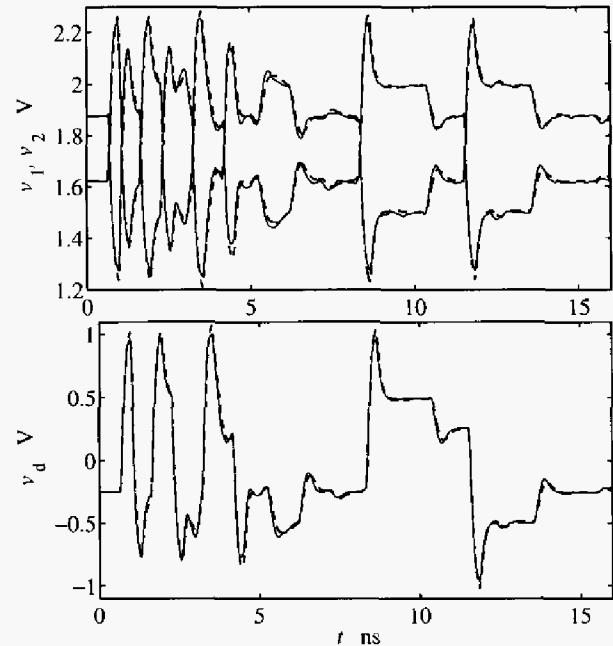

Figure 6: Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the example driver loaded by a coupled transmission line (see text). Solid line: reference, dashed line: macromodel.

vices, thus preserving the intellectual proprietary of vendors. Besides, model parameters can be effectively obtained from device port responses and have been proven to be accurate and efficient enough for the application in the performance predictions of multi-gigabit serial links. Besides, they can be easily implemented in any EDA tool as SPICE-like subcircuits or as metalanguage descriptions like VHDL-AMS.

Acknowledgements

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