Innovative Systems Design and Engineering
ISSN 2222-1727 (Paper) ISSN 2222-2871 (Online)
Vol 3, No 2, 2012

Low Power Schmitt Trigger

Swati Kundra*, Priyanka Soni
Mody Institute of Technology & Science, Lakshmangarh-332311, India
* E-mail of the corresponding author: swati.kundra87@gmail.com

Abstract

The Schmitt Trigger is a comparator circuit that incorporates positive feedback. Noise is being ignored by CMOS Schmitt Trigger as the hysteresis in a Schmitt Trigger circuit offers a better noise margin and noise stable operation. And the simulation has been done on Tanner EDA tool at TSMC 130nm technology with 1 V supply voltage. TSPICE simulation results of the circuit confirm the effectiveness of the approach. Proposed Schmitt Trigger is designed by using less transistor count and a capacitor which results in less average power consumption with decrease in area. Delay is also decreased by using only one PMOS as because delay is more concentrated to PMOS due to less mobility of PMOS compare to NMOS.

Keywords: CMOS Schmitt Trigger, Delay, Low power consumption

1. Introduction

Sometimes an input signal to a digital circuit doesn't directly fit the description of a digital signal. For various reasons it may have slow rise and/or fall times, or may have acquired some noise that could be sensed by further circuitry. It may even be an analog signal whose frequency we want to measure. All of these conditions, and many others, require a specialized circuit that will "clean up" a signal and force it to true digital shape. The required circuit is called a Schmitt Trigger. It has two possible states just like other multivibrators. However, the trigger for this circuit to change states is the input voltage level, rather than a digital pulse. That is, the output state depends on the input level, and will change only as the input crosses a pre-defined threshold. Therefore Schmitt triggers are bistable networks that are widely used to enhance the immunity of circuits to noise and disturbances [1]. They play a critical role in a number of emerging applications including frequency doublers [2], retinal focal plane sensors [3], sub-threshold SRAM [4], image sensors [5], and wireless transponders and sensors [6], [7], to name a few. Schmitt triggers are traditionally implemented using operational amplifiers with a resistive positive feedback [8]. These Schmitt triggers suffer from high power consumption.

The main difference between Schmitt triggers and comparators lies in the DC transfer characteristics. The comparator shows only one switching threshold, while Schmitt trigger shows different switching thresholds for positive-going and negative-going input signals. This characteristic is called hysteresis. If the noise magnitude of the input signal is less than the switching threshold difference, Schmitt trigger will not respond, thus making Schmitt trigger immune to the undesired noise. The Schmitt trigger is a circuit that converts a varying voltage into a stable logical signal (one or zero). The DC transfer characteristic needs hysteresis to reduce the sensitivity to noise and disturbances. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. With proliferation of portable devices, low power circuits are extremely desirable. In a recent work [9], a low power Schmitt trigger circuit design is reported for 3V operations.

2. Schmitt Trigger

When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to

trigger a change. This dual threshold action is called hysteresis, and implies that the Schmitt Trigger has some memory. The benefit of a Schmitt Trigger over a circuit with only a single input threshold is greater stability (noise immunity).

With only one input threshold, a noisy input signal near that threshold could cause the output to switch rapidly back and forth from noise alone. A noisy Schmitt Trigger input signal near one threshold can cause only one switch in output value, after which it would have to move to the other threshold in order to cause another switch. The Schmitt Trigger circuit has been widely used in the input buffers to increase noise immunity. The circuit and the transfer curve of the conventional Schmitt Trigger circuit are shown in conventional circuit. Transistors P1, P2, P3, N1, N2, and N3 in Figure 1 are the I/O devices with the normal operation voltage of V_{DD}. If the board voltage is equal to V_{DD}, the gate-drain and gate-source voltages of transistors P1, P2, P3, N1, N2, and N3 in Fig.1 will not exceed V_{DD}. Thus, the conventional Schmitt Trigger circuit can be operated without suffering high-voltage gate-oxide overstress. As shown in Figure 1, the conventional Schmitt Trigger circuit with different high-to-low and low-to-high transition threshold voltages (and) has better noise immunity than the inverter means switching voltage V_{hl} and V_{lh} is shown is shown in this Figure 2. When the input signal IN goes up to V_{DD} means V_{OH} from GND, the threshold voltage of the conventional Schmitt Trigger circuit is. In other words, the output signal OUT is pulled low when the signal IN exceeds the high-to-low threshold voltage. Similarly, when the input signal IN goes down to V_{OL} i.e GND from V_{OH}, the threshold voltage of the conventional Schmitt Trigger circuit. In other words, the output signal OUT is pulled up when the input signal IN is lower than the low-to-high threshold voltage. Hence, the noise immunity of the conventional Schmitt Trigger[10] circuit is better than that of inverter. The threshold voltages and can be adjusted by controlling the device dimensions of those transistors [11].

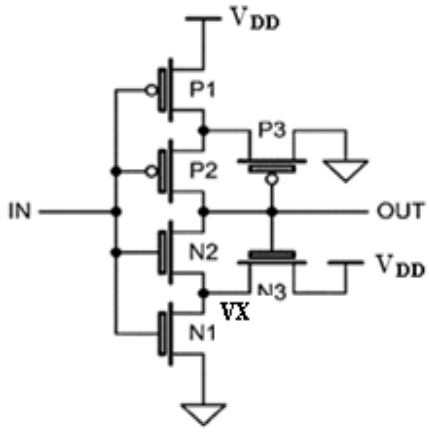

Figure 1. Schmitt Trigger.

The standard cascade architecture used in the CMOS Schmitt Trigger circuit design [12] is shown in the Figure 1 limits lowering of the operating voltage. The operation of the Schmitt Trigger circuit is as follows. Initially, IN = 0 V, the two stacked p-MOSFET (P1 and P2) will be on. Hence OUT = V_{DD}. When IN rises to V_{TN}, N1 is on. But N2 is still off since N3 is on and source voltage of N2 is V_{DD}. Now N1 and N3 form an inverting NMOS amplifier. Thus, source voltage of N2 is falling with increasing IN. When source voltage of N2 drops to V_{TN}, N2 is on. Now both N2 and N1 are on, OUT approaches to 0V rapidly and N3 becomes off. When IN approaches V_{DD}, the two stacked n-MOSFET (N1 and N2) will be on. Hence OUT = 0. When IN falls to $|V_{TP}|$, P1 is on. But P2 is still off since P3 is on and source voltage of P2 is 0 V. Now P1 and P3 form an inverting PMOS amplifier. Thus, source voltage of P2 is rising with decreasing IN. When source voltage of P2 rises to $|V_{TP}|$, P2 is on. Now both P1 and P2 are on, OUT approaches to V_{DD} rapidly and P3 becomes off.

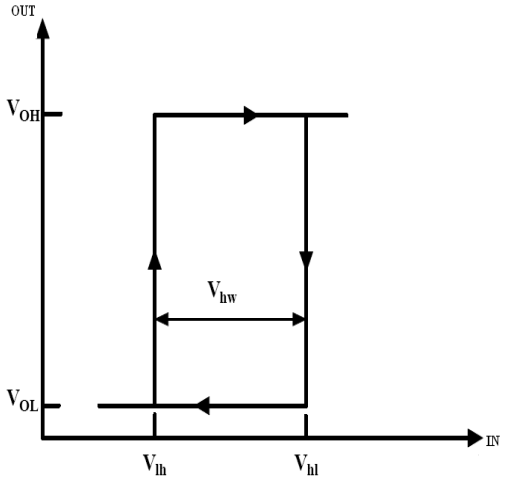

Figure 2. Voltage Transfer Curve

The voltage transfers characteristic exhibits a typical hysteresis behavior as shown in Figure 2. In Figure 2, V_{OH} is the maximum output voltage and V_{OL} is the minimum output voltage. V_{hl} is the input voltage at which output switches from V_{OH} to V_{OL}. V_{lh} is the input voltage at which output switches from V_{OL} to V_{OH}. V_{hw} is called the hysteresis width[13]. The voltages, V_{hl}, V_{lh} and V_{hw} are given by [12].

$$V_{hl} = \frac{V_{DD} - RV_{TN}}{R+1} \tag{1}$$

$$V_{lh} = \frac{R|V_{TP}|}{R+1} \tag{2}$$

$$V_{hw} = V_{hl} - V_{lh} = \frac{V_{DD} - R(V_{TN} - |V_{TP}|)}{R+1} \tag{3}$$

where the ratio $R = \sqrt{\beta_n/\beta_p}$. The n- and p-MOSFETs' transconductance parameters are β_n and β_p, respectively.

The basic circuit of Schmitt Trigger is shown in Fig.1. We can divide into two parts, depending on whether the output is high or low. If the output is low, then P3 is on and N3 is off and p-channel portion is used in calculating the switching point voltages, while if the output is high, N3 is on and P3 is off and n-channel portion is used to calculate the switching point voltages. Also, if the output is high, P2 and P1 are on, providing a DC path to V_{DD}. Now assume that output is high (=V_{DD}) and the input is low (=0V). The bottom portion of the Schmitt Trigger in calculating the upper switching point voltage, V_{hl}. MOSFETs N1 and N2 are off, with IN = 0V while N3 is on. The source of N3 floats to V_{DD}-V_{THN}, or approximately 4V for V_{DD}=5V. This point is labeled as V_x.

With IN less than the threshold voltage of N1, V_x remains at V_{DD}-V_{THN3}. As IN is increased further, N1 begins to turn on and the voltage, V_x, starts to fall toward ground. The high switching point voltage is defined when

$$IN = V_{hl} = V_{THN2} + V_x \tag{4}$$

or when N2 starts to turn on. As N2 starts to turn on, the output starts to move toward ground, causing N3

to start turning off. This in turn causes Vx to fall further, turning N2 on even more. This continues until N3 is totally off and N2 and N1 are on. This positive feedback causes the switching point voltage to be very well defined [13]. When equation (4) is valid, the currents flowing in N1 and N3 are essentially the same. Equating these currents gives

$$\frac{\beta_1}{2}(V_{hl} - V_{THN})^2 = \frac{\beta_3}{2}(V_{DD} - V_X - V_{THN3})^2 \tag{5}$$

Since the sources of N2 and N3 are tied together, $V_{THN2} = V_{THN3}$ the increase in the threshold voltages from the body effect is the same for each MOSFET. The combination of equations (4) and (5) yields

$$\frac{\beta_1}{\beta_2} = \frac{W_1 L_2}{L_1 W_2} = \left[\frac{V_{DD} - V_M}{V_M - V_{THN}}\right]^2 \tag{6}$$

The threshold voltage of N1, given by V_{THN} in this equation, is zero body bias threshold voltage (=0.8V in our long channel CMOS process and 0.25V in the short channel process). Given a specific upper switching point voltage, the ratio of MOSFET transconductors is determined by solving this equation. A general design rule for selecting the size of N2, that is, β_2, is to require that

$$\beta_2 \geq \beta_1 \text{ or } \beta_3 \tag{7}$$

Since N2 is used as a switch.

A similar analysis can be used to determine the lower switching point voltage, V_{lh}, resulting in the following design equation. Means in this upper half of the circuit is used for calculating this value with the help of P1, P2, P3.

$$\frac{\beta_3}{\beta_2} = \frac{W_3 L_2}{L_3 W_2} = \left[\frac{V_{lh}}{V_{CC} - V_{lh} - V_{THP}}\right]^2 \tag{8}$$

3. Conventional Schmitt Trigger

The schematic of conventional CMOS Schmitt Trigger is shown in Figure 3. and its corresponding input output waveform in Figure 4. The average power consumed is 6.654744e-008 watts.

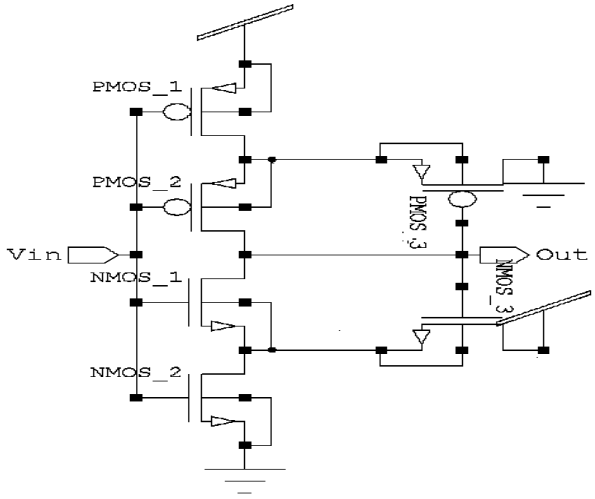

Figure 3. Schematic of conventional Schmitt Trigger.

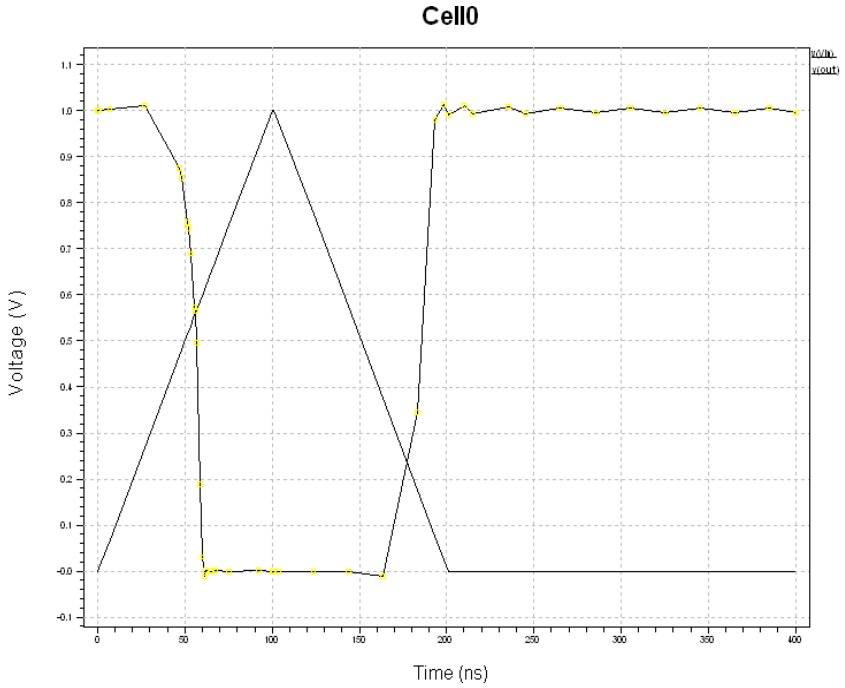

Figure 4. Input and output waveform of the conventional Schmitt Trigger

Hysteresis loop of the Schmitt Trigger is shown in Figure 5.

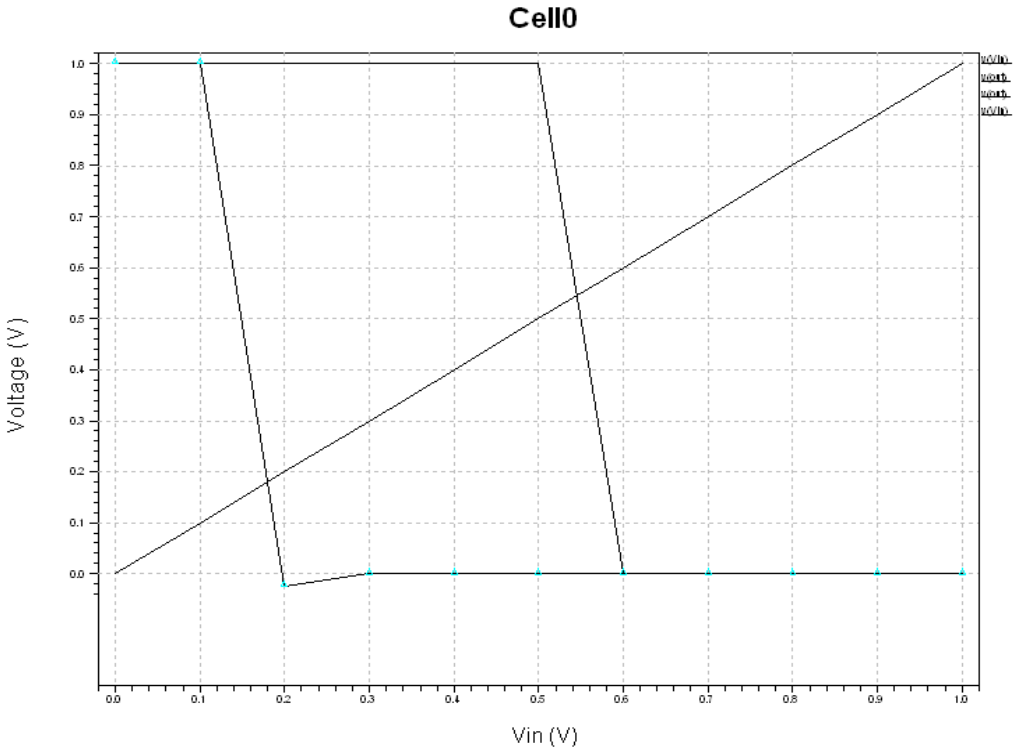

Figure 5. Hysteresis curve of the conventional Schmitt Trigger

4. Proposed Schmitt Trigger

Compared with the traditional 6-transistors Schmitt trigger, Schmitt trigger composed is designed of four transistors. And designed by using one PMOS and three NMOS and a capacitor, to stable the circuit capacitor is used between them. And the delay decreases as the delay is more concentrated due to PMOS because of less mobility of holes as compared to electrons. By using this, less area is used, less delay and have low average power consumption than the conventional. The schematic of proposed Schmitt Trigger is shown in Figure 6 and the input output waveform is shown in Figure 7 and hysteresis is shown in Figure 8. The average power consumed is 5.039027e-008 watts.

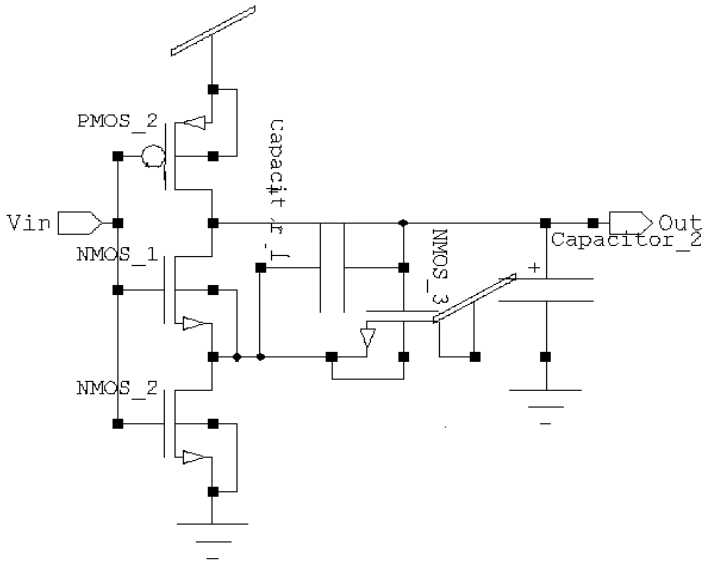

Figure 6. Schematic of Proposed Schmitt Trigger

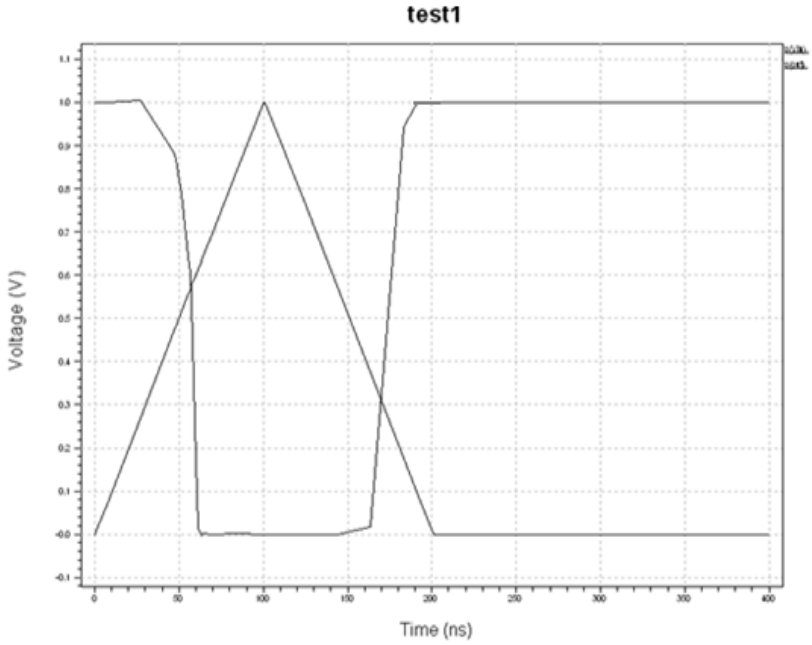

Figure 7. Input and Output waveform of proposed Schmitt Trigger.

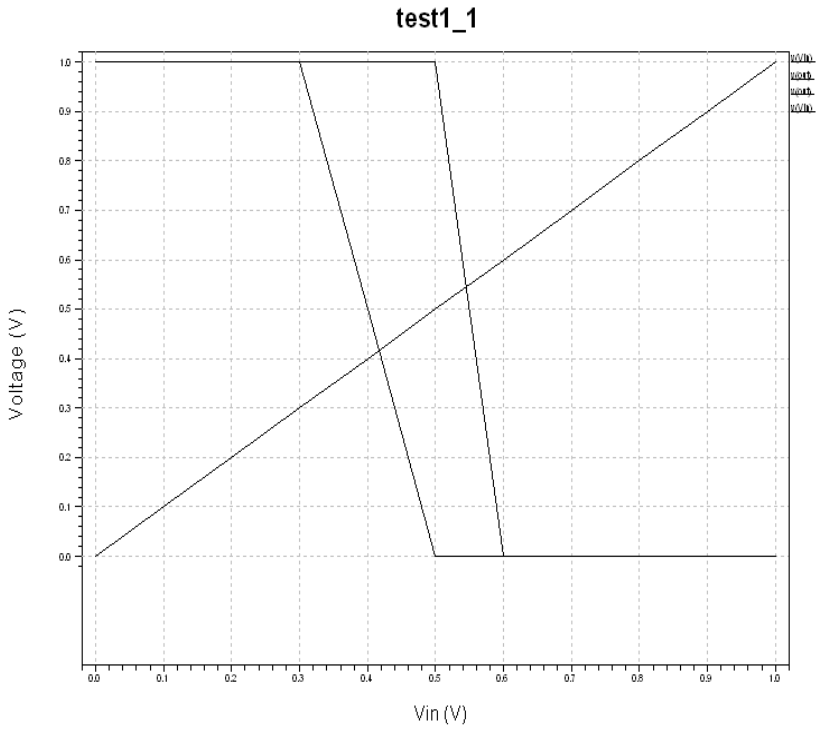

Figure 8. Hysteresis curve of proposed Schmitt Trigger

5. Conclusion

Simulation has been done on tanner EDA tool at TSMC 130nm technology with 1 V supply voltage. TSPICE simulation results of the circuit confirm the effectiveness of the approach. Proposed Schmitt Trigger is modified by using four transistors having less average power consumption with decrease in area. Delay is also decreased by using only one PMOS as because delay is more concentrated to PMOS due to less mobility of holes compare to electrons. Proposed Schmitt Trigger is formed by using four transistors and have better performance than the conventional Schmitt Trigger. As there is less transistor count by which area is reduced and delay is also reduced. The average power consumption of the proposed Schmitt Trigger is less in comparison to conventional Schmitt Trigger. Measured results verified the principle of operation and the characteristics of this low power Schmitt trigger circuit. The circuit has been used in the design of low power, very low frequency integrator oscillators.

References

[1] O. Schmitt (Jan 1938), "A thermionic trigger," *J. Scientific Instruments*, pp. 24-26.

[2] S. Seo, Y. Jeong, and J. Kenney (2007), "A modified CMOS frequency doubler considering delay time matching condition", *Proc. Int 'I Symp. Info. Tech. Converg.*, pp. 392-395.

[3] C. Wu and C. Chiang (Aug 2004), "A low-photo current CMOS retinal focal-plane sensor with a pseudo-BJT smoothing network and an adaptive current Schmitt trigger for scanner applications," *IEEE Sensors J.* **4**(4), 510-518.

[4] Kulkarni, K. Kim, and K. Roy (Oct 2007), "A 160 mV robust Schmitt trigger based sub-threshold SRAM," *IEEE J. Solid-State Circuits* **42**(10), 2303-2313.

[5] D. Park, 1. Rhee, and Y. Joo (2009), "Wide dynamic range and high SNR self reset CMOS image sensor

using a Schmitt trigger", *Proc. IEEE Sensor Conf.*, pp. 294-296.

[6] W. Liu, K. Vichienchom, M. Clements, S. DeMarco, C. Hughes, E. McGucken, M. Humayun, E. de Juan, J. Weiland, and R. Greenberg (Oct 2000), "A neuro-stimulus chip with telemetry unit for retinal prosthetic device", *IEEE J. Solid-State Circuits* **10**(35), 1487-1497.

[7] B. Choi, 1. Yao, S. Han, X., Xie, G. Li, and Z. Wang (2007), "A 2.4 GHz low power wireless transceiver analog front-end for endoscopy capsule system", *Analog Integr Circ Sig Process* **51(**14**),** 59-71.

[8] A. Sedra and K. Smith (1998), *Microelectronic circuits*, (4th Edition), New York.

[9] AL-SARAWI, S.F. (2002), "Low power Schmitt trigger circuit", *Electron. Lett*. **38**(18), 1009–1010.

[10] Filanovsky, I. M., Baltes, H. (1994), "CMOS Schmitt Trigger Design", *IEEE Transactions Circuits System* **41**(1), 46-49.

[11] D. A. Hodges and H. G, Jackson (1983), *Analysis and Design of Digital Integrated Circuits*, New York: McGraw- Hill.

[12] D. A. Hodges, H.G. Jackson and R. A. Saleh (2004), *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology* (3rd Edition), New York: McGraw-Hill.

[13] R. Jacob Baker (1964), *CMOS Circuit Design, Layout and Simulation* (3rd Edition), New York: Wiley.