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Transmissor de Comunicações Móveis Outphasing

Outphasing Mobile Communications Transmitter

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Dr. José Carlos Pedro, Professor Catedrático, e do Dr. Pedro Miguel Cabral, Professor Auxiliar, ambos do Departamento de Electrónica Telecomunicações e Informática da Universidade de Aveiro

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Palavras-Chave

Amplificadores de Potência, Rádio-frequência, Outphasing, Chireix, Transmissor, Classe F, PAPR, OPBO, GaN HEMT, ADS

Resumo

Esta dissertação propõe a implementação de uma aquitectura Outphasing de amplificador de potência para transmissores de comunicações móveis. O principal foco do trabalho é a obtenção de um protótipo funcional, que demonstre melhorias em termos de rendimento de potência em regime de *back-off*, em relação a outras configurações tradicionais.

A arquitectura proposta sugere que o separador de sinais seja implementado no domínio digital, conferindo maior versatilidade ao dispositivo. Para além disso, ao contrário do Outphasing tradicional, a potência dos sinais de entrada dos ramos do PA não é constante: poderá variar livremente para beneficiar o PAE a maiores OPBOs.

O amplificador foi implementado usando dois GaN HEMT de 10 W e obteve uma potência máxima entre 43.42 dBm e 43.73 dBm na banda [2.25; 2.40] GHz (a sua banda de operação). Desta forma o amplificador possui 6.5 % de largura de banda. Em termos de rendimento de dreno, os valores máximos variam entre 64.3 % e 68.7 %, enquanto que o PAE máximo varia entre 55.9 % e 58.4 %. Para 2.3 GHz, a sua melhor frequência de operação, o PAE mantém-se superior a 50 % até -6.0 dB de OPBO.

Para poder implementar esta configuração num sistema de comunicações móveis de forma menos exigente para a unidade de processamento digital, foi estudada a implementação do separador de sinais através de equações polinomiais que traduzam o sinais de entrada do sistema nos sinais necessários para os ramos. Nos testes feitos, foi possível verificar que o desempenho do PA, em termos de potência e eficiência, não varia substancialmente, mesmo quando a ordem do polinómio é baixa. No entanto, esta redução da ordem do polinómio pode comprometer a linearidade do amplificador.

Quando testado com um sinal LTE com 10.33 dB de PAPR ou com um sinal GSM de 4 portadoras com 6.2 dB, ambos com 10 MHz de largura de banda, o amplificador demonstra níveis de distorção consideráveis. Isso é demonstrado nas três métricas de desempenho avaliadas: AM-AM; AM-PM; e ACLR. Os níveis de eficiencia média atingem os 50 % para o sinal GSM e 36% para o sinal LTE. Após a utilização de pré-distorção, o amplificador melhorou as métricas avaliadas. Este cenário foi testado para o sinal LTE e utilizando um polinómio de 7ª ordem no separador de sinais. O ACLR baixou de -21 dBc para -56 dBc; a variação AM-AM de 2.3 dB para 0.6 dB; e a variação AM-PM de 61.0º para 3.2º. Isto enquanto o rendimento médio aumentou de 30 % para 36 %.

No final, os objectivos do trabalho foram concluídos, pelo que o protótipo produzido se equipara a alguns trabalhos de referência presentes na literatura.

Palavras-Chave

Power Amplifiers, Radio Frequency, Outphasing, Chireix, Transmitter, Class F, PAPR, OPBO, GaN HEMT, ADS

Abstract

This dissertation proposes the implementation of an Outphasing PA architecture for mobile communication transmitters. In this work, the main focus is the development of a functional prototype that demonstrates power efficiency improvements at high power back-off, when compared to traditional configurations.

The proposed architecture suggests the signal component separator to be implemented in the digital domain, allow the device to become more flexible. Also, unlike the traditional Outphasing, the input power at the branches is not constant: it can change freely to benefit PAE at higher OPBO.

The amplifier was implemented using two 10 W GaN HEMT and it obtained a maximum power between 43.42 dBm and 43.73 dBm in bandwidth of [2.25;2.40] GHz (its operational bandwidth). The drain efficiency, the maximum values vary between 64.3 % and 58.4 %, and the maximum PAE between 55.9 % and 58.4 %. For 2.30 GHz, its best operational frequency, PAE is higher than 50 % until -6.0 dB of OPBO.

To be able to implement this configuration on a mobile communication system in a less demanding manner for the digital processing unit, the usage of polynomial equations, that describe the power of the input signal into the necessary branch signals, has been studied in this document. In the performed tests, it was observed that the power and the efficiency performances of the PA does not substantially change, even with the usage of low order polynomials. Yet, low order polynomials may compromise the linearity of the amplifier.

When tested with a LTE signal with PAPR of 10.33 dB or with a 4-carrier GSM signal with PAPR of 6.2 dB, both with a bandwidth of 10 MHz, the amplifier shows considerable amounts of distortion. That is demonstrated in the three evaluated performance metrics: AM-AM; AM-PM; and ACLR. The average efficiency levels reach 50 % for the GSM signal and 36 % for the LTE one. After digital predistortion was applied, an improvement of the evaluated metric was observed. This scenario was tested for the LTE signal, using the 7th order polynomial in the signal component separator. The ACLR lowered from -21 dBc to -56 dBc; the AM-AM variation from 2.3 dB to 0.6 dB; and the AM-PM variation from 61.0º to 3.2º. This while the average efficiency increased from 30 % to 36 %.

In the end, the objectives of this work were concluded, and the produced prototype can equate to some of the state-of-the-art reference works.

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Acronyms

4G	Forth Generation of Communication Systems
5G	Fifth Generation of Communication Systems
ACLR	Adjacent Channel Leakage Ratio
ADS	Advanced Design Simulator
AM	Amplitude Modulation
CW	Continuous Wave
DC	Direct Current
DhPA	Doherty Power Amplifier
DPD	Digital PreDistortion
DUT	Device Under Test
G_{Op}	Operative Gain
G_T	Transducer Gain
GMSK	Gaussian Minimum-Shift Keying
GSM	Global System for Mobile communications
HEMT	High Electron Mobility Transistor
IoT	Internet of Things
LINC	LInear amplification using Nonlinear Components
LTE	Long Term Evolution
LUT	Look Up Table
Msc.	Master of Science
OPBO	Output Power Back-Off
Oph	Outphasing
OphPA	Outphasing Power Amplifier
P_{AV}	Available Power
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PF	Power Factor
PSD	Power Spectral Density
RF	Radio Frequency
S Parameter	Scaterring Parameters
VNA	Vector Network Analyzer

VSG	Vector Signal Generator
W-CDMA	Wide-Band Code-Division Multiple Access

Chapter 1

Introduction

1.1 The Evolution of Communication Systems and the Power Amplifier

The most power consuming component of a modern mobile transmitter is the Power Amplifier, PA [1,2]. These components suffer from a crippling trade-off between power efficiency and linearity. Classical PAs are either efficient, if operated as in switching modes, or linear, if operated as current sources [3]. In previous communication generations, in order to be able to utilize power efficient PAs, spectral inefficient modulation schemes were used. An example is the GMSK used in the GSM standard, in which all information was stored in its phase [1]. Modulation schemes with better spectral efficiency require phase and amplitude modulation and only linear amplifiers can be used.

As modulation schemes grew in complexity, the communication signals gained different characteristics. One of the most important characteristics in these scenarios is the Peak-To-Average Power Ratio, PAPR. With the evolution of communication systems, amplitude modulation increased the signals PAPR, meaning that the devices would more often be operated in lower power regions. In PA design, that meant that the focus could no longer be confined to peak efficiency and its performance at low power regions gained an ever increasing importance.

Newer generations of communication systems also demand the PA to handle higher data rates in a more efficient manner. This demand encourages the scientific community to rethink this device. Since single transistor amplifiers could no longer provide the necessary performance goals, other more complex techniques began to be explored [4]. As it often happens, scientific innovation can also occur by reviving and giving new purposes to old or almost forgotten techniques. In this case, architectures such as the Doherty PA [5] and the Outphasing PA [6], used in the AM radio broadcast era, resurfaced and drew the attention of the scientific community.

The Doherty power amplifier has established its place as an efficient and fairly linear alternative. These characteristics allied with its relatively low complexity made the Doherty PA very popular. But, this architecture also has its own disadvantages: its nonlinearities are still significant [7]; it usually has narrow bandwidth [8]; and still low peak efficiency caused by the usage of linear PAs in the branches [8]. The Outphasing amplifier only made a strong resurgence more recently with the development of digital signal processing [8]. It has some advantages when compared to the Doherty PA like bandwidth [9, 10] and reconfigurability

[11]. It also allows higher peak efficiencies, because highly efficient PAs can be used in the branches [12].

As technology develops, techniques can be applied to innovate the usage of the PA. The design proposed in this work presents a slightly different approach, as the PA is being partly united with the already common digital processing unit, in order to be able to achieve better efficiency/linearity trade-offs. Here, the amplification circuit is not the sole responsible for the performance of the architecture. The evolution of digital processing units allowed these components to become cheaper and faster [3], so complex operations to generate the necessary driving signals to the amplifier become feasible and allow the engineers to explore techniques to improve PA performance, as presented in [1, 13, 14].

1.2 The Next Generation of Communication Systems

The 2010s decade brought a massive expansion of wireless connected devices and it seems that this tendency is in accelerated growth. Reports state that wireless data is increasing well over a factor of 100 within this decade [15]. This expansion is mostly caused by the massification of smart-phones, tablets and video streaming. These facts are expected to push the limitations of the current LTE-based 4G [16]. The scientific community is working on the development of a new generation of communication systems to face the arising challenges. That will be the Fifth Generation of Communications, 5G. But what are the expectations for this new era? What are its characteristics?

The connected devices are not only expected to grow in number, but they are expected to present different requirements. As the IoT, Internet of Things, makes its appearance, machine-to-machine communications are expected to change the panorama of mobile connectivity [17]. The agglomerate of these changes require 5G to be capable of [17]:

- **Massive System Capacity:** The networks must reduce the cost per bit in delivering data to increase the number of devices;
- **High Data Rates:** 10 Gbps in indoor and dense outdoor scenarios, 100 Mbps in urban and suburban environments and 10 Mbps everywhere else;
- **Low Latency:** Critical applications will require latencies bellow 1 ms;
- **High Reliability and Availability:** Some applications will require the standards of communications to ensure quality connections in any situation;
- **Low Cost:** To enable that sheer number of devices, the infrastructure will, in many cases, have to adapt to cheaper, more efficient and smaller options.

These are some of the fairly-well established characteristics. Since this document is focused on the power amplifier used in wireless transmitters, it is important to affer what this paradigm change represents to these devices.

The effects of the signals PAPR have already been discussed and, although signal waveforms have not been established, it makes sense that this will continue to happen in 5G. To obtain a massive number of connections in a certain space without lowering the standards, the signals spectral efficiency is very important. So, it is most likely that phase and amplitude modulation schemes will still be used. Even if some other technique is used, in some

cases the system is expected to be LTE-compatible [16, 17]. So, those signals will still be, at least partly, used. High power efficiency performances at lower output powers is expected to continue to be an important requirement of a power amplifier.

The next generation will also broaden the used spectrum. In 4G the frequencies do not surpass 6 GHz, but in 5G reaching frequencies close to 100 GHz is under consideration [17]. Yet, the backbone of telecommunications is not expected to be above 10 GHz. Higher frequencies are planned to be used as an addition used for very demanding areas or systems since they can provide very hide bandwidths [17]. With such a broad spectrum, the operational bandwidth of the power amplifier is a very important requirement to fulfill.

Since the 5G standards are still being determined, many other challenges may be presented to PA design in the following years. So, the ones presented in this document may only represent a small portion of them. Since, the goal is that the first 5G networks start to appear by the start of the next decade, the next few years may dictate the exact conditions and requirements of the technology.

1.3 Work-plan

1.3.1 Objectives

In this work, the main goal is to fully design and measure an Outphasing architecture with digitally-driven branch PAs. Those amplifiers were previously set to be operated in class B or class F. The idea is to obtain a feasible, fairly linear, amplifier architecture with good power efficiency performance: this means high peak efficiency and good values for the low power regions. The best compromise between these metrics must be obtained to get an amplifier that corresponds to the increasing demands on transmitter technology. The produced amplifier must have a realistic practical application, so real world non-idealities must be taken into consideration. Ultimately, the device must be compared with other alternatives presented in the literature. As in any Msc. dissertation, with this work the author aims to expand his knowledge and to acquire the necessary skills to be able to produce quality work in this engineering field.

1.3.2 Document Outline

This document is divided in five chapters. It is organized in a manner that almost chronologically describes the necessary steps needed to fully design and measure an Outphasing Power Amplifier like this one.

Chapter 1, Introduction, starts by establishing the basis where this work is set and explains the current state of power amplifier technology as it presents some of its challenges. It also analyzes the predictions for the near future and the next generation of communication systems. Some of the expected challenges to PA design that arise with this development are also briefly exposed.

Chapter 2, Power Amplifiers, sets the theory behind PAs: addressing both its characteristics and performance metrics. It acts as a State-of-the-Art to the developed work, since it constitutes the starting point of this entire process.

Chapter 3, The Outphasing Design, as its name indicates, is the design stage of this work and it is entirely done on the simulator. It begins by using the previously presented concepts to introduce the Outphasing architecture. After the basic concept is established, the branch

amplifier is designed and then the output combiner. The last part of this chapter tests the produced amplifier to find the best possible driving signals.

Chapter 4, The Outphasing Practical Implementation, aims to reproduce the previous chapter results in a practical scenario, so the same tests are performed. Before those measurements are done, some stability tests are conducted to safeguard the equipment.

Chapter 5, Conclusions and Future Work, is the overall conclusions of the entire work as well as the comparison with other alternatives existent in the literature. Future work proposals are also presented in this chapter.

Chapter 2

Power Amplifiers

2.1 Introduction

A Power Amplifier, PA, is a signal amplifier designed to deliver the maximum power to the output. Because of their high power, PAs usually display nonlinear behavior and require different design techniques when compared to the ones used in small-signal amplifiers [18]. In small-signal amplifiers the main goals are gain, noise and linearity. However in PA design the most important metrics are output power and efficiency. To accomplish this, the amplifier definition must not be forgotten: an electrical amplifier is a device that converts DC power into signal power [19]. So, analyzing efficiency is the same as analyzing how well that conversion is performed.

The focus of this chapter is the study of the PA and how to characterize it properly. Proper characterization techniques are of utmost importance when designing a Power Amplifier, because they determine how its performance is evaluated. The main architectures of amplifiers are also briefly described further in the chapter.

2.2 PA Efficiency

As it was previously said, analyzing a PA efficiency is the same as analyzing its power conversion. In that sense, efficiency should be a ratio between DC power and output power. However this is not the most accurate metric to use. The DC feed is not the only source of power in these circuits; there is also the input signal power. Because of its small gain this a very important factor to take into account when designing a PA. In fact, when dealing with high gain amplifiers, the input is so small when compared to the output and DC power, that it does not make a difference [19].

So, when designing a PA there are two efficiency-related figures of merit to look into. The Drain Efficiency, η, and the Power Added Efficiency, PAE. The latter uses the concept of Added Power, P_a, which is simply the difference between the output and the input power as seen in (2.3).

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.1}$$

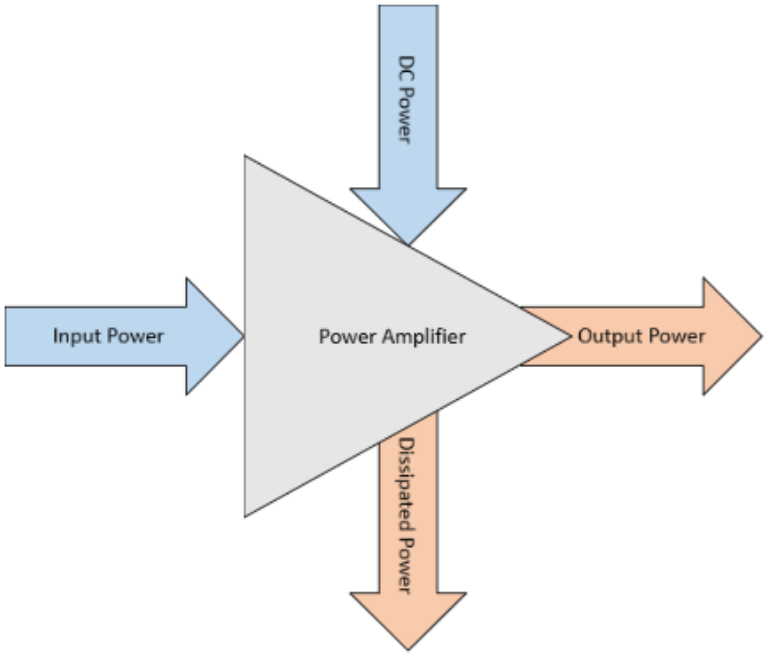

Figure 2.1: Power balance in an amplifier.

$$PAE = \frac{P_a}{P_{DC}} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.2}$$

$$P_a = P_{out} - P_{in} \tag{2.3}$$

2.3 PA Gain

When dealing with PAs, the interest, in terms of gain, will always be power gain. However there are different ways to express the gain of a certain amplifier. In order to be sure that there are not any misunderstandings, the different ways to express gain have been formalized by representing the PA as the two-port network illustrated in Figure 2.2. From this it is possible to extract two ways of expressing power: Available Power, P_{AV}, and Delivered Power, P.

The most important definition in PA design is the Transducer Gain, G_T, defined as a ratio the power delivered to the load and the power available at the source. In this work, this is the most used definition since it provides a reliable representation of the entire system.

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.4}$$

$$G_T = \frac{1 - \left|\Gamma_S^2\right|}{\left|1 - \Gamma_S \Gamma_{IN}\right|^2} \left|S_{21}\right|^2 \frac{1 - \left|\Gamma_L^2\right|}{\left|1 - S_{22}\Gamma_L\right|^2} = \frac{1 - \left|\Gamma_S^2\right|}{\left|1 - \Gamma_S S_{11}\right|^2} \left|S_{21}\right|^2 \frac{1 - \left|\Gamma_L^2\right|}{\left|1 - \Gamma_{OUT}\Gamma_L\right|^2} \tag{2.5}$$

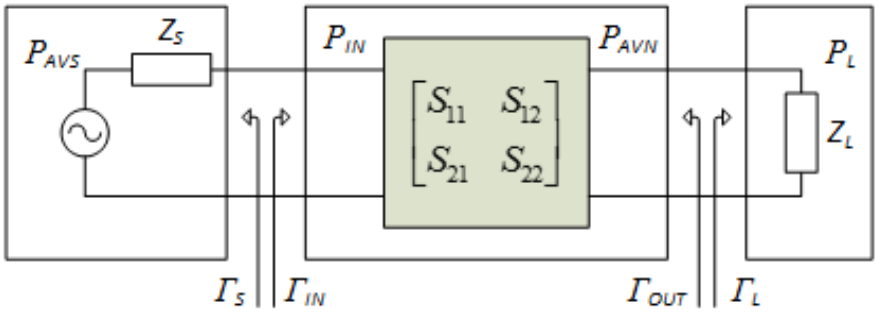

Figure 2.2: Two-port network representation a Power Amplifier [20].

There is another useful definition in PA design, the Operative Gain, G_{Op}. This gain is defined as a ratio between the power delivered to the load and the power delivered to the amplifier. So, it assumes that there is maximum power transfer at the input. This definition can be used when the input matching network is not devised to get an estimate of the PA gain, since, in theory, the network performs complex conjugate matching.

$$G_{Op} = \frac{P_L}{P_{IN}} \tag{2.6}$$

$$G_{Op} = \frac{1}{|1 - \Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L^2|}{|1 - S_{22}\Gamma_L|^2} \tag{2.7}$$

2.4 Linearity and Distortion

A linear amplifier is expected to present the same gain value regardless of its input power. This means that there is no gain compression and the frequency components at the output and input are same. One can easily understand that such a device does not exist. The amplifier is always, at least, limited by its DC sources. So, the amplifier linearity further deteriorates as power levels get closer to this limit. As PAs often operate within the gain compression region, it is very important to analyze their linearity. In many cases, linearization techniques must be employed so that the PA fulfills the specifications of certain applications.

The frequency components generated by distortion may also be problematic as they may cause the transmitter to operate outside its designated bandwidth and, with the ever rising demands on the available spectrum, this is a major issue. In fact, the PA is usually the main contributor to the transmitter nonlinearity.

These concepts can be formulated. Considering the input signal as

$$x(t) = A(t)cos[\omega t + \Theta(t)] \tag{2.8}$$

For example, the response of a nonlinear polynomial system to this signal would be

$$y_{NL}(t) = \sum_{k=1}^{\infty} a_k x(t - \tau_k)^k \tag{2.9}$$

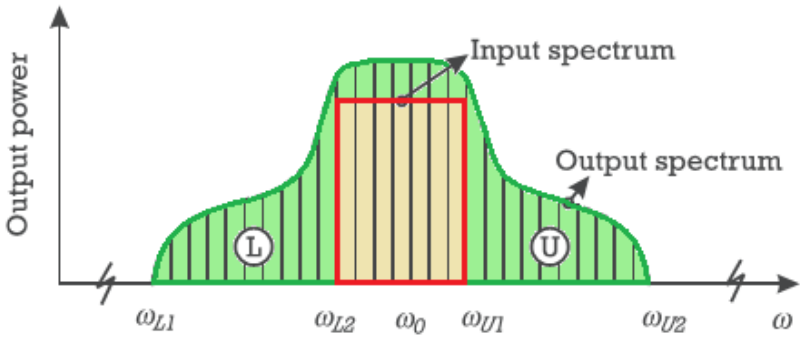

Figure 2.3: Spectrum of a nonlinear multi carrier system [19].

The effects of these systems in a multi carrier signal are illustrated in Figure 2.3. There are ways to characterize these behaviors that will be discussed further on this document.

2.4.1 One-Tone Characterization

One-Tone Characterization is performed by submitting the Device Under Test, DUT, to a sinusoidal Continuous Wave, CW, usually testing several power levels. This method can be used to test a sum of figures of merit such as maximum output power, PAE, η, amongst others. This test may also provide information about the DUT gain and phase-shift evolution with the power levels. By measuring the output power and plot it against the input power, one may get the AM-AM characteristic. That is simply the evolution of the gain. By measuring the phase-shift, the AM-PM characteristic is obtained.

AM-AM characterization

As discussed earlier, AM-AM characterization consists in measuring the DUT gain for several power levels. Through this process, one is able to characterize gain compression or expansion of a nonlinear device [19]. There is an important figure of merit to acquire from the AM-AM characterization: the 1dB Gain Compression Point, P_{1dB}. This consists in the output power in which the gain has decreased 1dB from its small-signal level as illustrated in Figure 2.4.

AM-PM characterization

Another form of characterization of interest is the AM-PM characterization, which consists in measuring the phase of the output signal for multiple power levels. In a linear DUT the phase would remain constant with the variation of the input power. But, in a real device, this is not expected. This nonlinear behavior is mainly influenced by memory effects caused by the transistor parasitic capacitances [21]. As it is to be expected, the more the transistor is driven into the gain compression region the more these effects are noticed, meaning that the AM-PM modulation increases with the output power.

In this characterization, we ought to relate the output signal phase with the input power for a certain frequency [19]. The resulting plot should resemble the one from Fig 2.5.

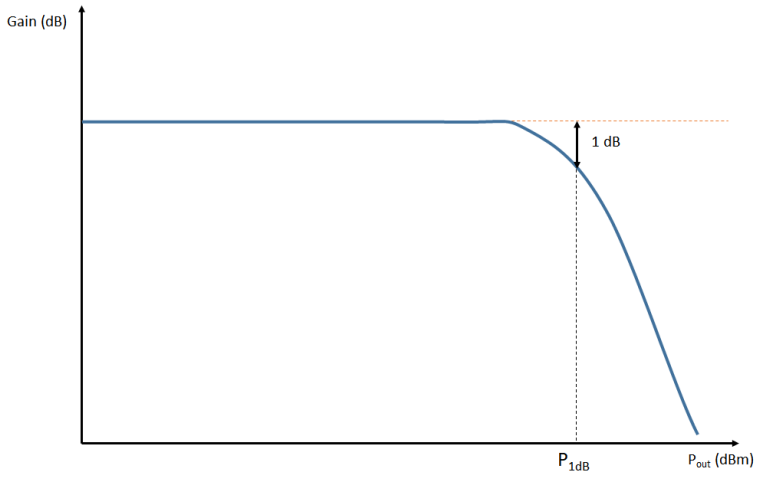

Figure 2.4: Illustration of 1dB Gain Compression Point.

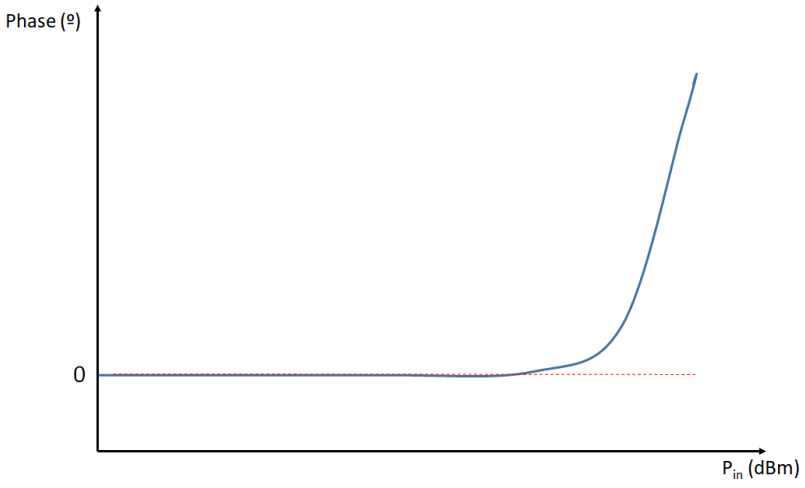

Figure 2.5: Illustration of a typical AM-PM characterization plot.

2.4.2 Two-Tone Characterization

Although the one-tone characterization is a very useful tool to characterize and evaluate a PA, it does not provide a good representation of real telecommunications signals. In order to make a better representation, one must do two-tone characterization tests that provide information of the generation of harmonic components as well as information about mixing components close to the fundamental frequency. These are called the in-band components and establish the main sources of nonlinear distortion [19].

These tests are achieved by exiting the PA with a sum of two tones with frequencies very close to each other. These two tones create different frequency components, whose spectral location depends on the frequency of the tones used to generate them. A generic two-tone excitation signal may be represented by (2.10).

$$x(t) = A_{i1}cos(\omega_1 t) + A_{i2}cos(\omega_2 t) \tag{2.10}$$

The output to this signal is (2.11) [19].

$$y_{NL}(t) = \sum_{r=1}^{\infty} A_{o_r}cos(\omega_r t), \;\; \omega_r = m\omega_1 + n\omega_2 \; and \; m, n \in \mathbb{Z} \tag{2.11}$$

This equation shows that there is a huge amount of frequency components, but typical RF applications utilize narrow band systems. This way one may divide these terms in in-band and out-of-band components, $m + n = 1$ and $m + n \neq 1$, respectively. In this work only the in-band ones will be studied, since RF systems naturally attenuate out-of-band frequencies.

Intermodulation Distortion

As previously established, the nonlinear response of a PA generates frequency components in and out-of-band. The most difficult frequencies to eliminate are the in-band components, because these cannot be filtered out. These frequencies are called Intermodulation Distortion, IMD. An important concept that must be defined is the Intermodulation Ratio, IMR, described by (2.12).

$$IMR = \frac{P_{fund}}{P_{IMD}} = \frac{P(\omega_1)}{P(2\omega_1 - \omega_2)} \tag{2.12}$$

Third Order Interception Point

Third Order Interception Point, IP3, is used as a figure of merit that relates the evolution of the third order IMD to the evolution of the fundamental frequency. These evolutions are represented in Figure 2.6. In small-signal the third harmonic component increases at 3dB/dB, but the fundamental increases at only 1dB/dB. This means that at some point the two plots intercept. This interception point is the IP3, but, as it can also be seen, at higher powers the curves compress. Then, the IP3 is not a real point, it is only a theoretical concept.

This point corresponds to the theoretical point where the third harmonic has the same power as the fundamental frequency, corresponding to an $IMR = 1$.

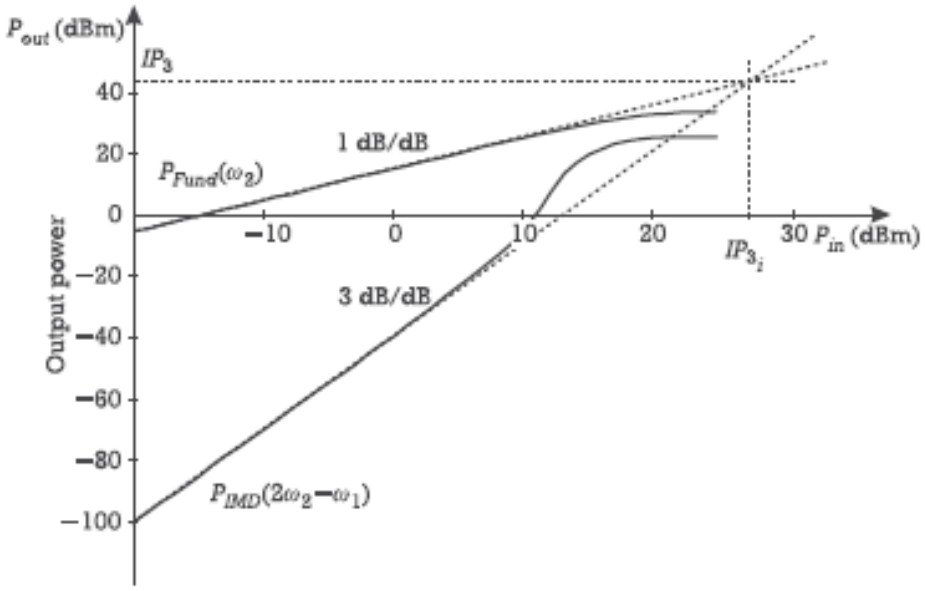

Figure 2.6: IP3 representation [19].

2.5 Stability

When designing a PA for RF/microwave systems it is of utmost importance to guarantee the stability of the circuit. If that is not done, the device may become unstable and, consequently, damaged. So, this has to be dealt with beforehand, in the design stage. It is possible to analyze PA stability through an S Parameter analysis like the one in Figure 2.2.

When either the input or the output of a two-port network presents negative resistance, oscillation may occur [22]. This means that $|\Gamma_{IN}|$ or $|\Gamma_{OUT}|$ is higher than 1. So, to guarantee unconditional stability at a certain frequency (2.13) and (2.14) need to be assured to all terminations, that is $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$. If these conditions are not assured, the device will be potentially unstable.

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1, \quad if\ |\Gamma_L| < 1 \tag{2.13}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1, \quad if\ |\Gamma_S| < 1 \tag{2.14}$$

Contrary to passive devices, an active device may become unstable. That happens if S_{12} is high enough to make $|\Gamma_{IN}| > 1$ and $|\Gamma_{OUT}| > 1$.

An important metric to use is the Rollet factor. The stability conditions according to this metric are $K > 1$ and $|\Delta| < 1$, with K and Δ obtained by (2.15) and (2.16).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.15}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2.16}$$

This, however, raises a question: how to know which loads guarantee stability if $K < 1$? To address this question, the stability circles must be drawn in a Smith Chart [22]. These can be obtained through the $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$ conditions that represent the stability limit for a given frequency. The circles are therefore given by (2.17) and (2.18), where r and C are the radius and the center of the circle. Those parameters are calculated through (2.19) and (2.20) at the output and through (2.21) and (2.22) at the input.

$$|\Gamma_L - C_L| = |r_L| \tag{2.17}$$

$$|\Gamma_S - C_S| = |r_S| \tag{2.18}$$

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2.19}$$

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \tag{2.20}$$

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.21}$$

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \tag{2.22}$$

These equations represent the limit between the stable and the unstable regions in a Smith Chart, but they do not offer any information on which is which. There is, however, a method to discover this: to calculate the stability condition for a certain load in the Smith Chart. Usually, the chosen point is either the center of the stability circle or the center of the Smith Chart. Calculating the latter one may be simpler, since in that case the reflection coefficient is 0. In PA design it is important to guarantee all these conditions not only in the in-band frequencies, but also in the out-of-band ones.

In-band frequencies also need to be tested under large-signal conditions. Transistors characteristics change with the input power, so guaranteeing small-signal is not enough to assure that the power amplifier does not oscillate. Large-signal stability can be verified by mapping the stability circles in a Smith Chart for several power levels.

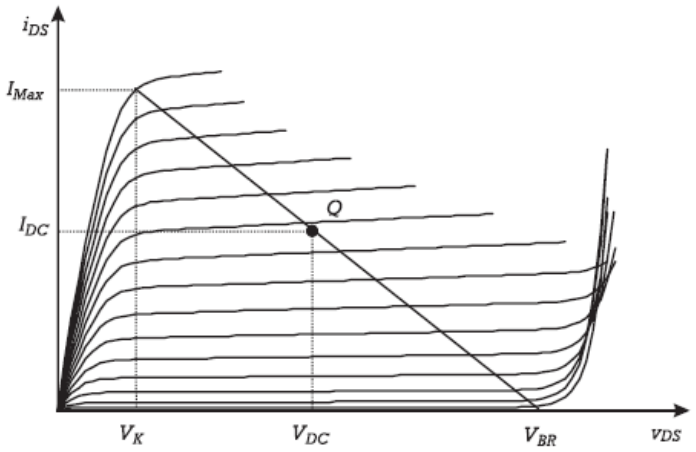

Figure 2.7: Typical I_{DS}/V_{DS} of a transistor [19].

2.6 PA Classes

Many of the PA characteristics rely on the chosen operation class. A lot can be said about each amplification class. However, since that is not the goal of this work, only a brief analysis will be made. Each operation class encompasses a different trade-off between linearity and efficiency. In this document the following classes will be discussed: A, AB, B, C and F. Although there are some other examples, such as D and E, those will not be analyzed.

Starting with the classic operation classes: A, AB, B and C. The main difference in these configurations is their bias point. As it is simple to comprehend, changing the bias point of a transistor imposes major changes to its behavior.

Following Figure 2.7, two voltages are defined: Knee Voltage, V_K, and Breakdown Voltage, V_{BR}. The first one defines the limit between the linear and the saturation regions. If the V_{DS} decreases beyond this point, I_{DS} compresses, increasing nonlinear effects. The latter defines the maximum drain-source voltage supported by the transistor.

These operation classes share the same schematic. In fact, the difference between classes A, AB, B and C is simply the quiescent point. A general circuit is presented in Figure 2.8. The transistor operates as a current source in this circuit. The portion of the signal period in which the transistor conducts is defined by the quiescent point meaning that it will be dependent on the operation class. This portion of the signal period is the conduction angle, 2θ.

With these concepts it is possible to determine the maximum efficiency of each PA class. Assuming that the transistor is being driven by a sine wave, the DC Power, P_{DC}, can be defined as in (2.23) and the Maximum Output Power, P_{Lmax}, as in (2.24). Note that I_P is the difference between the maximum current and the quiescent current.

$$P_{DC} = V_{dc}\frac{I_P}{\pi}[sin(\theta) - \theta\, cos(\theta)] \tag{2.23}$$

$$P_{Lmax} = \frac{1}{4\pi}(V_{dc} - V_K)I_P[2\theta - sin(2\theta)] \tag{2.24}$$

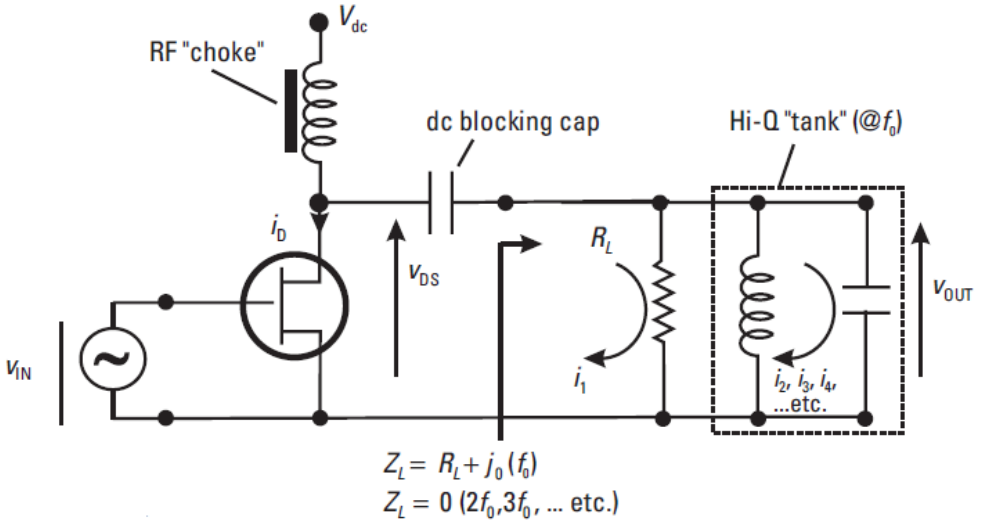

Figure 2.8: Generic representation of a RF PA [23].

So, the maximum PA efficiency is

$$\eta_{max} = \frac{1}{4}\frac{2\theta - sin(2\theta)}{sin(\theta) - \theta\, cos(\theta)}\frac{V_{dc} - V_K}{V_{dc}} \tag{2.25}$$

Class A operation is defined by having a conduction angle of 2 π. This means that the active device is always conducting, even when there is no input signal. Understandably, it has a very poor performance in terms of efficiency. Assuming a transistor with V_K=0, the maximum efficiency value is 50%.

Class B has a conduction angle of π, meaning that the transistor conducts half of the period. An advantage of this operation class is that, when there is no input signal, there is no current on the drain of the transistor. This means no power consumption when the device has no input. With this class, one can expect a maximum efficiency of 78.5%.

Class AB is defined by $\pi < 2\theta < 2\pi$. Although not as efficient as Class B operation, it may guarantee a better linearity/efficiency trade-off for some applications.

Class C has a $2\theta < \pi$, so for most of the time the transistor does not conduct. The efficiency increases as the conducting angle decreases, but the same happens to the output power. In fact, class C operation is not very common in RF PAs as the decrease in the output power imposes smaller power gain. Decreasing power gain further devalues drain efficiency, meaning that the high efficiency of this class is not that good if PAE is taken into account. There is another reason for the lack of use of this class: as the transistor is further biased in the cut-off region, it is more likely to be subjected to to high reverse voltages as the input power increases, thus risking to damage the device.

These definitions are derived from a piece-wise linear transistor model, however real transistors do not have those idealized I_{DS}/V_{GS} characteristics. The cut-off region to conduction region transition is smooth; so it is important to determine what should be considered the Threshold Voltage, V_{th}, in a transistor.

A good way to define V_{th} is the point in the I_{DS}/V_{GS} plot where the variation of I_{DS} is greater. This corresponds to the inflexion point of the curve, i.e. the maximum of its second derivative.

2.6.1 Class F Operation

The only operation class that is yet to be defined is class F. The definition of this class is different than the previous definitions, as it is not just the bias point that differs from them.

In the previous classes, it was always assumed that the current waveforms would either be a sine-wave or a portion of it, while the voltage waveform is always a sinusoid. As can be seen in Figure 2.9 a, the Class B operation voltage is a full sinusoid while the current is only the positive half of the sine-wave. When the current is zero, there is no power consumption in the transistor. The only consumption happens when the voltage is below its average value. If instead of a sine-wave, the voltage was a square-wave the power consumption would ideally be zero. As can be understood, this would mean an increase in the PA efficiency and output power. However, its linearity would decrease. This is the basic idea behind the class F operation that was introduced by V. Tyler in [24].

Now that the concept of the operation class is known, it is necessary to understand how a sine-wave can be substituted by a square-wave. From a mathematical point of view, a square-wave can be expressed by a sum of sine-waves, encompassing the fundamental frequency and its odd harmonic components. In electronic terms, the idea would be to eliminate the even harmonics, similarly to the previously studied operation classes, but preserving the odd harmonics. So, at the odd harmonics the transistor must be terminated in an open circuit while to the even ones must be presented a short circuit. The waveforms are represented in Figure 2.9 b).

In a real circuit it is impossible to obtain a perfect square-wave. Firstly, the device may not produce high order harmonics; secondly, presenting an open circuit to a lot of harmonic frequencies would require a very long and complex matching network which would be difficult to implement. The efficiency of this class decreases as the waveform strays further away from a square-wave. So, efficiency is lower if only low order harmonics are handled.

In all these amplification classes, to obtain the efficiency values, it was always assumed that the device was being driven by a continuous wave at maximum input power. However, that is not the case for real world applications where the signals are modulated. Besides having a more complex spectrum, their PAPR, Peak-to-Average Power Ratio, is high, meaning that the average power is much lower than its maximum value. The PA is mostly operated in lower power regions, resulting on a severe degradation of its efficiency. To be able to increase the efficiency of the PA at lower powers, different and more complex techniques must be applied.

2.7 The Doherty Power Amplifier

The Doherty Power Amplifier, DhPA, was introduced by William Doherty in 1936 in order to improve vacuum tube power amplifiers efficiency for AM broadcasts [5].

A generic schematic representing this architecture is presented in Figure 2.10 and, although there are only two branches in this Figure, it is possible to design a DhPA with a higher number of them. The branch amplifiers serve different purposes and they can be named as main and peaking amplifiers. When the device is driven by a low power signal, the main amplifier is conducting by itself. The peaking amplifier only activates when the power level increases and,

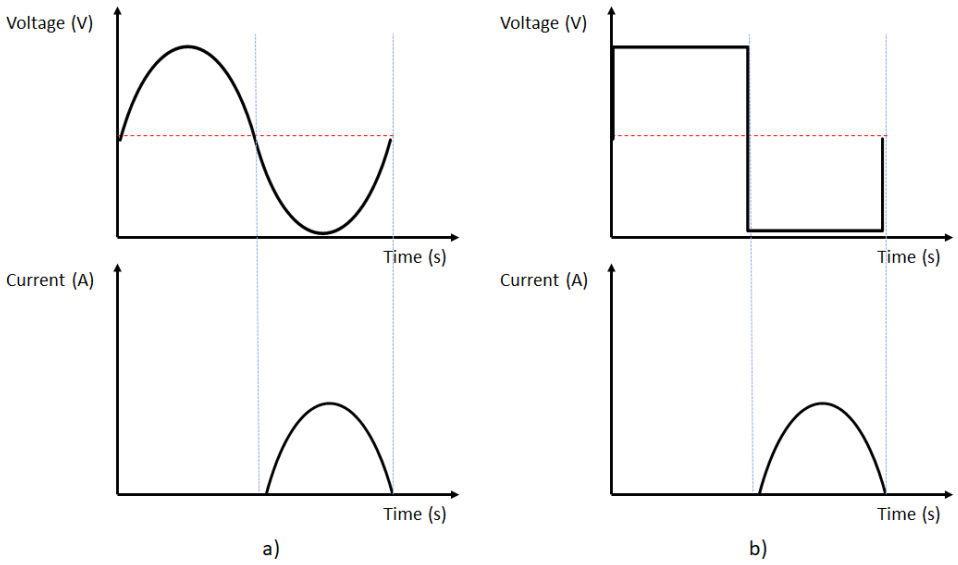

Figure 2.9: a) Class B drain voltage and drain current; b) Class F drain voltage and drain current.

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in those conditions, both amplifiers provide power to the output. To achieve this, the main amplifier is biased in class B or AB, while the peaking amplifier is biased in class C operation. When both branches are conducting, the load seen by each amplifier is affected by the other. This phenomenon is called Load Modulation. To maximize the efficiency of the DhPA, the peaking amplifier is designed to only be activated when the main one is saturated. Further improvements on the architecture may be achieved if more branches are added [25, 26] or if asymmetric power division is applied [20, 27].

The DhPA is popular for its simplicity, high efficiency at high power back-off and modulation bandwidth. However, it has its downsides: mainly its reduced linearity and low operational bandwidth. The peaking amplifier is known to cause significant amounts of distortion compromising the overall linearity of the DhPA. The power combiner at the output is

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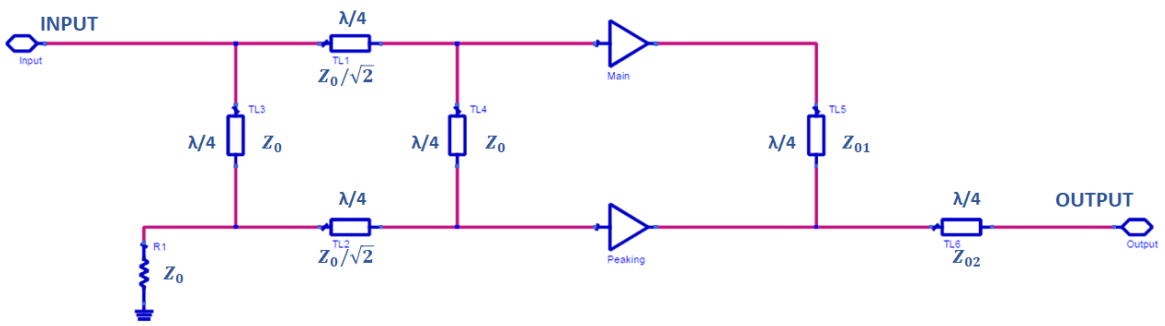

Figure 2.10: Generic schematic for the Doherty amplifier.

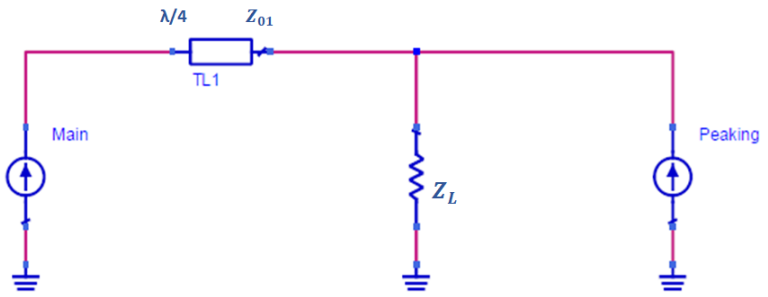

Figure 2.11: Doherty output combiner simplification

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the main contributor to the device limited bandwidth. This does not only renders the device unusable in multi-band transmitters, but causes memory effects, making it difficult to utilize predistortion algorithms [25, 28].

The load modulation in a DhPA is responsible for much of its characteristics. Being so, it is important to realize what really is the load modulation in this architecture. The best way to start is to describe the combiner as in Figure 2.11. As the active devices are not biased in saturated classes, it is reasonable to describe them as current sources dependent on the input voltage. Note that when the peaking amplifier is not conducting the circuit is simplified by the removal of its respective current source. Also, to simplify the expressions : $Z_L = \frac{Z_{02}^2}{Z0}$, assuming that the output is terminated in a Z_0 load.

So, from this circuit one can easily obtain the following load for the main amplifier:

$$Z_M = \frac{Z_{01}^2}{Z_L(1 + \frac{I_P}{I_C})} \tag{2.26}$$

So, as the currents on both amplifiers tend to equalize, the load tends to half of the value it takes when the peaking amplifier is turned off. In practice the load presented to the main amplifier at lower power is the one that maximizes efficiency in detriment of maximum output power. When the peaking amplifier is activated, the load gradually moves towards the maximum output power load. This phenomenon can be seen in Figure 2.13.

The impedance seen by the peaking amplifier can be obtained by:

$$Z_P = Z_L \left(1 + \frac{I_C}{I_P}\right) \tag{2.27}$$

The impedance starts as open circuit, when $I_P = 0$, and then it tends to $2Z_L$. This is usually designed to reach the maximum power output load, in similarity with the main amplifier's load. This is done so that the DhPA is able to deliver the maximum possible power to the load.

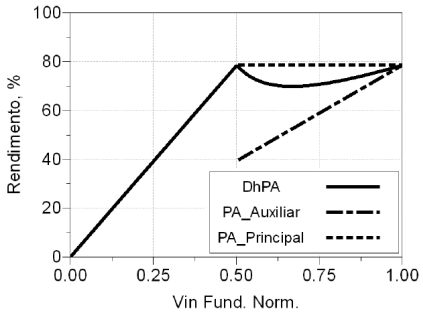

Figure 2.12: Drain Efficiency of a Doherty power amplifier and its respective branch amplifiers [20].

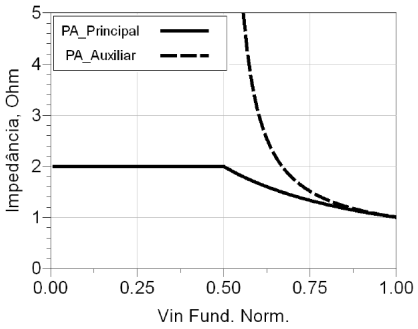

Figure 2.13: Load Modulation on a Doherty power amplifier [20].

With this, the efficiency of the Doherty power amplifier resembles the plot in Figure 2.12. This pattern portraits the behavior that was previously described. Up until the first peak only the main amplifier is turned on. Then, when the peaking amplifier starts conducting the efficiency drops. This drop is due to the extra DC consumption brought by the peaking amplifier. However, the efficiency ultimately rises again. This plot shows that the Doherty amplifier is truly able to accomplish higher efficiencies at higher output power back-off than single ended amplifiers. The practical efficiency will not be as good since in this analysis ideal transistors were considered. In real DhPAs, the first peak of the efficiency plot is most likely to be lower than the second one [20, 25, 28, 29].

2.8 The Outphasing Power Amplifier

This concept firstly appeared in 1935, presented by Henri Chireix in [6]. The broadcast base stations of that time operated at tens of kilowatts, so there was a need for highly efficient amplifiers. In his work, Chireix proposed an amplification architecture that was capable of achieving higher average efficiencies than linear amplifiers while presenting higher linearity than the nonlinear ones. Several years later, in 1974, D. C. Cox reintroduced the outphasing concept in [12], introducing the term LINC (LInear amplification using Nonlinear Components). As the name indicates, this work proposes a linear amplifier that combines the output of two nonlinear amplifiers.

2.8.1 Outphasing Concept

The basic concept of the Outphasing PA is shown in Figure 2.14 and its block diagram in Figure 2.15. Both branches are operated at a constant power level that favors efficiency. The output signal amplitude is managed by changing the phase difference of the branches. So, in order to achieve maximum output power, the signals must be in-phase. In this architecture the branches must be equal to each other in order to accomplish better linearity. The nonlinearity of the branches does not have significant influence on the overall linearity. So, if no nonlinearities are introduced by the Signal Component Separator or the Power Combiner, the device will be highly linear.

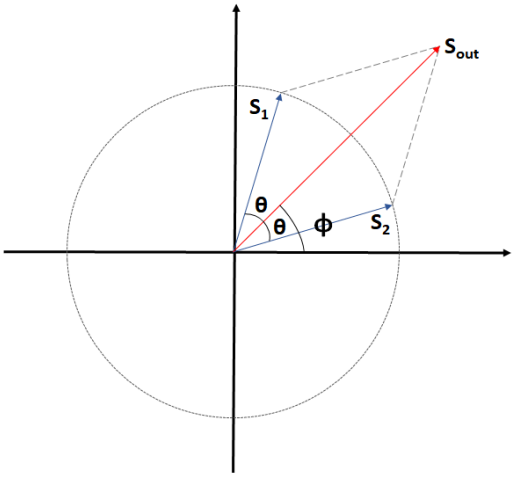

Figure 2.14: The outphasing concept from a mathematical point of view.

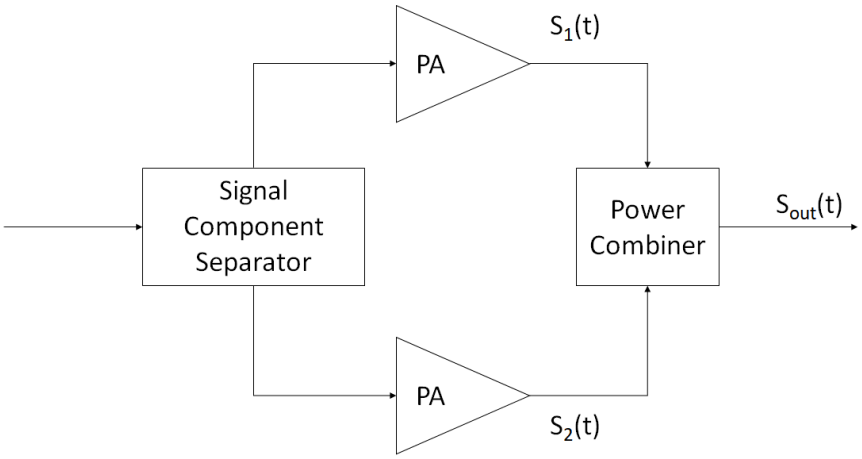

Figure 2.15: Block diagram of the Outphasing PA.

The $S_1(t)$ and $S_2(t)$ signals can be described by (2.28) and (2.29), respectively.

$$S_1(t) = A\ cos(\omega t + \phi(t) + \theta(t)) \tag{2.28}$$

$$S_2(t) = A\ cos(\omega t + \phi(t) - \theta(t)) \tag{2.29}$$

The outphasing angle is represented by θ, and ϕ represents the desired phase for the output. The output signal, $S_{out}(t)$, should be the sum of $S_1(t)$ and $S_2(t)$, as given by (2.30), where E(t) is the amplitude obtained from the outphasing process. As both phase and amplitude information are preserved, this signal should be an amplified replica of the input signal of this system. The outphasing angle can be given by (2.31).

$$S_{out}(t) = E(t)cos(\omega t + \phi(t)) \tag{2.30}$$

$$\theta(t) = arccos(\frac{E(t)}{2\ A}) \tag{2.31}$$

2.8.2 The Power Combiner

Up until now, the combiner was assumed to perform an ideal sum, i.e. lossless and the ports were isolated. However there is no real component that complies with these requirements, so some compromises must be made. Chireix proposed a lossless combiner in his work [6]. As it was not isolated, it was important to determine what would be the influence that it would have on the branches. This influence is what is described as Load Modulation. Also in his work, Chireix was able to take advantage of the Load Modulation induced by the combiner to further enhance the efficiency of his design.

Isolated Combiner

An isolated combiner can be achieved using a Wilkinson Power Combiner, represented in Figure 2.16, but the problem with this option is that the resistor needed between the input ports will dissipate power. When in-phase, that resistor does not conduct, but it increases its power consumption as the outphasing angle increases [30]. This means that for real signals the average efficiency of this architecture is low.

Although there are some proposed techniques to improve this problem [31, 32], they are not effective enough to justify the implementation of this configuration.

The Differential Combiner

The simplest concept of a lossless design is the differential combiner presented in Figure 2.17. The PAs on the branches are assumed to act as identical voltage sources, V_1 and V_2, directly applied to a floating load. V_1 and V_2 can be described as (2.32) and (2.33) so that

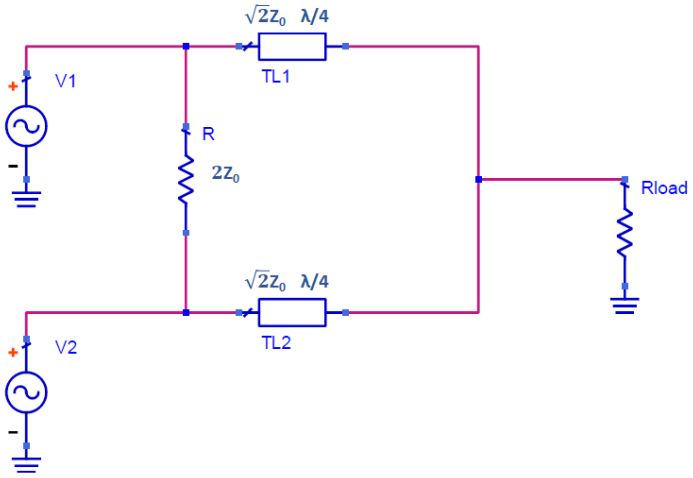

Figure 2.16: Wilkinson power combiner concept.

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the output current, I_o, is given by 2.34. The representation of the PAs as voltage sources is valid, since highly saturated amplifiers are usually used in outphasing configurations.

$$V_1 = V\ e^{j\theta} \tag{2.32}$$

$$V_2 = V\ e^{-j\theta} \tag{2.33}$$

$$I_o = \frac{V_1 - V_2}{R_{load}} = \frac{j2V\ sin(\theta)}{R_{load}} \tag{2.34}$$

Having this, it is possible to determine the loads presented to the PAs. As confirmed by (2.35) and (2.36), the PAs have a strong influence on each other. In this circuit, when the branches are in-phase there is no current flowing through the load, hence the delivered power is zero. When the outphasing angle, θ, is 90º, the load is purely real, so the delivered power peaks. This is the opposite of the behavior previously described in the outphasing concept.

$$Z_1 = \frac{R_{load}}{2}(1 - j\ cotan(\theta)) \tag{2.35}$$

$$Z_1 = \frac{R_{load}}{2}(1 + j\ cotan(\theta)) \tag{2.36}$$

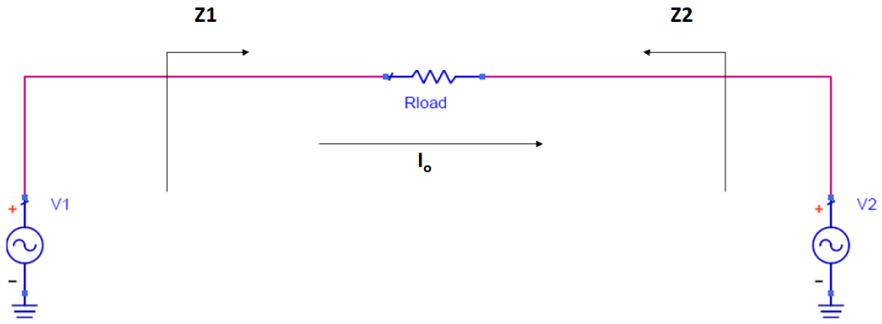


Figure 2.17: Differential power combiner concept.

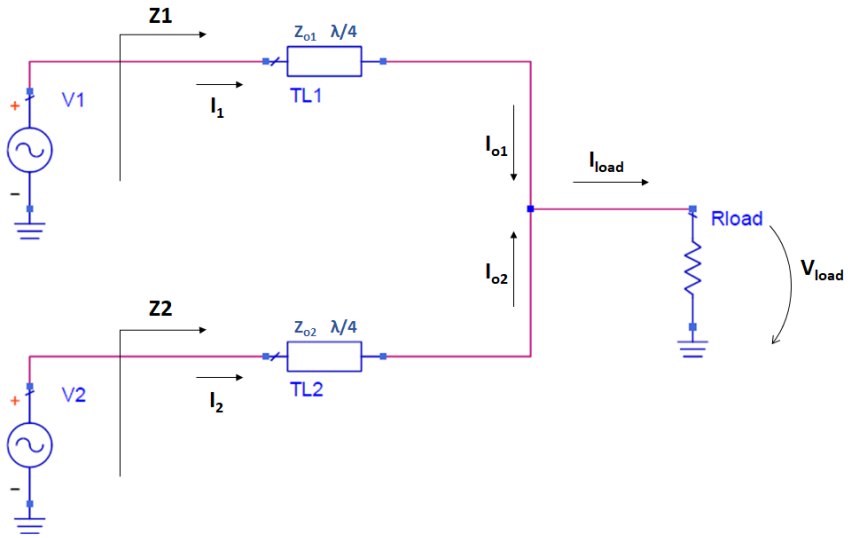


Figure 2.18: Chireix power combiner with Transmission Lines.

The Chireix Combiner

However, in the previous circuit the load is not grounded. This is a major issue for most applications, so it is important to make changes to this design. The result is the Chireix Combiner, represented in Figure 2.18. This design resembles the well-known Wilkinson Power Combiner without the resistor connecting both inputs. The lack of this resistor allows for Load Modulation, but also makes the device lossless. Again, the branch PAs are represented by the voltage sources V_1 and V_2 as in (2.32) and (2.33). With the addition of the quarter-wavelength transformer to the circuit, it is possible to determine the current at the end of the line, I_{o1} and I_{o2}, by calculating the Norton's equivalent of the voltage source/transmission line duo. The result is presented at (2.37) and (2.38). The current that flows through the load is then given by (2.39) and assuming $Z_{o1} = Z_{o2} = Z_0$:

$$I_{o1} = -j\frac{V_1}{Z_0} \tag{2.37}$$

$$I_{o2} = -j\frac{V_2}{Z_0} \tag{2.38}$$

$$I_{load} = I_{o1} + I_{o2} = \frac{2V\,cos(\theta)}{jZ_0} \tag{2.39}$$

Having this, the impedances Z_1 and Z_2 are determined by (2.40) and (2.41).

$$Z_1 = \frac{(1 + j\,tan(\theta))}{2}\frac{Z_0^2}{Z_{load}} \tag{2.40}$$

$$Z_2 = \frac{(1 - j\,tan(\theta))}{2}\frac{Z_0^2}{Z_{load}} \tag{2.41}$$

As can be seen in (2.39), the output current is now a function of cosine of θ, and the reactances in (2.40) and (2.41) are a function of a tangent of θ. This means that the maximum delivered power occurs when the branches are in-phase, i.e. $\theta = 0^o$; when $\theta = 90^o$ they cancel each other. This behavior is now in agreement with the concept of outphasing described in the beginning of this section.

From the expressions of Z_1 and Z_2, one can see that complex impedances are presented to the transistor. In fact, the only case where the reactance is null is when the branches are in-phase. This has some implications in terms of power delivery to the load and, consequently, affects the overall efficiency of this architecture. There is an important metric to take into account in this situation, the Power Factor, PF, that is used to measure the impact of the reactive impedance. In fact, some authors utilize this concept to define the combiner efficiency [3, 4, 30].

$$PF = \frac{P_{active}}{\sqrt{P_{active}^2 + P_{reactive}^2}} = cos(\theta) \tag{2.42}$$

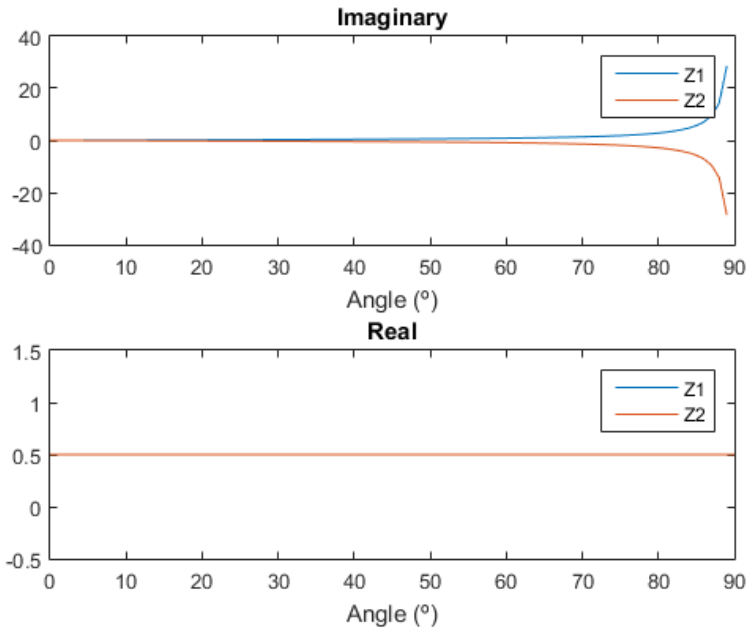


Figure 2.19: Impedances presented to each PA in a non-compensated Chireix.

The efficiency of the overall Chireix amplifier is given by (2.43). If the branch amplifiers are operated in class B, the efficiency would be (2.44).

$$\eta = PF * \eta_{branchPA} \tag{2.43}$$

$$\eta = PF * cos(\theta) * \frac{\pi}{4} \tag{2.44}$$

The impedances seen by the branch PAs are depicted in Figure 2.19 showing that the real part remains constant as the imaginary part increases with the outphasing angle. The power factor is also shown in Figure 2.20.

So far, this configuration does not fulfill the true purpose of the Outphasing amplifier: higher efficiency at higher Output Power Back-Off, OPBO. Maximum efficiency is obtained when the signals are in-phase which is also the case when maximum output power is obtained.

Chireix Combiner with Compensation

There is a way to overcome the shortcomings of the previous design: the introduction of compensation impedances to tune-out the reactances at certain angles. Having no imaginary part in the load impedance increases the efficiency for different angles than before. The impedances presented to the PAs, Z'$_1$ and Z'$_2$, can be given by the following equations:

$$Z_1' = \frac{1 + j\,tan(\theta) \; - j\,tan(\theta_{comp})}{2} \frac{Z_0^2}{Z_{load}} \tag{2.45}$$

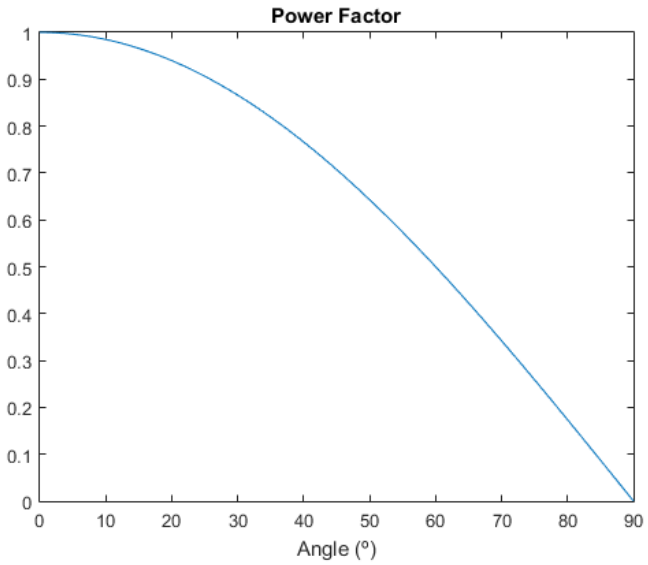


Figure 2.20: Power Factor in a non-compensated Chireix.

$$Z_2' = \frac{1 - j\,tan(\theta) + j\,tan(\theta_{comp})}{2} \frac{Z_0^2}{Z_{load}} \tag{2.46}$$

This means that the impedances can be a series inductor with impedance obtained by (2.47) and a series capacitor obtained by (2.48).

$$Z_{comp1} = -j \frac{tan(\theta_{comp})}{2} \frac{Z_0^2}{Z_{load}} \tag{2.47}$$

$$Z_{comp2} = j \frac{tan(\theta_{comp})}{2} \frac{Z_0^2}{Z_{load}} \tag{2.48}$$

The circuit for this concept may be found in Figure 2.21. Choosing an outphasing angle ensures that there is in fact two compensation angles, θ_{comp} and 90^o- θ_{comp}. High efficiency at these compensation angles is one of the key aspects of proper Outphasing systems [4]. One of the angles corresponds to the maximum output power, while the other one corresponds to a high efficiency point at a lower output power. The efficiency format is be defined by the chosen angle as can be seen in Figure 2.22.

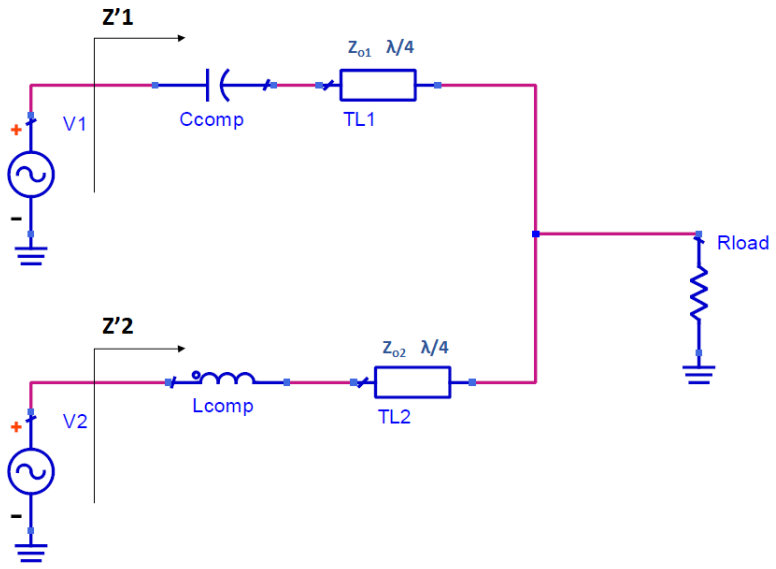


Figure 2.21: Chireix power combiner with load compensation.

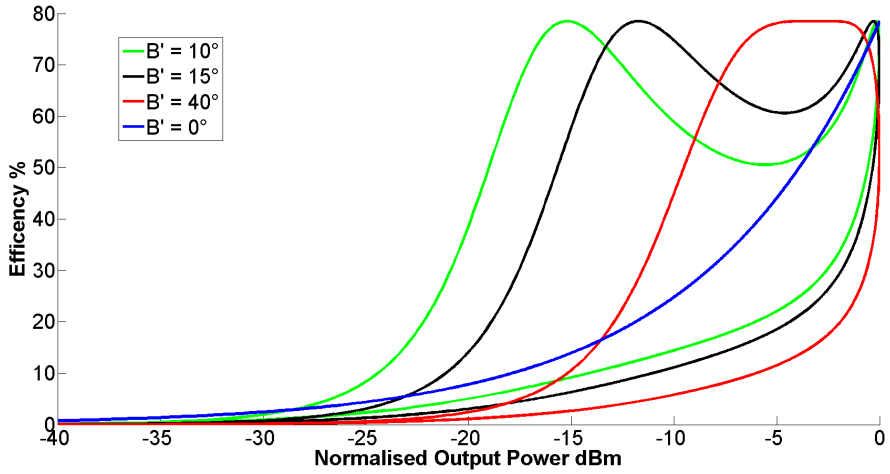


Figure 2.22: Chireix's efficiency for different compensation angles [33].

Chapter 3

The Outphasing Design

3.1 Introduction

This work proposes the full design and implementation of a power amplifier for 2.45 GHz that maximizes power efficiency in a Outphasing architecture. The transistor selected for this purpose is the CGH 40010F, from Cree [34], and the substrate used is the Rogers RO4350B [35].

3.1.1 Concept

The previously presented Outphasing architecture exhibits a major downside that severely compromises its implementation. In its conceptualization, the Outphasing amplifier proposes that the input power remains the same, regardless of the desired output power. This means that only the phase difference between the signals is changed. If PAE is considered, one may realize that, for low powers, this is not a smart approach since it implies that cases will occur where the input power is considerably higher than the output power. This leads is case, for example, where, to get 0 W at the output, the signals are outphased by 180º. In terms of energy efficiency this is not recommendable.

To address this issue, the digitally driven Outphasing, OphPA, architecture is proposed. This PA is designed to get the benefits of the Outphasing PA in high power stages, while gaining some of the advantages of the Doherty PA. The load modulation on a DhPA is controlled by its input power, while on a classical Outphasing PA, that process is controlled by its phase. The proposed architecture suggests that the load modulation should be controlled by both. The idea is to get the best possible amplifier from an Outphasing-like architecture. To get this, several input power/phase combinations must be tested. Although the controlling signals may be complicated to produce in an analogical system, modern day transmitters already utilize digital components that can be used to address this situation. So, in this architecture, the Signal Component Separator is a digital system.

There have been several approaches to amplifiers that tried to combine the advantages of the Doherty and the Outphasing PAs in recent literature [10,36–38], showing some advantages to these implementations.

In order to visualize the task at hand, the proposed amplifier can be represented by the block diagram in Figure 3.1, dividing it in four blocks. As two of the blocks are the same, this architecture is composed by three major components with the following characteristics:

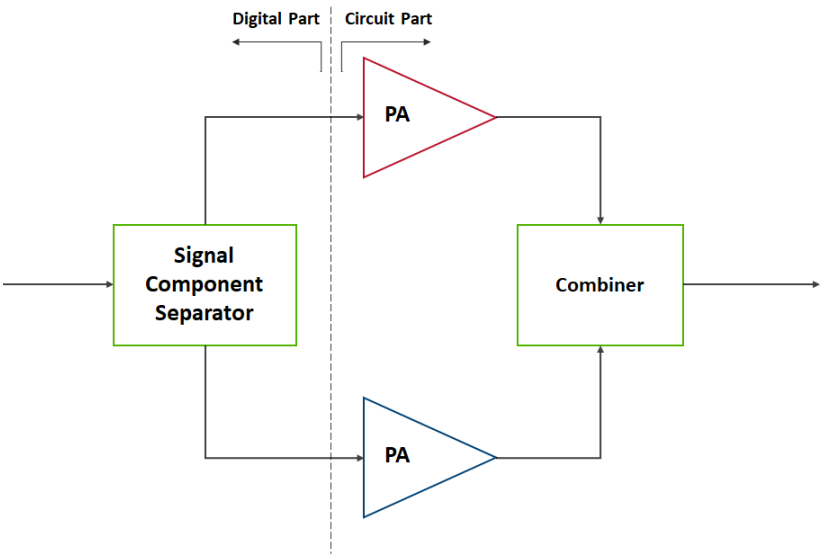


Figure 3.1: Block Diagram of the proposed OphPA.

- **Branch Power Amplifiers -** these serve a similar function as in a classical Outphasing amplifier. They should be as equal as possible to preserve linearity, and must be highly efficient. As these are classical PA classes, high efficiency may compromise linearity;

- **Power Combiner -** combines the output power of the branch amplifiers and must be design in a way that maximizes efficiency at both low and high powers. This component along with the branch amplifiers forms the analog circuit used in this architecture;

- **Signal Component Separator -** it must convert the input signal of the system into the necessary driving signals of the branch amplifiers. As this implementation allows the variation of both phase and amplitude of the driving signals, this component must be implemented in the digital domain.

3.1.2 Structure of the Design Stage

In this work, the design of the digitally driven Outphasing power amplifier was accomplished according to the following major steps: Design of a Class F PA for the branches; Design of the output power combiner; Test of the input power/phase combinations; Selection of the best driving signals; Linearization of the referred signals to simplify the practical implementation.

During the design stage, the Advanced Design Software, ADS, was used to simulate the circuits. This software allows for circuit, electromagnetic and hybrid simulations. A hybrid simulation is the usage of an electromagnetic model, obtained from an electromagnetic simulation, in a circuit simulation. With this, the results are much closer to the practical implementation.

3.2 Branch PA

The branch amplifier is supposed to be a highly efficient one. Among the present operation classes, the one that better fulfills these needs is the class F PA. With the operation class established, it is important to outline some primary design goals and characteristics.

As stated, class F, in theory, requires all harmonic frequencies to be treated, but that is not a realistic goal. There are mainly two limiting factors that determine how many harmonics can be treated: the first being the length and complexity of the matching network needed to produce the required load terminations; and the second being the limits of the transistor model in terms of frequency. As the PA is being designed for a fundamental frequency of 2.45 GHz, only the second and third harmonics will be taken into account. The main goal for the load termination at the fundamental frequency is to be the one that maximizes power added efficiency, as that is the most reliable metric to measure PA efficiency. This was set this way, because through experimentation it was observed that the overall OphPA would achieve higher PAE values with this termination than when presented with one that maximizes output power. This will be explored later in this document. In order to transmit a real telecommunications signal, the PA must be able to respond as equally as possible within a certain bandwidth. For this class F PA, the goal is to have a good response in a 200MHz bandwidth centered at 2.45 GHz.

3.2.1 Biasing of the transistor

As previously said, the selected transistor is the CGH 40010F from Cree and it is a GaN HEMT RF transistor. The datasheet for this device provides useful information on how to properly bias the transistor. It is recommended that the Drain to Source Voltage, V_{DS}, should be 28 V. With that settled, the Gate to Source Voltage, V_{GS}, needs to be chosen.

In a real transistor the Threshold Voltage, Vth, is not as clearly defined as in the amplifier theory. The transition between the cut-off and conduction regions is not abrupt, it is smooth, implying that it is harder to define. A good way to do this is to measure the evolution of the Drain Current, I_{DS}, with V_{GS} and finding its inflexion point [19]. This was performed using a simulation model of the chosen transistor in a simulation environment. The results are presented in Figure 3.2. In this plot, V_{th} was determined to be -3.135 V.

Also in Figure 3.2, there is a marker named BiasPoint. As the name indicates, this is the chosen bias point for the transistor. One may realize that, since it not biased with $V_{GS} = V_{th}$, this deviates from the class F definition. That is in fact a true statement, however, this value was chosen through load-pull simulations in order to maximize the PAE values in high power regions in this specific configuration. Those load-pull were repeated for several bias points, and the maximum PAE loads were compared. Through these tests, the chosen bias point was observed to be the one that better fulfilled that role. During this process the measurements were always done for a 3dB gain compression. The reasons for this are stated in the next section. Table 3.1 displays the DC values of V_{GS} and I_{DS} for the chosen bias point.

$\mathbf{V_{GS}}$	$\mathbf{I_{DS}}$
-2.9 V	0.111 A

Table 3.1: Bias Point of the branch transistors.

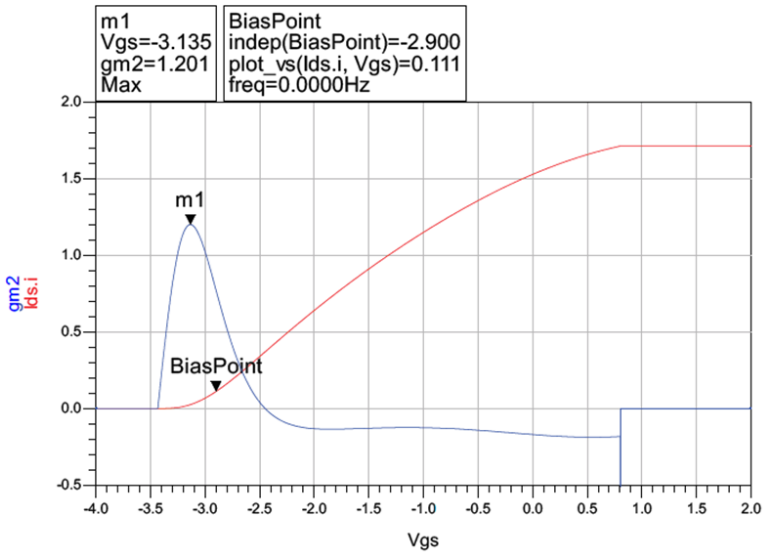


Figure 3.2: I_{DS}/V_{GS} simulation using the CGH 40010F model (red plot: I_{DS}; blue plot: second derivative of I_{DS}).

3.2.2 Load-Pull

A good way to increase the maximum efficiency of a PA is to drive the transistor further into the gain compression region. The cost of that is, naturally, a decrease in linearity. So, although these load-pull simulations are typically performed for 1dB gain compression, in this case the transistor will be tested at 3dB gain compression.

Load-pull simulations or measurements are crucial in PA design. They are performed by varying the load presented to a transistor and measuring the output power and efficiency. It is well-known that different loads provide different values to these metrics and these tests allow them to be mapped in a Smith Chart.

Through load-pull simulations, the output power and efficiency contours may be plotted in a Smith Chart and the desired load terminations may be selected. Since the amplifier is being designed to operate within a certain bandwidth, this process needs to be performed in that range of frequencies. The load modulation in the OphPA will move the load from the maximum efficiency termination to the maximum output power one. So, when designing the branch amplifier, either load may be chosen. Both cases were tested in this work, and it was concluded that the overall architecture would benefit from higher efficiency peak values if, in this stage, the maximum efficiency load was to be selected.

The load terminations at the harmonics also need to be determined. Although, in theory, they are either short or open circuits, in a real transistor, the parasitic components may deviate these loads. So a load-pull must also be done at the harmonic frequencies. Figure 3.3 shows the plot for the 2^{nd} and 3^{rd} harmonics of the fundamental frequency of 2.45 GHz. In these plots the chosen loads are identified and correspond to the ones that maximize efficiency. The chosen loads are presented in Table 3.2 along with their characteristics.

With that settled, the load termination at the fundamental frequencies was adjusted. Figure 3.4 shows the plot at 2.45 GHz. The load that provided the maximum efficiency was selected for all the bandwidth. Table 3.3 shows the chosen fundamental terminations.

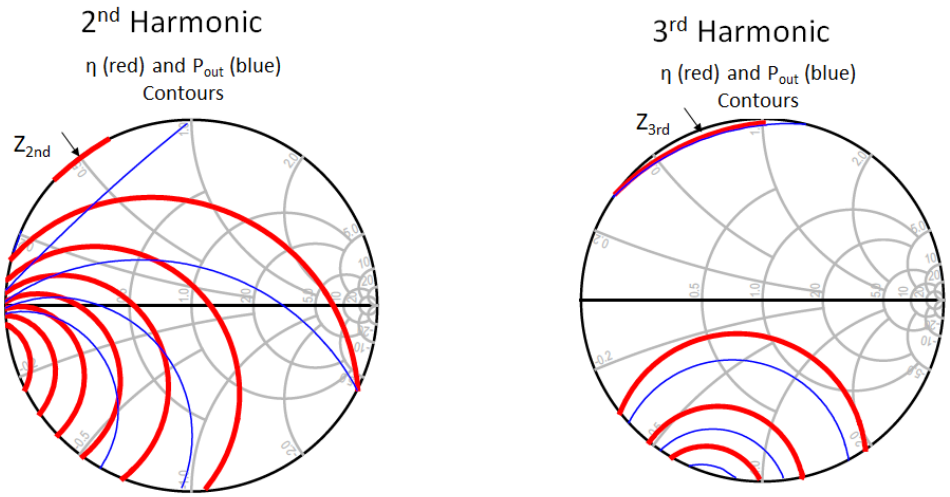


Figure 3.3: Load-Pull results for the second and third harmonics of the fundamental frequency of 2.45 GHz. The blue lines represent the P_{out} contours and the red lines the η ones.

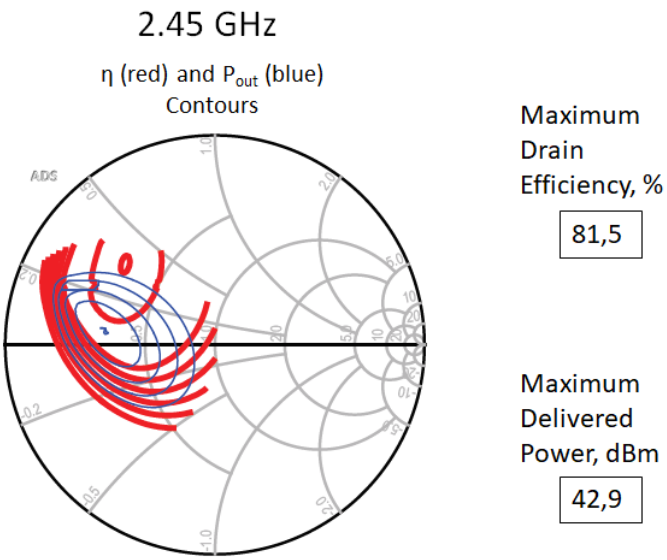


Figure 3.4: Load-Pull results for 2.45 GHz. The blue lines represent the output power contours and the red lines the η ones.

Second Harmonics

4.7 GHz	4.9 GHz	5.1 GHz
$3.2 * 10^{-4} + j\ 27.3\ \Omega$	$3.1 * 10^{-4} + j\ 23.7\ \Omega$	$2.9 * 10^{-4} + j\ 20.6\ \Omega$

Third Harmonics

7.05 GHz	7.35 GHz	7.65 GHz
$4.1 * 10^{-4} + j\ 40.4\ \Omega$	$3.42 * 10^{-4} + j\ 30.3\ \Omega$	$3.2 * 10^{-4} + j\ 27.3\ \Omega$

Table 3.2: Harmonic terminations obtained from a load-pull simulation.

In-band Frequencies

Frequency	2.35 GHz	2.45 GHz	2.55 GHz
Load (Ω)	$14.9 + j\ 19.3$	$15.6 + j\ 17.3$	$15.1 + j\ 18.1$
η_{max} (%)	82.74	81.50	82.55
P_{max} (dBm)	40.08	40.34	40.01

Table 3.3: In-band terminations obtained from a load-pull simulation.

3.2.3 Output Matching and Bias Network

The loads were determined in order to maximize efficiency throughout the passband. However, these loads are very close to each other, so the output matching network must be able to present only a slight impedance variation between 2.35 GHz and 2.55 GHz. The harmonic frequencies also need to be addressed. Although in this stage a 50 Ω termination is assumed, when the branch PA is employed in the Oph configuration, the load-modulation will present different loads. This phenomenon is not only expected, but it is also desired in the passband frequencies. At the harmonic frequencies, however, the load modulation should not influence the impedance seen by the transistor. So, the output matching network must be designed to guarantee this.

In this work, in order to fulfill all the specifications, the design of the output network was divided into two stages. The harmonic terminations were projected along with the bias network, and only then the passband terminations were designed.

The bias network is used to deliver DC power to the transistor drain and it must not affect the impedances seen by it at passband frequency. Since the DC voltage source is seen by the signal as a short circuit, adding a quarter wavelength transformer will turn it into an open circuit. That open circuit will be in parallel with the rest of the matching network, so it will not affect the impedance at those frequencies. However, only ideal voltage sources can be considered short circuits, real voltage sources at these frequencies will present unpredictable behaviors, so the short circuit must be created in a different way. A good way to do it is by adding a parallel open stub or a capacitor at the end of the line. In this case, a radial stub was designed to this effect because, in this configuration, it presented lower impedance variation than a capacitor. It is common practice to place some parallel capacitors after the stub in order to eliminate out-of-band frequencies.

With the bias network designed, the second and third harmonic terminations must be dealt with. The optimum impedances were already established, but, in order to accomplish

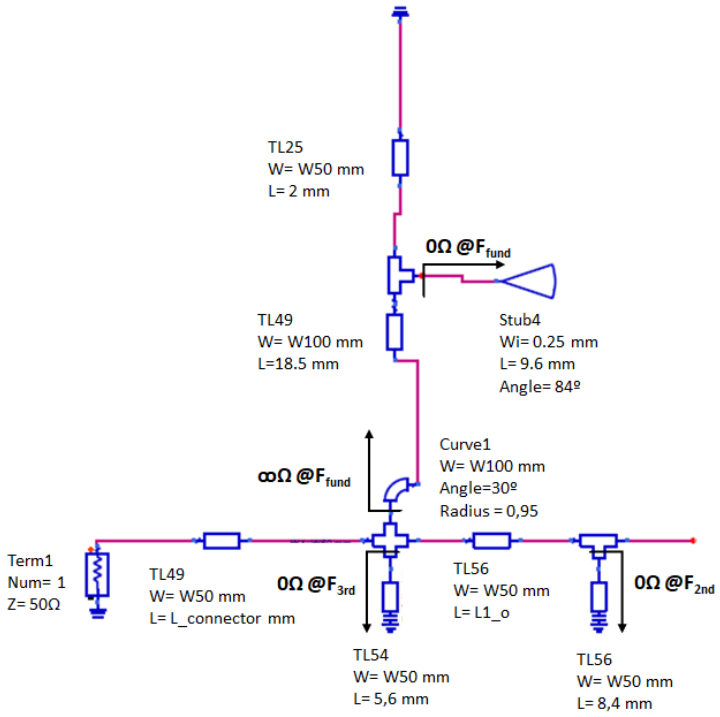


Figure 3.5: Schematic of the first part of the output matching network.

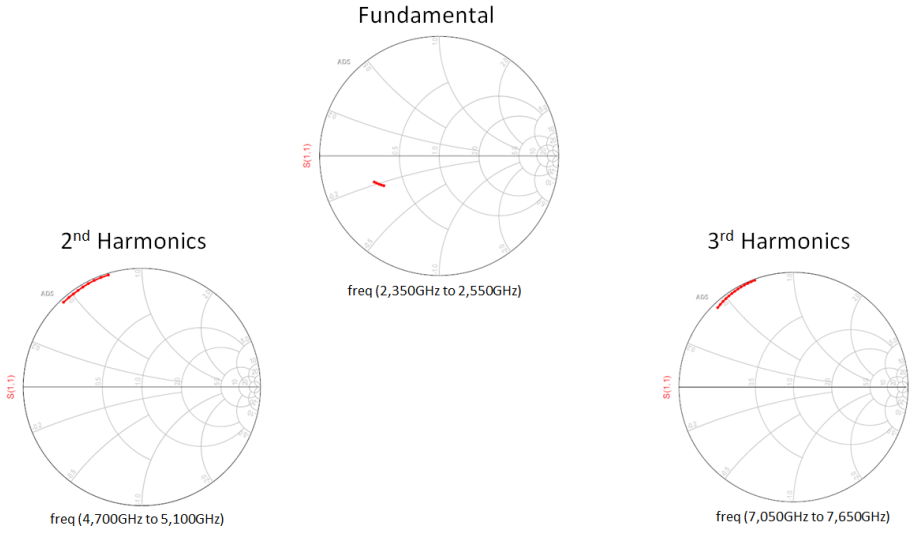
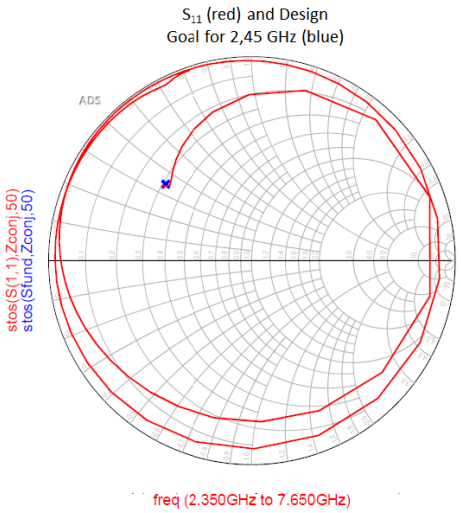


Figure 3.6: Resulting impedances of the first part of the output matching network terminated with a 50 Ω load.



Frequency (GHz)	Impedance (Ω)
2.35	15,15 + j 16,44
2.45	16,09 + j 17,03
2.55	16,57 + j 17,62

Figure 3.7: Smith Chart from 2.35 to 7.65 GHz of the impedance seen by the transistor drain and in-band load information.

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all the goals with a simple network, these only served as reference point, not as a rigorous design goal. A good way to make these terminations independent from the presented load is to create parallel short circuits. These can either be obtained by a parallel capacitor or a parallel stub with the RF path. The latter option was chosen in this implementation. Since the desired load terminations to the harmonics are on the outskirts of the Smith Chart, the short circuit only needs to be preceded by a transmission line in order to place them where they should be. It is also important to ensure that the impedance variation in the 2nd and 3rd harmonic bandwidths[1] is low. Several variations were tested and the one that showed the best results was chosen.

The final network is shown in Figure 3.5. This network produces the impedances presented in Figure 3.6 when terminated with a 50 Ω load. Several load terminations, ranging from a short circuit to an open circuit, were used to test this network. The impedances at the harmonics remained the same for all these cases, showing that the desired design goals were accomplished.

With the first part of the network design concluded, the passband impedances must be generated. There are mainly two goals in this stage: the impedances must be as close as possible to the ones determined through the load-pull simulation; and the network must present low losses. As stated earlier, the loads are very close to each other, so the variation must be very low. A good way to do this is to create a resonance around that frequency range, that can be achieved through two sets of line/stub. A capacitor is also placed in series with the network to block any DC components. To measure the losses, the S_{21} parameter is measured to guarantee that it does not decrease from -0.5dB. The complete network results for the impedances are presented in Figure 3.7. As seen in Figure 3.8, the S_{21} parameter is always above -0.26 dB with a variation around 0.04dB through the entire band of 2.35-2.55 GHz. The final network dimensions are stated in Table 3.4 and the schematic is shown in

[1] 4.7-5.1 GHz and 7.05-7.65 GHz, respectively

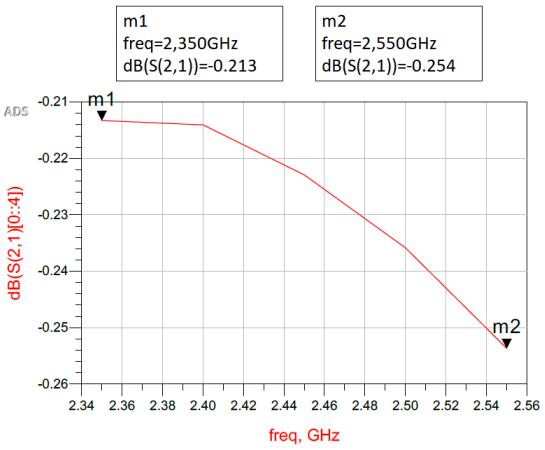

Figure 3.8: S_{21} parameter in dB from 2.35 to 2.55 GHz.

Figure 3.9.

3.2.4 Input Bias Network

The output termination is the one that defines most of the PA characteristics, but the input network defines its gain. But, before starting to design the matching network, the bias network must be devised. Similarly to the output, the goal is to provide a DC power to the transistor, in this case to its gate, and to minimize its influence in the RF signal. It should present an open circuit between 2.35 and 2.55 GHz. The way to produce this is the same as before, a short circuit at those frequencies must be created at the top and a quarter wavelength transformer will turn it into an open circuit. This time, a parallel capacitor substitutes the radial stub. The capacitor offers the advantage of being smaller than the stub and, since a real model is used, the results are reliable. After the capacitor, a 25 Ω resistor was placed to deal with the stability problem, but this will be explored later. The final design is presented in Figure 3.13 along with the rest of the input network and, in Figure 3.10 the impedance results for the bias network.

3.2.5 Input Matching Network

The input termination determines the gain of the PA. Naturally, the gain is an important parameter since it directly affects the PAE of the amplifier. To maximize gain, the input matching network must be designed to present complex conjugate matching. The problem is when the amplifier is unstable. If that happens, its gain must be reduced.

With this transistor, the PA becomes potentially unstable at the passband frequencies if the maximum gain is applied. There are some different techniques for gain reduction that can be applied, and in this case two of them were used. The first is to mismatch the input matching network. A source pull simulation may be performed to test the possible impedances. This simulation, presented in Figure 3.11, was used to choose the impedance for the input matching. The gain was reduced from around 22 dB to 14.8 dB. To obtain this gain and use a purely real impedance, the input matching network must produce a 25 Ω

Dimensions	mm
W_connector	1.40
L_connector	2.00
L_cap	4.60
L1_o	0.20
L2_o	1.51
L3_o	14.09
L4_o	3.10
L5_o	7.96
L6_o	11.20
W3_o	1.26
W5_o	2.50
W50	1.65
W100	0.39

Table 3.4: Final output matching network dimensions.

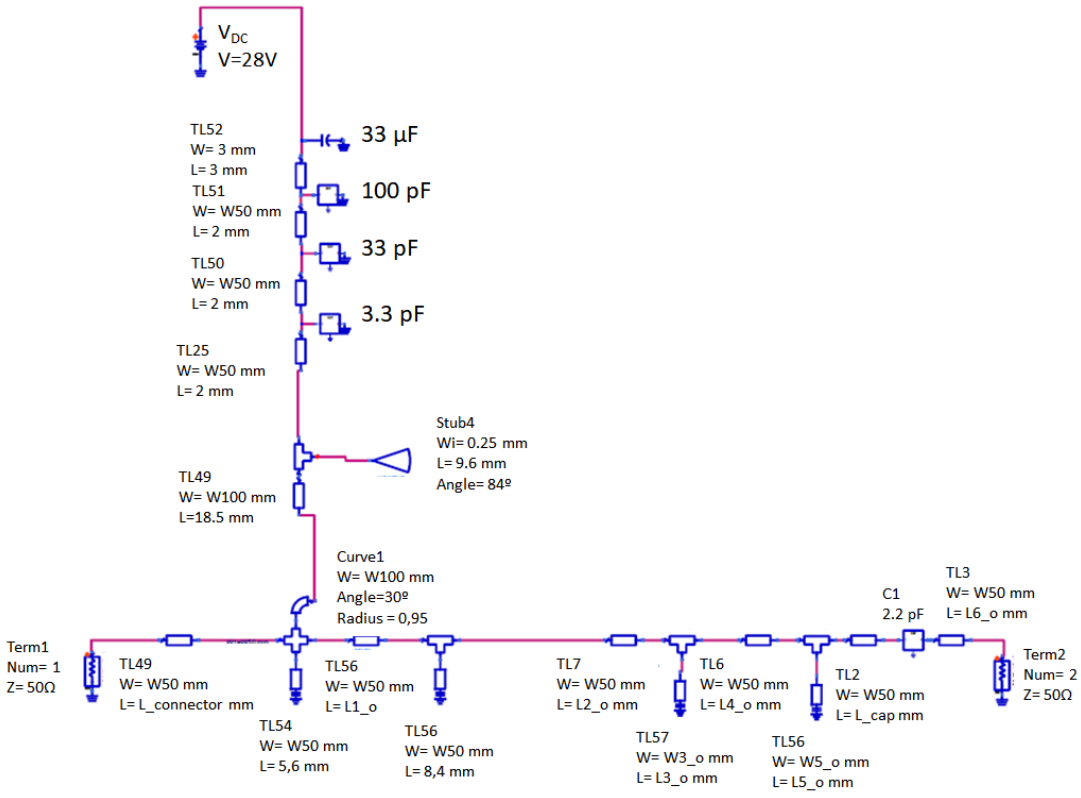

Figure 3.9: Final Schematic of the output matching network.

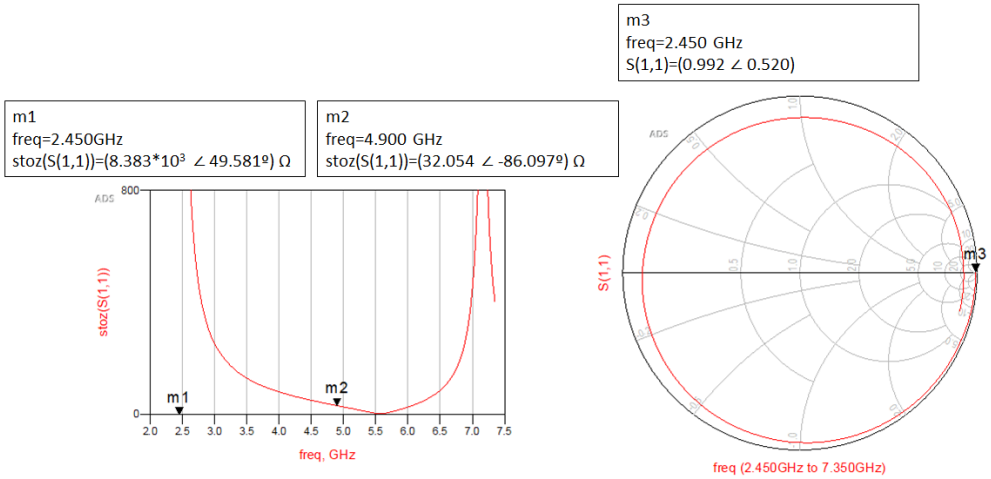

Figure 3.10: Impedance results of the input bias network.

impedance. The second gain reducing technique employed was the usage of a resistor in series with the bias network, but the reason for this will be discussed later in this document.

The main goal for the input matching network is to generate 25 Ω while not allowing the impedance to change too much in the passband frequencies. The losses on this network are also important, and they were set to be as low as possible and to be constant throughout the entire band. A DC block capacitor also needs to be used just as in the output network and the chosen value was 3.3 pF. One may notice that there is a capacitor in parallel with a resistor in this network. That is used to guarantee stability in the lower frequencies, but this is to be further explored later. The final network is presented in Figure 3.13 and the results are presented in Figure 3.12. The impedance, although it presents some variation, follows the desired pattern shown in Figure 3.11 and the S_{21} varies between 0.599 dB and 0.605 dB showing consistent and low losses in passband.

3.2.6 Stability

If this branch PA was to be used by itself, i.e. as a single-ended PA, the stability challenge would be simpler. However, since load modulation will occur, guaranteeing stability in the center of the Smith Chart is not enough; all the loads presented to it must be inside the stable region.

The first design of the input bias network did not include the gain reducing techniques described earlier[2]. Those additions were made afterwards, after analyzing the PA stability. There are mainly two stability measurements that should be performed: one for small signals; and another for large signals.

When dealing with small signals, it is important to analyze the entirety of the spectrum

[2] The resistor in the bias network, the capacitor/resistor parallel in the matching network and the impedance mismatch

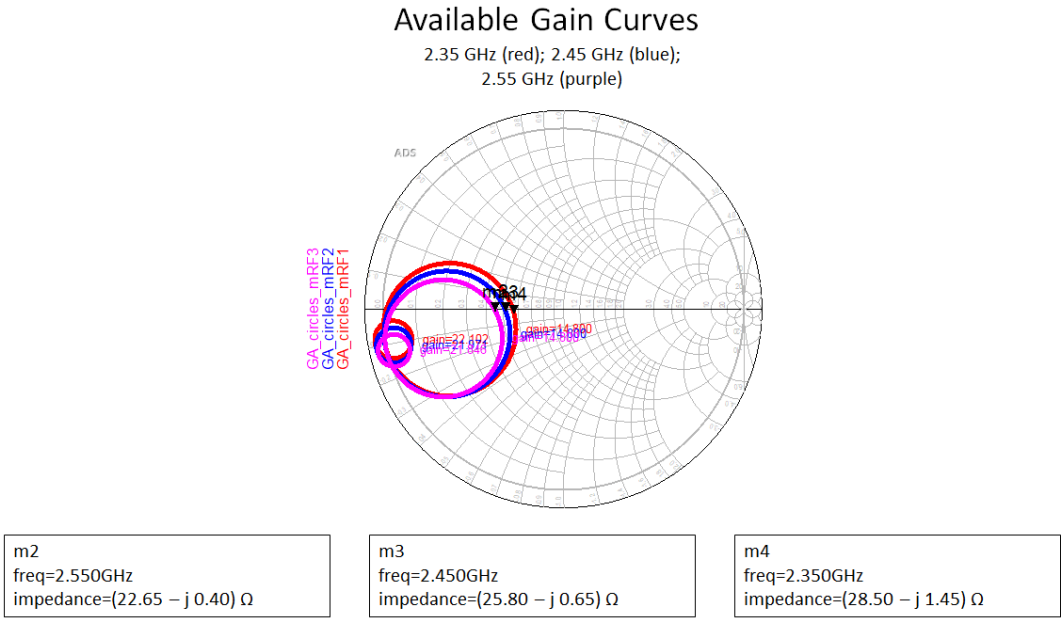

Figure 3.11: Source Pull Results for the chosen gain reduction. The three frequencies analyzed are plotted: 2.35 GHz (red); 2.45 GHz (blue); and 2.55 GHz (purple).

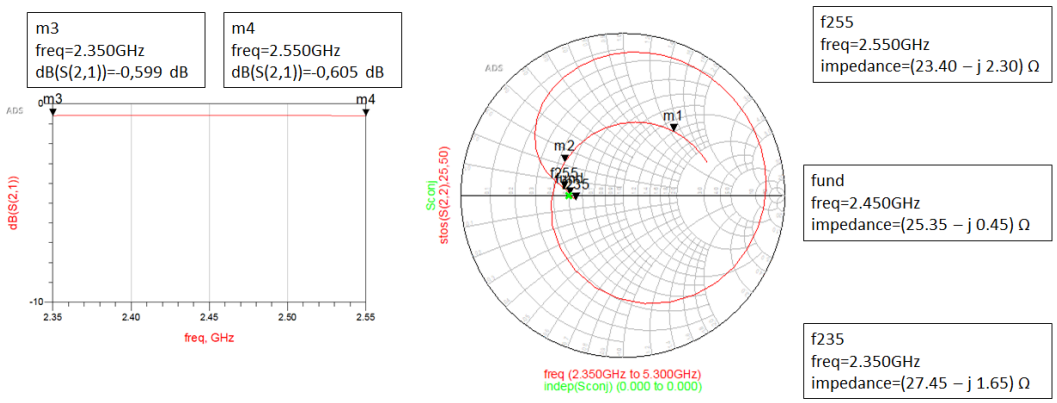

Figure 3.12: Impedance and S_{21} results of the input matching network.

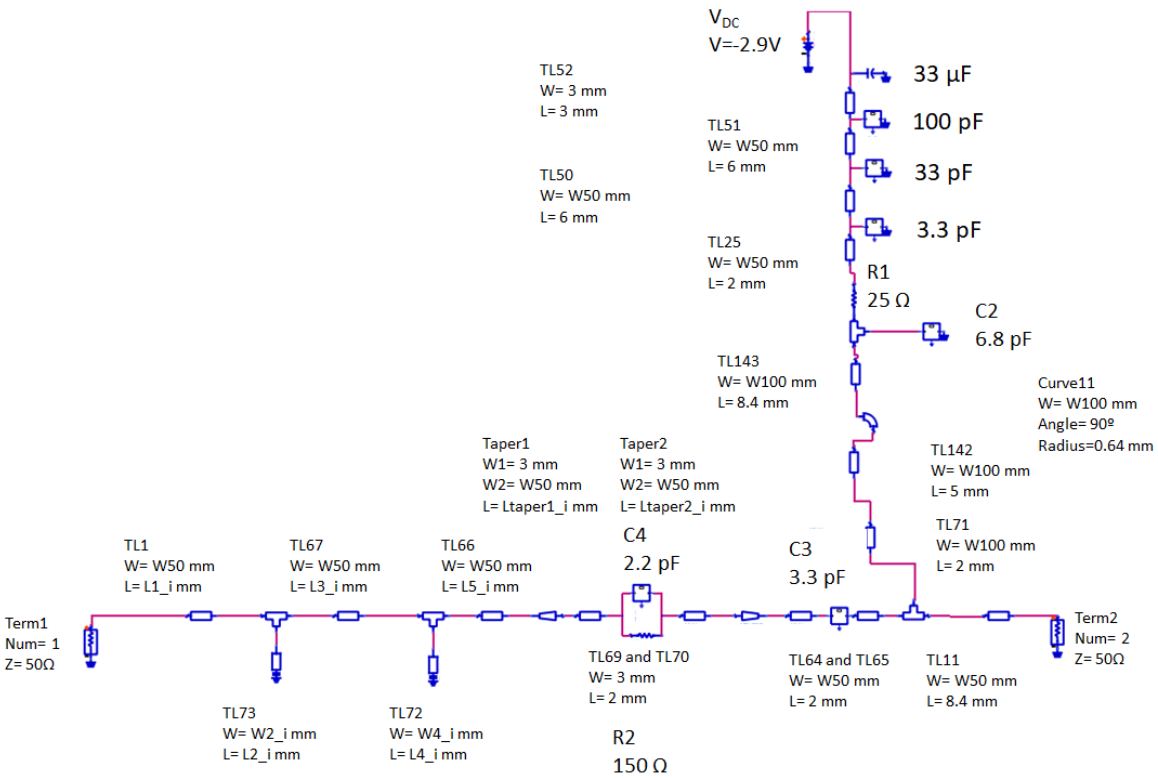

Figure 3.13: Final Schematic of the input matching network.

Dimensions	**mm**
L1_i	0.50
L2_i	7.32
L3_i	9.20
L4_i	10.97
L5_i	12.30
Ltaper1_i	0.50
Ltaper2_i	0.50
W2_o	1.83
W4_o	2.50

Table 3.5: Final input matching network dimensions.

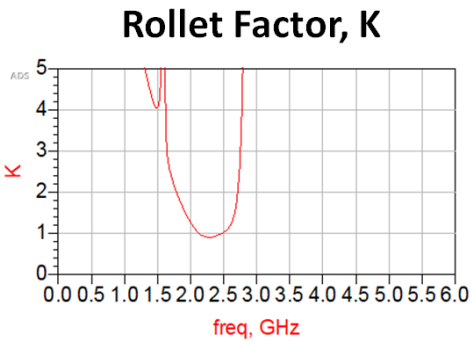

Figure 3.14: Rollet Factor of the branch PA from 0 to 6 GHz.

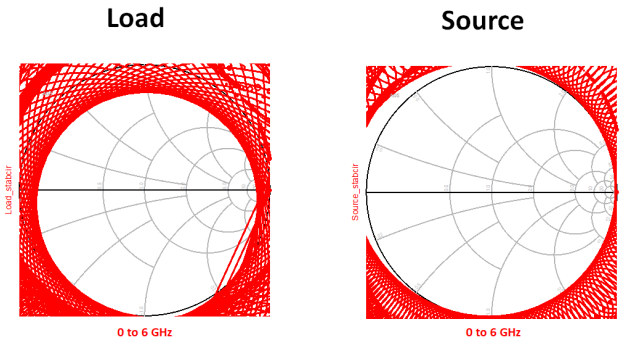

Figure 3.15: Small signal stability curves of the branch PA from 0 to 6 GHz.

in which the active device operates. In this case from 0 to 6 GHz. One way to do it is to plot the input and output stability curves to ensure that all the desired load terminations are in the stable region. This can be a cumbersome endeavor, but there is a way to do this more efficiently: to calculate the Rollet factor, K. This way, the unconditionally stable frequencies can be excluded from the analysis. As stated, the first design of the input matching network was shown to be potentially unstable. There were mainly three problematic frequency bands: 0.1-0.4 GHz; 0.55-1.25 GHz; and 2.0-3.0 GHz.

The first two can be simply dealt with by adding a parallel RC low pass filter in series with the input network.This reduces the gain to these frequencies, while not affecting the RF frequencies. The components were adjusted to be a 2.2 pF capacitor, C4, and a 150 Ω resistor, R2.

The other band presents a different challenge, since it encompasses the passband frequencies. Here the adjustments must be made prudently so that the amplifier can still retain as much gain as possible. The first implemented technique was the mismatch of the input matching network. The final value was obtained by slowly mismatching the amplifier until the results were satisfying. The final value, as shown in Figure 3.11, was around 14.8dB. After this was implemented, there was still some risk of entering the unstable region. Another technique was employed to solve this problem: a resistor was added in series with input bias network. A 25 Ω resistor, R1, was adjusted to fulfill this purpose.

After these additions, the simulation results of the stability curves, as well as of the Rollet factor, confirm that there is no longer the risk of instability of the PA. The K factor is presented in Figure 3.14 and Smith Charts with the circles of the input and output loads for small signal is presented in Figure 3.15. Although some curves intersect the Smith Chart, the loads presented to the amplifier were confirmed to be well within the stable region.

At last, since large signal will only occur in the passband, there is no interest in testing any other frequency range. In Figure 3.16, the curves are plotted for 2.45 GHz with Pin varying from 10 to 30 dBm. This simulation was repeated throughout the passband, showing similar results. These results confirm that the PA is stable for both large and small signal operation.

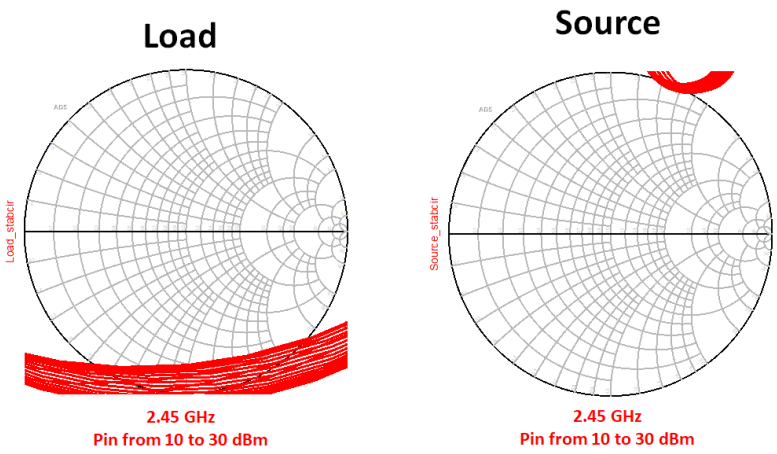

Figure 3.16: Large signal stability curves of the branch PA for 2.45 GHz.

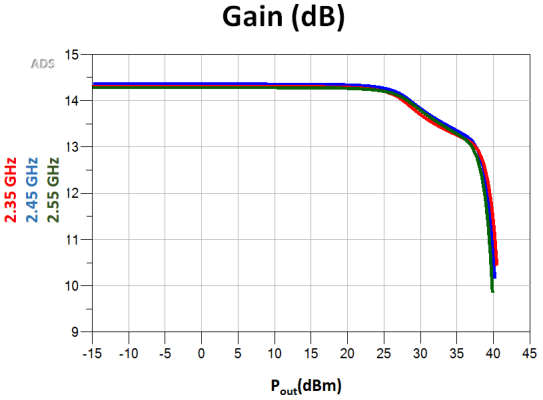

Figure 3.17: AM-AM characterization across the passband.

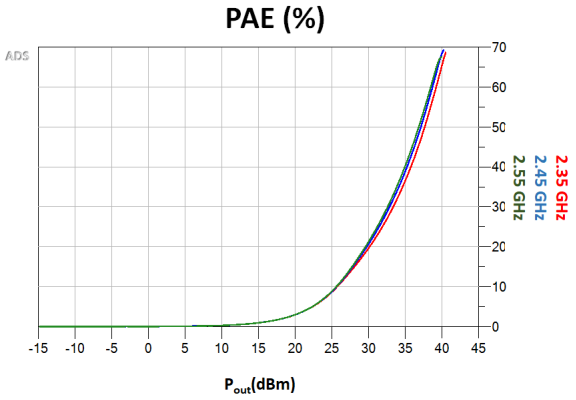

Figure 3.18: PAE measurement across the passband.

3.2.7 Simulated Results

The branch amplifier is finally concluded and ready to be tested. Since the goal is to incorporate this PA in a Oph architecture, at this stage only circuit simulations are performed and distortion characterization is not required. The most important metrics at this stage are gain and efficiency. The PA must also present similar values for these metrics between 2.35 GHz and 2.55 GHz. Figure 3.17 and 3.18 display these informations for 2.35 GHz, 2.45 GHz and 2.55 GHz, showing that the PA gain and efficiency maintain a similar response in this bandwidth with the maximum gain varying between 14.28 dB and 14.35 dB. In order to increase the overall efficiency, the amplifier is driven to a 3dB gain compression point, as has already been discussed, so it is important to characterize the device at this point. Table 3.6 presents these informations, confirming the PA consistency within the desired bandwidth.

	2.35 GHz	2.45 GHz	2.55 GHz
$\mathbf{P_{out}}$ **(dBm)**	39.96	39.76	39.31
$\boldsymbol{\eta}$**(%)**	70.31	72.72	70.68
PAE (%)	65.29	67.28	65.45

Table 3.6: Pout, η and PAE results for a 3dB gain compression point.

3.3 Digitally Driven Outphasing Amplifier

With the branch amplifier fully designed, the challenge is to implement it in an Outphasing architecture. This amplifier is not a well established concept in state-of-the-art literature, so it is important to set up some of its characteristics. The circuit configuration of this PA is the same as the classical Outphasing amplifier: two highly efficient PAs are used and their outputs are merged using a Power Combiner. Both branch amplifiers should be as equal as possible. The criteria for the combiner configuration should also be the same, so a Chireix power combiner is used in this work. What sets this OphPA apart from the classical Outphasing PA is how the circuit is used. The input signals should be determined through intensive tests in order to obtain the signals that maximize the efficiency of the amplifier. As the resulting signals may be complex, the Signal Component Separator is a digital system.

With that settled, the next step is to design the output power combiner. As the impedance presented to each transistor is supposed to move from the maximum efficiency to the maximum output power load, the combiner must be conceived to that end. But first, those loads need to be located. To do so, a load-pull simulation may be done to the branch amplifier. After the combiner is designed, all the reasonable input power/phase combinations must be tested in order to extract signals that produce the best results.

At the end of this stage, a layout is produced to generate a electromagnetic model that is then used to validate the design. With satisfying and consistent results, a circuit can be fabricated from this layout.

3.3.1 Branch Amplifier Load-Pull

In order to properly design the power combiner, it is important to determine which are the loads that most benefit the branch amplifier. So a load-pull simulation needs to be done using the complete design of the amplifier. Through this simulation, the efficiency and output power contours are plotted and can be used as a reference when designing the combiner. The load modulation, may then be used to move between the maxima of efficiency and power.

With the designed PA, the resulting contours are demonstrated in Figure 3.19 for a input power of 28 dBm and 2.45 GHz. The markers m1 and m2 respectively show the maximum efficiency and maximum power loads. This input power was chosen because the 1-tone analysis has shown that it is the one that grants a higher PAE. For the other in-band frequencies, the position of the contours rotate counterclockwise with the increase of the frequency. This causes some problems with the bandwidth of the overall architecture as it will be further explained in this document.

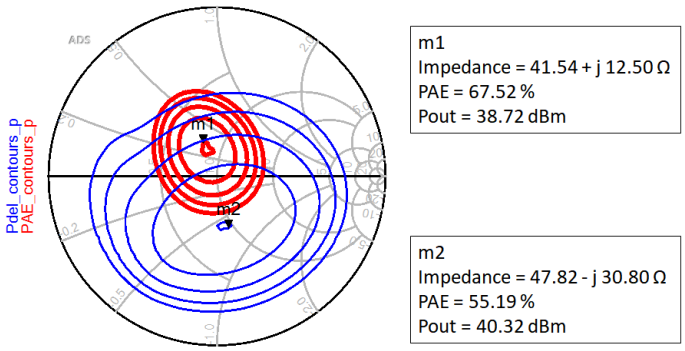

Figure 3.19: Load-Pull simulation of the branch PA with m1 and m2 corresponding to the maximums of efficiency and power, respectively.

3.3.2 Output Power Combiner

Designing the output power combiner is one of the main steps to produce an Outphasing PA. Among the known combiners, the Chireix Combiner with Compensation was chosen for this application. As explained earlier in this document, the compensation is performed for certain angles in order to increase efficiency at higher OPBO. That can be achieved either by using lumped components or transmission lines. If the latter option is chosen, the compensation can be done by adding a certain electrical length to a branch and removing that same length from the other. The effects of this change are better demonstrated in a Smith Chart by varying the outphasing angle and the length difference between the branches of the combiner. This behavior is presented in Figure 3.20, where the results are obtained using ideal transmission lines. The represented impedances correspond to the top branch, in red, and the bottom branch, in blue. The referred Figure shows four different plots that represent the electrical length[3] added to the top branch and subtracted to the bottom one. Both lines, in this case, have a characteristic impedance of 50 Ω and the load presented to the combiner is 25 Ω.

By changing only these lengths and the characteristic impedance of the lines, different load modulation schemes will appear, but the interceptions will always occur on purely real impedances. If these are not desired, there is a simple way to obtain complex interception points: adding or subtracting a certain electrical length in both branches. Figure 3.21 shows a compensated Chireix combiner, with 145° and 65° of electrical length in the branches terminated with a 50 Ω load. The electrical length values were respectively obtained by the following equations: $90^o + 40^o + 15^o = 145^o$; and $90^o - 40^o + 15^o = 65^o$. Presenting 50 Ω to the combiner actually means that each branch is presented with two times that impedance, since two equal currents flow through the load.

The main goal of this combiner design is to achieve the pattern in Figure 3.22 for its load modulation. As can be easily seen, to get this, all three techniques described above need to be employed. This grants the designer a decent amount of variables and, since automatic optimization may be complicated to realize due to the difficulty in setting the necessary optimization goals, the best strategy may rely on the manual tuning of those variables. For-

[3] The electrical length of an ideal transmission line can be represented by an angle, where 360° corresponds to λ

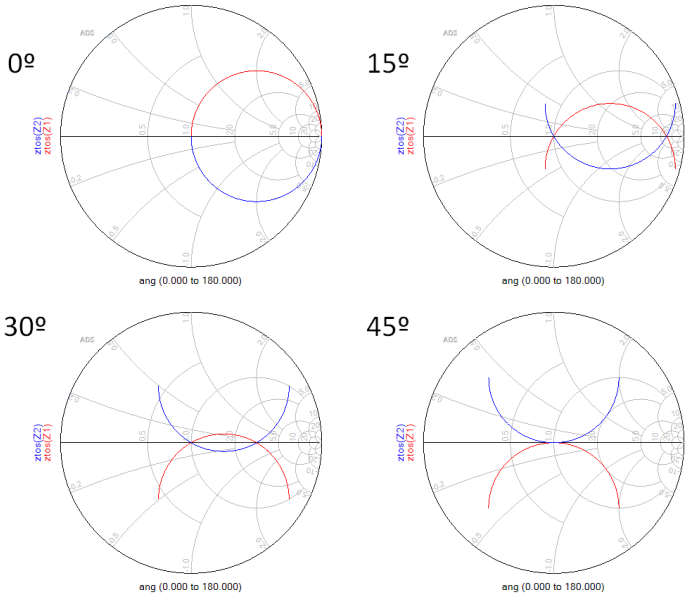

Figure 3.20: Examples of Chireix combiners with compensation based on ideal transmission lines.

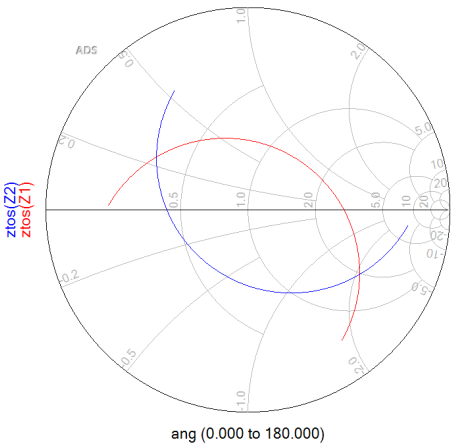

Figure 3.21: Example of a Chireix combiner with compensation with 145º and 65º of electrical length in the branches and a 50 Ω load.

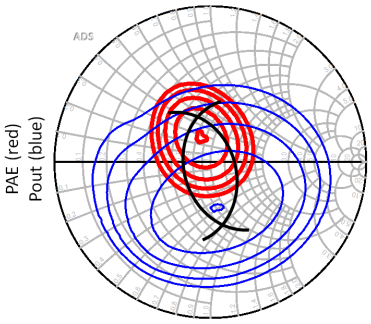

Figure 3.22: Desired Load Modulation pattern, in black, shown along with the PAE and P_{out} contours, in red and blue, respectively.

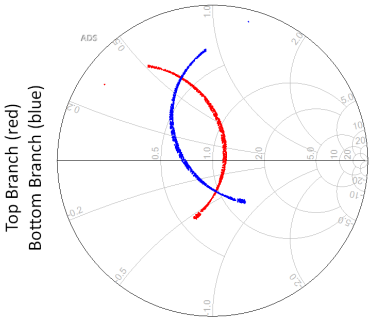

Figure 3.23: Load Modulation pattern of the designed Chireix combiner with the top and bottom branch impedances in red and blue, respectively.

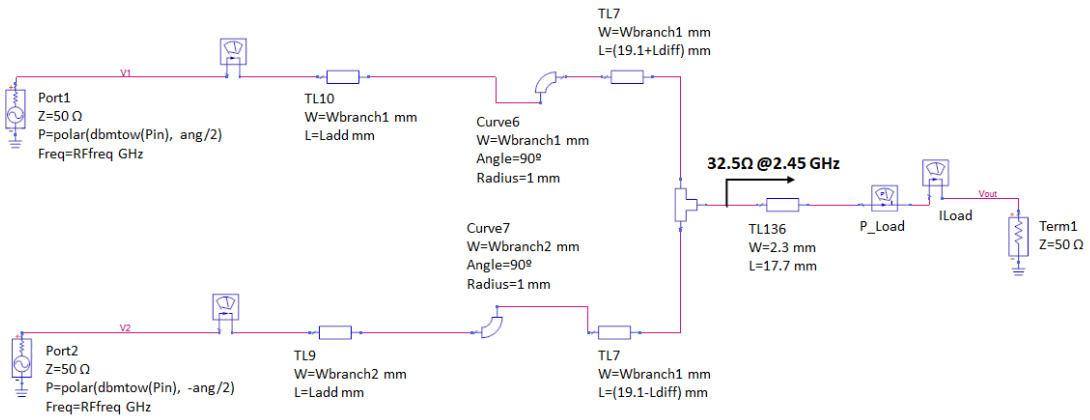

Figure 3.24: Final design of the Chireix power combiner.

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tunately, ADS also provides a tool that simplifies the task. The resulting combiner, shown in Figure 3.24 presents a load modulation pattern close to the desired one, as can be seen in Figure 3.23. The dimensions of the combiner are indicated in Table 3.7.

While designing the combiner, it was noticed that the evolution of the load modulation curves with the frequency could compromise the bandwidth of the overall amplifier. As the frequency increases, the load modulation rotates in the opposite direction of the maximum efficiency and output power loads. As moving from one to another is the goal, this fact will degrade the performance as the signal frequency moves away from 2.45 GHz and consequently diminish the bandwidth of the amplifier. The designed combiner aims to reduce the rotation of the load modulation with the frequency and this is the reason why there are differences between Figures 3.22 and 3.23.

Dimensions	mm
Wbranch1	1.85
Wbranch2	1.85
Ladd	4.00
Ldiff	11.40

Table 3.7: Final Chireix power combiner dimensions.

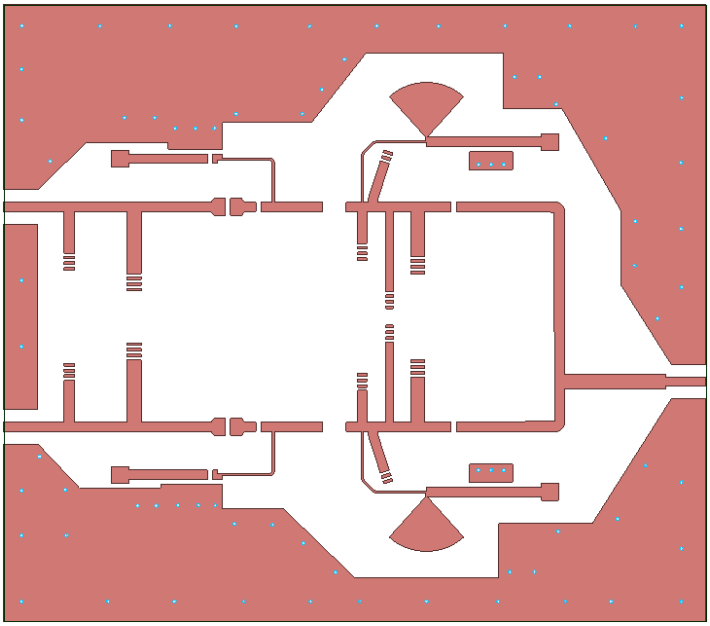

Figure 3.25: Layout of the implemented board for the Outphasing power amplifier.

3.3.3 Simulation Results

Up until now the process has been almost the same as it would have been if this was a typical Outphasing PA. The differences lie on the driving signals, as in this case the amplitude and phase are allowed to change freely. The best combination of driving signals needs to be determined and tested in the real transistor. The best possible combination of driving signals is recorded in a LUT, Look Up Table, that can be determined by varying the phase and amplitude of the driving signals. Since this is the last stage of the amplifier design, a complete electromagnetic model must be obtained and utilized in a circuit simulation in order to obtain reliable results. With this process completed and its results validated, the circuit may be implemented in practice.

The final board is presented in Figure 3.25. Its dimensions are 125x100 mm. This board was used to obtain the results presented throughout the following sections.

LUT Determination

The LUT for this amplifier needs to be determined. The best way to do it is to try the possible combinations of the input signals. In order to obtain it faster and without overloading

the simulator, the Monte Carlo algorithm was used. The range of values in which the variables should vary, as well as the number of different combinations, need to be set.

There are three variables to use: the top branch PA input power; the bottom branch PA input power; and the phase difference between the two input signals. However, this PA evolved to only have two control variables. Through several simulations, it was concluded that allowing the input powers to be different would not benefit the PA performance. The PAE curves are roughly the same if the PAs are driven by the same input power, so this solution was chosen. Having less variables may, actually, simplify the practical implementation of the amplifier. With the top and bottom branches being A and B, respectively, the phase difference, θ, is defined by $\theta = \theta_A - \theta_B$ and it may take any value within [0º; 180º].

Although circuit simulations were performed at this stage and they were useful to adjust the combiner, the results presented in this section are acquired through hybrid simulations since they make a better representation of the practical system. The results are, consequently, more reliable. Whenever a new electromagnetic model is calculated the hybrid simulation must be compared with the circuit one, and they should present similar results.

The proposed design, whose layout is presented in Figure 3.25, was tested in the previously described conditions. The maximum P_{out} is 43.8 dBm, obtained in the hybrid simulation. The circuit simulation is able to deliver 44.1 dBm, but the difference was considered reasonable. The hybrid simulation also shows that the drain efficiency reaches its maximum value of 72.7 % at a OPBO of -1.6 dB, as seen in Figure 3.26, and the PAE peaks at 65.2 % at -0.7 dB of OPBO, seen in Figure 3.27. As can be confirmed in Table 3.8, this is very similar to the results obtained from the circuit simulation. The PAs gain, presented in Figure 3.28, is calculated by adding both input powers and, just like the previous metrics, both simulations showed similar results.

	Hybrid	Circuit
Maximum η @ OPBO	72.71% @ -1.59dB	73.38% @ -1.22dB
Maximum PAE @ OPBO	65.16% @ -0.74dB	66.35% @ -0.67dB
Maximum P_{out}	43.75 dBm	44.10 dBm

Table 3.8: Comparison between the hybrid and circuit simulations.

The consistency in simulations is an encouraging indicator that the PA is well designed. It is, however, important to compare the maximum values of the Oph configuration to the ones obtained from the branch PA. Since in the latter case only circuit simulation was performed, it should be compared to the same kind of simulation of the Oph. The results of the efficiency metrics and gain versus OPBO for the branch PA are presented in Figure 3.29. With the input power of 30 dBm, the branch PA presents: η = 76.5% ; PAE = 69.1%; and P_{out} = 40.2 dBm. The maximum gain is 14.4 dB. It is possible to realize that the efficiency metrics decreased in the Oph, but this behavior was expected. The cost of getting higher efficiencies at lower powers, is the degradation of maximum values of these metrics. The output power increased[4] in the OphPA, but that can easily be explained by the load modulation. The branch PA gain seems to fit the results obtained for the Oph.

The tests performed up until now allowed to identify which input power/phase combination grants the best performance for the designed PA. Since the main goal of this architecture

[4] If an ideal sum was performed, two PAs would deliver 43.2 dBm; the OphPA delivers 44.1 dBm.

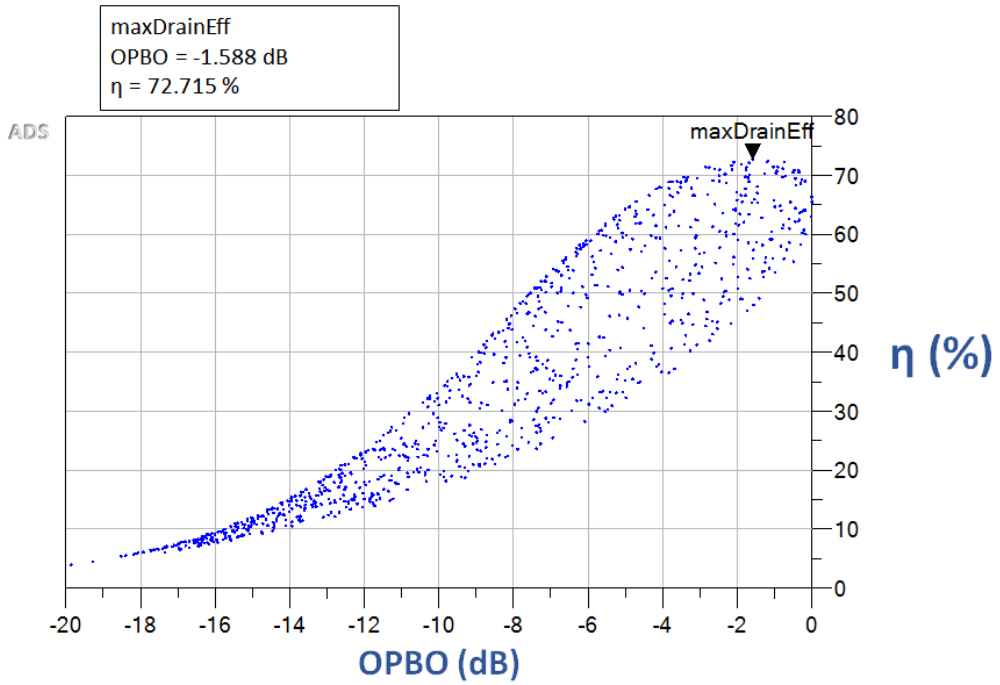

Figure 3.26: Drain Efficiency plot obtained from the hybrid simulation.

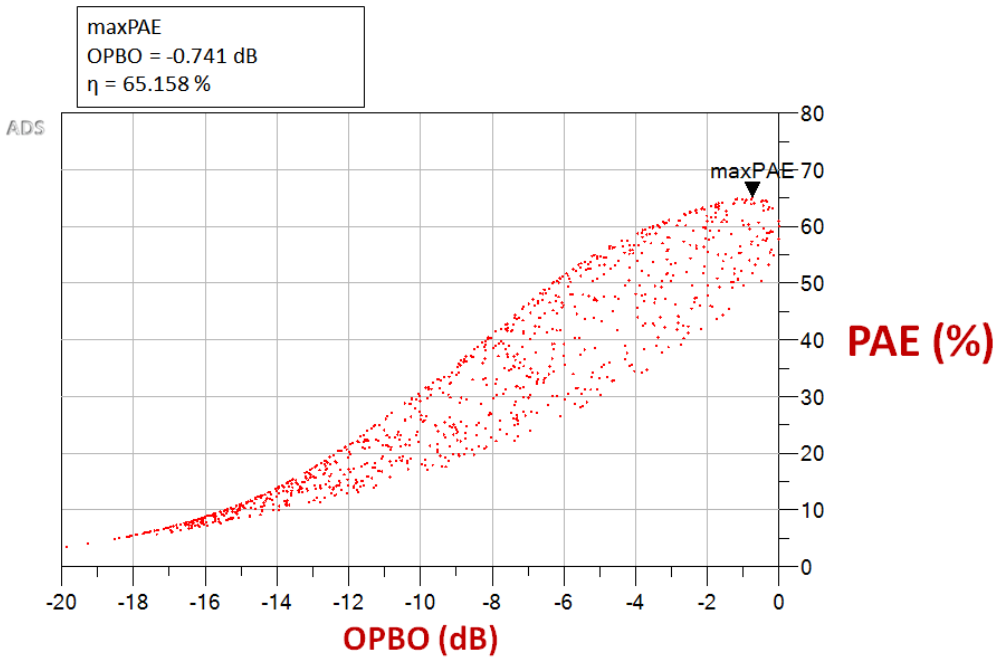

Figure 3.27: Power Added Efficiency plot obtained from the hybrid simulation.

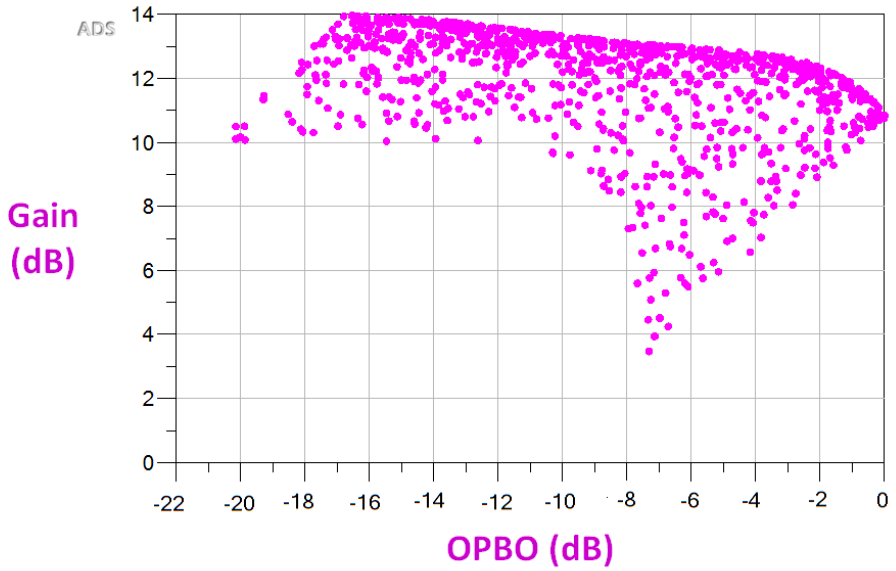

Figure 3.28: Transducer Power Gain plot obtained from the hybrid simulation.

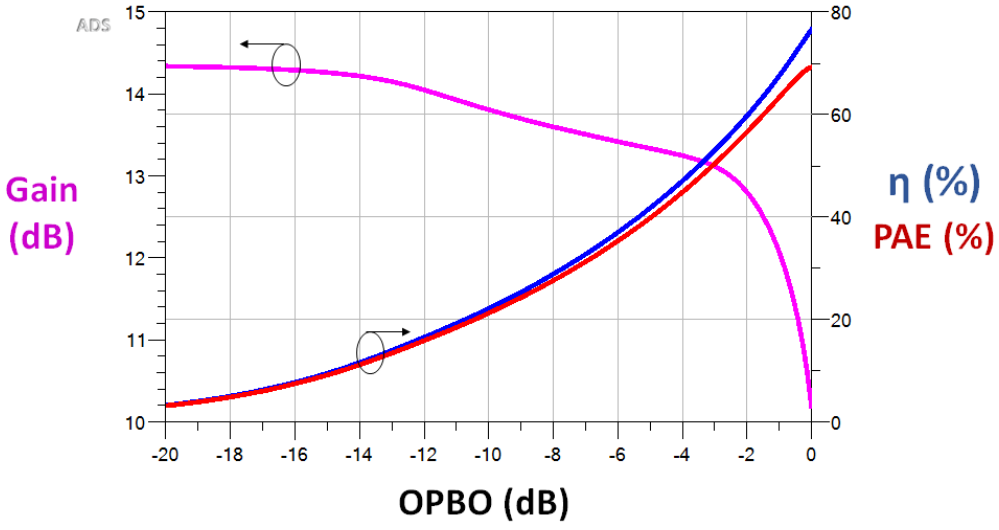

Figure 3.29: Branch amplifier performance in a circuit simulation.

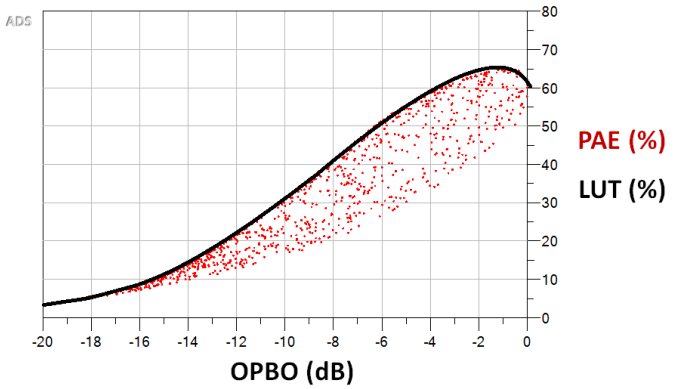

Figure 3.30: PAE curves generated by the LUT (black) compared to the PAE plot of the possible input combinations (red).

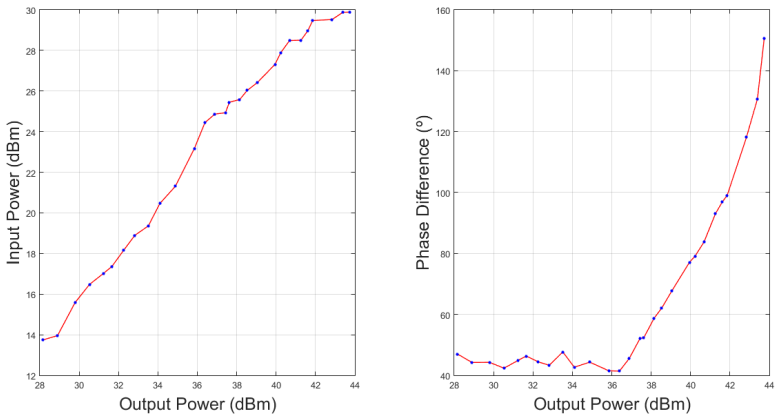

Figure 3.31: LUT signals extracted from the hybrid simulation and its linear interpolation.

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is to get high efficiency, it makes sense to prioritize this metric. The LUT will then represent the combinations that benefit PAE. The result should resemble the black curve in Figure 3.30.

LUT Representation

There are different combinations that produce similar results, specially in lower power regions. The LUT points were selected to avoid abrupt changes, as can be seen in Figure 3.31, but they form a scattered graph, limiting the possibilities for the driving signals. An easy solution when, as in this case, the selected points are not widely spaced is to do a simple linear interpolation using the acquired data. This is also shown in Figure 3.31. In CW measurements, is possible to use this LUT, but in a real scenario additional considerations must be taken.

In a real scenario, there is an input signal modulated in phase and amplitude. That will have to be converted into the driving signals. Since this architecture performance is influenced by the phase difference, not the absolute phase values, the phase information can

be kept by adding that same value to both driving signals. Then, it is the amplitude that must be converted. This can be achieved by a function that receives the input signal power and returns the driving signals. With that in mind, a problem arises: representing the LUT as an equation is not a simple task. So, the best approach is to approximate it by a polynomial equation. That polynomial should not have a very high order, otherwise it becomes too demanding for the processing unit, and it must not have even order terms, because they will generate out-of-band frequencies that cannot be produced.

To obtain such an equation, the coefficients of the polynomial must be determined using the LUT data. A polynomial function may be represented by (3.1), where P is the highest order, $y(k)$ is the driving signal and $x(k)$ is the input signal.

$$y(k) = \sum_{p=1,\, p\, odd}^{P} a_p x^p(k) \tag{3.1}$$

Using matrices, (3.1) takes the form of (3.2). So, the coefficients, represented by $\mathrm{A_p}$, may be obtained by (3.3).

$$Y = X * A_p \tag{3.2}$$

$$A_p = X \setminus Y \tag{3.3}$$

Using the determined coefficients, any input can be converted into the driving signals. This is the Least Squares Approximation. One may notice that this equation only returns a single output[5], but since both driving signals always have the same power, they can be easily obtained by the output of this function. This is the main reason why, in the design stage, the driving signals were set to have the same power. The results of this process are represented in Figures 3.32, 3.33 and 3.34 for 2.45 GHz. As expected, increasing the order of the polynomial, increases the approximation accuracy.

LUT Simulation

With the input signals determined, the Oph amplifier can be analyzed under more realistic conditions. It is also important to assess the validity of the polynomial approximations and the impact of its order on the amplifier performance.

Measuring and analyzing a configuration such as this implies that some traditional PA concepts may be challenged. An example of this is the definition of the PA gain and what information it can provide. Usually, a power amplifier is a device whose input and output are both RF signals. In this Oph that is not the case: the input is in the digital domain. The circuit does receive RF inputs, but they represent a conversion of the input signal, not the signal itself. With that in mind, two different concepts were defined: Gain; and AM-AM characteristic. Considering the following Figure[6]:

[5] The equation returns a complex number, whose magnitude represents the driving signals power and the phase represents their phase difference.

[6] The Signal Component Separator converts a digital signal into two RF signals; DUT, Device Under Test, represents the designed circuit.

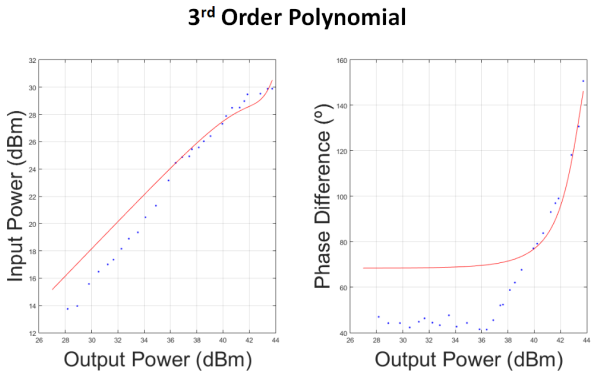


Figure 3.32: Third order approximation (red) and extracted LUT (blue) signals.

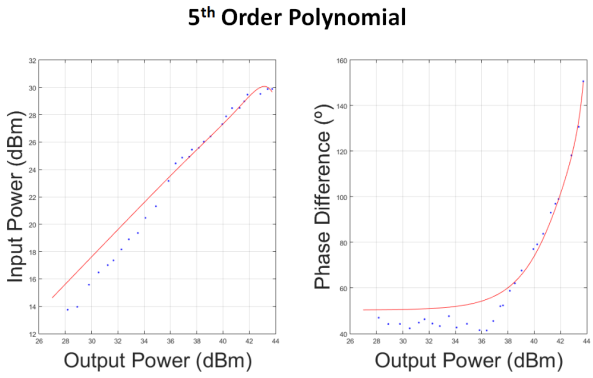


Figure 3.33: Fifth order approximation (red) and extracted LUT (blue) signals.

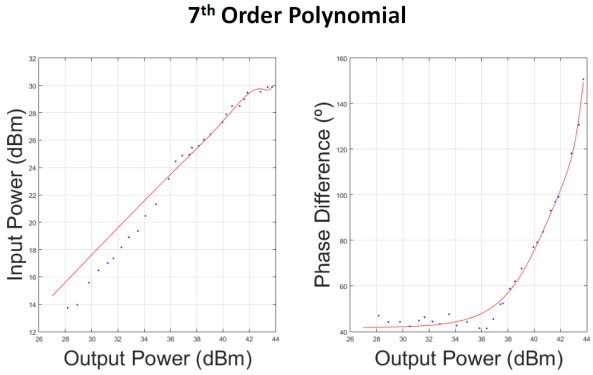


Figure 3.34: Seventh order approximation (red) and extracted LUT (blue) signals.

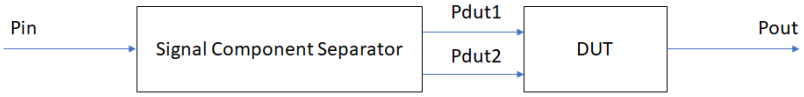


Figure 3.35: Block diagram of the OphPA.

The PA Gain is defined as (3.4) and the AM-AM characteristic as (3.5).

$$Gain = \frac{Pout}{Pdut1 + Pdut2} \tag{3.4}$$

$$AMAM = \frac{Pout}{Pin} \tag{3.5}$$

With this definition, the PA gain is no longer a strong indicator of the PA linearity. It serves as another metric to analyze the relation of the available power with the delivered power in the DUT. In Figure 3.28 the possibilities for the gain in this PA are presented. The AM-AM characteristic replaces gain as a linearity indicator, hence the given name. However, it compares an RF signal with a digital one, so it cannot be analyzed as if it was a traditional PA gain. Its absolute value does not hold any meaning, but its variation provides information about the distortion caused by the PA.

The first results that must be analyzed are the ones obtained from the interpolated LUT. The PAE curve is shown in Figure 3.36 and it demonstrates that the results of this method, in red, correspond to the highest PAE points acquired earlier, in black, with only slight deviations. Those are due to the interpolation process. Since the chosen LUT benefits PAE, the η curve may not reach the highest possible values, as can be seen in Figure 3.37. The PAE reaches the maximum of 65.2% and η goes up to 72.3%. The LUT was also able to drive the amplifier to a maximum of 43.7 dBm at the output. A comparison between the gains is shown in Figure 3.38. The maximum value is around 12.6 dB compressing up to 2.6 dB. The AM-AM characteristic forms the pattern presented in Figure 3.39, with a maximum variation of 0.9 dB.

The results demonstrate that the interpolation method does not significantly affect the PAE of the amplifier, but the signals necessary to drive it are highly irregular. Besides the previously discussed difficulty to mathematically describe those signals, their form affects the AM-AM characteristic. Although its variation is not too high, the pattern is far from smooth.

The polynomial approximation goal is to replicate these results, while simplifying the practical implementation of the OphPA. Comparing Figures 3.30, 3.32, 3.33 and 3.33 it is possible to verify that the driving signals describe smoother patterns in the polynomial approximations. This fact also affects the AM-AM characteristic and gain. The PAE results of these approximations are presented in Figure 3.40 for the 3^{rd} order and 7^{th} order polynomial approximations. The Drain Efficiency, Gain and AM-AM are, respectively, displayed in Figures 3.41, 3.42 and 3.43.

Table 3.9 shows the performance of simulated cases to allow a better interpretation of the data. The efficiency performance of the amplifier is better with the interpolated LUT, as it would be expected since it is the most faithful representation of the best scenario. Increasing

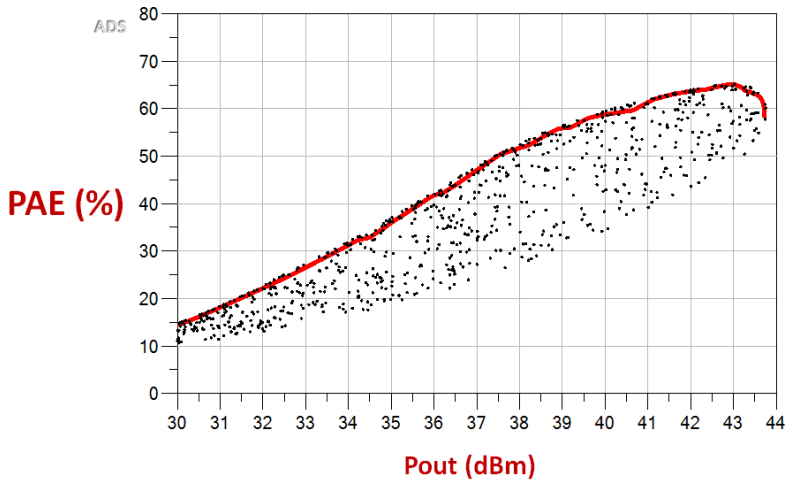


Figure 3.36: PAE curve obtained by the interpolated LUT, in red, compared with the results of the previously tested input combinations, in black.

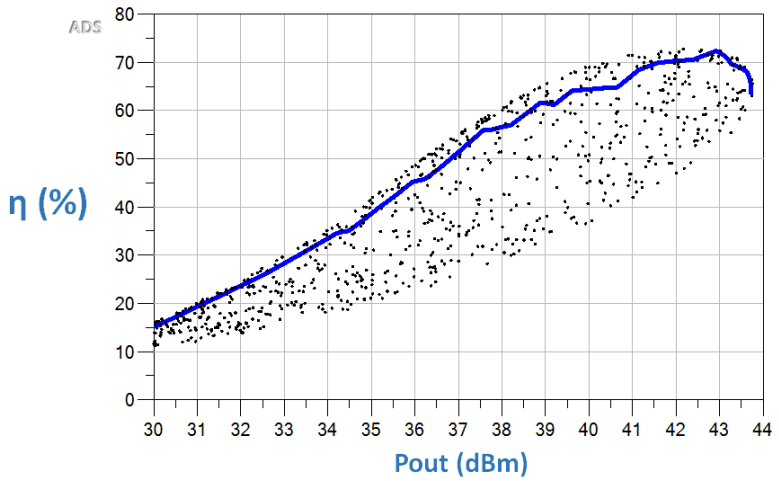


Figure 3.37: Drain Efficiency curve obtained by the interpolated LUT, in blue, compared with the results of the previously tested input combinations, in black.

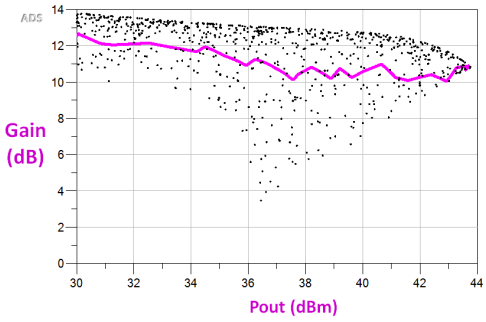


Figure 3.38: Oph Gain obtained by the interpolated LUT, in purple, compared with the results of the previously tested input combinations, in black.

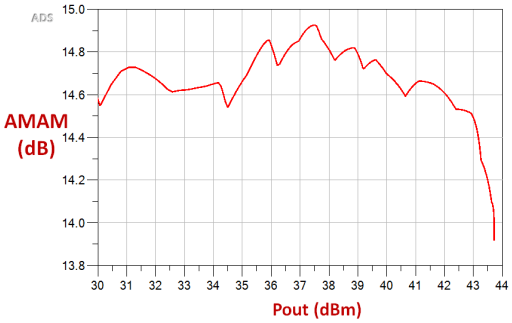


Figure 3.39: Oph AM-AM characteristic obtained by the interpolated LUT, in red, compared with the results of the previously tested input combinations, in black.

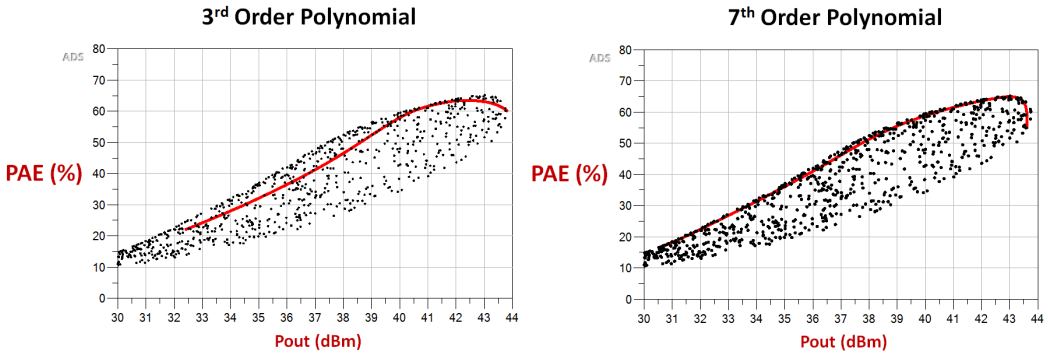


Figure 3.40: PAE comparison of the polynomial approximations, in red, with the results of the previously tested input combinations, in black.

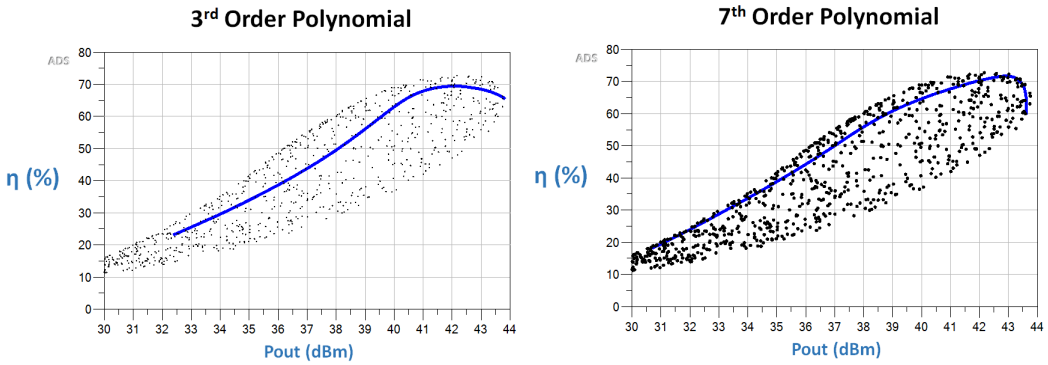


Figure 3.41: Drain Efficiency comparison of the polynomial approximations, in red, with the results of the previously tested input combinations, in black.

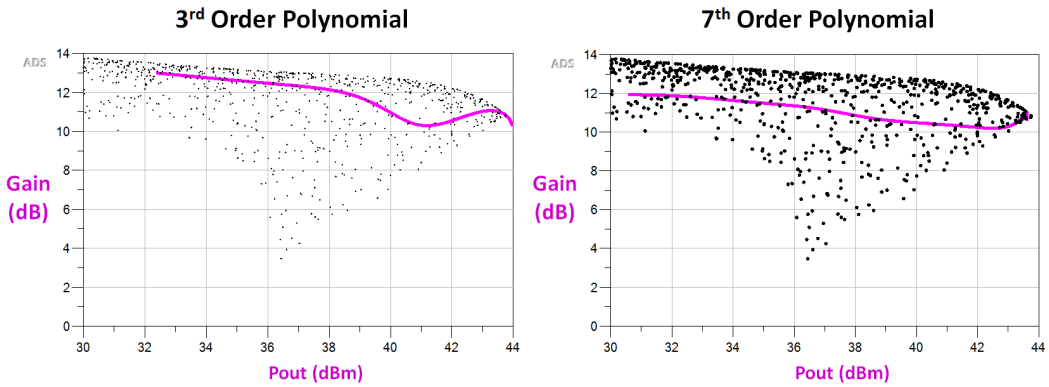


Figure 3.42: Gain comparison of the polynomial approximations, in red, with the results of the previously tested input combinations, in black.

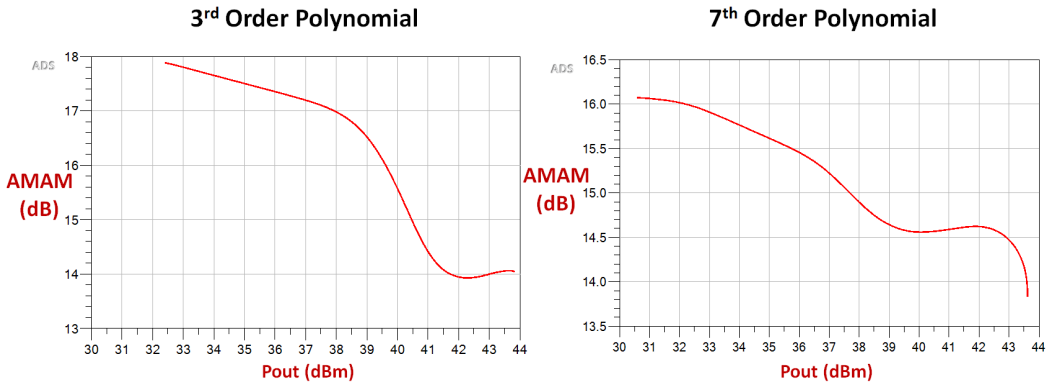


Figure 3.43: AM-AM characteristic comparison of the polynomial approximations, in red, with the results of the previously tested input combinations, in black.

the order of the polynomial improves the PAE and η curves. The AM-AM characteristic presents a 0.9 dB compression for the interpolation that worsens in the approximations. However, the latter cases present smoother patterns and higher order polynomials decrease the compression values, as seen in the 7^{th} order approximation. On the other hand, gain compression does not follow the same behavior: the interpolation results are actually worse that the ones from the 7^{th} order polynomial. This shows that, in fact, gain does not hold the same value as a distortion-evaluation metric as it does in traditional PAs. The maximum output power does not change significantly in these tests.

These results seem to indicate that polynomial approximations may not severely affect neither the efficiency performance nor the maximum output power of the amplifier. The most significant changes appear when analyzing the AM-AM characteristic, since a trade-off between simplicity and gain compression occurs. Lower order polynomials, although less demanding to process, generate higher compressions. These results now need to be verified in practice: that is the theme of the next chapter.

	Interpolation	Polynomial	
		3rd Order	7th Order
Maximum P_{out} (dBm)	43.7	43.8	43.6
Maximum PAE (%)	65.2	63.5	65.0
Maximum η (%)	72.3	69.4	71.4
Maximum Gain (dB)	12.6	13.0	11.9
Gain variation (dB)	2.6	2.7	1.7
AM-AM variation (dB)	0.9	3.9	2.4

Table 3.9: Comparison of the tested LUT representations

Chapter 4

The Outphasing Practical Implementation

4.1 Introduction

The simulations results not only showed the promising performance of the Oph configuration, but also demonstrated consistency. After this process, the practical circuit can be fabricated using the layout presented in Figure 3.25. It is well-known that, usually, practical circuits have some performance deviations from the simulations. The accuracy of the used models, especially of the transistor, imperfections in the substrate and the PCB, Printed Circuit Board, printer precision can all be the causes for such deviations. The main goal of this stage is to assess if the OphPA still operates within the expected parameters and if its results correlate with the simulated ones.

4.2 The Practical Circuit

The final circuit is shown in Figure 4.1. At first sight, one might notice that there are small pieces of conductor at the end of every stub. Knowing the probable behavioral deviation a practical circuit may have, it is important to allow the circuit to be tuned. These pieces allow the length of the stubs to be increased. In this case, there was no need to perform this tuning, so the lengths remained the same. Another detail that catches the eye is the boxes on top of the transistors. These are screwed to the metallic base and hold the transistor in place, making sure their terminals make contact with the PCB.

4.2.1 PCB S Parameters

To assess if the PCB did not have serious deviations, a S Parameter analysis may be performed. That can be done using a VNA, Vector Network Analyzer. The transistors were also removed in this measurements. The results may then be compared to the ones obtained from a simulation performed under the same conditions. Additional details on these measurements are presented in Appendix A.

As seen in Figure 4.2, the input matching network measurements turned out very close to the simulated values. They describe a similar behavior, but the practical is slightly more

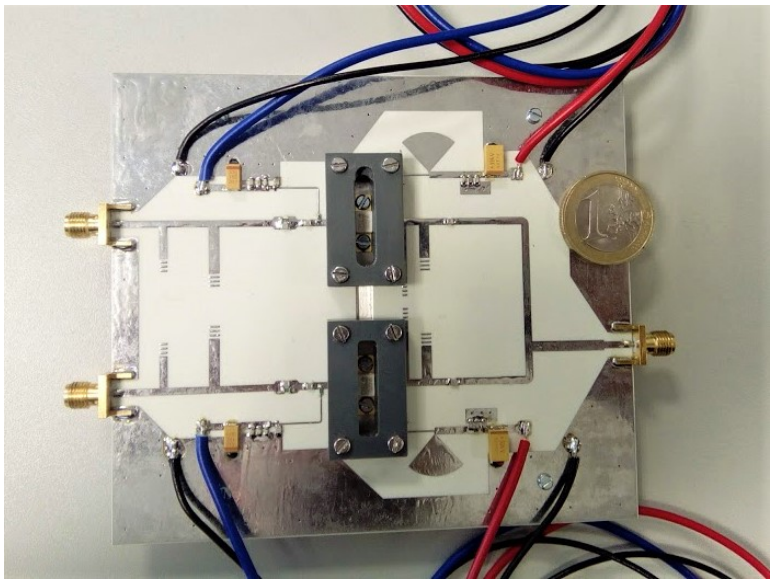


Figure 4.1: Final Outphasing Power Amplifier.

dissipative. That is, however, a reasonable occurrence. There is another important comparison that can be made: the similarity of both inputs. It has been established that these configurations require both branches to be as equal as possible and this should reflect on the S_{11} and S_{22} parameters. Figure 4.3 confirms that they are, in fact, very similar.

The output port also shows very similar results between practice and simulations, but it seems to have a phase shift. In Figure 4.4 these results are demonstrated. The overall results of these measurements are encouraging, since they show a very clear similarity between simulation and practice.

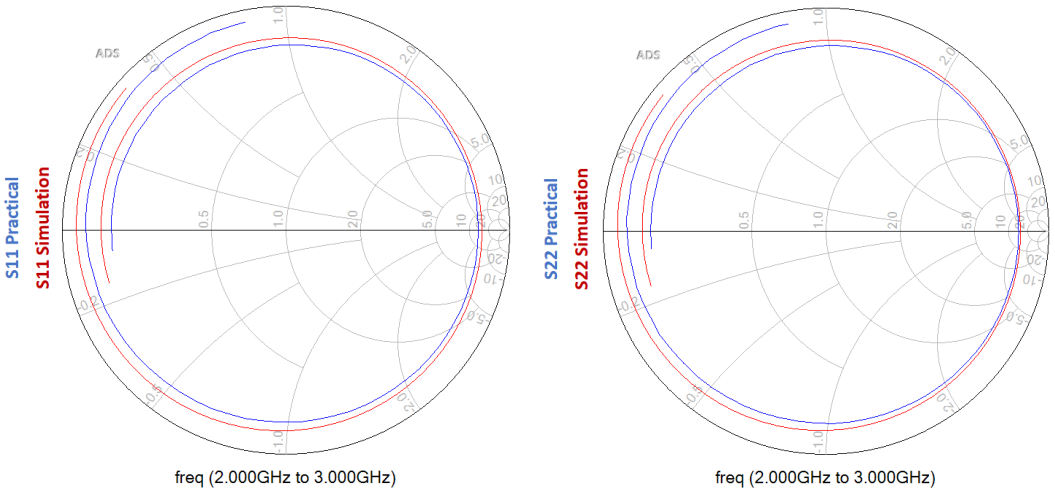
4.2.2 Stability tests

Anytime a power amplifier is implemented, the first test to perform is a small-signal stability test. This test was used as an early troubleshooting tool to guarantee that the transistors would not be damaged in the next tests. A Spectrum Analyzer showed that there was no stability problem in these conditions, as shown in Figure 4.5.

This first stability test, naturally, does not ensure that the amplifier is stable, so it needs to be tested under different conditions. It is important to analyze the device in large signal operation, so, a Vector Signal Generator is used to produce the input power, and the output, just like before, is connected to a Spectrum Analyzer.

These measurements demonstrated that there was a stability problem with the produced amplifier. When exited with either low or high power signals there was no oscillation, but whenever it transitioned from large to small-signal operation a frequency component of around 300MHz appeared in the Spectrum Analyzer. This problem was simply solved by the addition of a 21 Ω resistor to input bias networks, near the RF path[1]. After this change was tested in

[1] Note that, in the presented design, a 25 Ω resistor was placed close to the decoupling capacitors on each input bias network.



(a) S_{11} practical (blue) and simulation (red) results.

(b) S_{22} practical (blue) and simulation (red) results.

Figure 4.2: Input ports S Parameter comparison.

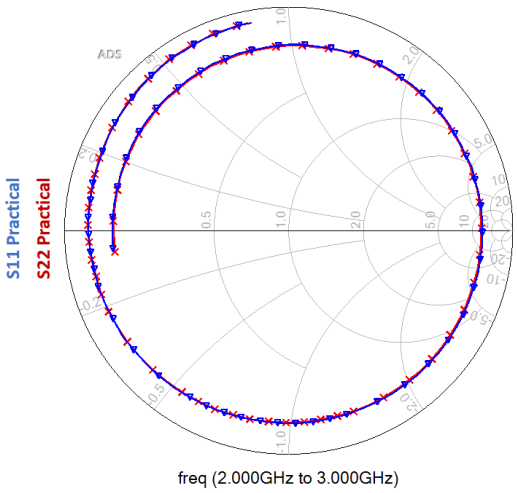
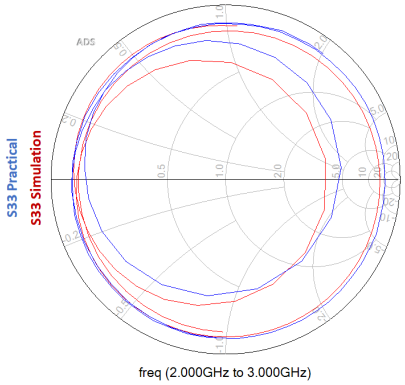
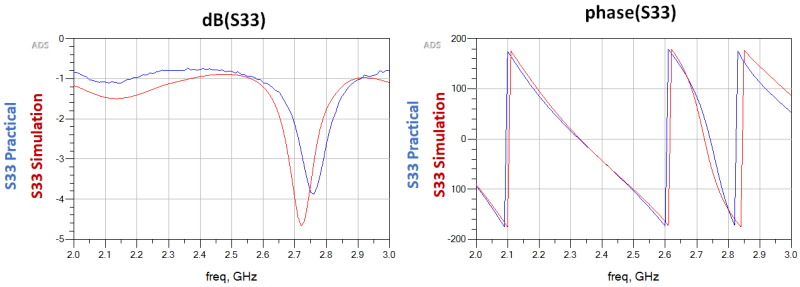


Figure 4.3: S_{11} and S_{22} comparison on the practical circuit.



(a) S_{33} practical (blue) and simulation (red) results in a Smith Chart.



(b) S_{33} practical (blue) and simulation (red) results in magnitude (dB) and phase (°).

Figure 4.4: Output port S Parameter comparison.

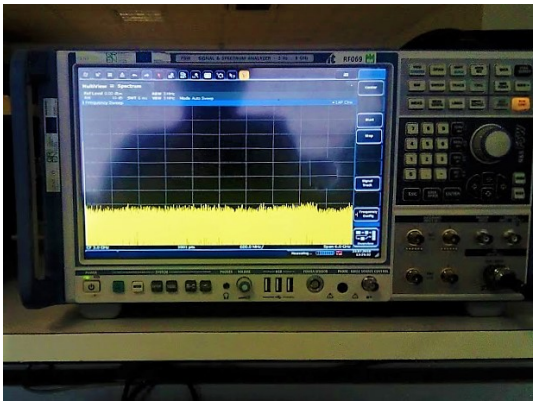


Figure 4.5: Small-signal stability test results from 0 to 6 GHz.

the simulator to confirm that it did not affect the performance of the amplifier, the stability problem was considered to be solved.

4.3 LUT Determination

The process of obtaining the practical LUT is the same as in the simulator: several input power/phase combinations need to be tested. The set-up used in these measurements is properly explained in Appendix B. The first tests performed to the PA, confirmed that there was, in fact, a frequency shift and the PA optimal operational bandwidth move to the frequency range between 2.25 GHz and 2.45 GHz. So, the LUT determination tests were performed at these frequencies. Through these tests, the actual operation bandwidth can be determined.

The efficiency results for the tested frequencies are presented in Figure 4.6. Table 4.1 displays some additional information.

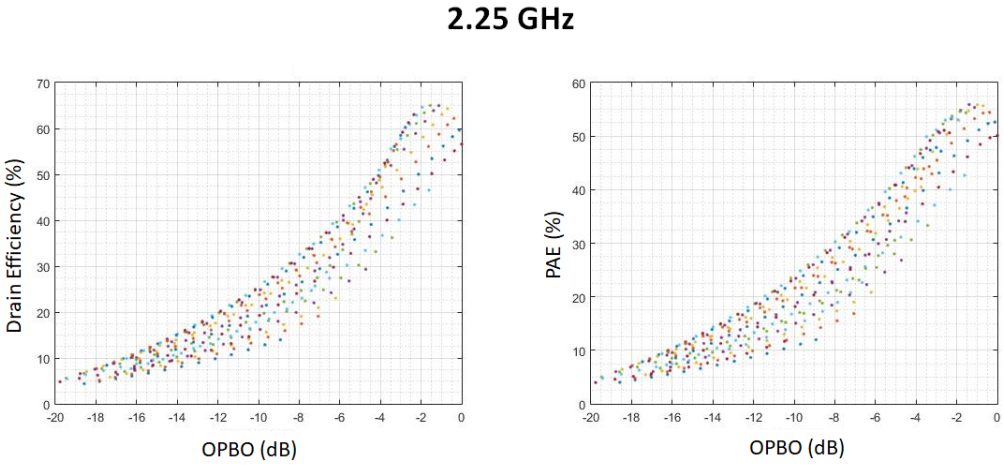
Frequency (GHz)	η_{max} (%)	PAE_{max} (%)	$Pout_{max}$ (dBm)	OPBO (dB) @ PAE=50%	OPBO (dB) @ η=50%
2.25	64.9	55.9	43.42	-3.4	-4.1
2.30	68.7	58.4	43.62	-6.0	-7.3
2.35	65.1	56.4	43.71	-4.9	-6.9
2.40	65.8	57.8	43.73	-4.1	-5.3
2.45	64.3	56.8	43.23	-2.8	-3.3

Table 4.1: Outphasing PA maximum values across the tested bandwidth.

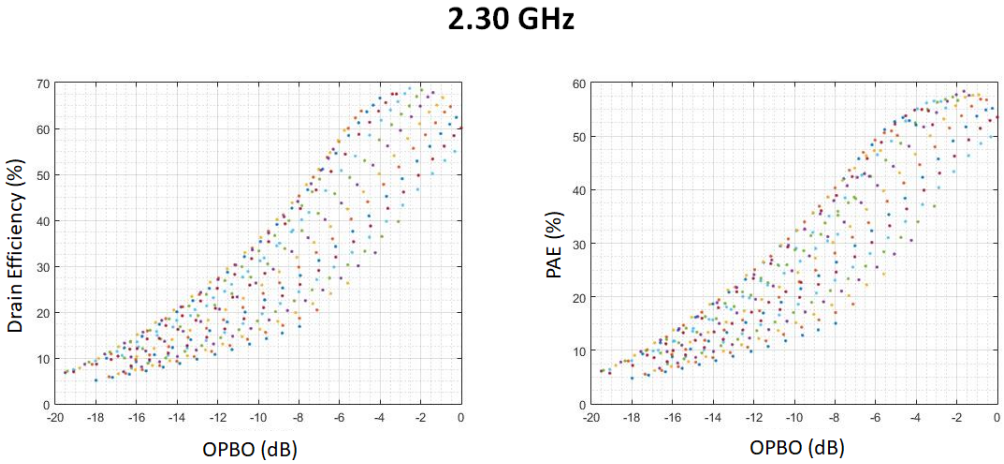
In traditional PA design, the operational bandwidth is typically defined by its small-signal gain. When the PA gain drops 3 dB bellow its value at the central frequency, the maximum and minimum operational frequencies are determined and, consequently its operational bandwidth. This definition cannot be applied to this architecture, so another one must be defined. Since the main goal of a OphPA is to have high efficiencies at high OPBO, its bandwidth definition should take this into consideration. So, in this work, a frequency is considered to be within the operational bandwidth if the PAE it at least 40% at 6 dB of OPBO. Following this definition, the designed amplifier operates between 2.25 and 2.40 GHz: a 150 MHz bandwidth. This represents 6.5% of its central frequency.

The maximum output power does not significantly change within these boundaries and peaks at 43.73 dBm at 2.40 GHz. The efficiency results are clearly better at 2.30 GHz, with $\eta = 68.7\%$ and $PAE = 58.4\%$ and $Pout_{max} = 43.62\ dBm$. This frequency also clearly has the best efficiency values at high OPBOs meaning that this is the best operational frequency for this OphPA. Since, in the simulation, the best results are at 2.45 GHz, the practical PA suffers from a 6% deviation.

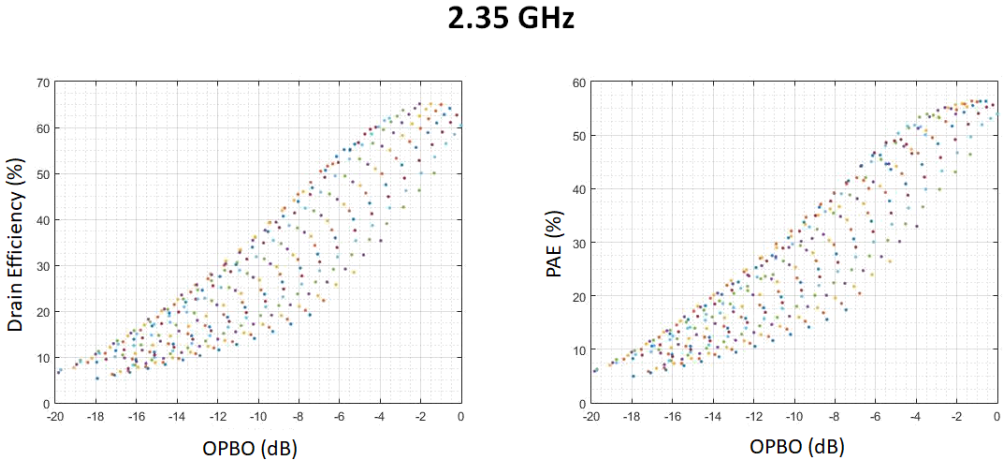
In the previous chapter, the PA was more thoroughly analyzed for 2.45 GHz, the frequency that provided the best performance, so it only makes sense to do the same with the practical implementation at the operational frequency of 2.30 GHz. Then, Figures 4.7, 4.8 and 4.9 can be directly compared to Figures 3.26, 3.27 and 3.28, respectively. Naturally, the maximum values for these metrics are lower than the ones from the simulator. In the efficiency metrics the maximum difference is 5.5% for η and 6.5% for PAE. The gain is remarkably similar in both scenarios, even with the change made to the practical circuit. In terms of output



(a) Efficiency results 2.25 GHz.

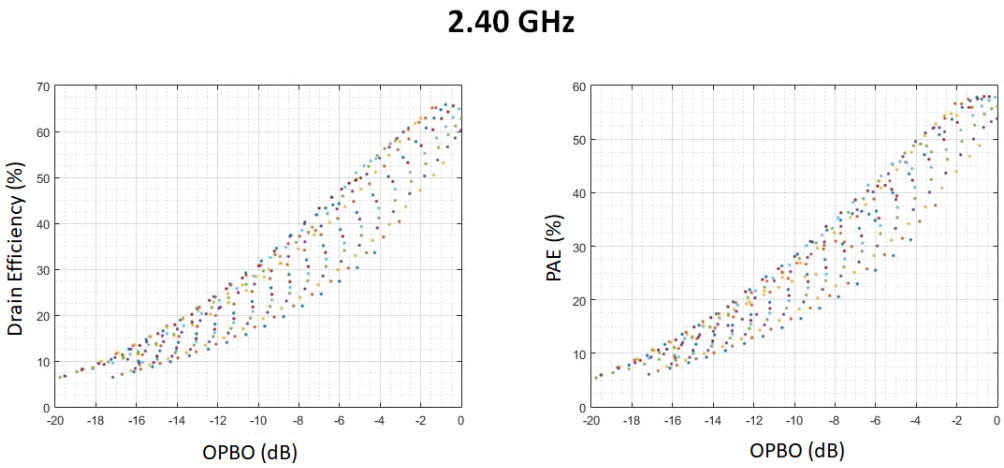


(b) Efficiency results 2.30 GHz.

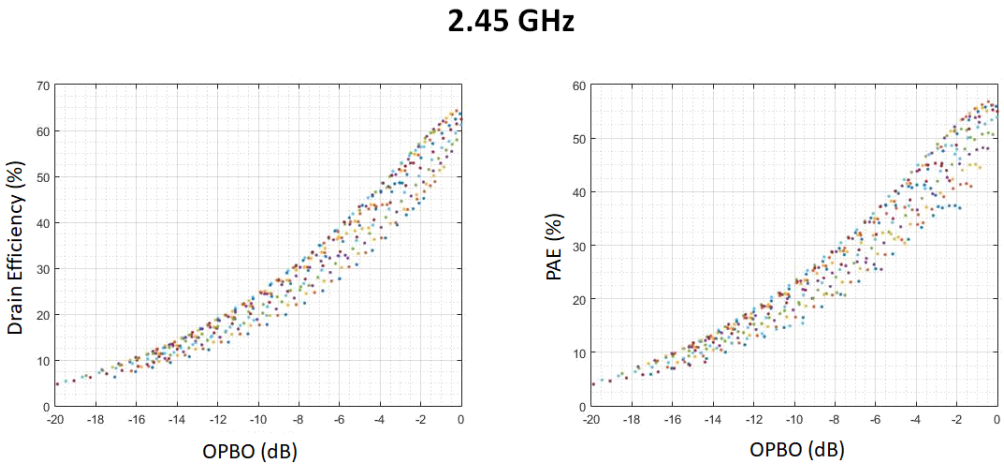


(c) Efficiency results 2.35 GHz.

Figure 4.6: Efficiency results of the practical OphPA in the tested bandwidth. (continues in the next page)



(d) Efficiency results 2.40 GHz.



(e) Efficiency results 2.45 GHz.

Figure 4.6: Efficiency results of the practical OphPA in the tested bandwidth.

	Simulation 2.45 GHz	Practice 2.30 GHz
OPBO (dB) @ η=50%	-7.6	-7.3
OPBO (dB) @ PAE=50%	-6.2	-6.0

Table 4.2: OPBO at 50% of the efficiency metrics comparison between simulation and practice.

OPBO (dB)	η(%)	
	Simulation	Practice
0	65.5	60.0
-2	72.2	68.4
-4	68.9	66.6
-6	58.9	57.2
-8	47.4	45.3
-10	32.9	36.2

Table 4.3: Drain Efficiency comparison between simulation and practice.

OPBO (dB)	PAE (%)	
	Simulation	Practice
0	60.0	53.5
-2	63.6	57.7
-4	58.7	55.1
-6	51.7	49.7
-8	41.6	40.3
-10	30.6	32.4

Table 4.4: PAE comparison between simulation and practice.

power, there was a decrease from 43.75 dBm, in the simulation, to 43.62 dBm, in practice. Table 4.2 shows that the OPBO @ 50% efficiency metrics are very similar in both cases, but, if the maximum values are taken into consideration, it can be verified that the practical implementation actually remains closer to its highest efficiency levels at higher OPBOs. In fact, the gap closes down when the power decreases and, at -10dB of OPBO, the practical PA presents better PAE and ηthan the simulation. This can be confirmed in Tables 4.4 and 4.3.

Overall, the designed PA performs as it was expected, being very consistent with the simulation results. The only major deviation is its operational frequency, that dropped from [2.40; 2.50] GHz to [2.25; 2.40] GHz. This could be corrected if the stub lengths were changed, but, since that would be a very time-consuming task that does not benefit the goals of this work, that will not be done.

4.4 LUT Representation

The problems of representing the optimal PAE LUT are already known: they were analyzed in the previous chapter. With that settled, this section can focus only on displaying the proposed solution in the practical scenario.

The interpolated LUT, represented in Figure 4.10, shows a very close resemblance with the one obtained from the simulation, seen in Figure 3.31. The major disparity lies on the absolute values of the phase difference, but that is mostly due to the drivers introduced in the practical set-up[2]. This similarity may indicate that the previous results may be confirmed in practice. Using the same Least Squares Approximation explained in the previous chapter, the signals presented in Figures 4.11 a) and b) are obtained. Comparing them with the simulated

[2] See Appendix B.

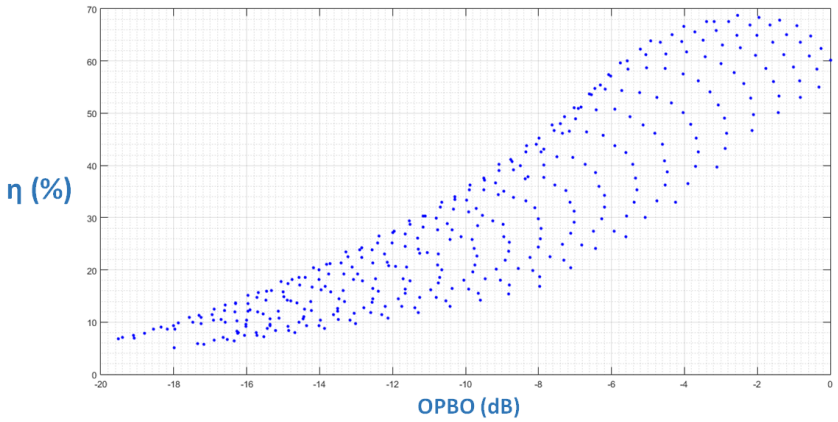


Figure 4.7: Practical Drain Efficiency plot for 2.30 GHz

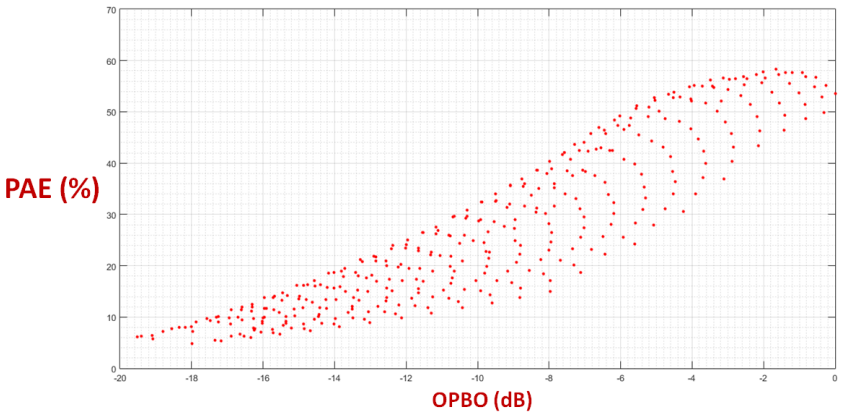


Figure 4.8: Practical PAE plot for 2.30 GHz

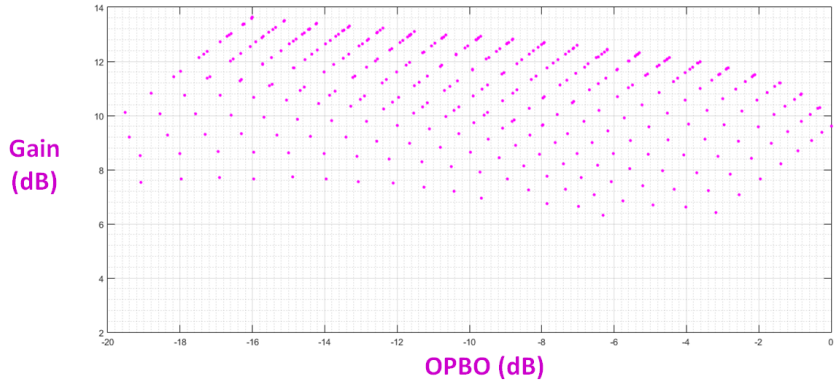


Figure 4.9: Practical Gain plot for 2.30 GHz

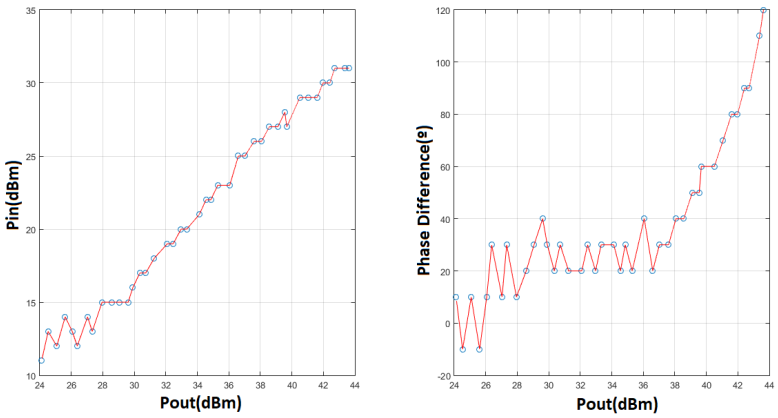


Figure 4.10: LUT signals extracted from the hybrid simulation and its linear interpolation.

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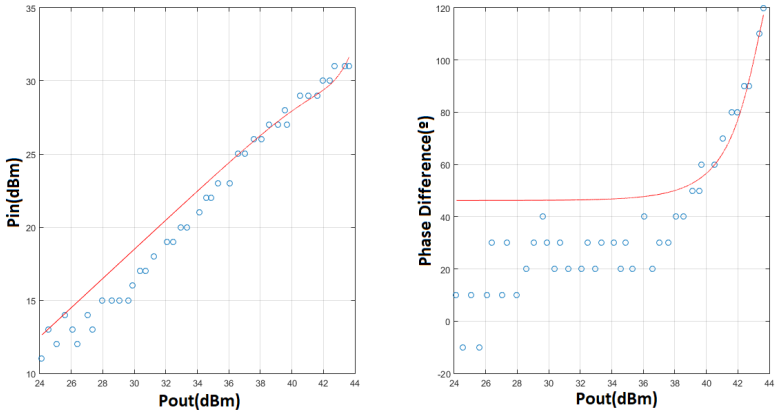
ones, presented in Figures 3.32 and 3.34, it can be observed that they also are very similar. As the polynomials order increases, the approximation accuracy also increases.

4.5 LUT Practical Tests

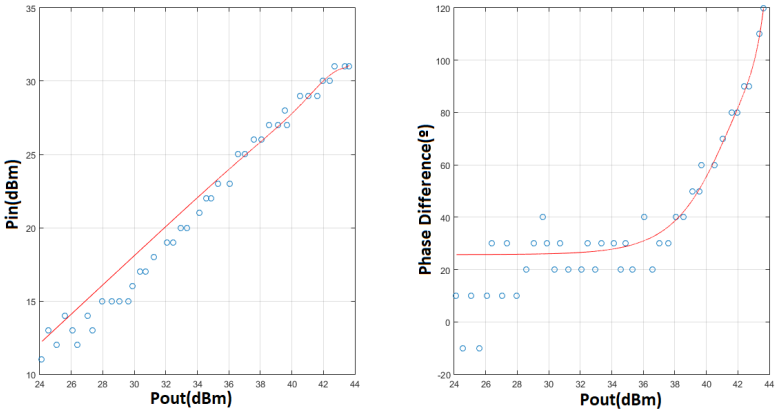
With the driving signals determined, the Oph can be truly measured. The practical set-up described in Appendix B was also used in these measurements. For better results the LUT Determination and its practical tests can be measured in the same conditions, i.e. same equipment and calibration set.

The first results that need to be analyzed are the ones from the interpolated LUT. The PAE results are displayed in Figure 4.12 and they clearly represent the best PAE results identified earlier. In fact, at some points they are slightly higher, because they correspond to combinations that had not been tested. As seen in simulation, the drain efficiency, presented in Figure 4.13, does not reach the maximum possible values. The maximum values are 59.9% for PAE and 67.8% for η. The output power reaches a maximum of 43.65 dBm. The PA gain peaks at 10.9 dB and has a variation of 2.0 dB, as shown in Figure 4.14. Finally the AM-AM characteristic, seen in Figure 4.15, has a maximum variation of 0.3 dB. Comparing this with Figure 3.39, one might notice that the absolute values do not correlate, but it must be kept in mind that these do not hold any meaning, only the variation matters. In the previous case, a normalized reference was used. It can be seen that, in the practical scenario, the AM-AM results are actually better, decreasing from 0.9 dB to 0.3 dB.

Practical results correlate with the ones observed in the simulator: the signals and AM-AM characteristic are highly irregular, although they present very good results. The PAE curves of the 3^{rd} and 7^{th} orders, displayed in Figure 4.16, show that the lower order polynomial gets worse approximations at higher OPBOs, but performs well in the high power regions. This was also seen in the simulator, but it is noticeable that in practice the PAE performance is less deteriorated by the 3^{rd} order polynomial approximation. The same can be said about the drain efficiency, seen in Figure 4.17. As expected, the gain and AM-AM characteristic, respectively shown in Figures 4.18 and 4.19, worsen with polynomial approximation, but higher order polynomials benefit these metrics. All these comparisons can be seen in Table 4.5. Overall,



(a) Third order approximation.



(b) Seventh order approximation.

Figure 4.11: Polynomial approximations (red) and extracted LUT (blue) signals from the practical PA.

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the simulated and practical results are very similar, with some of the metrics being actually higher in the latter case. The most noticeable cases are the AM-AM compression, which is consistently lower, and the performance with a low order polynomial approximation. It can be concluded that it is possible to design a OphPA with a Signal Component Separator implemented with a low order polynomial, and still achieve good performances in terms of efficiency. The linearity, though, is clearly compromised. However, increasing the order of the approximation will provide a better compromise between overall performance and needed processing resources. The outcome of this work is, certainly, a working power amplifier that fulfills the defined goals.

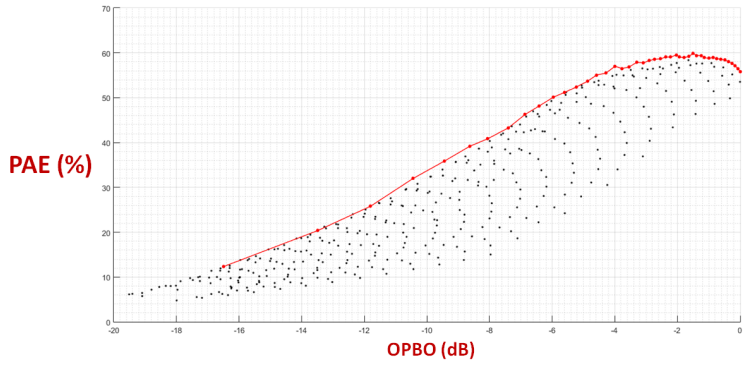

Figure 4.12: Practical PAE curve obtained by the interpolated LUT, in red, compared with the results of the previously tested input combinations, in black.

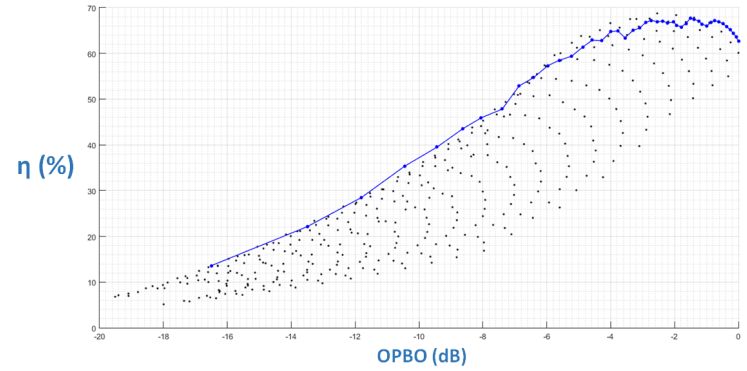

Figure 4.13: Practical Drain Efficiency curve obtained by the interpolated LUT, in blue, compared with the results of the previously tested input combinations, in black.

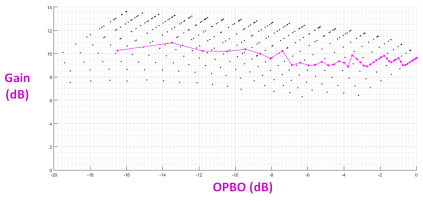

Figure 4.14: Practical Oph Gain by the interpolated LUT, in purple, compared with the results of the previously tested input combinations, in black.

Figure 4.15: Practical Oph AM-AM characteristic obtained by the interpolated LUT, in red, compared with the results of the previously tested input combinations, in black.

	Interpolation		Polynomial			
			3rd Order		7th Order	
	Simulation	Practice	Simulation	Practice	Simulation	Practice
$Pout_{max}$ (dBm)	43.7	43.7	43.8	43.9	43.6	43.8
PAE_{max} (%)	65.2	59.9	63.5	59.3	65.0	59.6
η_{max} (%)	72.3	67.8	69.4	67.1	71.4	67.6
$Gain_{max}$ (dB)	12.6	10.9	13.0	11.7	11.9	10.9
$Gain_{var}$ (dB)	2.6	2.0	2.7	2.6	1.7	1.7
AM-AM_{var} (dB)	0.9	0.3	3.9	3.4	2.4	2.0

Table 4.5: Comparison of the tested LUT representations in both practice and simulation

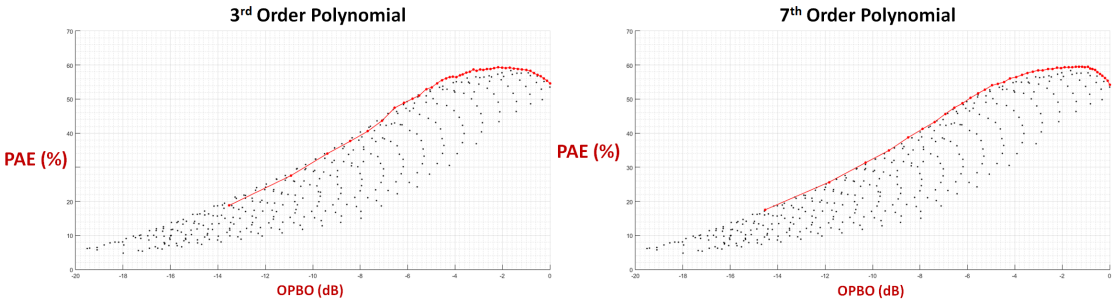

Figure 4.16: Practical PAE curves obtained by the polynomial approximations LUT, in blue, compared with the results of the previously tested input combinations, in black.

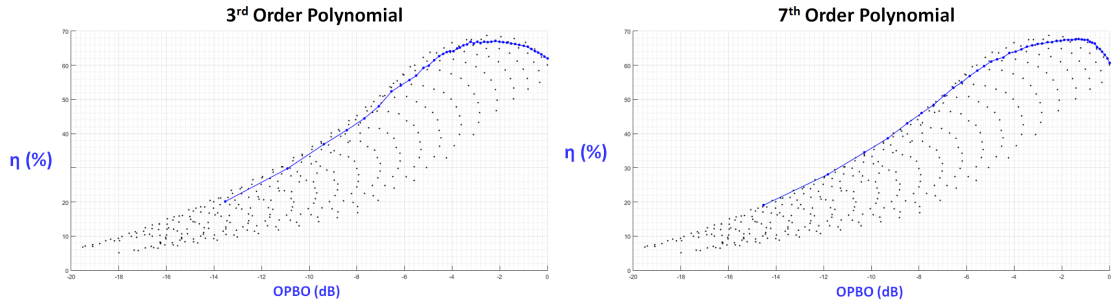

Figure 4.17: Practical Drain Efficiency curves obtained by the polynomial approximations LUT, in blue, compared with the results of the previously tested input combinations, in black.

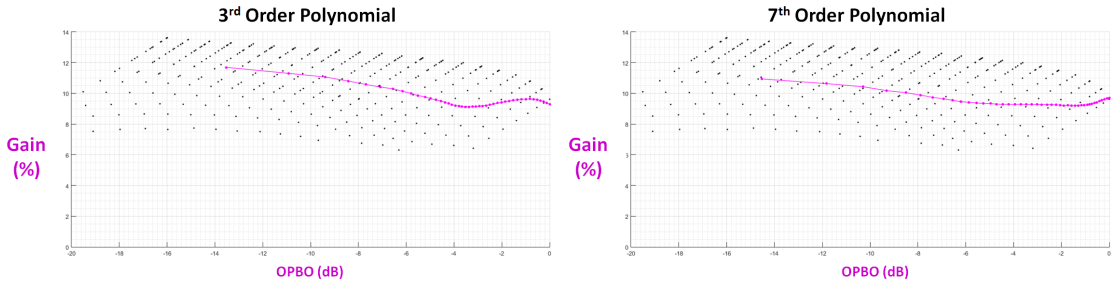

Figure 4.18: Practical Gain curves obtained by the polynomial approximations LUT, in blue, compared with the results of the previously tested input combinations, in black.

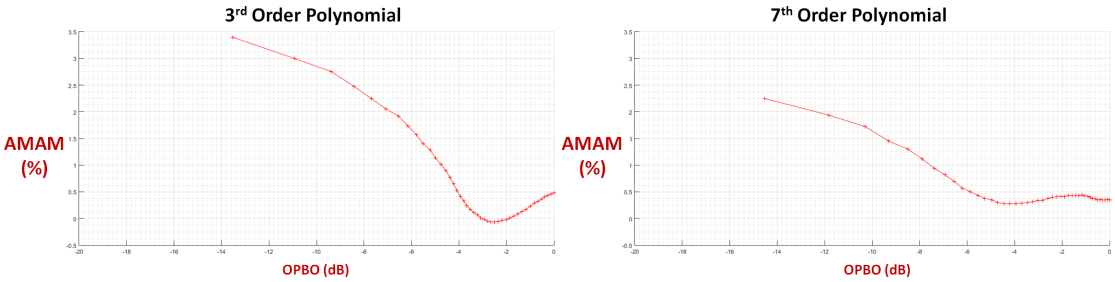

Figure 4.19: Practical AM-AM characteristic curves obtained by the polynomial approximations LUT, in blue, compared with the results of the previously tested input combinations, in black.

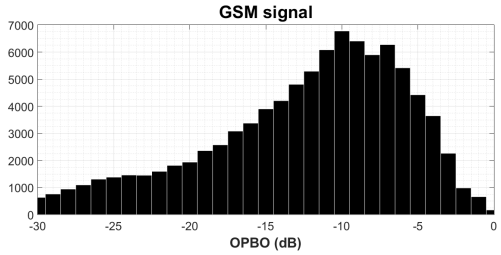

Figure 4.20: Input GSM signal histogram.

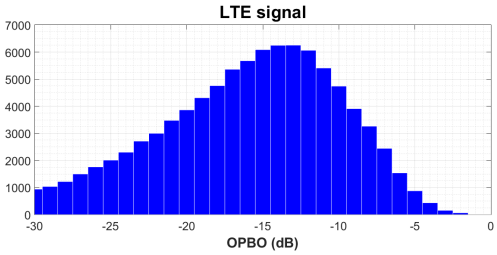

Figure 4.21: Input LTE signal histogram.

4.6 Modulated Signal Measurements

After the CW measurements are completed, in PA design it is important to test the power amplifier under more realistic and demanding conditions. The approach that better fulfills these goals is to use a modulated signal. It is also a good practice to use signals that represent the most commonly used signals in modern communication systems: phase and amplitude modulation; and high PAPR. To test this OphPA, two different signals were used: a LTE-like signal with PAPR of 10.33 dB; and a 4-carrier GSM signal with PAPR of 6.2 dB. Both signals have a bandwidth of 10 MHz. Three cases were tested: the interpolated LUT; the 3rd order polynomial approximation; and the 7th order polynomial approximation.

Using the previously determined LUTs, the input signal power can be converted into the driving signals. So, it is only necessary to add the input phase. As explained earlier in this document, that can be done by adding that same phase value to both branches. Naturally, modulation signal measurements do not provide the same metrics as the previous CW ones. So, those need to be defined.

To measure efficiency, a slightly different concept can be formulated: the Average Efficiency, η_{avg}. This metric provides information on what will be the average drain efficiency of a certain power amplifier when driven by a certain input signal. That can be measured by using the average output power and the average dissipated DC power during the time-span of those tests.

These measurements also allow some linearity metrics to be evaluated. The AM-AM and AM-PM conversions may be calculated by measuring the output signal power and phase, and then comparing them to the input signal. Another possible metric is the adjacent channel leakage ratio, ACLR. That is obtained using the spectrum at the output and measuring the power difference between the used communication channel and the ones next to it.

To measure all these metrics, a minor modification had to be done to the measurement set-up described in Appendix B: in the output, right before the attenuators, a Signal Analyzer was introduced using a coupler. The signal directed to the Signal Analyzer is attenuated by 20 dB. The rest of the system remains the same, but the losses in the Power Meter path are increased by 0.2 dB.

Figures 4.20 and 4.21 show the histogram of the GSM and LTE signals, respectively, used throughout these measurements. Their normalized baseband Power Spectral Density, PSD, is shown in Figures 4.22 and 4.23. These PSDs can be used as a comparison to the output ones, since, ideally, they would be the same as in the input. Both lower and upper ACLR are around -75 dBc for the GSM signal. The LTE signal value of this metric is around -66 dBc.

To facilitate the identification of each input signal tests, the GSM results are always

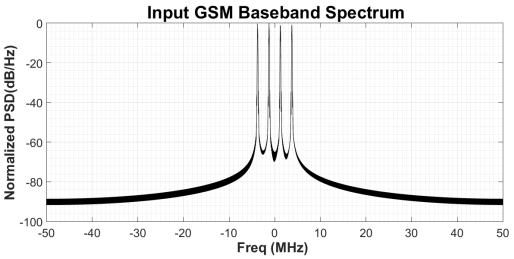

Figure 4.22: Input GSM signal PSD.

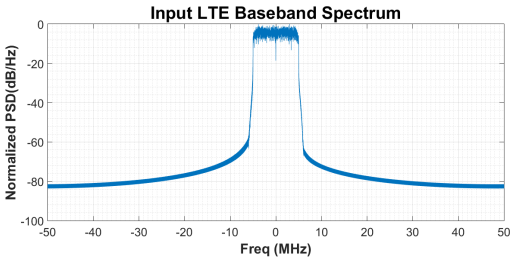

Figure 4.23: Input LTE signal PSD.

presented in black and the LTE ones in blue. With that settled, Figures 4.24, 4.26 and 4.28 represent the measured results of the produced Oph amplifier using the interpolated LUT when driven by the GSM signal. The same measurements for the 3rd order approximation can be seen in Figures 4.30, 4.32 and 4.34 and the ones for the 7th order approximation in Figures 4.36, 4.38 and 4.40. The measured metrics are presented in Table 4.6 and, from those and the overall aspect of the results, it is possible to verify that a considerable amount of distortion is produced. The ACLR seems to show that the three cases do not significantly vary. That statement is also confirmed by the AM-AM and AM-PM plots; when the variation in one of them decreases, the variation of the other seems to increase. The AM-AM and AM-PM variations seem to indicate that the interpolated LUT presents a slightly worse linear performance. In terms of efficiency, the approximations seem to present better results, with the 3rd order approximation reaching η_{avg}= 50%.

The LTE results are presented in Figures 4.25, 4.27 and 4.29 for the interpolated LUT; Figures 4.31, 4.33 and 4.35 for the 3rd harmonic approximation; and Figures 4.37, 4.39 and 4.41 for the 7th order approximation. In Table 4.7 the linearity and efficiency metrics are presented for the LTE-driven amplifier. The same statements made in the GSM case can be replicated in this one. This time, the highest η_{avg} was achieved also by the 3rd order approximation, but it only reached 36%. The decrease is expected since the PA is more often operated in higher back-off levels.

Overall, the results show that the amplifier produces a considerable amount of nonlinearities. This is a common occurrence in PAs of this kind when driven by multi-tone signals, as can be observed in [10,25,39]. The most problematic metric is the ACLR, since it determines how much the PA pollutes the closest communication channels. The power leakage to the adjacent channels must be low[3]; if it is not, the device cannot be used.

[3] The exact value depends on the legislation for each communications standard.

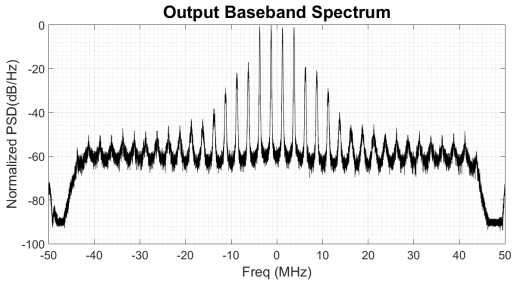

Figure 4.24: Output PSD with a GSM signal and using the interpolated LUT.

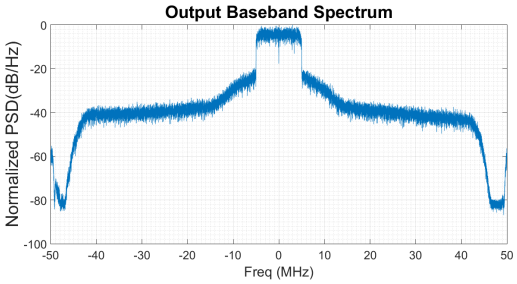

Figure 4.25: Output PSD with a LTE signal and using the interpolated LUT.

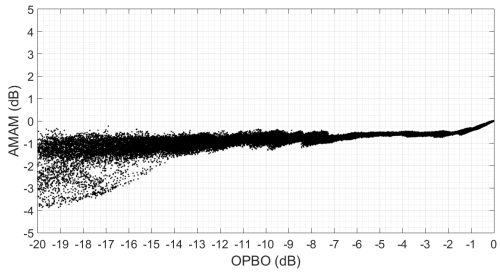

Figure 4.26: Output AM-AM conversion with a GSM signal and using the interpolated LUT.

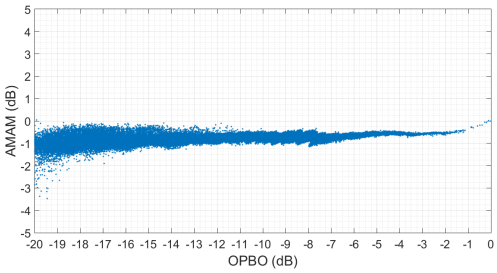

Figure 4.27: Output AM-AM conversion with a LTE signal and using the interpolated LUT.

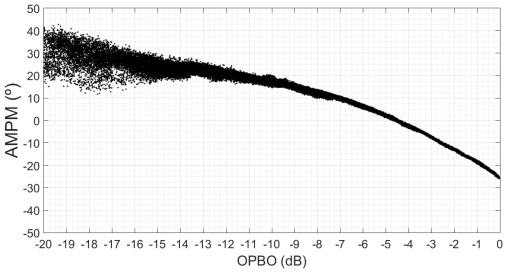

Figure 4.28: Output AM-PM conversion with a GSM signal and using the interpolated LUT.

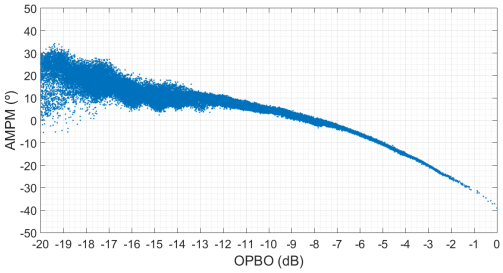

Figure 4.29: Output AM-PM conversion with a LTE signal and using the interpolated LUT.

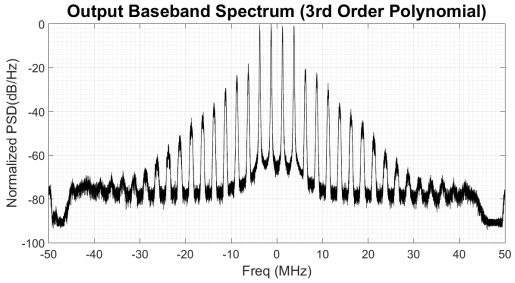

Figure 4.30: Output PSD with a GSM signal and using the 3rd order approximation.

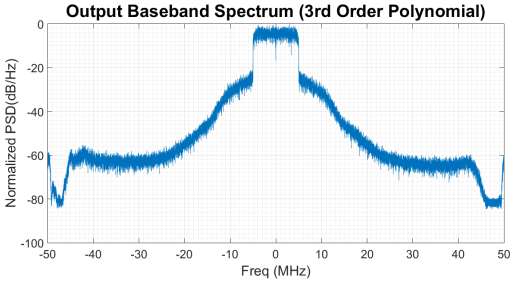

Figure 4.31: Output PSD with a LTE signal and using the 3rd order approximation.

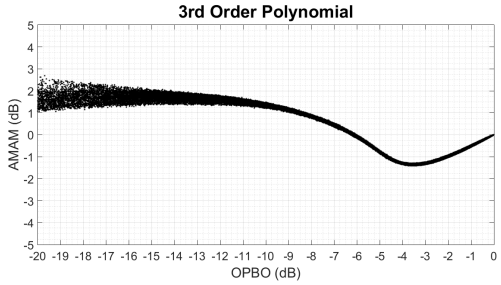

Figure 4.32: Output AM-AM conversion with a GSM signal and using the 3rd order approximation.

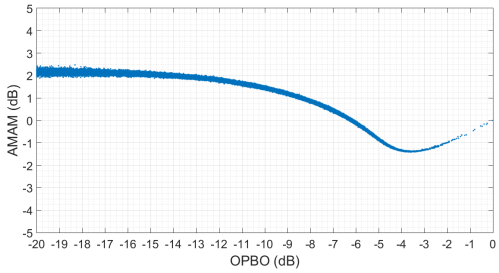

Figure 4.33: Output AM-AM conversion with a LTE signal and using the 3rd order approximation.

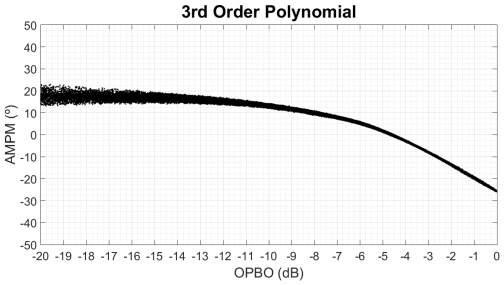

Figure 4.34: Output AM-PM conversion with a GSM signal and using the 3rd order approximation.

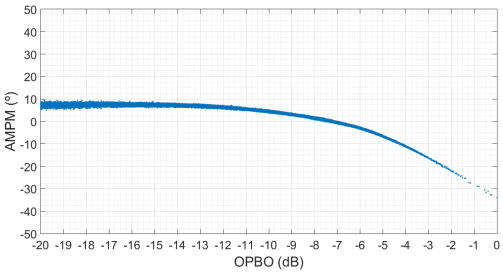

Figure 4.35: Output AM-PM conversion with a LTE signal and using the 3rd order approximation.

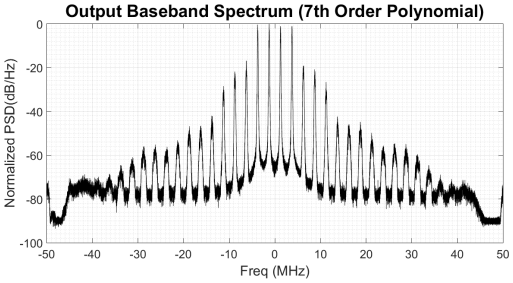

Figure 4.36: Output PSD with a GSM signal and using the 7th order approximation.

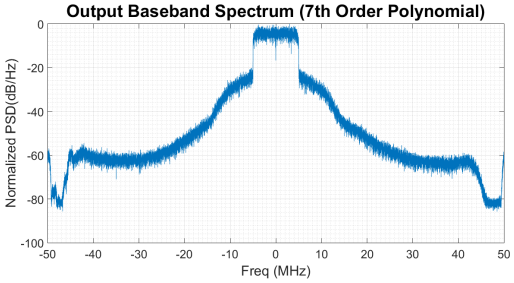

Figure 4.37: Output PSD with a LTE signal and using the 7th order approximation.

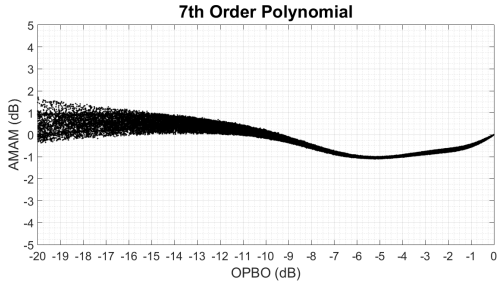

Figure 4.38: Output AM-AM conversion with a GSM signal and using the 7th order approximation.

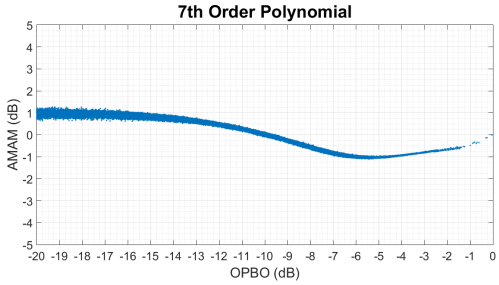

Figure 4.39: Output AM-AM conversion with a LTE signal and using the 7th order approximation.

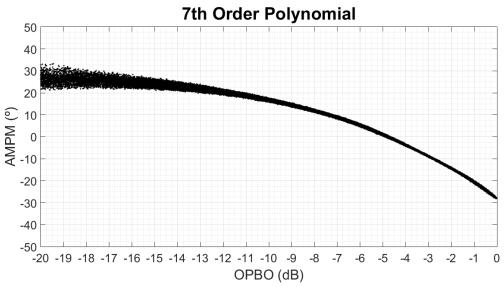

Figure 4.40: Output AM-PM conversion with a GSM signal and using the 7th order approximation.

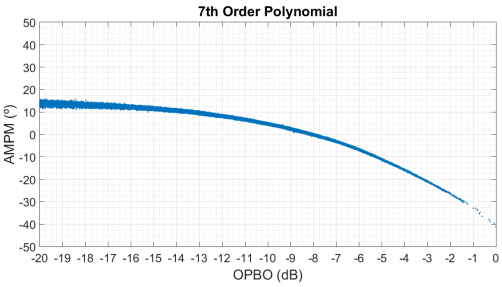

Figure 4.41: Output AM-PM conversion with a LTE signal and using the 7th order approximation.

GSM

LUT	η_{avg}	$ACLR_{upper}$	$ACLR_{lower}$	AM-AM_{var}	AM-PM_{var}
Interp	45 %	-19 dBc	-17 dBc	4.0 dB	68.6º
3rd Order	50 %	-21 dBc	-18 dBc	4.1 dB	48.7º
7th Order	47%	-19 dBc	-17 dBc	2.8 dB	61.1º

Table 4.6: Comparison of the measured metrics with the GSM signal for the several LUT representations.

LTE

LUT	η_{avg}	$ACLR_{upper}$	$ACLR_{lower}$	AM-AM_{var}	AM-PM_{var}
Interp	28 %	-21 dBc	-20 dBc	3.5 dB	73.3º
3rd Order	36 %	-22 dBc	-21 dBc	3.8 dB	43.1º
7th Order	30 %	-21 dBc	-21 dBc	2.3 dB	61.0º

Table 4.7: Comparison of the measured metrics with the LTE signal for the several LUT representations.

4.7 Linearization

When a PA does not comply with the necessary requirements in terms of ACLR, it needs to be linearized. To do this is to compensate the nonlinear behavior of the amplifier, and that is achieved using predistortion techniques. This architecture already utilizes a digital processing unit. So, the requirements needed to use Digital PreDistortion, DPD, are already employed. Since DPDs are a complex topic that exceeds the goals of this work, the actual implementation will not be addressed in this document. It can only be stated that the used DPD format was a Generalized Memory Polynomial [40] whose polynomial order was 9 and memory-depth was 3 for the Memory Polynomial terms; and the polynomial order was 3 and memory-depth 1 for the cross-terms. Further information on their details can be found on literature, and the methodology used in this application follows these publications [41, 42].

With that settled, the focus can move to the results of the linearization using DPD. The objective is to improve the linearity measurements. The variation of the AM-AM and AM-PM conversions must be very low, and their plot should resemble a straight line parallel to the xx-axis. The PSD should demonstrate lower power levels on the adjacent channels.

The linearization was performed using the LTE signal and the 7th order approximation, so its results can be directly compared to the previous ones in those conditions. Starting the comparison by the PSD: analyzing Figures 4.37 and 4.42 it is possible to verify that the latter one shows clear improvements as both ACLR values decrease by around 30 dB. In terms of AM-AM and AM-PM conversions: Figure 4.43 presents an almost linear response as the AM variation decreases 1.7 dB, when compared to Figure 4.39; and Figure 4.44 also shows the improvement in terms of linearity as the PM variation decreases by 57.9º, comparing to Figure 4.41. The average efficiency increases by 3 % when the DPD is employed. That is an interesting occurrence that was not expected, but it happened because the modifications in the driving signals cause the efficiency performance to increase in the most common power levels of the input signal. All the mentioned metric values can be confirmed in Table 4.8.

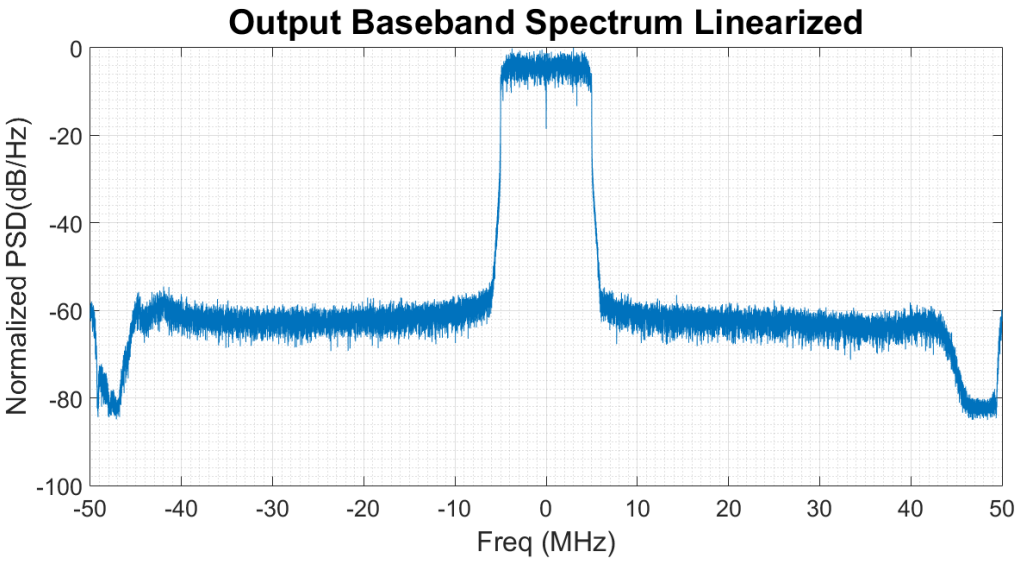

Figure 4.42: Linearized output PSD with a LTE signal and using the 7th order approximation.

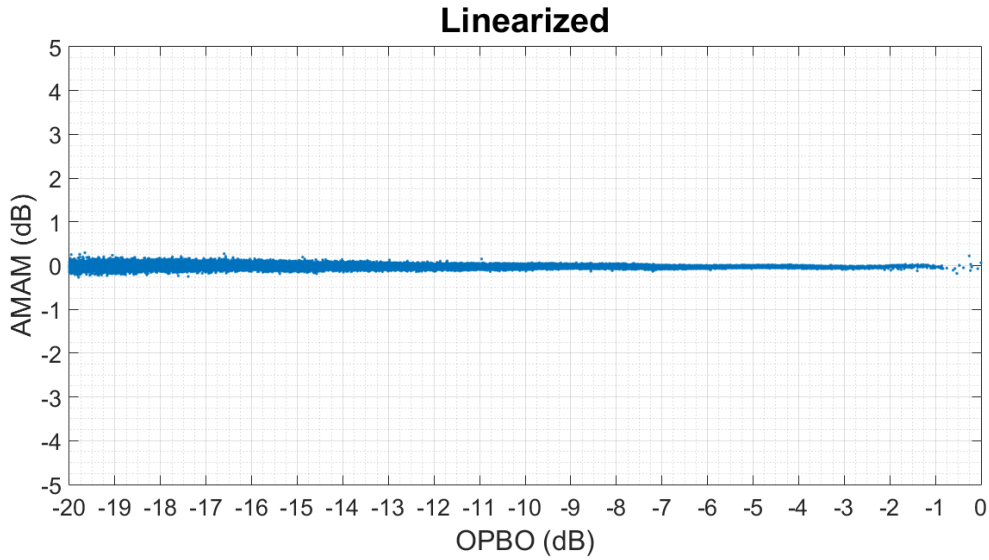

Figure 4.43: Linearized AM-AM conversion with a LTE signal and using the 7th order approximation.

Linearization Comparison

DPD	η_{avg}	$ACLR_{upper}$	$ACLR_{lower}$	$AM\text{-}AM_{var}$	$AM\text{-}PM_{var}$
No	30 %	-21 dBc	-21 dBc	2.3 dB	61.0^o
Yes	36 %	-56 dBc	-57 dBc	0.6 dB	3.2^o

Table 4.8: Comparison of the measured metrics with the LTE signal with and without DPD.

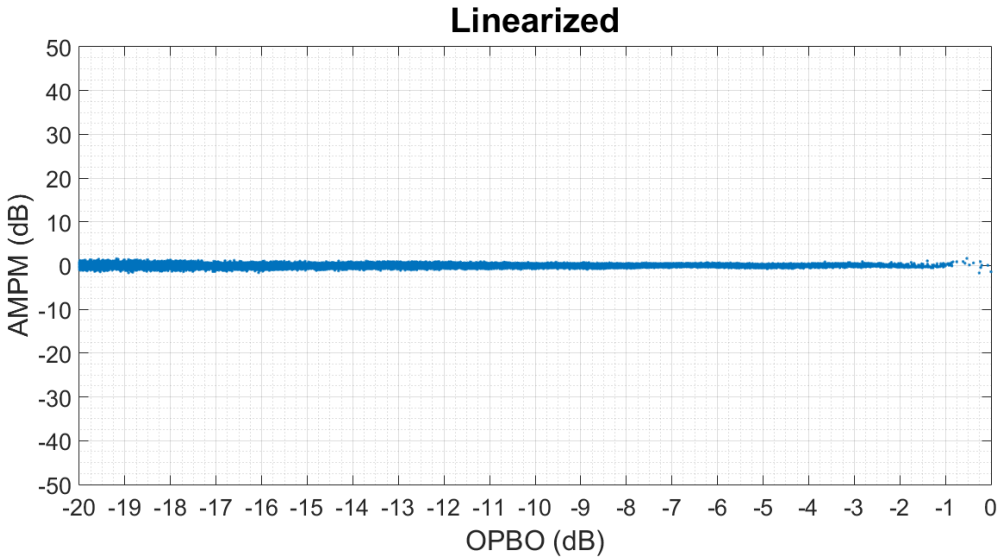

Figure 4.44: Linearized AM-PM conversion with a LTE signal and using the 7th order approximation.

Chapter 5

Conclusions

This chapter makes an analysis of the work performed under this Msc. dissertation. In this analysis it is important to: verify if the defined goals were accomplished; assert how well the developed amplifier compares with other state-of-the-art examples; and to identify its shortcomings. Future work suggestions are also portrayed in this chapter.

5.1 Critical Analysis

The first step when evaluating any work is to verify if the previously established goals were accomplished. These kinds of architectures only make sense if they provide clearly better efficiencies at high OPBO, when compared to single-transistor amplifiers. To make this comparison, the branch amplifier can be used. In terms of peak efficiencies, the branch PA reaches η = 72% and PAE= 67%. So, the practical circuit suffers from a decrease of 3% for η and 9% for PAE. Those are reasonable differences, since the first case is a circuit simulation and the second case a real circuit. But even with that clear disadvantage, the practical circuit excels at lower powers. The branch PA presents PAE values of 35% and 27% versus the measured 57% and 45%, respectively for -6 dB and -8 dB of OPBO. This represents an increase of around 20%. If the OPBO@PAE=50% metric is taken into account, the branch amplifier presents only -3 dB. This means that the practical OphPA is able to keep PAE> 50% at half the power the branch PA can. The efficiency advantages are clear in this implementation.

Table 5.1 presents the comparison of this PA with other Doherty or Outphasing-like architectures existent in the current literature. The best amplifiers the author found in the literature were chosen for this comparison, as well as another Msc. dissertation developed at Universidade de Aveiro. At the first sight, one may realize that the operational frequency is similar for most cases. Although the first two examples present clearly better results, the other ones are comparable to the produced amplifier. In [38] an OPBO@η=50% of -12 dB, but a very complex structure of 4 transistors is required and no information is given about its PAE performance. [36] and [43] present lower drain efficiency maximum values, and also do not give much information about the PAE. If [44], the other Msc. dissertation, is used to compare, this work presents slightly higher η peaks, but lower PAE ones. In terms of efficiency performance at OPBO, both metrics are better in this work.

In Table 5.1, information about the operational bandwidth of the amplifiers is omitted. That happens, because the definition of operational bandwidth is not the same in all of them

Refs.	RF Inputs	Transistors No.	Freq. (GHz)	η/PAE max (%)	η/PAE (%) @ Pmax	Pmax (dBm)	OPBO (dB) @ PAE=50%	OPBO (dB) @ η=50%
[10]	2	2	1.20	x/70	64/60	44.4	-6.8	x
[39]	2	2	2.15	78/75	77/74	49.6	-6.5	-9.1
[38]	2	4	2.14	66/x	66/x	50.5	x	-12
[36]	1	2	2.17	61/x	57/x	51.4	x	-8
[43]	2	2	2.14	63/x	57/x	25.7	-6.0	x
[44]	2	2	1.80	65/62	63/59	42.8	-4.8	-5.7
This work	2	2	2.30	69/58	60/54	42.6	-6.0	-7.3

Table 5.1: Comparison of the produced power amplifier with other works in literature.

Refs.	Signal Type	PAPR (dB)	Signal Bandwidth (MHz)	η_{avg} (%)	ACLR (dBc)
[10]	W-CDMA	6.7	5	40	-57
[39]	W-CDMA	9.6	3.8	50	-49
[36]	x	7.5	3.8	46	-50
This work	LTE	10.3	10	36	-56

Table 5.2: Comparison of the produced power amplifier with DPD with other works in literature.

and there is not enough information to make a rigorous analysis using consistent criteria. Anderson, in [10] defines it as the frequency range where PAE at OPBO=-6 dB is higher than 45%, and under those conditions, his works achieves a remarkable 100% bandwidth. Qureshi in [39], defines it as having at least 48 dBm of peak output power with $\eta > 60\%$ and presents a 7% bandwidth. These are only two examples, but demonstrate the problem. Until a standardized definition of operational bandwidth is agreed upon, directly comparing this metric in these architectures is not a rigorous task.

The linearity analysis presented very interesting results. The designed OphPA produces considerable nonlinear distortion, but that is also seen in other similar implementations. Since this architecture already requires a digital processing unit to generate its driving signals, the usage of DPD algorithms does not come at a high cost. In fact, if that processing unit is capable of doing it, it is only a natural step to take in the implementation. After the DPD was employed, the amplifier improved all the measured metrics and reached linearity metrics on a par with other state-of-the-art works as seen in Table 5.2. Some of the previously presented works were not used in these comparisons, because either they did not present modulated signal results or did not go through a linearization process. The average efficiency of this work is the lowest, but it also uses the highest PAPR values. The efficiency could be improved if this PA was design from the start to benefit this specific signal. In terms of ACLR, this work excels as it is roughly equal to [10]. All these results were obtained with

the highest signal bandwidth across the mentioned works, as they do not exceed 5MHz and this work used a 10MHz signal.

The produced amplifier shows signs that it can be used in real applications, according to the tested metrics. Through simulations and measurements, it was demonstrated that it can be operated using a simple polynomial equation to produce the driving signals without compromising PA performance. The acquired results also showed that even low order polynomials can provide reasonable solutions. Modulated signal measurements also demonstrated that the polynomial approximations did not hurt the average efficiency, and in the tested cases it actually improved it. This representation of the LUT is, therefore, validated throughout all the performed tests.

The produced amplifier suffers from a clear shortcoming that may compromise its usage in the next generation of communication systems: the sensitivity to the load changes. That, as previously stated, is a problem that has only recently began to be addressed, so that the existent work is still at an early stage of development.

5.2 Future Work and Recommendations

There are not many more measurements to be done to test the performance of this amplifier. The only suggestions the author makes is to; test different DPD techniques to verify their performance; and try to adjust the frequency-shift.

The full implementation with a real digital processing unit used in telecommunication applications is also important, since, in this work, that device was substituted by a personal computer.

Finally, if new implementations of this idea are to be designed, the author proposes some recommendations:

- **Use a more efficient branch PA:** to get higher peak efficiencies to better compete with some state-of-the-art amplifiers, a more efficient PA configuration can be used in the branch. A class E implementation can be tested, but it is possible to improve it with a class F PA, if the transistor is characterized for higher frequencies. The matching networks may become more complex with this.
- **Avoid the usage of class AB polarizations:** although in this implementation that was done to increase gain, it is not an optimal solution, because it increases PA power consumption when there is no input power. In short, biasing points closer to the class B amplifier are recommended.
- **Desensitize the PA to load variations:** the solution to this is not clear and more research needs to be done, but, for using amplifier configurations like this one in 5G, it is crucial to find a new solution or to test the already existent ones in this scenario.
- **Increase the operational bandwidth:** this is also an important improvement that needs to be made to tackle the arising challenges. Approaches like [10] can be followed to achieve this goal.
- **Design to a specific signal:** If the amplifier is being designed to operate with specific types of signals, it is beneficial to have that in mind in the design stage to maximize its average efficiency.

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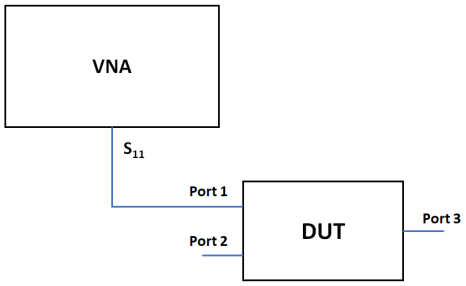
Appendices

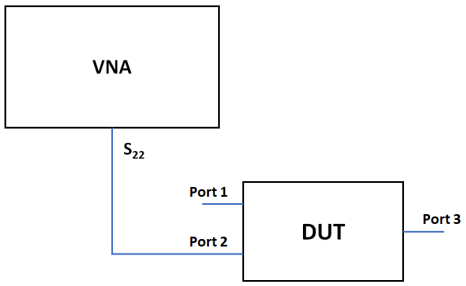
Appendix A

S Parameters Measurement

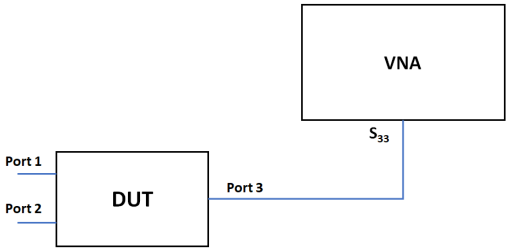
To perform these measurements the transistors must be removed to guarantee that they are not damaged in the process. The reflection coefficient must be measured in all the ports of the DUT and, since there is no active device, there is no need to take additional precautions in the process. These conditions must be replicated in the simulator, using an electromagnetic model. The removal of the transistor also makes the device ports isolated, meaning that there will be no transmission between ports. So, to each port it only makes sense to measure the S_{nn} parameter. The practical measurements may be performed using a VNA, Vector Signal Analyzer as described in Figures A.1. After this process is concluded, the practical and simulation results should be similar, as any deviation indicates there are unpredicted differences in the practical implementation. The isolated ports will also allow to better locate the problem in the circuit.



(a) S_{11} measurement.



(b) S_{22} measurement.



(c) S_{33} measurement.

Figure A.1: Block Diagram of the S Parameters measurements.

Appendix B

Outphasing CW Measurements

A lot of a power amplifier characteristics may be analyzed in continuous wave measurements. In this OphPA, the set-up represented in Figure B.1 was used throughout all the performed CW tests. Naturally, it has a crucial role in this work. So, it is important to properly detail the role of each part of the set-up.

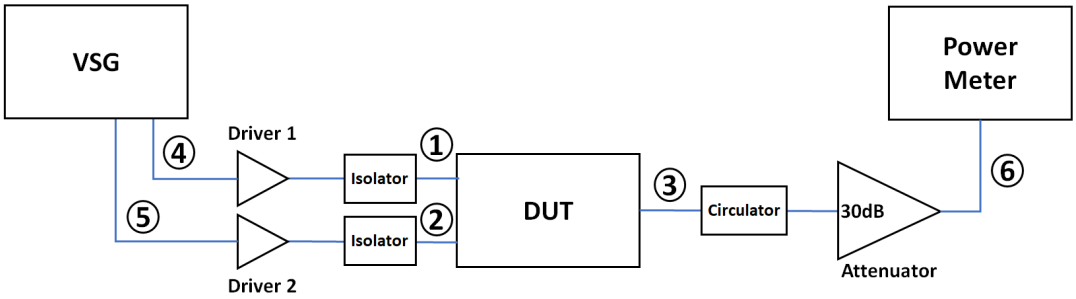


Figure B.1: Block diagram of the continuous wave measurements set-up.

Starting with the VSG: it controls the DUT input signals. In this case controls the input power and the phase difference, since no information is being transmitted. The used VSG is not capable of supplying the necessary input power to the device, so the Drivers 1 and 2 were introduced consisting of two sets of power amplifiers. Although these are highly linear PAs, they are not perfectly linear and have different AM-AM and AM-PM conversions. Before starting to measure the DUT, their power and frequency responses must be measured in order to adjust the outputs of the VSG to compensate it. Since two Drivers are used and their AM-PM conversion is not the same, that could cause complications when testing the OphPA. But, since new LUTs must be extracted, these differences are taken into account and the PA performance will not be compromised. The Isolators are placed to protect the drivers from reflected waves. The DUT is powered by a DC voltage source capable o measuring how much DC power is being delivered to it. The circulator protects the DUT output from reflected waves. The power meter, as the name indicates, measures the output power of the DUT. But, since the power meter cannot measure the high output powers of this PA, a 30 dB attenuator is placed.

Since there are several pieces of equipment surrounding the DUT, to get precise measurements it is important to exclude their influence. So, before any test is done, a proper calibration of the equipment needs to be performed. These need to be done to all frequencies and power levels to be effective. In the following list, the indicated number correspond to the ones represented in Figure B.1. The calibrations steps are the following:

1. Calibrate the power meter;
2. Measure the outputs of the VSG, connecting 4 and 5 to 6;
3. Measure the output attenuator and circulator, connecting 4 and 5 to 3;
4. Measure the two Drivers separately, connecting 1 and 2 to 3;

The difference between the LUT determination and measurement is only on the signals sent by the VSG, so this set-up and calibration procedure is valid for both cases.