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# **Two terminal organic nonvolatile memory devices**

By

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A thesis submitted in partial fulfillment for the  
degree of Doctor of Philosophy

in the

College of Physical and Applied Sciences

School of Electronics

June 2014

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## Abstract

The behaviors of organic memory devices based on carbon nanotubes in two-terminal structures are reported. The memory structures were fabricated in the forms of metal-insulator-semiconductor (MIS) and metal-insulator-metal (MIM) structures. The devices utilize  $\text{AlO}_x$  or layer-by-layer (LbL) deposited single walled carbon nanotubes (SWCNTs) in the memory stack. For MIS-based memories, SWCNTs were embedded, between SU8 and polymethylmethacrylate (PMMA) to achieve an efficient encapsulation. The devices produced a clear clockwise hysteresis (with a 6V memory window) centered closed to 0V. Hysteresis in these devices attributed to the charging and discharging of SWCNTs from metal gate electrode. The devices exhibited high charge storage densities and demonstrated 94% charge retention due to virtue of the superior encapsulation. CNTs is also used for the MIM memory structures as charge traps embedded between two PMMA insulating layers. The stack was sandwiched between two aluminium electrodes to form an Al/PMMA/SWCNTs/PMMA/Al structure. The current-voltage (I-V) characteristics of this type of memory devices exhibit electrical bistability and non-volatile memory characteristics in terms of switching between high conductive (ON) and low conductive (OFF) states. The two conductive states were programmed by applying a positive and negative voltage pulses for the ON and OFF states, respectively.

Another filamentary based electrochemical metallization (ECM) memory structure based on  $\text{AlO}_x$  was also fabricated and characterized. Copper/ $\text{AlO}_x$ /tungsten (Cu/ $\text{AlO}_x$ /W) ECM memory cells show reproducible resistive switching with an ON/OFF ratio of about  $5 \times 10^2$  at a reading voltage of 0.1 V and reliable retention characteristics. The conduction of the devices was explained through back-to-back Schottky contacts in the OFF state, while it exhibits ohmic behavior in the ON state. Thermionic emission model was used to calculate the barrier heights of the Schottky contacts. The rupture of the Cu filament proved to occur at the weakest point of the filament inside the  $\text{AlO}_x$ . Using Ohms Law, the slope of the linear I-V characteristics in the ON state was used to extract the Cu filament resistance and its diameter was estimated to be between 6 and 23 nm.

# Publications

## Book Chapter:

1. **A. Sleiman**, M.F. Mabrook, P.W. Sayers and D.A. Zeze, “Two terminal Organic non-volatile memory (ONVM) devices”, Handbook of flexible organic electronics, Materials, manufacturing and applications, Woodhead Publishing, In press, 2014.

## Journal Papers:

2. H. S. Alaabdlqader, **A. Sleiman**, P. Sayers and M. F. Mabrook, “Graphene Oxide-Based Non-volatile Organic Field Effect Memory Transistors,” IET Circuits, devices & systems, In press, 2014.
3. **A. Sleiman**, P.W.Sayers, M.F.Mabrook, “Mechanism of resistive switching in Cu/AlO<sub>x</sub>/W nonvolatile memory structures,” J. App. Phys., vol. **113**, p. 164506, 2013.
4. **A. Sleiman**, M. F. Mabrook, R. R. Nejm, A. Ayesh, A. Al Ghaferi, M.C. Petty, and D.A Zeze, “Organic bistable devices utilizing carbon nanotubes embedded in poly (methyl methacrylate),” J. App. Phys., vol. **112**, p. 024509, 2012.
5. **A. Sleiman**, M. C. Rosamond, M. Alba Martin, A. Ayesh, A. Al Ghaferi, A. J. Gallant, M. F. Mabrook, and D. A. Zeze, “Pentacene-based metal-insulator-semiconductor memory structures utilizing single walled carbon nanotubes as a nanofloating gate,” Appl. Phys. Lett., vol. **100**, no.2, p. 023302, 2012.

## Conference Papers:

6. **A. Sleiman**, M. Kreyenborg-Nichols, T. Alshahrani, D. Ashall, P. W. Sayers and M. F. Mabrook, “Enhanced holes mobility in AlO and pentacene-based OTFTs due to the passivation of the oxide surface using PVP,” E-MRS, Lille, France, 26-30 May, 2014.
7. T. Alshahrani, A. El-Betany, M. F. Mabrook, H. Tai, I. Alrougy, **A. Sleiman** and N.McKeown, “The effect of pH of a new PAMAM dendritic material on the performance of organic bi-layer solar cells,” E-MRS, Lille, France, 26-30 May, 2014.
8. **A. Sleiman**, Dagou A Zeze, Razan R. Nejm, Ahmad Ayesh, Amal Al Ghaferi and Mohammed F. Mabrook, “Carbon Nanotubes in Organic Memory Structures,” 12th European Conference on Molecular Electronics, London, UK, 3–7 September, 2013.
9. **A. Sleiman**, A. Albuquerque, S.J.Fakher, M.F.Mabrook, “Gold nanoparticles as a floating gate in Pentacene/PVP based MIS memory devices,” IEEE NanoTechnology, Birmingham, UK, 20-23 August, 2012.
10. **A. Sleiman**, M.F.Mabrook, “Solution-deposited nanoparticles as nanofloating gates in organic memory devices,” International conference on advanced materials energy and environment, Ohio, USA, 09-11 May, 2012.

*Dedicated to my Mom, my Dad, Jaafar, Rania, Nisrine, Sonia, Chirine, Jaymee and especially Hassan*

## **Acknowledgements**

I would like to thank my supervisor, Dr. Mohammed Mabrook, for his endless support and encouragement. His scientific and research experience helped me a lot throughout my work. I do thank him as well for sharing his life experience, his advice and support about everyday life situations. He was a tutor, a teacher, a supporter and an advisor to me throughout all my PhD studies at Bangor University.

I would like to thank Dr. Dagou Zeze at the school of engineering and computing sciences, Durham University, Durham, UK. Dr. Dagou Zeze supported and encouraged me in difficult times and he believed in my ability at the beginning of my research career. His non-stopping support, encouragement and recommendations were a main reason in the completion of this work. The collaboration with him, Dr. Ahamd Ayesh and Dr. Amal Al-Ghaferi in the layer-by-layer deposition of carbon nanotubes was fruitful.

Special thanks to Dr. Paul Sayers for his support, help and encouragement in our cleanroom facility at Bangor University. His endless help and advice in technical and scientific aspects of my research were very beneficial. I would also like to thank all members of Plastic Electronics Research group, especially Prof Martin Taylor, Dan, Colin and Thamraa for their encouragement and discussions.

I would like to thank Bangor University for the award of a 125 anniversary studentship.

Last but not least, many thanks to all my friends who made my stay in Bangor a better experience, especially Talal, Hassan and Mohammed.

# Chapter 1

## Introduction and Motivation

### 1.1. Introduction

The evolution of information and communication technologies in the last few years has resulted in increased demand for new data storage systems with higher storage capacities. All the new applications and devices in the market such as high definition TVs, iPADS, iPODs, kindles, MP3s and smart phones operates through the storage of large amounts of data. Most of these devices are made to be hand-held and portable devices for everyday use for communication or entertainment purposes. Thus the speed and size of the memory devices used to store such large amount of data are considered important parameters when choosing the type of memory used. Moreover, the energy efficiency of the storage device is a very important parameter when considering hand-held devices which need to keep running for a long time without the consumption of a lot of power.

Depending on the energy consumption of the storage device, the memory devices are split into two types: volatile memory (VM) and nonvolatile memory (NVM) devices [1]. VM devices need constant supply of power to keep the data stored inside it, while NVM devices are able to keep the data stored even when the power is switched off. Thus NVM technology is a suitable candidate for the storage of large amounts of data when considering energy efficiency for hand-held and portable devices.

Nowadays, the most familiar type of the NVM for everyday users is the flash memory. Flash memories are very useful and power-efficient devices used in most of our portable and hand-held devices. Behind the tremendous success story of the flash memory is the NVM technology which depends on a metal-oxide-semiconductor field-effect-transistor (MOSFET) embedded with a floating gate on which charges can be stored [2]. The success of the flash memory in hand-held devices might be hindered by its limited scalability [3]. One of the major parameters that the memory technology should have is its ability to be scalable down to be compatible with highly desirable small sizes of the hand-held devices. The physical scalability of the flash memory concept is limited to around 32 nm thick oxide [3], and this might be a problem in the near future if the evolution of the electronic devices

continues reducing its dimensions. Alternative memory technologies are being investigated to have better scaling capabilities such as the two terminals NVMs [4, 5].

## 1.2 Two terminals NVM devices and the crossbar structure

Two terminal NVM (2T-NVM) devices composed of different materials (insulators or semiconductors) sandwiched between two electrodes exhibit two stable electrical states which can be controlled by an external electrical bias. The two stable electrical states (namely, ON and OFF states) may be resistive, ferroelectric or capacitive depending on the device structure [1-4]. The simple device structure of the 2T-NVM makes the scaling capabilities much better than the existing floating gate MOSFET flash memory technology. In this technology the scalability depends only on the width of the top and bottom electrodes and the thickness of the material in-between. The simple structure of 2T-NVM makes such devices very easy to integrate in electronic circuits; one of the simplest ways to integrate such structures in a circuit is using crossbar structure. In a crossbar structure the bottom electrodes are deposited on the substrate, the active layer is engineered

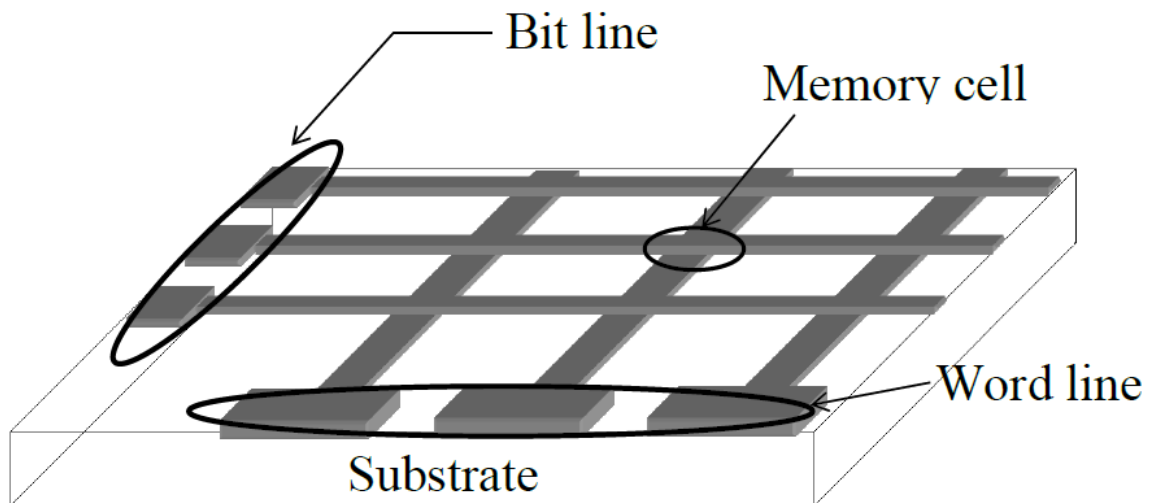


Figure 1.1: cross bar structure and the resulting array of memory devices.

depending on the type of 2T-NVM devices, and then the top electrodes are deposited to form an array as shown in Figure 1.1. Each cross area between the bottom electrode and the top electrode is a storage memory cell. However, the external stimulus and control of each cell in the crossbar structure itself is not the simplest. The application of an external electrical stimulus on a top electrode affects the neighboring and same row memory cells through leakage currents, the so-called cross talk interference mechanism. The addition of a diode or a transistor with each cell that allows or blocks the current from reaching the cell would improve the reading capability and reduce the effect of the cross talk interference [5].

2T-NVM devices also have the ability to be integrated in architectures which benefit from a third dimension in the memory stack. The third dimension is a vertical stack of memory cells separated by an insulator. The vertical stack is expected to increase the memory storage density without any consequences on the memory performance. Depending on the type of 2T-NVM consequent layers may be added on top of the first memory stack, to end up in a larger number of memory devices in the same area of substrate. Song et al. [4] demonstrated on a resistive type organic NVM (ONVM) with three consecutive stacks of memory devices in a 8x8 cross bar architecture. The performance of 2T-NVM device is tested by its retention characteristics, ON/OFF ratio, endurance upon ON/OFF cycling and switching speed. Retention characteristics measures the time a device can maintain its electrical state while the power is turned off, a retention characteristics of several years have been demonstrated for different 2T-ONVM [6-7]. ON/OFF ratio is the ratio of the current in both states, high ON/OFF ratios was reported for certain 2T-ONVM structures [6]. Life time endurance characteristics of the memory device is the number of times the device can operate, i.e. perform the write-read-erase-read cycle, endurance characteristics vary in different 2T-ONVM structures and more than  $10^5$  cycles has been demonstrated for some devices which is comparable to the flash memory performance [7]. Resistive switching speed is the speed a 2T-ONVM can respond to the external electrical stimulus and switch from one state to another, a voltage pulse of several nanoseconds was reported to result in resistive switching of the devices in the resistive type 2T-ONVM [8]. Such interesting scalability features, the simple cross bar structures, 3D stack and the high performance made the 2T-NVM a potential candidate for future NVM applications.



### **1.3. Organic 2T-NVM for flexible electronics applications**

Another revolution in the electronic devices designs is the fabrication on flexible substrates. In late 2013, Samsung Electronics demonstrated a phone that consists of a matchbox-sized hard enclosure, with a paper-thin, flexible color screen attached to one end. The bendable screen consisted of organic light emitting diodes deposited on a plastic substrate [9]. As such, organic materials have attracted a lot of attention recently in research due to their interesting features and potential applications in flexible electronics. Unlike most silicon based devices, organic materials have an inherent flexibility, which make them viable for use on flexible substrates without developing stress fractures or losing their electronic characteristics. This has allowed for the development of a new generation of electronic devices called organic electronic devices. Such devices have attracted interests from both academic and industrial researchers due to their low cost, low temperature processing and mechanical flexibility. Applications such as organic solar cells [10], light emitting displays [9], organic field-effect transistor [11] and sensors [12] are all rather in advance stages of research.

A major part of organic electronics research is targeted towards the fabrication of a reliable storage media to be used in flexible electronics applications. Organic NVM (ONVM) emerges as the leading candidate for such applications, offering flexibility, printability, low fabrication cost, and most importantly the two key parameters for future memory applications: power efficiency and the simple device architectures which allows its scalability. Many small organic molecules and polymers such as pentacene, polymethymetacrylate and polychloro-paraxylylene have been used for 2T-NVM applications [13-15].

## 1.4 Single walled carbon nanotubes as charge storage nodes

In this thesis, the fabrication and characterization of ONVM devices using single walled carbon nanotubes (SWCNTs) as charge storage nodes will be presented. The SWCNTs have attracted a lot of attention recently and been utilized in different electronic applications [16]. For the nano-floating gate application, it is believed that discrete charge storage nodes display longer charge retention characteristics than the traditional continuous floating gate equivalents [17, 18]. Typically, Au, Ag or Ge nanocrystals (NCs) or C60 functional materials are discrete charge storage nodes in Metal-Insulator-Semiconductor (MIS) or transistor memory devices [19-21]. Issues related to lack of chemical inertness, mechanical and thermal stability of such materials hinder their applications as storage nodes in ONVM devices [22] especially in organic and plastic electronics where low temperatures fabrication processes are desired. SWCNTs were found to be more favorable for such applications because of their higher thermal stability, chemical inertness, reduced surface states and favorable work function (4.8 eV for pristine SWCNTs) [22]. For instant, reduced surface state densities enhances the retention capability of SWCNTs, while the tunable band gap of SWCNTs helps in the selection of metallic versus semiconducting SWCNTs for such application [22]. SWCNTs embedded in a high-k dielectrics were reported as a nanofloating gate in MIS [23] and transistor memory devices [22]. The nearly ideal surface states enhances SWCNTs' charge retention characteristics compared to that of metallic NCs [24-25]. Their high thermal and mechanical stability and relative chemical inertness also make SWCNTs attractive choices for organic and flexible electronics applications. Earlier reports used SWCNT as a floating gate in hybrid organic/inorganic memory devices. The hybrid memory devices where fabricated on Si/SiO<sub>2</sub> substrates using SWCNTs as a floating gate [22-23]. The use of silicon as a semiconductor and SiO<sub>2</sub> as the first insulating layer simplifies the analysis of the effects of SWCNTs. However, Si/SiO<sub>2</sub> is not suitable substrate for the use in flexible electronics.

In this work layer-by-layer (LbL) deposited SWCNTs will serve as charge storage nodes in 2T-ONVM devices. The 2T-ONVM devices will be fabricated in the simple Metal-Insulator-Metal (MIM) and Metal-Insulator-Semiconductor (MIS) structures where the SWCNTs will be embedded in the middle of the insulating stack in both structures to

produce the memory effect. The memory effect will be characterized through the hysteresis in the capacitance-voltage (C-V) characteristics of the MIS structure and resistive switching between two stable resistive states in the current-voltage (I-V) characteristics of the MIM structure. SWCNTs will be deposited using the LbL deposition technique which ensures the SWCNTs to be deposited in a thin-film-like layer to have charge retention advantages for such applications [26].

### **1.5 Filamentary-based MIM resistive switching 2T-NVM**

Another part of this work will present the fabrication and characterization of 2T-NVM in the filamentary-based resistive switching MIM devices. NVM devices exhibiting resistive switching (RS) phenomena due to the formation and rupture of a metallic filament inside an oxide thin film, emerges as a reliable candidate for the next generation of non-volatile memory devices [27]. The formation of the metallic filament under sufficient applied voltage occurs either due to the anionic migration of oxygen vacancies inside the thin film [28], or due to the migration of the cations of an electrochemically active electrode (AE) inside the thin film [29]. NVM devices benefiting from RS due to cationic migration are usually known as electrochemical metallization cells (ECM). The structure of an ECM consists of an AE (usually Cu or Ag) which acts as a source of mobile cations, the switching medium (usually thin oxides [30], sulphides [31] or selenides [32] which acts as a thin film of solid electrolyte inside which the metal ions migrate, and an electrochemically inert counter electrode (CE) (usually Pt or W) where the cations get reduced to build up the metallic filament. As such, the mechanism of RS in an ECM is widely accepted [29-32] as a redox reaction which involves the oxidation of the AE atoms to produce mobile cations that migrate inside the thin film and reduced at the CE to form a metallic filament in the ON state, and the dissolution and/or rupture of this metallic filament in the OFF state.

Aluminum oxide ( $\text{AlO}_x$ ) has been widely reported as a switching medium in different memory structures, which use ultra-thin  $\text{AlO}_x$  with Pt, Al, Ti, or TiN metal electrodes in the memory stack [33-34]. In these structures the formation of a filament is attributed to the anionic migration of oxygen vacancies inside the  $\text{AlO}_x$  thin film. In this study we report on the mechanism of resistive switching in  $\text{AlO}_x$ -based ECM memories based on the cationic migration of electrochemically active copper (Cu).

## 1.6 Thesis structure

The main purpose of this thesis was to investigate the use of 2T-NVM devices using low cost structures for future applications. As charge storage nodes, SWCNTs have been used in silicon-based devices as a floating gate in memory structures [22, 23]. In 2T-ONVM, SWCNTs have been used as charge traps in embedded MIM memories as they were distributed uniformly throughout the insulator and no retention characteristics were reported [35]. In this study, the fabrication of 2T-ONVM using SWCNTs as charge storage nodes in MIS and MIM memory structure is the first part of this work. However, in our new approach SWCNTs is utilized as the floating gate in a middle-trap-structure. Layer-by-layer technique was used in the deposition of SWCNTs and results in a thin-film structure of the SWCNTs in-between two organic insulators. The electronic properties of the structure exhibited clear resistive switching behaviour and enhanced retention properties. The second approach investigated in this study is the fabrication of AIO-based filamentary-based RS memories, the so-called ECM memories. In the filamentary-based ECM memory structure, the use of different counter electrodes to be compatible with  $\text{AlO}_x$  as the electrolyte is investigated. The selection is based on the fabrication of low-cost materials for the emerging ECM memory technology. In our ECM structure a combination of copper as an active electrode,  $\text{AlO}_x$  as the electrolyte and tungsten as the counter electrode. Such combination of low-cost materials to fabricate ECM with enhanced memory characteristics is one of the main highlights of this work.

Chapter 2 will present different 2T-NVM structures in the literature and will emphasize on the physics and working mechanisms of the structures of interest in this thesis: embedded MIS, embedded MIM and the filamentary-based ECM memory.

The materials used in this investigation, the deposition techniques used to deposit different materials and build the memory structures will be introduced in Chapter 3. The LbL deposition technique of the SWCNTs will also be detailed.

Chapter 4 will present the control MIS devices fabricated without CNTs as a floating gate. The utilization of LbL deposited SWCNTs in embedded MIS and MIM structures will be presented in Chapter 5. The memory performance in terms of hysteresis in the C-V characteristics of the MIS structures and resistive switching in the I-V characteristics of the

MIM structures will be presented. The analysis and the understanding of the memory behavior of the structures in terms of trapping and detrapping of charges will be explained through the appropriate physics modules. Calculations of the amount of charges stored in the structures will be presented in addition to the recorded charge retention characteristics of the devices.

In Chapter 6, the fabrication, characterization and mechanism for resistive switching in AIO-based filamentary-based ECM memories is presented. The RS behaviour and the retention of its ON and OFF states will be presented. The analysis of the filament formation and rupture is introduced. The position of the filament rupture is determined from the shape of the I-V characteristics and from the schottky-barriers heights differences between electrodes. Calculation of filament diameter through physical models is also presented.

Chapter 7 will give a brief summary of the work presented in the thesis and will conclude the work. Further work is suggested to further contribute to the enhancement of the fabricated 2T-NVM for future applications.

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## Chapter 2

### Two terminal nonvolatile memory structures

#### 2.1. Introduction

In general, nonvolatile memory (NVM) technologies can be divided into two types depending on the way we externally stimulate and control the device. First type is NVMs that can be mechanically addressed such as hard disks, optical disks, floppy disks or magnetic tapes, these types of technologies are not of particular interest in this study. The second type includes the NVMs that are electrically addressed which again can be divided into many types depending on their structure, working mechanism and the electrical value that defines the ON and OFF states.

A definition of the electrically addressed nonvolatile memory devices and how to perform WRITE, ERASE and READ processes will be presented in section 2.2. The electrical parameters that define the ON and OFF states of the NVM can be polarization, resistance or capacitance.

The structures of interest in this thesis are embedded metal-insulator-semiconductor (MIS) (capacitive), embedded metal-insulator-metal (MIM) and the filamentary-based electrochemical metallization (ECM) (resistive) memories. Thus detailed descriptions of the physics and the working mechanism of these structures will be presented. Section 2.5.2 will present the structure of the filamentary-based MIM devices, the resistive switching modes, bipolar and unipolar, which these types of devices exhibit, typical I-V characteristics and the resistive switching mechanism in terms of the formation of the conducting filament. While section 2.5.3 will present another type of resistive memory structures based on embedded MIM devices. Their structure, typical RS behavior, typical I-V characteristics and working mechanism will also be explained.

The physics of capacitance-based NVM in the form of embedded MIS structure will be detailed in section 2.6. Firstly the simple MIS capacitor structure will be presented in section 2.6.1. Its band structure, flatband voltage under different biasing regimes, the

threshold voltage condition and the resultant C-V characteristics will be explained in sections 2.6.2, 2.6.3, 2.6.4 and 2.6.5, respectively. As the fabricated embedded MIS memory will be based on organic materials, organic MIS structure and the difference from simple silicon-based MIS will be shown in section 2.6.6. Finally, the memory application of the MIS structure where the floating gate is added within the insulator will be presented in section 2.6.7. The interface states non-ideality, fixed dielectric traps non-ideality, the charges trapped in the floating gate and the resultant hysteresis in the C-V characteristics of the embedded MIS structure plus an explanation of the WRITE-READ-ERASE processes will be detailed in sections 2.6.7.1, 2.6.7.2, 2.6.7.3 and 2.6.7.4, respectively.

## **2.2. Definition**

Electrically addressed NVMs are devices that exhibit two distinct and stable electrical states. The NVM device should be able to perform the WRITE, ERASE and READ processes. This means, the user should be able to impose any of the two distinct electrical states; i.e. perform the WRITE process of a certain state and consequently perform the ERASE process of the other state. In addition to the WRITE and ERASE processes the user should be able to sense in which state is the device without changing the status of the device; i.e. perform the READ process [1-4]. From electrical point of view, this can be achieved using an external voltage stimulus on the device. Applying a certain voltage will impose on the device to be in the first state, while another voltage will impose the second state, these are the WRITE and ERASE processes. The READ process can be performed if at a certain range of voltages the two states exist, and applying a voltage in this range will identify what the previous state of the device was, without changing it [1-4].

Figure 2.1 is an example of a NVM memory device that exhibit two distinct and stable electrical states, namely “Electrical State 1” and “Electrical state 2”. Despite the electrical unit of the value tested, we define “Electrical State 1” as the ON state and “Electrical state 2” as the OFF state, the WRITE, ERASE and READ processes are explained as follows in the suggested example. At voltages lower than -8 V, electrical state 1 is imposed on the device, this is the WRITE process of state 1 and the device is in the ON state. At voltages

higher than 10 V, electrical state 2 is imposed and consequently this is the ERASE process of state 1 and the device is in the OFF state. In the range of voltages between -8 V and 10 V, state 1 and state 2 co-exist and thus any voltage in this range can perform the READ process and sense in which state is the device.

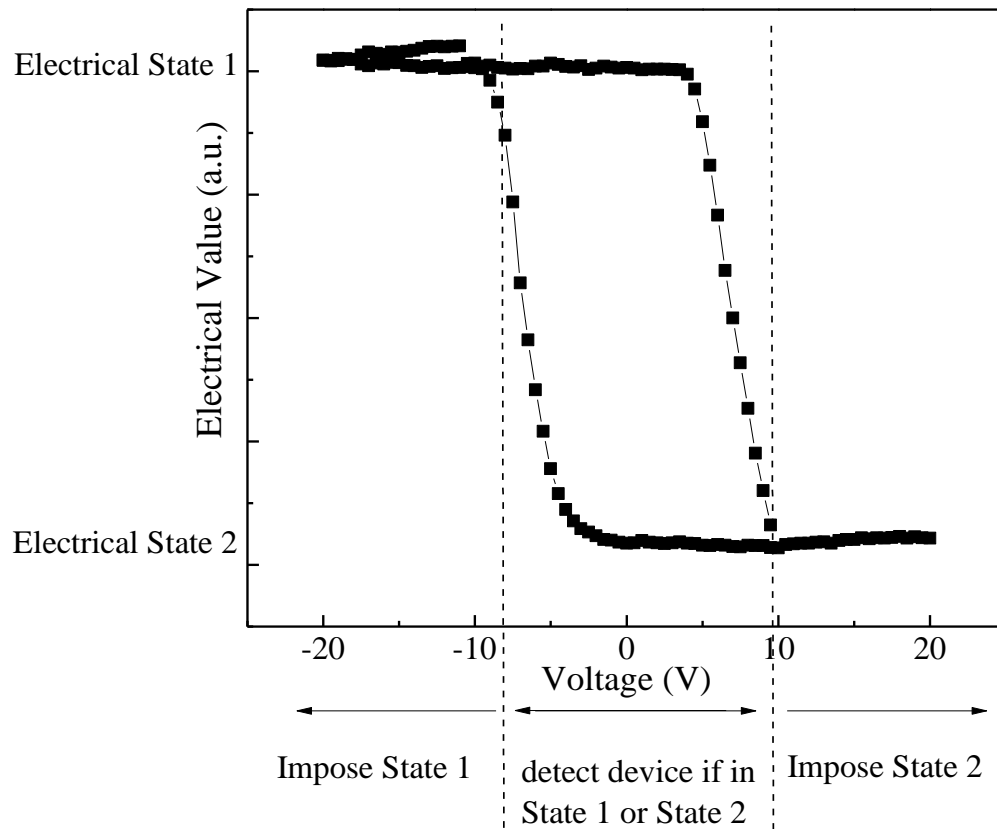


Figure 2.1: READ, WRITE and ERASE processes of distinct electrical states of NVM devices.

### 2.3 Types of NVM technologies

The NVMs can be divided into different types depending on the electrical value that defines its states [5-9]. The NVMs can be polarization-based such as Ferroelectric Random-Access-Memory (FeRAM), resistive switching such as filamentary-based MIM, charge transfer based MIM memory and embedded MIM structures, or capacitive such as floating gate embedded MIS structures (Figure 2.2).

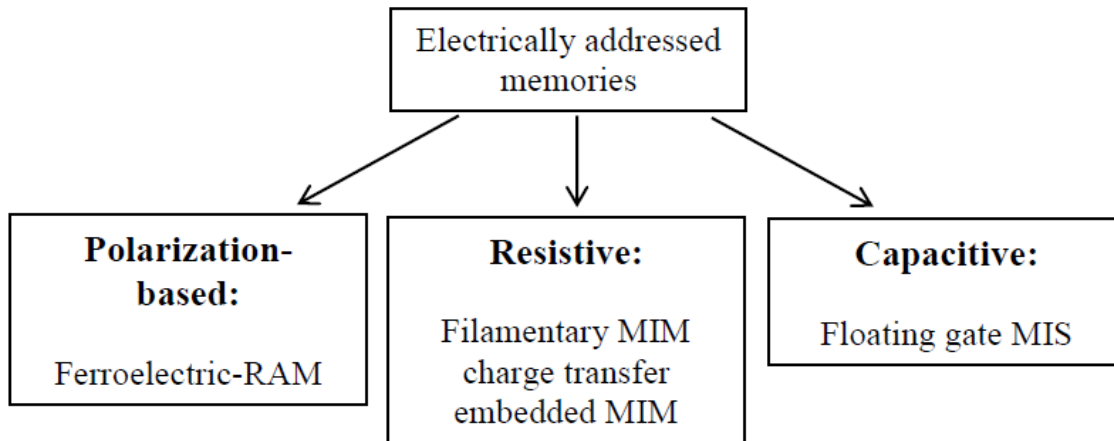


Figure 2.2: Electrically addressed two terminal memory devices

## 2.4 Polarization-based NVM

Polarization-based NVM are devices that exhibit two distinct and stable polarization values. Ferroelectric RAM (FeRAM) is an example of polarization-based NVM and its working mechanism is similar to that of the volatile Dynamic-RAM (DRAM) except that the dielectric material of the DRAM's capacitor is replaced by ferroelectric material [10], which results in non-volatile memory behavior. In DRAMs, the memory structure consists of one transistor connected to a capacitor that gets charged or discharged to define the ON and OFF states. When the transistor is switched ON, the current reaches the capacitor and charges it. When the power is turned OFF the capacitor gets discharged and the memory is turned to its OFF state. When the memory is in the ON state the capacitor loses the charges gradually, thus a continuous charging is needed to maintain the electrical state, which results in a volatile memory. On the other hand, in FeRAM, the ferroelectric material in the capacitor has remanent polarization characteristics and thus it exhibits a hysteresis loop in the polarization-voltage (P-V) characteristics. This hysteresis results in two stable electrically addressed polarization states which may define the ON and OFF states and results in nonvolatile memory behavior of the FeRAM [10]. Although FeRAM is an interesting application for NVM, it is not of particular interest in this study.

## **2.5 Resistive-based NVM**

Resistive-based NVM are devices that exhibit two distinct and stable resistance or conductance states. In turn, resistive-based NVM can be divided to many types depending on the physics behind the resistive switching of the devices. Examples of resistive-based NVM are charge transfer based MIM memory, filamentary-based MIM and embedded MIM structures [1-8].

### **2.5.1 Charge transfer based MIM memories**

Charge transfer memories consist of a combination of two materials, one is an electron donor and the other is an acceptor. The charge transfer that occurs from the donor to the acceptor upon the applied bias, changes the resistivity of the acceptor material and the device between two different stable resistance states [10]. Charge transfer based MIM memories attracted a lot of attention for organic electronics applications recently [11] however it is not the focus of this thesis.

### **2.5.2 Filamentary-based MIM memories**

#### **2.5.2.1 The structure of filamentary-based MIM devices**

Filamentary based MIM memory device is also called resistive switching RAM (ReRAM) and exhibit resistive switching (RS) between two stable resistance states due to formation and dissolution of a metallic filament [12]. The basic structure of the ReRAM is an oxide sandwiched between two metals in the MIM structure. Upon the application of different biases a conducting filament formed and rupture inside the oxide. The class of ReRAM that relies on the deposition of an active electrode metal such as Ag or Cu is called electrochemical metallization (ECM) memory [12, 13]. The structure of the ECM can be considered as an electrochemical cell consisting of an active electrode (AE), an electrolyte and a counter electrode (CE) as shown in Figure 2.3. The memory behavior is represented by the switching behavior of its current-voltage (I-V) characteristics between two stable

resistance states, low and high resistance states (ON and OFF states) upon the formation and dissolution of a conducting filament inside the electrolyte [13].

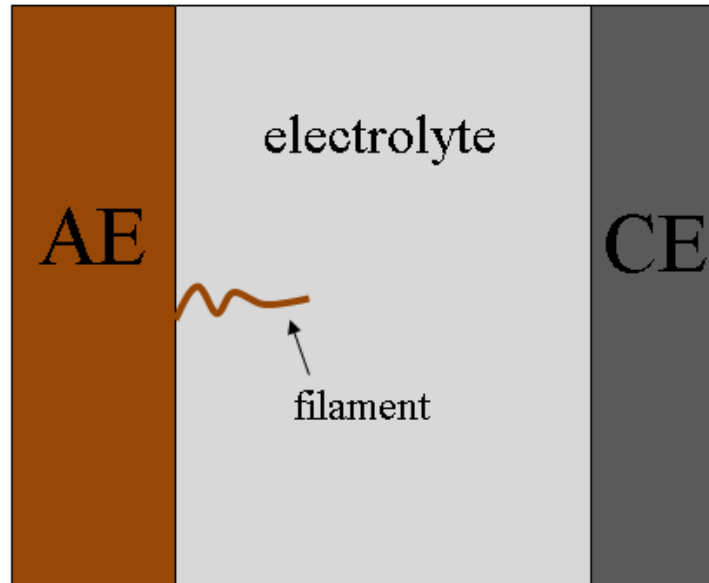


Figure 2.3: The structure of the ECM memory cell which consists of AE/electrolyte/CE.

#### 2.5.2.2 Types of resistive switching, bipolar vs unipolar

The resistive switching can be divided into two types depending on the electrical polarity required to respectively switch the device between its electrical states [14]. The high resistance low conductance electrical state is said to be the OFF state while the low resistance high conductance electrical state is the ON state. The SET voltage is defined by the voltage at which the device switches from its OFF state to ON state. The RESET voltage is the voltage at which the device switches from the ON to the OFF state [15].

The two types of RS are bipolar and unipolar resistive switching. The bipolar RS is when the SET and RESET voltages of the device happen at opposite polarities. On the other hand, the unipolar RS is when the SET and RESET voltages happen at the same polarity [12-15]. As shown in Figure 2.4 (a), in the bipolar RS mode the SET of the devices occurs at positive voltages while the RESET happens at negative voltages. On the other hand, the

SET and RESET of the devices occur at same polarity voltages in the unipolar RS mode as shown in Figure 2.4 (b).

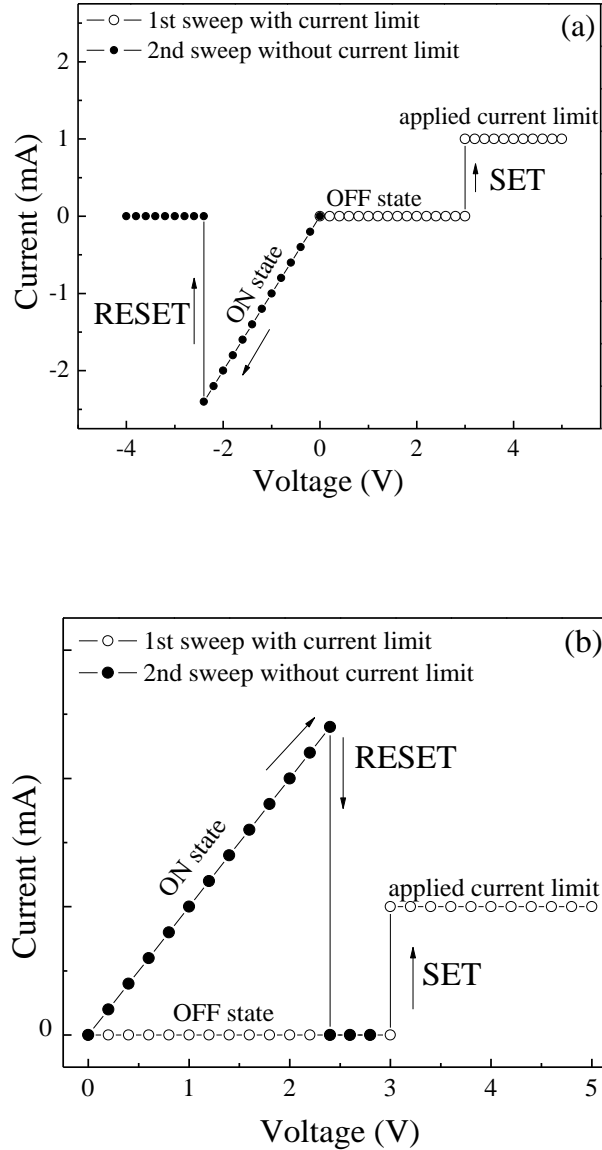


Figure 2.4: Typical I-V characteristics of RS in the (a) bipolar or (b) unipolar modes.

### 2.5.2.3 Resistive switching mechanism

The SET process in RS devices occurs upon the application of a positive bias on the active electrode which gets reduced to cations, migrates, oxidizes on the counter electrode and forms a metallic filament that “short-circuits” the electrolyte and switching the device to

its low-resistance ON state as shown in stage 1 in Figure 2.5. A current limit is applied to prevent the total damage and irreversible short-circuit of the electrolyte (stage 2 in Figure 2.5) [16-17]. The RESET process happens in the bipolar RS mode upon the application of a negative bias on the active electrode to reverse the process, leads to the electrochemical dissolution of the filament and turns back the device to its high-resistance OFF state (stage 3 and 4 in Figure 2.5) [12-17]. On the other hand, the RESET process happens in the unipolar RS mode due to a thermochemical mechanism where a fuse-antifuse process occurs upon the removal of the current limit and temperature increases due to high currents and rupture the filament Joules effect heating [12-17]. The unipolar RS appears more in devices that forms the filament due to the oxygen vacancies in metal-oxides electrolytes. The bipolar RS mode usually characterize in ECM devices structures where the metal acts as an active electrode.

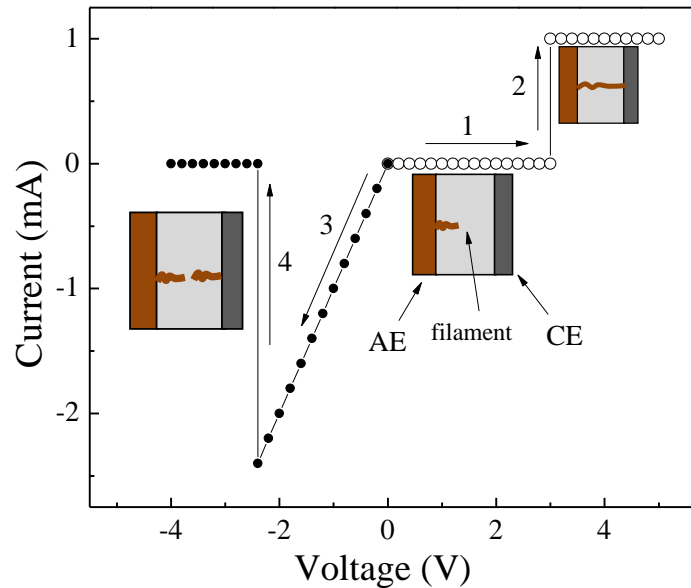


Figure 2.5: A schematic diagram of the filament formation and dissolution.

In ECM cells the active electrodes used are usually either Ag or Cu. Different structures using different solid electrolytes and different counter electrodes used Ag as an active electrode in an ECM memory structures. Examples of these structures are: GeS as an electrolyte with W as a counter electrode [18, 19], GeSe with W [20], Pt [21], or Ni [22],



GeTe with TiW [23], SiO<sub>2</sub> with Co [24], WO<sub>3</sub> with W [25], TiO<sub>2</sub> with Pt [26], ZrO<sub>2</sub> with Au [27] and solid polymer electrolyte with Pt [28]. Different combinations of materials reported for the electrolyte and counter electrode in the fabrication of reliable filamentary-based ECM [28]. The use of these materials was to lower the cost of the emerging memory technology.

On the other hand a combination of different electrolyte materials using different counter electrodes were combined with Cu as an active electrode to build the ECM memory. Examples of the structures that used Cu as an AE are: GeTe as an electrolyte with TaN as a counter electrode [29], Cu<sub>2</sub>S with Pt [20], Ta<sub>2</sub>O<sub>5</sub> with Pt [31] or Ru [32], SiO<sub>2</sub> with W [33], Pt or Ir [34] and P3HTPCBM with ITO [35]. In this investigation, AlO<sub>x</sub> based ECM memories will be fabricated, the detailed description of its structure and characterization will be presented in Chapter 6 section 2.

### **2.5.3 Embedded MIM**

#### **2.5.3.1 The structure of embedded MIM devices**

One of the simplest structures in electronics is the metal-insulator-metal stack, consists of a capacitor with the insulator acting as the dielectric layer (Figure 2.6 (a)). It is the building block of many electronic devices. Recently, embedded MIM structure was investigated as a 2-dimensional (2D) novel, low cost and high speed NVMs [6-9]. This is done through doping the insulator of the embedded MIM structure with charge traps. The embedment of the charge traps will result in the resistive switching and the memory characteristics of the structure. Thus the structure of the embedded MIM memory devices is similar to that of the capacitor but having charges traps doped in the insulator and sandwiched between two metal electrodes as shown in Figure 2.6 (b). In our research, we investigate the potentials of embedded MIM structures as organic nonvolatile memory device, using carbon nanotubes as traps doped in the organic insulator.

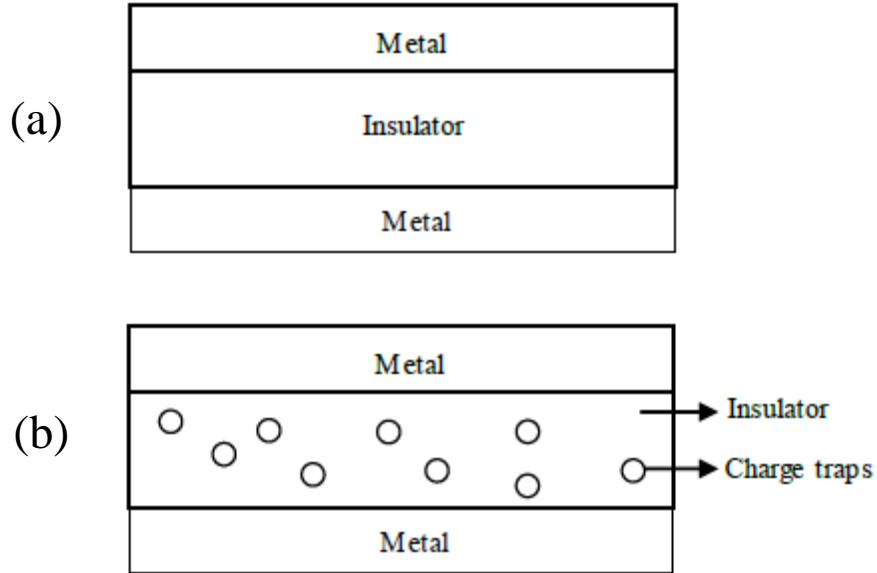


Figure 2.6: The structure of an MIM device (a) without embedded charge traps and (b) the same structure with embedded charge traps inside its insulator.

### 2.5.3.2 Current-voltage characteristics and memory application

Embedded organic MIM memory devices are resistive type memories where the two states (ON and OFF) are defined by two resistive values. The memory behavior of the devices is shown by the switching in the I-V characteristics between two resistive states; ON and OFF states. Typical I-V characteristics of embedded MIM memory devices exhibiting RS behavior upon application of opposite voltages are shown in Figure 2.7. Upon sweeping the bias on the device and if the device is initially in the OFF state (stage 1 in Figure 2.7), at a certain voltage (1.2 V in Figure 2.7) the device current will increase abruptly and thus switch to ON state (stage 2 in Figure 2.7), that voltage is called the writing voltage. In the example shown in Figure 2.7, the switching to the ON state happens at 1.2 V. The device stays in the ON state as shown in stages 3, 4, 5 and 6 in Figure 2.7. Upon sweeping in the opposite direction at a certain voltage the current will abruptly go back to its initial values (OFF state), this is called the erase voltage which is -0.8 V and occurs at stage 7 in Figure 2.7. At any voltage between the writing and the erase voltages, the device can exhibit both states ON or OFF (depending on the previously applied voltage) and thus the range of voltages between the write and erase voltages may be used as the read voltage (between -

0.8 V and 1.2 V in Figure 2.7). Usually the read voltage is chosen at the highest ON/OFF ratio to be able to easily distinguish between the different states.

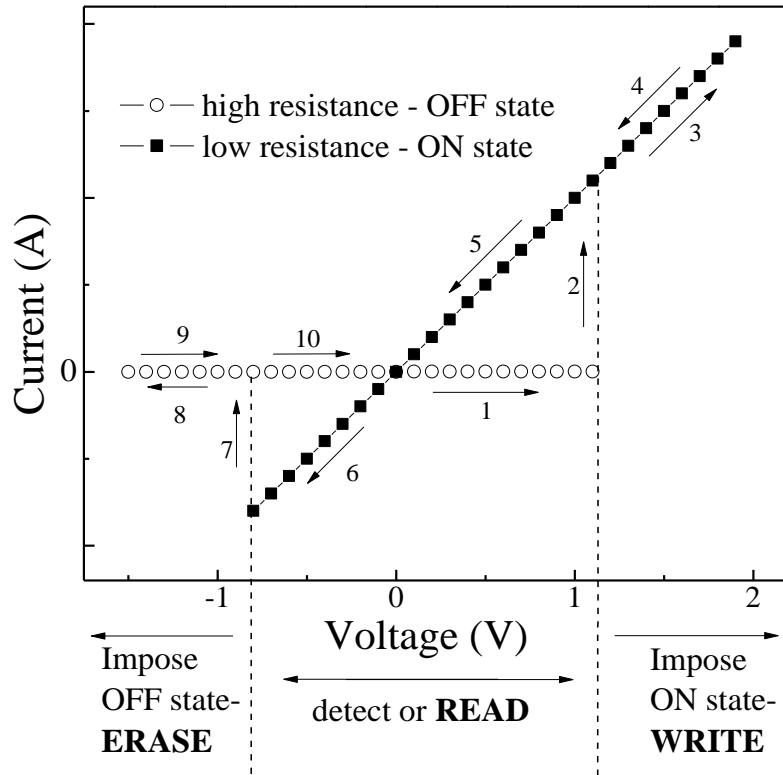


Figure 2.7: Typical I-V characteristics of embedded MIM memory devices exhibiting RS behavior.

Different organic embedded MIM memory structures have been reported to exhibit RS upon the doping of different organic insulators with different types of charge traps. Examples of these organic embedded structures are PCBM blended in PMMA [36], FeS<sub>2</sub> blended in P3HT [37], ZnO embedded in PMMA [38], Au-DT blended with P3HT, CuPC, Cr, Ag, Mg, Al embedded inside Alq<sub>3</sub> and graphene embedded between two layers of PMMA [39]. In this investigation an organic embedded MIM structure using layer-by-layer deposited single walled carbon nanotubes (SWCNTs) as charge trapped doped between two PMMA insulators. SWCNTs unlike other small organic molecules exhibit chemical inertness, stability and tunable band gap which make them favorable for such

application [40, 41]. The chemical inertness and stability enhances SWCNTs lifetime inside the organic compound without changing the chemical or physical states [40]. The tunable bandgap of SWCNTs results in specifying its desired electrical characteristics, i.e. the ratio of the metallic to semiconducting SWCNTs embedded in the structure can be controlled [41]. A detailed description of the fabricated SWCNT-based MIM will be presented in Section 5.3.2.

## **2.6 Capacitance-based NVM**

One of the most important structures in the electronics is the metal-insulator-semiconductor stack. It is the building block of the mostly-used well-known metal-oxide-semiconductor-field-effect-transistor (MOSFET), which is in turn the most widely utilized in computers and digital hardware. Recently, MIS structure was investigated as a novel, low cost and high speed NVMs [42]. In our research, we investigated the potentials of the MIS structure as an organic memory device, using carbon nanotubes as the charge element.

### **2.6.1 Metal-Insulator-Semiconductor Capacitor**

The MIS stack is depicted in Figure 2.8, it consists of a semiconductor connected externally through an ohmic contact, an insulator layer (dielectric material), and a metal layer called “the control gate” deposited on the insulator layer. The main purpose of the insulating layer in the MIS capacitor is to inhibit a current flow from the metal gate to the semiconductor beneath, and thus maintain a capacitance structure.

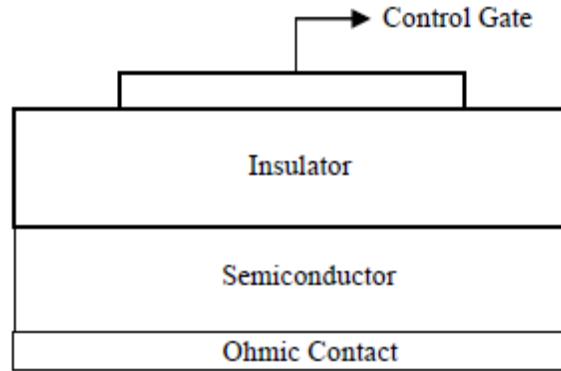


Figure 2.8: Metal-Insulator-Semiconductor Capacitance.

The main challenge in growing a reliable MIS structure is the quality of the insulator-semiconductor interface. A high quality interface is one that has the minimum number of interface state density, i.e. has the minimum number of traps in the bandgap at the insulator-semiconductor interface. It is worthy to mention that the success of the Si electronic market is due to the nearly ideal interface that can be obtained between silicon and silicon dioxide ( $\text{SiO}_2$ ) [43, 44], unlike most of other semiconductors where it is very hard to achieve such high quality semiconductor-insulator interfaces.

### 2.6.2 Band structure and the flat band voltage

To understand the performance of MIS capacitor, we consider first an ideal case where no interface states are present. The band diagram of the individually separated metal, insulator, and a p-type semiconductor is presented in Figure 2.9. As shown in Figure 2.9 the Fermi level of the metal (unlike semiconductors and insulators) lies in an allowed band, and the bandgap of the an insulator is much larger than that of the semiconductor. The two main parameters that mostly concern our application are the misalignment of the Fermi levels and that the metal work function is greater than that of the semiconductor. This will affect the band structure of the MIS stack and lead to remarkable electronic features of the MIS stack.

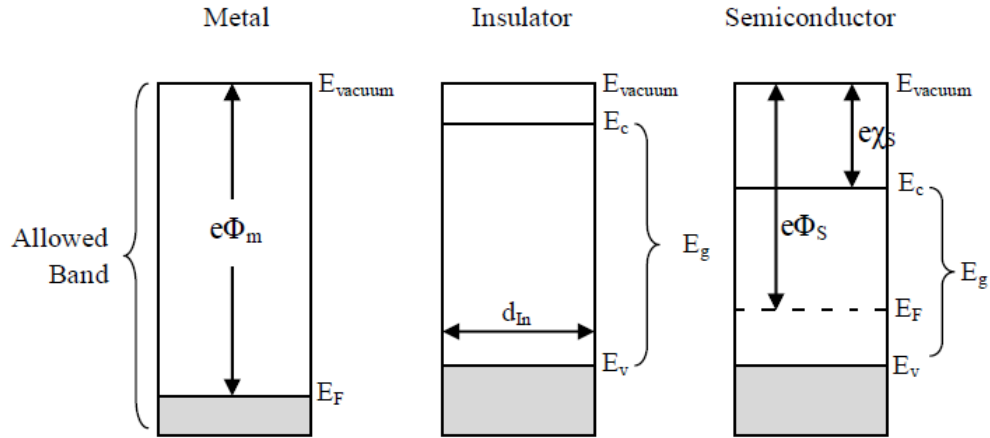


Figure 2.9: Separate band structures of a metal, an insulator, and a p-type semiconductor.

When the three materials (M, I, and S) come to contact to form the MIS structure, modifications on the band structure of the stack occur which lead to the formation of MIS capacitor where its capacitance is controlled by the applied voltage on the metal. The Fermi level ( $E_F$ ) of the semiconductor is the chemical potential of the material, i.e. it tells us the level of carriers in the material. In an intrinsic semiconductor for example, the  $E_F$  lies in the midgap region (equal numbers of holes and electrons), when the semiconductor is p-doped the  $E_F$  shifts toward the valence band ( $E_v$ ) implying the presence of more holes, when it is n-type doped  $E_F$  shifts toward the conduction band ( $E_c$ ) implying the presence of more electrons. Under no bias, the Fermi levels of different materials in any stack should align, due to chemical stability, so that no gradient exist. Moreover, in the MIS structure the conduction band of the semiconductor is at a lower level than that of the insulator. Therefore the semiconductor band structure will bend in a way that satisfies the alignment of the Fermi levels and the continuity of the conduction level. The band bending of MIS stack consisting of a p-type semiconductor is illustrated in Figure 2.10.

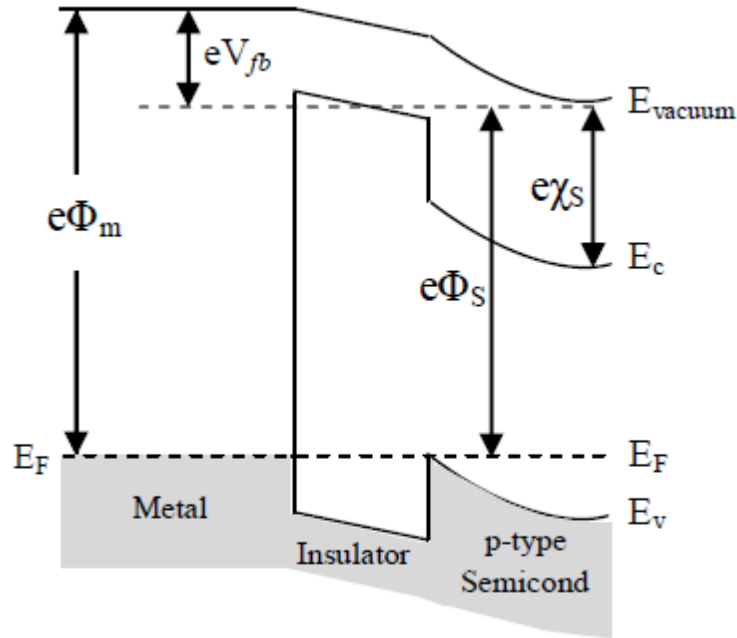


Figure 2.10: Band structure of the MIS capacitor.

The semiconductor band-bending is determined by the difference of the metal work function ( $\Phi_m$ ) and the semiconductor work function ( $\Phi_s$ ). The external voltage needed to remove this band bending and reach a flat band condition is called the flat band voltage ( $V_{fb}$ ) and is given by Eq. 2.1:

$$eV_{fb} = e\Phi_m - e\Phi_s \quad (2.1)$$

where  $e$  is the electron charge. The flat band voltage is a very important parameter in the MIS capacitor, and the shift in this voltage ( $\Delta V_{fb}$ ), as will be shown later, is an important parameter in the memory effects of MIS-based memories.

### 2.6.3 Different biasing regimes

The importance of MIS structure is the dependence of capacitance on the voltage applied to the metal gate. This happens due to the semiconductor band-bending at the insulator-semiconductor interface and results in three regimes of biasing: accumulation, depletion, and inversion. In the inversion regime the p-type semiconductor will behave as an n-type

due to the carrier concentration change as an effect of the applied voltage. The three regimes are described below in details for a MIS structure having a p-type semiconductor [43, 44].

#### **2.6.3.1 Accumulation Regime:**

Accumulation occurs when a negative bias is applied to the metal gate with respect to the semiconductor; i.e.  $V_{GS} < 0$ . Electrons are injected to the metal resulting in a band-bending of the valence band to come closer to the Fermi level. The schematic diagram of the band bending is shown in Figure 2.11 (a). As a result of band bending, an equal number of holes accumulate at the semiconductor near the insulator interface.

#### **2.6.3.2 Depletion Regime:**

As can be inferred from its name, the region of the semiconductor near the insulator is depleted from carriers. This happens when a positive voltage is applied to the gate with respect to the semiconductor ( $V_{GS} > 0$ ), this induces a band bending as depicted in Figure 2.11 (b). The conduction band will bend towards Fermi level while the valence band will bend away, to reach a region where the Fermi level is at the midgap, which is the same case in intrinsic (undoped) semiconductors. So in depletion region the semiconductor “loses” its p-type doping and is more like an intrinsic one.

#### **2.6.3.3 Inversion Regime**

In Inversion regime, the p-type of the semiconductor will be inverted to an n-type. This occurs when the applied voltage in the depletion region is increased further ( $V_{GS} \gg 0$ ) to an extent that the conduction and valence bands bend in a way that makes the  $E_F$  more closer to the conduction band than the valence band as shown in Figure 2.11 (c). In this case the semiconductor loses its intrinsic behavior and start to have an n-type behavior.



The modification in the semiconductor status in the three regimes between p-type, intrinsic and n-type is the reason for the voltage dependence of the MIS capacitance.

#### **2.6.4 The threshold voltage:**

The inversion regime is of high interest in memory devices, as the capacitance in this region depends on the frequency and the rate of scan. The voltage needed at which inversion occurs in the semiconductor is called the threshold voltage ( $V_T$ ). A quantitative analysis of the inversion region is needed to understand the parameters that control  $V_T$  [43,44].

Figure 2.12 gives a more detailed scheme of the band-bending of an MIS structure based on p-type semiconductor. The quantity  $e\Phi_F$  is the difference between intrinsic Fermi level ( $E_{Fi}$ ) and the bulk Fermi level ( $E_F$ ) in the neutral region:

$$e\Phi_F = E_{Fi} - E_F \quad (2.2)$$

Thus for a p-type semiconductor,  $e\Phi_F$  is positive; while for an n-type it is negative. So we can describe the band bending by the quantity  $e\Phi_F$ , and the surface band bending  $eV_S$ . Simple conditions involving  $e\Phi_F$  and  $eV_S$  can be generated for different applied biases:

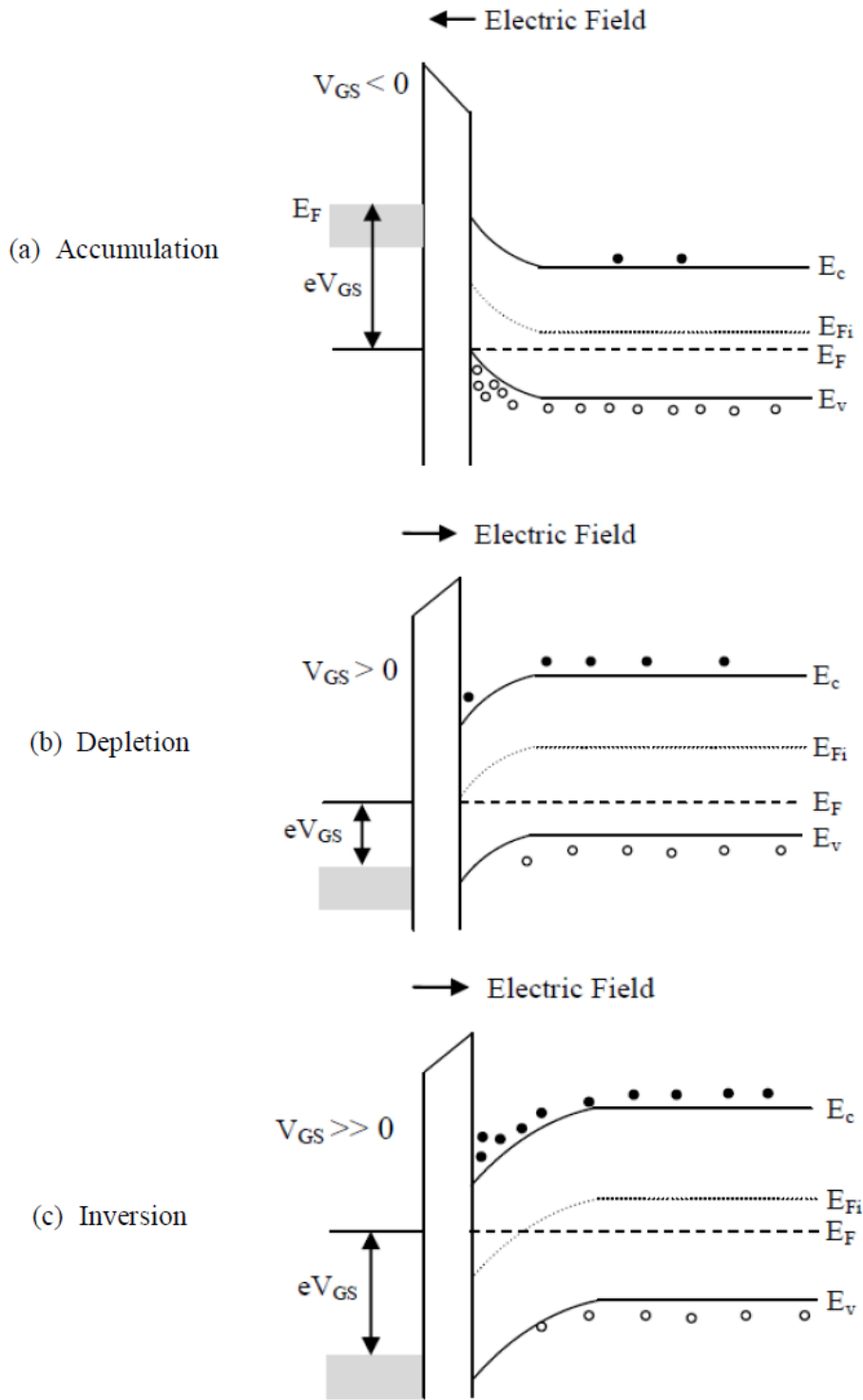


Figure 2.11: Band structure of MIS structure in three different regimes: (a) Accumulation, (b) Depletion, (c) Inversion.

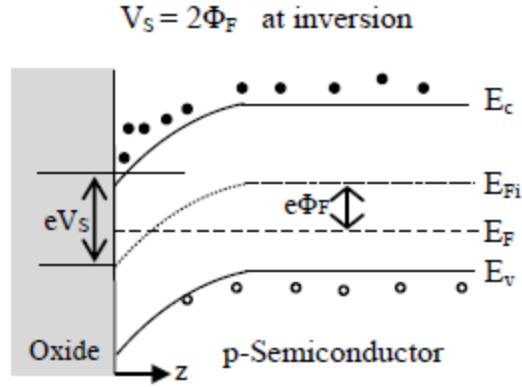


Figure 2.12: Band-bending and surface potential at inversion.

- At flat band voltage:  $eV_S = 0$ .
- In depletion regime:  $eV_S > 0$ .
- After inversion:  $eV_S > 0$  and  $eV_S > e\Phi_F$ .

A strong inversion can be reached when the electron concentration at the interface equals the holes concentration in the bulk semiconductor; in other words when the ‘strength’ of the n-type at the interface equals the p-type ‘strength’ in the bulk. This happens when the band-bending is induced by a sufficient voltage [43, 44]:

$$V_S(\text{inv}) = -2\Phi_F \quad (2.3)$$

The negative sign exists in either p-type or n-type, because in both cases the signs of  $V_S$  and  $\Phi_F$  are opposite. Using Boltzmann statistics [43, 44]:

$$\Phi_F = -\frac{K_B T}{e} \ln\left(\frac{p}{n_i}\right) \sim -\frac{K_B T}{e} \ln\left(\frac{N_a}{n_i}\right) \quad (2.4)$$

Where  $K_B$  is boltzman constant,  $T$  is the temperature,  $p$  is the holes concentration,  $n_i$  is the intrinsic carriers concentration and  $N_a$  is the acceptors concentration. The surface bending using strong inversion criterion becomes [43, 44]:

$$V_S(\text{inv}) = -2\Phi_F = -2\frac{K_B T}{e} \ln\left(\frac{N_a}{n_i}\right) \quad (2.5)$$

We are interested in calculating  $V_T$ , the voltage needed to make inversion in the semiconductor; to do that we have to calculate the charges at the semiconductor/insulator interface and relate them to the externally applied voltage using Poisson equation.

Surface charge density and surface field can be related using Gauss's law [43, 44]:

$$|Q_S| = \epsilon_S |E_S| \quad (2.6)$$

Where  $Q_S$  is the total surface charge density at the semiconductor/insulator interface,  $\epsilon_S$  is the permittivity of the semiconductor, and  $E_S$  is the applied electric field at the surface. Indeed  $Q_S$  goes to zero as applied voltage approaches  $V_{fb}$ . Using continuity equations [43, 44]:

$$\epsilon_S E_S = \epsilon_{ins} E_{ins} \quad (2.7)$$

Where  $\epsilon_{ins}$  is the insulator permittivity, and  $E_{ins}$  is the Electric field in insulator at interface. The applied gate voltage ( $V_{GS}$ ) is simply the sum of the flatband voltage ( $V_{fb}$ ), insulator voltage ( $V_{ins}$ ), and interface potential ( $V_S$ ):

$$V_{GS} = V_{fb} + V_{ins} + V_S \quad (2.8)$$

But:

$$V_{ins} = d_{ins} E_{ins} = \frac{d_{ins} \epsilon_S E_S}{\epsilon_{ins}} = \frac{\epsilon_S E_S}{C_{ins}} \quad (2.9)$$

Where  $d_{ins}$  is the insulator thickness and  $C_{ins}$  is the capacitance per unit area of the insulator; thus

$$V_{GS} = V_{fb} + V_S + \frac{\epsilon_S E_S}{C_{ins}} = V_{fb} + V_S + \frac{Q_S}{C_{ins}} \quad (2.10)$$

This equation is very important as it relates the charges at the interface to the applied voltage, it can be used to get the threshold voltage and to study the capacitance of the MIS structure.

As mentioned before, the threshold voltage is the voltage at which the inversion starts, thus at this voltage the charges at the interface are depletion charges:

$$Q = N_a W \quad (2.11)$$

Where  $W$  is the depletion width given by [43, 44]:

$$W = \left[ \frac{2\epsilon_S |V_S|}{eN_a} \right]^{\frac{1}{2}} \quad (2.12)$$

Using Eq. (2.12) we get:

$$Q_S = eN_a W = (2\epsilon_S eN_a |V_S|)^{1/2} = (4\epsilon_S eN_a |\Phi_F|)^{1/2} \quad (2.13)$$

The threshold voltage can be thought to be the  $V_{GS}$  at the condition  $V_S = -2\Phi_F$  and the  $Q_S$  given by Eq. (2.13). To get  $V_T$ , we substitute in Eq. (2.10) the two conditions, i.e. Eq.(2.3) and Eq.(2.13); and therefore:

$$V_T = V_{fb} - 2\Phi_F + (4\epsilon_S N_a |\Phi_F|)^{1/2} \frac{1}{C_{ins}} \quad (2.14)$$

When inversion is satisfied, the density of electrons induced inhibits any further increasing of the depletion width; thus the maximum depletion width is given by Eq. (2.12) provided that  $V_S = -2\Phi_F$ ; and therefore:

$$W_{max} = \left[ \frac{4\epsilon_S |\Phi_F|}{eN_a} \right]^{\frac{1}{2}} \quad (2.15)$$

### 2.6.5 MIS capacitance-voltage characteristics:

In the previous section we described the basics of the MIS structure and derived the basic relations between the charge density and the voltage applied. The utilization of MIS devices in memory applications and transistors is due to voltage-dependent capacitance. C-V characteristic is obtained by applying a dc voltage ( $V$ ) to the metal gate, plus a very small ac signal, around 5mV, to extract the capacitance at the applied bias.

The equivalent circuit of the MIS structure consists of two capacitors in series, one representing the insulator ( $C_{Ins}$ ) and the other representing the semiconductor ( $C_S$ ) (Figure 2.13).

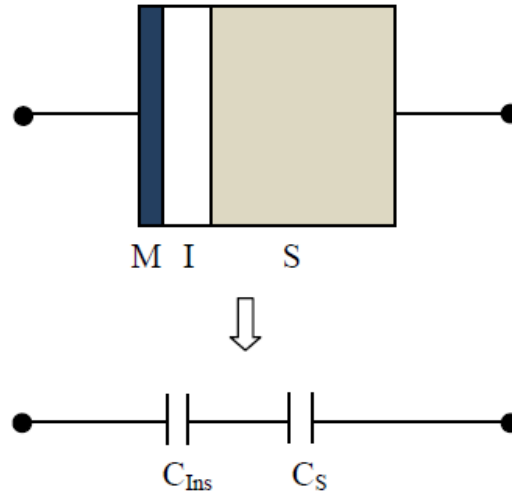


Figure 2.13: The MIS equivalent circuit.

The capacitance per unit area of the MIS ( $C_{MIS}$ ) structure is a series summation of  $C_{Ins}$  and  $C_S$ :

$$C_{MIS} = \frac{C_{Ins}C_S}{C_{Ins} + C_S} \quad (2.16)$$

Where  $C_S = dQ_S/dV_S$ ; as discussed in the previous section, the capacitance is dependent on the voltage applied and thus the three regimes (accumulation, depletion, and inversion) are reflected in the C-V curve [43, 44].

### 2.6.5.1 Capacitance in accumulation

In accumulation ( $V_{GS} < 0$ ):  $C_S$  is much larger than  $C_{Ins}$ , this is due to the accumulation of the holes near the surface and a little change in the applied voltage induces a large change in the carrier concentration, thus

$$C_{MIS} \cong C_{Ins} = \frac{\epsilon_{Ins}}{d_{Ins}} \quad (2.17)$$

### 2.6.5.2 Capacitance in depletion

When depletion region is reached ( $V_{GS} > 0$ ): a depletion capacitance ( $C_{dep}$ ) is introduced, and it depends on the depletion width,  $C_{dep} = \epsilon_S/W$ , thus using eq. 2.17

$$C_{MIS} = \frac{C_{Ins}}{1 + \frac{C_{Ins}}{C_S}} = \frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins}W}{\epsilon_S}} \quad (2.18)$$

As the applied voltage increase, the depletion width increase, as discussed before, and thus the capacitance decrease.

### 2.6.5.3 Capacitance in the inversion regime

In the inversion regime ( $V_{GS} \gg 0$ ): at the end of the depletion region, the depletion width reaches its maximum ( $W_{Max}$ ) and the capacitance reaches its minimum, with  $W=W_{Max}$ . At the minimum capacitance point, no carrier density exists. When the applied voltage is further increased ( $V_{GS} \gg 0$ ), electrons start to accumulate at the interface, this does not happen instantaneously, it happens through electron-hole generation or through diffusion from the bulk semiconductor, thus the accumulation of the electrons needs time. Therefore the C-V characteristics of MIS structure in the inversion regime are dependent on the scanning frequency. This introduces two cases:

**(i) Low frequency case:**

If the variation is slow, electrons accumulate at the interface and the depletion width is maintained at  $W_{Max}$ , thus any little change in applied voltage, a significant change in electron density is induced, using  $C_s = dQ_s/dV_s$ , the MIS capacitance is back to the insulator capacitance:

$$C_{MIS} \cong C_{Ins} = \frac{\epsilon_{Ins}}{d_{Ins}} \quad (2.19)$$

Slow variation allows all this to be detected and the capacitance will increase again as voltage is further increased. This happens at low frequencies of approximately 1Hz and below [43].

**(ii) High frequency case:**

If the variation is fast, the semiconductor capacitance will not contribute to the MIS capacitance which will be dominated by the depletion capacitance, i.e. stays at its minimum capacitance,  $C_{min}$ , and probably decrease even more. A frequency of 1KHz and above will be sufficient to inhibit the increase of the capacitance.

The different operating regimes of the MIS structure are illustrated in the C-V characteristics (Figure 2.14) under different biasing conditions and under low and high frequency scanning conditions.

As discussed before, the shift in flatband voltage is critical in the MIS-based memory devices, thus the capacitance at this voltage is also important and it can be derived in the same manner as above to reach:

$$C_{MIS}(fb) = \frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins}}{\epsilon_S} \sqrt{\frac{K_B T}{e} \frac{\epsilon_S}{e N_a}}} \quad (2.20)$$



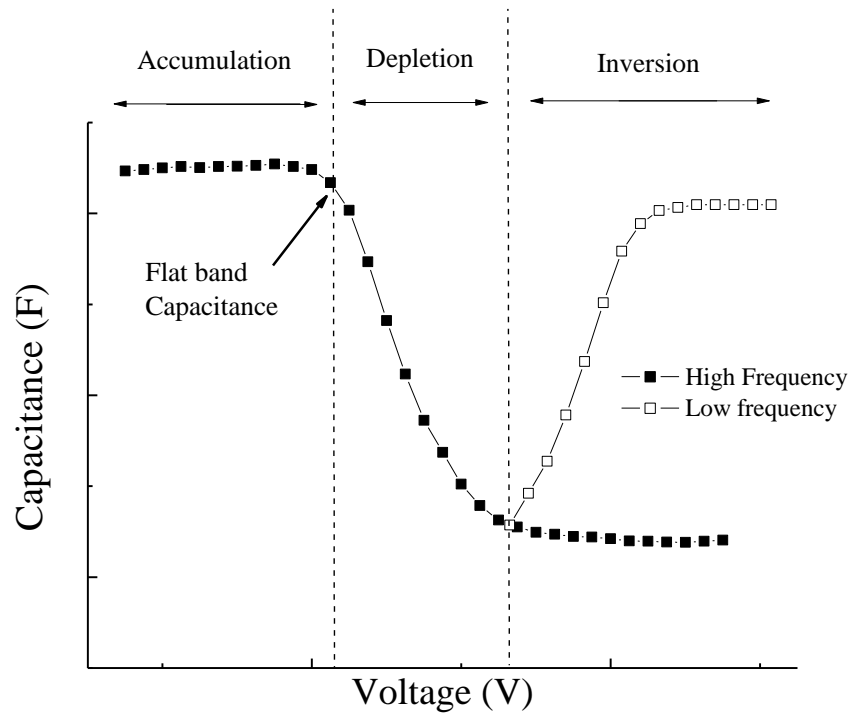


Figure 2.14: C-V characteristics under different applied bias and under low and high frequencies.

### 2.6.6 Organic MIS structure

The organic MIS structure is a stack fabricated using organic materials, i.e. organic insulators and semiconductors. The main difference between the silicon-based MIS structures and the organic based MIS structure is the frequency response of the capacitance of the stack in the inversion regime. Actually in the organic-based MIS structures no inversion occurs. Instead a deep depletion occurs and this is due to the very slow response time  $\sim 10^7$  sec in organic semiconductors [45,46]. Unlike silicon, organic semiconductors have low intrinsic carrier density and even at very low frequencies (mHz) the inversion is not observable in the organic MIS stack. A deep depletion will occur in the organic MIS stack and there is no frequency dependence on the value of the capacitance in the inversion regime. An example of C-V characteristics showing the capacitance in deep depletion of the organic MIS stack is shown in Figure 2.15. Although this difference exists between the silicon-based and the organic-based MIS structures, but in our application of the organic

memory MIS structure this will not be an issue. The devices are all characterized at high frequencies to show the memory effect and the charging and discharging of the embedded floating gate.

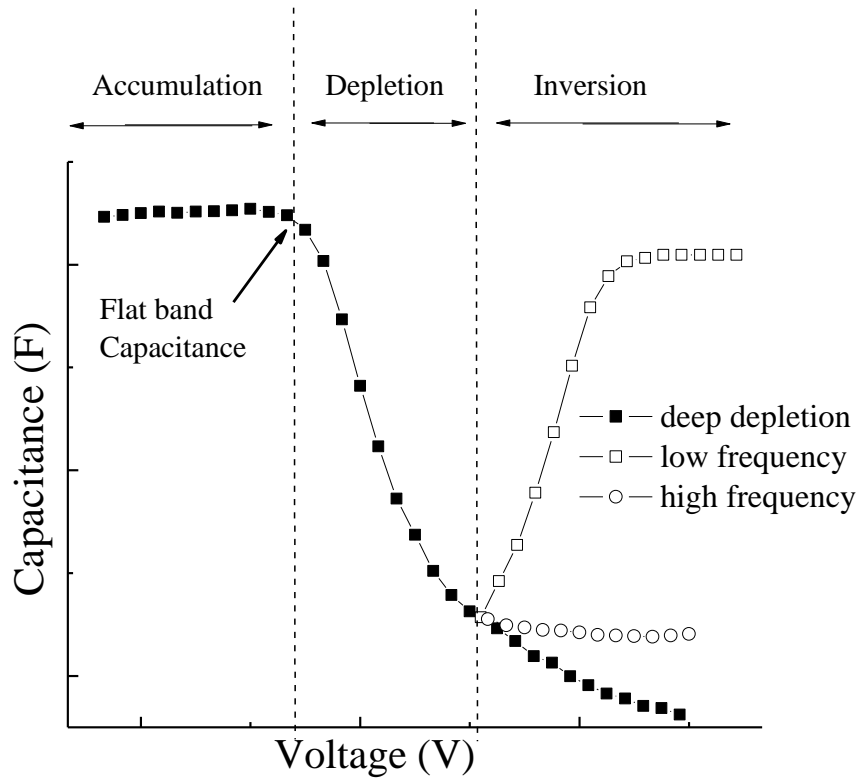


Figure 2.15: C-V characteristics under different applied bias and under low and high frequencies.

### 2.6.7 Memory application of the MIS structure

The Memory application of MIS stack comes from the non-ideality of the above presented structure. Until now the described MIS structure is ideal, i.e. there is no trap present. The non-ideality of the MIS stack can be described in two kinds of traps; interface traps at the I/S interface, or fixed traps inside the dielectric layer. The later non-ideality is the one that we benefit from in memory applications, while the first one is just a hindering agent to our memory device. Both kinds of non-ideality and their effects on the C-V characteristics of the device are presented below.

### 2.6.7.1 Interface states non-ideality:

The non-ideality comes from the existence of traps at the interface between the insulator and the semiconductor, these traps give rise to a density of states at the interface in the bandgap region. The density of these interface states depends on the growth technique and conditions [43, 44, 47]. The effect of the interface states on the C-V characteristics is illustrated in Figure 2.15. Carriers can move in and out of these states, when the interface

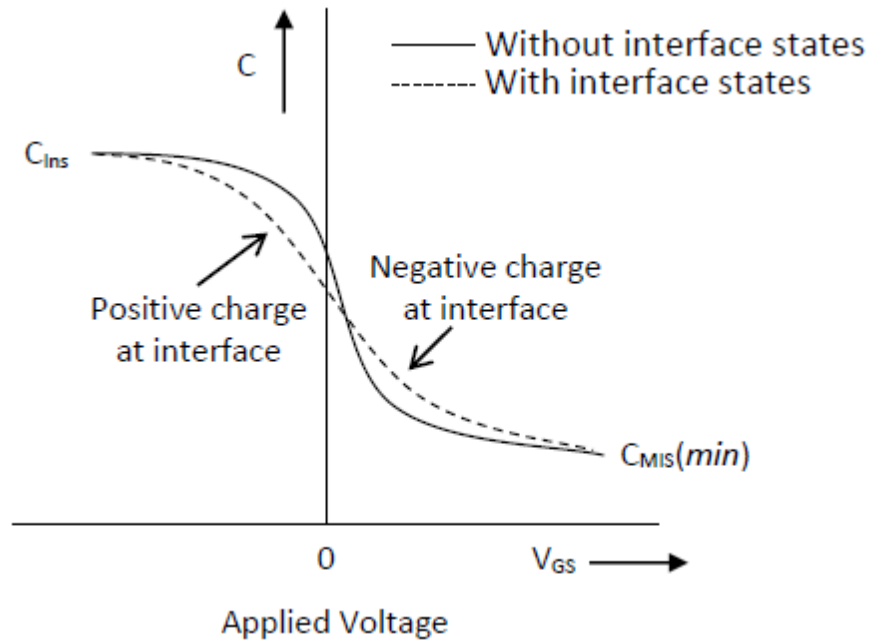


Figure 2.16: Effect of interface states on the C-V characteristics.

states are positive (negative), the C-V curve in the negative-bias (positive-bias) regime bends in the way shown in Figure 2.16. The extremely ideal case is when the curve looks like a step function, these interface states changes the slope of curve bending and makes it more shallow. This kind of non-ideality hinders the performance of the device, and it cannot be utilized in any application.

### 2.6.7.2 Fixed dielectric traps non-ideality:

Unlike interface states, the fixed insulator states can be utilized for memory applications of the simple MIS structure. Introducing fixed traps in the insulating layer results in a hysteresis in the C-V characteristics of the structure and thus a memory effect [48]. When a floating gate is introduced, a modification on the MIS structure is introduced and the insulating layer will be split into three regions named tunnel insulation layer, floating gate and control insulation layer. Other names of the three layers can be found in the literature [40-42]. The modified MIS structure after introducing the floating gate is depicted in Figure 2.17.

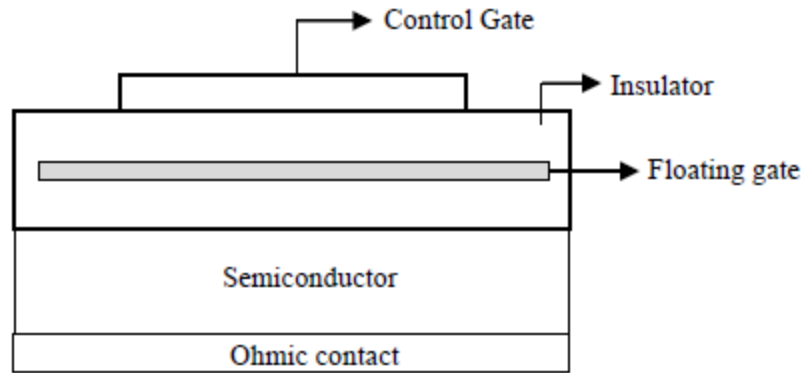


Figure 2.17: Modified MIS structure embedded with a floating gate used in memory applications.

### 2.6.7.3 Charges trapping:

Fixed traps in the insulating layer causes voltage drop due to the fixed charges that will be induced upon applying bias to the structure [48]. The voltage drop will be [48]:

$$\Delta V = \frac{-Q_{ss}}{C_{ins}} \quad (2.21)$$

Where  $Q_{ss}$  is the insulator fixed charge density ( $\text{cm}^{-2}$ ), independent of the applied voltage. Thus the induced fixed charges in the insulating layer cause the entire C-V curve to shift either to the right or to the left, depending on the kind of carriers injected or from where they are injected [49]. In other words, a double sweep of the voltage, forward and backward

(from accumulation to inversion or vice versa) will result in a hysteresis loop in the C-V characteristics of the MIS structure.

#### **2.6.7.4 Hysteresis in the C-V characteristics and the WRITE-READ-ERASE processes:**

MIS memory devices are capacitive type memories where the two states (ON and OFF) are defined by two capacitive values [43-50]. The C-V characteristic of a simple p-type MIS structure is shown Figure 2.18 (a); no hysteresis observed upon the double bias sweep. On the other hand, in the embedded MIS memory devices the C-V characteristics exhibit a clear hysteresis upon the double bias sweep (Figure 2.18 (b)). If we define the high accumulation capacitance by the ON state and the low deep-depletion capacitance by the OFF state, the hysteresis enables us to use the device as a memory device as it was defined in Section 2.2.

As shown in Figure 2.18 (b), if we apply a certain voltage (less than -7.5 V) we impose on the device to be in its high accumulation capacitance and thus perform the WRITE operation of the ON state. On the other hand if we apply another voltage (higher than 10 V) we impose on the device to be in its low deep-depletion capacitance thus perform the ERASE operation and have the device in its OFF state. At a certain range of voltages (between -7.5 V and 10 V) the hysteresis in the C-V characteristics enabled both states, the ON and the OFF states, to co-exist. An application of a voltage this range and reading the corresponding capacitance can sense in which state is the device without changing it. The sensing of the device state through reading the capacitance without changing it is the READ operation of the memory device. As such the WRITE-READ-ERASE operations of a nonvolatile memory device can be performed on an embedded MIS structure with hysteresis in its C-V characteristics.

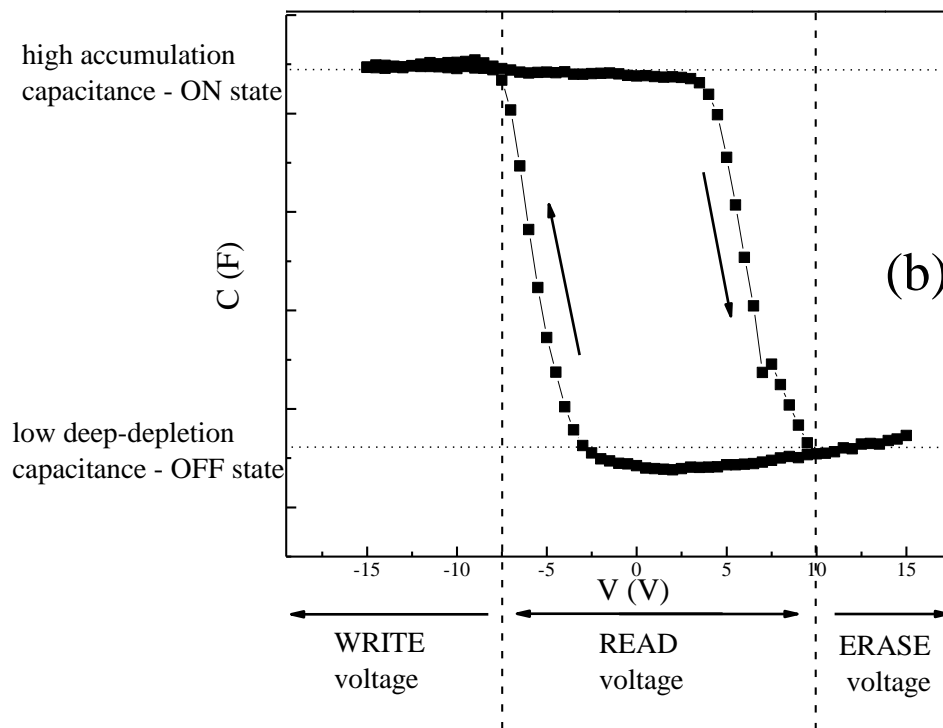
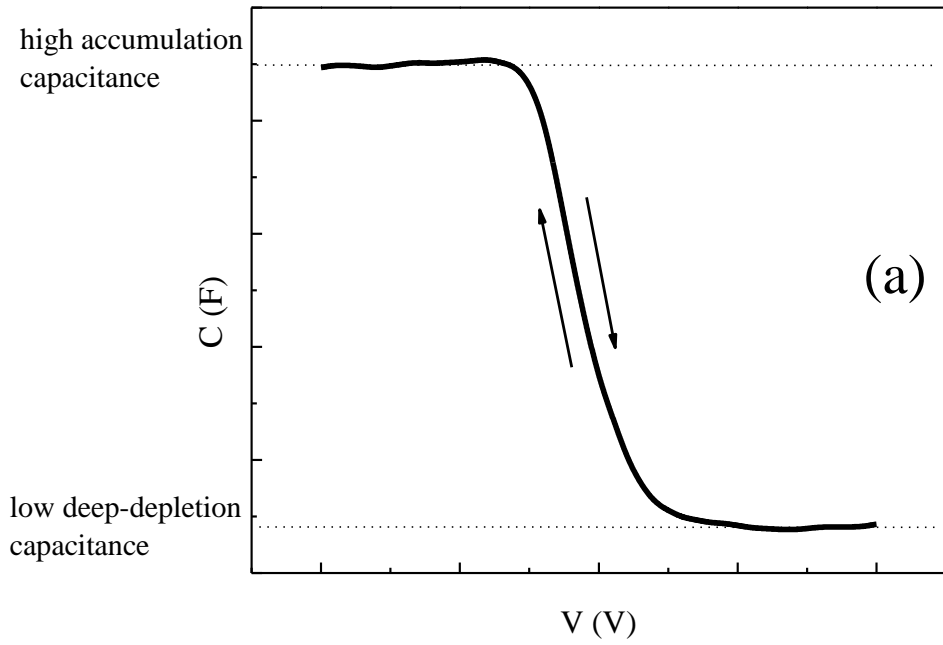


Figure 2.18: (a) typical C-V characteristics of a simple p-type MIS structure (b) Hysteresis in the C-V characteristics of an embedded MIS structure.

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## Chapter 3

### Materials and Experimental details

#### 3.1. Introduction

In this study, three different types of two terminal nonvolatile memory (2T-NVM) devices were fabricated and studied. In the first two types, organic embedded metal-insulator-semiconductor (MIS) and organic embedded metal-insulator-metal (MIM) memories, with single-walled carbon nanotubes (SWCNTs) as a floating gate or charge storage elements were investigated. The third type is a filamentary based MIM memory in the electrochemical metallization structure using  $\text{AlO}_x$  as a resistive switching medium. SWCNTs and the organic materials used in this study are introduced in section 3.2. The experimental techniques used in this investigation are introduced in section 3.3. The layer-by-layer deposition technique of SWCNTs which is a main part of the work is explained in details in section 3.3.1, while the other conventional thin film deposition techniques are briefly introduced in section 3.3.2. The fabrication procedure of the three different types of devices are shown in section 3.3.4. The characterization of the devices in terms of surface morphology, AC measurements and DC measurements are explained in sections 3.5.1 to 3.5.3, respectively.

#### 3.2. Materials

##### 3.2.1 Carbon nanotubes

Carbon nanotubes (CNTs) are graphene flakes rolled up in a cylindrical nanostructure. They were discovered in NEC Corporation in 1991 by Iijima [1, 2]. CNTs can be single-walled carbon nanotubes (SWCNTs) or multi-walled carbon nanotubes (MWCNTs) depending on the number of layers of graphene rolled in each cylindrical nanostructure. SWCNTs consist of a monolayer of graphene flake rolled in a cylindrical shape while MWCNTs consist of a roll of multilayer flakes as shown in Figure 3.1. SWCNTs diameter

can range between 0.8 nm to 2 nm while the diameter of MWCNTs ranges between 5 to 20 nm, although can exceed 100 nm in some cases. On the other hand, CNTs length may

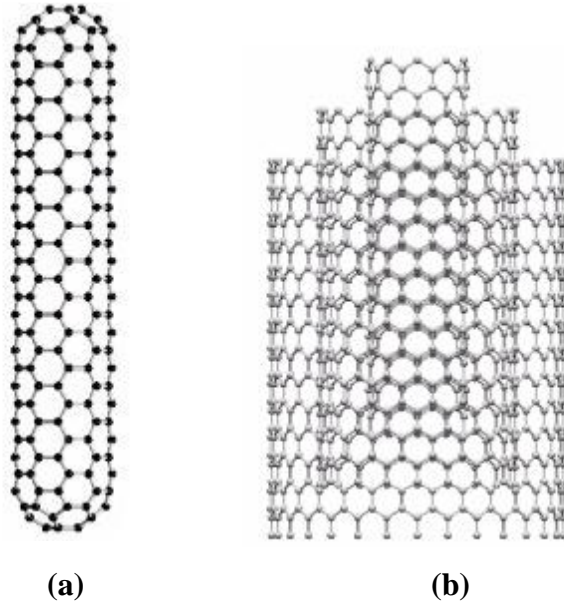


Figure 3.1: (a) SWCNTs and (b) MWCNTs cylindrical nanostructures [3].

vary depending on the growth conditions, it may be less than 100 nm or several centimeters[1, 2].

The SWCNT properties are determined by the diameter of the nanotube and by rolling angle of the graphene sheet. For example the rolling angle of the SWCNT may alter the band structure of the SWCNT and may determine if the SWCNT is of a semiconductor or of a metallic nature [4, 5]. The wrapping of the SWCNTs is determined by its chiral vector  $\text{Ch}$  [5]; where:

$$\text{Ch} = n\mathbf{a}_1 + m\mathbf{a}_2 \tag{3.1}$$

where the indices  $n$  and  $m$  are the number of unit vectors ( $\mathbf{a}_1$  and  $\mathbf{a}_2$ ) in the honeycomb structure of the graphene sheet along two directions as shown in Figure 3.2. For instance,

the nanotube is referred to as a zigzag nanotube if  $m = 0$ . While the nanotube is called an armchair nanotube if  $n = m$  [1-5].

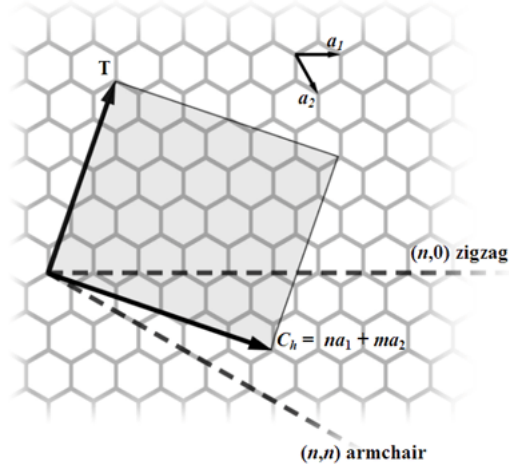


Figure 3.2: The chiral vector (Ch) naming in the honeycomb graphene sheet of SWCNT depending on the  $n$  and  $m$  indices [6].

SWCNTs have been used in various applications in microelectronics [1]. Their low electron scattering and tunable bandgap made them attractive for field effect transistors (FET) applications. Sub-10 nm channel lengths SWCNT-based FET showed a normalized current density better than those obtained in silicon-based FETs [7, 8]. In another application, SWCNTs were used in flexible devices such as flexible SWCNTs-based thin film transistors (TFTs) achieving a mobility of  $35 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [9]. SWCNTs-based TFTs were attractive for driving organic light-emitting diodes (OLEDs) displays. A vertical SWCNT-based FET showed sufficient currents to enable the red-green-blue emission of OLEDs [10]. In memory applications, SWCNTs were used as floating gates in silicon-based devices and were embedded in high- $k$  dielectrics to serve as a storage element [11, 12]. Their higher thermal stability, chemical inertness, reduced surface states and favorable work function made SWCNTs more suitable than metallic nanocrystals for applications as a floating gate in organic 2T-NVM [13]. Hybrid organic/inorganic 2T-NVM devices using SWCNTs as a floating gate were demonstrated by Alba-Martin et al [13]. The devices used silicon as the semiconductor which is incompatible with flexible electronics applications. In this study, SWCNTs will be used as a floating gate in organic 2T-NVM devices using

all-organic active layers which is compatible with flexible and plastic electronics applications.

### 3.2.2 Pentacene

Pentacene is a p-type small molecule organic semiconductor, it is one of the polycyclic aromatic hydrocarbons and its structure consists of five benzene rings linearly stacked next to each other [14-16]. A schematic diagram of the structure of one molecule of pentacene is shown in Figure 3.3.

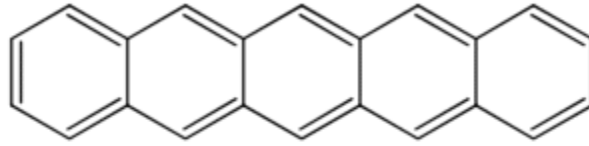


Figure 3.3: The structure of a molecule of pentacene.

Pentacene has high electrical conductivity ( $\sim 0.1 \text{ } \Omega \cdot \text{cm}$ ) under high pressure, at room temperature, and an insulating property under ambient pressure [16]. Its chemical structure is sensitive to oxidation and it slowly degrades when intensively exposed to light or air [14, 15]. Pentacene have been used and studied as an active layer in organic thin film transistors since 1990s [17, 18], a carrier mobility of  $0.002 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  was reported [19]. Since then intense research was carried on pentacene and a carrier mobility of  $5.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  was reported for organic thin film transistors based on pentacene derivatives in 2006 [20].

### 3.2.3 SU8 negative photoresist

SU8 is a negative near-UV epoxy photo-resist and it has insulating properties [21, 22]. SU8 was developed by IBM and is widely used in micro fabrication [21, 22]. The SU8 molecular structure is shown in Figure 3.4 and has eight epoxy groups. The SU8 epoxy groups is crosslinkable upon photo-polymerization [21, 22]. SU8 negative photoresist solution consists of the SU8 epoxy resin, cyclopentanone or gamma butyrolactone as a solvent and a photo-acid generator. The photo-polymerization happens when the coated SU8 thin film is exposed to UV light and  $\text{HSbF}_6$  acids are produced that causes the SU8 epoxy groups to

cross-link upon baking. In this study SU8-2000 was used as the insulating layer of memory structures.

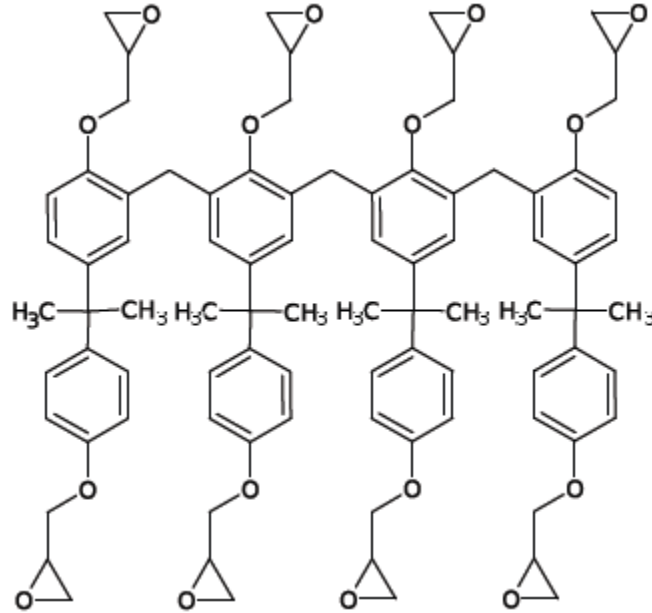


Figure 3.4: The structure of a molecule of SU8 molecule with eight epoxy groups.

### 3.2.4 Polymethylmetacrylate

Poly methyl methacrylate (PMMA) is a synthetic polymer of methyl methacrylate (MMA) and is formed by polymerization of fine droplets of MMA in water under the influence of free-radical initiators [23]. The molecular structure of PMMA is shown in Figure 3.5. PMMA has an insulating nature with a resistivity of more than  $2 \times 10^{15} \Omega \cdot \text{cm}$  and a dielectric constant  $\sim 3$  [23, 24]. Thus PMMA is widely used as an organic insulator in plastic electronics applications and was first used as a gate insulator in 1933 [25].



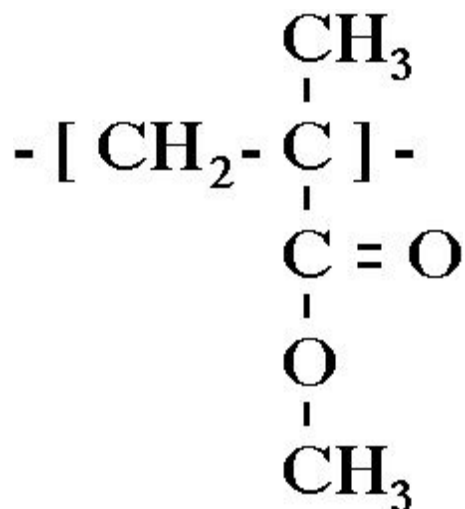


Figure 3.5: The structure of a molecule of PMMA.

### 3.3. Experimental techniques

#### 3.3.1 Layer-by-layer deposition technique

Layer-by-layer deposition is a frequently used technique to build up layers of organic molecules, it is a template-assisted procedure where the substrate is usually a solid having charged surface [26]. It is simply building up oppositely charged molecular layers on top of each other, where the adsorption occurs at high concentrations of the desired material. After each adsorption step the new surface will have an opposite charge sign to the initial one, this is due to adsorbed ionic groups that are still exposed at the surface. Each pair of oppositely charged adsorbed layers is called a bi-layer and is denoted by (cationic/anionic)<sub>x</sub>, where x is the number of times this bi-layer was deposited. It is important after each deposition step to rinse the sample with pure water to remove extra weakly bonded ions. A multi-layer architecture is built after deposition of several bi-layers. This technique is suitable for our research (to build a thin film of deposited SWCNTs) where it controls the agglomeration tendency of the nanotubes [26].

### 3.3.1.1 Functionalization of the SWCNTs

To produce a good architecture and dispersion of SWCNTs, appropriate oppositely charged surfactants are chosen to modify the SWCNTs and prepare them for the self-assembly process. Sodium dodecyl sulphate (SDS), an anionic surfactant, and dodecyltrimethylammonium bromide (DTAB), a cationic dispersion agent, both charged on one end, were used to modify the SWCNTs and make a good separation between the bundles of SWCNTs due to repulsion forces between the constituents of a single solution. The chemical structures of the surfactants used, SDS and DTAB, are illustrated in Figure 3.6, while the modified SWCNTs which were surfactant-coated with oppositely charged outer surfaces are schemed in Figure 3.7. Although the figure gives a scheme of single nanotube coated, but it is very hard to have only one coated nanotube, it is in most cases a bundle of nanotubes coated together. The SWCNT that was modified by the anionic surfactant SDS is denoted SWCNT<sub>a</sub>, and the one that was modified by DTAB (cationic) is SWCNT<sub>c</sub>.

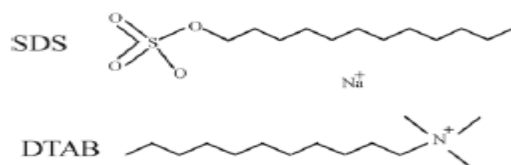


Figure 3.6: Chemical Structures of the surfactants used to modify SWCNTs, SDS and DTAB.

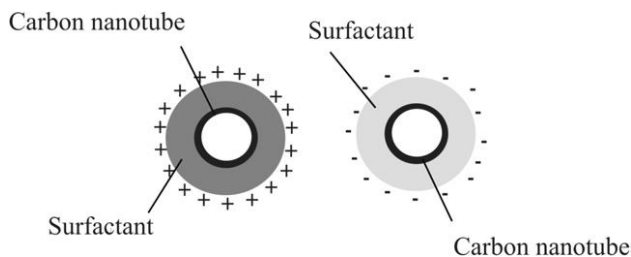


Figure 3.7: Oppositely charged modified SWCNTs, SWCNT<sub>a</sub> and SWCNT<sub>c</sub>.

Two polyelectrolytes, Poly(ethyleneimine) (PEI) ( $M_w=25000$ ) and poly(acrylic acid) (PAA) ( $M_w=4,000,000$ ), were used to provide a seed layer upon which the carbon nanotube thin film was built. Polyelectrolytes are usually polymers that has a repeated units of electrolyte group, that will dissociate in aqueous solutions and make the polymers charged. PAA will lose protons in aqueous solution and be negatively charged, while PEI behaves the other way around. The chemical structure of the polyelectrolytes used for the seed layer is depicted in Figure 3.8.

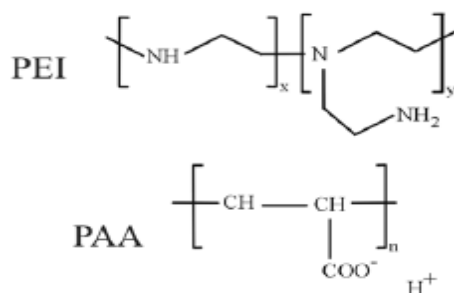


Figure 3.8: Chemical Structure of PEI and PAA.

### 3.3.1.2 Preparation of the building-block solutions

The building blocks solutions of the layer-by-layer deposition are the PEI cationic solution, PAA anionic solution, a solution containing SWCNT<sub>a</sub> (SWCNT modified by SDS anionic surfactant), and a solution containing SWCNT<sub>c</sub> (SWCNT modified by DTAB cationic surfactant). To prepare these four building blocks solutions we have to prepare first the Tris solution, SDS and DTAB.

A Tris solution is needed to dissolve the PEI and PAA where the atomic weight of Tris is  $M_w=121.14$  g/mol and the concentration of the Tris solution is 0.01M (0.01mol/1L). Dissolving Tris powder in de-ionized water yielded a pH=10, while the desired pH=6. The pH then was corrected by adding drops of HCl 50%v1 solution. A 1%wt of SDS was dissolved in de-ionized water. Desired pH=6.5 was achieved by pH correction using HCl or NaOH. And a 0.65% wt of DTAB was dissolved in de-ionized water. pH correction was achieved using NaOH or HCl to obtain a pH=7. The three solutions (Tris, SDS, and DTAB)

are prepared in advance as they are needed in the recipe of the four building blocks solutions.

Commercial PEI was mixed in the Trix solution at 2% v/v, a pH of 8.5 was obtained. And commercial PAA was obtained the same way and a correction of pH was used to reach 6.5. Pure SWCNTs were dispersed in the SDS solution with a concentration of 0.25mg/ml, the solution was then sonicated overnight to allow the clusters to break into bundles and ideally to individual tubes modified by SDS to finalize the SWCNT<sub>a</sub> solution. Similar to SWCNT<sub>a</sub>, pure SWCNTs were dispersed with a concentration of 0.25mg/ml in the DTAB solution. The dispersion was also sonicated. The SWCNT<sub>a</sub> and SWCNT<sub>c</sub> solutions are sonicated for at least one hour before use.

### 3.3.1.3 Possible architectures

The four solutions that were prepared can contribute to four combinations of (anionic/cationic) bi-layers, (PEI/PAA), (PEI/SWCNT<sub>c</sub>), (SWCNT<sub>a</sub>/PAA), or (SWCNT<sub>a</sub>/SWCNT<sub>c</sub>) falling into three architectures categories:

- 1- architecture 1: A reference device structure where no SWCNTs are embedded, this is achieved by the growth of several (PEI/PAA) bi-layers (Figure 3.9 (a)).
- 2- architecture 2: A structure where only one modified SWCNT (anionic or cationic) per bi-layer is deposited, this can be achieved by depositing several bi-layers of (PEI/SWCNT<sub>c</sub>) or (SWCNT<sub>a</sub>/PAA) (Figure 3.9 (b)).
- 3- architecture 3: A structure of alternating SWCNT<sub>a</sub> and SWCNT<sub>c</sub>. This structure is achieved by the growth of one or several (SWCNT<sub>a</sub>/SWCNT<sub>c</sub>) bi-layers (Figure 3.9 (c)).

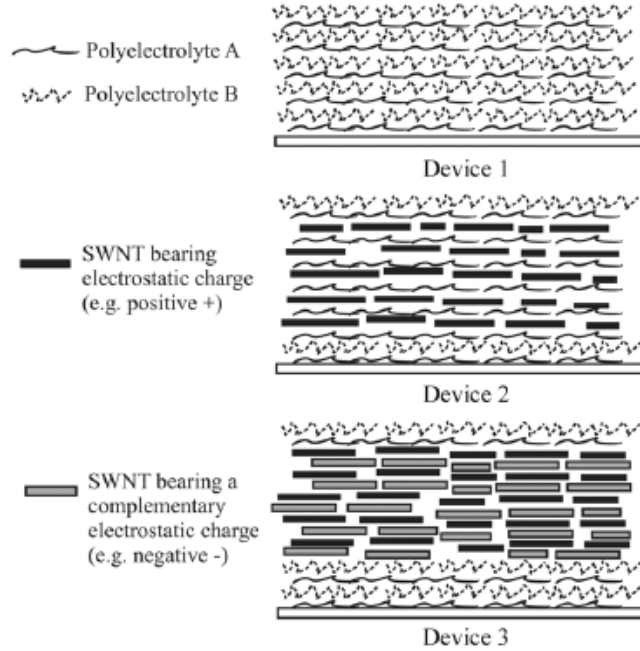


Figure 3.9: Device 1: no SWCNTs are involved. Device 2: Only one SWCNT in a bi-layer. Device 3: Two SWCNTs in a bi-layer [26].

### 3.3.1.4 Carbon nanotubes LbL deposition procedure:

Once we had the four solutions SWCNT<sub>a</sub>, SWCNT<sub>c</sub>, PEI, PAA ready. The LbL thin film deposition in this investigation was performed using the architecture of type 2 (PEI/PAA)<sub>1</sub>+(PEI/SWCNT<sub>c</sub>)<sub>5</sub> structure. This architecture proved to be the optimal in terms of charge storage and retention for the application of SWCNTs as a floating gate in silicon based devices [13]. The deposition began by the alternate immersion of the substrate in PEI and PAA solutions, for 15 min each to form seed layers which facilitate the adhesion of SWCNTs. The substrate was then repeatedly immersed in PEI solution for 15 min then SWCNT<sub>c</sub> solution for 30 min. After each immersion, the substrate was rinsed with deionized water and dried with nitrogen. The final SWCNTs matrix consisted of five SWCNTs - PEI bilayers. A schematic diagram of the LbL deposition is presented in Figure 3.10 (a) and an AFM image of deposited SWCNTs using LbL technique is shown in Figure 3.10 (b). The AFM image shows that the SWCNT has a length of around 400 nm and a diameter less than 5 nm, which is an indication that the LbL techniques ensures that the SWCNTs are dispersed and deposited horizontally onto the substrate.

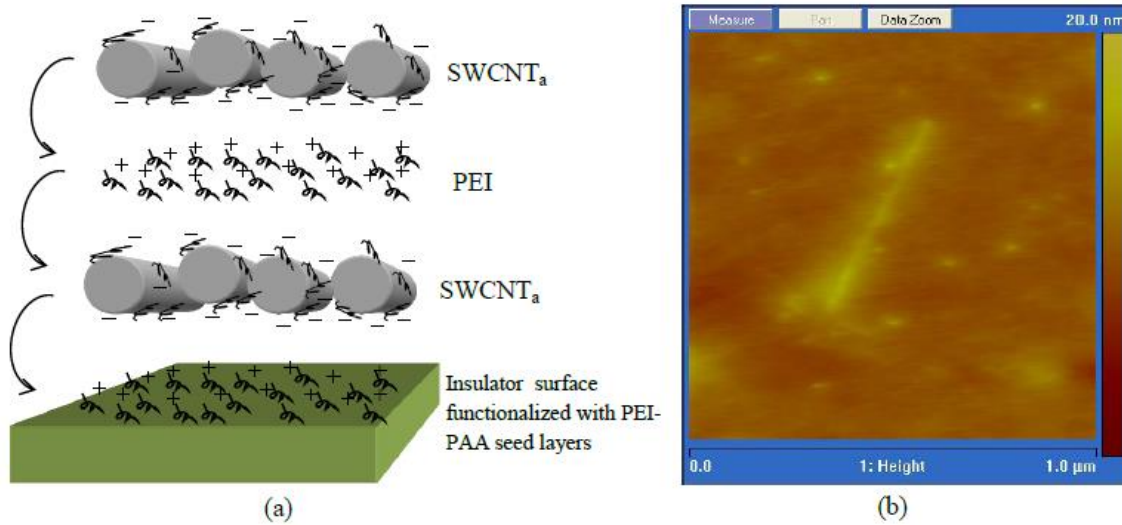


Figure 3.10: (a) schematic diagram of the LbL technique, (b) AFM image of the deposited SWCNTs.

### 3.3.2 Thin film deposition techniques: Spin coating, Thermal, E-beam evaporation and sputtering

The other layers of the fabricated devices were deposited using conventional deposition techniques such as spin coating, evaporation or sputtering.

Organic insulators used in this investigation, SU8 or PMMA, were spin coated. Pentacene was thermally evaporated in a Kurt Lesker organic evaporator. Aluminium oxide (AlO<sub>x</sub>) and tungsten (W) were evaporated using Leybold 350 E-Beam evaporator. Aluminium (Al) and gold (Au) contacts were thermally evaporated using an Edwards 306 Turbo evaporator. Copper (Cu) was deposited using RF sputtering in an argon plasma using a Leybold 350 sputterer.

### 3.4. Fabrication of devices

Three types of different 2T-NVM are fabricated and its structures are shown in Figure 3.11. The first type is a pentacene based embedded MIS structure using SWCNTs as a floating gate (Figure 3.11 (a)). The second type is an embedded MIM structure using SWCNTs as charge storage elements (Figure 3.11 (b)). And the third type is a filamentary based MIM in the electrochemical metallization (ECM) structure using  $\text{AlO}_x$  as the resistive switching medium (Figure 3.11 (c)).

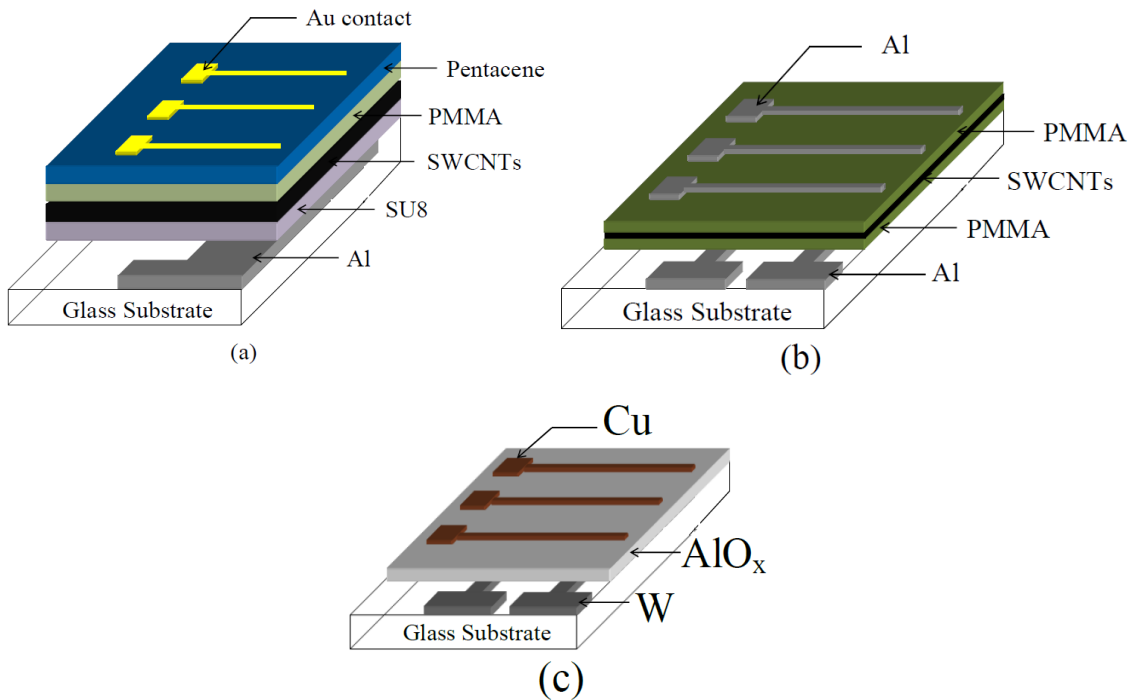


Figure 3.11: The structures of 2T-NVM memory devices fabricated. (a) Pentacene-based MIS using SWCNTs as a floating gate. (b) Embedded MIM structure using SWCNTs as charge storage elements. (c) Filamentary based MIM in the ECM structure using  $\text{AlO}_x$  as the RS medium.

The embedded MIS and MIM memories (Figure 3.11 (a) and (b)) were fabricated as follows: glass substrates were cleaned through successive ultrasonic treatments in acetone, methanol and isopropanol, then they were rinsed with deionized water and dried with nitrogen flow. A 100 nm thick Al gate was thermally evaporated through a shadow mask.

The first insulator was deposited using spin coating. SWCNTs were deposited by the layer-by-layer (LbL) deposition as explained in section 3.3.1.5. The second insulator was subsequently spin coated to encapsulate the SWCNTs. For the embedded MIM memories, the top Al electrode was thermally evaporated to a 100 nm thickness to finalize the device structure shown in Figure 3.11 (b). While for the embedded MIS structure, pentacene was thermally evaporated at a rate of 0.01-0.07 nm/s to a thickness of ~30 nm. Finally, 30 nm of gold was deposited, through a shadow mask, to form Ohmic contacts to finalize the device structure shown in Figure 3.11 (a).

On the other hand, the  $\text{AlO}_x$  filamentary based ECM memories (Figure 3.11 (c)) was fabricated by evaporating the Tungsten bottom through a shadow mask using e-beam evaporator to a thickness of 75 nm at a rate of 0.1 nm/sec. Then a 20 nm thick  $\text{AlO}_x$  was deposited on the whole slide using e-beam evaporation at a deposition rate of 0.2 nm/sec. Finally, a thin layer of copper was sputtered through a 1 mm wide shadow mask in an argon plasma at a pressure of  $1.2 \times 10^{-2}$  mbar to a thickness of 50 nm with a deposition rate of 0.5 nm/sec to complete the  $\text{Cu}/\text{AlO}_x/\text{W}$  device structure (Figure 3.11 (c)).

## **3.5 Characterization**

### **3.5.1 Surface morphology**

The characterization of the fabricated devices was performed through recording its current-voltage (I-V) or capacitance-voltage (C-V) characteristics depending on the memory type. Also, surface morphology of deposited layers was performed in order to optimize the device structure. The surface morphology characterization was done through Atomic force microscopy (AFM). AFM is a high-resolution scanning probe microscopic technique [27, 28]. The scanning process of an AFM is done by placing a sharp tip of a microscopic cantilever close to the surface of the sample. The attractive force from the surface towards the tip through scanning is used to take a surface morphology image of the sample. The image is took by a laser spot reflected to a sensor upon the bending of the cantilever tip upon the applied force of the surface. In this study the morphology of the grown pentacene was studied using AFM scans performed in the tapping mode. And the thickness of the deposited insulators was also measured using an AFM.



### **3.5.2 C-V characteristics**

The C-V characteristics of the embedded MIS memory devices, fabricated in air under ambient cleanroom laboratory conditions, were performed through double 100 mV AC measurement sweep using a PC driven LCR Bridge (HP-4192). The C-V behavior of the MIS devices was recorded at 400 kHz with a 0.5 V/sec scan rate. Each test consisted of a double sweep (positive – negative) at room temperature in air.

### **3.5.3 I-V characteristics**

The I-V characteristics of the embedded MIM and filamentary based MIM devices, fabricated in air under ambient cleanroom laboratory conditions, were performed through a double DC measurement sweep using a PC driven HP 4140b pA Meter/DC Voltage Source. The I-V characteristics of the devices were recorded at a scan rate of 0.2 V/sec and each test consisted of a double sweep at room temperature in air.

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# Chapter 4

## Control MIS devices

### 4.1. Introduction

In this chapter the fabrication and characterization of pentacene-based organic metal-insulator-semiconductor (MIS) devices without embedded floating gates will be presented. The different MIS devices will be fabricated with different insulators to optimize the device performance in terms of low operating voltages and absence of charge trapping. The insulators used were the negative photoresist SU8 and polymethylmetacrylate (PMMA). PMMA was dissolved in two different solvents; chloroform and chlorobenzene. The MIS devices without embedded CNTs as a floating gate were fabricated as control devices and its characteristics will be used to be compared with those of floating gate memory devices.

### 4.2. Control devices structure

Four different control devices with combinations of different insulators were fabricated. The fabricated devices are as follows:

- 1- SU8-based MIS
- 2- PMMA-based MIS
  - a- PMMA dissolved in chlorobenzene
  - b- PMMA dissolved in chloroform
- 3- SU8/PMMA-based MIS

All of four control devices were fabricated in the same structure under the same laboratory conditions, at room temperature, in air and in a cleanroom environment. The structure of the control devices is Al/insulator/pentacene/Au and is depicted in Figure 4.1. Briefly, a non-conductive soda-lime glass substrate was cleaned using piranha solution and a 100 nm thick Al gate was thermally evaporated through a shadow mask. Afterwards, the insulator (SU8, PMMA or a combination of both) was deposited using the relevant

deposition technique for each insulator used. Pentacene was thermally evaporated at a rate of 0.01-0.07 nm/s to a thickness of ~30 nm. Finally, 30 nm of gold was thermally evaporated from a tungsten boat at a rate 0.2 nm/sec, through a shadow mask, to form Ohmic contacts with the semiconductor. The thicknesses of the thermal evaporation was monitored through a crystal monitor to determine the deposition rate and the film thickness. In each control device fabricated, the morphology of the pentacene layer deposited on different insulators was investigated using Veeco NanoMan Atomic Force Microscopy (AFM) operated in the tapping mode. The thickness of each insulator was measured through the AFM scan, by etching part of the deposited insulator using plasma dry etching and measuring the depth at the edge of the patterned insulator. A PC driven LCR Bridge (HP-4192) was used to record the capacitance-voltage (C-V) behavior of the devices at 400 kHz with a 0.5 V/sec scan rate. Each test consisted of a double sweep (positive – negative) at room temperature in air.

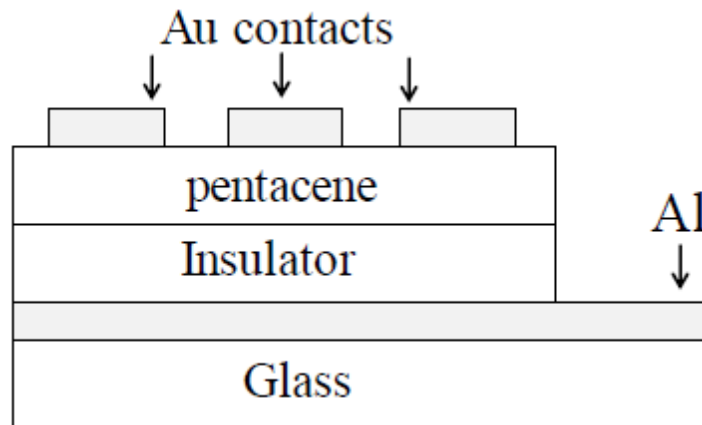


Figure 4.1: The structure of the fabricated control MIS devices.

### 4.3. Control devices using SU8 as an insulator

The control device using SU8 as an insulator is in the Al/SU8/pentacene/Au structure similar to that depicted in Figure 4.1. The SU8 was spin coated for 10 sec at 500 rpm then for 30 sec at 3000 rpm and hard-baked for 5 min at 95 °C. Afterwards the spin-coated thin

film was cross-linked by exposing to 66 mJ/cm<sup>2</sup> of UV radiation, then baked at 65 °C and 95 °C for 2 and 5 min, respectively.

#### **4.3.1 Thickness of the SU8 film**

The thickness of the deposited SU8 insulator was measured through the AFM scan. The SU8 was etched through plasma dry etching using a shadow mask, the shadow mask consists of 4 x 4 circular holes as shown in Figure 4.2 (a). The thickness of the SU8 thin film was measured by measuring the difference between the bottom of the hole and the top edge of it. The difference between the minimum peak and the maximum peak of the scan of 1 hole was 63.262 nm as shown in Figure 4.2 (a). The average of the holes depth calculated for 4 diagonal holes was around 65 nm, as shown in Figure 4.2 (b). This shows the uniform coating of the SU8 layer over the whole slide. This is essential for the fabricated MIS devices because the uniformity of the insulator will result in reproducible and repeatable devices all over the area of the slide.

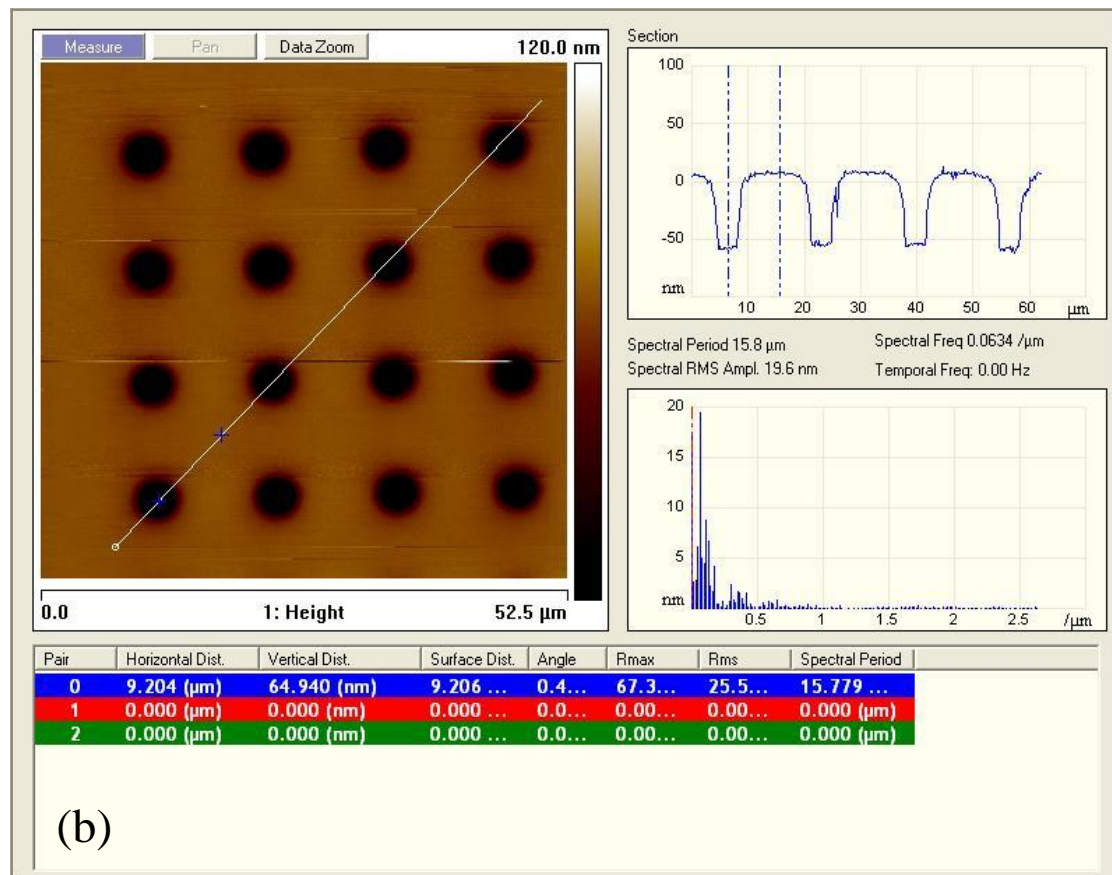
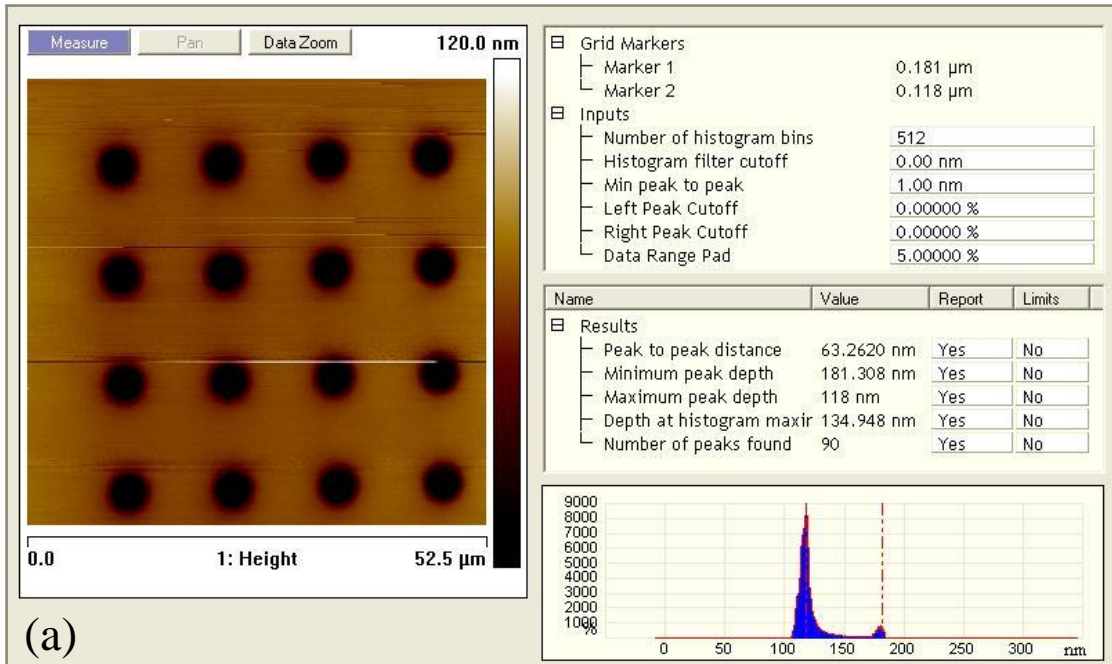


Figure 4.2: (a) AFM image of the etched SU8 film and the measured thickness of one hole. (b) The average measured thickness of four diagonal etched SU8 holes



### **4.3.2 Surface morphology of pentacene-on-SU8**

The surface morphology of the evaporated pentacene is a very important influential factor for the semiconducting behavior of pentacene [1-3]. Thus, the surface morphology in terms of the grain size of the grown pentacene is very important to the devices performance [4-6]. In the fabricated devices structures, pentacene was evaporated on top of an insulator. The selection of that insulator depends on how pentacene grows and crystallize on the insulator surface. The three insulators used in this study are SU8, PMMA-in-chloroform and PMMA-in-chlorobenzene and were deposited onto different substrates. The three substrates with the SU8, PMMA-in-chloroform and PMMA-in-chlorobenzene layers were placed in the organic thermal evaporator where pentacene was deposited at the same evaporation conditions. The surface morphology of the pentacene grown on SU8, PMMA-in-chloroform and PMMA-in-chlorobenzene was studied to evaluate its quality.

The AFM image of the surface morphology of pentacene thin film evaporated on top of the SU8 insulator is shown in Figure 4.3. The surface morphology shows that the pentacene film has nearly amorphous morphology with grain sizes in the range of  $0.5\mu\text{m}^2$ .

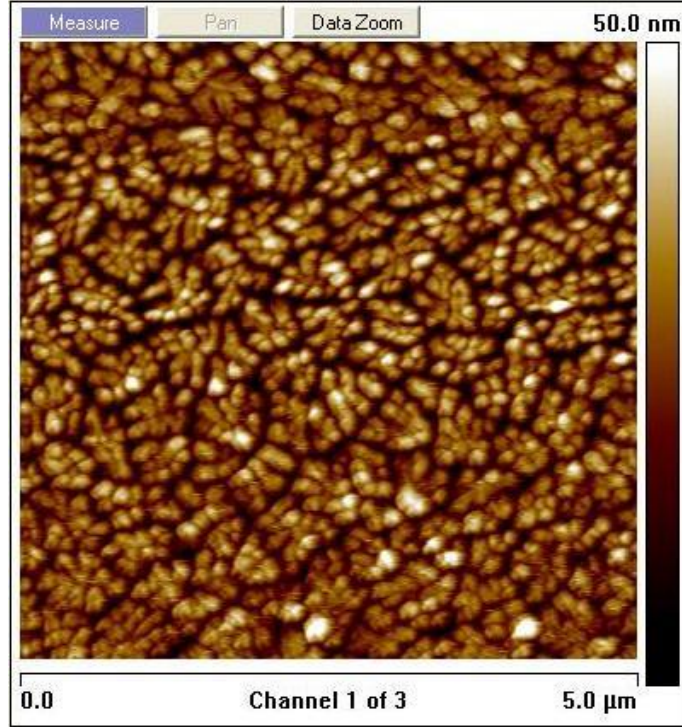


Figure 4.3: AFM image of the surface morphology of pentacene thin film evaporated on top of the SU8 insulator.

#### 4.3.3 Electrical characterization of Al/SU8/pentacene/Au

The C-V characteristics of the control device Al/SU8/pentacene/Au was measured at a frequency of 400 KHz and is shown in Figure 4.4. The control device exhibited the usual characteristics of MIS structures based on p-type semiconductors, with flatband voltage of -7.5 V and full semiconductor depletion at 0 V. The double voltage sweep exhibited almost no hysteresis which is indicative of the absence charge trapping in the bulk SU8 dielectric or at its interface with pentacene. Assuming that the MIS structure consist of an insulator capacitance ( $C_{Ins}$ ) connected in series with a semiconductor capacitance ( $C_s$ ), the C-V characteristics of the control devices may be used to extract some of the fabrication parameters [7-10]. The majority carriers accumulate at the interface between the insulator and semiconductor when the device operates in the accumulation region [11-14]. Thus, the maximum accumulation capacitance ( $C_{max} = 280$  pF) can be used to estimate the dielectric constant of the insulator stack using [15]

$$C_{max} \cong C_{Ins} = A \epsilon_{Ins}/d_{Ins} \quad (4.1)$$

where  $\epsilon_{Ins}$  is the dielectric constant of the SU8 insulator,  $d_{Ins}$  the SU8 thickness and  $A$  the device area ( $1 \text{ mm}^2$ ). Using the insulator stack thickness measured using AFM (65 nm), we obtained  $\epsilon_{Ins} = 36.52 \times 10^{-12} \text{ F/m}$ , corresponding to an effective relative permittivity of 2.372 which is close to reported values in the literature [16]. The intrinsic doping concentration ( $N_a$ ) of the pentacene thin film semiconductor is calculated using [15]:

$$C_{FB} = A \frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins}}{\epsilon_S} \sqrt{\frac{K_b T}{e} \frac{\epsilon_S}{e N_a}}} \quad (4.2)$$

Where  $C_{FB}$  is the flatband capacitance,  $\epsilon_S$  is the dielectric constant of pentacene ( $3 \times 8.85 \times 10^{-12} \text{ F.m}^{-1}$ ) [17],  $K_b$  the Boltzmann constant and  $T$  the temperature (300 K),  $e$  the electric charge. The measured capacitance at the flatband voltage (-7.5 V) is estimated to be 268 pF (Figure 4.4). Accordingly, the calculated intrinsic doping concentration was  $\sim 2.42 \times 10^{17} \text{ cm}^{-3}$ , in a close agreement with recently reported values [17]. Applying a positive DC bias to the gate of a p-type organic MIS capacitor causes majority carriers in the semiconductor to be repelled from the insulator interface. This is associated with a decrease in the capacitance as the depletion region expands. For a thin film, the capacitance is at its minimum when the organic semiconductor is fully depleted (the equivalent of the inversion regime for a conventional Si/SiO<sub>2</sub> MOS device). Thus, the minimum capacitance is determined by the insulator and semiconductor capacitances in series. The minimum capacitance ( $C_{min}$ ) corresponding to full depletion is then given by [15, 18]:

$$C_{min} = A \frac{\epsilon_{Ins}}{d_{Ins} + \frac{\epsilon_{Ins} W_{Max}}{\epsilon_S}} \quad (4.3)$$

The maximum depletion width of  $W_{Max} = 28.63 \text{ nm}$  is close to the estimated pentacene thickness of 30 nm which was measured during the thermal evaporation using a crystal thickness monitor.

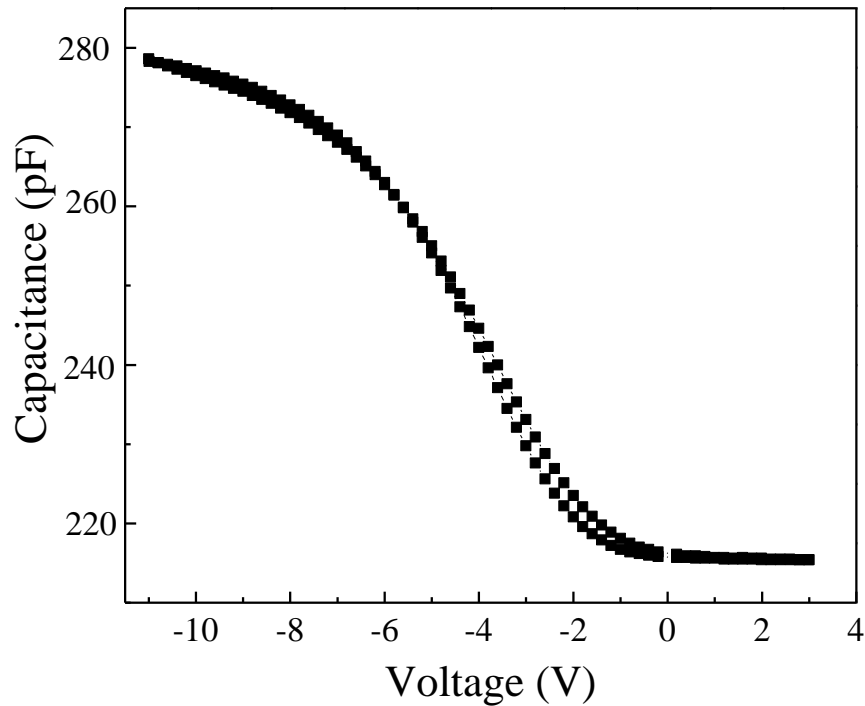


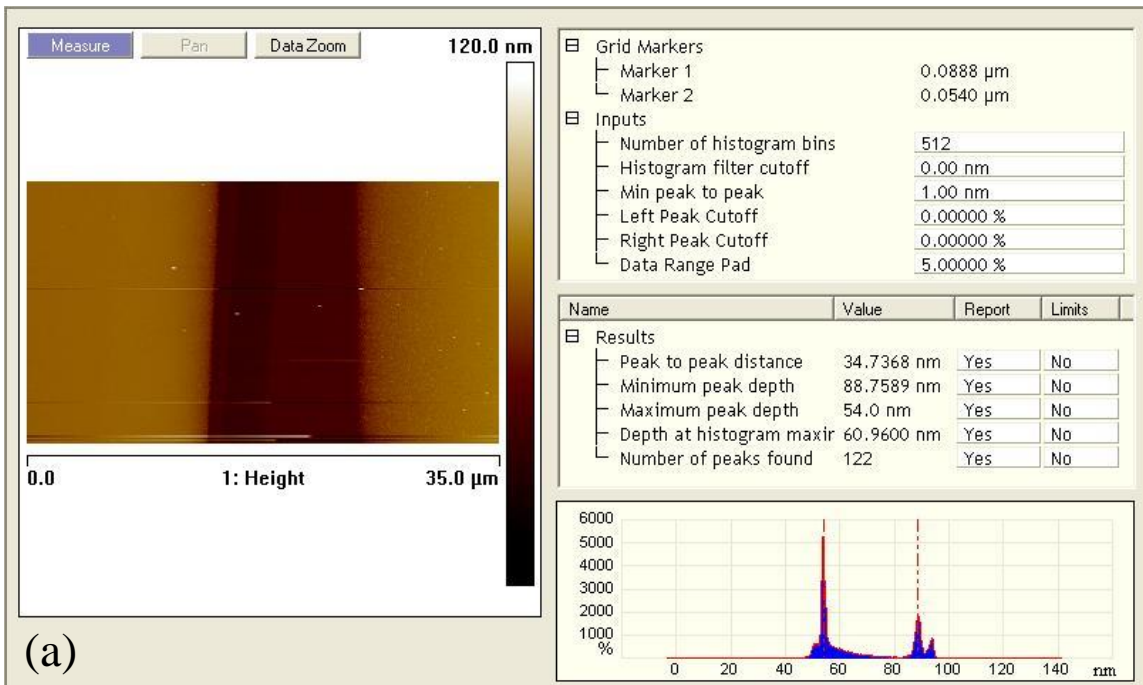
Figure 4.4: C-V double sweep of Al/SU8/pentacene/Au control devices.

#### 4.4 Control devices using PMMA as an insulator

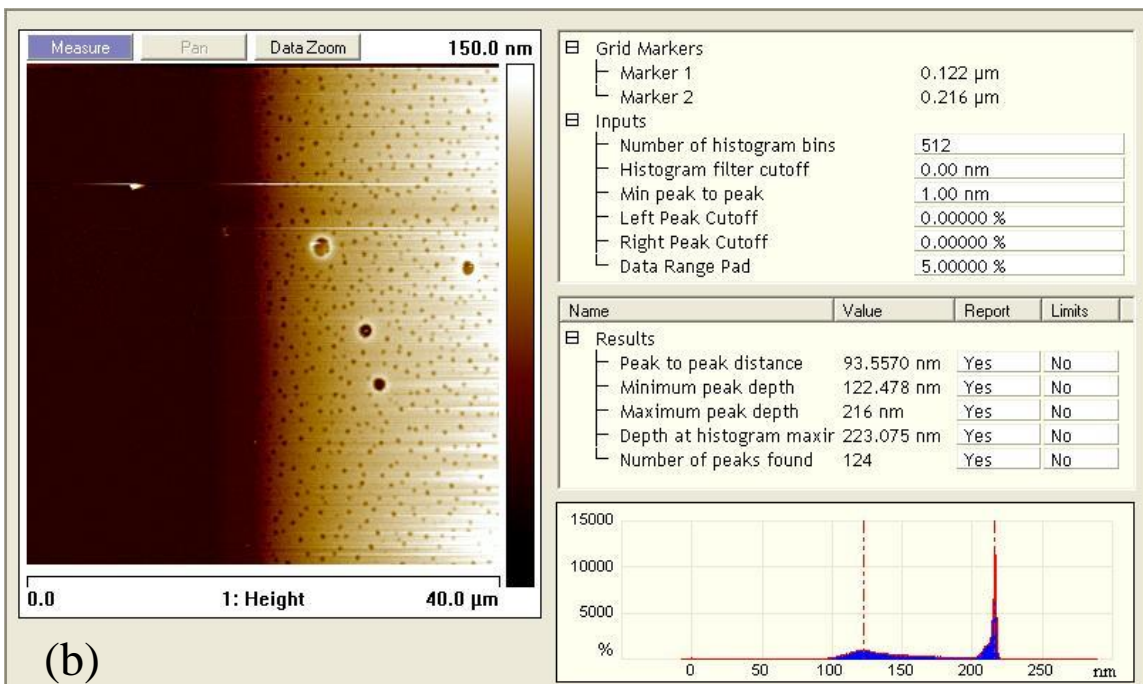
The control device using PMMA as an insulator is in the same structure as depicted in Figure 4.1 (Al/PMMA/pentacene/Au). As mentioned in Section 4.1, the PMMA was dissolved in two different solvents; chloroform and chlorobenzene. The PMMA thin film deposited from that dissolved in chloroform will be named in this section PMMA-in-chloroform, while the other will be named PMMA-in-chlorobenzene. Both solutions were made in the same concentration (20 wt%) and both thin films were deposited in the way using spin coating (10 sec at 500 rpm then for 30 sec at 6000 rpm) and baked for 25 min at 120 °C.

#### **4.4.1 Thickness of the PMMA film**

The thickness of the deposited PMMA insulator was measured in a similar way the SU8 was measured through the AFM scan. Where part of the deposited insulator was etched and the scan measured its depth. Figure 4.5 (a) and (b) shows the AFM scan of the patterned PMMA-in-chlorobenzene and PMMA-in-chloroform, respectively. The thickness of the deposited PMMA-in-chlorobenzene was measured to be around 35 nm as shown in Figure 4.5 (a). While the thickness of the PMMA-in-chloroform thin film was measured to be around 94 nm as shown in Figure 4.5 (b). As the spin coating conditions are the same for both samples, it is clear from the above results that PMMA was dissolved in chlorobenzene more uniformly than chloroform. The PMMA-in-chloroform surface morphology shows some pin-holes in the deposited thin film (Figure 4.5 (b)) which may be due to the non-perfect dissolution of PMMA in the chloroform solvent. On the other hand no voids or holes appear in the PMMA-in-chlorobenzene thin film (Figure 4.5 (a)).



(a)

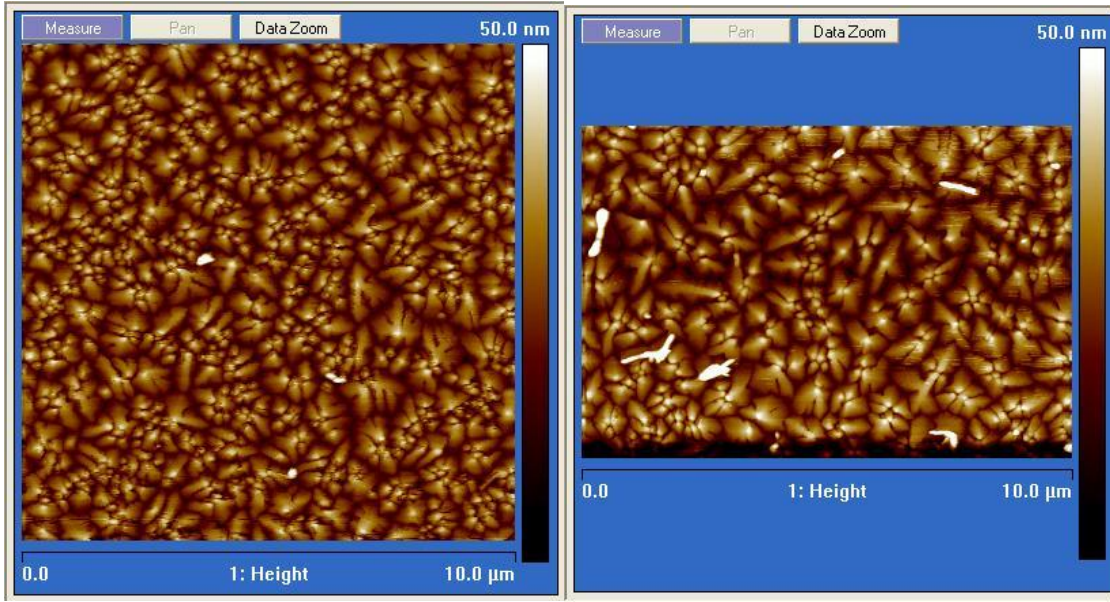


(b)

Figure 4.5: AFM image of the etched film and its measured thickness of (a) PMMA-in-chlorobenzene (b) PMMA-in-chloroform.

#### 4.4.2 Surface morphology of pentacene-on-PMMA

The AFM images of the surface morphology of pentacene thin film evaporated on top of the PMMA-in-chlorobenzene and PMMA-in-chloroform thin films are shown in Figure 4.6 (a) and (b), respectively. The surface morphology shows that the pentacene film, unlike its amorphous structure on top of SU8, has a polycrystalline structure when evaporated on the PMMA insulator. Figure 4.6 shows that relatively large grain sizes were found when pentacene was deposited on both PMMA thin films dissolved in chloroform or in chlorobenzene. A pentacene grain size of about  $1.2 \mu\text{m}^2$  was observed when deposited on PMMA-in-chlorobenzene as shown in Figure 4.6 (a). Similar pentacene grain sizes  $\sim 1.1 \mu\text{m}^2$  was found when pentacene was deposited on PMMA-in-chloroform as shown in Figure 4.6 (b). A clear disorders appears in Figure 4.6 (b) of pentacene evaporated on PMMA-in-chloroform which might be related to the pin-holes and voids that appeared in the morphology of the PMMA-in-chloroform thin film shown in Figure 4.5 (b). Despite these disorders, the grain sizes of pentacene deposited on PMMA was almost the same size despite the type of solvent employed. The grain size of pentacene on PMMA is almost twice as much as the grain size of pentacene on SU8. This shows that pentacene grows and crystallizes on the PMMA much better than on the SU8 due to the difference in the surface energy and roughness of different insulators [10]. Pentacene shows higher charge carrier mobility with larger grain size [10], thus PMMA was used as the insulator were pentacene is grown rather than SU8.



(a)

(b)

Figure 4.6: AFM image of the surface morphology of pentacene thin film evaporated on top of the (a) PMMA-in-chlorobenzene (b) PMMA-in-chloroform thin films.

**4.4.3 Electrical characterization Al/PMMA/pentacene/Au**

Two control devices were fabricated using the PMMA insulator, one using PMMA-in-chloroform and the other using PMMA-in-chlorobenzene. The structures of the fabricated control devices are Al/PMMA-in-chloroform/pentacene/Au and Al/PMMA-in-chloroform/pentacene/Au and are in the same structure that is depicted in Figure 4.1. The C-V characteristics of the control devices Al/PMMA-in-chloroform/pentacene/Au and Al/PMMA-in-chlorobenzene/pentacene/Au were measured at a frequency of 400 KHz and are shown in Figure 4.7 (a) and (b), respectively. Both devices characteristics in Figure 4.7 (a) and (b) exhibited the usual characteristics of MIS structures based on p-type semiconductors, with flatband voltage of -4 V and -4.5 V and full semiconductor depletion at 0.5 V and 1 V, respectively. For both devices, the double voltage sweep exhibited no hysteresis which is indicative of the absence of charge trapping in the bulk PMMA dielectric. Similar to Section 4.2.3.3, the maximum accumulation capacitance can be used to estimate the dielectric constant of the insulator stack. Using Eq. 4.1 and the insulator thickness



measured using AFM (40 or 95 nm) and the  $C_{\text{Max}} = 145$  or  $154$  pF, we obtained  $\epsilon_{\text{Ins}} = 18.8 \times 10^{-12}$  or  $29.2 \times 10^{-12}$  F/m, corresponding to an effective relative permittivity of 2.13 or 3.3 for PMMA-in-chloroform or PMMA-in-chlorobenzene, respectively. The values are in the range of calculated relative permittivity of PMMA found in the literature [19-23].

For both devices  $N_a$  of the pentacene thin film semiconductor is calculated using Eq. 4.2. The measured capacitance at the flatband voltage (-4 V and -4.5 V) is estimated to be 142 pF and 151 pF from Figure 4.7 (a) and (b). Accordingly, the calculated intrinsic doping concentration was  $\sim 4.71 \times 10^{17} \text{ cm}^{-3}$  and  $5.36 \times 10^{17} \text{ cm}^{-3}$  for PMMA-in-chloroform or PMMA-in-chlorobenzene devices, respectively. The  $W_{\text{Max}} = 11.6$  nm and  $10.7$  nm was calculated from Eq. 4.3 and using the minimum capacitance 145 pF and 154 pF for PMMA-in-chloroform or PMMA-in-chlorobenzene, respectively. The maximum depletion width in this case is clearly lower than the estimated thickness of pentacene (30 nm). This is an indication that the devices in this case (unlike the SU8 case) did not reach the full depletion region as shown in Figure 4.7 as the capacitance did not reach a constant minimum value. This reflects the fact that some carriers still exist in the pentacene which might be a leakage current through the PMMA itself. This also reflects on the low dielectric constant calculated for PMMA from the C-V characteristics of the whole structure.

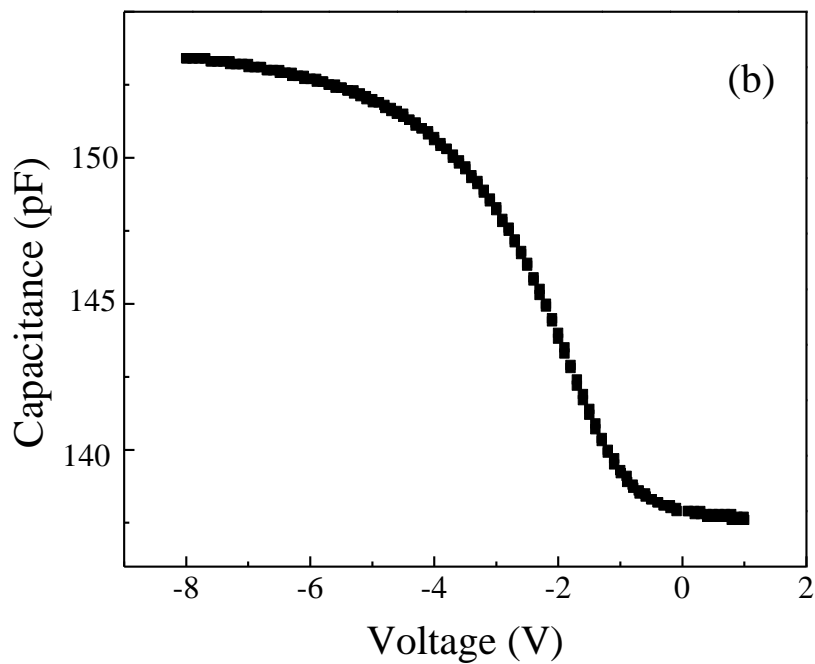
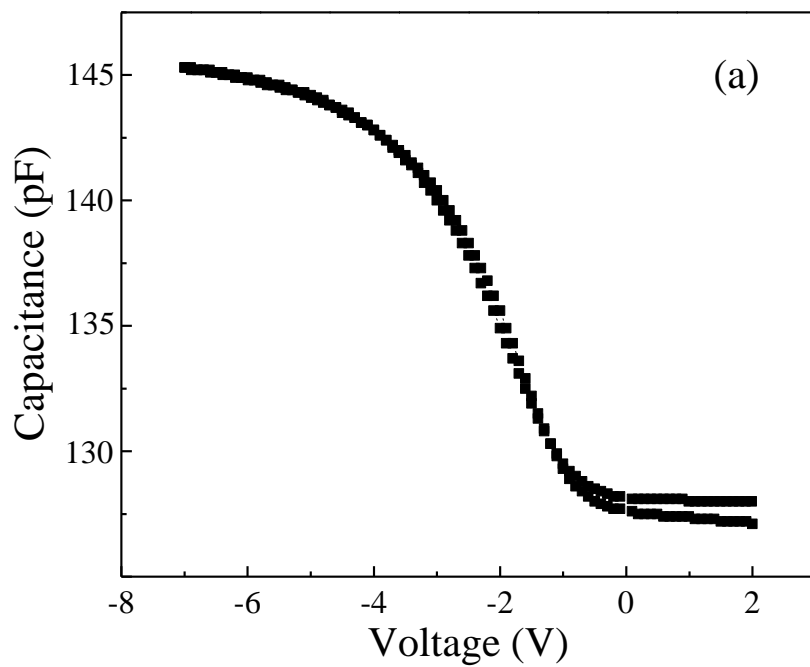


Figure 4.7: C-V double sweep of (a) Al/PMMA-in-chloroform/pentacene/Au and (b) Al/PMMA-in-chlorobenzene/pentacene/Au control devices.

## **4.5 Control devices using SU8/PMMA as an insulator**

### **4.5.1 Thickness of the SU8/PMMA/pentacene stack**

A control device using a combination of two layers of SU8 and PMMA was also fabricated in the Al/SU8/PMMA/pentacene/Au structure. The deposition of each layer was performed in a similar way used in previous devices. Thus measuring the thickness of the active layer will be beneficial to check the reproducibility and reliability of the deposited layers. The active layer of the device is the two organic insulators and the organic semiconductor, i.e. the SU8/PMMA/pentacene stack. After the successive deposition of SU8, PMMA and pentacene, the organic SU8/PMMA/pentacene stack was etched using plasma dry etching. The thickness was measured using an AFM, similar to the way the thicknesses of SU8 and PMMA layers were measured in Sections 4.3.1 and 4.4.1, respectively. Figure 4.8 shows the AFM image of the etched SU8/PMMA/pentacene stack and the measured thickness which was in the region of ~ 109 nm. The measured thickness is roughly the summation of the individual thicknesses of SU8 (65 nm, Section 4.3.1), PMMA (~35 nm, Section 4.4.1) and pentacene (30 nm). The measured thickness of the tri-layer SU8/PMMA/pentacene stack shows that each individual layer is reproducible in the same thickness at different slides. This is essential for the reproducibility of the fabricated memory devices. It also shows that the deposited layers do not affect each other and the spinning of PMMA does not affect the deposited SU8 layer.

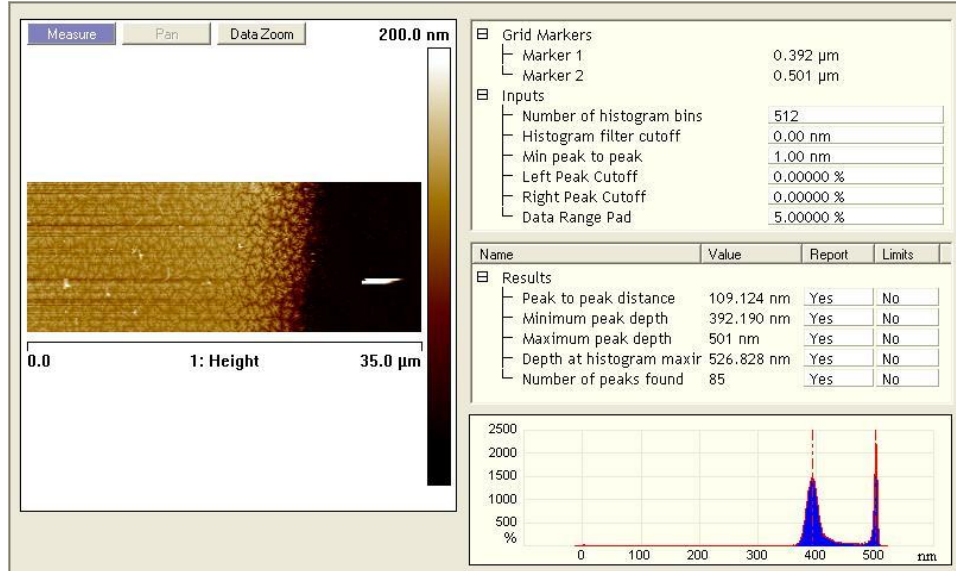


Figure 4.8: AFM image of the etched SU8/PMMA/pentacene trilayer and its measured thickness.

#### 4.5.2 Electrical characterization Al/SU8/PMMA/pentacene/Au

The C-V characteristics for the device is shown in Figure 4.9 (a) and (b) for a scan sweep range of  $\pm 5$  V and  $\pm 20$  V, respectively. Similar to the previously fabricated control devices, the device exhibited the usual characteristics of MIS structures based on p-type semiconductors, with flatband voltage of -2.5 V and full semiconductor depletion at 0 V. The double voltage sweep exhibited no hysteresis which is indicative of the absence charge trapping in the bulk dielectrics, at the surface of the SU8 and PMMA layers or at the PMMA/pentacene interface. The maximum accumulation capacitance ( $C_{\text{max}} = 332$  pF) can be used to estimate the dielectric constant of the SU8/PMMA insulator stack using Eq. 4.1. Using the insulator stack thickness which can be considered the cumulative SU8 and PMMA thicknesses measured using AFM ( $\sim 100$  nm), we obtained  $\epsilon_{\text{Ins}} = 36.5 \times 10^{-12}$  F/m, corresponding to an effective relative permittivity of 4.12 of the SU8/PMMA stack. The measured capacitance at the flatband voltage (-2.5 V) is estimated to be 320 pF (Figure 4.9 (a)). Accordingly, the calculated intrinsic doping concentration was  $\sim 4.61 \times 10^{17} \text{ cm}^{-3}$ , in a close agreement with recently reported values [16, 17]. The  $W_{\text{Max}} = 26$  nm was calculated from Eq. 4.3 and using the minimum capacitance 256 pF of the control device.

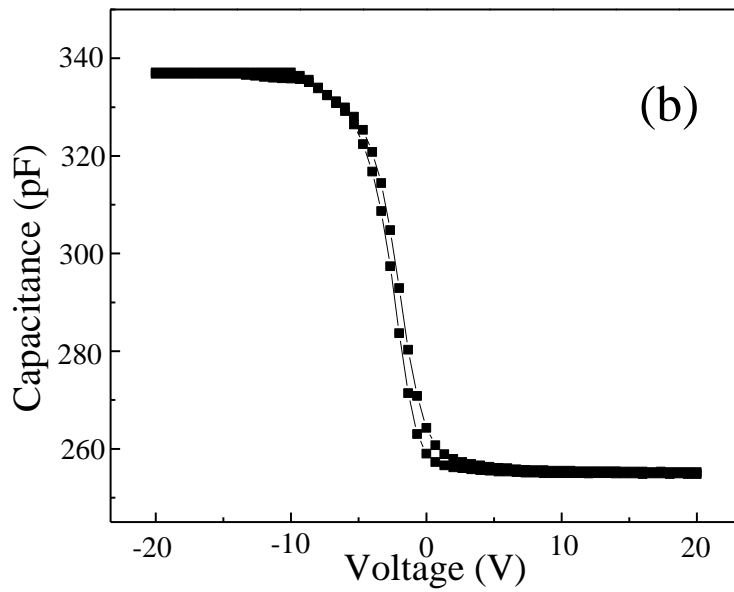
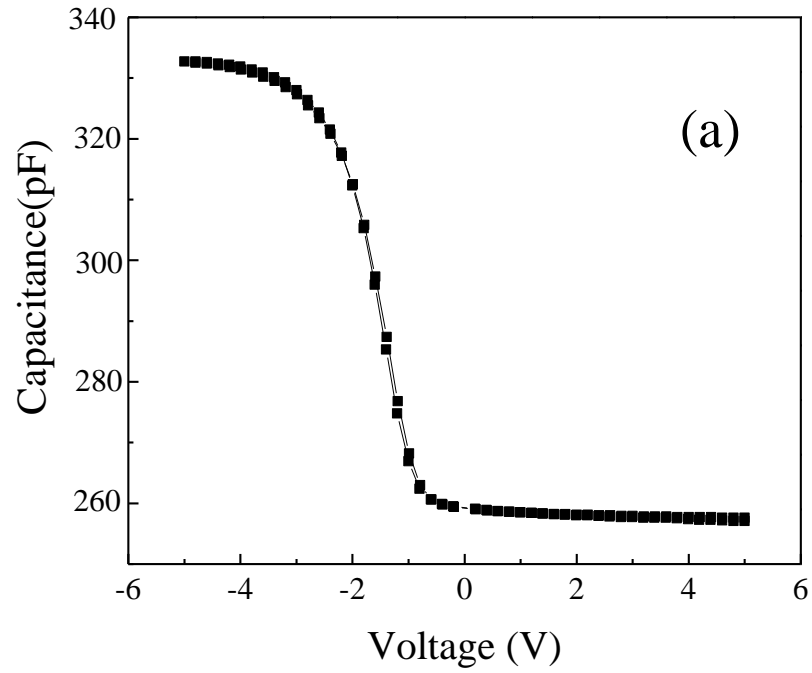


Figure 4.9: C-V characteristics of the control Al/SU8/PMMA/pentacene/Au device at a scan sweep range of (a)  $\pm 5$  V and (b)  $\pm 20$  V.

## 4.6 Summary of the fabricated control devices

In summary, different control devices structures using different insulators were fabricated. The fabricated control devices structures and their extracted electronic parameters from the C-V characteristics is shown in table 4.1. The C-V characteristics were used to calculate some parameters of interest, a summary of the calculated parameters is shown in table 4.2 for the four fabricated control MIS devices. A comparison between the extracted parameters of the fabricated structures shows that the operating absolute values of voltages of the control devices can be reduced by the larger grain size of the pentacene semiconductor which supports the correlation found in the literature [1, 24]. As shown in table 4.1 a grain size less than  $0.1 \mu\text{m}^2$  will lead to a MIS structure (Al/SU8/pentacene/Au) that reaches its flatband voltage at  $-7.5 \text{ V}$ , while the flat band voltage can be closer to  $0 \text{ V}$  ( $\sim -2.5 \text{ V}$ ) when the grain size of pentacene in the MIS structure (Al/SU8/PMMA/pentacene/Au) is larger than  $1.2 \mu\text{m}^2$ . The low operating voltages around  $0 \text{ V}$  is favorable for the READ, WRITE and ERASE operations of the MIS memory applications [25, 26]. It can be deduced from table 4.1 that the selection of the insulator is important for the next step of fabricating low-operating-voltage memory devices. Thus the use of SU8 as an insulator to evaporate the pentacene will be excluded from the next step of fabricating an embedded MIS memory devices. On the other hand, the evaporation of pentacene on top of PMMA, showed a larger grain size pentacene and this was reflected in the lower absolute value of the operating voltages of the Al/PMMA/pentacene/Au and Al/SU8/PMMA/pentacene/Au structures as shown in table 4.1.

Although the fabricated control devices exhibit different C-V characteristics and different operating voltages, but in terms of the application as floating gate-based MIS memory devices the important feature in the control devices is to make sure that there is no traps effect in those devices. This was clear through the double sweep of the C-V characteristics of all control devices. All four fabricated control devices were traps free and this was concluded from the absence of hysteresis of its C-V characteristics upon the double sweep. The absence of traps in the four control devices also shows the reproducible clean fabrication of the MIS structure and will clearly show the effect of the addition of a floating gate to the structure. Thus the next step of the addition of CNTs will show if the CNTs are

able to trap the carriers inside the structure and if it can be used as charge storage elements in the MIS memory application.

Table 4.1: The extracted parameters of the fabricated control devices from C-V characteristics

Control device structure	Grain size of pentacene	Measured $d_{Ins}$	$V_{FB}$	$C_{FB}$	$V_{dep}$	$C_{max}$	$C_{min}$
Al/SU8 /pentacene/Au	$0.5 \mu m^2$	65 nm	-7.5 V	268 pF	0 V	280 pF	215 pF
Al/PMMA(chlrfrm) /pentacene/Au	$1.1 \mu m^2$	95 nm	-4 V	142 pF	0.5 V	145 pF	128 pF
Al/PMMA(chlrbnzn) /pentacene/Au	$1.2 \mu m^2$	40 nm	-4.5 V	151 pF	1 V	154 pF	137 pF
Al/SU8/PMMA /pentacene/Au	$1.2 \mu m^2$	105 nm	-2.5 V	320 pF	0.5 V	332 pF	256 pF

Table 4.2: The calculated parameters of the fabricated control devices from C-V characteristics

Control device structure	$\epsilon_{Ins}$	$\epsilon_r$	$W_{max}$	$N_a$
Al/SU8 /pentacene/Au	$2.1 \times 10^{-11}$ F/m	2.37	28.6 nm	$2.42 \times 10^{17}$ cm <sup>-3</sup>
Al/PMMA(chlrfrm) /pentacene/Au	$1.88 \times 10^{-11}$ F/m	2.13	11.6 nm	$4.71 \times 10^{17}$ cm <sup>-3</sup>
Al/PMMA(chlrbnzn) /pentacene/Au	$2.92 \times 10^{-11}$ F/m	3.3	10.7 nm	$5.36 \times 10^{17}$ cm <sup>-3</sup>
Al/SU8/PMMA /pentacene/Au	$3.65 \times 10^{-11}$ F/m	4.12	26 nm	$4.61 \times 10^{17}$ cm <sup>-3</sup>

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## Chapter 5

# Layer-by-layer deposited SWCNTs as storage elements in MIS and MIM memory structures

### 5.1. Introduction

The most promising two terminal organic nonvolatile memory (ONVM) candidates are those that use charge traps inside a simple and well-known structure to induce the memory behavior [1]. The controlled embedment of charge traps inside a simple metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) structure results in a controlled memory behavior [2]; this may be reflected in the concentration of charges that a memory can store which will be directly proportional to the number of traps doped within the structure [3].

As explained in section 2.5.3, the embedded charge traps will result in a switching in the I-V characteristics between two different resistance states in the MIM structure, or a hysteresis in the MIS structure to define two capacitance states [4]. The amount of charges stored is reflected by the ON/OFF ratio of the MIM memory and by the memory window at the flat band capacitance of the MIS memory [1-4]. The amount of charges and the retention time inside the traps may be optimized by engineering the traps within the insulator.

#### 5.1.1 Charge traps in two terminal ONVM devices

There are two methods to embed the traps inside the insulator: first method is to blend the particles or traps in the insulator solution and spin the solution to create a thin film of the organic insulator, and the traps will be distributed almost uniformly throughout the organic film (Figure 5.1 (a)). The second approach is to deposit the traps in the middle of the insulating layer, which can be achieved as follows: spin coating a first insulating layer to form a surface where an assembly layer (matrix or thin film) of the traps are deposited on

top. After the deposition of the traps, another insulating layer is spin coated on top of the traps to complete its confinement in the middle of two insulators (Figure 5.1(b)). Although the uniform distribution of the traps may result in a lower operating voltage while charging the storage nodes, but the confinement of the traps in the middle of the insulating layer was reported to have the longest retention time [5]. This is attributed to the relatively thicker insulators confining the traps in the middle-trap-layer stack, thus whenever the charges are stored, it is trapped between two high and thick potential barriers which minimizes the chances of charge leakage and thus optimizes the retention characteristics [1-5].

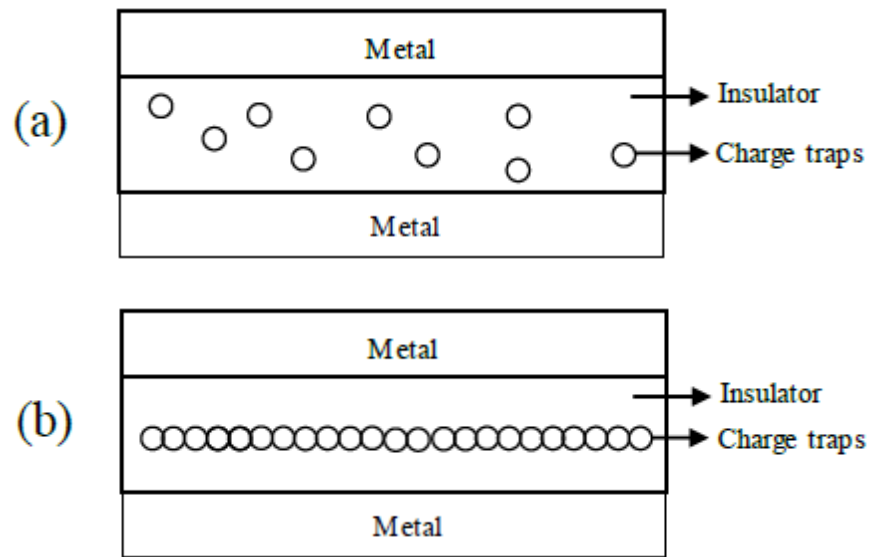


Figure 5.1: (a) charge traps uniformly distributed inside the insulator, (b) charge traps located in the middle of the insulator

In this chapter, the utilization of layer-by-layer (LbL) deposited single-walled carbon nanotubes (SWCNTs) as charge storage nodes in different memory structures will be presented. The SWCNTs deposited using LbL technique form a thin film of matrix which will serve as middle-trap-layer similar to that depicted in Figure 5.1 (b). Two different structures will be presented: in the first structure the SWCNTs were used as a nanofloating gate in MIS memory structure based on pentacene as an organic semiconductor and a

combination of different insulators selected from the fabricated control MIS devices in chapter 4. While in the second structure the LbL deposited SWCNTs were embedded between two polymethylmetacrylate (PMMA) organic insulators to serve as charge traps and result in resistive switching and memory behavior in the MIM memory structure.

Section 2 of this chapter will present the different MIS memories fabricated based on SWCNTs as charge traps and the selection of different insulators to optimize the device performance in terms of charge retention and low operating voltages. The electrical characterization, hysteresis direction, charge injection analysis and charge retention characteristics of each structure will be explained.

On the other hand Section 3 will present the use of SWCNTs as charge traps between two PMMA insulators in the MIM memory structure. The fabricated device structure, electrical characteristics, retention characteristics, switching analysis, out-of plane carrier transport mechanism and the relevant charge conduction models will be detailed.

## **5.2. SWCNTs as nanofloating gate in MIS memory structures**

### **5.2.1 Memory devices structures**

In this section LbL deposited SWCNTs were embedded in the insulator of the MIS control devices fabricated in chapter 4 to result in a memory behavior of the structures. Two different MIS memory devices were fabricated in the same structure under the same conditions. The structure of the fabricated memory devices is Al/insulator/SWCNTs/insulator/pentacene/Au as depicted in Figure 5.2. Briefly, a glass substrate was cleaned using a piranha solution and a 100 nm thick Al gate was thermally evaporated through a shadow mask. Afterwards the first insulator (SU8 or PMMA) was deposited using the relevant deposition technique for each insulator used. On top of the first insulator, SWCNTs were deposited using LbL deposition technique which was detailed in chapter 3. In this structure, the deposition of SWCNTs began by the alternate immersion of the substrate in aqueous poly(ethyleneimine) (PEI) (cationic, pH = 8.5) and poly(acrylic acid) (PAA) (anionic, pH = 6.5) solutions, for 15 min each to form seed layers to facilitate the adhesion of SWCNTs onto the insulating layer. The substrate was then repeatedly immersed in PEI solution for 15 min then in anionic SWCNTs (SWCNT<sub>a</sub>)

solution dispersed in sodium dodecyl sulphate (SDS) for 30 min (as detailed in Section 3.3.1.2). After each immersion, the substrate was rinsed with deionized water and dried with nitrogen. The final SWCNTs matrix consisted of three SWCNT<sub>a</sub> - PEI bilayers. Afterwards, another insulating thin film was deposited on top of the SWCNTs to ensure their encapsulation. Then pentacene was thermally evaporated at a rate of 0.01-0.07 nm/s to a thickness of ~30 nm. Finally, 30 nm of gold was deposited, through a shadow mask, to form Ohmic contacts.

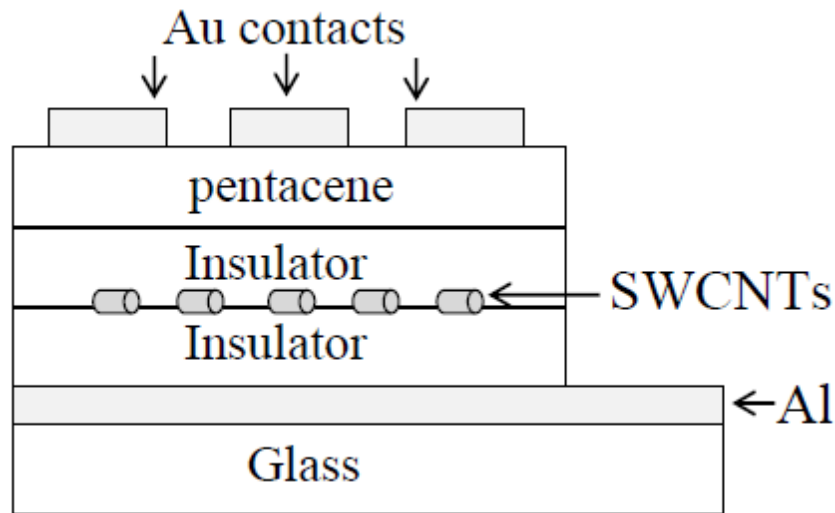


Figure 5.2: The structure of the fabricated embedded MIS memory devices.

As concluded from chapter 4 Section 2.6, the growth of pentacene on PMMA was better than its growth on SU8 in terms of the thin film grain size. Pentacene-on-PMMA had much larger grain size than pentacene-on-SU8 which was reflected in the performance of the MIS structure. Thus in all fabricated memory devices structures, PMMA was selected to be the second insulating thin film material rather than SU8. As such two memory device structures were fabricated, one benefits from PMMA as the first and the second insulator. The characteristics of the Al/PMMA/SWCNTs/PMMA/pentacene/Au memory device will be presented in Section 5.2.2. While the other structure benefits from SU8 as the first insulator and PMMA as the second insulator to produce a memory device in the form of Al/SU8/SWCNTs/PMMA/pentacene/Au structure. The memory characteristics of the later structure will be presented in Section 5.2.3.

In each memory device fabricated, a PC driven LCR Bridge (HP-4192) was used to record the capacitance-voltage (C-V) behavior of the devices at 400 kHz with 0.5 V/sec scan rate. Each test consisted of a double sweep (positive – negative) at room temperature, in air and under the same conditions that the control devices were tested.

## **5.2.2 Al/PMMA/SWCNTs/PMMA/pentacene/Au memory devices**

### **5.2.2.1 Electrical characterization**

The absence of hysteresis in the C-V characteristics of the Al/PMMA/pentacene/Au control device (Figure 5.3 (a)) was an evidence of the absence of charge carriers trapped inside the structure. The control device exhibit a flat band capacitance of 142 pF at a flat band voltage of -4 V. The value of the  $C_{FB}$  was approximated to be around 90% of the normalized capacitance [6], where the maximum capacitance is considered the 100% and the minimum capacitance is considered to be the 0%. The addition of SWCNTs as a floating gate to the control sample to form Al/PMMA/SWCNTs/PMMA/pentacene/Au, resulted in clear hysteresis in the C-V characteristics as shown in Figure 5.3 (b). The forward sweeps started from +20 V exhibited characteristics similar to those of the control devices, with ~135 pF accumulation capacitance. In contrast with control devices, when the accumulation was reached in the memory devices, a clear negative shift to more negative values in flatband voltage is evident for reverse voltage sweep as shown in Figure 5.3(b). The difference in the accumulation capacitance to the control device was expected due to a change in the effective insulator stack thickness when SWCNTs are embedded and another layer of PMMA was added. The reverse sweep showed a distinct change in the flatband voltage shifting to about 8 V for  $\pm 20$  V sweeping voltage range. The hysteresis is attributed to the presence of SWCNTs as a floating gate and results from the charging and discharging of the SWCNTs when negative and positive voltages are consecutively applied. Accordingly, the C-V curve in Figure 5.3 (b) is shifted towards more negative voltage. The charges stored in the SWCNTs floating gate (Q) can be estimated from  $Q = C_{FB} \times \Delta V_{FB}$ , where  $C_{FB}$  and  $\Delta V_{FB}$  are the flatband capacitance and flat band voltage shift, respectively [6]. For  $C_{FB} = 132$  pF and  $\Delta V_{FB} = 8$  V, there are approximately  $6.6 \times 10^{11} \text{ cm}^{-2}$  charges stored in the SWCNTs floating gate for  $\pm 20$  V sweep voltage.

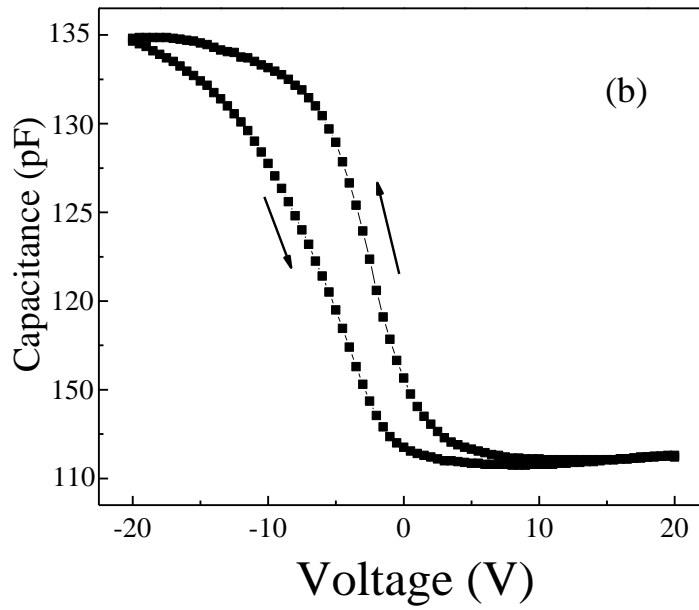
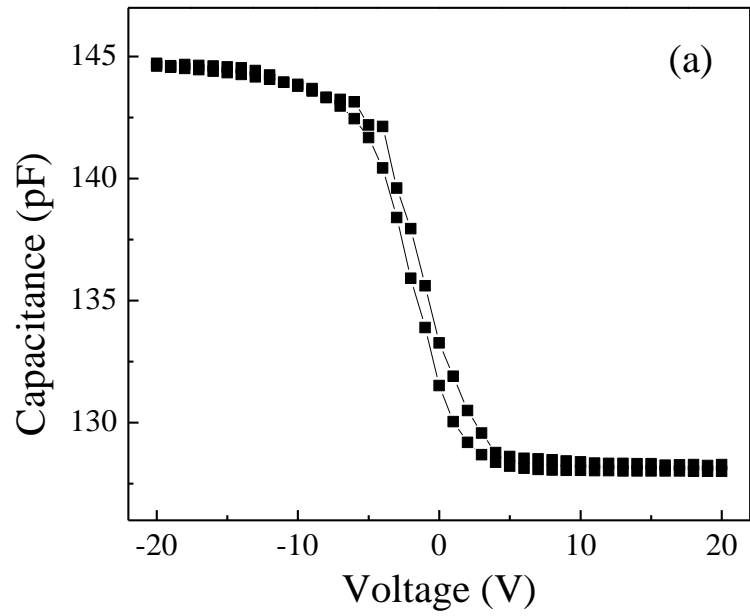


Figure 5.3: C-V double sweep of (a) control device Al/PMMA/Pentacene/Au and (b) SWCNT embedded memory device: Al/PMMA/SWCNTs/PMMA/Pentacene/Au



### 5.2.2.2 Hysteresis direction and charge injection

The most interesting parameter could be noticed in the C-V characteristics of the Al/PMMA/SWCNTs/PMMA/pentacene/Au memory devices is the direction of hysteresis. The hysteresis in the C-V characteristics upon the double sweep is a resultant of the shift of the whole C-V characteristics due to the charges trapped in the floating gate. The shift in the C-V characteristics to the left or right can result in a clockwise or anti-clockwise hysteresis. This is dependent on the type of carriers, holes or electrons, and the way of injection to the floating gate. Thus the direction of the hysteresis (clockwise or anti-clockwise; in our case here it is anti-clockwise) in the C-V characteristics can be used to explain the charge carriers transport inside the embedded MIS stack.

The double voltage sweep for the C-V characteristics of an embedded MIS structure based on a p-type semiconductor starts from the positive voltages (applied to the metal gate) towards the negative values and then back to the positive ones. For an organic MIS structure based on a p-type semiconductor, the accumulation occurs when negative bias is applied to the metal gate while deep-depletion occurs when positive bias is applied. As such the double voltage sweep starts from the deep-depletion towards the accumulation and then back to the deep-depletion region. When a positive bias is applied to the metal gate, the semiconductor is deeply depleted from charge carriers and thus the charging of the floating gate in deep-depletion is very difficult. On the other hand, when negative bias is applied, the carriers accumulate at the semiconductor-insulator interface and thus the charging of the floating gate is easier [7-9].

When the voltage sweep reaches the accumulation, the floating gate gets charged and a shift in the flat band voltage and consequently a shift in the whole C-V characteristics of the MIS structure occur [7-9]. If the shift in the flat band voltage occurs towards more negative values, similar to that shown for our devices in Figure 5.3 (b), this means that an anti-clockwise hysteresis in the double sweep will be observed as shown in Figure 5.4 (a). The shift of the flat band voltages toward more negative values means that more electrons on the gate are needed for the structure to reach accumulation and to reach the flat band capacitance. The more electrons needed is attributed to the existence of trapped positive charges or holes in the floating gate. This happens when a sufficient amount of negative

bias is applied to the gate in its accumulation regime, the electrons attract the holes accumulated at the semiconductor/insulator interface and the holes get injected from the interface to the floating gate at sufficient voltages. A schematic diagram of the holes injection from the semiconductor towards the floating gate is shown in Figure 5.4 (b). Thus when an anti-clockwise hysteresis is observed in the C-V characteristics of the devices, this means that positive charges or holes are charging the floating gate and that the holes are being injected to the floating gate from the semiconductor. The fabricated Al/PMMA/SWCNTs/PMMA/pentacene/Au devices display an anti-clockwise hysteresis, a negative flatband voltage shift in the C-V characteristics during the reverse voltage sweeps (Figure 5.3 (b)). These results are consistent with the behavior of a p-type pentacene in the MIS structure where holes are injected into the SWCNT floating gates from the pentacene through the PMMA organic insulator. We therefore believe that when a sufficient negative voltage is applied to the gate electrode, holes are injected from the pentacene through the PMMA thin film into the floating gate resulting in charging the SWCNTs layer. Equally, a higher positive gate voltage must be applied to reach depletion in the pentacene and discharge the SWCNTs from the holes.

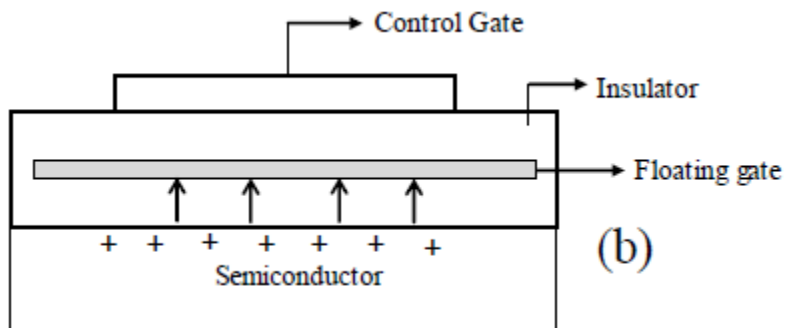
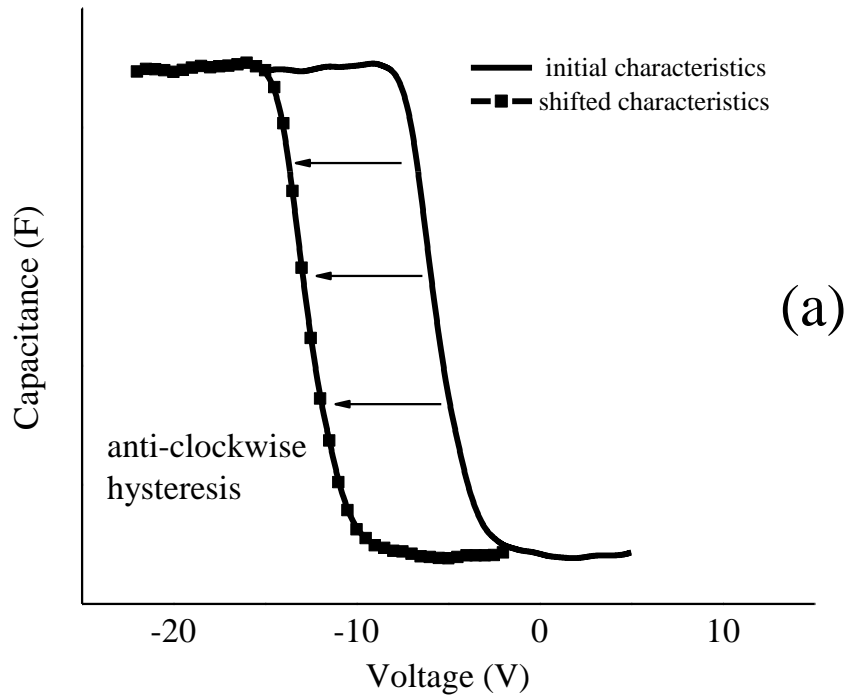


Figure 5.4: (a) The shift of the C-V characteristics of the embedded MIS structure towards more negative values (b) Schematic diagram of holes injection to floating gate.

### 5.2.2.3 Charge retention characteristics

The retention behavior of the MIS-based memory structures were observed by monitoring the capacitance with time after charging the device for few seconds and then applying a stress voltage. The stress voltage was chosen in the range where both capacitance states exist to monitor the change of the capacitance as a result of the charge leakage. Here, a two second -20 V pulse was applied to charge the memory device and the stress voltage was -7.5 V. 86% of the charges trapped in the SWCNTs remained confined in the floating gate over the measurement time of more than 6 hours of continuous testing as shown in Figure 5.5. The capacitance didn't reach a stable value after 6 hours of continuous testing. This indicates the very small constant leakage of charges after six hours of continuous testing indicates that the MIS memory structure has a good retention capacity and there is a very small leakage current in the MIS structure.

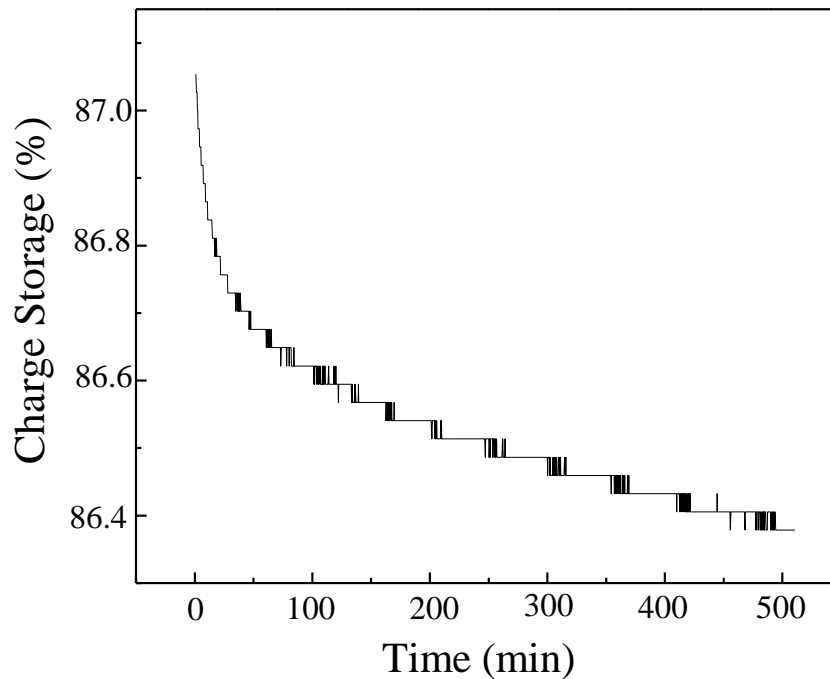


Figure 5.5: Charge retention characteristics of Al/PMMA/SWCNTs/PMMA/Pentacene/Au memory devices

### **5.2.3 Al/SU8/SWCNTs/PMMA/pentacene/Au memory devices**

#### **5.2.3.1 Electrical characterization**

The C-V characteristics of the Al/SU8/PMMA/pentacene/Au control device are shown in Figure 5.6 (a). The control device exhibit a flat band capacitance of 320 pF at a flat band voltage of -2.5 V. The absence of hysteresis in the control device was an evidence of the absence of charge carriers trapped at the SU8/PMMA and PMMA/pentacene interfaces. The addition of SWCNTs as a floating gate to the control device to form Al/SU8/SWCNTs/PMMA/pentacene/Au, resulted in clear hysteresis in the C-V curves (Figure 5.6 (b)). Forward sweeps below  $\pm 10$ V exhibited characteristics similar to those of the control devices, with 255 pF accumulation capacitance and a very small negative shift in the flatband voltage to -2.8 V (-2.5 V for the control device). In contrast, a clear positive shift in flatband voltage to (-1.8 V) is evident for  $\pm 15$  V voltage sweep as shown in Figure 5.6 (b). The difference in the accumulation capacitance to the control device was expected due to a change in the effective insulator stack thickness when SWCNTs are embedded.

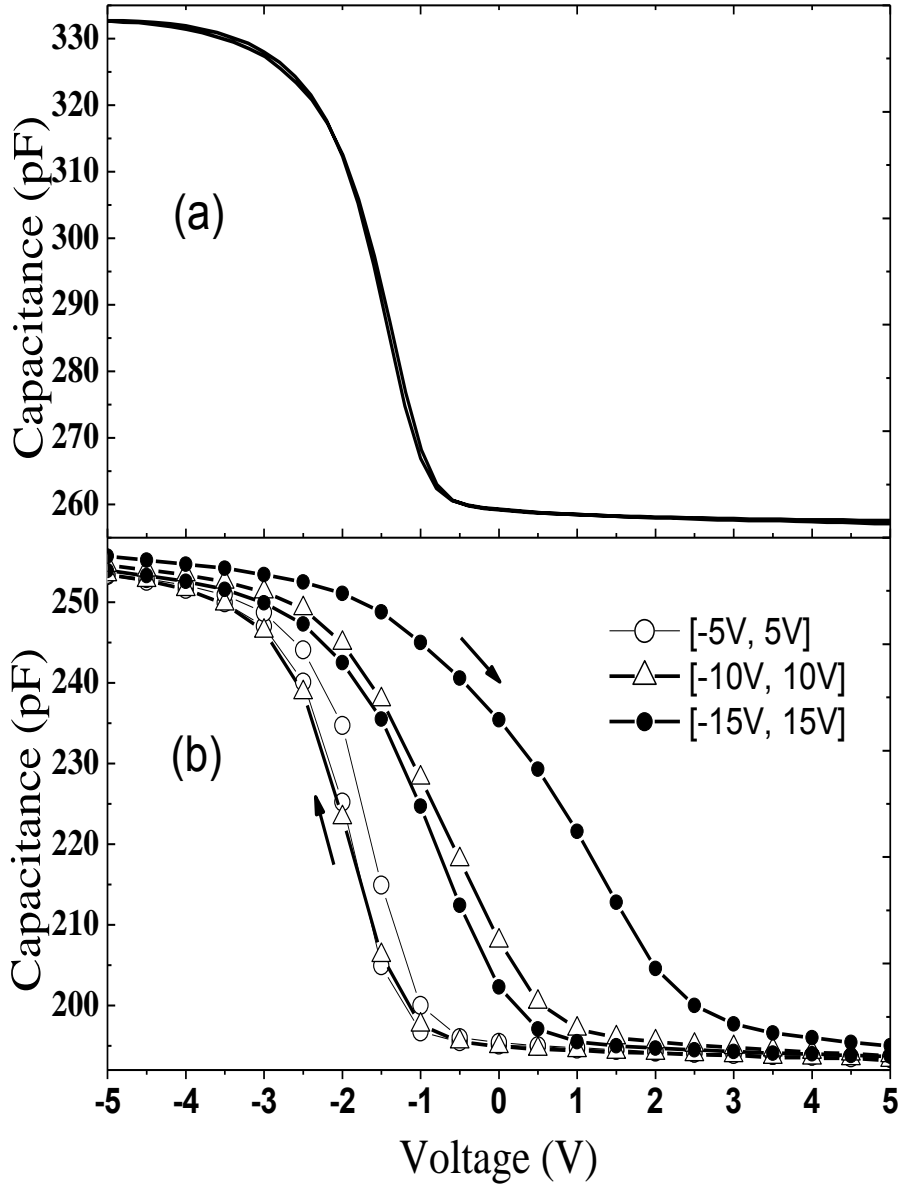


Figure 5.6: C-V double sweep of (a) control device Al/SU8/PMMA/Pentacene/Au and (b) SWCNT embedded memory device: Al/SU8/SWCNTs/PMMA/Pentacene/Au

The small negative shift in the flatband voltage (compared to the control device) after the forward sweep and for sweeping voltage below  $\pm 10$  V indicates that a very few incorporated holes originating from the pentacene become trapped on the SWCNTs layer. The positive shift in flatband voltage for the voltage sweep from 15 V to -15 V is attributed to the breakdown in the SU8 dielectric strength, resulting in a leakage current and electrons transfer through the SU8 film to the floating gate. Typical values for SU8 dielectric

strengths are 100-150 V/ $\mu\text{m}$  and thickness dependent. Hence, for a  $\sim 70$  nm thick SU8 layer, the breakdown voltage is very close to  $\sim 13$  V [10]. The reverse sweep showed a distinct change in the flatband voltage shifting to about 1.3 V for  $\pm 15$  V sweeping voltage range. The hysteresis is attributed to the presence of SWCNTs as a floating gate and results from the charging and discharging of the SWCNTs when negative and positive voltages are consecutively applied. The shape of the hysteresis curves for low sweeping voltages, below the SU8 breakdown voltage (Figure 5.6 (b), specifically the short depletion regions) reflects high charge transport mobility for the semiconductor layer. This will lead to fast charging and discharging of the SWCNTs in the memory stack. As shown Figure 5.7, the hysteresis in the C-V curves increased with sweeping voltages in the measured range (from  $\pm 5$  V to  $\pm 30$  V). For sweeping voltages below the SU8 breakdown voltage, the memory window increases almost linearly with increasing sweep voltages and becomes negligible for voltages below  $\pm 5$  V. However, at higher sweeping voltages (above  $\pm 15$  V), the memory window rises slightly sharper and reaches 6 V at  $\pm 30$  V due to the charge leakage induced by the soft breakdown in the SU8 dielectric strength. The fact that the center of the hysteresis is very close to the 0 V, makes the memory structures produced favorable for lower operating voltages. Subsequent measurements indicated that the typical results (Figure 5.6(b)) are repeatable after several rounds of re-testing. The charges stored in the SWCNTs floating gate (Q) can be estimated from  $Q = C_{\text{FB}} \times \Delta V_{\text{FB}}$ , where  $\Delta V_{\text{FB}}$  is the flatband voltage shift. This gives approximately  $9.15 \times 10^{11} \text{ cm}^{-2}$  charges stored in the SWCNTs floating gate for  $\pm 30$  V sweep voltage.

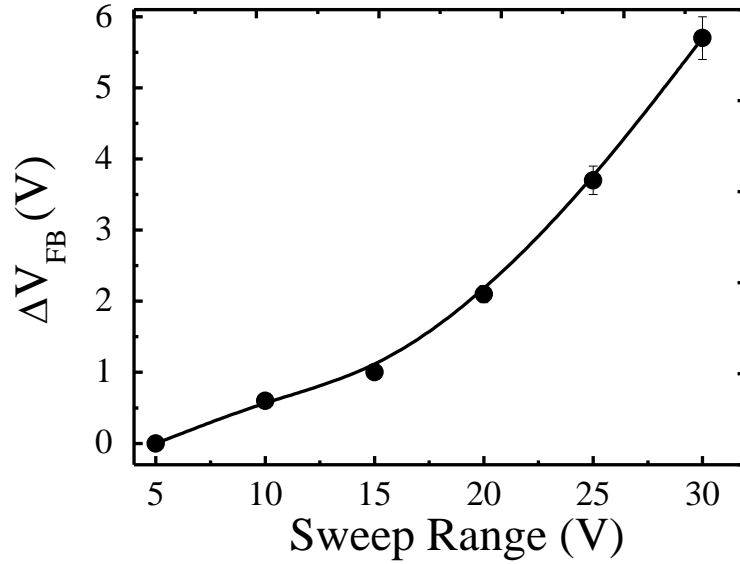


Figure 5.7: The plot of the memory window or the  $\Delta V_{FB}$  versus the increasing sweep voltages.

### 5.2.3.2 Hysteresis direction and charge injection

Unlike the hysteresis in the Al/PMMA/SWCNTs/PMMA/pentacene/Au devices which was analyzed in Section 5.2.2.2, the Al/SU8/SWCNTs/PMMA/pentacene/Au devices display a clockwise hysteresis. This indicates the positive flatband voltage shift in the C-V characteristics during the reverse voltage sweeps shown in Figure 5.6 (b). These results are consistent with the behavior of a p-type semiconductor (pentacene in this device) MIS structure where electrons are injected into the SWCNT floating gates from the Al electrode through the SU8 organic insulator. This could be due to the high resistivity of PMMA ( $10^{13} \Omega \cdot \text{cm}$  at  $10^6 \text{ V} \cdot \text{cm}^{-1}$  applied field) which prevents charges from tunneling from the pentacene through PMMA to the SWCNT floating gate [11]. And the shift of the flat band voltages toward positive values means that less electrons are needed for the structure to reach depletion and the flat band capacitance. This behaviour is attributed to the existence of trapped electrons in the floating gate. This occurs when a sufficient amount of negative bias is applied to the gate in the accumulation regime, electrons injected from the metal gate to the floating gate at sufficient voltages. A schematic diagram of the electron injection



from the gate towards the floating gate is shown in Figure 5.8 (b). Thus, when a clockwise hysteresis is observed in the C-V characteristics of memory devices, indicates that negative charges or electrons are trapped in the floating gate.

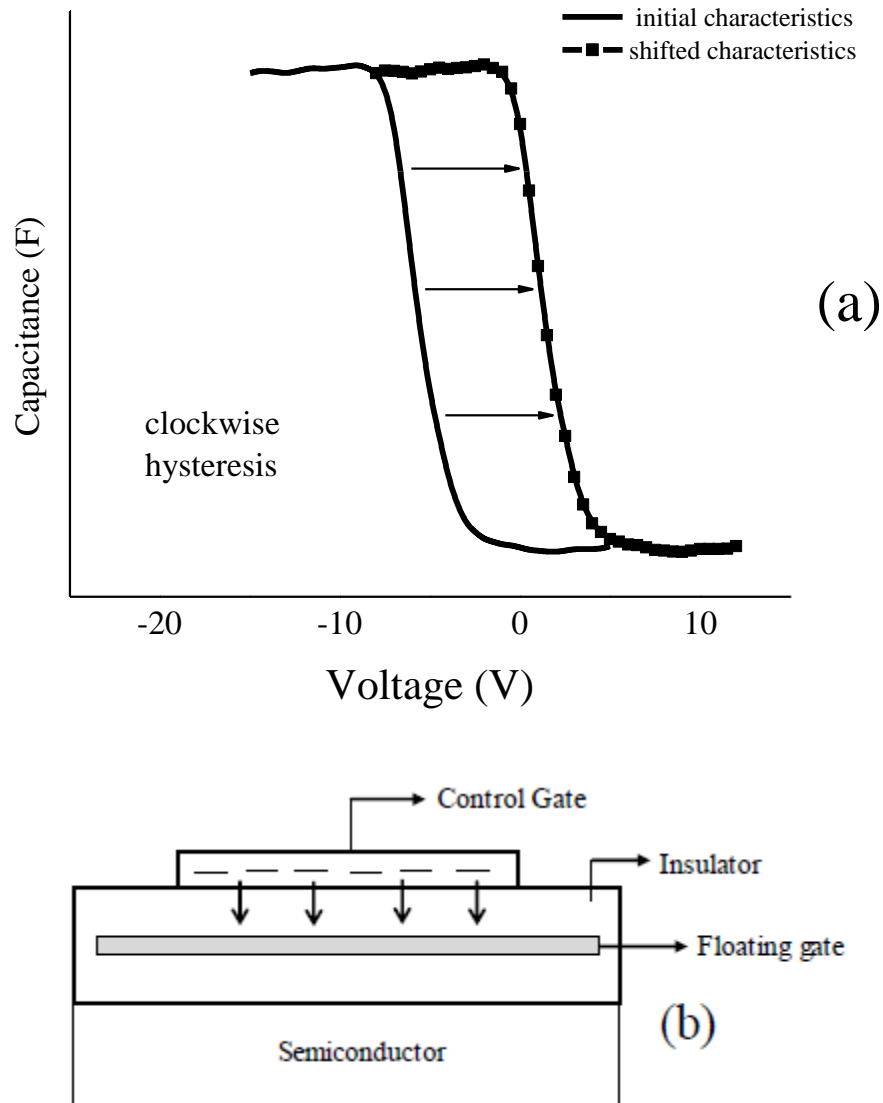


Figure 5.8: (a) The shift of the C-V characteristics of embedded MIS structure towards more positive values (b) Schematic diagram of electrons injection to floating gate.

We therefore believe that when a negative voltage (higher than the flatband voltage) is applied to the gate electrode, electrons are injected from the gate through the SU8 into the floating gate when the applied voltage approach the breaking down voltage of SU8 resulting in charging the SWCNTs layer. Equally, a higher positive gate voltage must be applied to reach depletion in the pentacene. Accordingly, the C-V curve in Figure 5.6 (b) is shifted towards more positive voltage.

### 5.2.3.3 Charge retention characteristics

The retention behavior of the MIS-based memory structures were observed by monitoring the capacitance with time after charging the device for a few seconds and then applying a stress voltage. Here, a two second -13 V pulse was applied to charge the memory device and the stress voltage was at 0 V where the two capacitance states exist. Over 94% of the charges trapped in the SWCNTs remained confined in the floating gate over the measurement time of more than 6 hours of continuous testing as shown in Figure 5.9. The relatively small change in the capacitance after six hours of continuous testing indicates that the MIS memory structure has a very good retention capacity and there is a very little leakage current in the MIS structure.

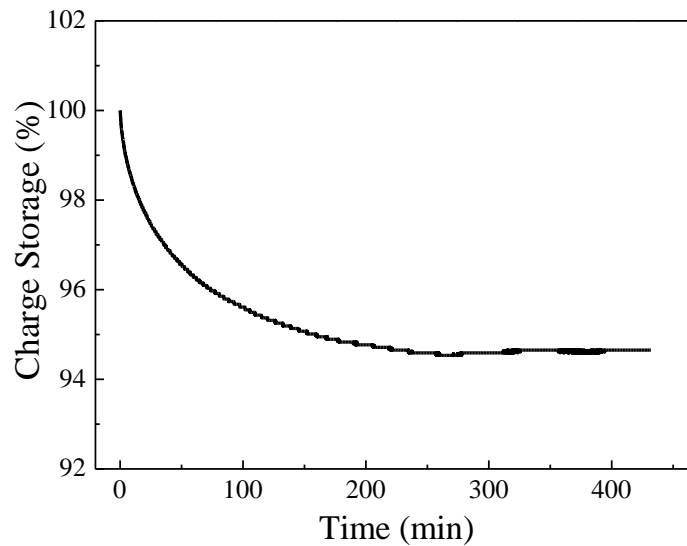


Figure 5.9: Charge retention characteristics of Al/SU8/SWCNTs/PMMA/Pentacene/Au memory devices

### **5.3. SWCNTs as charge traps in MIM memories**

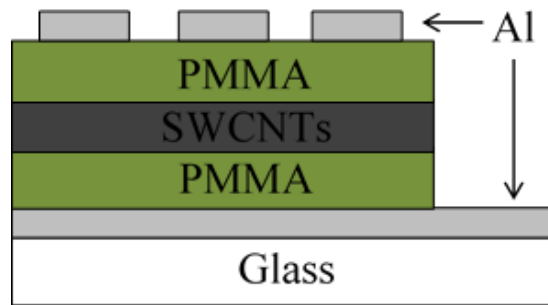
#### **5.3.1 Introduction**

Significant research has been devoted to developing organic bistable devices (OBDs) in the metal-embedded insulator-metal (MIM) structure utilizing inorganic nanoparticles embedded inside an organic insulator to form the charge storage stack [13-14]. These kinds of devices emerged as excellent candidates for non-volatile memory devices in organic and flexible electronics [15]. Low cost manufacturing, reliability as well as low operating power are the key drivers in the search for ideal data storage devices. Due to their exceptional properties and potential to achieve extremely high charge density, SWCNTs have attracted attention for the fabrication of memory devices. Previous efforts in integrating organic nanocomposites such as PCBM and graphene as charge traps in OBDs were attractive due to the simplicity of the structure and their easy fabrication methods [16-20].

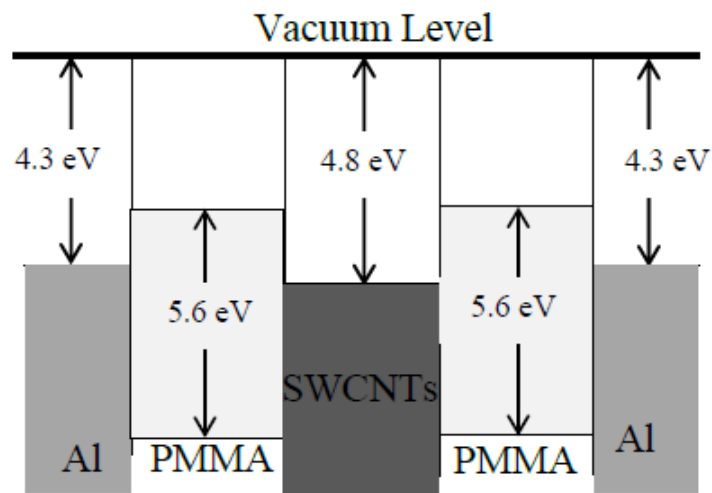
In this section, we present the fabrication and characterization of OBDs based on SWCNTs as charge storage nodes embedded between two PMMA insulating layers to form the active layer of the organic bistable memory devices. SWCNTs were deposited using the LbL technique, which ensures that the SWCNTs form a “thin-film” matrix. This technique will also ensure that the SWCNTs are confined between the bottom and top PMMA layers, allowing for switching behavior and the out of plane charge transport within the memory structure. The position of the charge traps in the middle of the insulating layer is believed to enhance the performance of the OBDs in terms of stability and retention [21]. PMMA was chosen as the insulator where the charge traps were embedded due to our previous knowledge about the low leakage current in PMMA under high gate voltages in metal-insulator-semiconductor and transistor structures [8, 9]. Furthermore, PMMA have been used as an insulator in similar structures (embedded with charge traps) and showed stability upon the applied voltages and reliability in the confinement of carriers inside the charge traps when the voltage was turned off [19]. Moreover, in our previous work on hybrid memory devices, charging and discharging of the charge elements were through a thin layer of PMMA (40 nm) [7]. The PMMA in this section will be hard backed for 75 min so the second layer will not affect the first thin film deposited as explained in section 5.2.4.

### 5.3.2 Device structure

A 100 nm thick aluminum (Al) bottom electrode was thermally evaporated on a glass substrate cleaned using the Piranha procedure. PMMA (20 wt% in chlorobenzene) was then spun coated to a thickness of 40 nm (6000 rpm for 50 s) and baked for 75 min at 120 °C in air at the cleanroom laboratory ambient humidity conditions. SWCNTs were deposited using LbL technique detailed in Chapter 3, and the structure of the SWCNTs matrix was deposited the same way as for the MIS devices explained in Section 5.2.1. A second layer of 40 nm PMMA was then deposited on the device to complete the SWCNTs encapsulation. Finally, the top Al electrode was thermally evaporated to finalize the fabrication of the device in a crossbar structure (Figure 5.10), with a surface area of 1 mm<sup>2</sup>. A schematic diagram of the fabricated structure is shown in Figure 5.10 (a). The structure ensures that the memory device benefit from the SWCNTs as a middle-trap-layer confined between two “thick” potential barriers (Figure 5.10 (b)). The band model depicted in Figure 5.10 (b) is used to explain the switching behavior in the I-V characteristics and carriers transport in the structure (Section 5.3.5). The device area was masked while the excess organic thin film was etched using oxygen plasma dry etching to reveal the Al bottom contact. A PC driven HP 4140b pA Meter/DC Voltage Source was used to record the current-voltage (I-V) characteristics of the devices with a scan rate of 0.2 V/sec. Each test consisted of a double sweep (positive – negative) at room temperature and laboratory conditions.



(a)



(b)

Figure 5.10: (a) schematic diagram and (b) band diagram of the Al/PMMA/SWCNTs/PMMA/Al memories.

### 5.3.3 Electrical Characterization

Figure 5.11 shows the I-V characteristics for an Al/PMMA/SWCNTs/PMMA/Al memory device in the linear scale (Figure 5.11(a)) and in the logarithmic scale (Figure 5.11(b)). The voltage applied to the device was split into two consecutive parts, a positive scan starting from 0 V towards 5 V and then back to 0 V, then a negative scan starting at 0 V towards -2.1 V and then back to 0 V. The I-V characteristics for the devices show clear electrical hysteresis behavior. Initially the device was in the low conductivity state (OFF state) during the positive scan. The conductivity of the device switches from its low conductivity to high conductivity (ON state) when the voltage exceeded a threshold voltage of 4.4 V, which represents the writing voltage. The high conductivity state was sustained even when the power was turned off (after sweeping back to 0 V) as shown in Figure 5.11. On the other hand, the negative scan causes the devices to switch from the ON to the OFF state; the transition to the OFF state was achieved by applying a reverse voltage of -2.1 V which represents the erase voltage. The maximum current ratio between the ON and OFF states for the tested devices is about  $2 \times 10^5$  using a low reading voltage of 1 V.

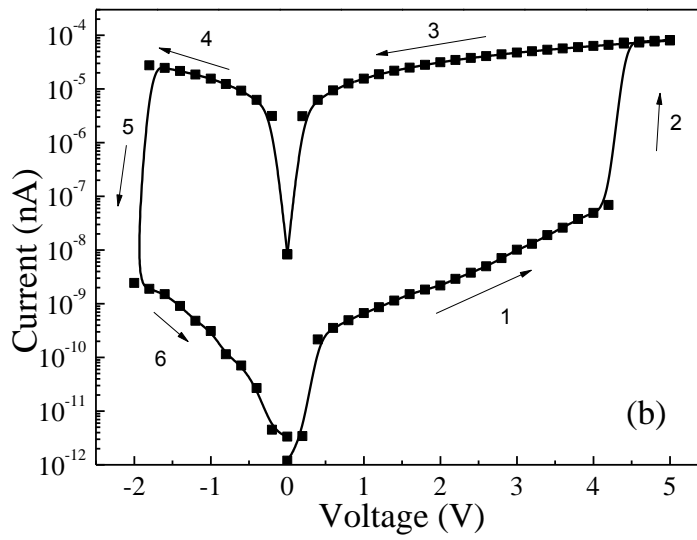
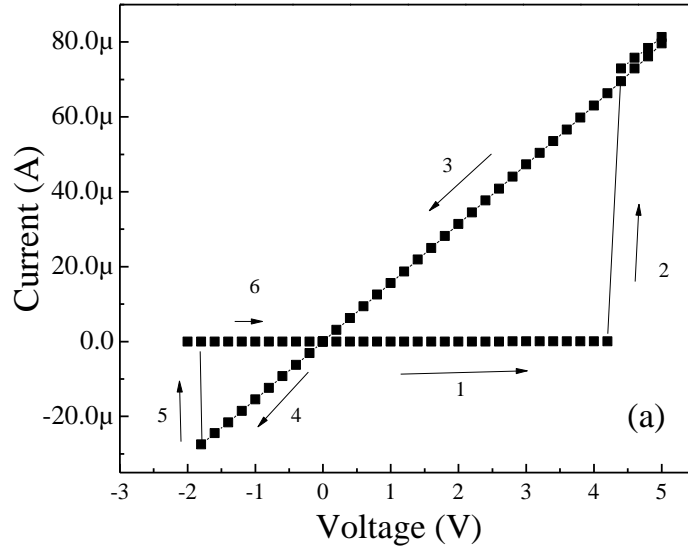


Figure 5.11: (a) I-V characteristics of the fabricated memories. (b) I-V characteristics in Log scale.

### 5.3.4 Retention characteristics

The stability and retention characteristics of the bistable memory devices were tested by monitoring the current in both ON and OFF states at a constant applied reading voltage of 3.5 V for more than 1000 seconds. The device was switched ON by applying a 1 second pulse of 4.5 V, then the retention of the ON state was recorded. The retention ability of the OFF state was also observed after switching the device back to the OFF state using a 1 second pulse of -2.1 V. The current-time characteristics of the ON and OFF states are shown in Figure 5.12, at a reading voltage of 3.5 V. The current maintained the original value of 40  $\mu$ A in the ON state, and 20 nA in the OFF state (representing a  $2 \times 10^3$  ON/OFF ratio at reading voltage 3.5 V). A systematic analysis of all the devices produced during this investigation showed that voltages of  $4.4 \pm 0.2$  V and  $-2.1 \pm 0.2$  V were sufficient to turn the device to its ON and OFF states respectively. In addition, the bistable behaviors of the devices were observed when the voltage sweep was repeated several times. The devices show reproducible memory behavior with a small shift to slightly lower voltages in the ON voltage after more than 25 measurements cycles. This kind of switching from ON to OFF and from OFF to ON states at different low voltages and the reliable retention characteristics make these devices potential candidates for applications in organic nonvolatile memory and in particular, where low power operation is a necessity.



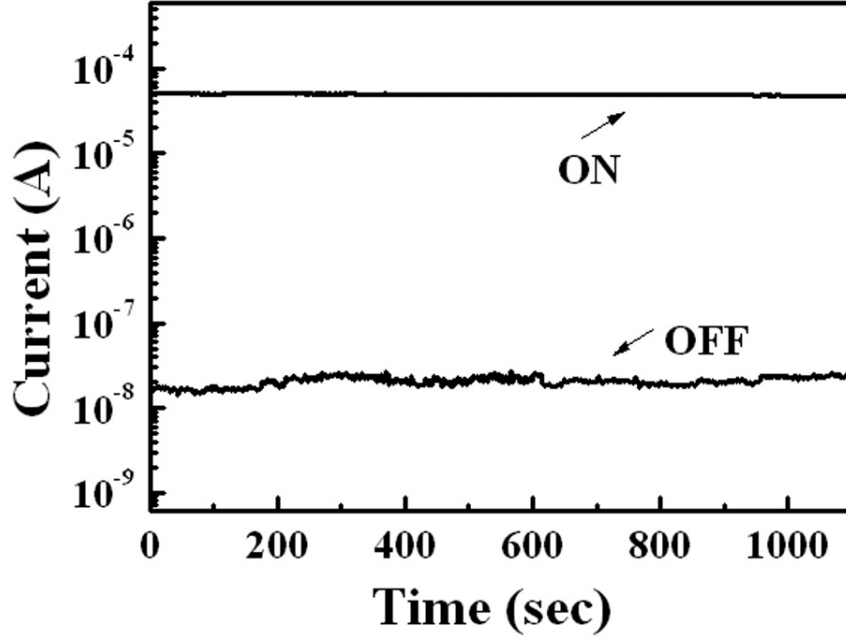


Figure 5.12: Retention of the ON and OFF states of the fabricated memories.

### 5.3.5 Switching behavior and carrier transport mechanism

In order to explain the memory behavior and the carrier transport mechanism of the fabricated devices, the I-V characteristics in Figure 5.11 were fitted using different conduction models (e.g. Poole-Frenkel, space charge limited conduction, Thermionic emission and Fowler-Nordheim Tunneling effect). The space charge limited conduction (SCLC) model showed the best fit to the data and thus was used to understand the carriers behavior in both the ON and OFF states of the devices. The current equation of the SCLC model is expressed by [12]

$$I_{SCLC} = \beta V^\alpha \quad (5.1)$$

where  $\beta$  is a constant and  $\alpha$  is the slope of the linear fitting of  $\ln(I)$  vs  $\ln(V)$ .

Figure 5.13 shows the  $\ln(I)$  vs  $\ln(V)$  plot for the data in Figure 5.11. The out-of-plane conduction mechanisms in the OFF and ON states, in both the positive (Figure 5.13(a)) and negative (Figure 5.13(b)) voltage scans were investigated. The data were fitted for the ON state and for the OFF state (before and after switching the device to the ON state). As

shown in Figure 5.13(a), the initial OFF state of the device in the positive scan (i.e. before switching to the ON state) can be divided into two distinct regions, which contributes to two different linear fitting behaviors. At voltages below 2.5 V in the initial OFF state, the slope of the fitting line is 1.33, which lies between the Ohmic conduction ( $\alpha = 1$ ) and the ideal case of SCLC ( $\alpha = 2$ ) and cannot really help understand the conduction mechanism. But the same region of the initial OFF state (i.e. below 2.5 V) shows an almost ideal fit to the thermionic emission model at which  $\ln(I)$  vs  $V^{1/2}$  exhibits a linear behavior as shown in the inset of Figure 5.13(a). This behavior shows that at low voltages electrons were accumulating at the barrier formed due to the potential profile between Al and PMMA and a thermionic conduction is taking place. This is consistent with similar behavior at similar potentials profiles in organic memory devices at low voltages [22]. As the voltage exceeds 2.5 V, the slope of the SCLC linear fitting increased gradually to 6.12 consistent with an increase in the number of charge carriers captured by the SWCNTs inside the PMMA. This high slope in the linear fitting of the SCLC is attributed to a conduction mechanism where the carriers are filling empty traps (SWCNTs) inside the out-of-plane medium (PMMA), the so-called trap-limited-SCLC [23]. After the transition to the ON state at 4.4 V, the I-V characteristics follow ohmic behavior: linear fitting of  $\ln(I)$  vs  $\ln(V)$  shows a slope equals 1 where the current is proportional to the applied voltage. Furthermore, this behavior extended into the ON state in the negative voltage scan; the slope of the linear fitting again is 1 as shown in Figure 5.13(b). There are several models been proposed to explain the switching in conductivity for such structures. Lauters et al (2006) suggested that the conduction mechanism in the ON state is due to the formation of a metallic filament within the PMMA stack at the transition state from OFF to ON states [24]. According to this model, a local conducting path with very low resistance is generated at high voltages allowing charges to be transported easily within the device. However, as only one third of SWCNTs are metallic while the other two thirds are semiconducting, it is very difficult to form a filament across the device structure. Therefore, we believe that the switching behavior is due to trapping and detrapping of electrons in the SWCNTs layer. Thus, in the ON state the carrier conduction in the devices follows an ohmic law which suggests that the SWCNTs were totally filled with injected electrons and the conduction mechanism follow a filled-traps SCLC [25].

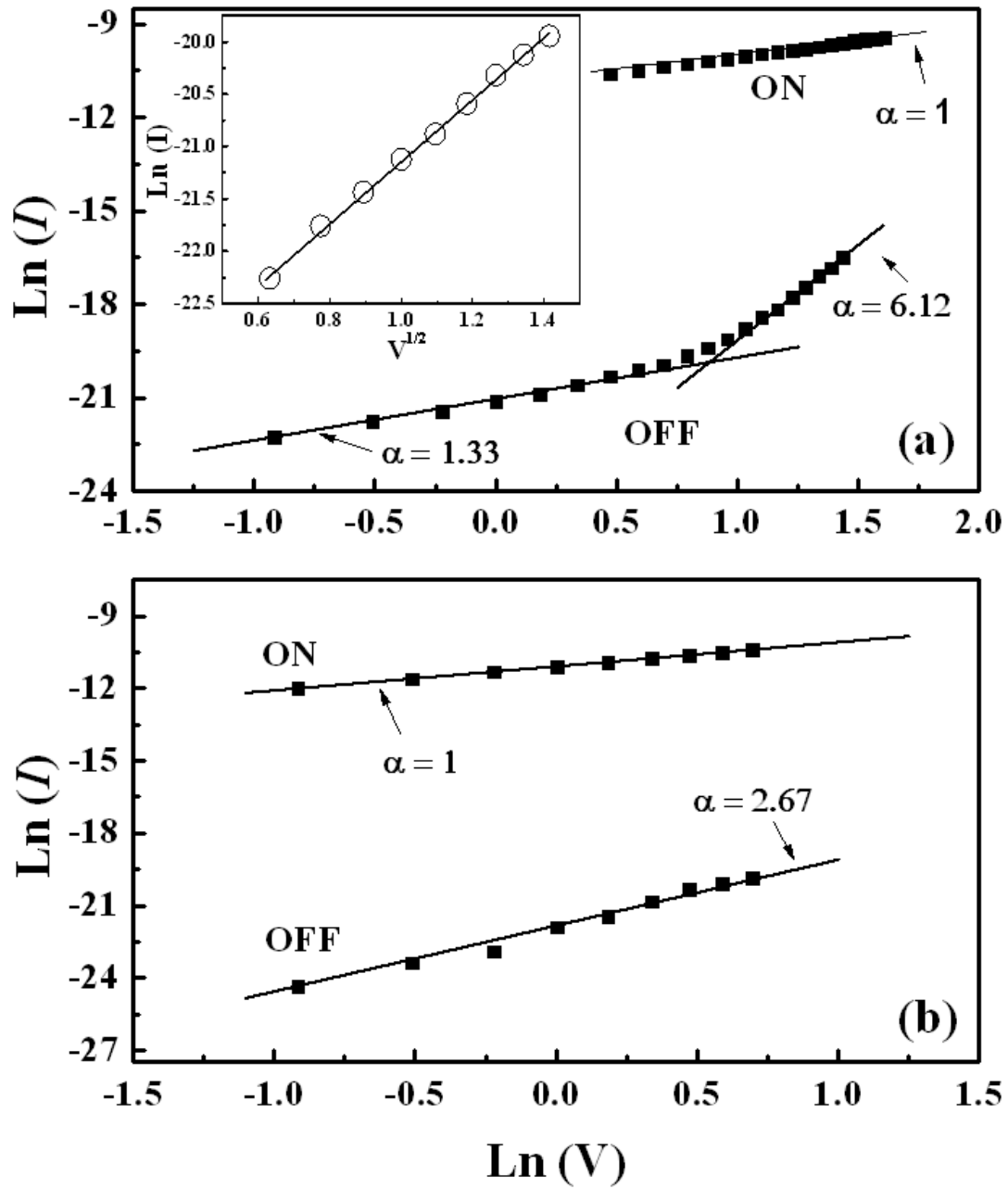


Figure 5.13: Ln-ln plots for the data in Figure 5.11 and fitting curves for the SCLC conduction mechanism during (a) positive and (b) negative voltage sweeps. Inset: Current versus square root of voltage at voltages below 2.5 V.

As electron capturing inside the SWCNTs layer no longer exists, as it is totally filled with electrons, the electrons flow is free from the influence of traps and electrons are able to reach the counter electrode much easier and thus the device conductivity switches to a high-conductance state (ON state). The current density ( $J$ ) in the ON state can be described using the equation  $J=qn_0\mu V/d$  where  $q$  is the electron charge,  $n_0$  is the density of free carriers,  $\mu$  is the electrons carrier mobility,  $V$  is the applied voltage and  $d$  is the thickness of the structure. This analysis is consistent with previously reported data that explains the electrical conduction in similar device structures, either using charge traps uniformly distributed within the volume of an organic insulator [21-25] or using charge traps in the middle of the insulator [26, 27], i.e. the charge traps separated with a thin film insulating layer from each of the metallic electrodes.

Consequently, when the device was turned OFF at -2.1 V, the electrons were detrapped from the SWCNTs. A linear fit with a slope of 2.65 for the SCLC model is observed (negative scan in Figure 5.13(b)). Similar to the OFF state in the positive scan, the current in this voltage range is attributed to the empty-traps SCLC mechanism, where the electrons being captured by the SWCNTs traps inside the PMMA rather than reaching the other electrode which explains the low-conductivity behavior of the devices. And the current density ( $J$ ) in the OFF state can be described using  $J=9\epsilon\epsilon_0\mu\Theta V^2/d^3$  [12] where  $\epsilon$  is the dielectric constant of PMMA,  $\epsilon_0$  is the free space permittivity and  $\Theta$  is the trapping fraction. Simplified band diagrams of the conduction mechanism of the devices in the OFF and ON states is depicted in Figure 5.14.

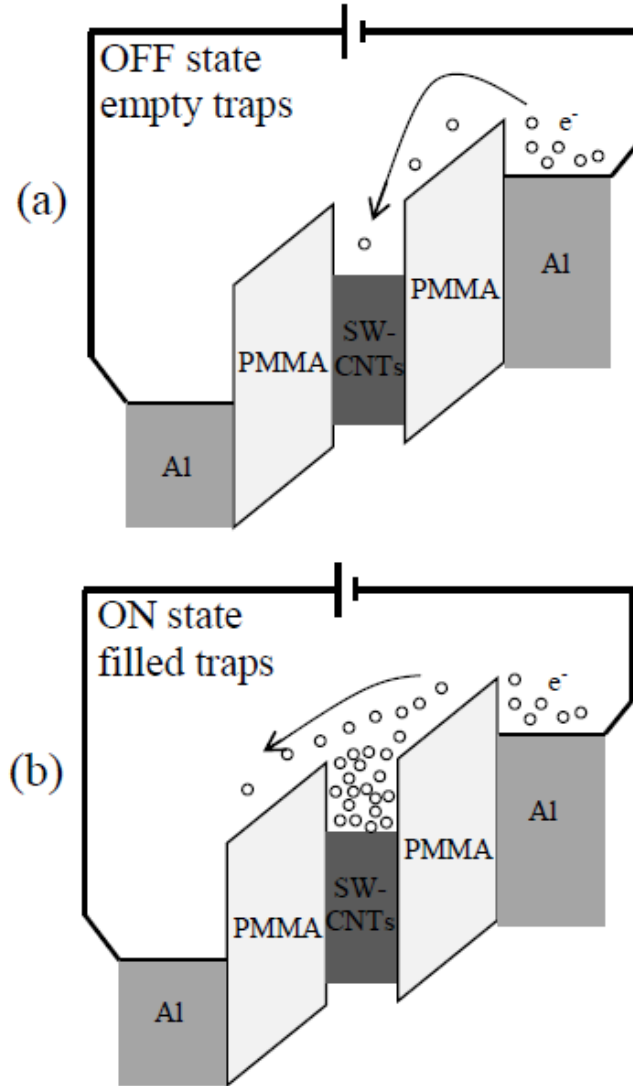


Figure 5.14: A simplified schematic of the band diagram and conduction mechanism of the devices in (a) the OFF state (traps empty) and (b) the ON state (traps filled).

In addition to the fitting of the I-V characteristics to the proposed conduction models in the ON and OFF states, we are able to extract the density of traps inside the device at the trap-filled voltage ( $V_{TFL}$ ); i.e. the switching voltage at which the traps are totally filled with electrons and the transition happens to the filled-traps conduction (4.4 V in our devices). The density of traps ( $N_t$ ), is given by [28]

$$N_t = \frac{3 \epsilon \epsilon_0 V_{TFL}}{2 q d^2} \quad (5.2)$$

using the dielectric constant of the PMMA to be between 2.89 and 3.66 [11], the density of SWCNTs charge traps inside the device was estimated to be between  $2.19 \times 10^{17} \text{ cm}^{-3}$  and  $2.78 \times 10^{17} \text{ cm}^{-3}$ .

Based on the above analysis, the conduction mechanism in the fabricated devices can be described as follows: the conduction mechanism in the initial OFF state follows a thermionic emission mechanism at low voltages where the electrons pass the potential barrier at the Al/PMMA interface and a trap-limited-SCLC at higher voltages where the SWCNTs trap the electrons (stage 1 in Figure 5.11). As the voltage is further increased to reach a threshold voltage where the SWCNTs traps are completely filled with electrons (stage 2 in Figure 5.11), the injected electrons flow independent of the traps influence and can easily reach the counter electrode and thus the device is switched to its ON state (stage 3 in Figure 5.11). On the other hand, a negative bias sufficient to de-trap the electrons will cause the filled states to become empty again and thus switch the device back to its OFF state (stage 5 in Figure 5.11).

#### **5.4. Summary**

In this chapter we presented the utilization of SWCNTs as charge storage nodes in two terminals ONVM. Two terminals ONVM benefit from the crossbar structure and their ability to be used in three dimensional memory stacks. SWCNTs were used as a floating gate in MIS memory and as charge traps in embedded MIM memory structures. The SWCNTs were deposited by LbL technique which results in a SWCNTs matrix and allows us to confine the traps between two insulating layers which optimizes the memory devices stability and retention characteristics.

In the MIS structures, two different devices using different insulators were fabricated. The first memory device uses PMMA as its gate insulator in the Al/PMMA/SWCNTs/PMMA/pentacene/Au structure while the other uses SU8 as its gate insulator in the Al/SU8/SWCNTs/PMMA/pentacene/Au structure. The fabricated memory devices structures and its extracted electronic parameters from its C-V characteristics is summarized in table 5.1.

Table 5.1: A summary of the fabricated MIS memory devices.

Memory device structure	Hysteresis direction	Charges stored	Charges injection	$\Delta V_{FB}$	Q	Charge retention
Al/PMMA/SWCNTs/PMMA/pentacene/Au	Anti-clockwise	Holes	Pentacene	8 V	$6.6 \times 10^{11} \text{ cm}^{-2}$	86%
Al/SU8/SWCNTs/PMMA/pentacene/Au	clockwise	electrons	Al gate	6 V	$9.15 \times 10^{11} \text{ cm}^{-2}$	94%

In the embedded MIM memory devices, an organic bistable device was fabricated benefitting from SWCNTs between two PMMA insulating layers (Al/PMMA/SWCNTs/PMMA/Al). The devices exhibit an electrical bistability and nonvolatile memory characteristics in terms of switching between ON and OFF states due to the application of positive and negative voltages, respectively. The retention characteristics showed two stable and distinct conduction states. The fabricated memory devices operate below 5V in terms of writing, reading, and erasing and have an ON/OFF ratio of  $\sim 2 \times 10^5$  at a 1 V reading voltage. The electrical bistability of the devices was attributed to the trapping and detrapping of electrons by SWCNTs.

The characteristics described in this work for two different memory structures clearly demonstrate the potential for SWCNTs to be used as storage elements in advanced non-volatile organic memory devices for flexible electronics. And it suggests the possibility for using simple and low cost structures for memory devices. Further work is needed on the long-term stability and write-read-erase endurance cycles of the devices.

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# Chapter 6

## AIO-based electrochemical metallization memories

### 6.1. Introduction

Filamentary based metal-insulator-metal (MIM) memory structures as explained in Section 2.3.2.1 is a part of resistive-based nonvolatile memory (NVM). This type of memory is also called resistive random access memory (RRAM) and exhibit resistive switching (RS) phenomena due to the formation and rupture of a metallic filament inside an oxide thin film. RS memory emerges as a reliable candidate for the next generation NVM devices [1]. The formation of the metallic filament under sufficient applied voltage occurs either due to the anionic migration of oxygen vacancies inside the thin film [2], or due to the cationic migration of the cations of an electrochemically active electrode (AE) inside the thin film [3]. NVM devices benefiting from RS due to cationic migration are usually known as electrochemical metallization cells (ECM). The structure of an ECM consists of an AE (usually Cu or Ag) which acts as a source of mobile cations, the switching medium (usually thin oxides [4], sulphides [5] or selenides [6] which acts as a thin film of solid electrolyte inside which the metal ions migrate, and an electrochemically inert counter electrode (CE) (usually Pt or W) where the cations get reduced to build up the metallic filament. As such, the mechanism of RS in an ECM is widely accepted [3-6] as a redox reaction which involves the oxidation of the AE atoms to produce mobile cations that migrate inside the thin film and are reduced at the CE to form a metallic filament inside the film in the ON state, and the dissolution and/or rupture of this metallic filament in the OFF state.

#### 6.1.1 Chapter overview

Aluminum oxide ( $\text{AlO}_x$ ) has been widely reported as a switching medium in different memory structures, which use ultra-thin  $\text{AlO}_x$  with Pt, Al, Ti, or TiN metal electrodes in the memory stack [7-9]. In these structures the formation of a filament is attributed to the anionic migration of oxygen vacancies inside the  $\text{AlO}_x$  thin film. In this chapter we report

on the mechanism for resistive switching in  $\text{AlO}_x$  ECM memories based on the cationic migration of electrochemically active copper (Cu). The switching medium ( $\text{AlO}_x$ ) have been used as the electrolyte inside which the Cu ions migrate.

The fabricated memory structures will be presented in section 2. Different memory devices with different counter electrodes will be used. The used counter electrodes will be Al, platinum palladium alloy (Pt/Pd), Au and Tungsten (W). Section 3 will present the electrical characterization of the devices using Al as a counter electrode. Section 4 and 5 will present the bipolar switching of the devices using Pt/Pd and Au as the CE, respectively. Section 6 will present RS in the devices using W, which exhibit the best and most reproducible and stable RS behavior. Its electrical characterization, conduction mechanism of the devices in the OFF state, formed filament shape, schottky barrier heights calculations, conduction mechanism of the devices in the ON state, filament resistance calculations and retention characteristics will be covered in Sections 6.6.1 to 6.6.7, respectively.

## **6.2. Memory devices structure**

Four memory devices structures will be fabricated with different CE metals. The metals will be used in the four different devices are: Al, Pt/Pd, Au and W. Except for the CE metal selection, all devices will be fabricated in the same structure and under the same fabrication conditions. The device structure, depicted schematically in Figure 6.1, was fabricated as follows: glass substrates were cleaned through successive ultrasonic treatments in acetone, methanol and isopropanol, then were rinsed with deionized water and dried with nitrogen flow. The bottom electrode or CE was deposited through the relevant deposition technique depending on the metal through a 1 mm wide shadow mask. A crystal monitor was used to estimate the thickness and rate of deposition; the acoustic impedance was changed for different metals deposited. Al was thermally evaporated to a thickness of 75 nm at a deposition rate of 0.2 nm/sec. Pt/Pd was sputtered in an argon plasma at a pressure of  $1.2 \times 10^{-2}$  mbar to a thickness of 75 nm. Au was thermally evaporated to a thickness of 75 nm at a deposition rate of 0.2 nm/sec, a very thin layer ( $\sim 5\text{nm}$ ) of chrome (Cr) was thermally

evaporated on the glass as a seed layer prior for the Au deposition. W was deposited using e-beam evaporation at a deposition rate of 0.1 nm/sec to reach the thickness of 75 nm. A 20 nm thick  $\text{AlO}_x$  was then deposited on the whole slide (except a small part to reach the bottom electrode contact) using e-beam evaporation at a deposition rate of 0.2 nm/sec. Finally, a thin layer of copper was sputtered through a 1 mm wide shadow mask in an argon plasma at a pressure of  $1.2 \times 10^{-2}$  mbar to a thickness of 50 nm with a deposition rate of 0.5 nm/sec to complete the  $\text{Cu}/\text{AlO}_x/\text{CE}$  device structure with an effective device area of  $1 \text{ mm}^2$ . The four fabricated devices were in the following structures:  $\text{Al}/\text{AlO}_x/\text{Cu}$ ,  $\text{PtPd}/\text{AlO}_x/\text{Cu}$ ,  $\text{Au}/\text{AlO}_x/\text{Cu}$  and  $\text{W}/\text{AlO}_x/\text{Cu}$ . The I-V characteristics of the fabricated devices were measured in air at room temperature using a PC driven HP 4140b pA Meter/DC Voltage Source with a scan rate of 50 mV/sec.

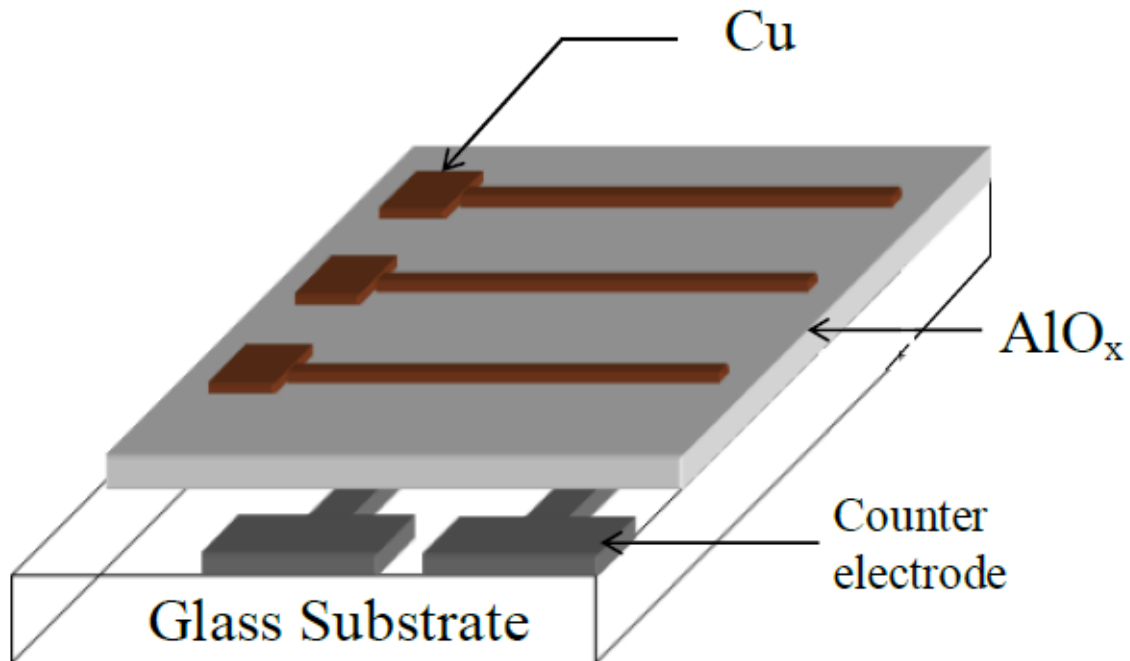


Figure 6.1: Schematic diagram of the fabricated ECM memory devices structure.

### **6.3. Memory devices using Al as the counter electrode**

The devices using Al as a CE in the Al/AIO<sub>x</sub>/Cu structure is the only structure between the four fabricated structure which exhibited both the unipolar and bipolar RS modes. All other devices were tested for both modes but none of the other structures was able to operate in the unipolar RS mode.

#### **6.3.1 Bipolar switching mode**

##### **6.3.1.1 Electrical characterization**

The I-V characteristics of the fabricated Al/AIO<sub>x</sub>/Cu memory devices are shown in Figure 6.2; the positive voltage is defined by the voltage applied at the Cu top electrode with the Al bottom electrode grounded, and vice versa for the negative voltage. Each test consists of a positive voltage sweep starting from 0 V reaching 3 V and back to 0 V with an applied current limit of 100 μA, followed directly with a negative voltage sweep starting from 0 V reaching -1.5 V and back to 0 V with no current limit applied. The current limit in the forward bias is applied to prevent a permanent damage of the device. On the other hand, the current limit is not applied in the reverse bias to ensure reversibility and to help reset the device to its initial state through resistive heating and rupture of the Cu filament. The positive voltage sweep show that the memory devices are initially in the high resistance state (OFF state) until a sufficient voltage is applied between 0.5 V and 2.5 V and the device switches to the state of low resistance (ON state) and reaches the current limit of 100 μA. The devices stay in the ON state when the power is turned off, i.e. when the voltage sweeps back to 0V. On the other hand, when a negative sweep is applied without a current limit, the devices at low negative voltages remain in its ON state, until it reaches a certain voltage between -0.5 V and -1.5 V where the device switches back to its initial OFF state. This kind of RS determines the nonvolatile memory characteristics of the devices, where a 2 V pulse (with the current limit applied) is sufficient to switch the devices to its ON state, i.e. the writing voltage; while a -1.5 V pulse (without a current limit applied) is sufficient

to switch the device back to its OFF state, i.e. the erasing voltage. A voltage range between 0.01 V and 0.5 V (with current limit applied) may be used to read the state of the device.

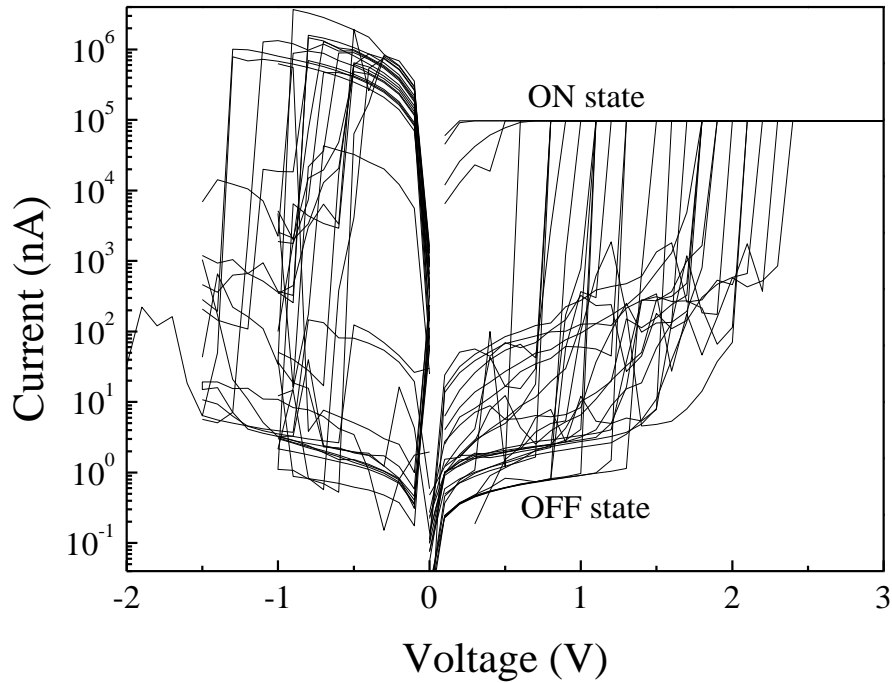


Figure 6.2: Consecutive bipolar resistive switching I-V cycles for Al/AIO<sub>x</sub>/Cu ECM memory cells.

The “SET” process, i.e. switching the device to the ON state, is achieved by applying a sufficient positive voltage to the AE where the Cu metal atoms get oxidized by the reaction  $\text{Cu} \rightarrow \text{Cu}^{2+} + 2\text{e}^-$ . The  $\text{Cu}^{2+}$  cations then migrate through the  $\text{AlO}_x$  and get reduced at the Al (CE) due to the reaction  $\text{Cu}^{2+} + 2\text{e}^- \rightarrow \text{Cu}$  and builds up the Cu filament that effectively short-circuits the  $\text{AlO}_x$  to provide a low resistance metallic path for electrons between the Cu electrode and the Al electrode, thus switching the device to the ON state. A schematic diagram that depicts the SET process is shown in Figure 6.3.

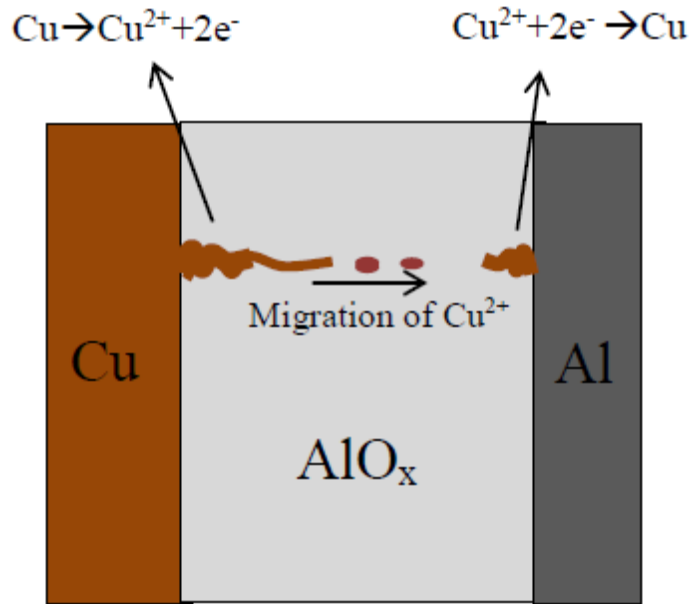


Figure 6.3: A schematic diagram of the SET process of the Al/AIO<sub>x</sub>/Cu devices.

The filament formation is likely to be formed in the less compact path through the AlO<sub>x</sub> thin film (void for example) and the ON state is achieved when the whole path is filled with copper atoms thus the conductive filament is achieved. The current limit of 100 μA is applied in the SET process in order to control the “short-circuit” of the AlO<sub>x</sub>, i.e. to control the filament to a minimum size in which it can be ruptured upon application of opposite polarity bias, otherwise a total damage of the device will occur and the “short-circuit” of the device will be irreversible. The initial SET process, known as the forming process, of a fresh device usually occurs at a higher applied voltage of the alternative SET processes, as shown in Figure 6.2 where the first cycle of the I-V characteristic has a shift to a higher SET voltage (~ 2.5 V). After the forming process at 2.5 V, and upon the ON/OFF cycling of the device, the consecutive SET processes exhibit a gradual shift towards lower voltages (2.5 V to 0.5 V). This shift towards lower voltages upon consecutive SET processes means that less voltage is needed to form the next Cu filament, which can be attributed to the Cu atoms residue left in the oxide film after the filament ruptured in the last RESET process. But the shift from 2.5 V to 0.5 V results in a very dispersed I-V characteristics upon the ON/OFF cycling of the devices which will affect the memory application of the device



especially in terms of the reading voltage. The dispersed I-V characteristics upon cycling will result in a lower range of reading voltage and thus results in the failure of the memory application upon repetitive usage of the memory. Ideally a non-dispersed I-V characteristics would be best for the device life-time. This is the main reason that different structures with different CE materials were fabricated to try to reduce the dispersion of the I-V characteristics upon cycling. The dispersion might be related to the role of oxygen vacancies at the Al/AlO<sub>x</sub> interface where the Al might reduce the AlO<sub>x</sub> upon the applied voltage and inhibit the Cu atoms from nucleation at the same path and thus different sites of nucleation will be formed and thus the I-V characteristics will be dispersed.

The relatively low forming voltage in the device in Figure 6.2 compared to other AlO<sub>x</sub> based RS memories is due to the fabrication parameters. The AlO<sub>x</sub> in the device in Figure 6.2 is deposited using e-beam evaporation rather than the atomic layer deposition technique that is commonly used to deposit very compact thin film. The density of the solid-electrolyte interface in such structures is always influence the formation process of the copper filament, especially in structures that uses bilayer solid electrolytes [10]. Also, the large area of our devices (1 mm<sup>2</sup>) increases the number of injected Cu<sup>2+</sup> inside the AlO<sub>x</sub> and thus reducing the forming voltage.

On the other hand, the “RESET” process in bipolar RS mode takes place when a voltage of opposite polarity is applied leading to the dissolution and/or rupture of the metallic filament, and hence switching the device from the ON state to the OFF state. In the RESET process the current limit is not applied and thus in addition to the electrochemical dissolution of the filament due to the reverse bias, resistive heating effects cause a thermal breakdown of the filament when the current reaches a value of more than 100 μA (the applied current limit in the SET process) and therefore causing the device to return to the OFF state.

## 6.3.2 Unipolar switching mode

### 6.3.2.1 Electrical characterisation

The Al/AIO<sub>x</sub>/Cu memory structure exhibited also the unipolar RS mode. The I-V characteristics of the one SET-RESET cycle in the unipolar RS mode of fabricated memory devices shown in Figure 6.4 (a), the I-V characteristics of the same memory device upon consecutive SET and RESET cycles are shown in Figure 6.4 (b). Unlike the bipolar RS mode, each test consists of two consecutive positive voltage sweeps: one sweep starts from 0 V reaching 2.5 V and back to 0 V with an applied current limit of 100  $\mu$ A, followed directly with another positive voltage sweep starting from 0 V reaching 2 V and back to 0 V with no current limit applied. Again, the current limit in the first sweep is applied to prevent a permanent damage of the device while it is not applied in the second sweep to ensure reversibility and to reset the device to its initial state through resistive heating and rupture of the Cu filament. The first voltage sweep (Figure 6.4 (a)) shows that the memory devices are initially in the high resistance state (OFF state) until a sufficient voltage is applied between 1 V and 2 V and the device switches to the state of low resistance (ON state) and reaches the current limit of 100  $\mu$ A. The devices stay in the ON state when the voltage sweeps back to 0V. In the second sweep without a current limit, the devices at low voltages remain in its ON state, until it reaches a certain voltage between 0.5 V and 1.5 V where the device exceeds the 100  $\mu$ A and switches back to its initial OFF state. This kind of RS determines the nonvolatile memory characteristics of the devices, where a 2 V pulse (with the current limit applied) is sufficient to switch the devices to its ON state, i.e. the writing voltage; while a 1 V pulse (without a current limit applied) is sufficient to switch the device back to its OFF state, i.e. the erasing voltage. A voltage range between 0.01 V and 0.5 V (with current limit applied) may be used to read the state of the device. This is the main feature of the unipolar RS mode, where the same polarity voltage enables the device to be SET and RESET. The only difference is that a current limit is applied in the SET process while no current limit is applied in the RESET process. The problem with dispersion of the I-V characteristics upon consecutive SET-RESET cycles still exists in the unipolar mode and is clear in Figure 6.4 (b).

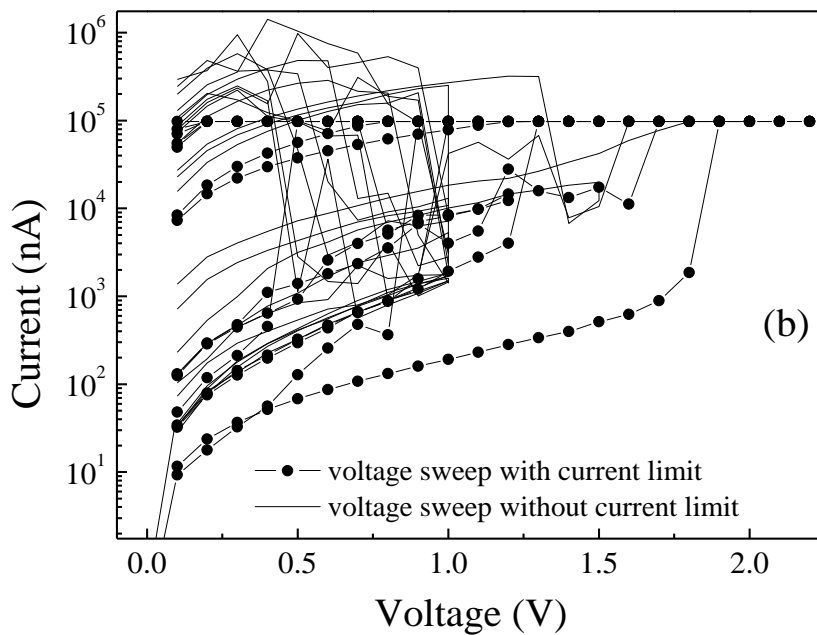
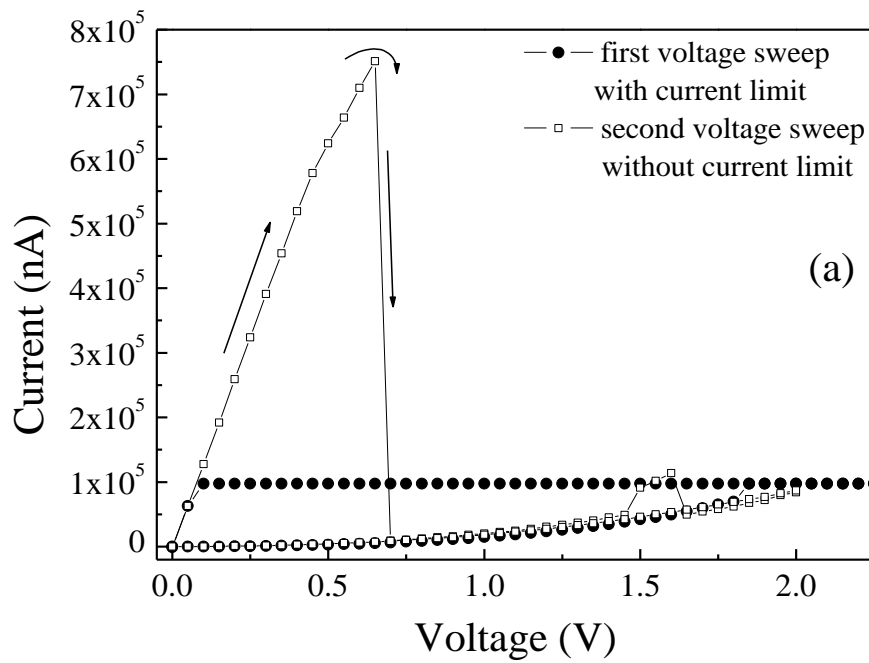


Figure 6.4: (a) Unipolar I-V resistive switching of Al/AlO<sub>x</sub>/Cu in the linear scale and (b) consecutive unipolar resistive switching I-V cycles.

In the unipolar RS mode, the SET process is exactly the same to that in the bipolar mode where the Cu atoms get reduced and then oxidized at the CE to form a metallic filament due to purely electrochemical reactions inside the electrolyte.

On the other hand, the RESET process in the unipolar mode is totally different than the bipolar mode. In the bipolar mode an opposite polarity is applied to reverse the electrochemical process that appeared in the SET process, the current limit is also removed to help the electrochemical dissolution through resistive joules effect heating. While in the unipolar RS mode, the RESET process depend only on the resistive joules effect heating to rupture the thin filament formed in the SET process. No electrochemical dissolution of the filament due to reverse polarity happens. Only the removal of the current limit in the RESET process will ensure that the current at the same applied bias polarity will reach much higher values than the formed filament is able to withstand and thus will rupture due to Joules resistive heating effect and switch back to its OFF state.

### **6.3.3 Retention characteristics**

The stability of the Cu filament in the unipolar and bipolar RS mode was studied through recording the retention characteristics of the devices. The device operating in the unipolar RS mode was switched ON using a 2 seconds long pulse at a voltage of 2 V with the application of a current limit and OFF using a 2 seconds long pulse at a voltage of 1.5 V without the current limit. The current was recorded versus time at a reading voltage as low as 0.05 V for both the ON and OFF states. The current maintained a value of 40  $\mu\text{A}$  in the ON state and a value of 3  $\mu\text{A}$  in the OFF state for more than  $10^3$  sec, as shown in Figure 6.5 (a).

The device operating in the unipolar RS mode was switched ON using a 2 seconds long pulse at a voltage of 3 V with the application of a current limit and OFF using a 2 seconds long pulse at a voltage of -1.5 V without the current limit. The current was recorded versus time at a reading voltage of 0.5 V for both the ON and OFF states. The current maintained a value of 100  $\mu\text{A}$  (the applied current limit) in the ON state and a value of 40 nA in the OFF state for more than  $10^3$  sec, as shown in Figure 6.5 (b).

The characteristics shows a reliable retention in the ON and OFF states of the Al/AlO<sub>x</sub>/Cu memory devices in both the bipolar and unipolar RS modes, but the dispersion of the I-V characteristics is still non-ideal for its memory application.

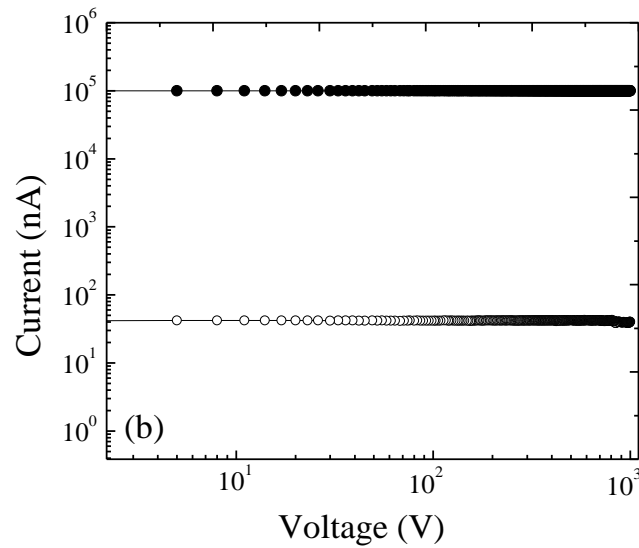
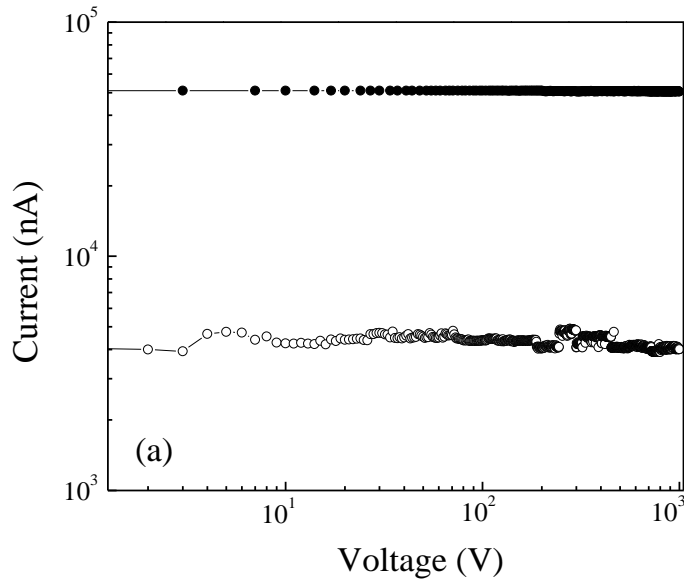


Figure 6.5: Retention characteristics of the Al/AlO<sub>x</sub>/Cu memory device in the ON and OFF states after consecutive (a) unipolar switching and (b) bipolar switching cycles.

## 6.4. Memory devices using PtPd as a counter electrode

### 6.4.1 Electrical characterization

In order to optimize the Al/AlO<sub>x</sub>/Cu ECM structure in terms of I-V characteristics dispersion upon consecutive cycles another counter electrode which does not react easily with oxygen was used. And thus upon the applied voltage it does not reduce the AlO<sub>x</sub> and result in oxygen vacancies in the AlO<sub>x</sub>. The use of Pt as a counter electrode is widely used in the literature due to its free energy where it does not get easily oxidized [1-10]. In this experiment an alloy of Pt and Pd which are both not easily oxidized have been used. Thus the fabricated ECM memory was in the form of PtPd/AlO<sub>x</sub>/Cu.

The I-V characteristics of the fabricated PtPd/AlO<sub>x</sub>/Cu memory devices upon consecutive cycling are shown in Figure 6.6. Each test consists of a positive voltage sweep starting from 0 V reaching 3.5 V and back to 0 V with an applied current limit of 100 μA, followed directly with a negative voltage sweep starting from 0 V reaching -2 V and back to 0 V with no current limit applied. The memory devices are initially in the OFF state until a sufficient voltage is applied between 0.25 V and 3 V and the device switches to the ON state and reaches the current limit of 100 μA. The devices stay in the ON state when the power is turned off and at low negative voltages until it reaches a certain voltage between -1 V and -2 V where the device switches back to its initial OFF state.

As shown in Figure 6.6, the problem of the dispersion of the WRITE voltage in the consecutive cycles was not solved in the adopted structure. Instead, it got worse as compared to the Al/AlO<sub>x</sub>/Cu structure (Figure 6.2). In the Al/AlO<sub>x</sub>/Cu structure the dispersion of the WRITE voltage was between 0.5 V and 2.5 V, while the dispersion in the PtPd/AlO<sub>x</sub>/Cu structure is between 0.25 V and 3 V. Although the PtPd alloy does not react with oxygen, but it provides two materials with two different affinities, free energy and thus two different sites of nucleation of Cu where the  $\text{Cu}^{2+} + 2\text{e}^- \rightarrow \text{Cu}$  reduction reaction can happen. Therefore different filaments get formed on different materials and dispersed the I-V curves and the results were similar to the dispersion due to oxygen vacancies.

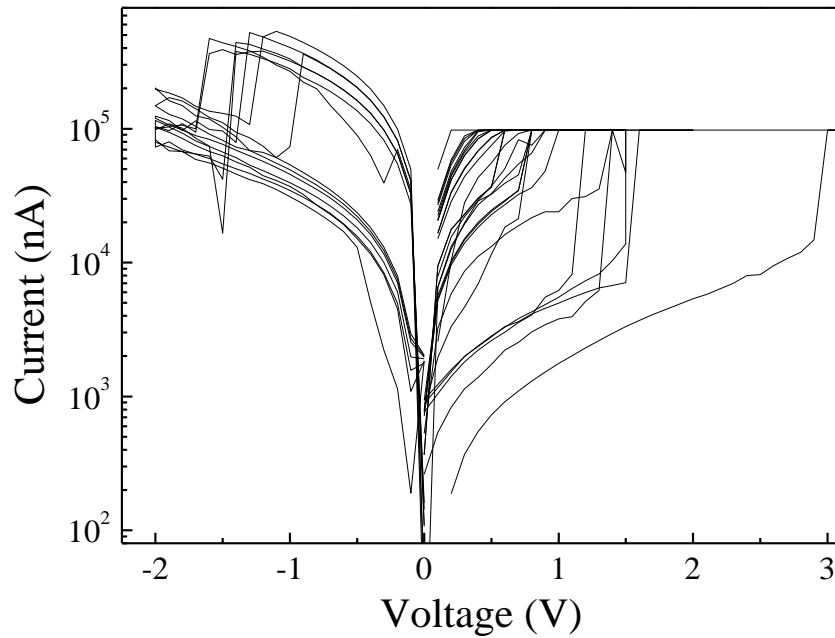


Figure 6.6: Consecutive bipolar resistive switching I-V cycles for PtPd/AlO<sub>x</sub>/Cu ECM memory cells.

## 6.5. Memory devices using Au as a counter electrode

### 6.5.1 Electrical characterization

Another ECM memory structure was fabricated to enhance the AlO<sub>x</sub> based memory in terms of the I-V characteristics dispersion upon consecutive cycles. The fabricated ECM memory used Au as a CE and was in the Au/AlO<sub>x</sub>/Cu structure.

The I-V characteristics of the fabricated Au/AlO<sub>x</sub>/Cu memory devices upon consecutive cycling are shown in Figure 6.7 (a). Similar to the characterization of the other memories, each test consists of a positive voltage sweep starting from 0 V reaching 3 V and back to 0 V with an applied current limit of 100 μA, followed directly with a negative voltage sweep starting from 0 V reaching -3 V and back to 0 V with no current limit applied. The memory devices are initially in the OFF state until voltage is applied between 1.25 V and 2.25 V and the device switches to the ON state and reaches the current limit of 100 μA. As shown

in Figure 6.7 (a), the problem of the dispersion of the WRITE voltage in the consecutive cycles was much improved in the Au/ $\text{AlO}_x$ /Cu. Compared to the Al/ $\text{AlO}_x$ /Cu structure (Figure 6.2) the dispersion of the WRITE voltage was between 0.5 V and 2.5 V, while the dispersion in the PtPd/ $\text{AlO}_x$ /Cu structure (Figure 6.6) is between 0.25 V and 3 V; while the dispersion in the Au/ $\text{AlO}_x$ /Cu structure was reduced to less than 1V.

On the other hand, another kind of failure appeared in the Au/ $\text{AlO}_x$ /Cu memory devices upon consecutive cycling. The devices didn't stay in the ON state when the power is turned off or at low negative voltages as shown in Figure 6.7 (b). This problem is much worse than the WRITE voltage dispersion problem because it results in the failure of the memory device function in terms of READ, WRITE and ERASE operations. The problem may be due to the imperfect interface that usually occurs between Au and oxides where a chrome adhesion layer should be introduced. Thus the built filament doesn't stay stable and does not nucleate well on the Au/oxide interface and thus the low resistance state is lost upon turning the bias to 0 V.



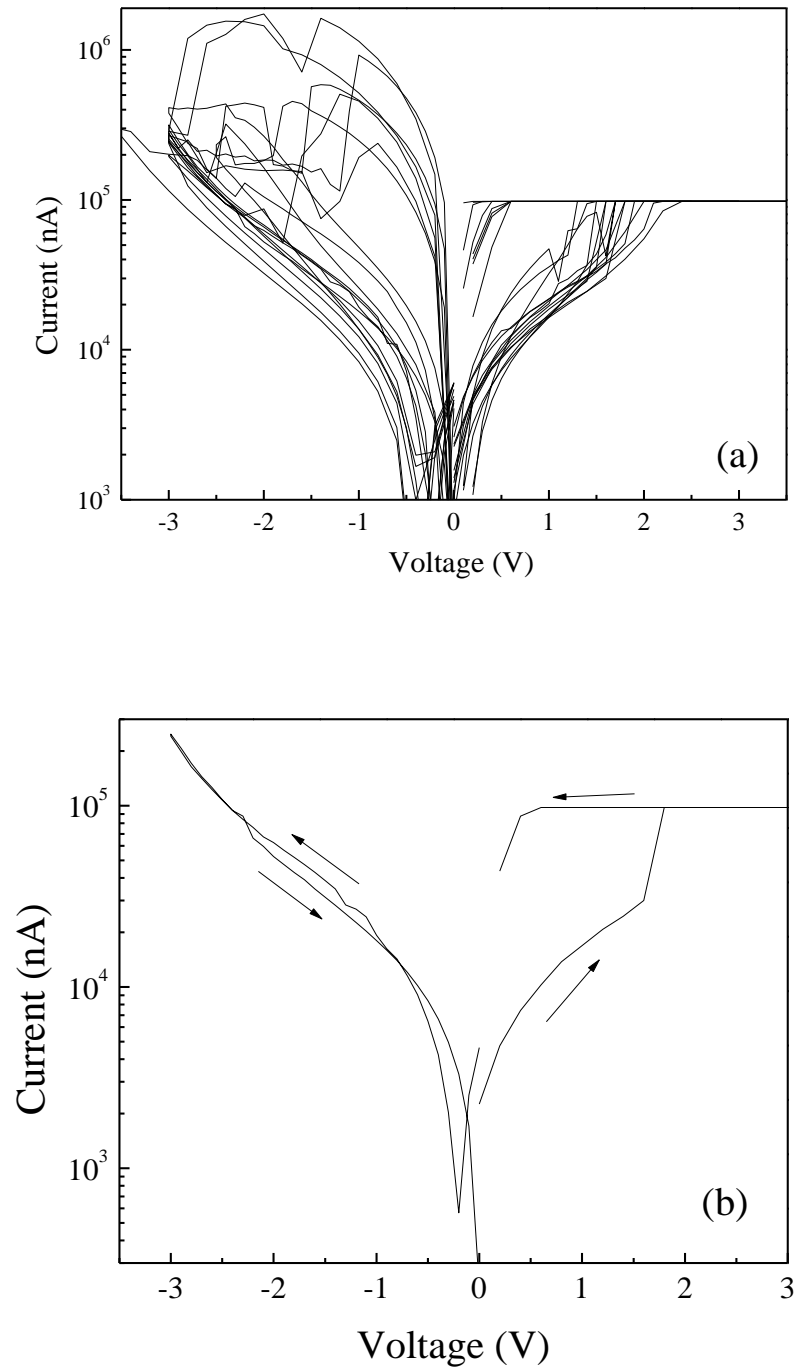


Figure 6.7: (a) Consecutive bipolar resistive switching I-V cycles for Au/AlO<sub>x</sub>/Cu ECM memory cells. (b) Failure of the Au/AlO<sub>x</sub>/Cu ECM to stay in the ON state upon the negative voltage sweep.

## 6.6. Memory devices using W as a counter electrode

### 6.6.1 Electrical characterization

Another fabricated ECM memories used W as a CE and was in the form of W/ $\text{AlO}_x$ /Cu structure. The I-V characteristics of the fabricated memory devices are shown in Figure 6.8. Each test consists of a positive voltage sweep starting from 0 V reaching 2 V and back to 0 V with an applied current limit of 100  $\mu\text{A}$ , followed directly with a negative voltage sweep starting from 0 V reaching -1.5 V and back to 0 V with no current limit applied. The I-V characteristics for all devices exhibit a clear RS behavior. The positive voltage sweep shows that the memory devices are initially in the high resistance state (OFF state) until a sufficient voltage is applied ( $1.3 \pm 0.05$  V) and the device switches to the state of low resistance (ON state) and reaches the current limit of 100  $\mu\text{A}$ . The devices stay in the ON state when the power is turned off, i.e. when the voltage sweeps back to 0V. On the other hand, when a negative sweep is applied without a current limit, the devices at low negative voltages remain in the ON state, until it reaches a certain voltage ( $-0.75 \pm 0.1$  V) where the device switches back to its initial OFF state. This kind of RS determines the nonvolatile memory characteristics of the devices, where a 2 V pulse (with the current limit applied) is sufficient to switch the devices to ON state, i.e. the writing voltage; while a -1.5 V pulse (without a current limit applied) is sufficient to switch the device back to the OFF state, i.e. the erasing voltage. A voltage range between 0.01 V and 1 V (with current limit applied) may be used to read the state of the device. As can be shown in Figure 6.8, the dispersion problem of the WRITE voltage was reduced compared to the structures using Al or PtPd as a CE, plus no failure in staying in the ON state as compared to the structures using Au as a CE.

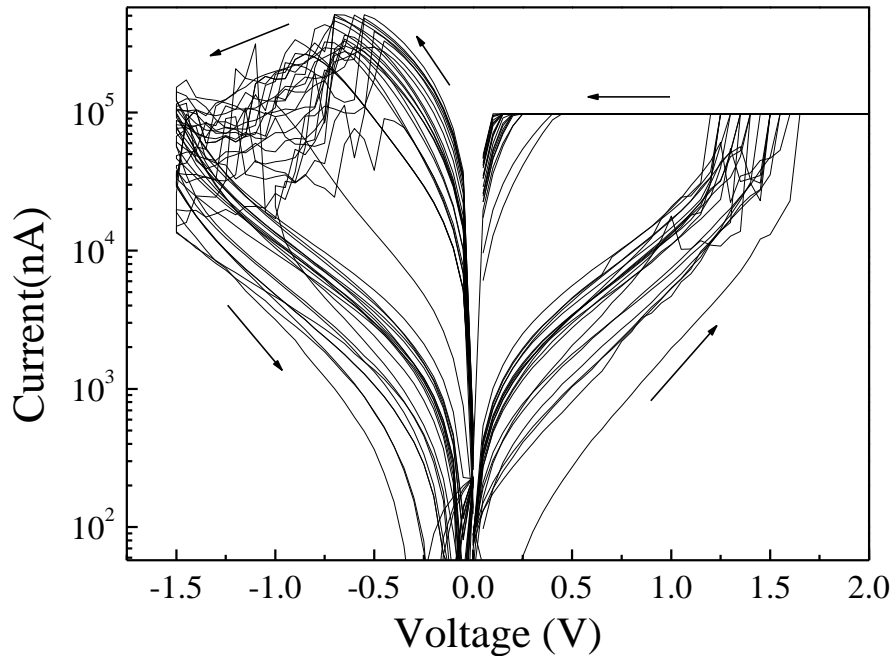


Figure 6.8: Consecutive bipolar resistive switching I-V cycles for W/AlO<sub>x</sub>/Cu ECM memory cells.

After the forming process at 1.7 V, and upon the ON/OFF cycling of the device, the consecutive SET processes exhibit a gradual shift towards lower voltages (1.6 V to 1.3 V). This shift towards lower voltages is negligible compared to the dispersion that happened in the Al/AlO<sub>x</sub>/Cu and PtPd/AlO<sub>x</sub>/Cu devices.

### 6.6.2 Conduction mechanism of the devices in the OFF state

The filament shape in oxide-based ECMs is believed to be conical with its vertex at the CE and thus the rupture of the filament is believed to happen at its weakest point, the electrolyte/CE anodic interface. Another hypothesis suggests that the shape of the filament might be cylindrical and the rupture might occur at any weak point throughout the whole filament length. The rupture of the filament is directly related to the conduction mechanism in the OFF state. The I-V characteristics of the devices in the OFF state, i.e. the behavior before switching to ON state and after switching back to OFF state, are shown in Figure

6.9 (a). The symmetric shape of the I-V characteristics in the OFF state can be related to the filament rupture through the conduction mechanism. To further analyze the conduction mechanism of the memory devices, the I-V characteristics in Figure 6.9 (a) were fitted to different conduction models (Fowler-Nordheim tunneling, trap-assisted space-charge-limited-current, Pool-Frenkel and Thermionic emission model). The best linear fitting was found to be to  $\log(I)$  vs  $V^{1/2}$  characteristics as shown in Figure 6.9 (b); which indicates that the conduction in the OFF state follows the Thermionic Conduction (TC) model where [11]

$$I \propto A^*T^2 \exp \left[ -\frac{q\phi}{kT} + q \left( \frac{q^3V}{4\pi\epsilon} \right)^{1/2} \right] \quad (1)$$

where  $A^*$  is the effective Richardson,  $T$  is the absolute temperature,  $q$  is the electron charge,  $\phi$  is the barrier height,  $k$  is the Boltzmann constant and  $\epsilon$  is the dielectric constant.

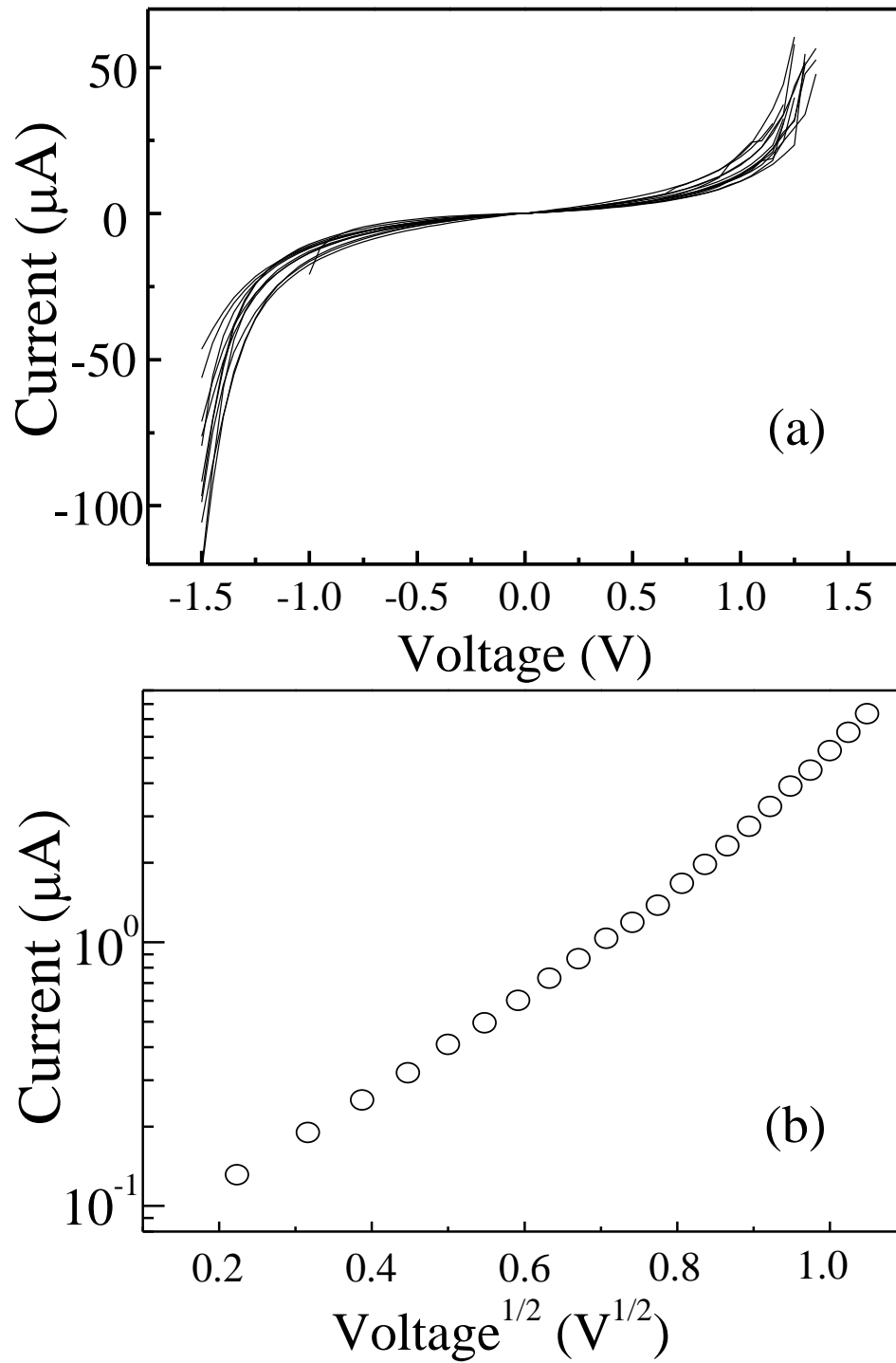


Figure 6.9: (a) The I-V characteristics of the devices in the OFF state; (b)  $\text{Log}(I)$  vs  $V^{1/2}$  fitting of the I-V characteristics in the OFF state.

This behavior explains the conduction inside the devices in the OFF state through a rectifying behavior which can be modeled, in theory, as a Schottky barrier. Schottky barriers usually occur at the metal-semiconductor interface due to the difference between the work function of the metal and the Fermi level of the semiconductor. In our memory structure, the OFF state takes place due to the rupture of the Cu filament which will result in a very thin (few nanometers) insulator between two metals (i.e. Cu-very thin  $\text{AlO}_x$ -Cu structure). The very thin insulating layer between the two metals allows the charges to tunnel through the insulator and thus the rectifying behavior of the I-V characteristics can be represented as a schottky barrier between the Cu and the very thin layer of  $\text{AlO}_x$ .

### 6.6.3 Filament shape

The shape of the I-V characteristics plays a crucial role in the understanding of the conduction of the device in the OFF state. The symmetrical shapes of the I-V characteristics in the positive and negative scans show that the conduction in the devices behaves as equal back-to-back Schottky barriers. In our device structure, the equal back-to-back Schottky barriers indicate that the device structure in the OFF state consists of  $\text{Cu}/\text{AlO}_x/\text{Cu}$  and W acts as an external conductor connected to the new Cu “filament electrode” (Figure 6.10 (a)). Such behavior shows that the rupture of the filament, which occurs due to the thermal resistive heating when the current exceeds the limit that the filament can withstand, occurs at any weak point through the filament length (Figure 6.10 (a)). If the rupture takes place at the  $\text{AlO}_x/\text{W}$  interface, the structure of the device in the OFF state would be  $\text{Cu}/\text{AlO}_x/\text{W}$  and will exhibit asymmetrical I-V characteristics (Figure 6.10 (b)). This behavior is expected due to the difference in the work functions between W (4.91 eV) and Cu (4.46 eV). The  $\text{AlO}_x/\text{W}$  interface would result in a Schottky barrier of 1.31 eV while the  $\text{AlO}_x/\text{Cu}$  barrier height is 0.86 eV [12-14]. The non-equal back-to-back Schottky barriers of the  $\text{Cu}/\text{AlO}_x/\text{W}$  structure expected to have asymmetrical I-V characteristics as the current will be dominated by one barrier, which is not the case in our devices. Simplified not-to-scale schematic diagrams for both cases are shown in Figure 6.10 (a, b).

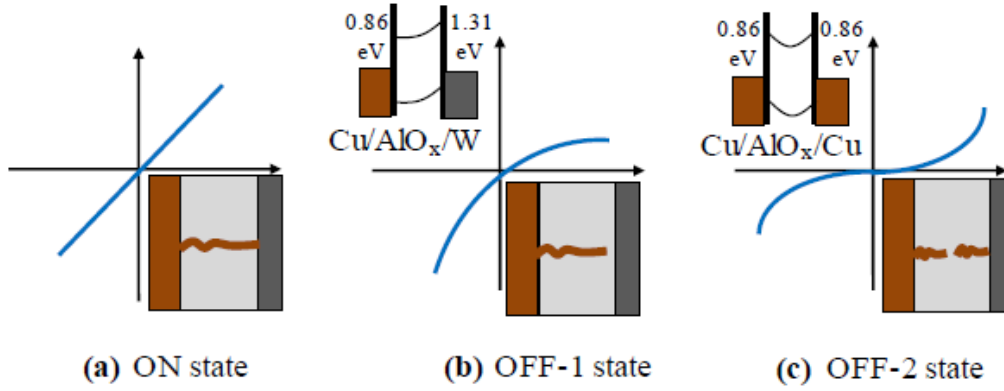


Figure 6.10: Possible shapes of the I-V characteristics of the RS cells in the OFF states.

#### 6.6.4 Schottky barrier heights calculations

The TE conduction model is also used to calculate the back-to-back Schottky barrier heights in the OFF state. The saturation current in the TE conduction model is given by [15]

$$I_0 = AA^*T^2 \exp\left(\frac{-q\phi_{b0}}{kT}\right) \quad (2)$$

A is the device area,  $A^*$  is the effective Richardson constant of  $\text{AlO}_x$ ,  $\phi_{b0}$  is the zero bias barrier height. The saturation current ( $I_0$ ) can be derived from the intercept at  $V=0\text{V}$  of the extrapolated linear regime of the  $\ln(I)$  vs  $V$  characteristics [16]. Thus the barrier height  $\phi_{b0}$  is determined from the experimentally extrapolated  $I_0$  and is given by the relation

$$\phi_{b0} = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right) \quad (3)$$

The  $\ln(I)$  vs  $V$  characteristics of the devices for the positive and negative scans are shown in Figure 6.11 (a) and (b), respectively. The extrapolation of the linear regime to  $V=0\text{V}$

gives a saturation current  $I_0 = 280$  nA for the positive scan and  $I_0 = 200$  nA for the negative scan (as shown in Figure 6.11 (a) and (b)). During this investigation, the measurements were performed at room temperature ( $T = 300$  K) and the active device area  $A = 1$  mm<sup>2</sup>. The value of Richardson constant is calculated from  $A^* = 120m^*/m_e$  [14, 15] where  $m_e$  is the electron mass and  $m^*$  is the effective electron mass in AlO<sub>x</sub> ( $m^* = 0.4m_e$  for AlO<sub>x</sub>) [17]; thus  $A^* = 48$ . Using Eq. 3 the zero bias barrier height was estimated to be  $\phi_{b0} = 0.66$  eV for the positive scan and  $\phi_{b0} = 0.67$  eV for the negative scan. These values, together with the data from Figure 6.9 (a), show that the devices exhibit almost equal back-to-back Schottky contacts which further support the fact that devices in the OFF state have Cu/AlO<sub>x</sub>/Cu structure and not Cu/AlO/W. These results also suggest that the rupture of the Cu filament in AlO<sub>x</sub> based ECMs occurs at the weakest point throughout the filament length inside the AlO<sub>x</sub> and not at the AlO<sub>x</sub>/W interface. Moreover, the filament shape is likely to be closer to cylindrical shape than conical.



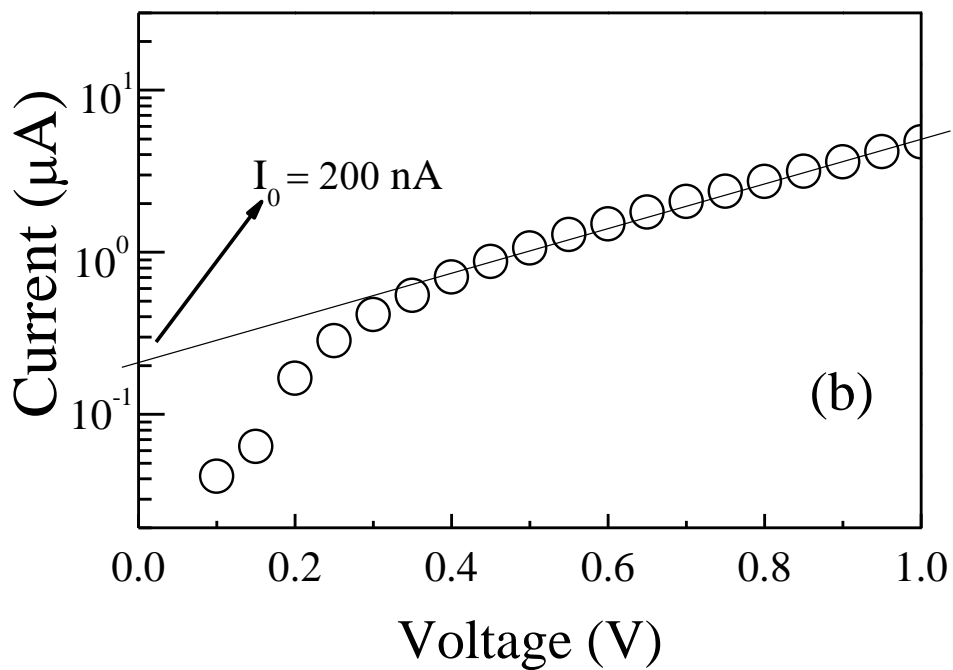
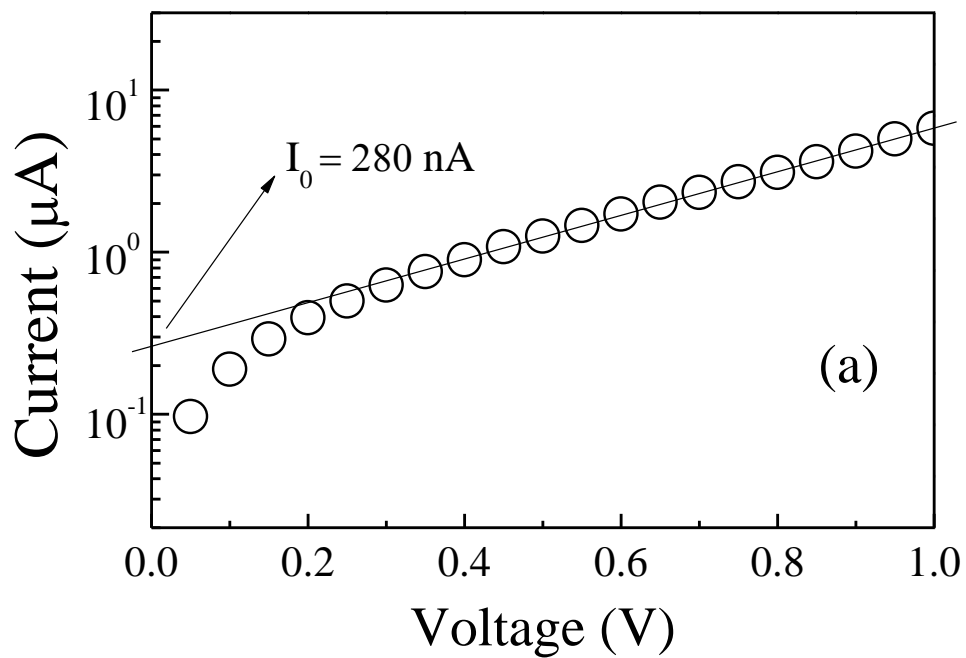


Figure 6.11: Extrapolation of the  $\log(I)$  versus  $V$  characteristics to extract  $I_0$  (a) in the positive scan and (b) in the negative scan.

### **6.6.5 Conduction mechanism of the devices in the ON state**

On the other hand, based on the presented mechanism, the ideal I-V characteristics of the ON state should be a linear behavior with the resistance of the Cu filament reflected in its slope. The I-V characteristics of our devices in the ON state except at voltages where the current limit applies are shown in Figure 6.12 (a). The linear behavior of the devices in the ON state, which is mostly applicable in the low bias region (0 to  $\pm 0.5$  V), supports the filamentary mechanism and shows that the devices exhibit a low resistance Ohmic conduction in the ON state. The proposed mechanism is also verified by fitting the data in the ON state to the Space-Charge-Limited-Current (SCLC) model, as shown in Figure 6.12 (b). The linear fitting of the  $\ln(I)$  vs  $\ln(V)$  exhibit a slope equals 1, where the current is directly proportional to the applied voltage and further supports the filamentary mechanism.

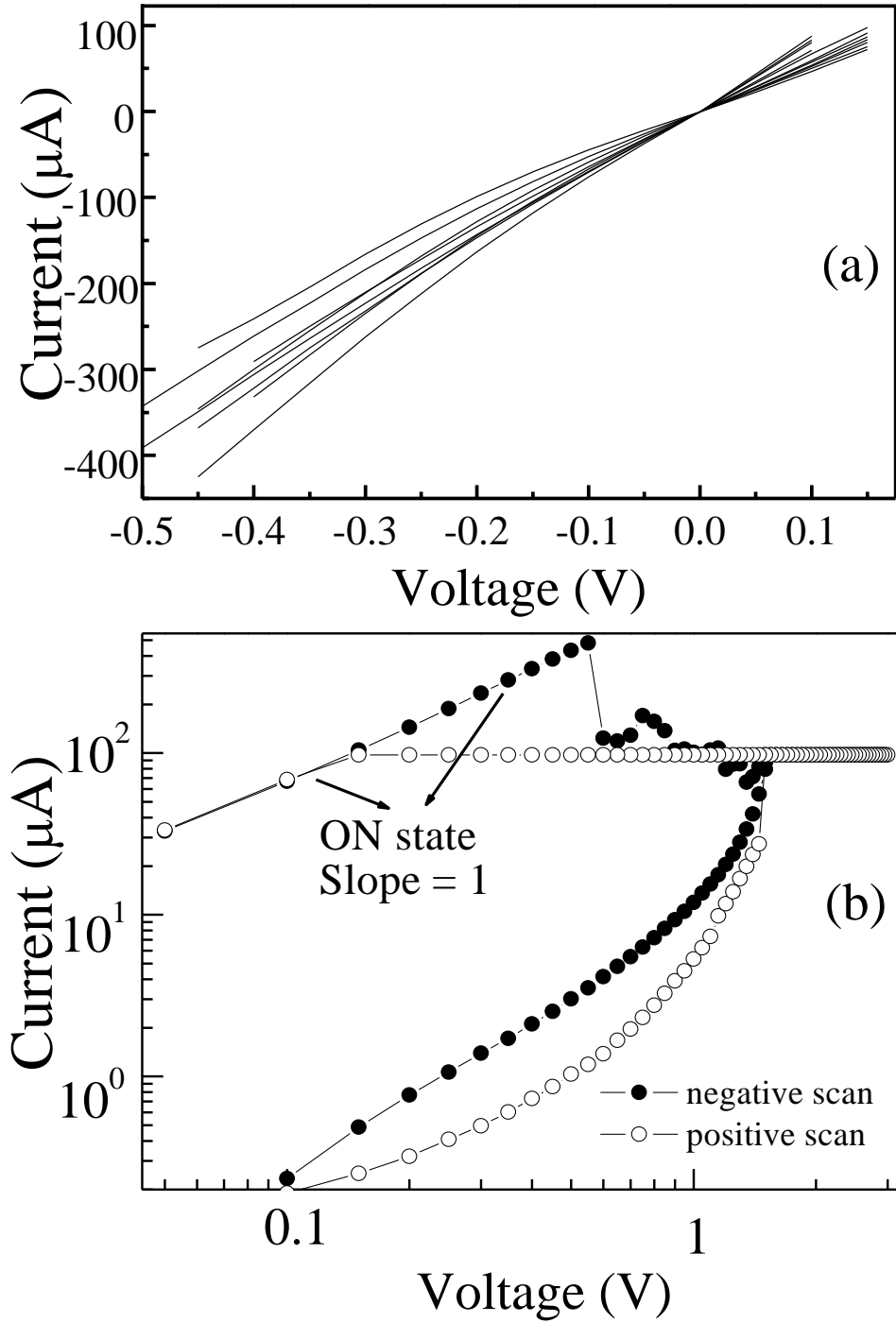


Figure 6.12: (a) The I-V characteristics of the devices in the ON state; (b)  $\text{Log}(I)$  vs  $\text{log}(V)$  linear fitting of the I-V characteristics in the OFF state.

### 6.6.6 Filament resistance calculations

Using such Ohmic behavior of the I-V characteristics, different parameters of interest can be extracted. Ohms law ( $V=RI$ ) is used to calculate “R” the resistance of the Cu filament. The average resistance was calculated to be about 1132  $\Omega$ . Moreover, using the formula:

$$R = \rho \frac{l}{A} \quad (4)$$

where  $\rho$  is the resistivity,  $l$  is the length, and  $A$  is the area of the filament. Using the calculated value of  $R$  from the I-V characteristics (1132  $\Omega$ ),  $l$  to be 20 nm (thickness of the  $\text{AlO}_x$  thin film) and  $\rho$  to be between 200 and 2300  $\mu\Omega\cdot\text{cm}$  [10], the cross section area of the Cu filament is calculated to be between  $3.53 \times 10^{-17}$  and  $4.06 \times 10^{-16}$   $\text{m}^2$ . Referring to the previous analysis regarding the shape of the filament and assuming it is perfectly cylindrical, where  $r$  is its radius ( $r = (A/\pi)^{1/2}$ ), the diameter ( $d$ ) of the Cu filament is calculated to be between 6.7 and 23 nm, in the same range with recent observations of such metallic filaments in similar memory stacks at similar applied current limits [10, 18].

### 6.6.7 Retention characteristics

The stability of the Cu filament was studied through recording the retention characteristics of the devices. The device was switched ON and OFF using 2 seconds long pulses; to switch the device ON the pulse was applied at 1.8 V with a current limit, while the pulse was applied at -1.5 V without current limit to switch the device OFF. The current was recorded versus time at a reading voltage as low as 0.1 V for both the ON and OFF states. The current maintained a value of 60  $\mu\text{A}$  in the ON state and a value of 0.1  $\mu\text{A}$  in the OFF state for more than  $10^3$  sec, as shown in Figure 6.13. The reproducible RS in the Cu/ $\text{AlO}_x$ /W ECM and its reliable retention in the ON and OFF states shows its potential in future nonvolatile memory applications.

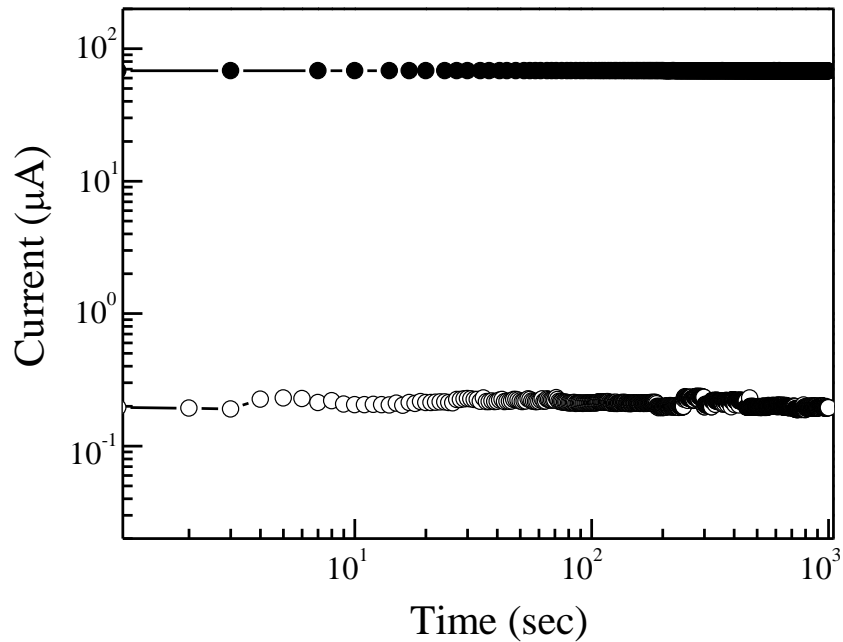


Figure 6.13: Retention characteristics of the RS W/AlO<sub>x</sub>/Cu memory devices in the ON and OFF states

### 6.7. Summary of the fabricated memory devices

In summary we fabricated an AlO<sub>x</sub> based ECM memory devices that benefit from the formation and rupture of a Cu filament to exhibit resistive switching (RS). Different ECM memory structures were fabricated in the CE/AlO<sub>x</sub>/Cu structure using different CE materials. The four metals that were used in the four different devices are: Al, Pt/Pd, Au and W. Devices using Al as a CE in the Al/AlO<sub>x</sub>/Cu structure is the only structure between the four fabricated structures exhibited both the unipolar and bipolar RS modes. Other devices were tested for both modes but none of the other structures was able to operate in the unipolar RS mode, it all exhibited only bipolar RS. But the devices using Al or PtPd as CE exhibited very dispersed I-V characteristics upon consecutive cycling. Devices using Au as the CE exhibited a failure to stay in the ON state upon consecutive cycling. The best fabricated devices were based on W as the CE. The device RS behavior was explained in term of filamentary mechanism and the I-V characteristics in the OFF state proved to fit

the thermionic emission model; and the conduction was explained by back-to-back Schottky contacts. The symmetrical shape of the I-V characteristics and the equal back-to-back Schottky barriers show that the rupture of the Cu filament occurs at the weakest point of the filament within the  $\text{AlO}_x$ . The I-V characteristics in the ON state showed Ohmic behavior were it fit the SCLC model with a slope equal to unity. The Ohmic behavior was used to calculate the Cu filament diameter which was found to be in the 6 to 23 nm range. The retention characteristics of the ON and OFF states were also studied and the memory retains its states for more than  $10^3$  sec of continuous testing. These results augur well for the development of memory devices based on resistive switching.

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## Chapter 7

### Conclusion and Further Work

#### 7.1 Conclusions

The main purpose of this thesis was to fabricate new two-terminals non-volatile memory (2T-NVM) devices for next generation NVM applications. One trend of the work was to fabricate novel two-terminals organic non-volatile memory (2T-ONVM) devices for the flexible and plastic electronics memory applications. Another trend was the fabrication of novel resistive switching filamentary based 2T-NVM based on low cost  $\text{AlO}_x$  switching medium and understand the resistive switching (RS) mechanism responsible for the switching behaviour.

##### 7.1.1 Fabrication of 2T-ONVM based on SWCNTs

The novelty of the work in the fabrication of 2T-ONVM was the utilization single-walled carbon nanotubes (SWCNTs) as charge storage elements in memory structures fabricated from all organic insulators and semiconductors. The 2T-ONVMs were fabricated in two different structures. First memory structure was a capacitive memory based on floating gates in the metal-insulator-semiconductor (MIS) structure. On the other hand, the other structure was a resistive switching memory based on embedded MIM structure. In the embedded MIS structure, SWCNTs were utilized as a floating gate, while in the embedded MIM structure the SWCNTs were utilized as charge traps to store the charge carriers. The SWCNTs in both structures were deposited using layer-by-layer (LbL) technique. In the LbL deposition, SWCNTs were functionalized by cationic and anionic surfactants and each layer was repeatedly deposited to build a matrix of SWCNTs using the charge reversal attraction. The LbL ensures that the SWCNTs are lying on the substrate to form a matrix or a thin film and thus can be embedded in the insulator in a middle-trap-layer to optimize the memory devices retention and stability.

For the embedded MIS structure, pentacene was used as the organic semiconductor and PMMA and/or SU8 as the organic insulators. Before fabricating the memory devices, control MIS devices were fabricated for comparison reasons. Four different control devices with combinations of different insulators were fabricated in the following structures: Al/SU8/pentacene/Au, Al/PMMA(chlorobenzene)/pentacene/Au, Al/PMMA(chloroform)/pentacene/Au and Al/SU8/PMMA/pentacene/Au. The results of the four control devices showed that the selection of the insulator affects the growth of the evaporated pentacene. The grain size of the pentacene affects the electronic performance of the fabricated MIS structures especially in terms of the operating voltages. A grain size of less than  $0.5 \mu\text{m}^2$  will lead to MIS structure (Al/SU8/pentacene/Au) that reaches its flatband voltage at  $-7.5 \text{ V}$ , while the flat band voltage can be closer to  $0 \text{ V}$  ( $\sim -2.5 \text{ V}$ ) when the grain size of pentacene in the MIS structure (Al/SU8/PMMA/pentacene/Au) is larger than  $1.2 \mu\text{m}^2$ . It was deduced that the evaporation of pentacene on top of PMMA, showed larger grain size pentacene films and was reflected in the lower absolute value of the operating voltages of the Al/PMMA/pentacene/Au and Al/SU8/PMMA/pentacene/Au structures. Thus PMMA (rather than SU8) was selected as the insulator to grow pentacene in the next step of fabrication of the embedded MIS memory devices.

All four fabricated control devices were traps free and this was concluded from the absence of hysteresis in the C-V characteristics upon the double voltage sweep. The absence of hysteresis shows that there are no carriers trapped within the structure. The absence of traps in the four control devices shows the reproducible clean fabrication of the MIS structures and will clearly act as evidence to show the effect of floating gate in memory structures.

The addition of the LbL deposited SWCNTs as a floating gate to fabricate embedded MIS memories resulted in a middle-trap-layer inside the insulator. First, an embedded MIS memory in the Al/PMMA/SWCNTs/PMMA/pentacene/Au structure was fabricated. The structure exhibited a clear hysteresis in the C-V characteristics which is an indication of charges stored in the SWCNTs. The structure exhibited an anti-clockwise hysteresis which is an indication that SWCNTs were charged and discharged by holes from the pentacene layer. The maximum memory window achieved was  $8 \text{ V}$  at  $-/+ 20\text{V}$  sweep range which resulted in a charge storage density of  $1.8 \times 10^{12} \text{ cm}^{-2}$ . The structure retained only  $\sim 86 \%$  of the stored charges where the confinement of the SWCNTs in the

PMMA/SWCNTs/PMMA structure using the same material and solvent was not that efficient. This could be due to the second spin of PMMA solution might have affected the first PMMA deposited layer and thinned it down. This process made the SWCNTs not effectively encapsulated in the middle-trap-layer structure, especially that first PMMA thin film was not hard baked for a long time. That was reflected in the losing of ~ 14 % of the stored charges.

To optimize the retention characteristics, another embedded MIS memory was fabricated using SU8 as a gate insulator in the Al/SU8/SWCNTs/PMMA/pentacene/Au. PMMA was used as the top insulator to enhance the pentacene growth. Unlike the first structure, the second Al/SU8/SWCNTs/PMMA/pentacene/Au devices exhibited a clockwise hysteresis which is an indication that the SWCNTs are being charged and discharged by electrons from the Al gate. The SWCNTs in the second structure were able to get charged and discharged at lower operating voltages than the first structure. A sweep voltage of  $\pm 5$  V was enough to get the SWCNTs charged. The maximum memory window achieved was 6 V at  $\pm 30$  V sweep range which reflects a charge storage density of  $9.15 \times 10^{11} \text{ cm}^{-2}$ . Unlike the first structure the Al/SU8/SWCNTs/PMMA/pentacene/Au structure was able to retain more than ~ 94% of the stored charges. The combination of insulators used kept the SWCNTs very efficiently encapsulated in a middle-trap-layer between two potential barriers and optimized the charge retention characteristics of the devices.

The second 2T-ONVM structure was the embedded MIM and was fabricated in the Al/PMMA/SWCNTs/PMMA/Al structure. The current-voltage (I-V) characteristics of the devices exhibited electrical bistability and non-volatile memory characteristics in terms of switching between high conductive (ON) and low conductive (OFF) states. The different conductive states were programmed by application of a positive and negative voltage pulses for the ON and OFF states, respectively. A maximum ON/OFF ratio of  $2 \times 10^5$  was achieved at low reading voltage of 1 V.

In order to explain the memory behavior and the carrier transport mechanism of the fabricated devices, the I-V characteristics were fitted using different conduction models. The space charge limited conduction (SCLC) model showed the best fit to the data and thus was used to understand the carriers behavior in both the ON and OFF states of the devices. Except at very low voltages of the OFF state, the current fit the thermionic

emission model which infers that electrons were accumulating at the barrier formed due to the potential profile between Al and PMMA. At higher voltages in the OFF state, the current fitted the so-called trap-limited-SCLC. The carriers are filling empty traps (SWCNTs) inside the out-of-plane medium (PMMA). In the ON state the carrier conduction in the devices follows an ohmic law which suggests that the SWCNTs were totally filled with injected electrons and the conduction mechanism follows a filled-traps SCLC. Using the proposed model of conduction the density of traps inside the device was estimated to be between  $2.19 \times 10^{17} \text{ cm}^{-3}$  and  $2.78 \times 10^{17} \text{ cm}^{-3}$ .

The characteristics described in this investigation for the two different types of 2T-ONVM fabricated clearly demonstrate the potential for SWCNTs to be used as storage elements in advanced ONVM devices in flexible electronics.

### **7.1.2 Fabrication of 2T-NVM based on $\text{AlO}_x$**

The second part of the investigation was the use of the low cost  $\text{AlO}_x$  as a switching medium in RS filamentary based MIM memories, the so-called electrochemical metallization (ECM) memories. Four different devices using four different counter electrodes (CE) in the following structures Al/ $\text{AlO}_x$ /Cu, PtPd/ $\text{AlO}_x$ /Cu, Au/ $\text{AlO}_x$ /Cu and W/ $\text{AlO}_x$ /Cu were fabricated and characterized. The Al/ $\text{AlO}_x$ /Cu structure is the only structure exhibited both the unipolar and bipolar RS modes. All the other devices exhibited the bipolar switching mode only. The unipolar RS in the Al/ $\text{AlO}_x$ /Cu was attributed to the role of the anionic oxygen vacancies which is a resultant of the oxidation of the Al counter electrode. This also caused the I-V characteristics to be dispersed upon consecutive ON/OFF cycling. To optimize the device behaviour in terms of I-V characteristics dispersion, different CE materials were used. PtPd did not improve the dispersion due to the existence of two different materials in the CE and the use of Au as a CE resulted in failure of the stability in the ON state.

On the other hand, the use of tungsten (W) as the CE resulted in a reproducible bipolar RS behaviour with much improved dispersion in the I-V characteristics upon consecutive ON/OFF cycling. To further understand the conduction mechanism of the memory devices, the I-V characteristics were fitted to different conduction models. The best fit in the OFF state follows the Thermionic Conduction (TC) model. Thus the conduction in the

OFF state can be modeled, in theory, as a back-to-back Schottky barrier. The symmetrical shapes of the I-V characteristics in the OFF state in the positive and negative scans show that the conduction in the devices behaves as equal back-to-back Schottky barriers. This indicates that the device structure in the OFF state is Cu/AlO<sub>x</sub>/Cu and the rupture of the filament occurs along the Cu filament length and not at the AlO<sub>x</sub>/W interface. On the other hand, using Ohms law, the slope of the linear I-V characteristics in the ON state was used to extract the Cu filament resistance and its diameter was estimated to be between 6 and 23 nm.

The results shows that AlO<sub>x</sub> can be utilized to fabricate reproducible low cost 2T-NVM using conventional metals such as Cu and W.

## **7.2 Further Work**

Further work can be suggested to enhance the ability to integrate the fabricated memory devices in future NVM applications.

Regarding the 2T-ONVMs fabricated, the same structure can be fabricated on flexible substrates to enhance the potentials of the use of SWCNTs as the charge traps in ONVM in the flexible electronics applications.

For the embedded MIS structure, further work on the optimization of the pentacene semiconductor is essential. A transistor using the same structure may be fabricated to calculate the mobility of the charge carriers inside pentacene in the embedded structures. Although the floating gate transistor using SWCNTs will not help in the 2T-ONVM applications but it will help understand more the physics of the charge conduction in the embedded MIS structure.

For the embedded MIM structure, further work on the operating voltages and the retention characteristics when fabricated on the flexible substrates is required. Because the SWCNTs matrix deposited using LbL might short circuit either insulators upon bending the structure. Regarding the ECM 2T-NVM based on AlO<sub>x</sub>, further work can be suggested to decrease the cost of the fabricated structure. The AlO<sub>x</sub> used in this investigation was deposited using e-beam evaporation which is done in vacuum under very high temperatures. Spin coated AlO<sub>x</sub> or anodized AlO<sub>x</sub> may be investigated for RS memories instead of the evaporated

$\text{AlO}_x$ . The thickness of the spin coated oxide will be an issue, the minimum thickness is required to exhibit such RS behavior. But if the spin coated layer exhibited RS behavior and was reproducible in a way to be used in 2T-NVM applications, the structure may be fabricated on flexible substrates as well to investigate the potential of such idea.