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Glasses for microphotonics

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glasses for microphotonics

International Workshop on Scientific Challenges for New Functionality in Glass

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Outline

❶ Microphotonics: photonics on/with (silicon) electronics

- ⇨ microphotonic devices (photonic crystals, microcavities, etc.)
- ⇨ motivation and drivers
- ⇨ back-end versus front-end integration of photonics

❷ Glasses as enablers of microphotonics

- ⇨ the glass transition as enabler
- ⇨ metastability as enabler
- ⇨ glasses as hosts: composite materials, etc.

❸ Scientific challenges for glasses in microphotonics

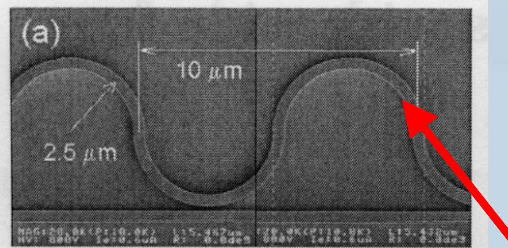
- ⇨ high index contrast devices
- ⇨ compatible processing: thermal 'window', etc. …

Microphotonics

❶ microphotonics (1) : technologies for realization of chip-scale (μm to mm) photonic devices

- ⇨ photonic crystal and wire waveguides and microcavities that enable light to be bent and confined on micron scales, without excessive light radiation
- ⇨ relies on high refractive index contrast between compatible materials

Source: NTT



Silicon (on insulator) photonic wire waveguides

❷ microphotonics (2) : fabrication of photonic/optical devices using the same processing steps employed in microelectronics

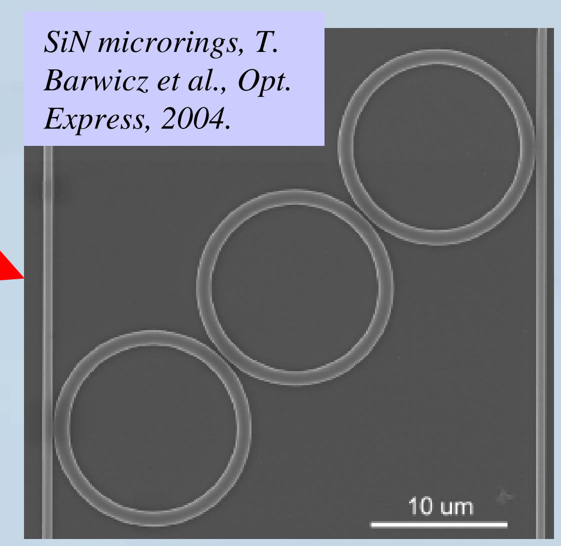
- ⇨ this definition is a bit more restrictive, implies CMOS compatible materials and process flow, etc.

Microphotonics – building blocks

❶ **photonic 'wires', microdisks, microspheres**

⇨ total internal reflection devices

⇨ microring resonators are a common example

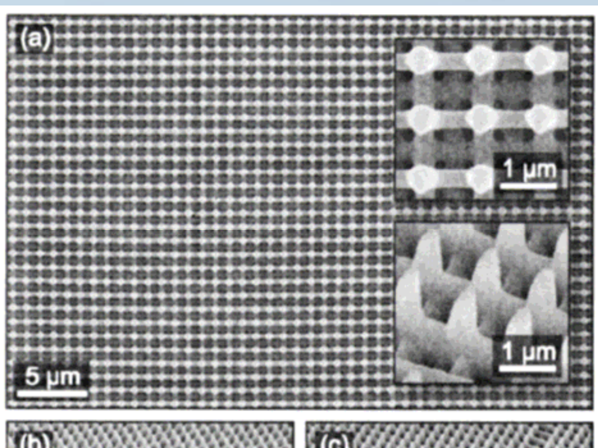


SiN microrings, T. Barwicz et al., Opt. Express, 2004.

❷ **photonic crystals (photonic bandgap devices)**

⇨ point defect microcavities

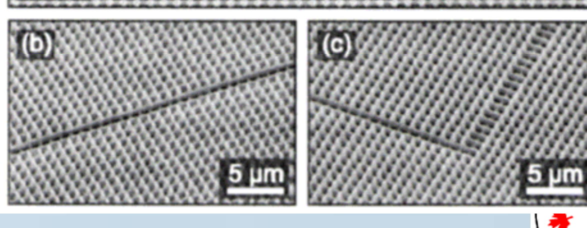
⇨ line defect waveguides



❸ **common denominator is *high index contrast***

⇨ $\Delta n > 0.2$ required for photonic wire bend radius < 10 µm

⇨ $n_2/n_1 \sim 2$ or greater required for full photonic bandgap in a 3-D photonic crystal



Glasses as microphotonics materials (1)

"Glass …(accounts) for more than 90 percent of all optical elements manufactured" – W.J. Tropf et al. in *OSA Handbook of Optics, Vol. II*

Many traditional advantages of glass transfer well to the microphotonics regime:

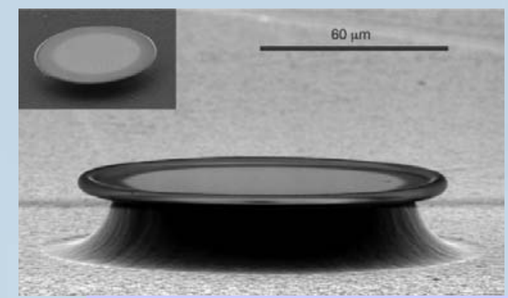
❶ ***cheap, isotropic, homogeneous:***

- ⇨ ease of forming high quality films, etc.
- ⇨ low volume scattering (no grain boundaries)
- ⇨ no 'preferred' directions (ie. on chip)

❷ ***processing enabled by glass transition:***

- ⇨ structures can be formed (molded, drawn, etc.) by heating above glass transition, then freezing in place
- ⇨ flow and reflow can produce nm-scale surface roughness

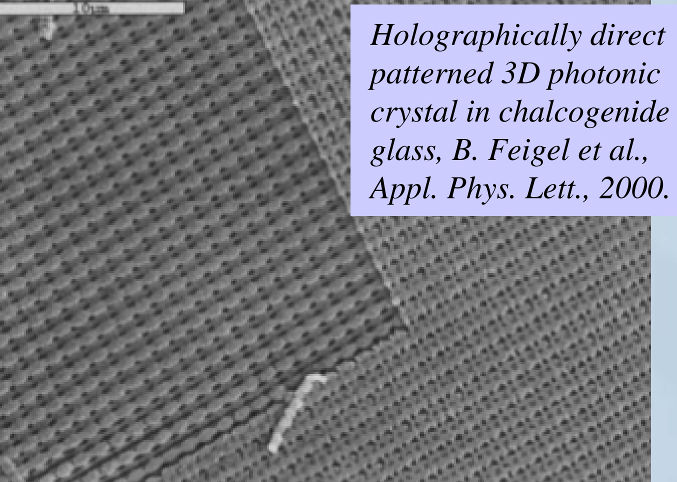
Source: Limin Tong et al., Nature, Dec. 2003



Source: D.K. Armani et al., Nature, Feb. 2003

Glasses as microphotonics materials (2)

Many traditional advantages of glass transfer well to the microphotonics regime:



Holographically direct patterned 3D photonic crystal in chalcogenide glass, B. Feigel et al., Appl. Phys. Lett., 2000.

❸ ***metastibility as an enabler:***

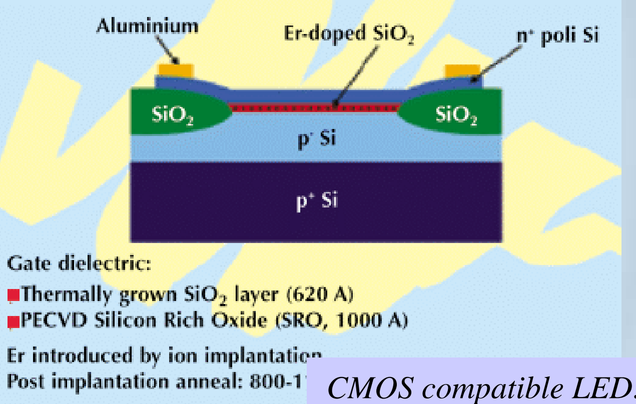
⇨ energetic beams (light, e-beams, ion beams) of modest intensity can often induce transitions between 'metastable states'

⇨ can be exploited for direct patterning of microdevices, and post-fabrication *trimming* of microphotonic devices

❹ ***functionality by 'doping' (glasses as hosts):***

⇨ rare-earth ions, quantum dots, metal nanoclusters can be incorporated for light emission, nonlinear, magneto-optic effects, etc.

⇨ the glass host lends its other advantages (ease of processing, etc.)

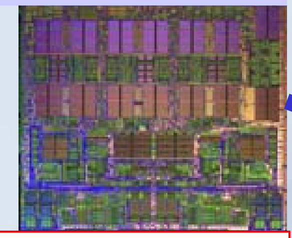


CMOS compatible LED: ST microelectronics, 2003

aside: amorphous materials (ie. SiO_2 gate dielectrics, etc.) continue to be of great importance to microelectronics

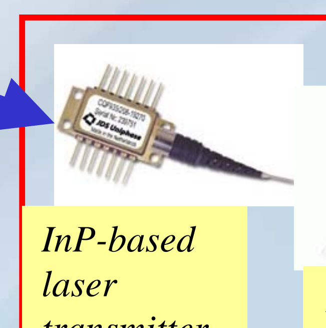
The silicon-photonics intersection

Microprocessor chip
Source: IBM



Silicon: the 'source' of data

Source: JDS Uniphase



InP-based laser transmitter

YIG-based isolator

$LiNbO_3$-based modulator

SiO_2/silicon-based AWG

Photonic components: at the intersection

Source: Corning

Fiber: the transporter of data

Starting Assumptions

❶ silicon (CMOS) is the dominant computing/electronics platform for the foreseeable future

❷ optical fiber is the best transport medium available

❸ traditional photonic devices are an impediment to 'pervasive' computing, sensing, and communications

The need for microphotonics in fiber networks (1)

Source: JDS Uniphase

❶ traditional photonics: <u>high-tech components, 'arcane and expensive' systems</u>.

- ⇨ different (specialized) material systems for every optical function
- ⇨ devices are 'integrated', but negligible system integration
- ⇨ devices typically interconnected by fiber pigtails

❷ current approach leads to <u>poor economics</u>

- ⇨ each photonic device is expensive (several k to several 10s of k)
- ⇨ optical alignment (of each device to its fiber pigtails) is critical and challenging; packaging accounts for ~50-90% of the cost of a device …

The need for microphotonics in fiber networks (2)

❶ the economics of optical networks needs fundamental change

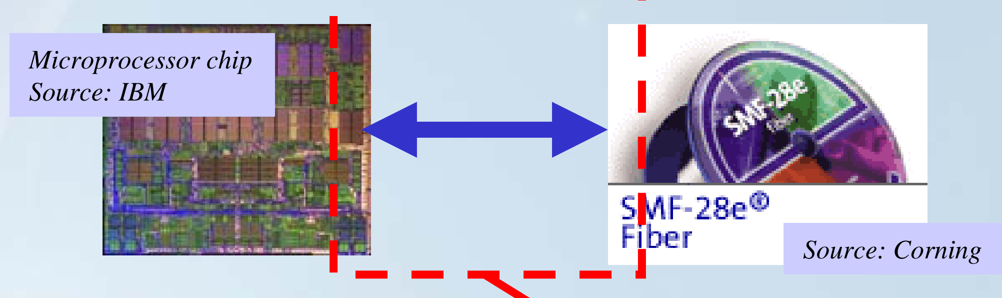
⇨ the current approach (no system integration) is economic (barely) for long-haul high-capacity systems

⇨ does not work as effectively in the sectors with high growth potential: fiber-to-the-home, pons, metro, etc.

❷ integration needed: of diverse photonic devices, between optics/electronics

⇨ traditional integrated approaches (InP, $LiNbO_3$ …) advancing but yet to break through (cost, yield, etc. remain issues)

⇨ need a single standard platform for optical integration (*silicon*?); glasses can play a role here (flexibility in processing, composition, etc.)



Integration of photonics on/with silicon: might 'streamline the intersection' between silicon electronics and photonic transport networks

"…optical networks are arcane and expensive … The goal of bringing optical networking down to the curb and ultimately to the PC can only be met if high-performance, low-cost, low-power optical components are available." M. Paniccia, Director of Photonics Research, Intel

Electronics & photonics – perfect marriage?

TRLabs

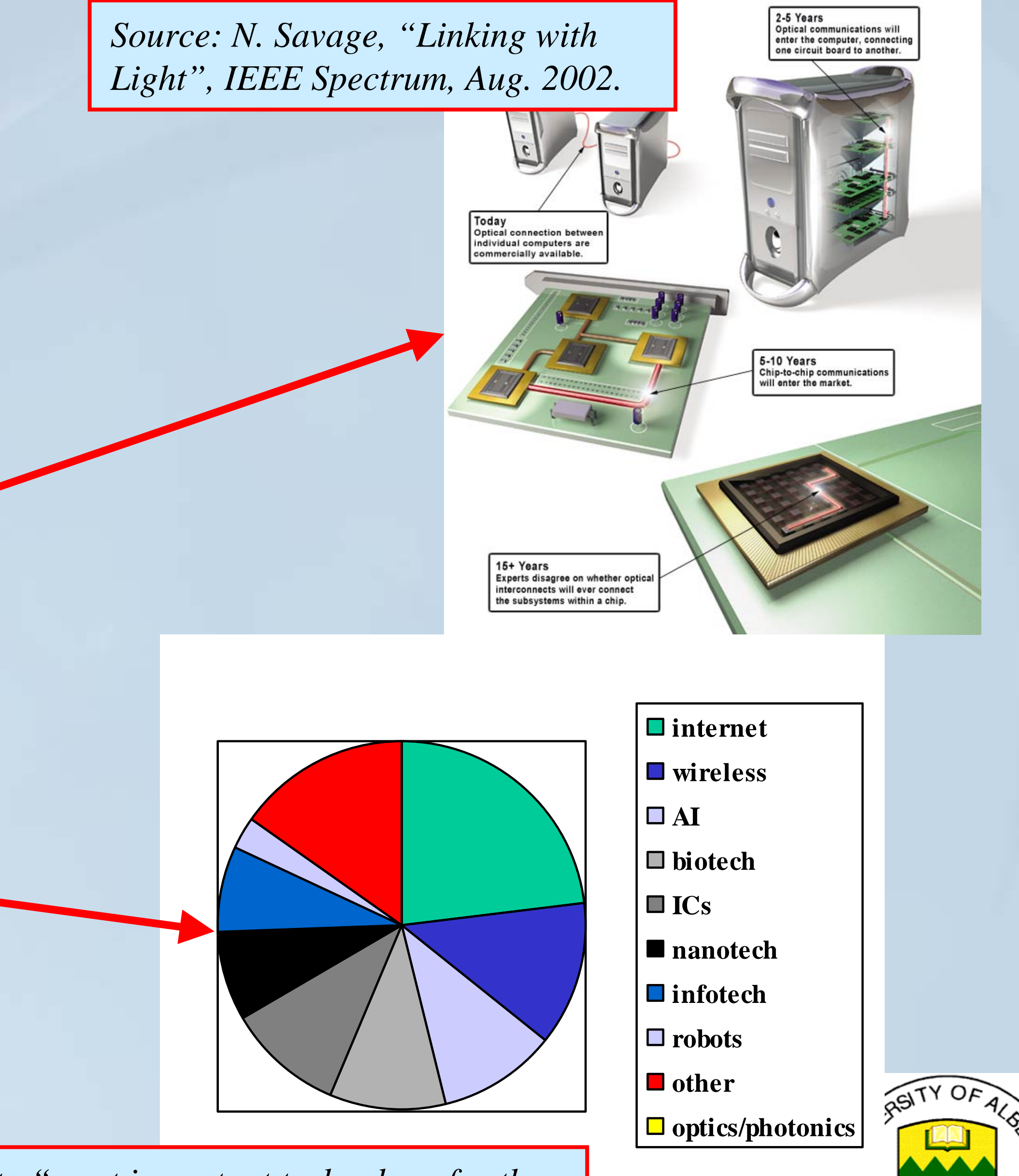
❶ they need each other

- ⇨ photonic networks need closer integration with silicon electronics (see above)
- ⇨ silicon electronics will increasingly need photonics for high speed interconnects (board to board, chip to chip, intrachip?)

❷ *microphotonics* might be a much needed boost for photonics:

- ⇨ recovery from the fiber boom/bust cycle has been slow

Source: N. Savage, "Linking with Light", IEEE Spectrum, Aug. 2002.



Answers to "most important technology for the coming decade" IEEE Spectrum, Nov. 2004

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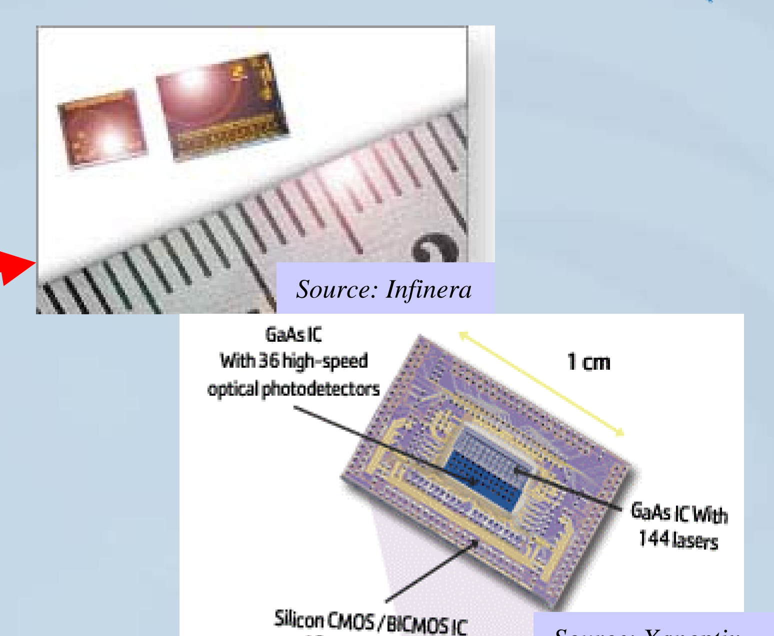
Silicon-Photonics Convergence in Industry

❶ **Optical networking industry**

- ⇨ hybrid integration between optical components and silicon CMOS increasing in sophistication…)
- ⇨ CMOS plays an increasingly important role in fiber networks (forward error correction, advanced line coding functions, O/E/O …)
- ⇨ is hybrid III-V / CMOS integration approach truly scalable in a mass-market sense?

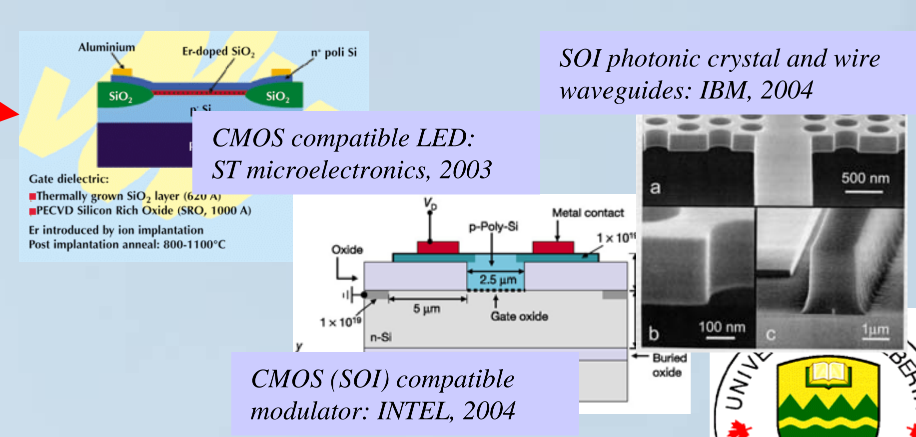


Source: Infinera

Source: Xanoptix

❷ **Silicon IC industry**

- ⇨ the big silicon firms have increased their investment in photonics
- ⇨ will a *truly integrated optoelectronics technology* be incubated by the IC industry, with optical networks as one of the main beneficiaries?

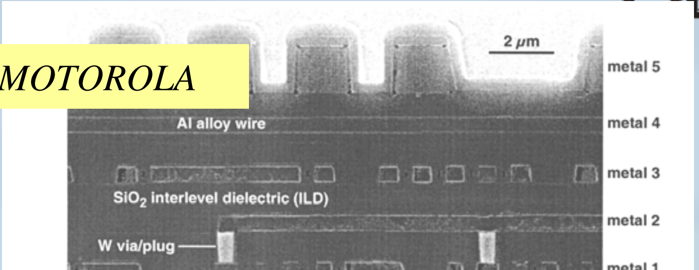


SOI photonic crystal and wire waveguides: IBM, 2004

CMOS compatible LED: ST microelectronics, 2003

CMOS (SOI) compatible modulator: INTEL, 2004

Monolithic / Hybrid Integration



Source: MOTOROLA

monolithic ➔ 'single stone'

❶ Strictly speaking, even a silicon IC is not a monolithic system

⇨ relies on a diverse set of mutually compatible materials (silicon, polySi, SiO_2, Al, Cu, W …)

⇨ sometimes monolithic is equated with processes restricted to the 'standard' set of materials

❷ same flexibility should be afforded to *photonic* integration as electronic integration; possible (?) *working definitions* are:

① **Monolithic integration**: system fabricated on a single wafer using automated mask alignment and a defined set of process steps (thin film dep, lithography, implantation, diffusion, etching)

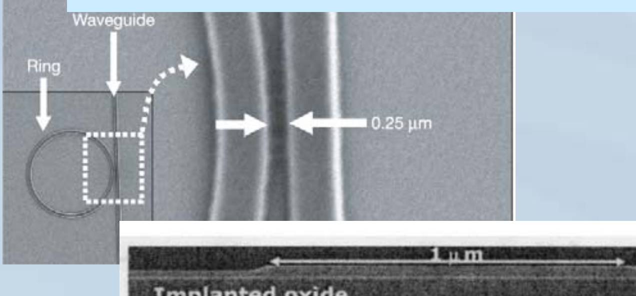
② **Hybrid integration:** system assembled by interconnecting separately fabricated parts, using techniques (pick and place, flip-chip, etc.) other than automated mask alignment

Approaches to photonics on silicon (1)

❶ **front-end approach (especially SOI):**

- ⇨ high-temperature processes OK
- ⇨ inherently compatible, but disruptive to the standard process flow
- ⇨ Photonics/electronics compete for real estate
- ⇨ restricted in terms of materials /functionality
- ⇨ range of photonic functions are possible using crystalline silicon

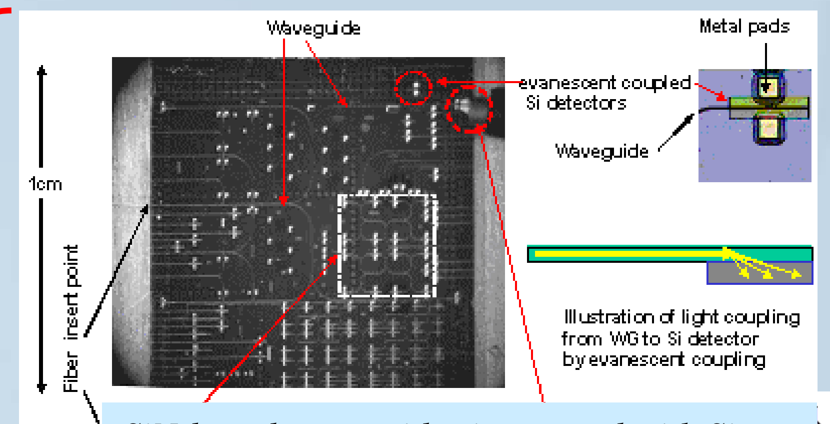
All-optical switch in SOI, source: V.R. Almeida et al., Nature, Oct. 28, 2004.



3-d photonic structures in SOI, source: P. Koonath et al., Appl. Phys. Lett., Aug. 2004.

❷ **middle-ground approach:**

- ⇨ use 'standard' CMOS materials (SiON, Ta_2O_5, etc.)
- ⇨ processing temperature somewhat variable, depending on exact placement in the process flow
- ⇨ more flexible than front-end approach



SiN-based waveguides integrated with Si detectors on CMOS, source: M.J. Kobrinsky et al., Intel Tech. J., May 2004.

Approaches to photonics on silicon (2)

❸ **back-end post-processing approach (above IC approach):**

⇨analogous to above IC approach used for integration of RF devices on CMOS

i. potential advantages

⇨ least disruptive to the standard CMOS process flow

⇨ wide range of functional materials can be employed, in theory at least

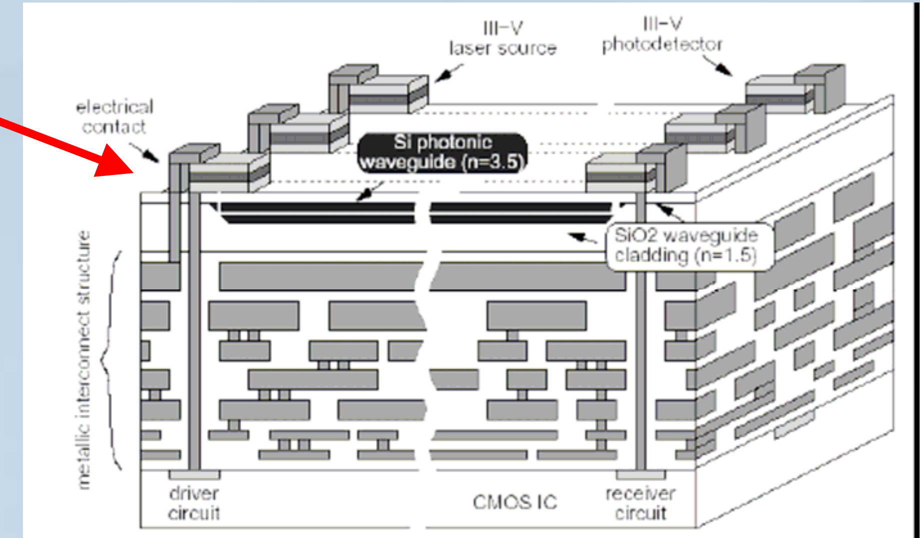
⇨Possibility for 3-d integration, within a set of photonic interconnect levels

ii. overriding challenges

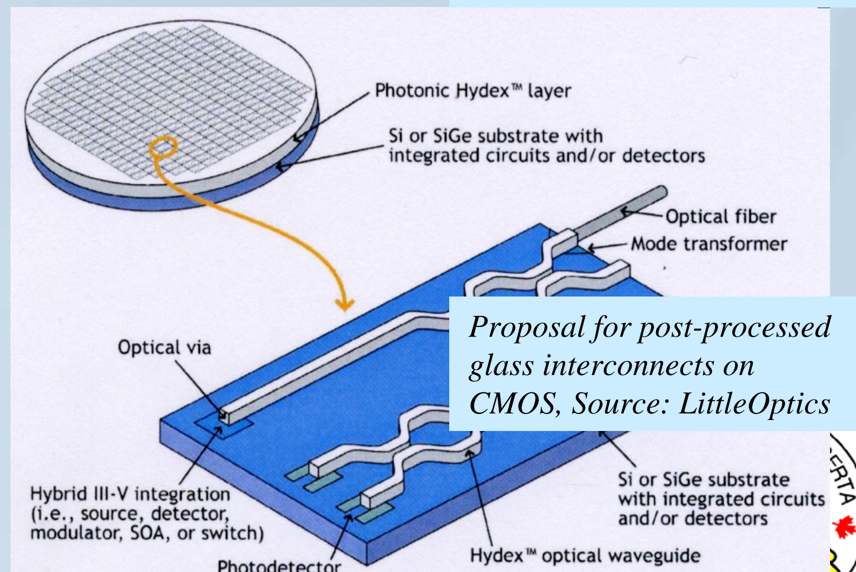
⇨ restricted processing temperatures (<400 C for 1-2 hours?), CTE issues

⇨ new materials/devices must be compatible with packaging-related temperature excursions and in-use IC temperatures (>100 C)

⇨ 'vias' required to link front-end opto-electronic devices (photodetectors, etc.) to back-end photonics



...transmission lines on CMOS, Source: G.J. Carchon et al., IEEE T-MTT, April 2004.



Proposal for post-processed glass interconnects on CMOS, Source: LittleOptics

Surface roughness in microphotonics (1)

❶ **Surface (interface) scattering loss is a major challenge in microphotonics**

⇨ chip-scale waveguides must be very small and have high core-cladding refractive index contrast

⇨ The Tien model for estimating scattering loss in a (slab) waveguide tells us:

SOI photonic wire, Sakai et al., Yokohama U.

$$\alpha_S \sim \sigma^2 \Delta n^2$$

α_S – *scattering loss coefficient*

σ – *standard deviation (characteristic amplitude) of the roughness*

$\Delta n^2 = n_{core}^2 - n_{cladding}^2$

❷ **scattering loss can be severe as Δn increases and core dimensions shrink ($\alpha_S \sim 1/d^4$)**

⇨ to minimize scattering loss, more accurate models (such as Payne-Lacey model) indicate that both the characteristic amplitude (σ) and the *correlation length* (L_C) of the roughness statistics must be low

Surface roughness in microphotonics (2)

Traditional integrated optics

microphotonics

Minimum bend radius for 'negligible' radiation loss

Bending Radius(µm)

10^3 10^2 10^1

1

Minimum Feature Size

Cladding: SiO_2
λ = 1.55 µm

2

Si

Slope = 3

Si_3N_4

2001

0.01 0.1 1

Δ n

10^2 10^1 10^0 10^{-1} 10^{-2}

Scattering Loss (dB/cm)

Approx. loss due to surface roughness, with surface roughness statistics as a parameter

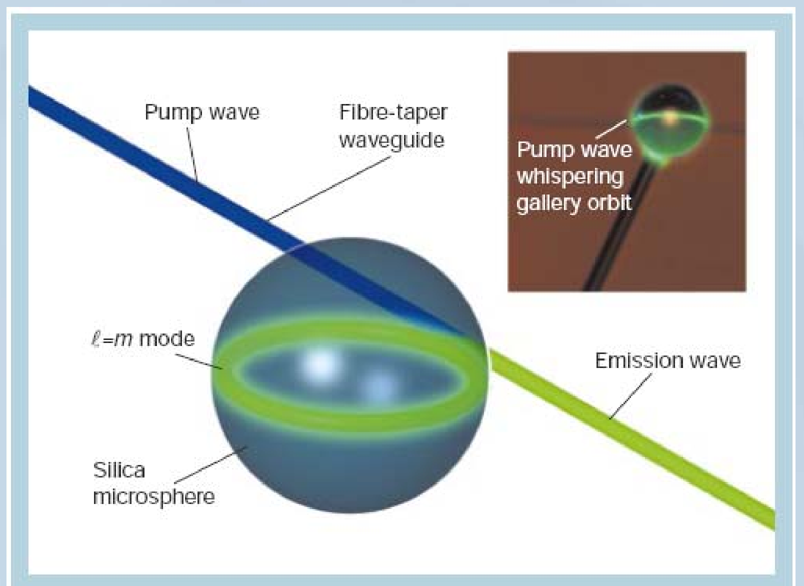
Core-cladding index contrast

Source: K. Wada, Proc. SPIE vol. 5357

❶ **light can be bent or confined on a µm scale, using either TIR or photonic crystal dielectric structures. Either approach requires:**

- ⇨ Δn~1 or greater
- ⇨ precise feature definition on a sub-µm scale
- ⇨ nearly atomic level feature smoothness to minimize light scattering

Surface roughness in microphotonics (3)



$$Q_{SS} = \frac{\lambda^2 D}{2\pi^2\sigma^2 L_C}$$

D – microsphere diameter

❶ **Q-factor of a microsphere cavity often limited by surface scattering**

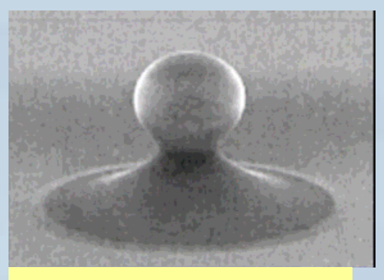
⇨ $Q \sim 10^{10}$ has been demonstrated for reflowed SiO_2 spheres formed at the end of glass fibers (the highest Q for any solid-state microcavity)

T_g-enabled fabrication of microphotonic structures

❶ **liquids have optical quality surfaces through 'self-assembly'**

⇨ glass devices can be formed from a liquid state, thus can benefit from the same surface-tension mediated assembly of smooth surfaces

Water droplet on a superhydrophobic surface, Source: C. Sanchez et al., J. Mater. Chem., vol. 15, 2005.



~50 μm microball lens by reflow of organic glass, Source: C.-T. Pan et al., Appl. Opt., vol. 43, 2004.

❷ **roughness of a melt-formed or reflowed glass is determined by surface capillary waves (small amplitude fluctuations at a liquid surface, frozen into place at T_g)**

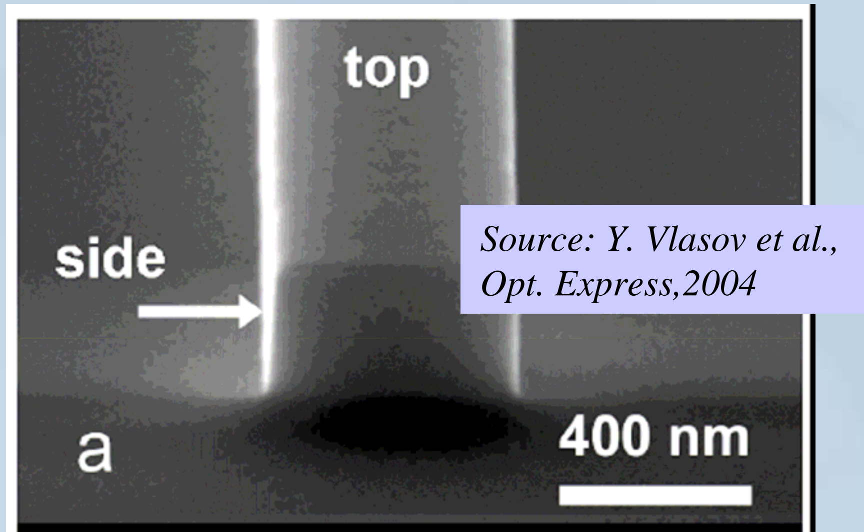
⇨ SiO_2 surfaces have predicted rms roughness ~0.1 nm, confirmed many times

$$\sigma \approx \sqrt{\frac{k_B T_g}{\gamma(T_g)}}$$

Photonic wires in crystals vs. glasses

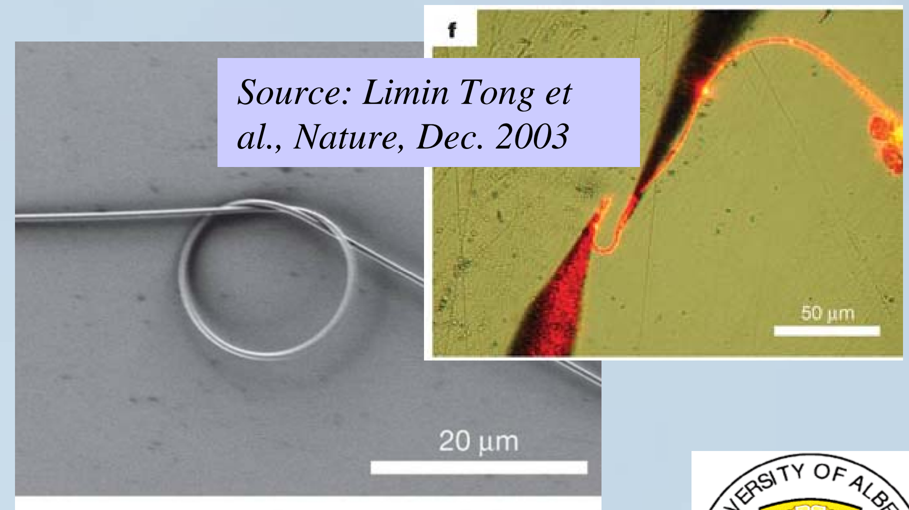
❶ ex. SOI photonic wires formed by state-of-the-art ebeam litho and dry etching

- ⇨ sidewall roughness as good as σ~5 nm, L_C~50 nm, with tight process control
- ⇨ propogation losses typically 3-10 dB/cm at λ=1550 nm

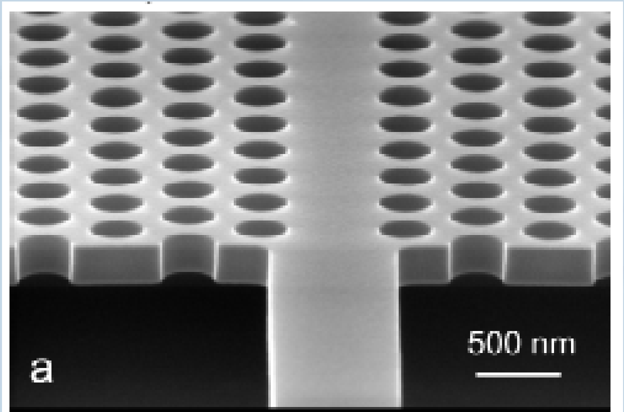


❷ ex. SiO_2 wires fabricated by straightforward flame drawing technique

- ⇨ surface roughness as good as σ~0.5 nm, L_C~50 nm, with tight process control
- ⇨ propogation loss <1 dB/cm at λ=633 nm

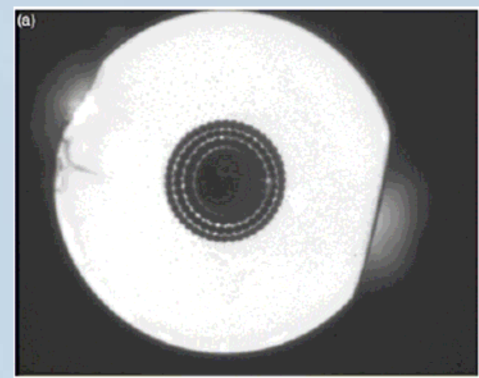


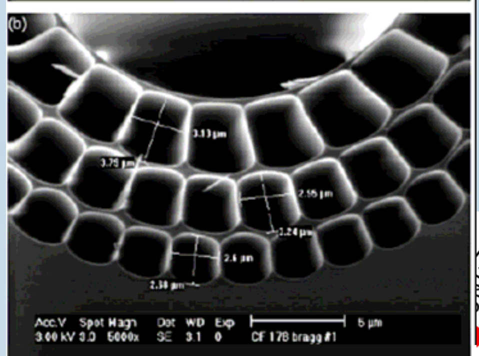
Photonic crystals – crystals vs. glasses



❶ **ex. line defect waveguides in 2-D SOI photonic crystals**

- ⇨ ebeam litho and etching
- ⇨ best propagation losses typically 10-30 dB/cm, limited by roughness/disorder





❷ **ex. air-core waveguides in 2-D glass photonic crystals (ie. photonic crystal fibers)**

- ⇨ rod and stack preform, fiber drawing
- ⇨ best propagation losses ~1 dB/km, limited by surface roughness of ~0.1 nm (see Roberts et al., *Opt. Express,* vol. 13, pp. 236-244 (2004).

Can these benefits (surface tension mediated surfaces and order) be transferred to 2-D and 3-D photonic crystals on chips?

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Microcavities in crystals vs. glasses

	Fabry–Perot	Whispering gallery		Photonic crystal
High Q	Q: 2,000 V: 5 $(\lambda/n)^3$	Q: 12,000 V: 6 $(\lambda/n)^3$	Q_{III-V}: 7,000 Q_{Poly}: 1.3×10^5	Q: 13,000 V: 1.2 $(\lambda/n)^3$
Ultrahigh Q	F: 4.8×10^5 V: 1,690 μm^3	Q: 8×10^9 V: 3,000 μm^3	Q: 10^8	glass?

Crystalline semiconductor microcavities, $Q<10^5$

Glass (SiO_2) microcavities, $Q>10^8$

Source: K. Vahala, Nature, vol. XXX, 2003

❶ Q factor of microcavities typically limited by surface scattering loss

- ⇨ lithography/etching steps used to form semiconductor microstructures
- ⇨ surface tension can be employed in the manufacture of glass microstructures

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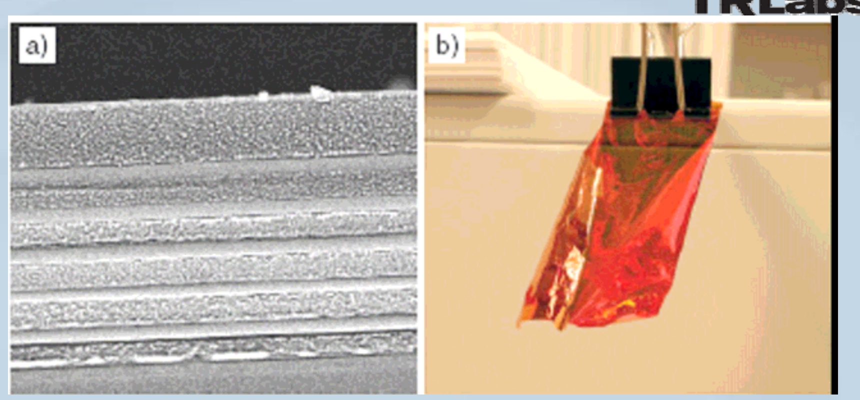
Glass composites

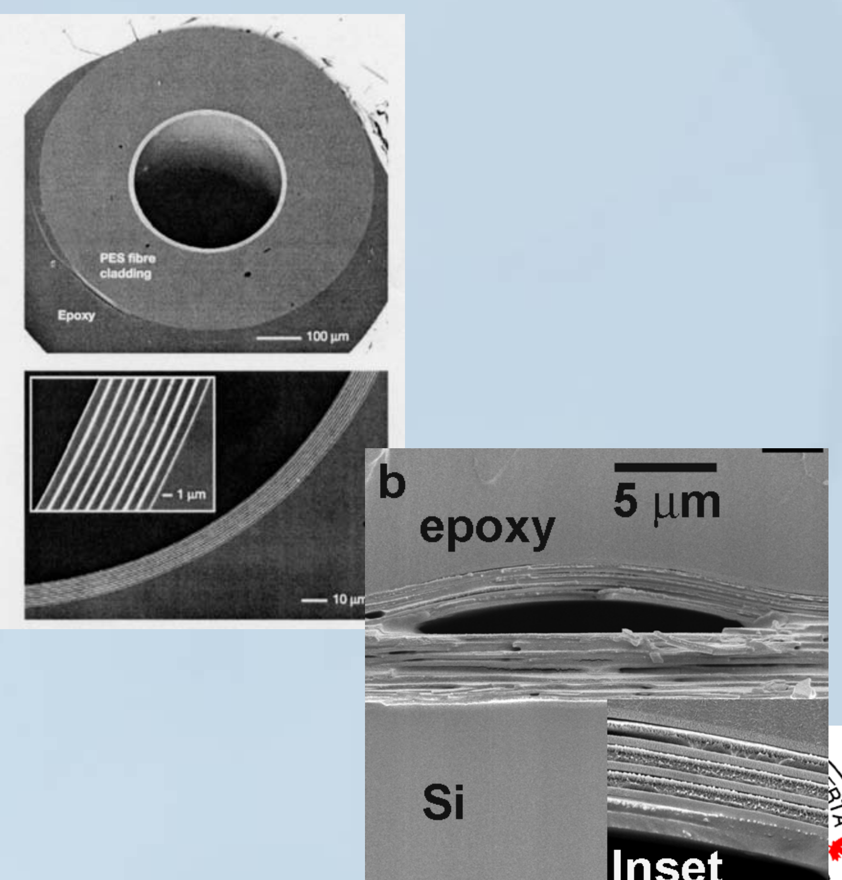
❶ **extensive research on nano-composite materials of numerous types:**

- ⇨ nanocrystal-embedded glasses
- ⇨ glass-ceramics
- ⇨ hybrid inorganic-organic materials

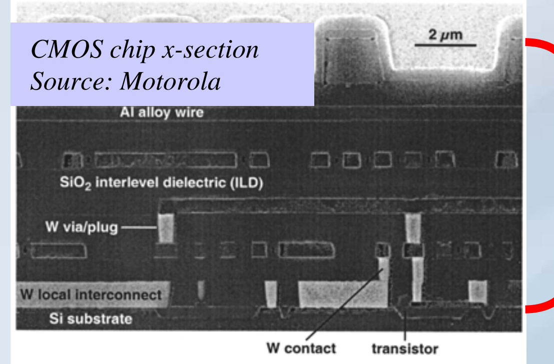
❷ **ex. chalcogenide glass / polymer composites can enable all-solid photonic crystals**

- ⇨ thermo-mechanical compatibility and $n_2/n_1 \sim 1.8$ or greater





Research challenge: glass/polymer microphotonics



<u>*A scientific challenge:*</u> is it possible (using organic and inorganic glasses) to build chip-scale microphotonics, with diverse functionality, within or above the interconnect layers of silicon chips?

Key material requirements:

❶ ***<u>Process compatibility</u>***

⇨ must be processible within a back-end 'thermal budget'

⇨ should not degrade the performance of underlying electronics (by contamination, etc.)

❷ ***<u>chip-scale integrated optics</u>***

⇨ must provide high index contrast (approaching that of SOI) to enable micron-scale bends, resonators, and photonic crystal building blocks

⇨ ideally should support *3d photonic integration*

❸ ***<u>multifunctional photonic circuitry</u>***

⇨ integration of passive/active materials is necessary

⇨ ideally, set of materials should enable a full range of active photonic functionality (photo/electroluminescence, electro-optic, Kerr nonlinear, acousto-optic, magneto-optic, thermo-optic, …)

Summary of Interests and Contact Information

❶ integrated optics for fiber networks and computing

❷ silicon-based microphotonics

❸ chalcogenide glasses for photonics

❹ rare-earth doped glasses for waveguide amplifiers and sources

❺ nonlinear integrated optics

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Silicon CMOS – a few facts (1)

❶ a microprocessor contains an incredibly complex on-chip network of interconnections

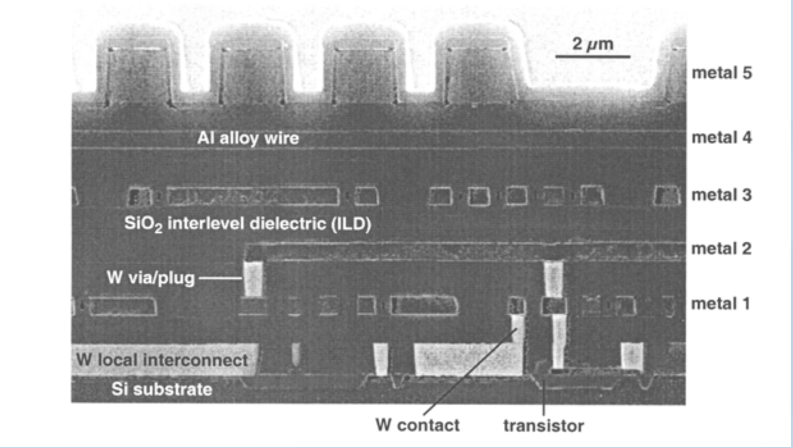
⇨ The Intel ‘Montecito’ processor (~2007) will contain > 1 billion transistors, clock rate >10 GHz

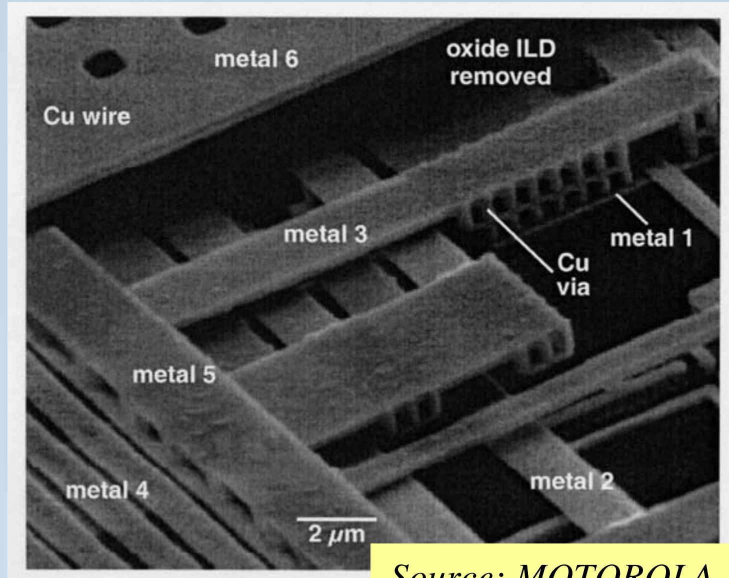
⇨ chips already contain >7 km of interconnect wires per cm^2

⇨ up to 9 layers of interconnects used now; >15 layers envisioned

⇨ Chip cost is dominated by wires; adding layers is expensive

⇨ microprocessors dissipate several hundred Watts per cm^2; ~50% is due to resistive losses in interconnect metal





Source: MOTOROLA

Silicon CMOS – a few facts (2)

❷ interconnects pose the greatest challenge to the continuation of Moore's law

⇨ wire 'bandwidth' scales downwards with feature size

⇨ processors increasingly 'wait around' for data (from memory etc.)

⇨Longer 'global' interconnects pose the biggest problem

⇨Copper wires and low k dielectrics developed at great cost to the industry; will provide temporary relief only

⇨ lots of solutions under study; new chip architectures, microwave/wireless solutions, on-chip optical interconnects

Source: J. Baliga, IEEE Spectrum, Mar. 2004

Source: ITRS 2003