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A study of DC-DC converters with focus on analysis techniques and current mode control

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A Study of DC-DC Converters

With Focus on Analysis Techniques and Current Mode Control
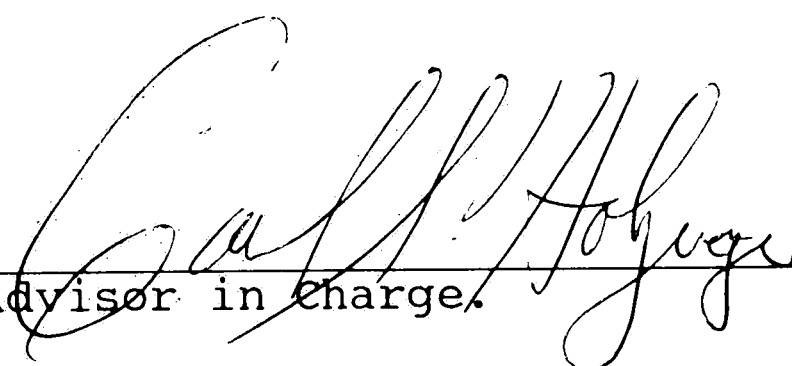
by

Douglas B. Lebo

A Thesis

Presented to the Graduate Committee

of

Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1991

This thesis is accepted and approved in partial
fulfillment of the requirements for the degree of Master
of Science in Electrical Engineering.

_____   5/6/91
Advisor in Charge.   Date

_____   5/6/91
CSEE Department Chairperson.   Date

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I would like to thank the following people for motivating me to write this paper:

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My advisor, who taught me a great deal when I was an undergraduate. Who shed light on the process of writing this paper; and gave me insight into the problem at hand, yet let me pursue the topic without interference.

My Grandfather, Homer C. Althouse, who got me interested in electronics many years ago; and who taught me much about problem solving and "Good old down home ingenuity". I dedicate this work in memory of him.

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Abstract

Switch mode DC-DC converters are becoming increasingly prevalent in today's miniaturized low power equipment. This paper investigates single inductor pulse width modulated converter topologies, and the analysis tools available to deal with these circuits. The Boost, Buck, Boost-Buck, and CUK topologies are introduced, and the large signal operation of each is discussed. Discontinuous operation, Duty cycle control, and Current mode control are presented as generalized extensions of the previous topologies. State Space Averaging and Linearization is introduced as a method of representing a time variant circuit as a time invariant one to facilitate small signal analysis. Nonlinear time invariant circuit models to aid in the characterization of converter circuits are derived from the concepts of state space averaging . These models are transformed into spice models using the nonlinear dependent source feature of spice. A sample Boost converter is designed using the spice models as a tool to compensate the feedback loop of the converter and a comparison is done between the real life implementation of the circuit and the predictions made by the model.

Introduction

Today's ever decreasing packaging volume requirements coupled with the increased use of battery powered applications has led to a wide spread adoption of Switch Mode power supplies in many applications. From commanding just 17% of the power supply market in 1979, the switch mode power supply market has grown to capture 63% of the market by year end of 1989.[1] Design of these supplies has long been considered a black art left to a vendor with a proven track record, while leaving small applications such as on card regulation to single chip power miserly linear solutions or expensive hybrid IC switch mode supplies. Recent offerings by semiconductor manufacturers of new control integrated circuits and complete "drop in solutions" has given the novice a path to the successful design of supplies provided that the semiconductor manufacturer's design notes are followed. Many of the predesigned integrated circuit solutions reduce the effort required to design a circuit at the expense of providing less than optimal efficiency and load regulation. While the simplification of switch mode power supply design has led to increased use, some designers are not comfortable using or modifying existing circuits which use a technology that they do not fully understand. It is the author's opinion that much of the reluctance of designers

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1 Electronic Design December 1990.

to use switchmode power supplies comes from a lack of understanding coupled with an extensive history of horror stories involving these circuits. This paper is intended to familiarize designers with some of the design strategies, analysis tools, and circuit topologies used for these circuits so they can be better equipped in the design, and selection processes of switch mode supplies.

As with any regulator circuit, there is a mechanism for controlling the flow of energy to the load to achieve regulation. Switching regulators store a fixed amount of energy supplied by the input source in the magnetic field of an inductor, and then later release the stored energy to the load. Storage and release of energy is governed by the circuits switch mechanism. Altering the output voltage of the supply is implemented by regulating the ratio of energy storage time to energy release time. This differs from the regulation mechanism in a linear supply which essentially operates as a variable resistive voltage divider to dissipate unused energy. Switching regulator control techniques will all center around the modulation of the switch on time to off time ratio since energy transfer is governed by the switching modulation method. Some of the modulation methods used are: fixed switch on time with variable switch off time, fixed switch off time with variable on time, and fixed cycle time where the sum

of the switch on and off time is constant. The latter is simply pulse width modulation of a fixed frequency clock and is by far the dominant method in use today for switch mode DC-DC converters. Pulse width modulation (PWM) control's key advantage is that the lowest frequency component of ripple generated by the switching action is constant lending to a simple output filter implementation to achieve low output ripple. However, other modulation methods are used to meet special performance requirements. Fixed on-variable off time is used by some of the single IC regulator solutions offered by IC vendors such as Linear Technologies. For example, the quiescent current of the LT-1073 is considerably lower than in a typical PWM controlled circuit. Throughout this paper we will focus on PWM so some definitions are in order. If one defines T to be the constant period of the clock and D the variable duty cycle of the switch, then switch on time will be denoted as ($t_{on} = D \cdot T$) and switch off time denoted as ($t_{off} = (1-D) \cdot T$). (See figure 1)
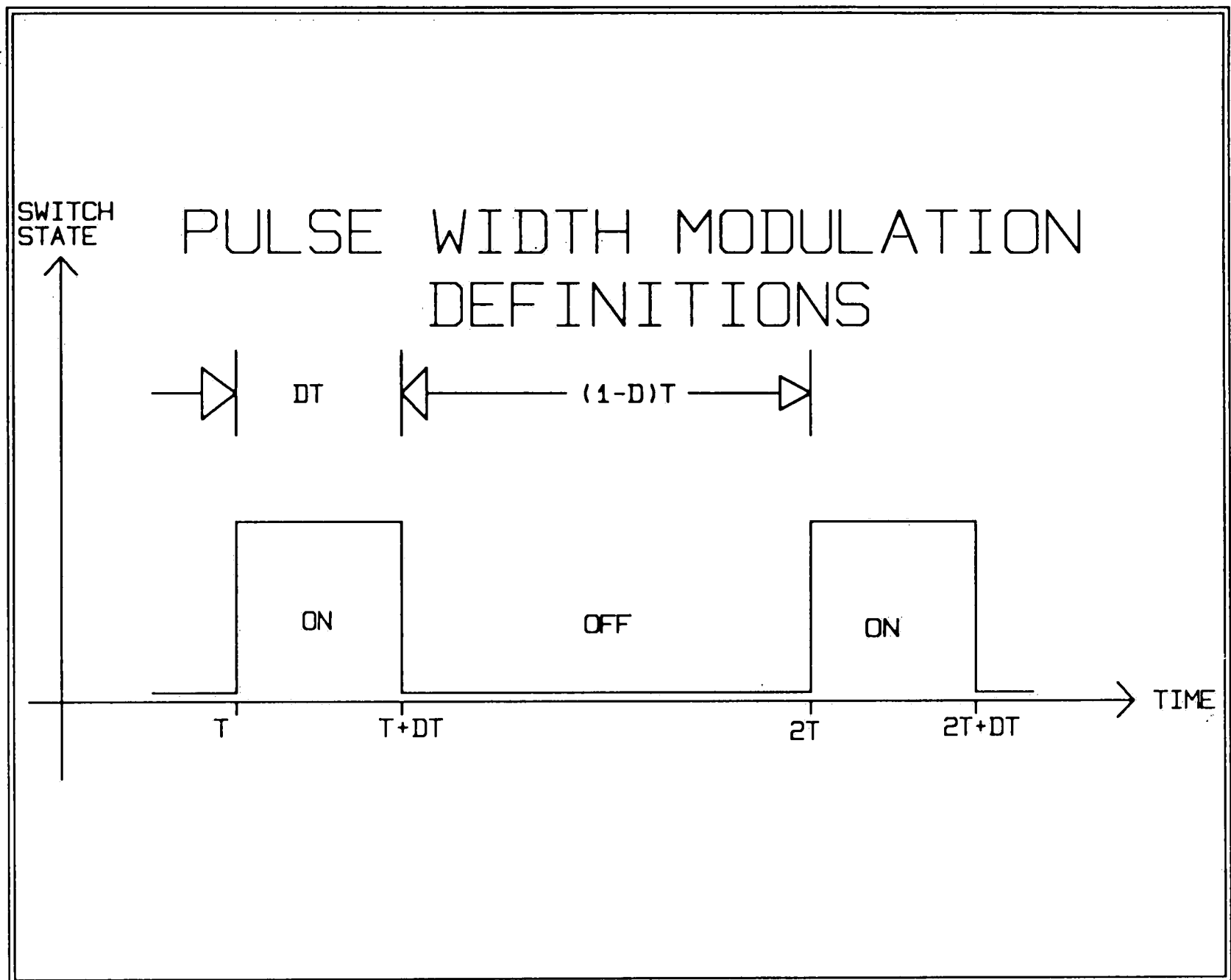
Figure 1 - Pulse Width Modulation Definitions.

Pulse width modulated switch mode supplies can be divided into one of the two following basic types: The Forward Converter Topology where current from the source flows from the source into the load during the switch on time; and the Flyback topology where energy is transferred from the source to the inductor during switch on time, and from the inductor to the load during switch off time. There is some discrepancy in the literature on these definitions especially concerning flyback topologies, so the reader should be aware of the use of them when reading other literature on the subject.

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Independent of what topology is used it is of the utmost importance to fully understand where energy is being supplied from, stored in, and dissipated to during each portion of the clock. For the purposes of the initial discussion of each topology, we will assume that there is energy stored in the inductor at the end of each cycle implying that there is current flow through the inductor.

Basic Topologies

Depending on the topology chosen, converters can produce an output voltage which has a magnitude greater or less than the input while maintaining or reversing the polarity relationship between the input and output. The Buck converter produces an output which is less in magnitude, and the same polarity as the input. The Boost topology maintains the polarity of the input, yet produces an output magnitude greater than that of the input. A Boost-Buck converter inverts the polarity of the input, but can produce an output voltage with a magnitude above or below that of the input.

The Buck Converter

A simplified diagram of a forward buck converter is shown in figure 2. As suggested by its name, the buck converter produces an output voltage which is less than the input potential.
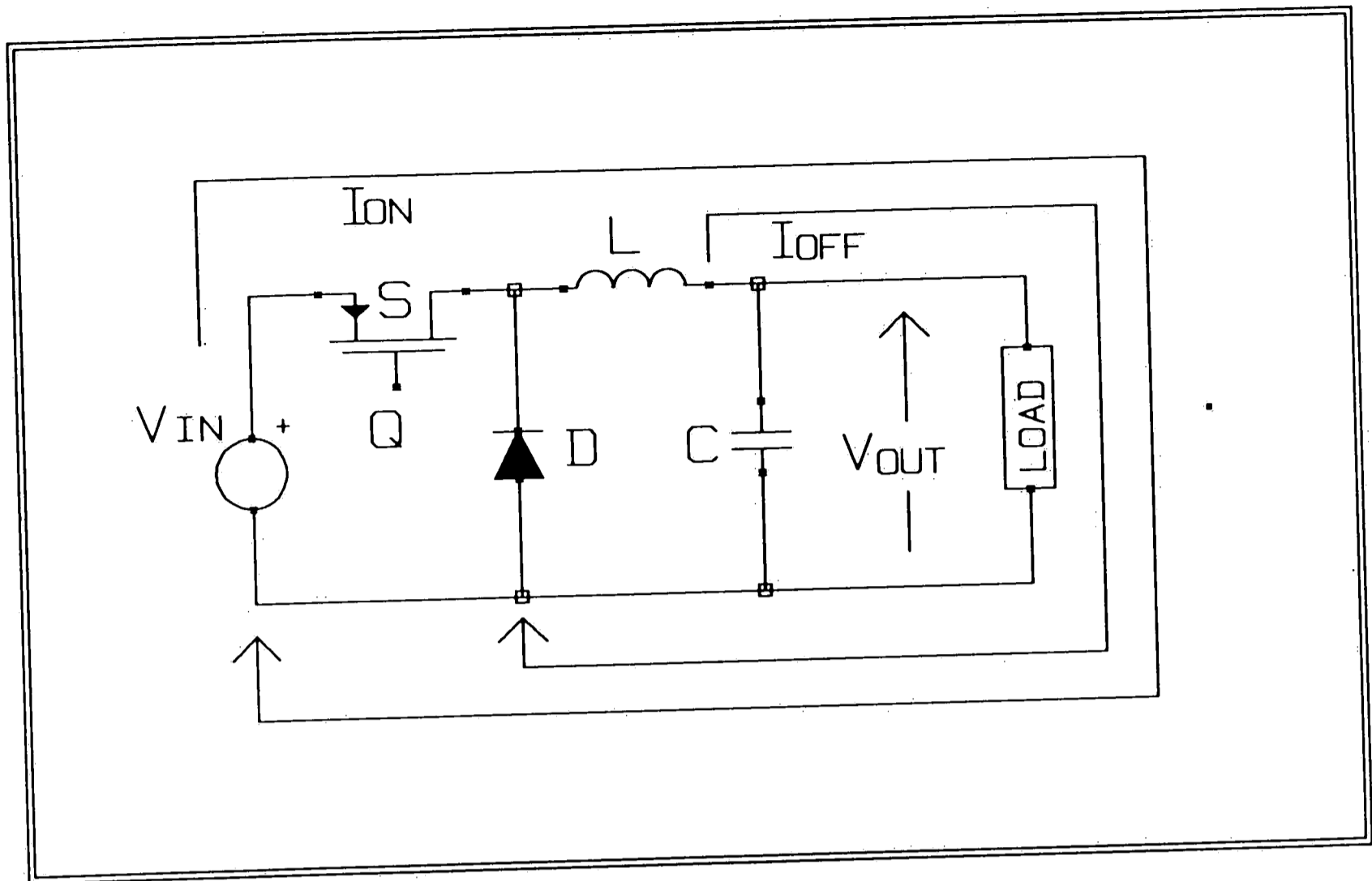
Figure 2 - Buck Converter.

(A) $\quad I_{L(t)} := \left[V_{in} - V_{out}\right] \dfrac{1}{L} t + I_0 \qquad$ For (0 < t < DT)

(B) $\quad I_{L(DT)} := \left[V_{in} - V_{out}\right] \dfrac{1}{L} D T + I_0 \qquad$ When switch opens up at t=DT

(C) $\quad I_{L(t)} := \left[\left[V_{in} - V_{out}\right] \dfrac{1}{L} D T + I_0\right] - \left[V_{out} - V_D\right] \dfrac{1}{L} (t - D T) \qquad$ For (DT < t <T)

(D) $\quad I_{L(T)} := \left[\left[V_{in} - V_{out}\right] \dfrac{1}{L} D T + I_0\right] - \left[V_{out} - V_D\right] \dfrac{1}{L} T (1 - D) \qquad$ For (t=T)

(E) $\quad I_{L(T)} := I_0 := \dfrac{1}{L} T \left[D V_{in} - V_{out} - V_D (1 - D)\right]$

(F) $\quad V_{out} := D V_{in} - V_D (1 - D) \qquad$ Since I_0 is steady state

Figure 3 - Buck Converter Equations.

To analyze the large signal behavior of the circuit, piecewise linear analysis techniques will be used in conjunction with making the assumption that the output of the supply is an ideal voltage source of magnitude V_{out}. If one assumes that the filter cap is large enough to maintain an approximately constant output voltage throughout a cycle then when the switch is closed at the beginning of a clock cycle, the inductor current will start to rise approximating a liner ramp as described in figure 3A. At the end of the switch dutycycle, the switch opens up defining the maximum inductor current as approximately that described in figure 3B. The voltage across the inductor will instantaneously reverse and increase in magnitude until the voltage across it is a diode drop above the output voltage; there it will remain clamped as long as there is energy stored in the inductor. Energy stored in the inductor is now discharged according to equation 3C until the end of the clock cycle T. Since the circuit is assumed to be in a steady state condition, the energy stored in the inductor at the start of the next cycle must equal that stored at the beginning of the present cycle. By invoking an inductor current boundary condition at the switch turn on point of the second cycle [$I_0(T-) = I_0(T+)$], a solution for the output voltage as a function of input voltage and duty cycle can be realized as carried out in figures 3E and 3F.

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The Flyback Boost Converter
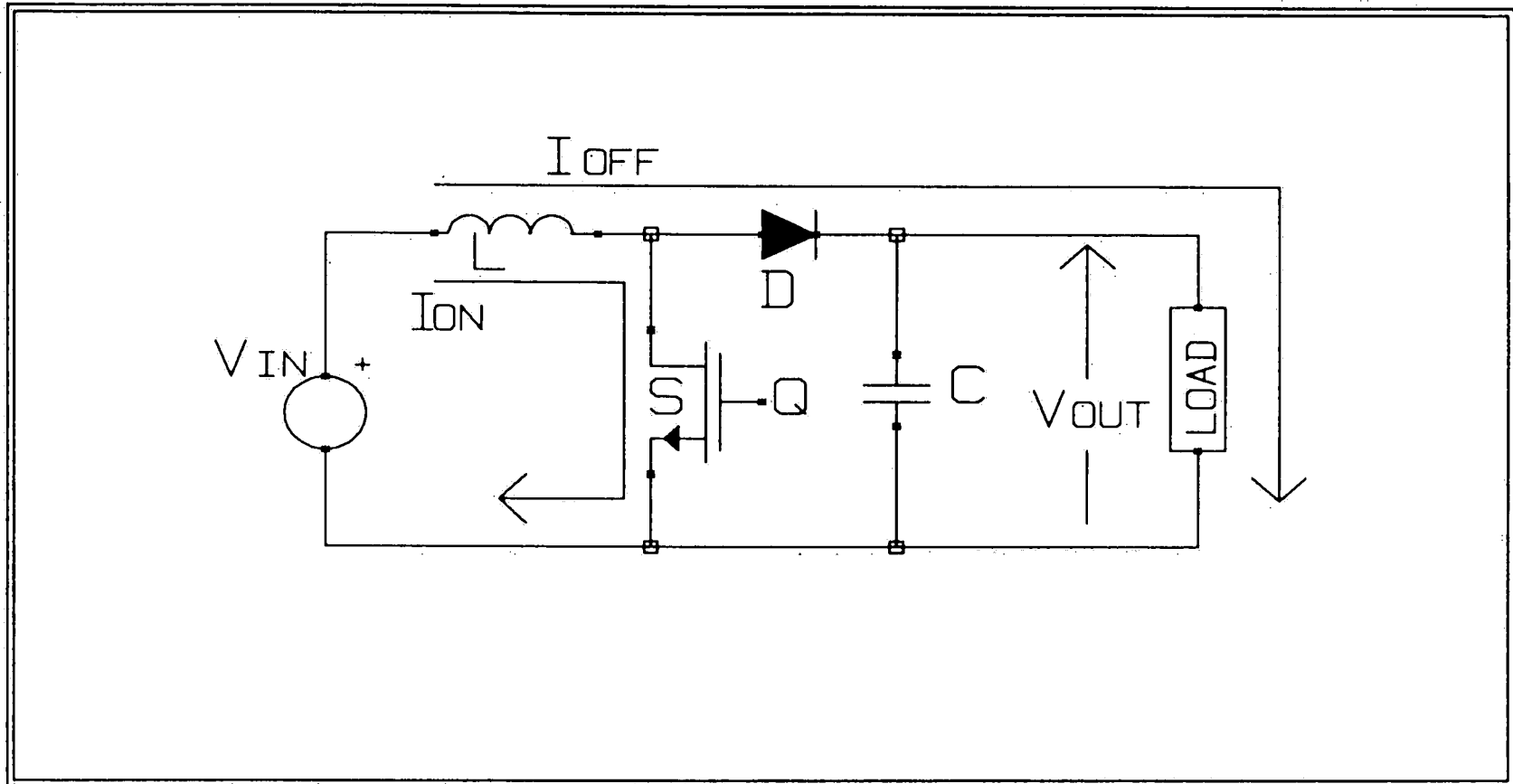
Figure 4 - Boost Converter.

$$(A) \quad I_{L(t)} := \begin{bmatrix} I_0 + V_{in} \dfrac{1}{L} t \end{bmatrix} \quad \text{For } 0 < t < DT$$

$$(B) \quad I_{L(DT)} := \begin{bmatrix} I_0 + V_{in} \dfrac{1}{L} D T \end{bmatrix} \quad \text{For } t = DT$$

$$(C) \quad I_{L(t)} := \begin{bmatrix} I_0 + V_{in} \dfrac{1}{L} D T \end{bmatrix} - \begin{bmatrix} V_{out} - V_D - V_{in} \end{bmatrix} \dfrac{1}{L} (t - DT) \quad \begin{array}{l} \text{For} \\ (DT < t < T) \end{array}$$

$$(D) \quad I_{L(T)} := \begin{bmatrix} I_0 + V_{in} \dfrac{1}{L} D T \end{bmatrix} - \begin{bmatrix} V_{out} - V_D - V_{in} \end{bmatrix} \dfrac{1}{L} T (1 - D) \quad \text{For } t = T$$

$$(E) \quad I_{L(T)} := I_0 \qquad 0 := \dfrac{1}{L} T \begin{bmatrix} V_{in} - \begin{bmatrix} V_{out} + V_D \end{bmatrix} (1 - D) \end{bmatrix}$$

$$(F) \quad V_{out} := V_{in} \dfrac{1}{1 - D} - V_D (1 - D) \quad \text{For } I_0 \quad 0$$

Figure 5 - Boost Converter Equations.

A flyback boost converter is pictured in figure 4. Boost converters use the same four basic components that their forward counterparts do, yet produce an output voltage which is greater than the input potential. During the switch on time interval the inductor is connected across the input source, while during the switch off period it is in series with the source and load. Effectively, the potential induced across the inductor is added to the input source there by boosting the output voltage above the input voltage. Since the inductor is across the source when the switch is closed, the inductor charging current is simply a linear ramp described by the equation in figure 5A. When the switch opens at the end of the duty cycle interval t=DT, the energy stored in the inductor is at its maximum and the voltage across the inductor reverses and rises until the blocking diode conducts. At this point, the voltage across the inductor is clamped to (V_{out} - V_{in} - V_{Diode}) so the energy stored in the magnetic field of the inductor is discharged into the load as described by the equation in figure 5C. If a steady state condition is assumed where the minimum inductor current I_0 is the same for all cycles of the clock; equation 5D can be solved for V_{out} as a function of V_{in} as carried out in figures 5E and 5F.
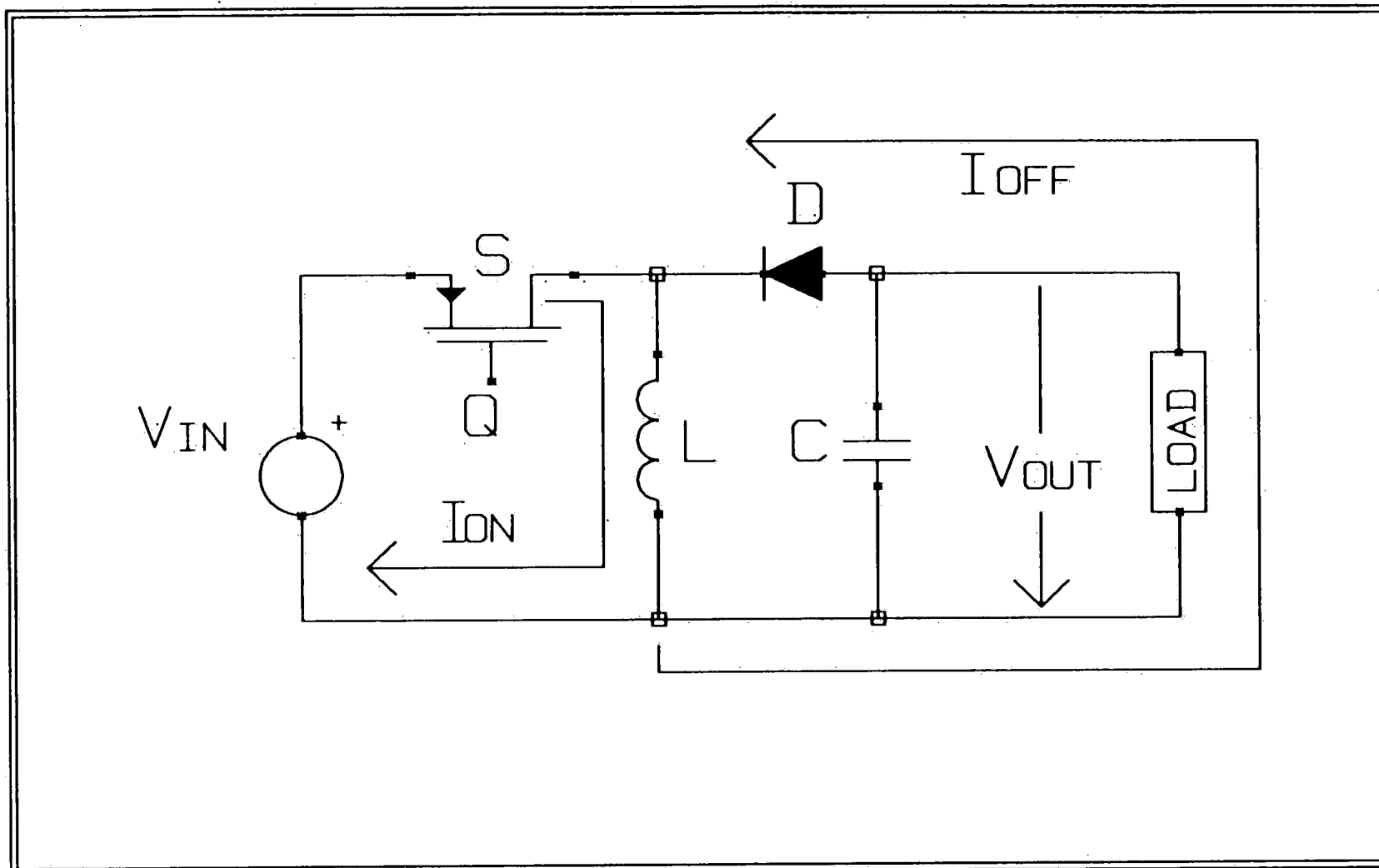
Figure 6 - Boost - Buck Converter.

(A)
$$I_{L(t)} := \left[I_0 + V_{in} \frac{1}{L} t \right] \qquad \text{For } 0 < t < DT$$

(B)
$$I_{L(DT)} := \left[I_0 + V_{in} \frac{1}{L} D T \right] \qquad \text{For } t = DT$$

(C)
$$I_{L(t)} := \left[I_0 + V_{in} \frac{1}{L} D T \right] + \left[V_{out} - V_D \right] \frac{1}{L} (t - DT) \qquad \begin{array}{c} \text{For} \\ (DT < t < T) \end{array}$$

(D)
$$I_{L(T)} := \left[I_0 + V_{in} \frac{1}{L} D T \right] + \left[V_{out} - V_D \right] \frac{1}{L} T (1 - D) \qquad \text{For } t = T$$

(E)
$$I_{L(T)} := I_0 \qquad 0 := \frac{1}{L} T \left[V_{in} + \left[V_{out} - V_D \right] \frac{1 - D}{D} \right]$$

(F)
$$V_{out} := V_{in} \left[\frac{-D}{1 - D} \right] \qquad \text{For } V_D = 0 \quad I_0 \quad 0$$

Figure 7 - Boost - Buck Converter Equations

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The Boost - Buck Converter

A simplified boost-buck flyback converter is shown in figure 6. The boost-buck regulator differs from the boost topology in that the inductor voltage is not added to the input voltage during the energy transfer period. This allows the magnitude of the output voltage to span from zero to above the input voltage depending on the switch duty cycle. The energy storage phase is the same as that of the boost converter, so the same equations for inductor charging current may be utilized. When the switch opens up at the end of the inductor charging phase, the potential across the inductor reverses and is clamped to V_{out} by the charge on the output capacitor. Consequently, the energy stored in the inductor is discharged as a current ramp until the end of the clock cycle as described by figure 7C. Again assuming a steady state condition for the minimum inductor current I_0, the output voltage can be calculated as demonstrated in equations 7E and 7F.

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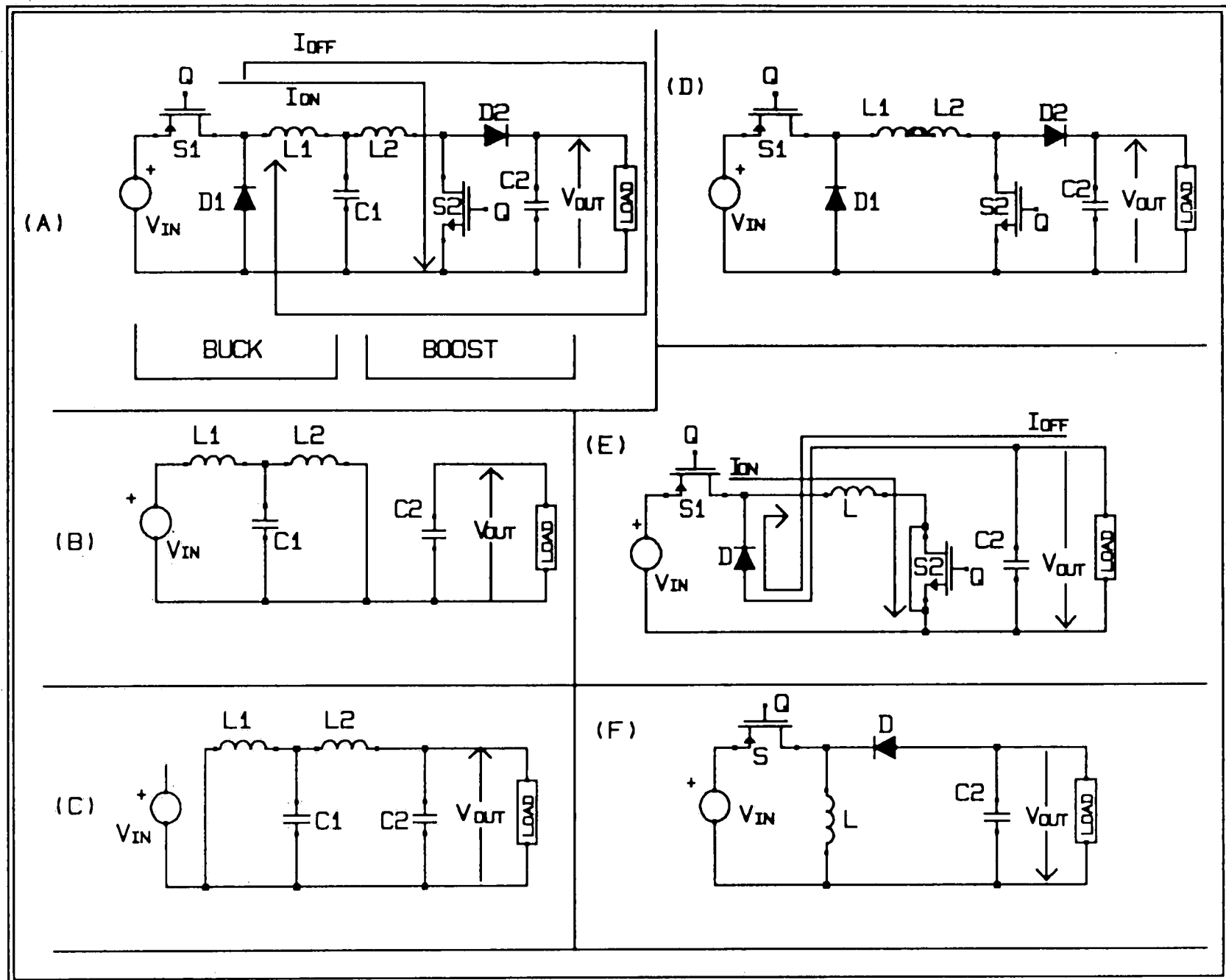
Figure 8 - The Creation of the Boost-Buck Converter from the Boost and Buck Topologies.

Although some consider the boost-buck converter to be a basic topology it can be thought of as a cascade of a buck and a boost converter. Consider the circuit shown in figure 8A consisting of a buck converter feeding the input of a boost converter. If one were to synchronize the switches it can be seen that during switch on time the current flows from the source to ground via the switches (Figure 8B). As discussed before, the only parameter which matters when the switch opens is the amount of

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energy stored in each inductor. The capacitor C1, located between the two converters, does little to alter this. By removing capacitor C1, and combining L1 and L2 into L a non-inverting two switch topology emerges (Figure 8D). The two switches can be combined into one by observing that both are only needed if polarity reversal is not desirable. Further reduction can be obtained by noting that the current flow in switch two is unidirectional so it can be replaced by a diode yielding the boost-buck topology as discused before (Figure 8E and 8F). If one examines the function for V_{out} previously derived in figure 7, one finds that it is the product of the boost and buck converter output voltage functions, further indicating the relationship between the topologies.

The CUK Converter

It can be observed from this discussion that "new" converter topologies can be synthesized from combinations of the basic boost or buck converter. As previously demonstrated, a boost buck converter is simply the cascade of two basic topologies. Of particular importance is the Cuk converter (Pronounced "Chook". Named after Dr. Slobodan Cuk) which is generated by preceding the buck converter with a boost converter; a reverse of the boost-buck topology (Figure 9A).

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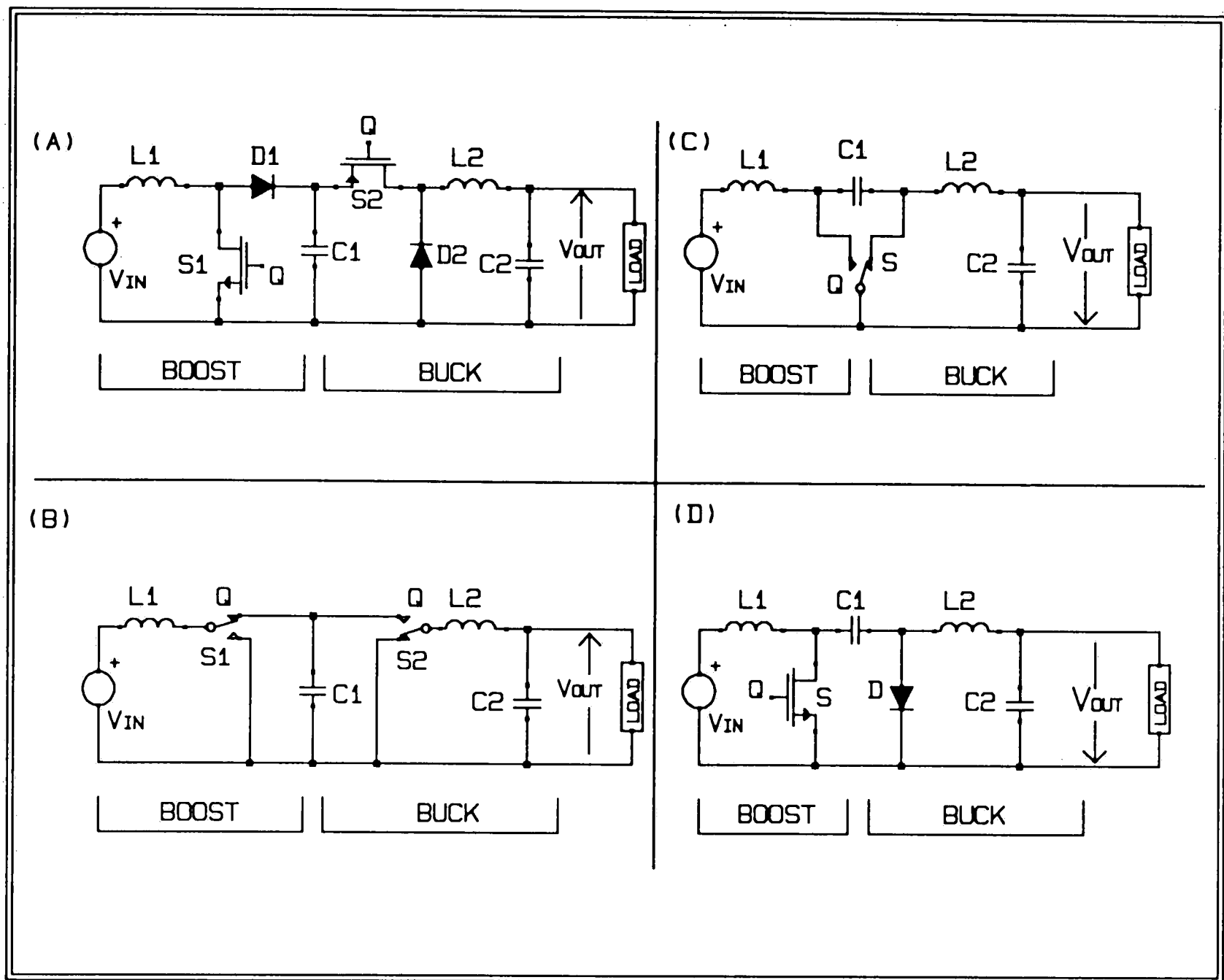
Figure 9 - The CUK Converter.

As before, integration of the two topologies starts with removing the diode and switch combinations by replacing them with there ideal switch counterparts (figure 9A to 9B). The second integrating step is observing the energy sources and sinks during each switch state. During the switch on period both inductors are being charged, one from the source and one from C1. During the switch off period inductor L1 is transferring its stored energy to C1 and inductor L2 is transferring its stored energy to the load filtered by C2. The load and the source are completely isolated during both periods of the clock. In

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this case, it is observed that the filter capacitor can not be omitted since energy stored in it during the switch off period is required to supply the second stage when the switches are on. By using the previous observations, the circuit in figure 9B can be transformed to that in figure 9C by moving C1 and combining S1 and S2. The circuit in figure 9C charges both inductors during the switch on period and discharges them during the switch off period. However, one functional difference does exist between figure 9B and 9C. The polarity of the output is inverted because the reference side of C1 is flipped between switch states.

A $\quad I_{L1(t)} := \left[I_{10} + V_{in} \dfrac{1}{L_1} t \right] \quad$ For $0 < t < DT$

B $\quad I_{L1} := \left[I_{10} + V_{in} \dfrac{1}{L_1} D\, T \right]$ For $t = DT$

C $\quad I_{L1(t)} := \left[I_{10} + V_{in} \dfrac{1}{L_1} D\, T \right] - \left[V_c + V_D - V_{in} \right] \dfrac{1}{L_1} (t - DT) \quad \begin{array}{c} \text{For} \\ (DT < t < T) \end{array}$

D $\quad I_{L1} := \left[I_{10} + V_{in} \dfrac{1}{L_1} D\, T \right] - \left[V_c + V_D - V_{in} \right] \dfrac{1}{L_1} T\, (1 - D)$ For $t = T$

E $\quad I_{L1} := I_{10} \quad 0 := \dfrac{1}{L} T \left[V_{in} - \left[V_c + V_D \right] (1 - D) \right]$

F $\quad V_c := V_{in} \dfrac{1}{1 - D} \quad$ For $V_D = 0 \quad I_0$

Figure 10 - CUK Converter Equations Part 1.

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A $\quad I_{L2(t)} := \left[I_{20} + \left[V_c - V_{out} \right] \frac{1}{L_2} t \right]$ For $(0 < t < D.T)$

B $\quad I_{L2} := \left[I_{20} + \left[V_c - V_{out} \right] \frac{1}{L_2} D T \right]$ For $t = DT$

C $\quad I_{L2(t)} := \left[I_{20} + \left[V_c - V_{out} \right] \frac{1}{L_2} D T \right] - \left[V_{out} + V_D \right] \frac{1}{L_2} (t - D T)$ For $DT < t$

D $\quad I_{L2} := \left[I_{20} + \left[V_c - V_{out} \right] \frac{1}{L_2} D T \right] - \left[V_{out} + V_D \right] \frac{T}{L_2} (1 - D)$ For $t = T$

E $\quad I_{L2} := I_{20} \quad 0 := \left[V_c - V_{out} \right] D - \left[V_{out} + V_D \right] (1 - D)$ At boundry condition

F $\quad V_{out} := D V_c - V_D (1 - D) = V_{in} \left[\frac{D}{1 - D} \right] - V_D (1 - D)$

Figure 11 - CUK Converter Equations Part 2.

Now that the CUK topology has been defined, the previously used analysis techniques can be applied to solve for V_{out} and the inductor currents. With the switch closed inductor L1 is being charged across the input source, so the current can again be described as a linear ramp defined in figure 10A. To describe the current in L2, an assumption needs to be made about the voltage across C1. The voltage across C1 should be relatively constant over a clock cycle since it is essentially the output filter capacitor of a boost regulator. With this assumption in hand, the current through L2 is simply another linear ramp described by figure 11A. When the

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switch opens, inductor L1 transfers its stored energy to C1. As discussed before, the voltage across C1 is relatively constant so the discharge current of L1 can be approximated by the equation in figure 10C. Inductor L2 is clamped across the output voltage during the switch off period, so the energy stored in it is discharged as described by figure 11C. By solving for the inductor currents at the end of each cycle, two expressions emerge: one for V_{C1} as a function of V_{in} and one for V_{out} as a function of V_{C1} (Figures 10F and 11F). Combining the two expressions yields the input voltage to output voltage function described in figure 11F. Comparing this with the individual functions of the boost and the buck converter shows that the CUK converter DC input to output function is the product of the two elementary converter input to output functions, as one would expect.

Discontinuous Operation

Up to this point we have assumed that the inductor current never reaches zero before the end of a clock cycle which implies that the load current is sufficient to maintain energy transfer during switch off time. As long as the load current is great enough to sink the energy from the inductor, the average charge on the filter capacitor will remain unchanged indicating that the output

voltage will remain constant (Figure 12A). If the output current is decreased to the point where the incremental energy stored in the inductor is greater than that consumed by the load; the excess energy will be dumped into the filter capacitor causing the output voltage of the circuit to increase until a new steady state output power is reached. An increase in steady state output voltage causes the inductor to discharge at a grater rate so the inductor current will reach zero before the end of the clock cycle as shown in figure 12B. This mode of operation is termed discontinuous operation since the inductor current flow is no longer continuous.
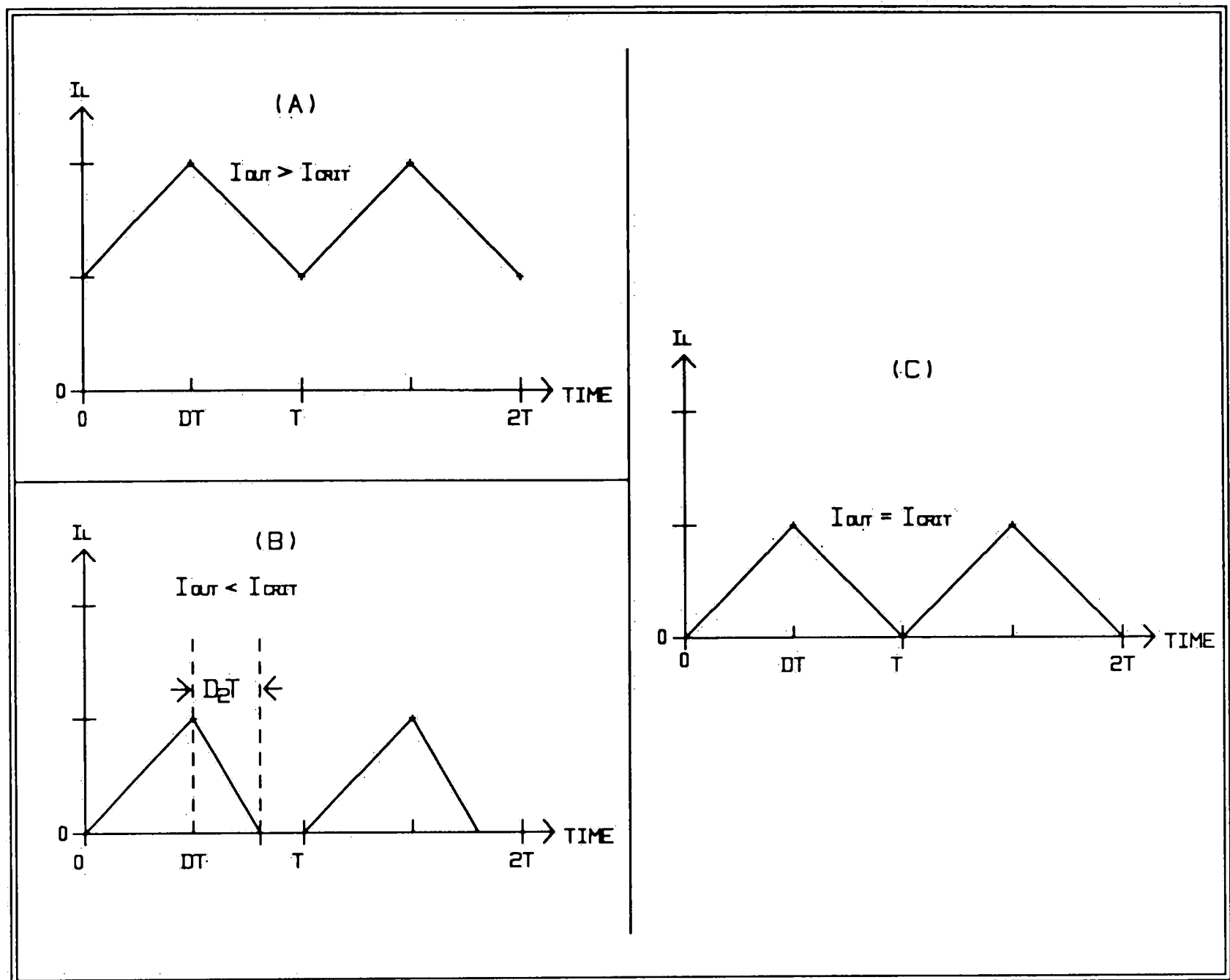
Figure 12 - Continuous vs Discontinuous Mode Inductor
Currents.

It should be noted that determining the mode of
operation the circuit is in, is of the utmost importance
when evaluating control loop stability since the loop gain
of the control loop depends on the mode of operation. The
boundary of continuous to discontinuous operation is
termed the critical load current and is defined as the
load condition that causes the inductor current to just
reach zero at the end of a cycle (Figure 12C).
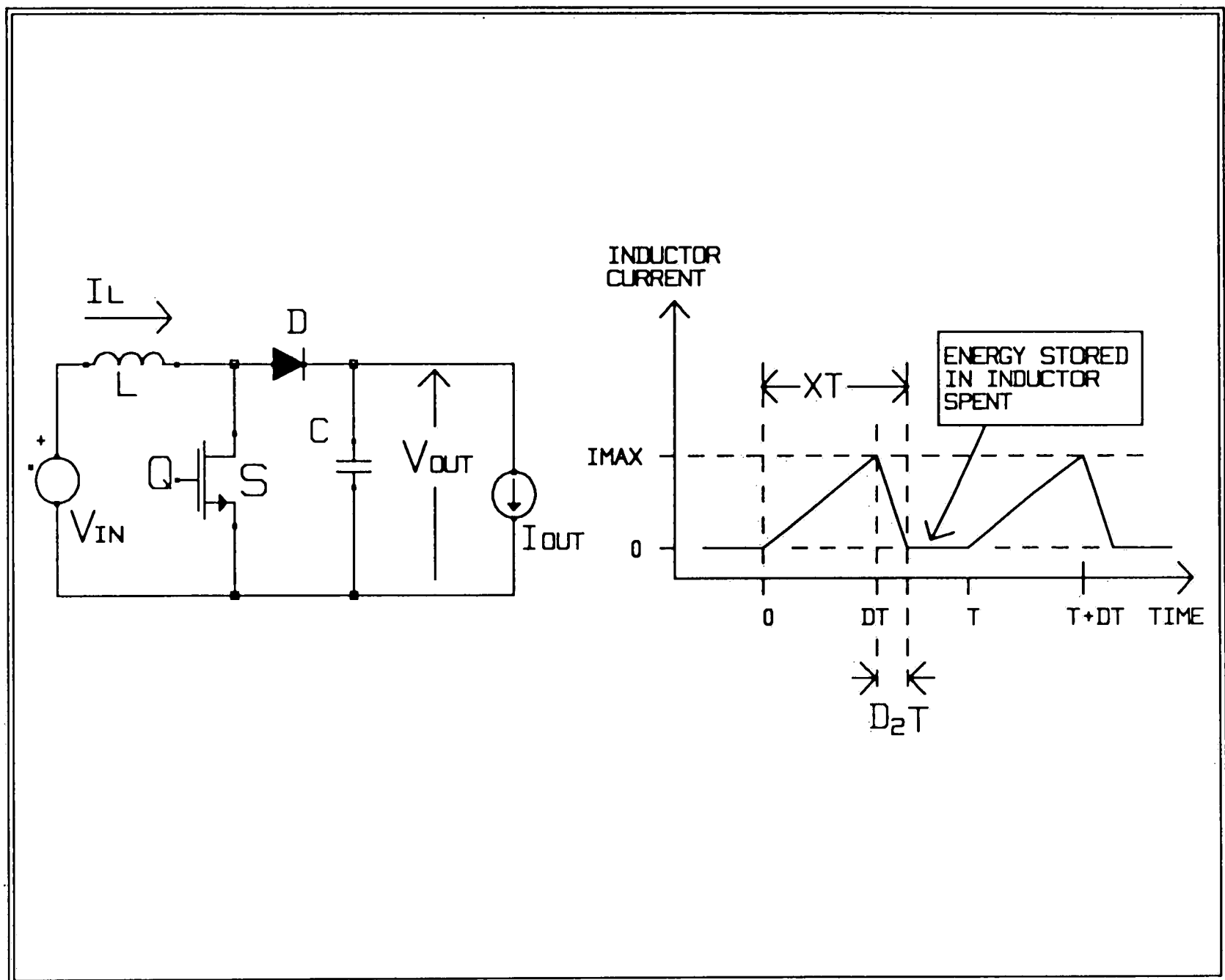
Figure 13 - Boost Regulator Operating in Discontinuous
Mode.

Consider the operation of the boost converter
operating in discontinuous conduction mode shown in
figure 13. To analyze the properties of the discontinuous
mode circuit we will assume that the inductor current
reaches zero at a point in time located between DT and T
defined as xT, and that the load voltage has stabilized to
some steady state value define as V_{out}.
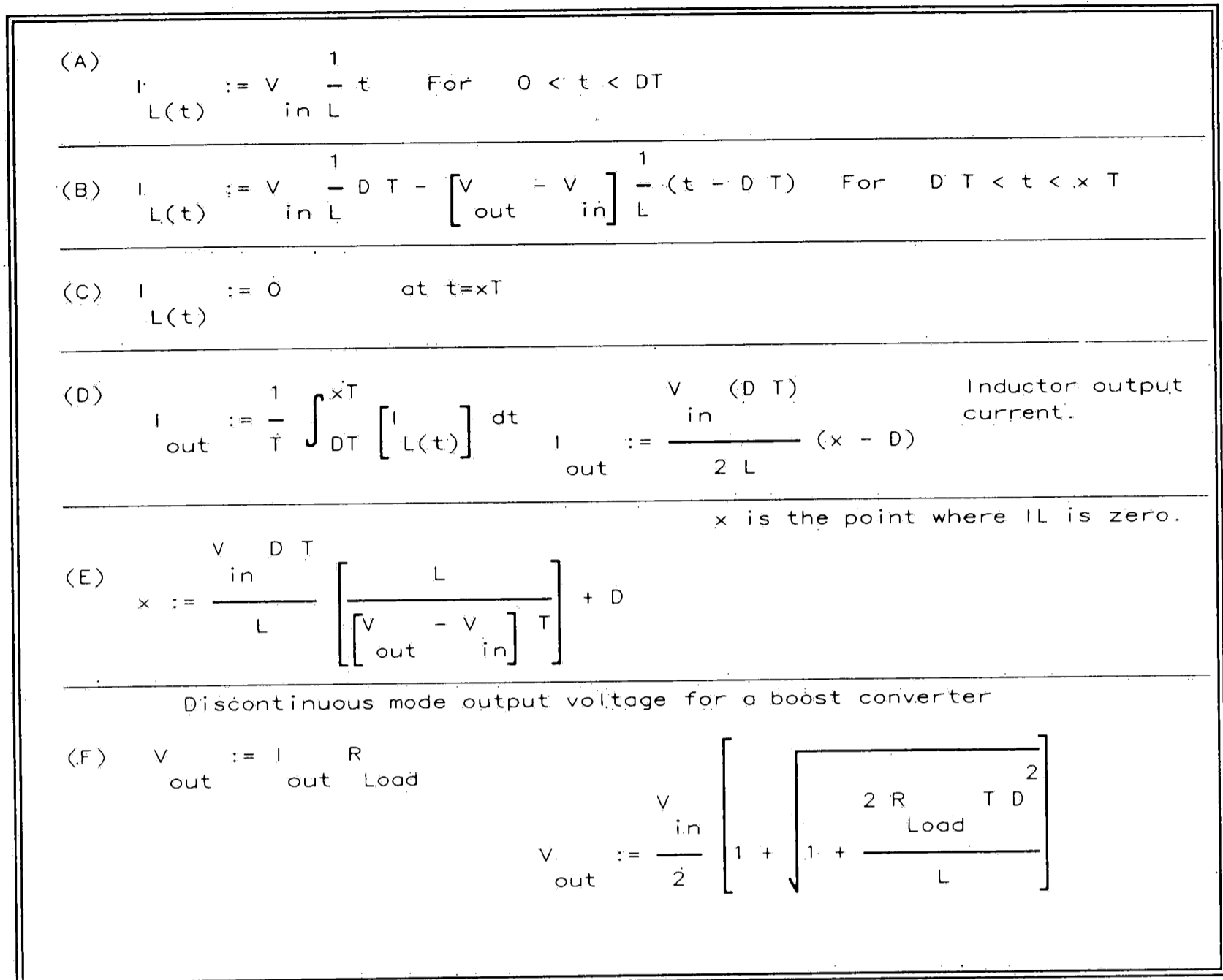
Figure 14 - Impact of Discontinuous Mode on the Boost
Regulator Input to Output Voltage Function.

For discontinuous operation the inductor always

starts charging from a totally discharged state since all

stored energy is expelled within each cycle of the clock.

As a result, the inductor charging current becomes a

simple function of duty cycle and input voltage

(figure 14A). When the switch opens up the inductor

discharges at a rate controlled by the difference between

the input and output voltages described by the equation in

figure 14B. By integrating the inductor current over the

time which current is flowing to the output a solution for

the output current as a function of dutycycle, input

voltage, and time point xT is obtained. The arbitrary
time point xT is simply the solution of equation 14B for
$I_L(t)=0$. Combining equations 14D and 14E and solving the
quadratic for V_{out} yields the discontinuous output voltage
function in equation 14F. An insight into the consequence
of discontinuous mode operation can be seen by comparing
equation 14F to the continuous case output equation. For
the continuous case the output voltage is only dependent
on duty cycle while for the discontinuous case the output
voltage is a function of the load, inductor value, clock
period, and duty cycle.

Current Mode Control

Up until now we have assumed the presence of a
feedback loop which adjusts the pulse width of the switch
to achieve output voltage regulation. Figure 15A shows a
boost-buck regulator with such a voltage feedback loop.
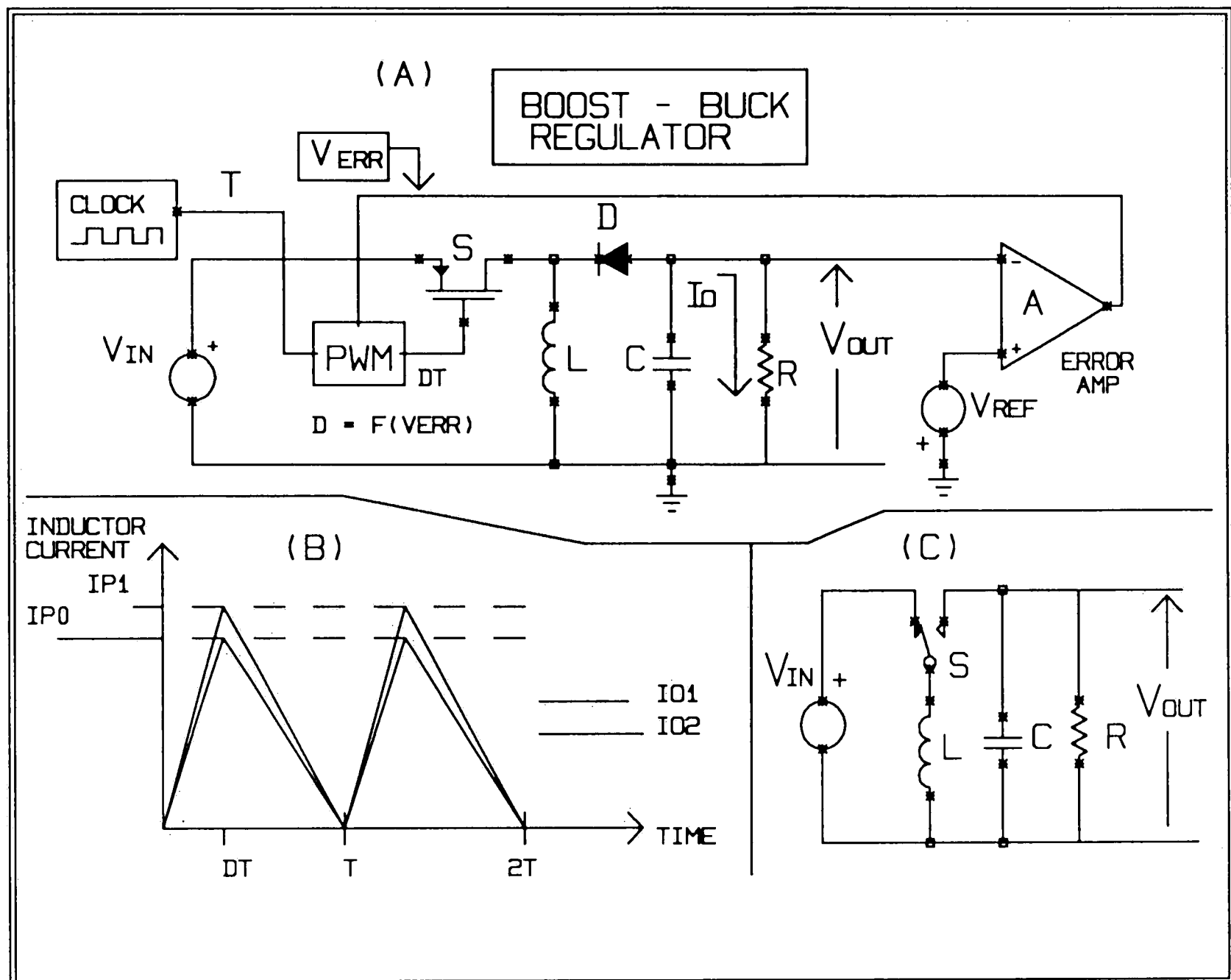
Figure 15 - Boost-Buck Regulator with a Voltage Feedback
Loop.

The feedback loop consists of an error amplifier which
feeds a correction signal to the pulse width modulator to
correct for a difference between the output and the
desired output or reference. For a constant output load
and input condition, the switch will remain at a constant
duty cycle D_1 and consequently the peak inductor current
will remain constant at I_{P0} (See figure 15B). If the
input voltage is suddenly increased then the energy stored
in the inductor must rise to a new value I_{p1} and the
output voltage must also rise until the feedback loop

responds, many clock cycles later, by decreasing the duty cycle to reduce the energy stored in the inductor. Since the source and load are disconnected during the energy storage and transfer periods, the energy transferred to the load must have been completely stored in the inductor at one time (See figure 15C). With this in mind, it stands to reason that controlling the peak inductor current in a boost-buck regulator is equivalent to controlling the output voltage for a given output load condition. If the voltage control loop were eliminated and replaced with a circuit which always charges the inductor to a preset value on every clock cycle then a change in V_{in} would not produce a change in V_{out} since the energy stored in the inductor is constant (See figure 17). Of course this is assuming that the output load condition is constant.
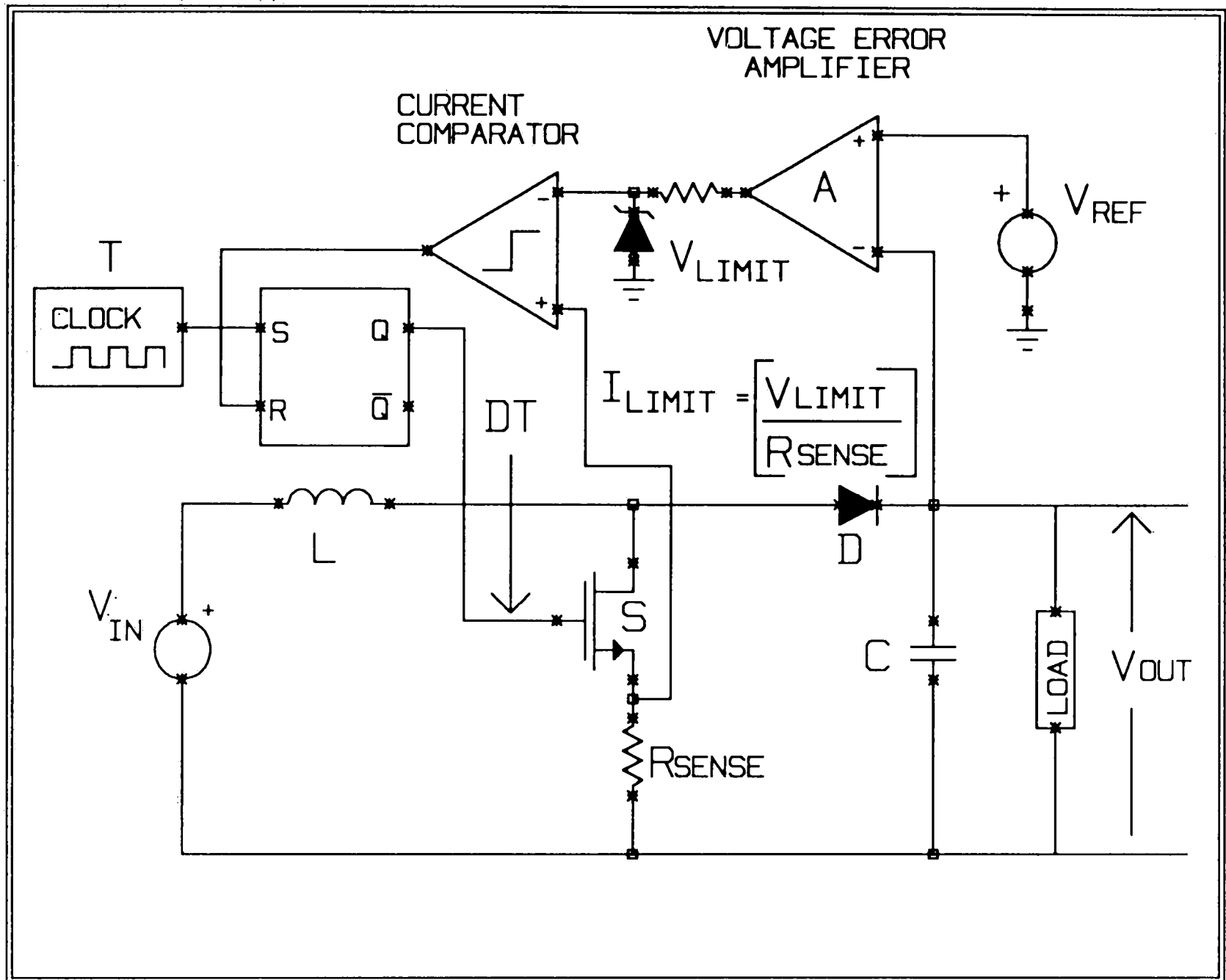
Figure 16 - Boost Regulator with Voltage and Current Feedback. (Current Mode)

Unfortunately load conditions do vary, so the previous concept must be integrated into a circuit which controls both peak inductor current and output voltage. The regulator shown in figure 16 has a secondary feedback loop which controls the peak inductor current on every cycle as a function of the error voltage generated by a primary voltage control feedback loop. The peak inductor current is fixed for a given set of output load conditions by the secondary current feedback loop. Regulating the peak inductor current inside the voltage feedback loop is

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termed current mode control. An error signal,
representing output voltage error generated from the
voltage feedback loop, controls the peak inductor current
and therefore the peak energy stored in the inductor. If
V_{in} should change, the current feedback loop compensates
by turning the switch off earlier or later depending on
the polarity of the disturbance. Current mode control can
be viewed as regulating the internal magnetic state of the
system by using the inductor current state variable as a
source of feedback. One benefit of controlling the peak
inductor current on a cycle by cycle basis is that cycle
by cycle current limiting can easily be added to a current
mode regulator by limiting the current feedback reference
signal. Cycle by cycle current limit can be used to
prevent inductor saturation. Inductor saturation can be
disastrous since the incremental inductance of a non air
core inductor decreases to a near core-less value during
saturation. A sharp decrease in inductance leads to a
rapid increase in inductor current since the inductor is
across a voltage source with a very low series resistance.
The rate of rise of switch current is inversely
proportional to the inductance, so decreasing the
inductance results in a runaway rise in inductor and
therefore switch current. High current stress of the
switch leads to semiconductor reliability limitations and
consequently should be avoided at all costs if future

component failures are to be avoided. Converters using
current mode control may have their outputs paralleled
without the fear of one supply current hogging. This
often is a requirement for high reliability systems.

Current mode control is not without some problems.
When used in the boost topology duty cycles must be
limited to less than 50% in order to prevent sub-harmonic
instability. Sub-harmonic instability is a oscillatory
effect which occurs independent of the presence of the
primary voltage feedback loop. Consider the operation of
the open loop current mode boost converter in figure 17.
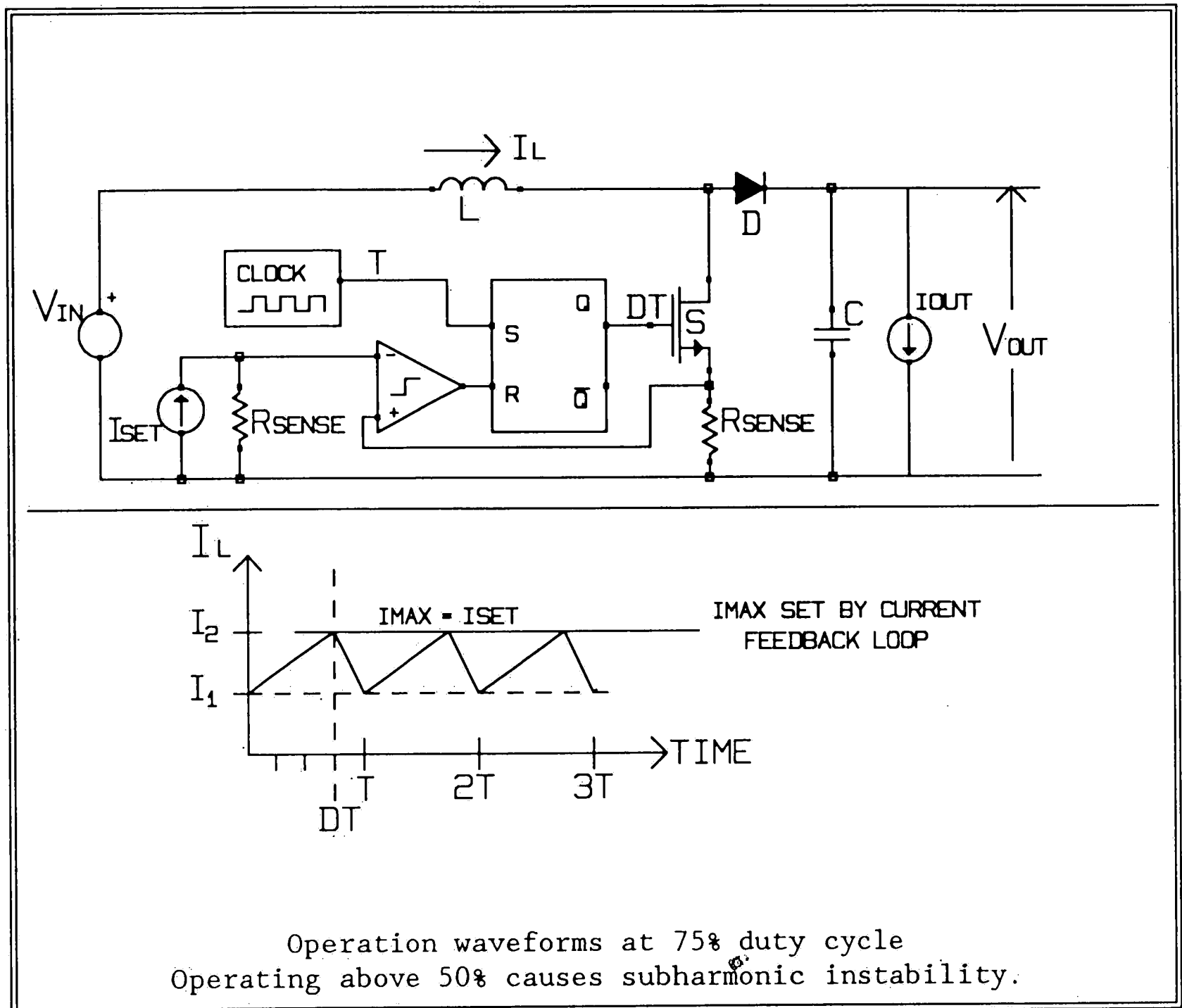
Figure 17 - Boost Regulator with Current Mode Feedback.

The waveforms shown look reasonable as derived from simple energy transfer methods but deficiencies are hidden in this type of analysis. Complications begin to show up if one inserts a small one cycle long glitch in the inductor current and follows the added current through successive cycles of the clock. The glitch can be viewed as a change in inductor charging slope perhaps caused by a disturbance in V_{in} which causes the inductor current at the end of the clock cycle not to equal the inductor current at the beginning of the cycle.

Consider the waveform shown in figure 18 where the inductor current relative to the minimum steady state inductor current is plotted against time. The first cycle displayed shows the inductor charging from I_{min} to the peak current set point I_{max} with a slope of m_1 and then discharging from I_{max} to I_{min} with a slope of m_2. On the second cycle the glitch energy is added to alter the charging rate so the inductor charges with a slope of (m1 + del) where del is caused by a glitch added to the supply of the regulator. For the case shown, the glitch causes the inductor to reach I_{max} earlier than expected. The inductor now discharges until the end of the clock cycle to a lower current than from which it began. The current is plotted as relative to "ideal current" so the graphed current at the end of each cycle is the glitch current for that cycle resulting from the initial glitch during the second cycle. Figure 19 provides a magnified view of the inductor current on the second cycle of the clock. Successive cycles of the clock depict the propagation of the glitch energy added on cycle number two through the next eight cycles. If we evaluate the glitch at the end of each clock interval it is obvious from figure 18 that the inductor current is unstable for this condition in view of the glitch energy growing from one cycle to the next.

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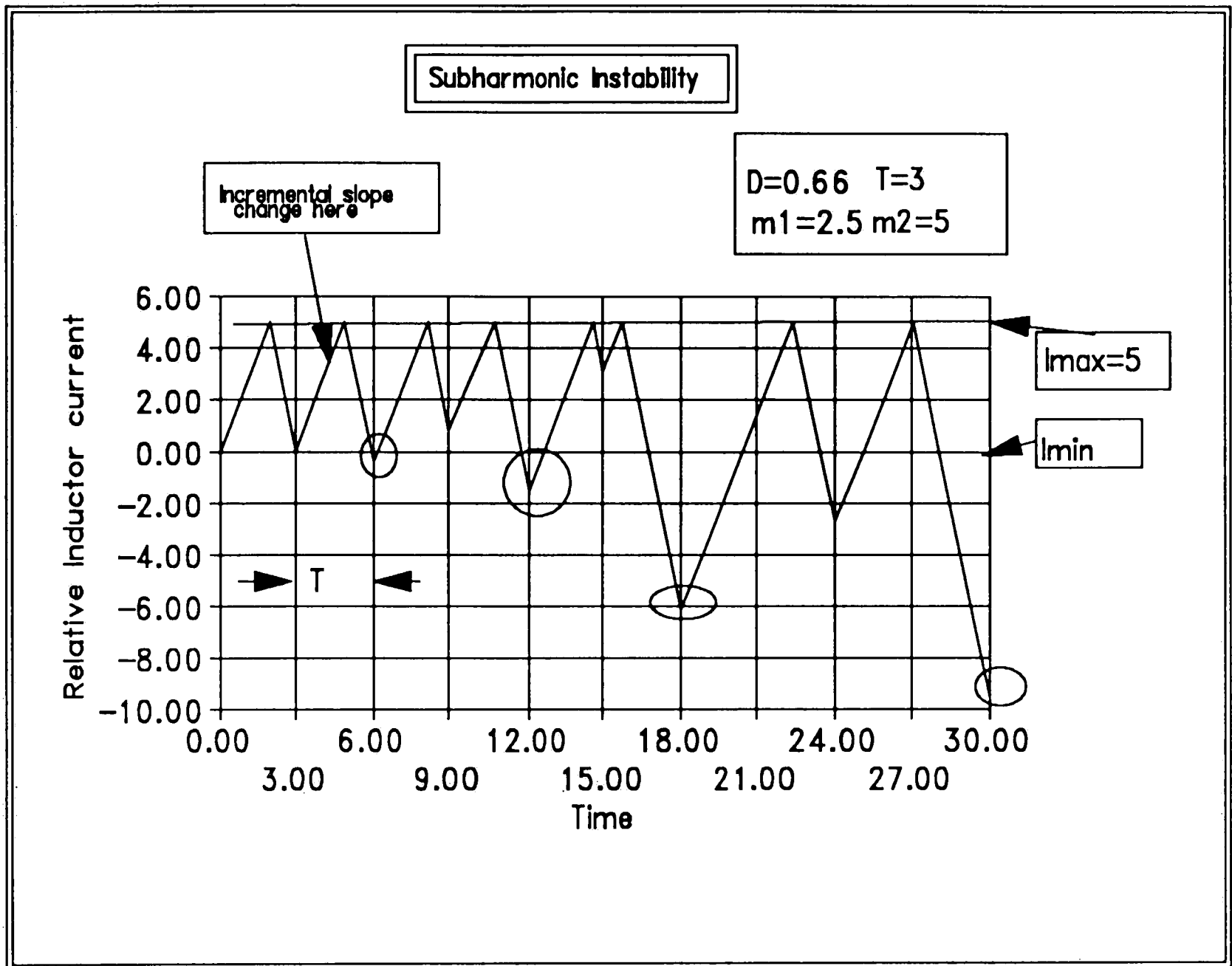
Figure 18 - Plot Showing Subharmonic Instability.
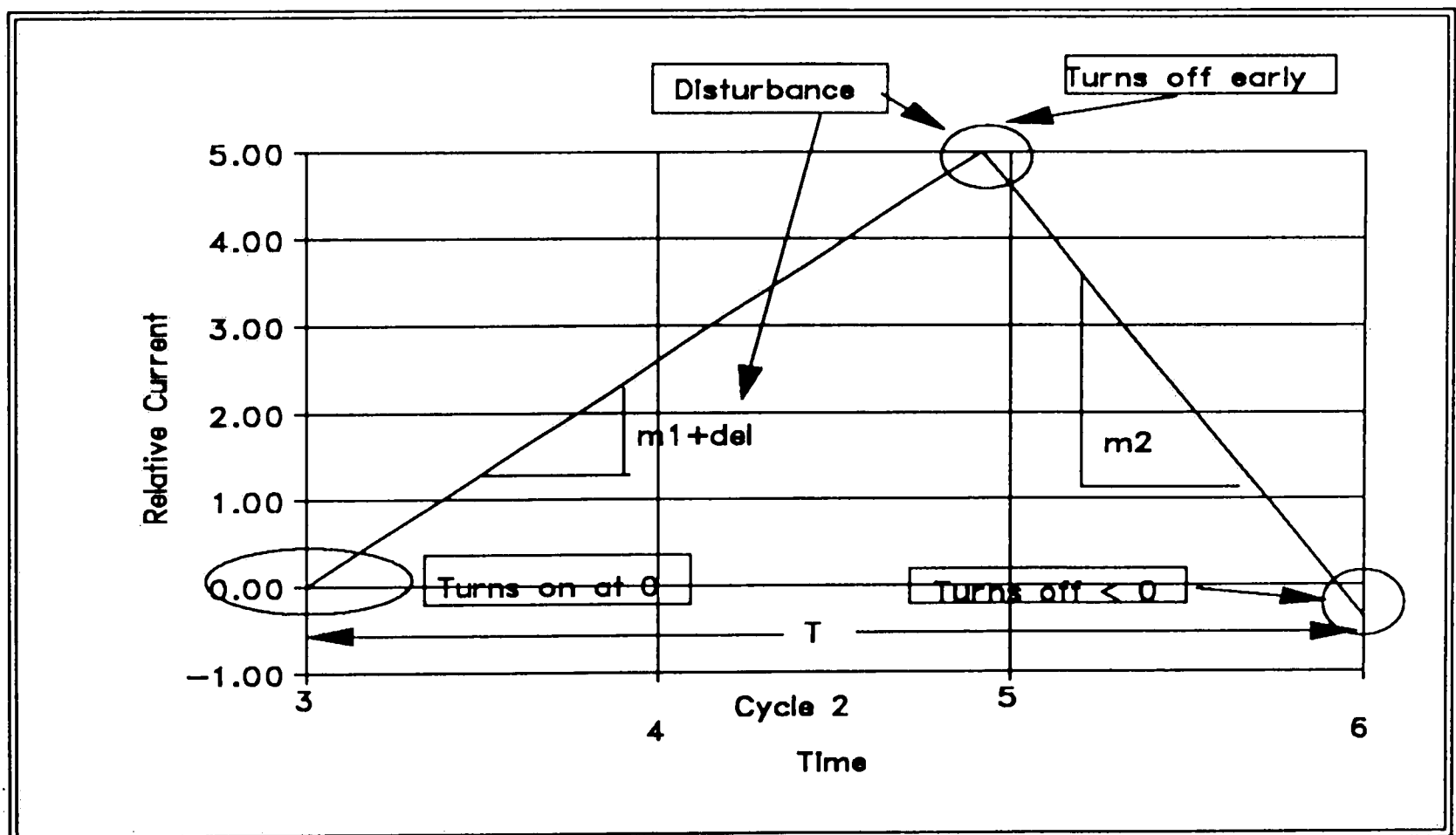
Figure 19 - Magnified Second Cycle of Previous Plot.
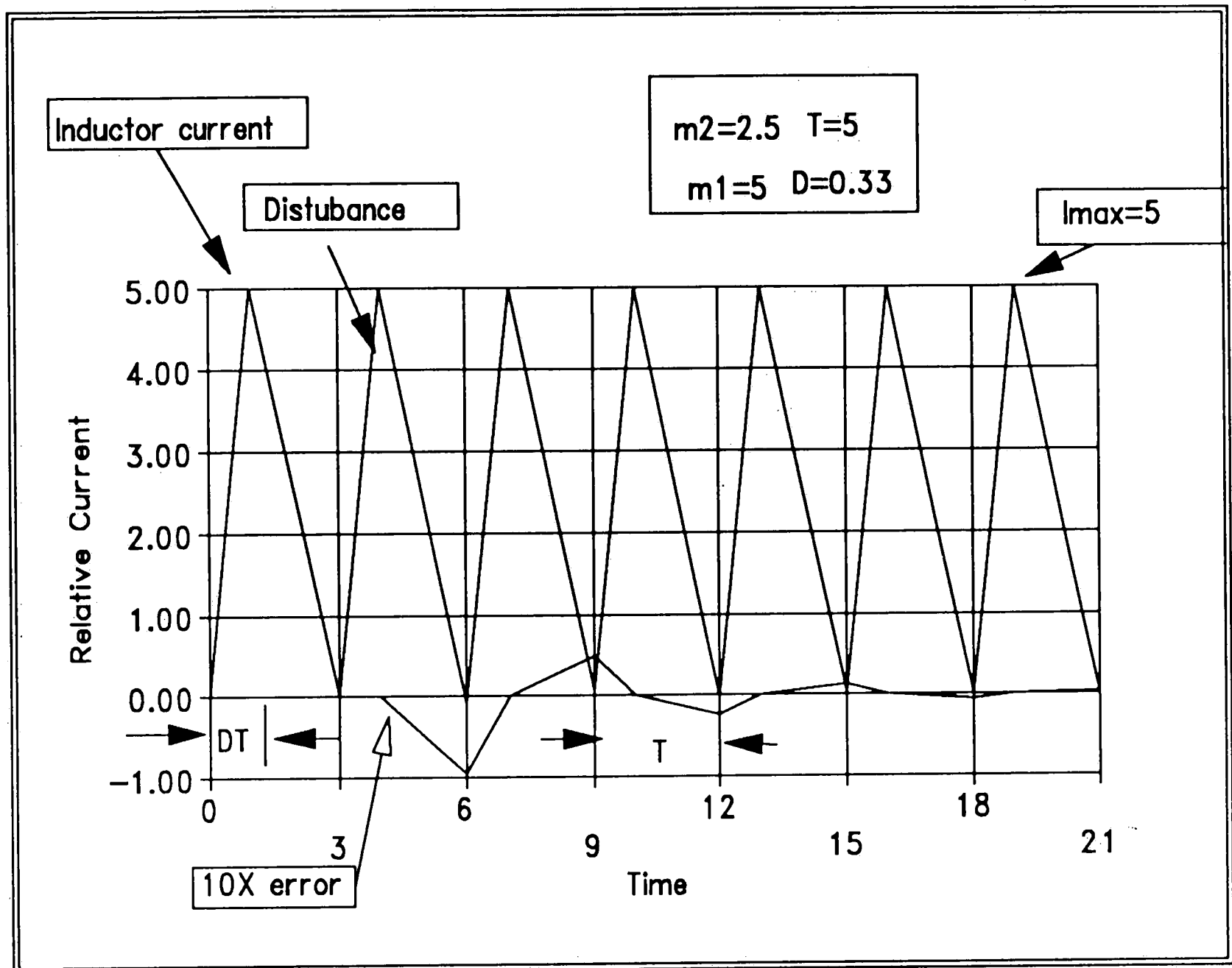
Figure 20 - Plot Showing Lack of Subharmonic Instability.
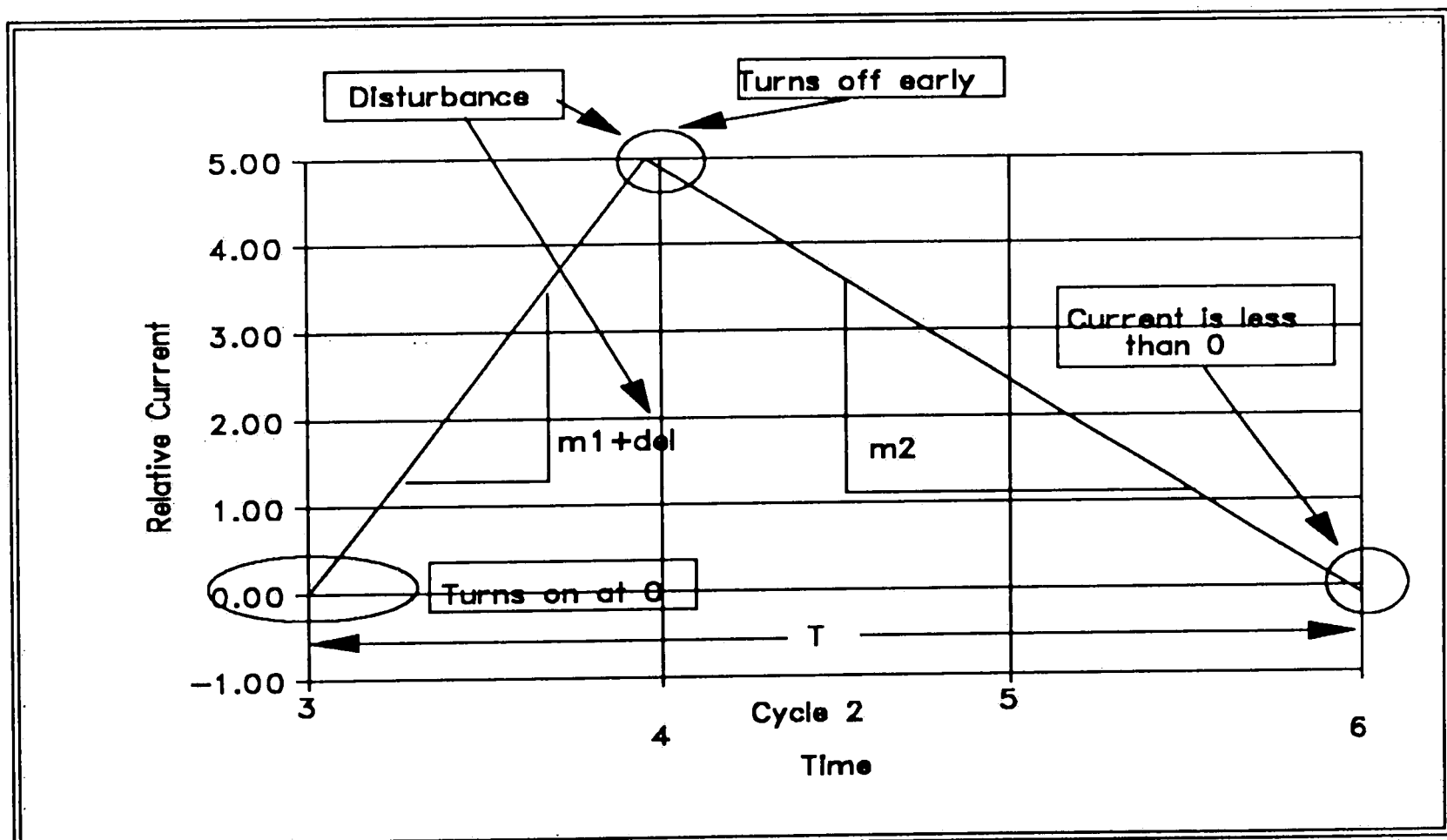
Figure 21 - Magnified Second Cycle of Previous Plot.

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If we change the duty cycle of the regulator to 33% as shown in figure 20; and again insert the glitch energy on cycle number two, a different result is uncovered. The added glitch energy decays to zero over the next few cycles of the clock. A dramatic difference between the 66% duty cycle case and the 33% duty cycle case is demonstrated by the need to plot the glitch energy at ten times its actual value for the 33% case to even see its effect on successive cycles. For the 33% duty cycle case the added glitch energy decays instead of growing as it did before which indicates that the system is stable.

A more quantitative solution to the problem can be obtained by assigning the notation d_n as the current glitch magnitude on clock cycle number n and d_{n+k} as the magnitude of the initial glitch current after k clock cycles from n. One can develop a open form expression for the glitch current by inserting the initial glitch on cycle n and developing an expression for the glitch size on cycle n+1, n+2, $\cdots$, and n+k as done in figures 22C-22G. A closed form expression for the glitch current can be realized by substituting equation 22C into equation 22H and reducing the infinite sum as demonstrated in equation 22H.

(A) Insert glitch on rising edge

$$i_2 := \left[i_1 + \delta_n + m_1 \cdot d \cdot T\right]$$

(B) Predict i1 from i2

$$i_1 := \left[i_2 - m_2 \cdot \left[1 - d_n\right] T\right]$$

(C) Steady state peak to peak amplitude

$$\left[i_2 - i_1\right] := \cfrac{\dfrac{m_2 \cdot T}{2}}{1 + \dfrac{m_2}{m_1}}$$

(D) Minimum current on the next cycle after the initial glitch was added.

$$\delta_{n+1} + i_1 := i_2 - m_2 \cdot \left[1 - d_n\right] \cdot T$$

(E) Added glitch current from cycle n propagated to cycle n+1

$$\delta_{n+1} := \left[\left[i_2 - i_1\right] \cdot \left[1 + \frac{m_2}{m_1}\right] - m_2 \cdot T\right] - \delta_n \cdot \frac{m_2}{m_1}$$

(F) Added glitch current from cycle n propagated to cycle n+2 as a function of the previous cycle

$$\delta_{n+2} := \left[\left[i_2 - i_1\right] \cdot \left[1 + \frac{m_2}{m_1}\right] - m_2 \cdot T\right] - \delta_{n+1} \cdot \frac{m_2}{m_1}$$

(G) Substitute E into F

$$\delta_{n+2} := \left[\left[i_2 - i_1\right] \cdot \left[1 + \frac{m_2}{m_1}\right] - m_2 \cdot T\right] \cdot \left[1 - \frac{m_2}{m_1}\right] + \delta_n \cdot \left[\frac{m_2}{m_1}\right]^2$$

(H)

$$\delta_{n+k} := \underbrace{\left[\left[i_2 - i_1\right] \cdot \left[1 + \frac{m_2}{m_1}\right] - m_2 \cdot T\right]}_{\text{Substitute equation C}} \cdot \underbrace{\left[1 + \sum_j \left[\frac{-m_2}{m_1}\right]^j\right]}_{} + \delta_n \cdot \left[\frac{-m_2}{m_1}\right]^K$$

$$\left[\frac{1}{1 + \frac{-m2}{m1}}\right] \quad \text{As } j \longrightarrow inf$$

(I)

$$\delta_{n+\infty} := \delta_n \cdot \left[\frac{-m_2}{m_1}\right]^\infty$$

(K)

$$\delta_{n+\infty} := \infty \quad for \quad \left[m_2 > m_1\right] \quad (d < .5)$$

$$\delta_{n+\infty} := 0 \quad for \quad \left[m_2 < m_1\right] \quad (d > .5)$$

Figure 22 - Quantitative Subharmonic Instability Derivation.

The closed form expression in figure 22I indicates that the glitch current decays for the condition of the time rate of inductor charge current greater than the time rate of discharge. In the opposite condition the glitch current grows leading us to the conclusion that the system is unstable.

Intuitively one can translate the inductor charging slope boundary condition ($m_1 = m_2$) to the condition where duty cycle equals fifty percent (D=0.5); therefore a current mode boost regulator operating in continuous conduction mode is unstable for duty factors greater than fifty percent (Figure 23). This finding concurs with the previous graphic example. It should be noted that this condition does not occur if the regulator in operating in discontinuous mode.
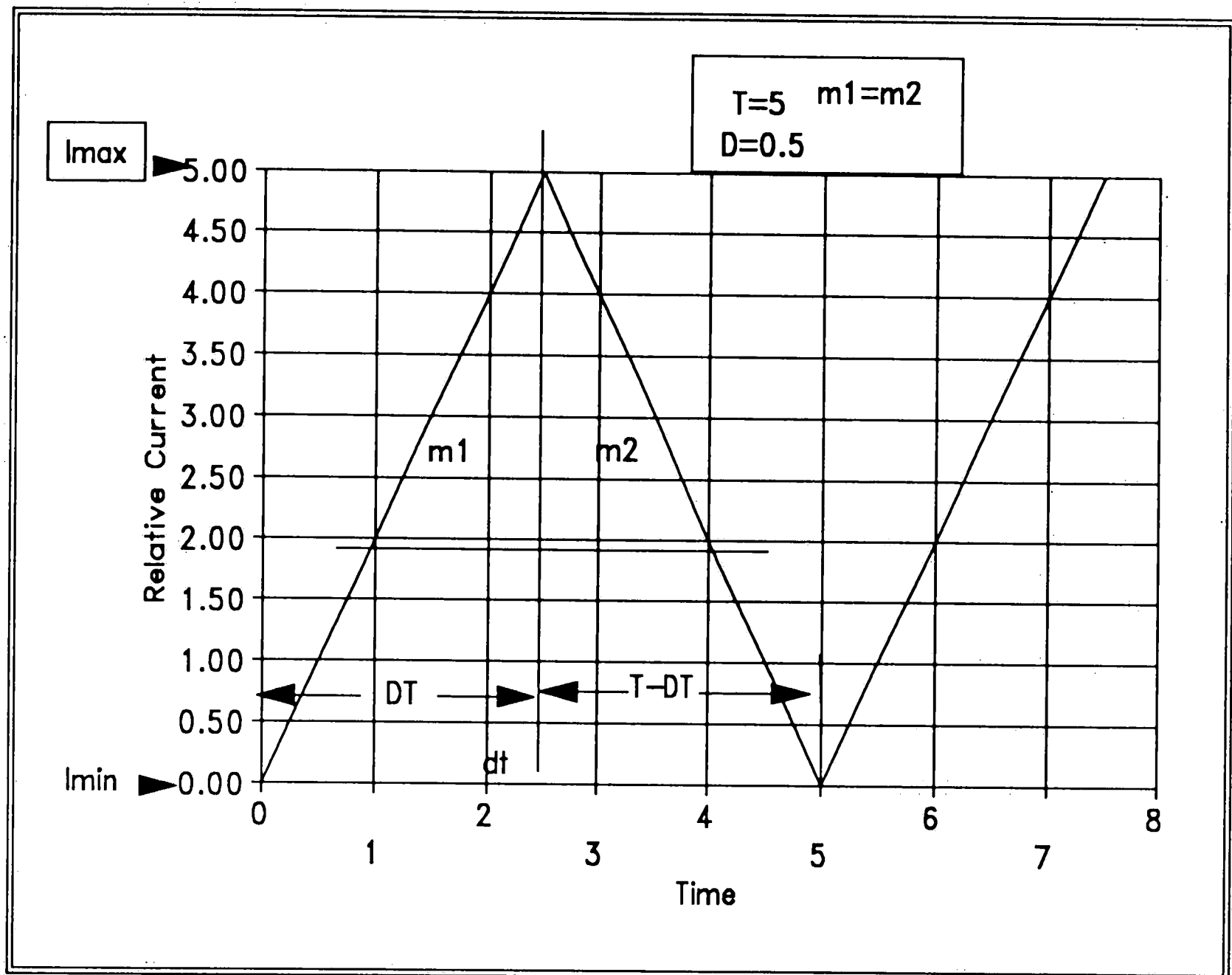
Figure 23 - Slope to Duty Cycle Linkage

Fortunately there are ways to alleviate subharmonic
instability without limiting the duty cycle of the
regulator to less then fifty percent. A technique known
as slope compensation modulates the current feedback
loop's peak inductor current set point as a function of
switch duty cycle. This is accomplished by deriving a
ramp from the clock and adding it to the sensed inductor
current or to the voltage error amplifier output. Some
integrated controllers such as the National LM1577-xx
provide slope compensation within the IC while others

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require the user to add peripheral circuitry to accomplish the task.

Analysis Techniques

At first look one might be tempted to consider a raw transient analysis approach using a generalized analysis program such as Spice for the analysis of switching regulator circuits. The drawbacks of this approach are that simulation times will be excessive and the stability of the control loop is often ignored due to the neglect of small signal analysis. Spice can only perform a small signal analysis in one state of the circuit at a time unless something is done to generate a circuit model which represents both states in one circuit.

It soon becomes obvious that more than one analysis technique may be required for every design. One technique is needed to determine the large signal state of the magnetics while another is needed to determine the stability of the feedback loop(s), input impedance, and output impedance. Small signal approaches must somehow combine the small signal models of the various switch states into one simulateble model which can be used to predict control loop stability. To be of any use, a solution must characterize the input to output path as well as the duty cycle to output of the circuit under

study. Modeling and analysis techniques must provide design insight into the circuit operation as well as solve the problem at hand. In the quest for accurate design tools the need for non-laborious solutions must not be overlooked.

State Space Averaging

State space averaging is a technique which is an extension of state variable analysis techniques used in linear circuit analysis. Let us first consider the state variable analysis of the linear time invariant LCR circuit shown in Figure 24A.
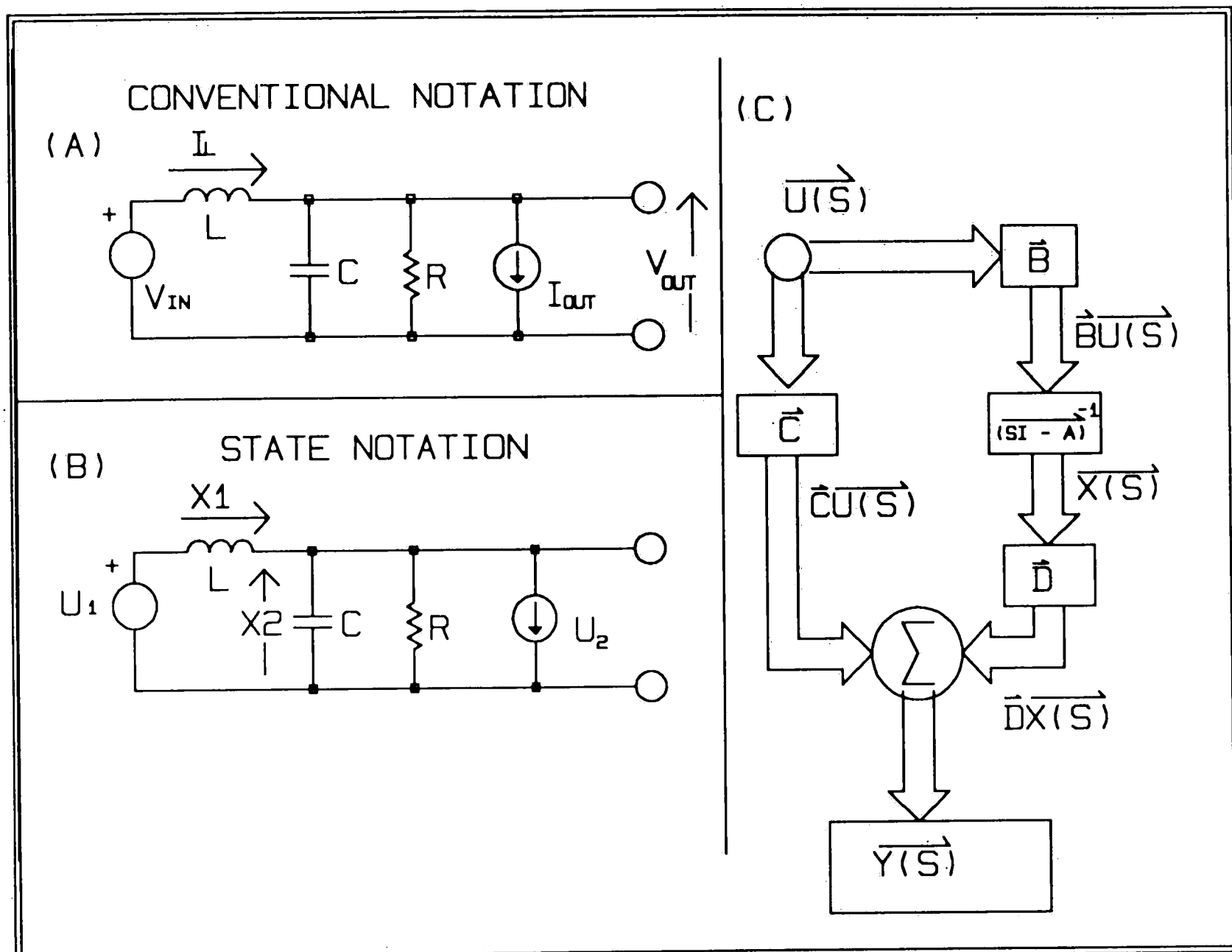
Figure 24 - Linear LCR circuit with Conventional and State Notation.

By writing a loop equation for V_{out} and a node equation for I_L one can rearrange the terms of each equation to solve for the derivatives of the inductor state I_L and the capacitor state V_C (See figure 25A and 25B). This now can be written in the general form shown in figure 25C where vector X represents the states of the two energy storing elements, vector U represents the input(s) to the system, matrix A describes the sourceless properties of the network, and matrix B describes the reaction of the system to the source vector. A solution for the state variables of the system may be solved for by converting the

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derivatives to a Laplace transform representation and applying the manipulation shown in figures 25D and 25E.

$$\text{(A)} \quad \frac{d}{dt}\,V_{out} := \frac{1}{C}\,I + \frac{-1}{RC}\,V + \frac{-1}{C}\,I_{out} \qquad\qquad \text{(B)} \quad \frac{d}{dt}\,I := \frac{1}{L}\,V + \frac{1}{L}\,V_{in}$$

General State Equation

$$\text{(C)} \quad \left[\frac{d}{dt}\,\vec{X}\right] := \left[A\,\vec{X} + B\,\vec{U}\right] \text{ Where } -----> \quad \vec{X} := \begin{bmatrix} I_L \\ V \\ C \end{bmatrix} \qquad \vec{U} := \begin{bmatrix} I_{out} \\ V_{in} \end{bmatrix}$$

Laplace Representation

$$\text{(D)} \quad S\,\vec{X}(S) := A\,\vec{X}(S) + B\,\vec{U}(S).$$

$$\vec{A} := \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \qquad \vec{B} := \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix}$$

Solution for state variables

$$\text{(E)} \quad \vec{X}(S) := \left[S\,\vec{I} - \vec{A}\right]^{-1} \vec{B}\,\vec{U}(S)$$

$$\vec{Y}(S) := \begin{bmatrix} V_{out} \\ I_R \end{bmatrix} \qquad \vec{C} := \begin{bmatrix} 0 & 1 \\ 0 & \frac{1}{R} \end{bmatrix}$$

Solution for output variables

$$\text{(F)} \quad \vec{Y}(S) := C\,\vec{X}(S) + D\,\vec{U}(S) \text{ Where } ----> \quad \vec{D} := \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$$

Figure 25 - Linear State Analysis of a LCR Circuit.

In most cases the state variables are not the variables of interest so a method to obtain the desired output variables is needed. The desired output variables represented by Y(S) in figure 24C and 25F are simply a sum of the state variables X(S) and the input source vector U(S) weighted by the matrices C and D.

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In order to apply the previously described technique to any system, the state variables must be a continuous linear function of time. Obviously switching regulators meet this criteria within each condition of the switch since they are combinations of linear circuit elements, but fail to meet the criteria across switch transition boundaries. If one were to separate the system into equivalent linear circuits for each condition of the system; the state variables within each time cell of these linear circuits could be solved for in a piecewise manner using the previously mentioned techniques provided that the boundary condition between each switch condition is known (See figure 26).

Generalized state equations for n time periods

within a period kT (k>=0

note that there are n unique A and B matrices pairs one

for each state of the system.

$x'(t) = A_1 x(t) + B_1 u(t)$ $\{kT < t < kT+t_1-\}$

$x'(t) = A_2 x(t) + B_2 u(t)$ $\{kT+t_1+ < t < kT+t_2-\}$

$x'(t) = A_3 x(t) + B_3 u(t)$ $\{kT+t_2+ < t < kT+t_3-\}$

· · ·

$x'(t) = A_n x(t) + B_n u(t)$ $\{kT+t_{n-1}+ < t < (k+1)T-\}$

Figure 26 - Generalized State Equations for a n Switch Condition Network.

Solving the separate state equations at each boundary condition for every clock cycle would become a computation intensive task which negates the original intent of modeling the system to allow classical small signal analysis techniques to be utilized. Since the switching regulator is discontinuous by its nature, it is necessary to force the system into a continuous representation by ignoring the switching components present in the state variables. In short, we are only interested in the value of the state variables $X(t)$ just before a change in system condition such as a switch transition point.

For initial discussion sake, let's consider the case of a system with two switch states ($n=2$). If we redefine the switch condition time intervals { t_1, t_2,..t_n } shown in figure 26 as percentages of the periodic interval T; t_1 on the kth cycle would be denoted { $d_{<1,k>}T$ }. Two state equations are now needed to describe the system, one for each switch condition. The first state equation describes the system during the time period $d_{<1,k>}T$, where the switch is closed while a second state equation is needed for the time period $d_{<2,k>}T = \{ 1 - d_{<1,k>}T \}$, where the switch is off. Matrices A_1 and B_1 describe the system while the switch is on and matrices A_2 and B_2 describe the system when the switch is off. In order to merge the two state equations into one, we must ignore the switching

components present in X(t) which implies that we are
sampling X(t) just before the switch transition points but
not during the actual transition where a discontinuity in
the signal is known to exist. We can consider X(kT) and
X((k+d)T) to be a sampled data representation of a
continuous version of X(t) with samples at the beginning
of the respective interval; whether it be the switch
opening or switch closing interval. Two state equations
may now be written in figures 27A-D using the sampled data
signal in place of the previously used continuous signals
X(t) and U(t). If we assume that the clock interval T is
much smaller than the smallest period of interest desired
from the analysis, then the derivative of the discrete
state variables X(kT) and X(kT+dT) may be approximated by
calculating the slope with respect to time between samples
(figures 27E and 27F).

$$(A)\quad \frac{d}{dt}X(t) := A_1\,X(t) + B_1\,U(t)\qquad \text{For}\quad kT \le t < (k+d)T$$

Where k is the cycle number

$$(B)\quad \frac{d}{dt}X(t) := A_2\,X(t) + B_2\,U(t)\qquad \text{For}\quad (k+d)T \le t < (k+1)T$$

Two State equations one for each switch condition

$$(C)\quad \frac{d}{dt}X(KT) := A_1\,X(kT) + B_1\,U(kT)\qquad \text{Evaluated at beginning of cycle k}$$

$$(D)\quad \frac{d}{dt}X((k+d)T) := A_2\,X((k+d)T) + B_2\,U((k+d)T)\qquad \text{Evaluated at end duty cycle k}$$

$$(E)\quad \frac{d}{dt}X(KT) := \left[\frac{X((k+d)T) - X(kT)}{d\,T}\right]\qquad \text{Slope at beginning of cycle k}$$

$$(F)\quad \frac{d}{dt}X((k+d)T) := \left[\frac{X((k+1)T) - X((k+d)T)}{(1-d)T}\right]\qquad \text{Slope at end of duty cycle k}$$

Approximate derivatives of X

Figure 27 - Sampled Data State Equations.

Inserting the approximated derivatives into the generalized state equation for each switch condition and changing the dependent variable time to the sample time generates a state equation for each switch condition on the kth cycle as detailed in figures 27E and 27F.

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$$(A) \quad \left[\frac{\overrightarrow{X((k+d)\,T)} - \overrightarrow{X(k\,T)}}{d\,T} \right] := \left[\overrightarrow{A_1}\,\overrightarrow{X(k\,T)} + \overrightarrow{B_1}\,\overrightarrow{U(k\,T)} \right] \quad \begin{array}{l}\text{Switch closed}\\\text{evaluated beginning}\\\text{of the cycle}\end{array}$$

$$(B) \quad \left[\frac{\overrightarrow{X((k+1)\,T)} - \overrightarrow{X((k+d)\,T)}}{(1-d)T} \right] := \left[\overrightarrow{A_2}\,\overrightarrow{X((k+d)\,T)} + \overrightarrow{B_2}\,\overrightarrow{U((k+d)\,T)} \right] \quad \Box$$

Switch open evaluated at the
beginning of the duty cycle

$$(C) \quad \overrightarrow{X((k+d)\,T)} := d\,T \left[\overrightarrow{A_1}\,\overrightarrow{X(k\,T)} + \overrightarrow{B_1}\,\overrightarrow{U(k\,T)} \right] + \overrightarrow{X(k\,T)}$$

$$(D) \quad \overrightarrow{X((k+1)\,T)} := (1-d)\,T \left[\overrightarrow{A_2}\,\overrightarrow{X((k+d)\,T)} + \overrightarrow{B_2}\,\overrightarrow{U((k+d)\,T)} \right] + \overrightarrow{X((k+d)\,T)}$$

Figure 28 - Sampled Data State Equations.

By choosing the beginning of the clock cycle as the reference point and applying the manipulations in figures 28A and 28B; an equation representing the value of the sampled state variables on the next clock cycle as a function of the current clock cycle is formed in figure 28C and 28D. The equation in figure 29A has terms which are first and second order functions of the clock period T that we have already assumed to be small compared to the period of interest. By setting second order time terms to zero and approximating the source vector U at time (k+dT) with its derivative in equation 29B, a function which

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describes the state difference between successive cycles emerges in figures 29C and 29D. The expression in figure 29D is obviously the original approximation of the derivative of the state variable X(t) evaluated from the samples at k. It should be reiterated that this is an approximation which holds true as long as T is small compared to the period of the input signal U(t) and the yet to be defined duty cycle signal d(s).

Comparing the equation in figure 29D to the general form of a state equation for a continuous system previously introduced in figure 25C, one can see the similarities between the two cases. New matrices A and B are formed which are a weighted sum of the matrices A_1, A_2, B_1, and B_2; previously defined for each switch condition (Figure 30).

(A)
$$\overrightarrow{X((k+1)\ T)} := \left[\overrightarrow{(1-d)\ T\ \overrightarrow{A}_2\ d\ T\ \overrightarrow{A}_1\ \overrightarrow{X(k\ T)}}\right] + \left[\overrightarrow{(1-d)\ T\ \overrightarrow{A}_2\ d\ T\ \overrightarrow{B}_1\ \overrightarrow{U(K\ T)}}\right] \ldots$$

$$+ \left[(1-d)\ T\ \overrightarrow{A}_2\ \overrightarrow{X(k\ T)}\right] + \left[(1-d)\ T\ \overrightarrow{B}_2\ \overrightarrow{U((k+d)\ T)}\right] \ldots$$

$$+ d\ T\ \overrightarrow{A}_1\ \overrightarrow{X(k\ T)} + d\ T\ \overrightarrow{B}_1\ \overrightarrow{U(k\ T)} + \overrightarrow{X(k\ T)}$$

(B)
$$\overrightarrow{U((k+d)\ T)} := \left[\overrightarrow{U(k\ T)} + d\ T\ \frac{d}{dt}\ \overrightarrow{U(k\ T)}\right]$$

(C)
$$\left[\overrightarrow{X((k+1)\ T)} - \overrightarrow{X(k\ T)}\right] := \left[(1-d)\ T\ \overrightarrow{A}_2\ \overrightarrow{X(k\ T)}\right] + \left[(1-d)\ T\ \overrightarrow{B}_2\ \overrightarrow{U(k\ T)}\right] \ldots$$

$$+ d\ T\ \overrightarrow{A}_1\ \overrightarrow{X(k\ T)} + d\ T\ \overrightarrow{B}_1\ \overrightarrow{U(k\ T)}$$

(D)
State side   Source side
$$\left[\frac{\overrightarrow{X((k+1)\ T)} - \overrightarrow{X(k\ T)}}{T}\right] := \overrightarrow{X(k\ T)}\left[(1-d)\ \overrightarrow{A}_2 + d\ \overrightarrow{A}_1\right] + \overrightarrow{U(k\ T)}\left[(1-d)\ \overrightarrow{B}_2 + d\ \overrightarrow{B}_1\right]$$

Figure 29 - State Equations for a Two Condition System.

Coefficient matrices for state space averaged system.

$$A = A_1 d + A_2(1-d)$$

$$B = B_1 d + B_2(1-d)$$

Figure 30 - State Space Averaged Matrix Definitions.

The result demonstrates that the continuous state and source matrices are functions of the matrices associated with each switch condition weighted by the time the respective switch condition is valid. One can now easily expand this to include more than two switch conditions as presented below in figure 31.

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(A)
$$\vec{A} := \vec{A}_1 \cdot d_1 + \vec{A}_2 \cdot d_2 + \vec{A}_3 \cdot \left[1 - d_1 - d_2\right] \qquad \text{Three switch conditions}$$

(B)
$$\vec{B} := \vec{B}_1 \cdot d_1 + \vec{B}_2 \cdot d_2 + \vec{B}_3 \cdot \left[1 - d_1 - d_2\right]$$

(C)
$$\vec{A} := \vec{A}_1 \cdot d_1 + \vec{A}_2 \cdot d_2 + \ldots + \vec{A}_{n-1} \cdot d_{n-1} + \vec{A}_n \cdot \left[1 - \sum_j d_j\right] \qquad \begin{array}{l} j = 1 \text{ to } n-1 \\ n \text{ switch} \\ \text{conditions} \end{array}$$

(D)
$$\vec{B} := \vec{B}_1 \cdot d_1 + \vec{B}_2 \cdot d_2 + \ldots + \vec{B}_{n-1} \cdot d_{n-1} + \vec{B}_n \cdot \left[1 - \sum_j d_j\right]$$

Figure 31 - State Space Averaged Matrix Definitions
Extended to 3 and n Switch Conditions.

Up until now we have considered X(t), U(t), and d(t) to be continuous but not necessarily linear. In order to use analysis techniques such as Laplace transforms the signal must be linearized around a point of interest much in the same way small signal parameters for a bipolar transistor are a linearization of a nonlinear device around a point of interest designated as the bias point. For the case of a switching regulator, the bias point also includes the duty cycle of the converter which must first be calculated from large signal models.

Small signal representation of X, U, and D

Signal = Bias Point + Small signal

(A)

$$\vec{X} := \begin{bmatrix} \vec{X}_0 + \vec{x} \\ 0 \end{bmatrix} \qquad \vec{U} := \begin{bmatrix} \vec{U}_0 + \vec{u} \\ 0 \end{bmatrix} \qquad D := \begin{bmatrix} D_0 + d \\ 0 \end{bmatrix}$$

State space averaged general state equations

(B)

$$\frac{d}{dt}\vec{X} := \vec{A}\,\vec{X} + \vec{B}\,\vec{U} \qquad \vec{A} := \vec{A}_1 D + \vec{A}_2 (1 - D) \qquad \vec{B} := \vec{B}_1 D + \vec{B}_2 (1 - D)$$

(C)

$$\frac{d}{dt}\begin{bmatrix} \vec{X}_0 + \vec{x} \\ 0 \end{bmatrix} := \begin{bmatrix} \vec{A}_1 \begin{bmatrix} D_0 + d \\ 0 \end{bmatrix} + \vec{A}_2 \begin{bmatrix} 1 - D_0 - d \\ 0 \end{bmatrix} \end{bmatrix} \begin{bmatrix} \vec{X}_0 + \vec{x} \\ 0 \end{bmatrix}$$

Insert the small signal variables ... into the general state equation

$$+ \begin{bmatrix} \vec{B}_1 \begin{bmatrix} D_0 + d \\ 0 \end{bmatrix} + \vec{B}_2 \begin{bmatrix} 1 - D_0 - d \\ 0 \end{bmatrix} \end{bmatrix} \begin{bmatrix} \vec{U}_0 + \vec{u} \\ 0 \end{bmatrix}$$

Figure 32 - Application of Small Signal Approximation to
the Nonlinear System.

To linearize the system consider the general form of the
state equations and redefine the state variables and
source variables as the sum of a small signal part and a
bias point as defined in figure 32A.

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(A) Small signal representation of X, U, and D.

Remove secondorder small signal product terms.

$$\frac{d}{dt}\left[\vec{X}_0 + \vec{x}\right] := \left[\vec{A}_1\left[D_0 + d\right] + \vec{A}_2\left[1 - D_0 - d\right]\right]\vec{X}_0 \ldots$$

$$+ \left[\vec{B}_1\left[D_0 + d\right] + \vec{B}_2\left[1 - D_0 - d\right]\right]\vec{U}_0 \ldots$$

$$+ \left[\vec{A}_1 D_0 + \vec{A}_2\left[1 - D_0\right]\right]\vec{x} + \left[\vec{B}_1 D_0 + \vec{B}_2\left[1 - D_0\right]\right]\vec{u}$$

(B) Recombine bias and small signal terms so as to recreate the general state space averaged equation plus an aditional term.

$$\frac{d}{dt}\left[X_0 + x\right] := \left[\vec{A}_1 D_0 + \vec{A}_2\left[1 - D_0\right]\right]\left[X_0 + x\right] \ldots$$

$$+ \left[\vec{B}_1 D_0 + \vec{B}_2\left[1 - D_0\right]\right]\left[U_0 + u\right] \ldots$$

$$+ \left[\left[\vec{A}_1 + \vec{A}_2\right]X_0 + \left[\vec{B}_1 + \vec{B}_2\right]U_0\right]d$$

(C) Redefine the state equation using the old definitions for A, but add the term E to represent the duty cycle port.

$$\frac{d}{dt}\left[X_0 + x\right] := \vec{A}_0\left[X_0 + x\right] + \vec{B}_0\left[U_0 + u\right] + \vec{E} d$$

Where $\vec{A}_0 := \left[\vec{A}_1 D_0 + \vec{A}_2\left[1 - D_0\right]\right]$ and $\vec{B}_0 := \left[\vec{B}_1 D_0 + \vec{B}_2\left[1 - D_0\right]\right]$

Figure 33 - Small Signal State Equations.

Substituting this into the general state equation yields a general form of the system in figure 33C. Note that products of small signal terms are ignored since it is assumed that the small signal part of each component is small compared to the bias point. By rearranging the equation to force it to look like the general state space

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averaging equation for a nonlinear circuit it becomes
easier to understand the significance of each term
(Figure 33B). It can be seen that the small signal part
of X and U both under go the same transformation as in the
case of the non-linear system, but added to the response
is a term which is dependent upon the small signal
variation of the duty cycle signal D(t) (Figure 33B). A
new general state equation appears which has three
components, though two are identical to the non-linear
case. The new component is defined as matrix E, and
represents the systems response to small signal changes in
duty cycle (Figure 33C).

Now that a linearized representation exists, Laplace
transforms can be used to rearrange and solve for state
variables X as a function of input and duty cycle as
described below in figure 34.

$$
\text{(A)} \quad \frac{d}{dt} X := A \cdot \vec{X} + B \cdot \vec{U} + E \cdot \vec{d}
$$

$$
\text{(B)} \quad s \cdot I \cdot \vec{X(s)} := A \cdot \vec{X(s)} + B \cdot \vec{U(s)} + E \cdot \vec{d(s)} \qquad \text{Convert to S plane}
$$

$$
\text{(C)} \quad \vec{X(s)} := \left[s \cdot I - A \right]^{-1} \cdot B \cdot \vec{U(s)} + \left[S \cdot I - A \right]^{-1} \cdot E \cdot \vec{d(s)}
$$

Figure 34 - Small Signal State Equation Definitions.

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STATE SPACE LINEARIZED REGULATOR

V(S)
IN

X(S)
$\overline{A}$ $\overline{B}$ $\overline{E}$

D(S)

Q(S)

F(S)

Σ

FEED-FORWARD

FEED-BACK

V(S) = X(S)
OUT   1
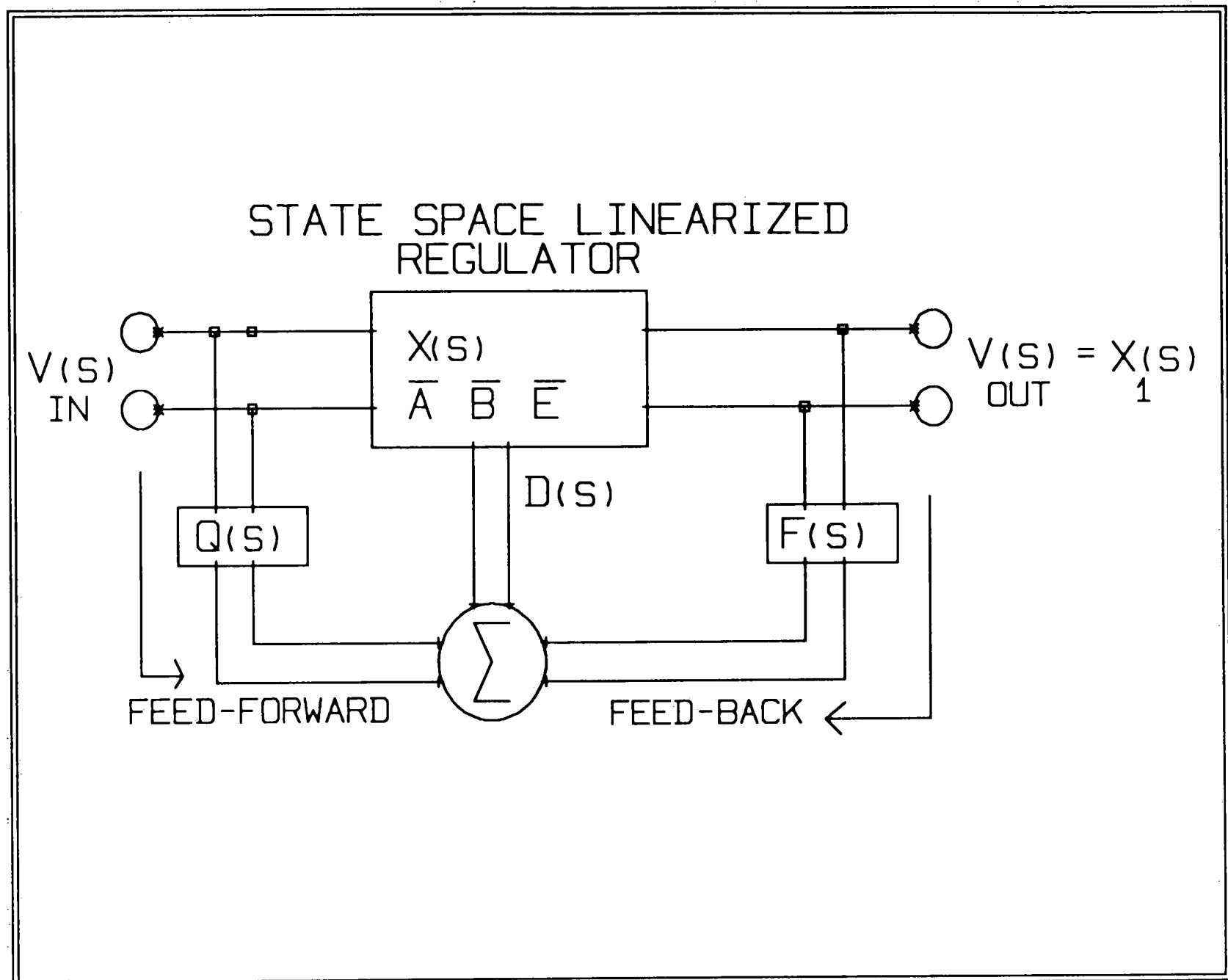
Figure 35 - Flow Diagram Depicting Feedback and
Feedforward Control.

With the switching portion of the regulator

described, the regulator control loop needs to be added to

the mathematical representation to complete the system.

If the duty cycle control signal D(s) is formed form a

general feedback model as shown in figure 35; D(s) is a

function of the input vector and the state vector of the

system. For a simple system where V_{out} is the capacitor

state and V_{in} is the only component of the input vector

then the control path from $V_{in}(s)$ to D(s) is feed-forward

control, and the path from $V_{out}(s)$ to D(s) is feedback

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control.   By defining a gain matrix Q and F in each path a

general feedback/forward model can be obtained

(Figure 36).   This model describes the basic small signal

function of the switching regulator.

```
┌─────────────────────────────────────────────────────────────────┐
│                                                                   │
│      Duty cycle = Network state + Input                           │
│                 =    Feed back  + Feed forward                    │
│  (A)                                                              │
│                   ⎯⎯→ ⎯⎯→   ⎯⎯→ ⎯⎯→                               │
│        d(S) := F(S)·X(S) + Q(S)·U(S)        Duty cycle control signal │
│                                                                   │
│                        Where  ....                                │
│                                              ┌ ┐            ┌ ┐   │
│          F(S) := (    )   Q(S) := (    )  U(S) := │ │   X(S) := │ │ │
│                                              └ ┘            └ ┘   │
│                                                                   │
├─────────────────────────────────────────────────────────────────┤
│  (B)                                        -1                    │
│                    ┌          ⎯→  ⎯→ ⎯⎯→ ⎤     ┌⎯→  ⎯→ ⎯⎯→ ⎤ ⎯⎯→  │
│        X(S) := │s·I - A - E·F(S) │    ·│B + E·Q(S)│·U(S)  │
│                    └                    ⎦     └          ⎦        │
│                                                                   │
│                  Solve for the state variables                    │
│                                                                   │
└─────────────────────────────────────────────────────────────────┘
```

$$d(S) := \overrightarrow{F(S)} \cdot \overrightarrow{X(S)} + \overrightarrow{Q(S)} \cdot \overrightarrow{U(S)}$$

$$X(S) := \left[s \cdot I - \overrightarrow{A} - \overrightarrow{E} \cdot \overrightarrow{F(S)} \right]^{-1} \cdot \left[\overrightarrow{B} + \overrightarrow{E} \cdot \overrightarrow{Q(S)} \right] \cdot \overrightarrow{U(S)}$$

Figure 36 - General State Space Averaged and Linearized
System Representation.

Extending State Space Averaging into a Computer Model

Although state space averaging yields a small signal

solution, it does so at the expense of simplicity.   We can

however use the success of state space averaging to

introduce a less cumbersome analysis method.

State space averaging removes the switch from the

circuit by redefining the inductor currents and capacitor

voltages as weighted averages dependent on duty cycle.   At

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the circuit level removal of the switch could be
translated into removing the switch and replacing it with
dependent current or voltage sources to mimic the average
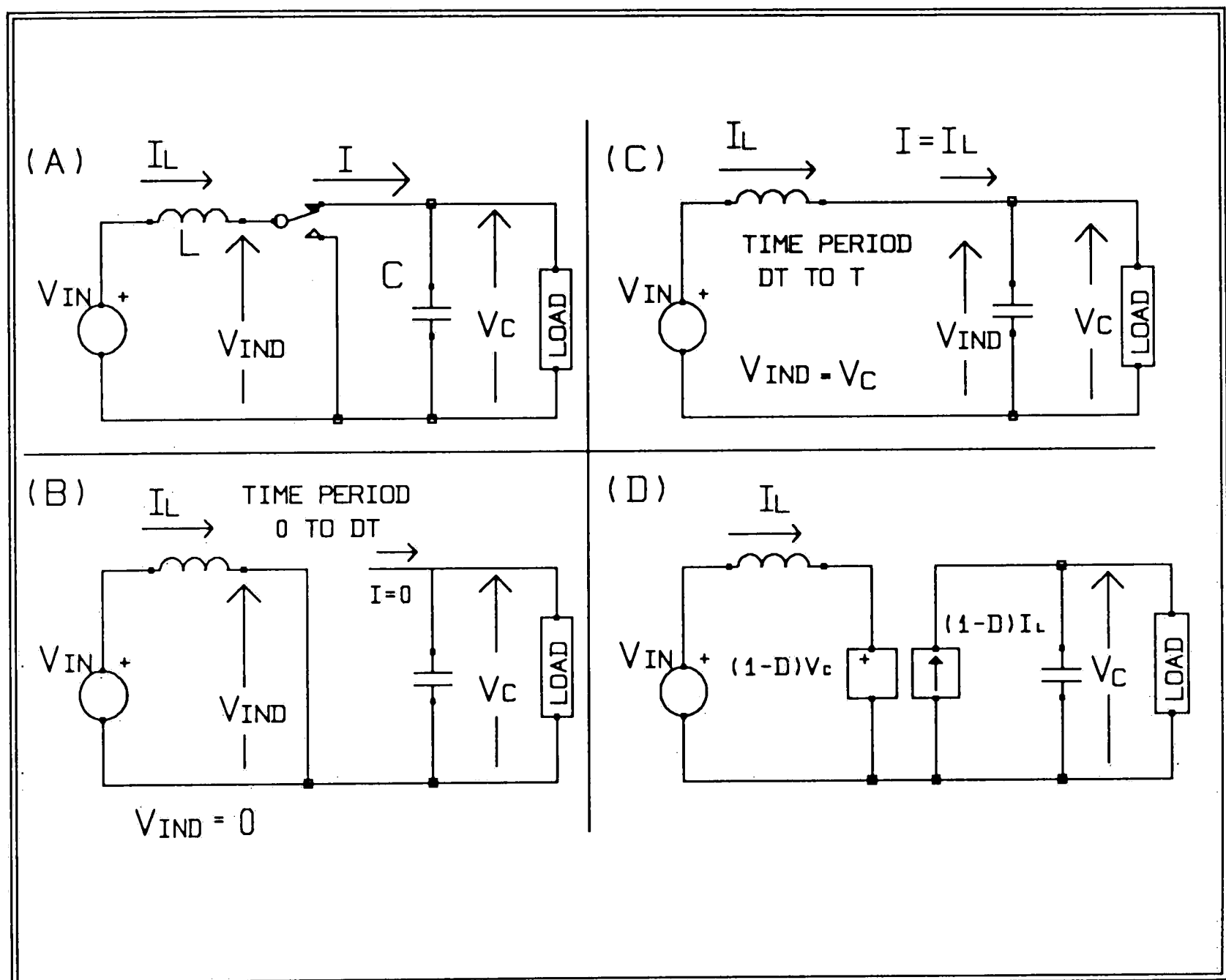in circuit terminal conditions of the switch.

Figure 37 - Switch Replacement Model for a Boost
Converter.

Continuous Mode Boost Converter Model

Consider the operation of the continuous mode boost
converter shown in figure 37A. When the switch is
activated over the duty cycle time 0 to DT, the inductor
node voltage V_{IND} is zero and the current I, into the

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output capacitor, is zero as shown in figure 37B. During the switch rest interval DT to T, the inductor node potential is equivalent to the voltage across the output capacitor V_C, and the switch current is equivalent to the inductor current I_L (Figure 37C). From this analogy the time averaged inductor node voltage is:

$$V_{IND} = [\ V_{OUT} \cdot (1-D)\ ]$$

and the time averaged switch to output node current is:

$$I = [\ I_L \cdot (1-D)\ ].$$

These average switch terminal conditions can be preserved in absence of the switch by inserting a voltage controlled voltage source in series with the inductor which is dependent on the output voltage, and a current controlled current source in parallel with the output capacitor which is dependent on the average inductor current (See figure 37D).

The model presented in figure 37D is non linear; consequently conventional circuit analysis techniques can not be used without linearizing the non linear dependent sources. Fortunately the circuit shown in figure 37D can be simulated using the nonlinear dependent source feature of Spice or in this case Pspice1. (All further references to Spice will refer to the Pspice version 3.08

---

1 Pspice is a registered trademark of Microsim Corporation.

implementation of Spice). A spice model of the equivalent circuit in figure 37A is shown in figure 38 where the duty cycle D is modeled as V_D and the ESR of the capacitor and inductor are also included in the model.

SWITCH MODEL

$$F1 = I(V_{IL}) * I(V_{ONE})$$

$$E1 = V(5,0) * V(10,9)$$

$$V(10,9) = (1 - V_D)$$

DUTY CYCLE
PORT

```
*
.PROBE
.AC   oct   5      1HZ     40E3HZ
.DC   LIN VD 0 .9 .01
* Input Source
Vin  1 0 5
*   Inductor model
RLS  1 2 .0001
L1   2 3 220U
VIL  3 4 0
*
*   Voltage at switch node
*               Vcap  (1-D)
E1   4 0 POLY(2) (5 0) (10 9) 0 0 0 0 1
*                 IL (1-D)
F1   0 5 POLY(2) VIL Vone 0 0 0 0 1
*
C1   5 6 100U
Resr 6 0 .2
RLoad      5 0 15
*
*   Duty Cycle Port Model D = Vd
VD   9 0 .667 AC .001
R2   9 10 1
Vone 0 10 -1
.END
```
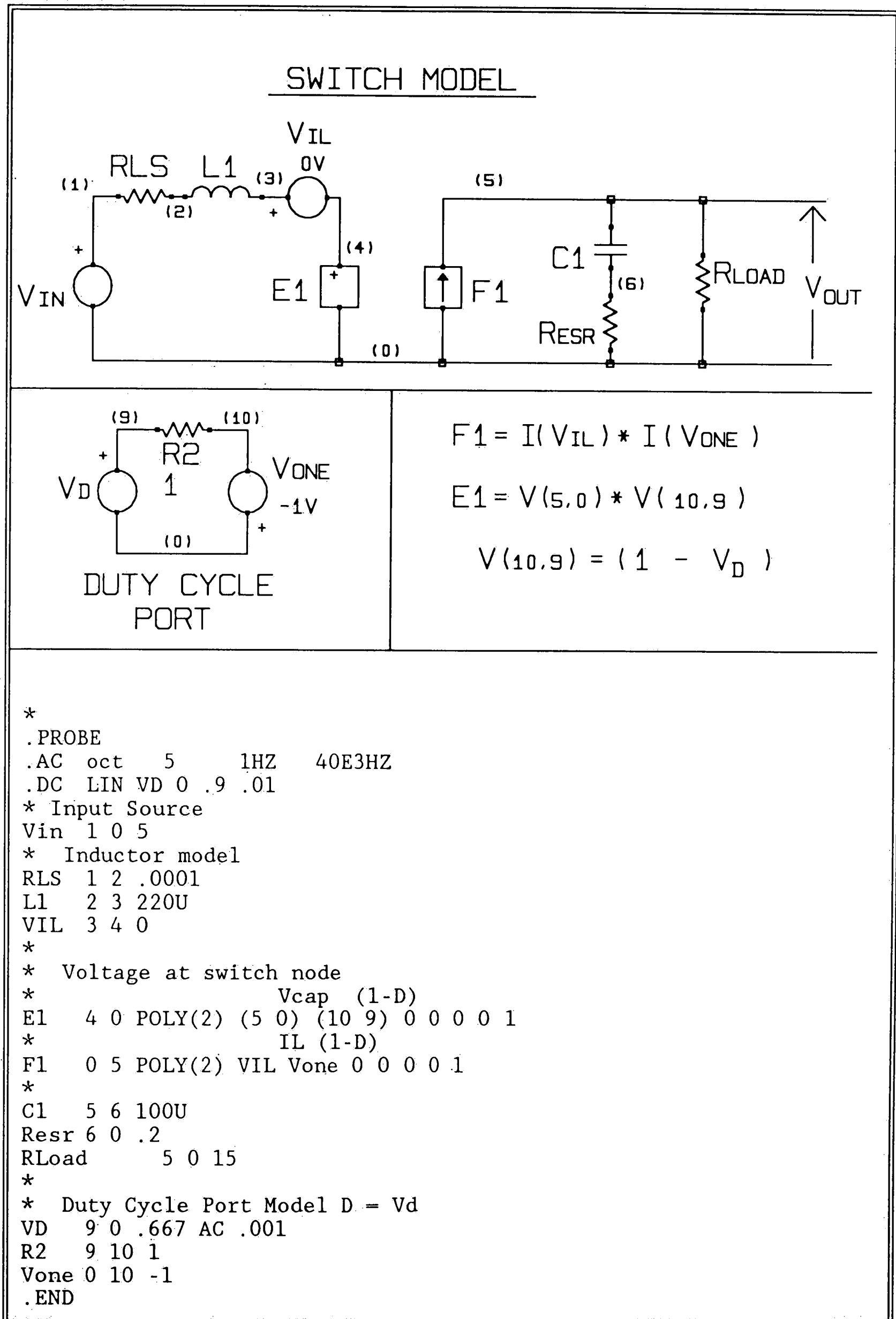
Figure 38 - Spice Model of a Continuous Mode Duty Cycle
Controlled Boost Regulator.

A demonstration of the continuous mode model is shown
in figure 39 where a DC sweep was used to obtain the DC
output voltage, input current, and load current as a
function of duty cycle. The small signal gain and phase
of the regulator from the duty cycle port to the output is
shown in figure 40 was obtained by a AC analysis with the
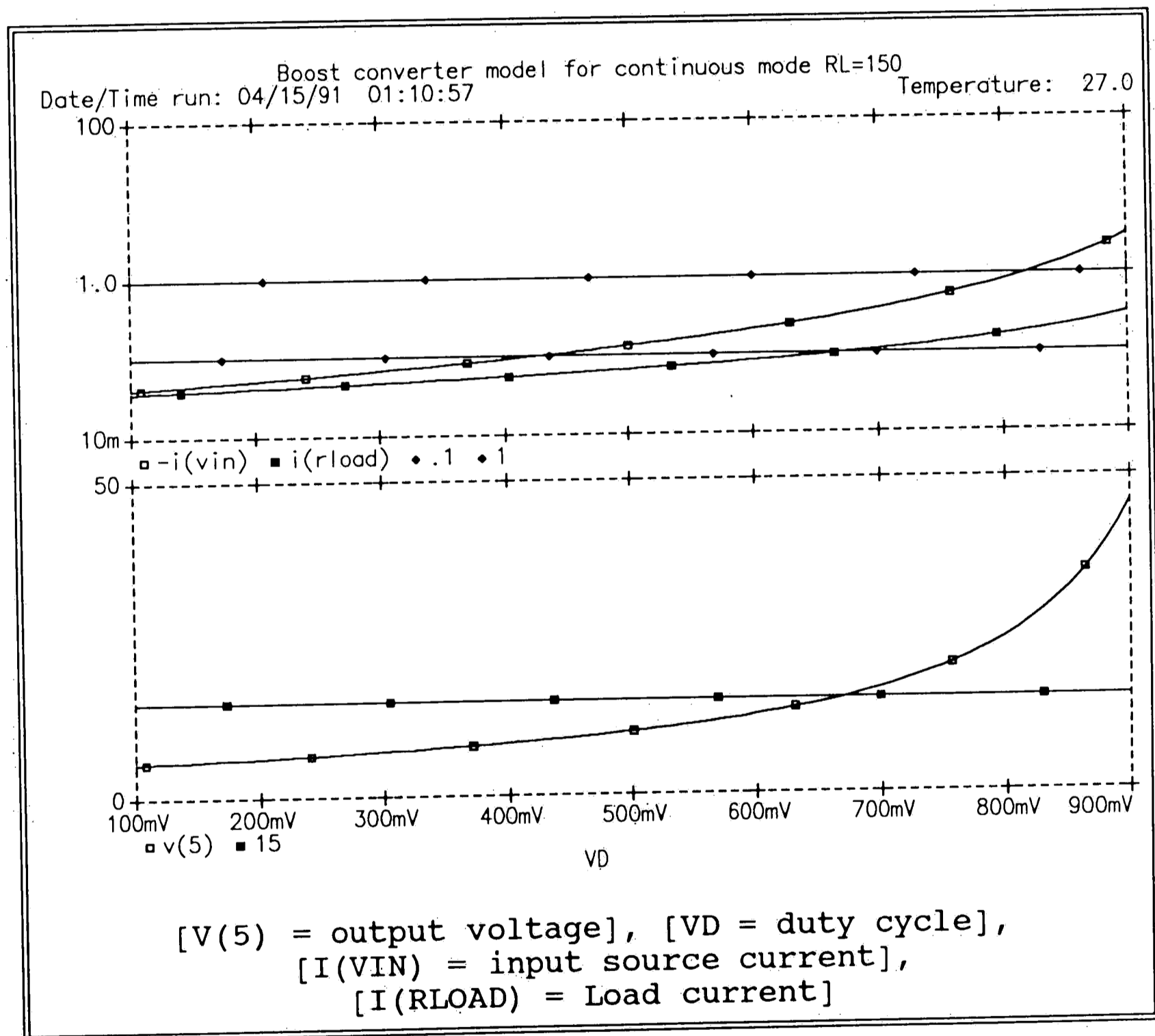duty cycle generator set to 0.66 VDC (66%).

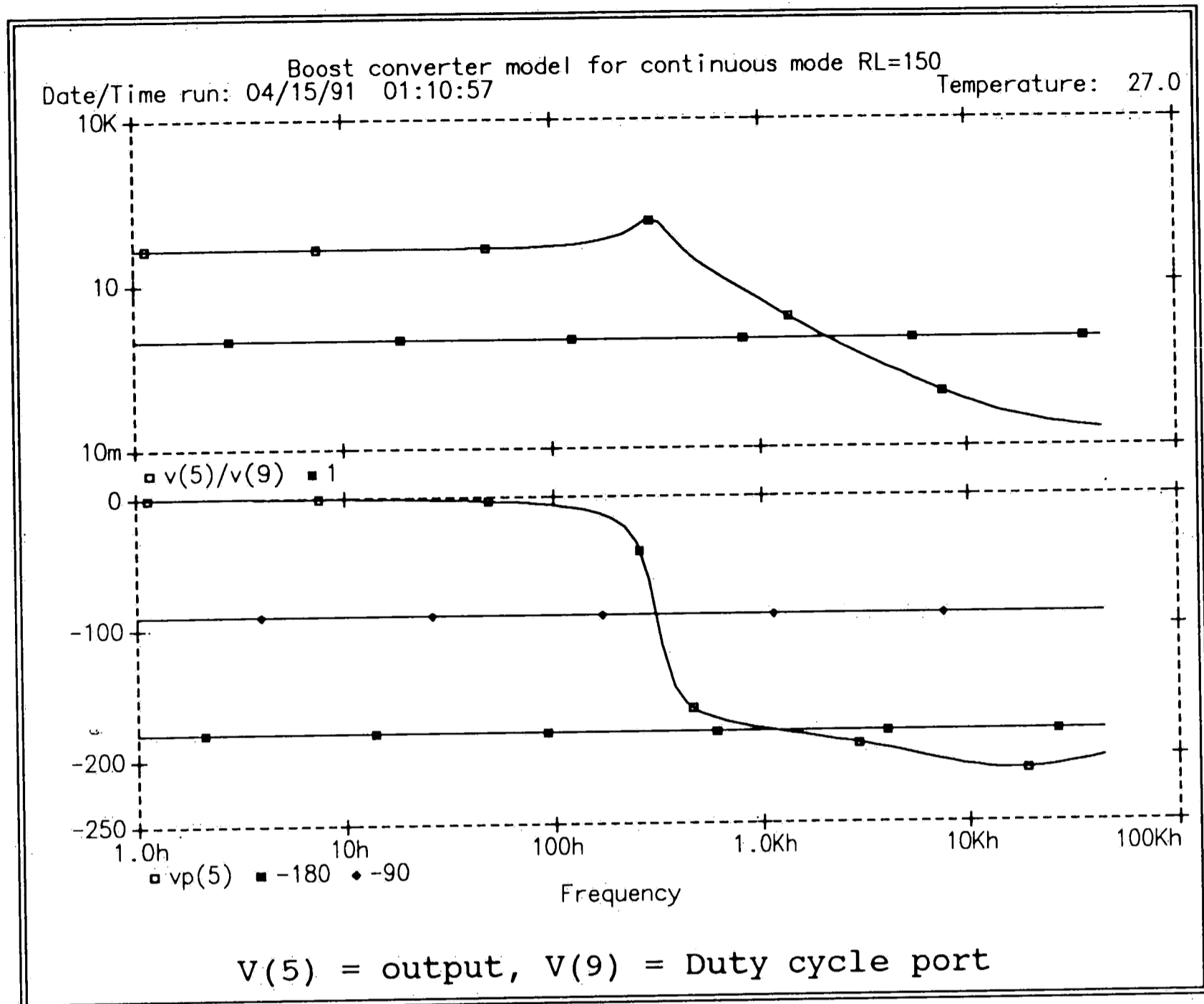Figure 39 - Boost Converter Simulation.

Figure 40 - Pspice Boost Converter Gain and Phase Plot.

Discontinuous Mode Boost Model

Unfortunately, the previously described model is only valid for continuous operation, nevertheless one can derive a similar model for discontinuous operation by writing equations to describe the switch terminal conditions for discontinuous operation (See figure 41A-41C).
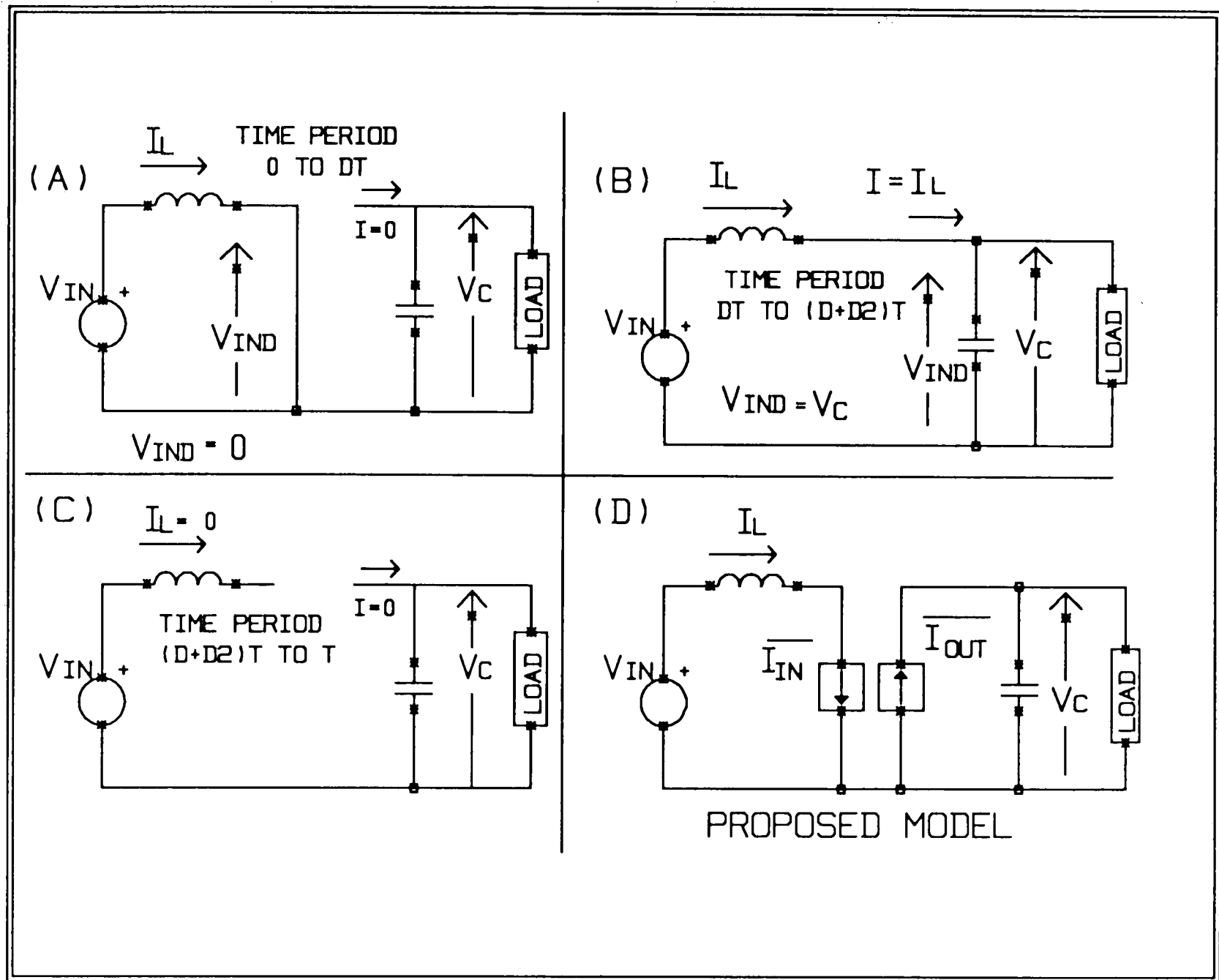
Figure 41 - Discontinuous Mode Switch Terminal Conditions.

Discontinuous operation adds a third equivalent circuit shown in figure 41C to the system describing the system when the inductor current is zero. The additional condition leaves no current flowing in either switch implying that the condition, and consequently the average circuit, must be modeled using a norton equivalent for the inductor side of the switch as shown in figure 41D.

$$\text{(A)} \quad I_{L(t)} := \left[Vin \; \frac{1}{L} \; t \right] \qquad \text{For } 0 < t < DT \qquad \text{Inductor charges from zero}$$

$$\text{(B)} \quad I_{L(t)} := \left[Vin \; \frac{1}{L} \; D\,T \right] - (Vout - Vin) \; \frac{1}{L} \; (t - DT) \qquad \text{Inductor discharges} \qquad \text{For} \quad \left[D\,T < t < \left[D\,T + D_2 \; \frac{T}{2} \right] \right]$$

$$\text{(C)} \quad I_{L(t)} := 0 \qquad \text{For} \quad \left[D\,T + D_2 \; \frac{T}{2} \right] < t < T \qquad \begin{array}{l} \text{Discontinuous} \\ \text{current zone.} \end{array}$$

$$\text{(D)} \quad Iout := \frac{1}{T} \int_{DT}^{T} \left[I_{L(t)} \right] dt \qquad Iout := Vin \; D_2 \left[\frac{D\,T}{2\,L} \right] \qquad \begin{array}{l} \text{Inductor output} \\ \text{current.} \end{array}$$

$$\text{(E)} \quad D_2 := \frac{Vin \; D \; T}{L} \left[\frac{L}{(Vout - Vin)\,T} \right] \qquad D_2 \text{ is the point where } IL \text{ is zero.}$$

$$\text{(F)} \quad I_{Lavg} := \frac{1}{T} \int_{0}^{T} \left[I_{L(t)} \right] dt \qquad i_{Lavg} := \left[\frac{D + D_2}{2} \right] I_{Lmax}$$

$$\text{(G)} \quad I_{Lavg} := \left[\frac{Vin \; D^2 \; T}{2\,L} + \frac{Vin^2 \; D^2 \; T}{2\,L\,(Vout - Vin)} \right] \qquad Iout := \left[\frac{Vin^2 \; D^2 \; T}{(Vout - Vin)\,2\,L} \right]$$

Figure 42 - Discontinuous Mode Average Terminal
Conditions.

To derive the dependency of each source in the model, we have to define an average inductor current I_{Lavg} for the purpose of modeling the input side of the switch, and an average output current I_{out} to model the output side of the switch. Before this can be accomplished, an expression for the inductor current $I_L(t)$ must be derived for the inductor charging interval { 0 to DT }, the inductor discharging interval { DT to $(D+D_2)T$ }, and the discontinuous interval { $(D+D_2)T$ to T } (Figures 42A-42C). I_{Lavg} is found by integrating $I_L(t)$ from 0 to T, and I_{out}

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is found by integrating $I_L(t)$ from DT to T (Figures 42D-42G). With the source dependencies known, the model is completed by inserting them into there respective places as shown in figure 43.
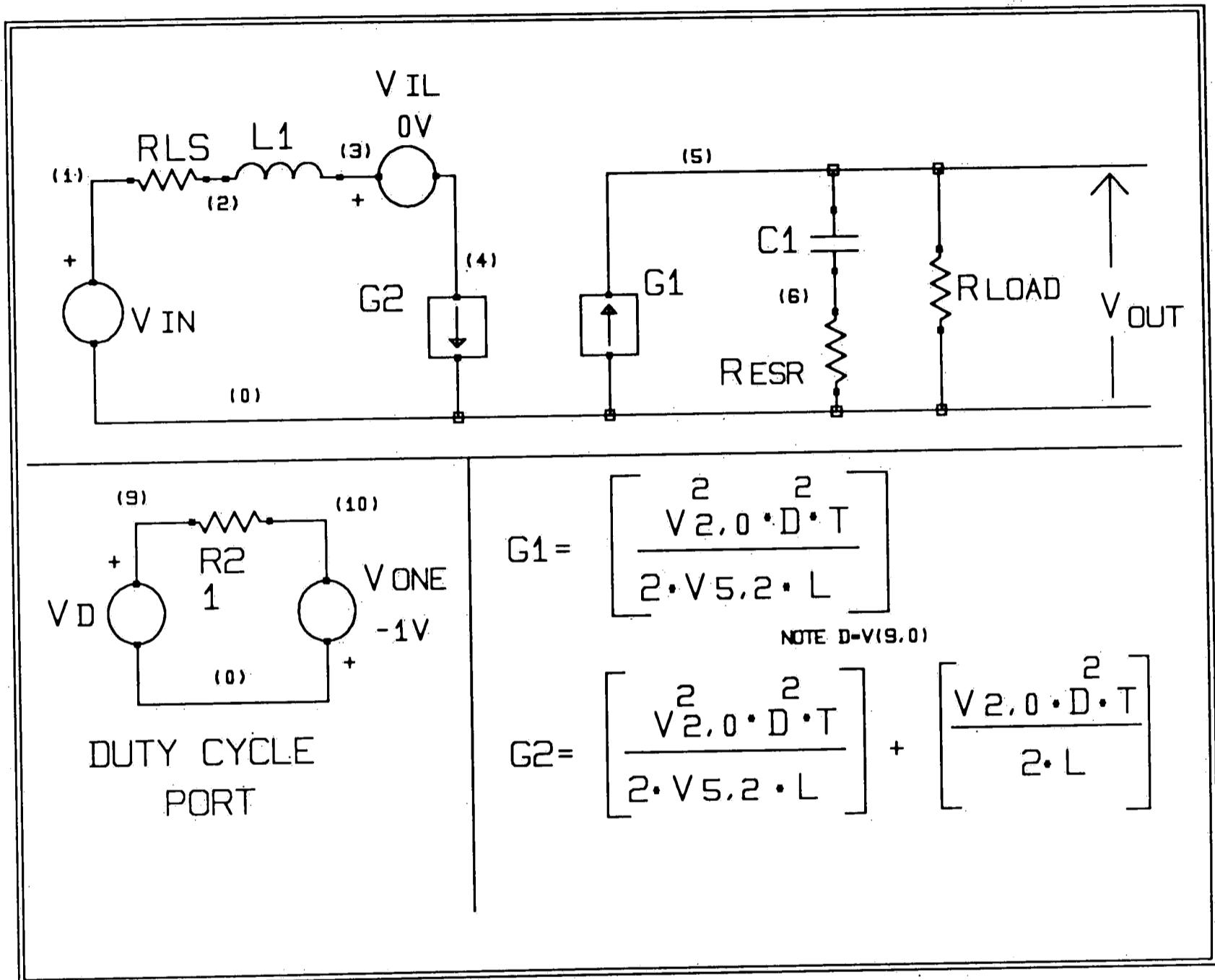

$$G1 = \left[\frac{V2,0^2 \cdot D^2 \cdot T}{2 \cdot V5,2 \cdot L} \right]$$

NOTE: D=V(9,0)

$$G2 = \left[\frac{V2,0^2 \cdot D^2 \cdot T}{2 \cdot V5,2 \cdot L} \right] + \left[\frac{V2,0 \cdot D^2 \cdot T}{2 \cdot L} \right]$$

Figure 43 - Discontinuous Mode Model.

(A) $\quad I_{L(t)} := \left[I_0 + Vin \frac{1}{L} t \right] \quad$ For $0<t<DT$

(B) $\quad I_{L(t)} := \left[I_0 + Vin \frac{1}{L} D T \right] - (Vout - Vin) \frac{1}{L} (t - DT) \quad$ For $(DT < t < T)$

(C) $\quad Iout := \frac{1}{T} \int_{DT}^{T} \left[I_{L.1(t)} \right] dt \qquad Iout := (1 - D) I_0 + (Vin\, D\, T) \frac{1 - D}{2 \cdot L}$

(D) $\quad I_0 := \frac{Iout}{1 - D} - \frac{Vin\, D\, T}{2\, L} \qquad I_0 := I_{Lmin}$ Where Iout is the average current leaving the inductor and I0 is the minimum inductor current.

(E) $\quad I_{Lavg} := \frac{1}{T} \int_{0}^{T} \left[I_{L(t)} \right] dt \qquad I_{Lavg} := \left[\frac{Iout}{1 - D} \right]$ Average Inductor current.

(F) Peak Inductor current
$\quad I_{Lmax} := I_{L(DT)} \qquad I_{Lmax} := \left[I_0 + Vin \frac{1}{L} DT \right]$

(G) $\quad \left[I_{Lmax} - Vin\, D\, \frac{T}{L} \right] := \left[I_{Lavg} - \frac{Vin\, D\, T}{2\, L} \right]$ Where $I_{Lmax} := \frac{Vc}{Rs}$

(H) $\quad D := \frac{2\, L}{Vin\, T} \left[\frac{Vc}{Rs} - I_{Lavg} \right]$ Current mode Duty cycle control function for continuous conduction

Figure 44 - Duty Cycle to Current Mode Control.

All the models discussed up to this point have all been duty cycle controlled, but current mode control can easily be added by noting that current mode control is simply a method of varying duty cycle to achieve a desired peak inductor current. If one defines current mode control as an input to the system Vc/Rs which sets the peak inductor current to Imax by varying the duty cycle then one can derive a function D(Imax) to describe current mode control. To accomplish this, the previously derived

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inductor current equations for the boost converter need to be modified to include I_{max}. I_{max} is simply the inductor current function $I_L(t)$ evaluated at the switch turn off point DT (Figure 44F). The average inductor output current I_{out}, the average inductor current I_{Lavg}, and I_{max} are combined to yield the function in figure 44H which is duty cycle as a function of V_{in}, I_{max}, and I_{Lavg}. Implementation of this function in the form of a model is shown in figure 45 where the duty cycle generator V_D from the duty cycle model in figure 38 has been replaced by a dependent source E_D whose voltage is dependent on the equation is figure 44H. A similar argument could be used to add slope compensation to this model since slope compensation is merely changing the current set point as a function of duty cycle.
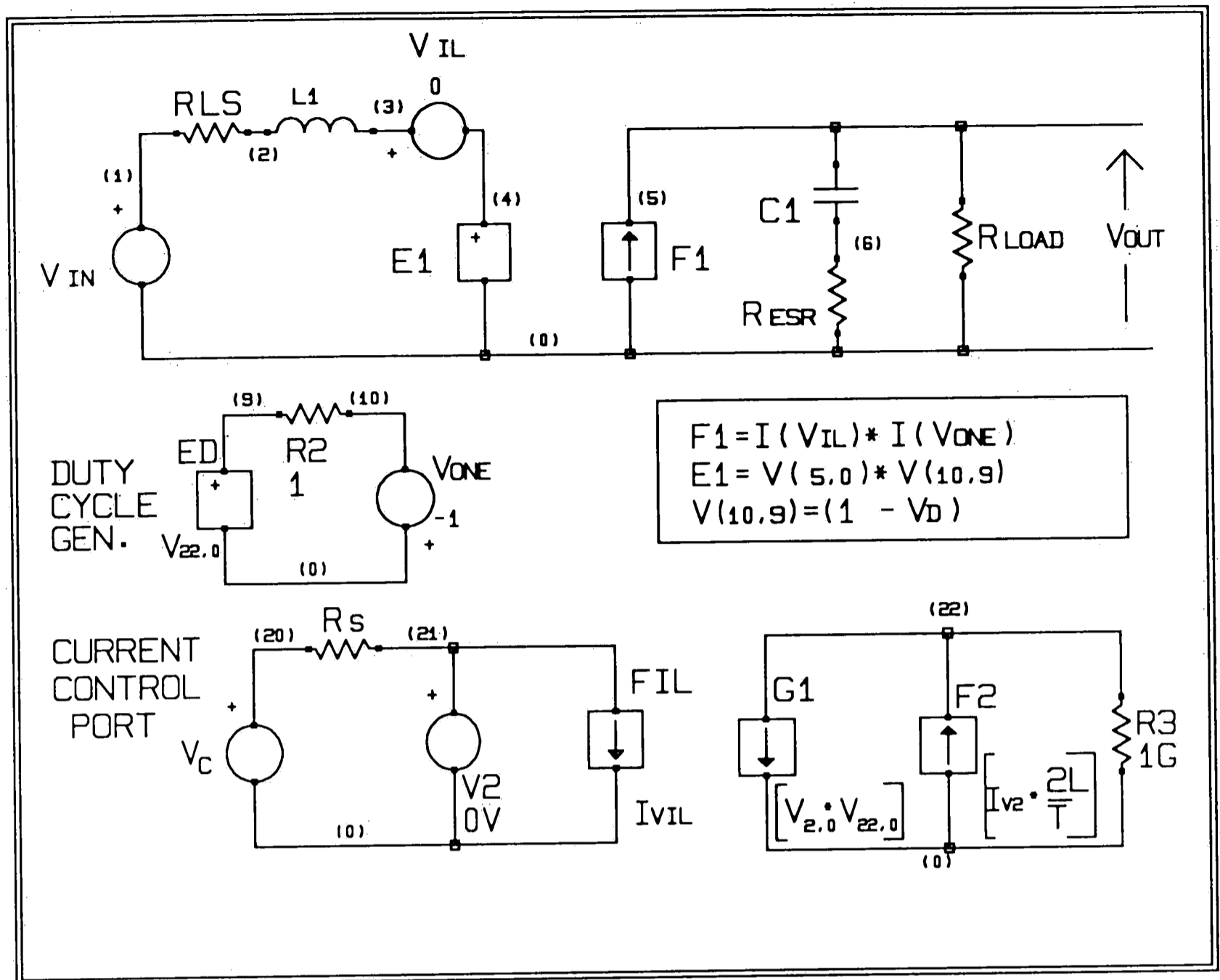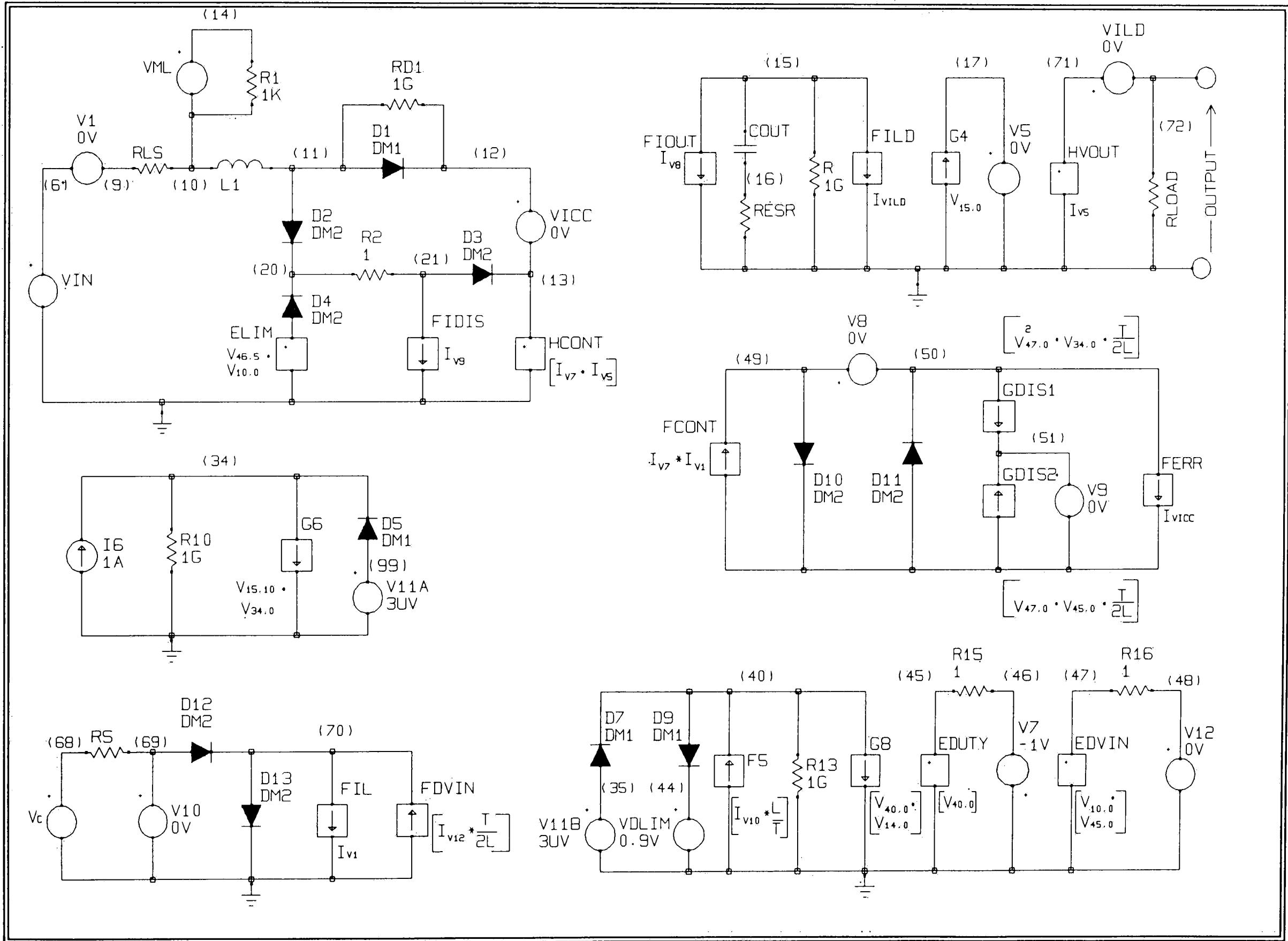
Figure 45 - Spice Model of a Continuous Current Mode
Controlled Boost Regulator.

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Figure 46 — Boost Converter Hybrid Model.

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Integrating Discontinuous and Continuous Mode Models

As previously discussed, the continuous model and the discontinuous model are separate; forcing the user to take note of the mode in which the converter is in before a simulation can be initiated. A model which implements both the discontinuous and continuous mode models by switching between the two model topologies is shown in figure 46.1 Mode switching is implemented in the model by using "ideal" diodes to change the model topology between the two equivalent circuits (An ideal diode is modeled by decreasing the emission coefficient to near zero in the spice diode model statement).

_____

1 Spice modeling for switching power converters with crossover between continuous and discontinuous conduction modes [15].

(A)

$$Voutd(Vin,D) := \frac{1}{2}\left[Vin + \sqrt{Vin^2 + 4\left[R\ T\ D^2\ \frac{Vin^2}{2\ L}\right]}\right]$$

Output voltage calculated for the discontinuous cas as a function of input voltage and duty cycle

(B)

$$Voutc(Vin,D) := \frac{Vin}{1 - D}$$

Output voltage calculated for the continuous case as a function of input voltage and duty cycle.

(C)

$$ILdis(D,Vin,Vout) := \left[D^2\ Vin^2\ \frac{T}{2\ L\ (Vout - Vin)}\right] + \left[D^2\ Vin\ \frac{T}{2\ L}\right]$$

Average inductor current in discontinuous mode

(D)

$$ILcont(D,Vin,Vout) := \left[\frac{Vout}{R\ (1 - D)}\right]$$

Average inductor current in continuous mode

(E)

$$Iodis(D,Vin,Vout) := \left[D^2\ Vin^2\ \frac{T}{2\ L\ (Vout - Vin)}\right]$$

Output current in discontinuous mode

(F)

$$Iocont(D,Iin) := Iin\ (1 - D)$$

Output current in continuous mode

$$Vin = 5 \qquad R = 2\ 10^2 \qquad L = 2.8\ 10^{-4} \qquad T = 2.5\ 10^{-5}$$
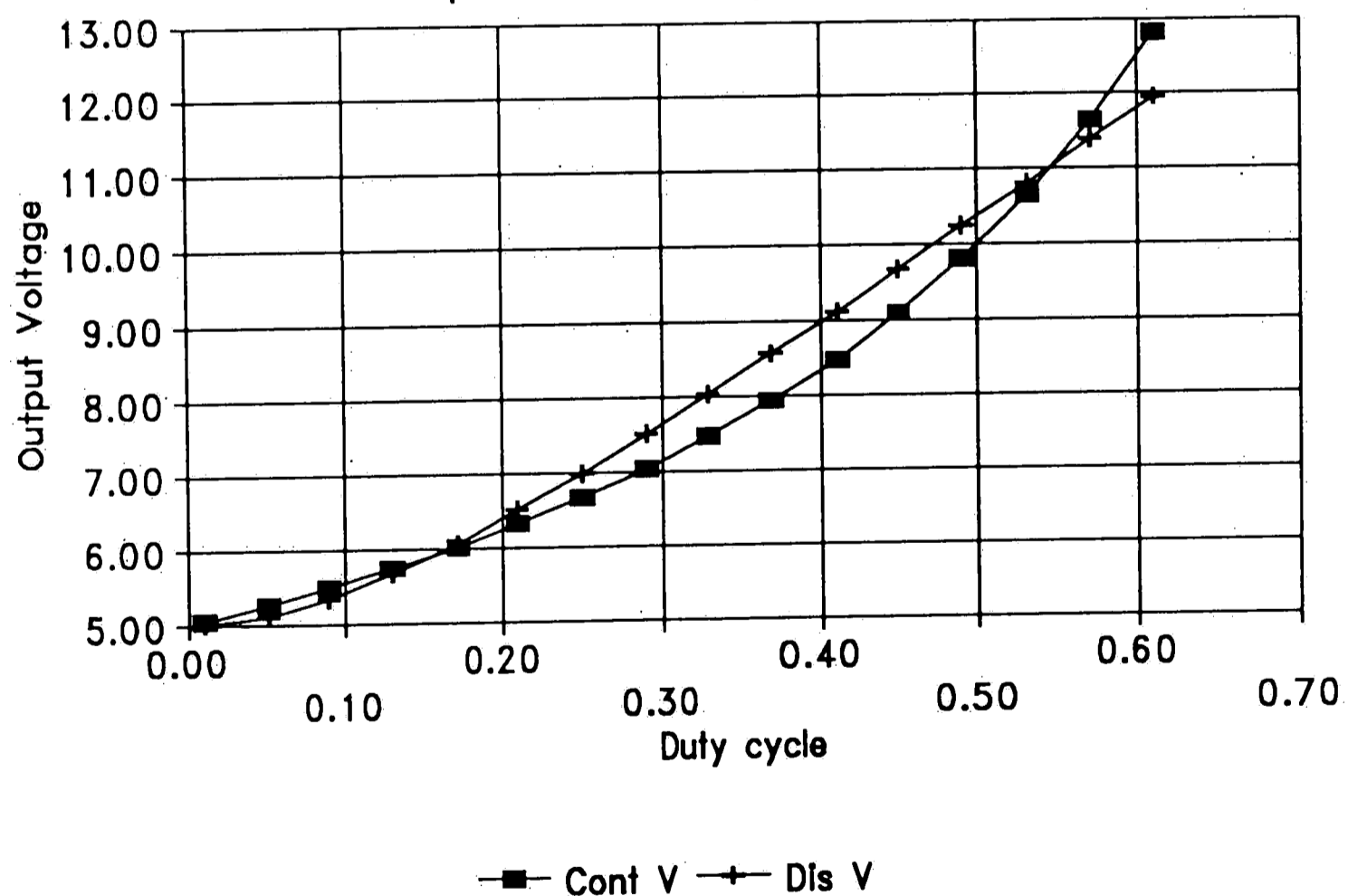
Figure 47 - Discontinuous vs Continuous Operation.

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Input current model
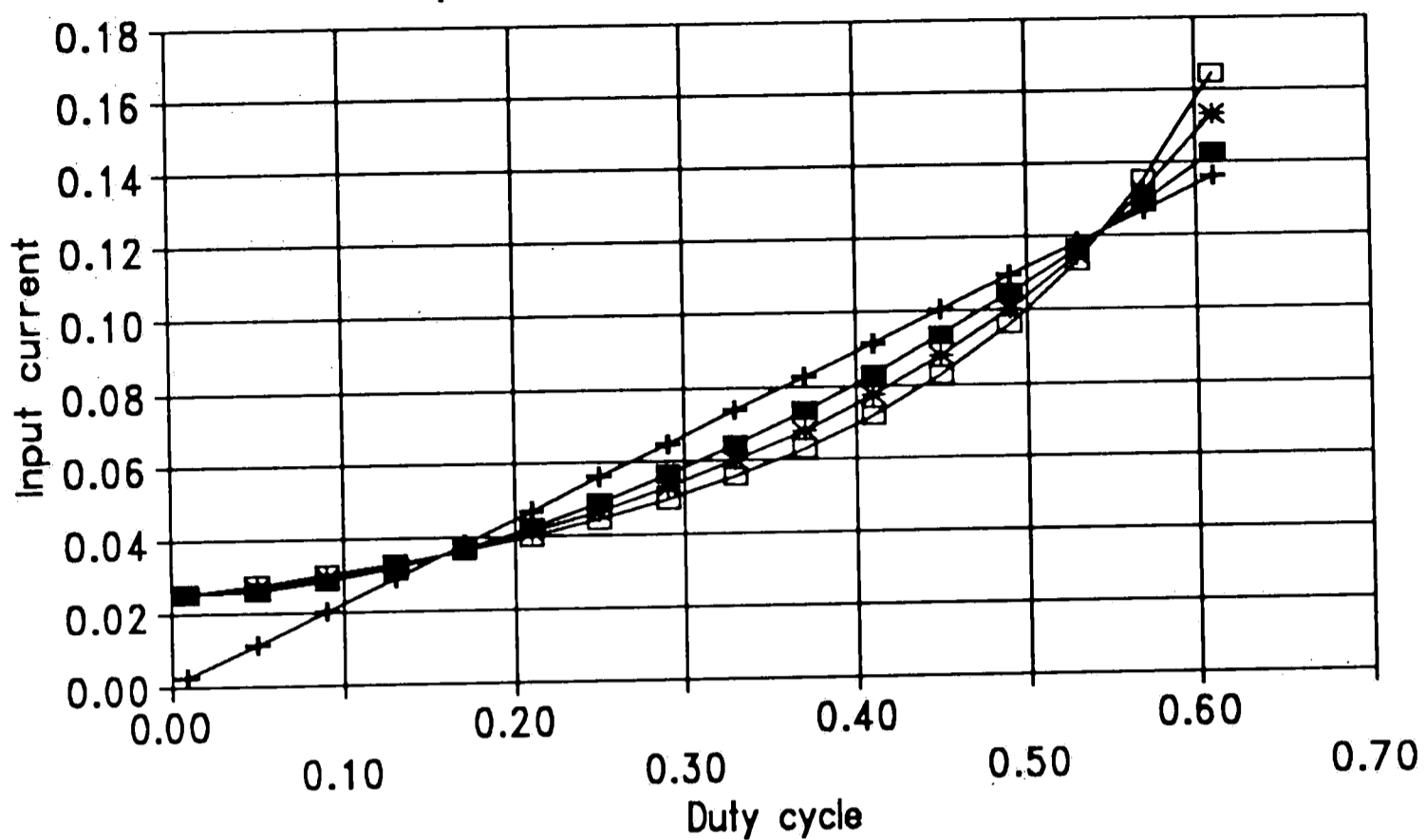
Output current model
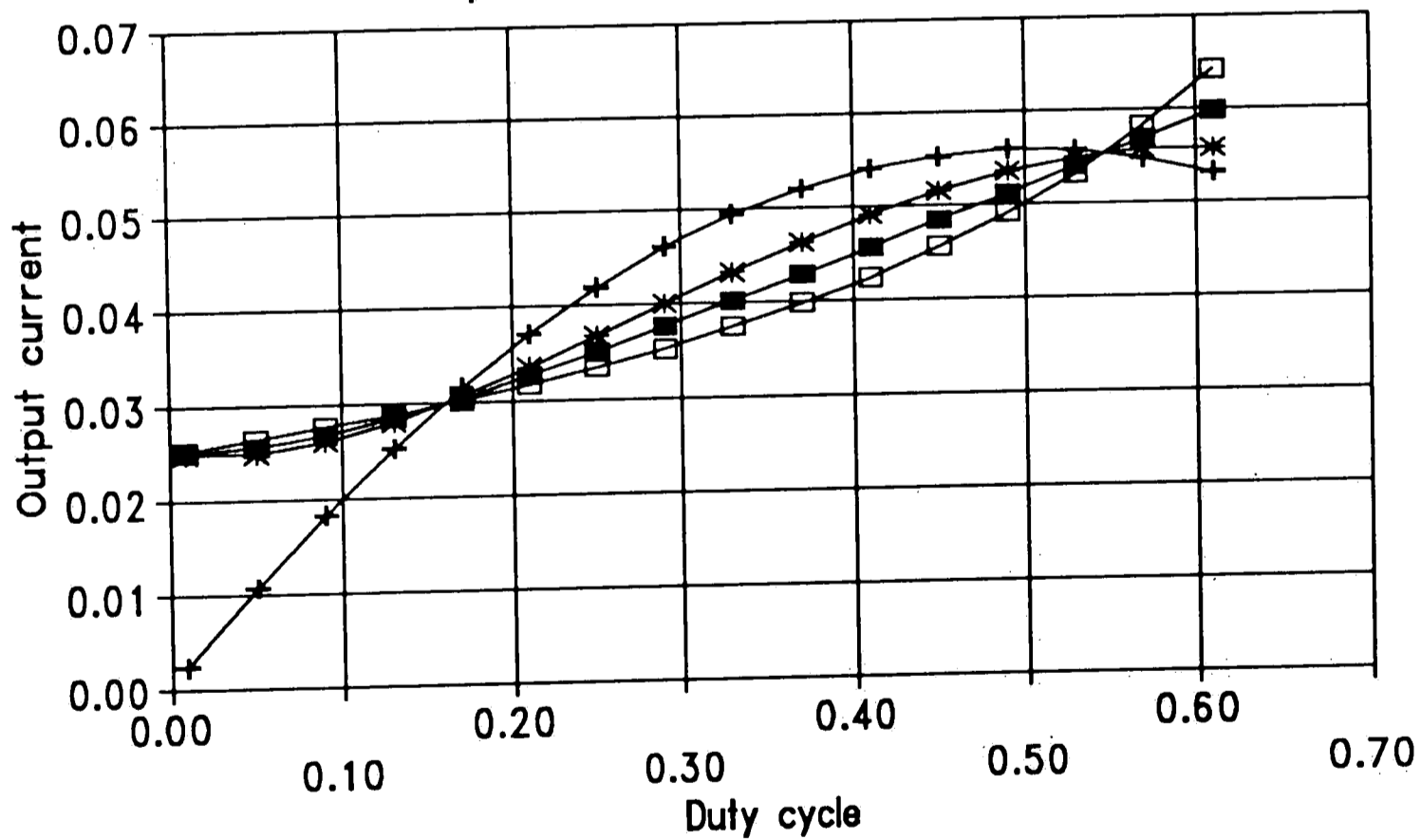
Figure 48 - Discontinuous vs Continuous Operation.

Equations describing the different switch terminal conditions which must be emulated by the model are defined in figure 47. From the previous models, it is evident that the inductor-switch node must see a current source with the dependency described by equation 47C when in discontinuous mode, and a voltage source with the dependency described by equation 47B when in continuous mode. The switch ouput is modeled by a current source in both cases but the source dependencies are different between modes (See figure 47E and 47F).

Switching between the two models is done by noting that the input current computed by the discontinuous mode model is less than that computed by the continuous mode model for continuous operation while the output voltage computed by the discontinuous mode formula is greater than that computed by the continuous mode formula when in discontinuous mode. Dependent source HCONT, and diode D1 generates the average inductor voltage according to the continuous mode model such that the dependent source can only sink current from the inductor at node 11. A current calculated from the discontinuous mode model is pulled from node 11 by dependent current source FIDIS. If the regulator is in continuous mode; the input current is more than the discontinuous model predicts via dependent source FIDIS so current flows into HCONT through D1 to make up

the difference (Essentially a voltage source in parallel
with a current source). If the regulator is in
discontinuous mode the output voltage of the regulator
rises above that of the continuous case which causes
dependent source HCONT to rise above V_{in} and turn off
diode D1 leaving the inductor current as that produced by
discontinuous model source FIDIS.

Output current is modeled in both modes by dependent
source FIOUT which monitors the current in independent
source V8. Source V8 and diodes D10 and D11 form a
circuit which steers the lesser of the two currents FCONT
or (GDIS1 + FERR) through source V8. Source GDIS1
produces the output current according to the discontinuous
model described by equation 47E while source FCONT1
produces a current according to the continuous model
equation 47F. When in discontinuous mode the current
predicted by GDIS1 is always less than that predicted by
FCONT so the model should pick the lesser of the two when
in discontinuous mode. However the opposite is true in
continuous mode. When in continuous mode the current
produced by GDIS1 is less than that produced by FCONT so
we need to pick the larger of the two in continuous mode.
Switching is accomplished by detecting which mode the
converter is in by monitoring the current in the
continuous mode input source HCONT. If there is no

current flow in HCONT, signifying discontinuous mode, then the circuit takes the lesser of the two currents generated by GDIS1 and FCONT. If there is current flow in HCONT, an error current is generated by FERR which is dependent on the current flowing in HCONT.. The error current is added to source GDIS1 to make the sum of the two greater than FCONT causing FCONT to flow through source V8.

Because this is a behavioral model certain restrictions need to be applied to it to prevent the occurrence of illegal conditions which can mathematically occur in the model but can not occur in a physical circuit. Some of these conditions are negative duty cycle, negative output voltage, duty cycles greater than unity, and Vout < Vin. Sources V11A, V11B, VDLIM, ELIM, and diodes D7, 9, 4 all serve to prevent such occurrences. To safeguard against convergence problems 1 gigohm resistors are placed in parallel with current sources which do not have a DC load path.

Design of a Boost Converter With the Aid of Pspice

To verify the hybrid converter computer model a sample design using the linear technologies LT-1070 boost converter was undertaken and the feedback loop stability was analyzed. A continuous conduction current mode boost

regulator with a duty cycle greater than 50% was chosen because according to the literature it is the most difficult configuration to compensate due to a right half plane zero in the response.

A supply with the following specifications was desired:

```
Input Voltage Vin = 5V +/-1V
Output Voltage Vout = 15V
Maximum output current Ioutmax = 300mA
Nominal output current Ioutnom = 100mA
Minimum output current .060mA
Maximum output ripple Vriprms= 100mVp-p
Frequency of operation 40KHZ (fixed by controller
choice)
Current mode control.
```

Figure 49 - Converter Design Specifications.

Design of the converter started with determining the inductance which has the following influences on the design.

1) L determines the peak inductor current ripple and consequently the peak switch current. The peak switch current coupled with the inductance determines the maximum power output of the supply.

2) The LT1070 has current mode control built in with a
fixed amount of slope compensation to make the
regulator stable for duty cycles beyond 50%. Since
the slope compensation is not user adjustable, its
presence imparts a maximum inductor current
discharging slope and consequently a minimum
inductance limit below which subharmonic oscillations
will occur.

3) Also limiting the minimum inductance is the desire to
stay in continuous conduction mode for the specified
load variations.

4) Increasing inductance reduces the supplies ability to
respond to changing load conditions due to the stored
energy in the inductor. It is advantageous to keep
the inductance low to optimize the transient
response.

In an effort to convey the design philosophy used
figures 50 and 51 were created to show the calculations
and tradeoffs used to obtain the final design.

Desired output   Input   Clock Period   Output
    Voltage   Voltage Range   current range

                                               -6
Vout := 15 V   Vin := 5 V   T := 25 10   S   Iomax := 0.300 A
                    Vmax := 6 V   Ionom := 0.100 A
                    Vmin := 4 V   Iomin := .06 A

Reference   Vref := 1.244 V   Slope   5
voltage   Compensation   M := 2 10   Amps/sec

              Vin   Dn(Vin) = 0.667   Compute duty cycle required to
$Dn(Vin) := 1 - \dfrac{Vin}{Vout}$ Dn(Vmax) = 0.6   obtain output voltage Vout for
              Vout   Dn(Vmin) = 0.733   range of Vin.

$DC\_gain := \left[\dfrac{Vout}{Vref}\right]$ DC_gain = 12.058   Gain required to bring
                                                                      reference voltage up to
                                                                      output voltage.

Choose RFB1 keeping in mind that bias current of error amp introduces an
error voltage across the parallel combination.

            5   RFB1   3
RFB1 := 1 10   ohms $RFB2 := \dfrac{RFB1}{DC\_gain - 1}$ RFB2 = 9.043 10   ohms

---

Calculate the minimum inductance required for stability with slope
compensation.

                                                     -5
$Lmin := \left[\dfrac{Vout - 2\,Vmin}{M}\right]$ Lmin = 3.5 10   H

   Compute Critical Inductance in henrys at minimum output
   current Iomin maximum input voltage.

D := Dn(Vmax)   D = 0.6

         $Lcrit := \dfrac{(1 - D)\,D\,T\,Vin}{2\,Iomin}$ -4   -6
                                            Lcrit = 2.5 10   H   L := 280 10   H

   Critical inductance is bigger than Lmin so set inductor to
   nearest standard value above Lcrit.

Figure 50 - Design Equations Part 1.

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For the chosen value of L compute the Inductor current parameters in Amps at maximum output current minimum output current.

$V := Vmin$
$D := Dn(V)$

$$Ipp(D,Vin) := \left[\frac{D\ T\ Vin}{L}\right]$$

Peak to Peak Inductor current.
$Ipp(D,V) = 0.262$ A

$$Iavg(Iout,D) := \left[\frac{Iout}{1-D}\right]$$

Average Inductor current.
$Iavg(Iomax,D) = 1.125$ A

$$Ipk(Iout,D,Vin) := \left[\frac{Iout}{1-D} + \frac{Ipp(D,Vin)}{2}\right]$$

Peak Inductor current.
$Ipk(Iomax,D,V) = 1.256$ A

Minimum Inductor current.
$$Imin(Iout,D,Vin) := (Ipk(Iout,D,Vin) - Ipp(D,Vin))$$ $Imin(Iomax,D,V) = 0.994$ A

Choose output capacitor based on ripple from esr and charge exchange.

Ripple from charge exchange
$Vrc := .050$ V

Ripple from ESR
$Vesr := .05$ V

$$C(D,Iout) := \frac{Iout\ D\ T}{Vrc}$$

$$Cesr(Iout,D,Vin) := \frac{Vesr}{Ipk(Iout,D,Vin)}$$

Worst case component values

$C(Dn(Vmin),Iomax) = 1.1\ 10^{-4}$ F $Cesr(Iomax,Dn(Vmin),Vmin) = 0.04$ ohms

---

Nominal case component values

$C(Dn(Vin),Ionom) = 3.333\ 10^{-5}$ F $Cesr(Ionom,Dn(Vin),Vin) = 0.111$ ohms

---

Since a 100UF capacitor with an esr of .100 is the best which is available it is necessary to recalculate the impact of this on total ripple. If further improvement is needed then an adioional ouptu filter or an increase in inductance is required.

Choose $C := 100\ 10^{-6}$ F   and $Cesr := .100$ ohms

$$Vrip(Iout,D,Vin) := \frac{Iout\ D\ T}{C} + Cesr\ Ipk(Iout,D,Vin)$$ Total ripple

$Vrip(Iomax,Dn(Vmin),Vmin) = 0.181$ V   Worst case

$Vrip(Ionom,Dn(Vin),Vin) = 0.062$ V   Nominal

Figure 51 - Design Equations Part 2.

For the design case chosen the duty cycle range was determined and then the critical inductance was calculated. Next the minimum inductance required to keep the regulator free from subharmonic instability with the internally fixed slope compensation of the LT1070 was calculated. In this case, the critical inductance proved to be the limiting factor for minimum inductance so the inductor was chosen to be a standard value slightly above the critical inductance. The inductor current parameters I_{max}, I_{min}, and I_{pp} were calculated at the worst case condition of minimum duty cycle with maximum load current, and were compared to the peak switch current specification of the LT1070 and the saturation current spec of the inductor.

Determining the output filter capacitor capacitance, voltage rating, and equivalent series resistance (ESR) at the frequency of the clock was done with output ripple as the primary concern. Output ripple is caused by the peak to peak inductor current generating an IR drop across the ESR of the output capacitor; and by discharge of the output capacitor during the inductor charging period, or addition of charge during the inductor discharge period. As a first approximation, half the ripple was designated to be ESR induced, and half charge exchange induced. Maximum ripple voltage occurs at minimum input voltage

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with maximum output current, so the component values were initially calculated at this point. This yielded a rather stringent requirement on the ESR, so a compromise described in figure 51 was made to allow capacitor with an ESR of 0.10 ohms to be used. The ripple current rating of the capacitor was then checked to verify that it was less than the peak to peak inductor current.

To adapt the model in figure 46 to the LT1070, information regarding slope compensation, error amplifier topology, current mode control implementation, and DC reference implementation were obtained or inferred from the LT1070 data sheet. The data sheet refers to error amplifier with a transconductance GMEA, open loop gain AV, and a single pole high frequency roll-off shown in a gain-phase plot. From this a model which implements this behavior was implemented as shown in figure 52 where feedback loop compensation has been added by the series RC network RCMP and CCMP which generates a zero and a pole described in figure 52D in the error amplifier response.
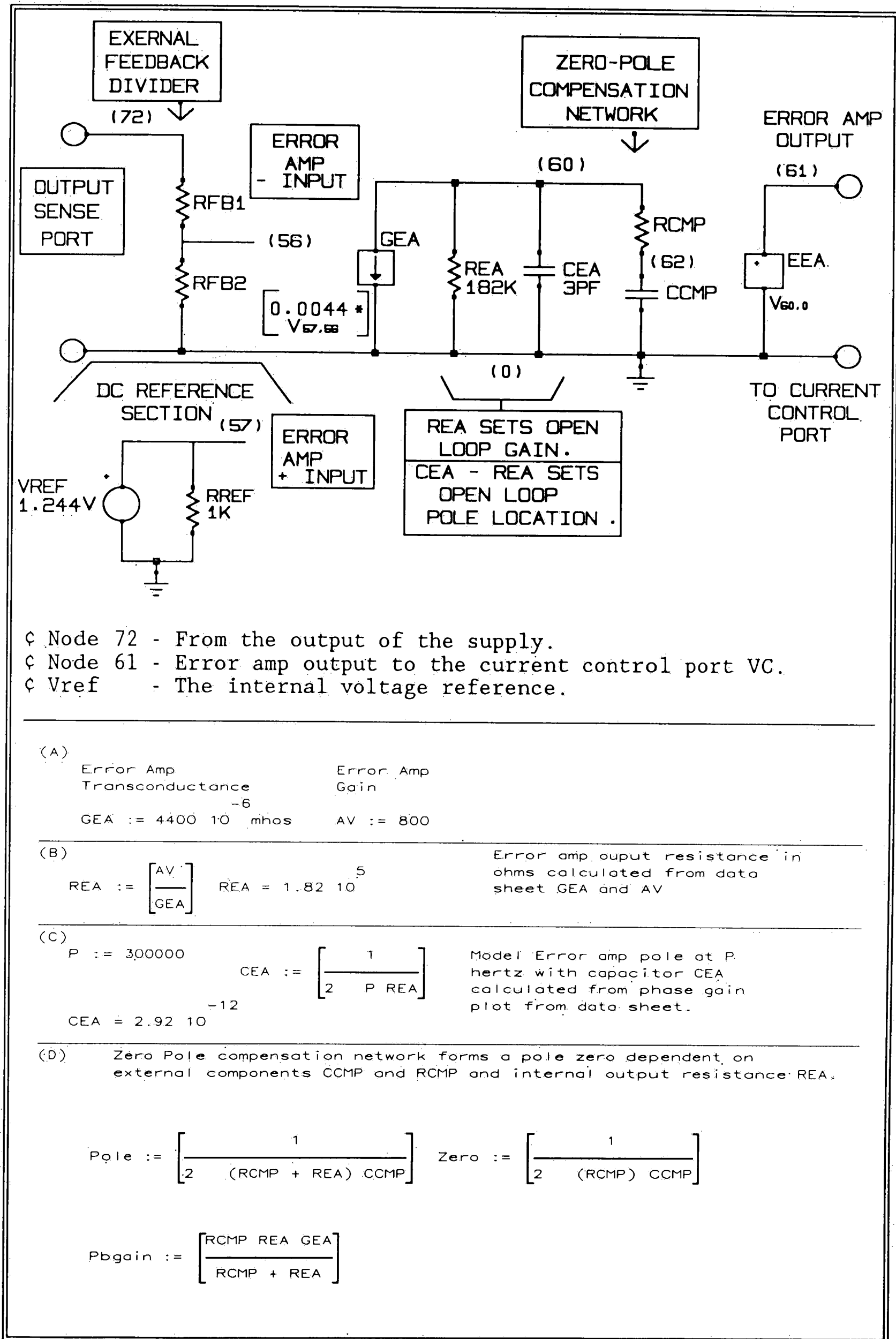
EXERNAL
FEEDBACK
DIVIDER
(72) ↓

ZERO-POLE
COMPENSATION
NETWORK
↓

ERROR AMP
OUTPUT
(61)

OUTPUT
SENSE
PORT

ERROR
AMP
- INPUT

(60)

RFB1

(56)

GEA

REA
182K

CEA
3PF

RCMP

(62)

CCMP

EEA

$V_{60.0}$

RFB2

$\begin{bmatrix} 0.0044 * \\ V_{57.56} \end{bmatrix}$

DC REFERENCE
SECTION
(57)

ERROR
AMP
+ INPUT

(0)

TO CURRENT
CONTROL
PORT

VREF
1.244V

RREF
1K

REA SETS OPEN
LOOP GAIN.
CEA - REA SETS
OPEN LOOP
POLE LOCATION.

¢ Node 72 - From the output of the supply.
¢ Node 61 - Error amp output to the current control port VC.
¢ Vref   - The internal voltage reference.

(A)
Error Amp
Transconductance

Error Amp
Gain

$GEA := 4400 \ 10^{-6}$ mhos $AV := 800$

(B)

$REA := \begin{bmatrix} \dfrac{AV}{GEA} \end{bmatrix}$ $REA = 1.82 \ 10^{5}$

Error amp ouput resistance in
ohms calculated from data
sheet GEA and AV

(C)
$P := 300000$

$CEA := \begin{bmatrix} \dfrac{1}{2 \quad P \ REA} \end{bmatrix}$

$CEA = 2.92 \ 10^{-12}$

Model Error amp pole at P
hertz with capacitor CEA
calculated from phase gain
plot from data sheet.

(D)   Zero Pole compensation network forms a pole zero dependent on
external components CCMP and RCMP and internal output resistance REA.

$Pole := \begin{bmatrix} \dfrac{1}{2 \quad (RCMP + REA) \ CCMP} \end{bmatrix}$ $Zero := \begin{bmatrix} \dfrac{1}{2 \quad (RCMP) \ CCMP} \end{bmatrix}$

$Pbgain := \begin{bmatrix} \dfrac{RCMP \ REA \ GEA}{RCMP + REA} \end{bmatrix}$

Figure 52 - Calculation of Error Amplifier Model
Parameters.

The current control signal port and the current mode sensing mechanism of the LT-1070 are slightly different than originally discussed in the current mode boost model. Potential across the current sense resistor is amplified by a factor of six so the resistor R_s in the model is entered in as 6 times its actual value in the block diagram of the LT-1070.

The final model of the LT1070 with all the parameters calculated, the error amplifier added, and the nominal output load added is shown in figures 52 and 53. To check the model a simulation of V_{out}, I_{in}, I_{out}, D, and $(I_{out}/(1-D))$ versus V_C into a fixed load was run and checked to make sure that the numbers seemed reasonable (Figure 54) (Note that $(I_{out}/(1-D))$ and I_{in} track each other as they should). Next the feedback loop was closed and the DC bias point was calculated to find the nominal values of duty cycle and V_C for the purpose of double checking them against the design points. The duty cycle came out to 66% as expected with the model in continuous mode.

Figure 53 – Final Model of Boost Converter.

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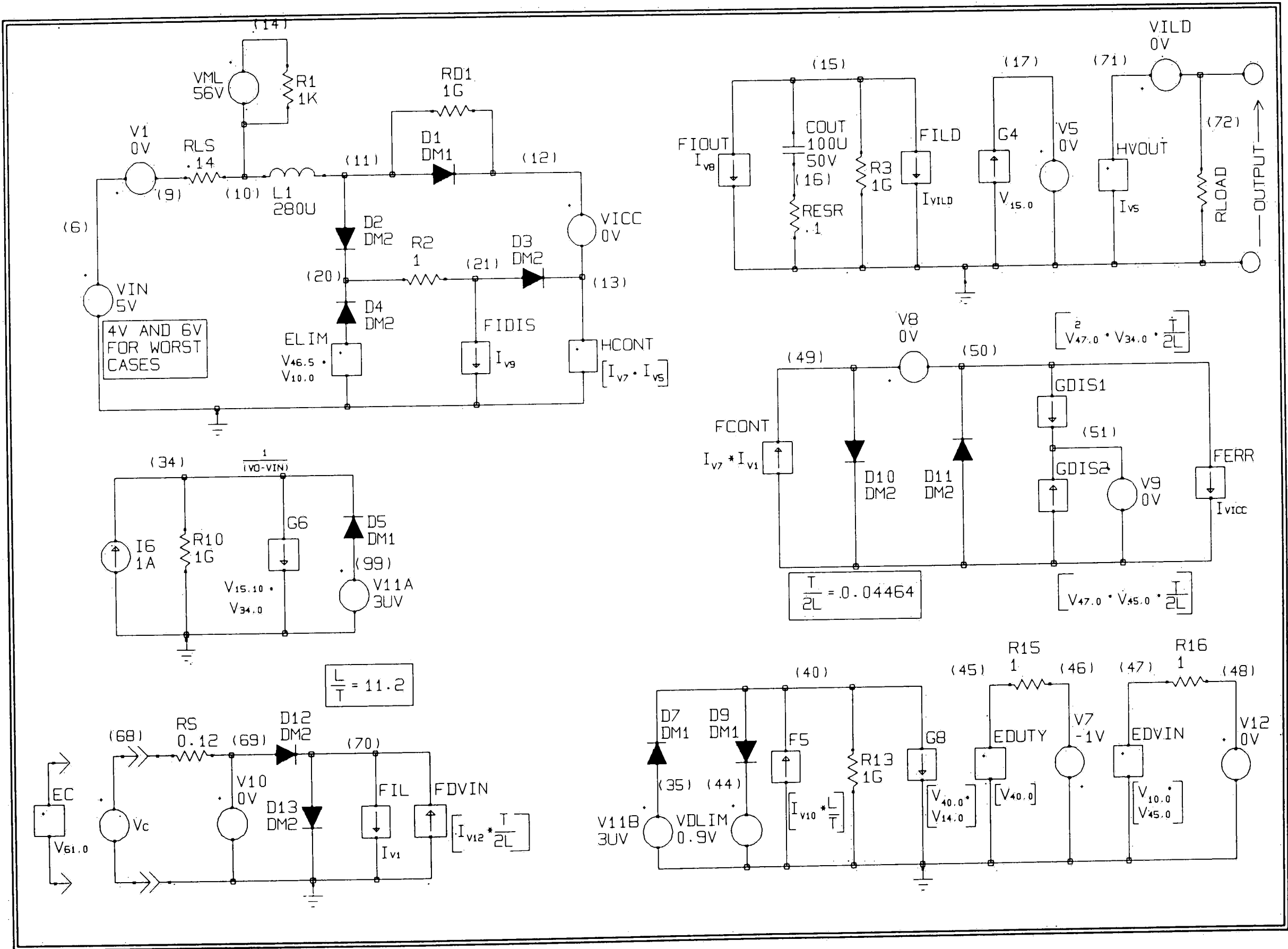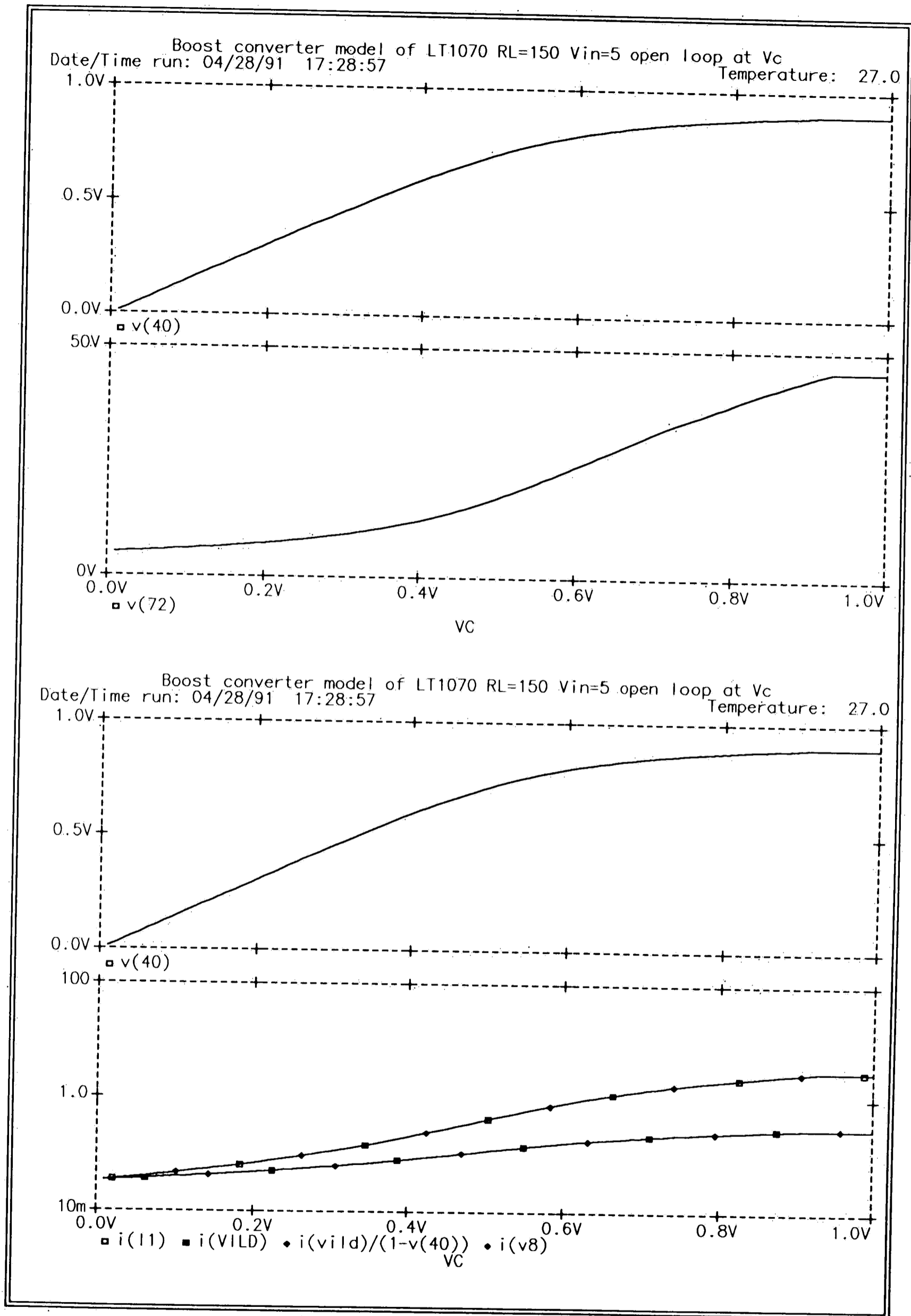
Figure 54 - DC simulation of Finished Circuit.
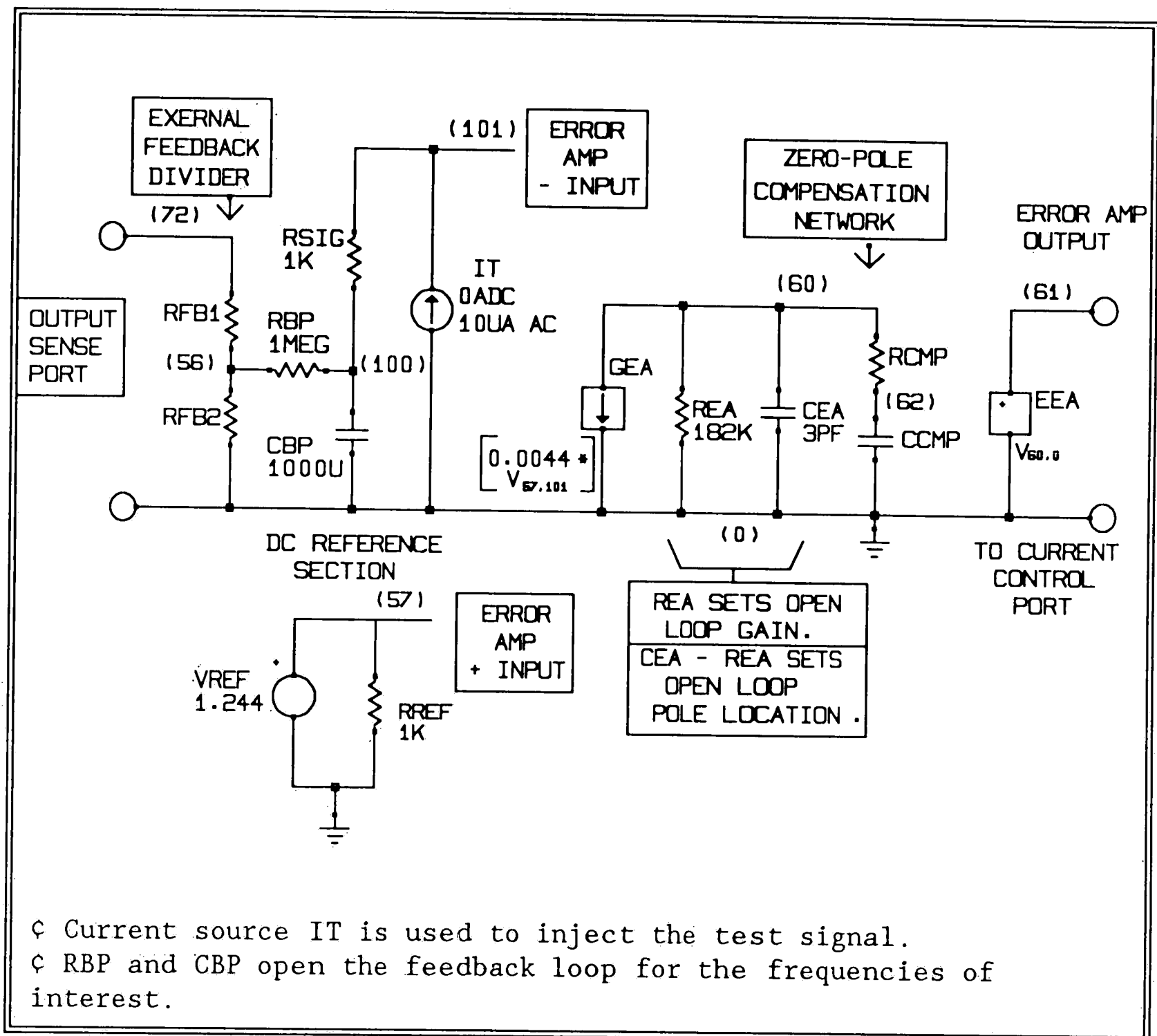
Figure 55 - Error Amplifier Model for Phase and Gain Simulations.

Simulation of the loop gain and phase requires the feedback loop to be open for the frequencies of interest. Modifications to the model were made to severely attenuate the AC components of the feedback while still passing the DC portion of the feedback signal making it possible for pspice to converge on the correct bias point. A test signal to evaluate the loop gain and phase was injected by current source IT at the inverting input of the error amp as shown in figure 55. The error amp compensation network

was disconnected to remove any compensation and the gain and phase of the regulator for the nominal load condition of RL=150 ohms was simulated. From the gain and phase plot the location of the compensation pole and zero was determined using the method described below.
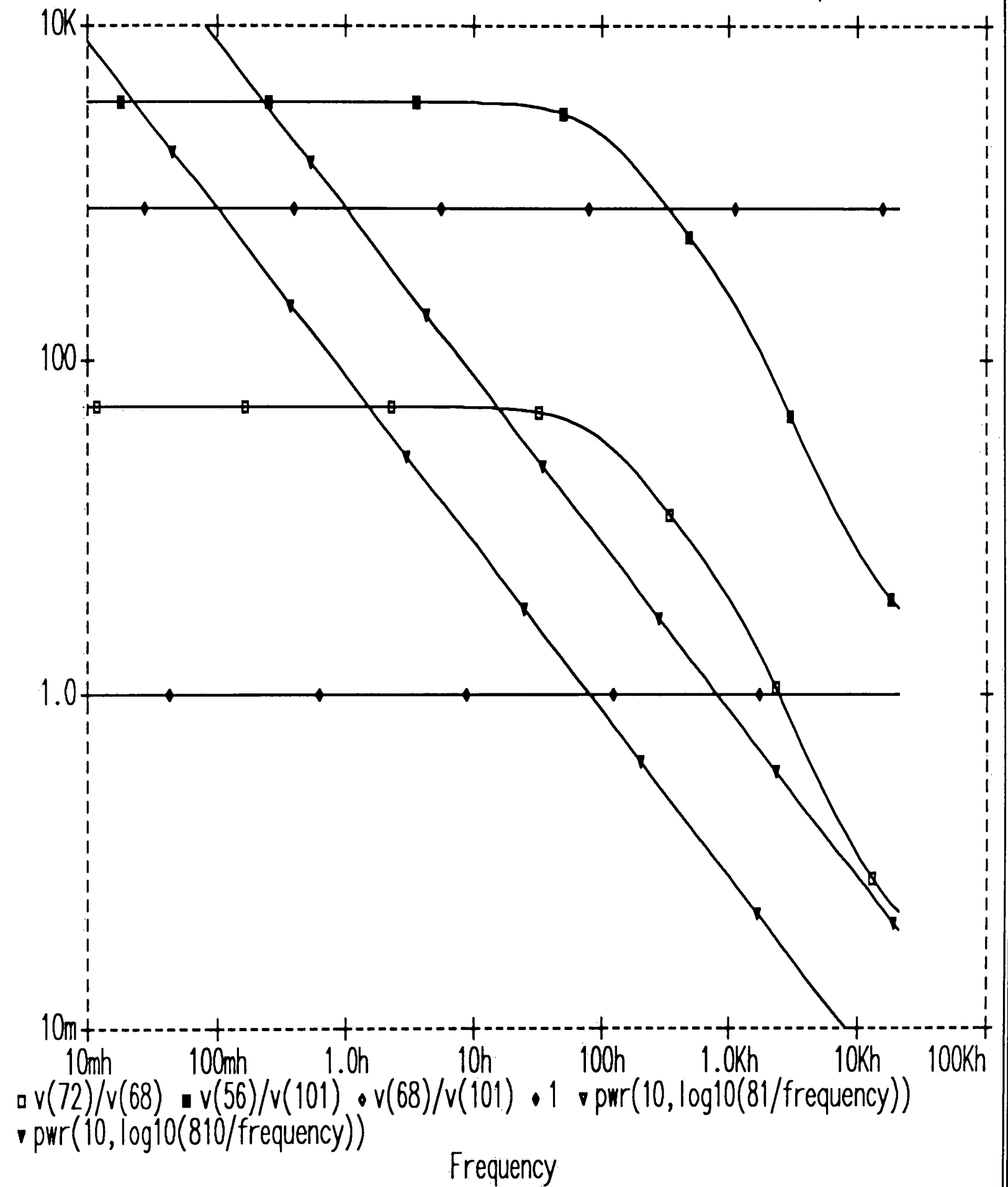
Figure 56 - 150 ohm Load Gain Plot With No Compensation.
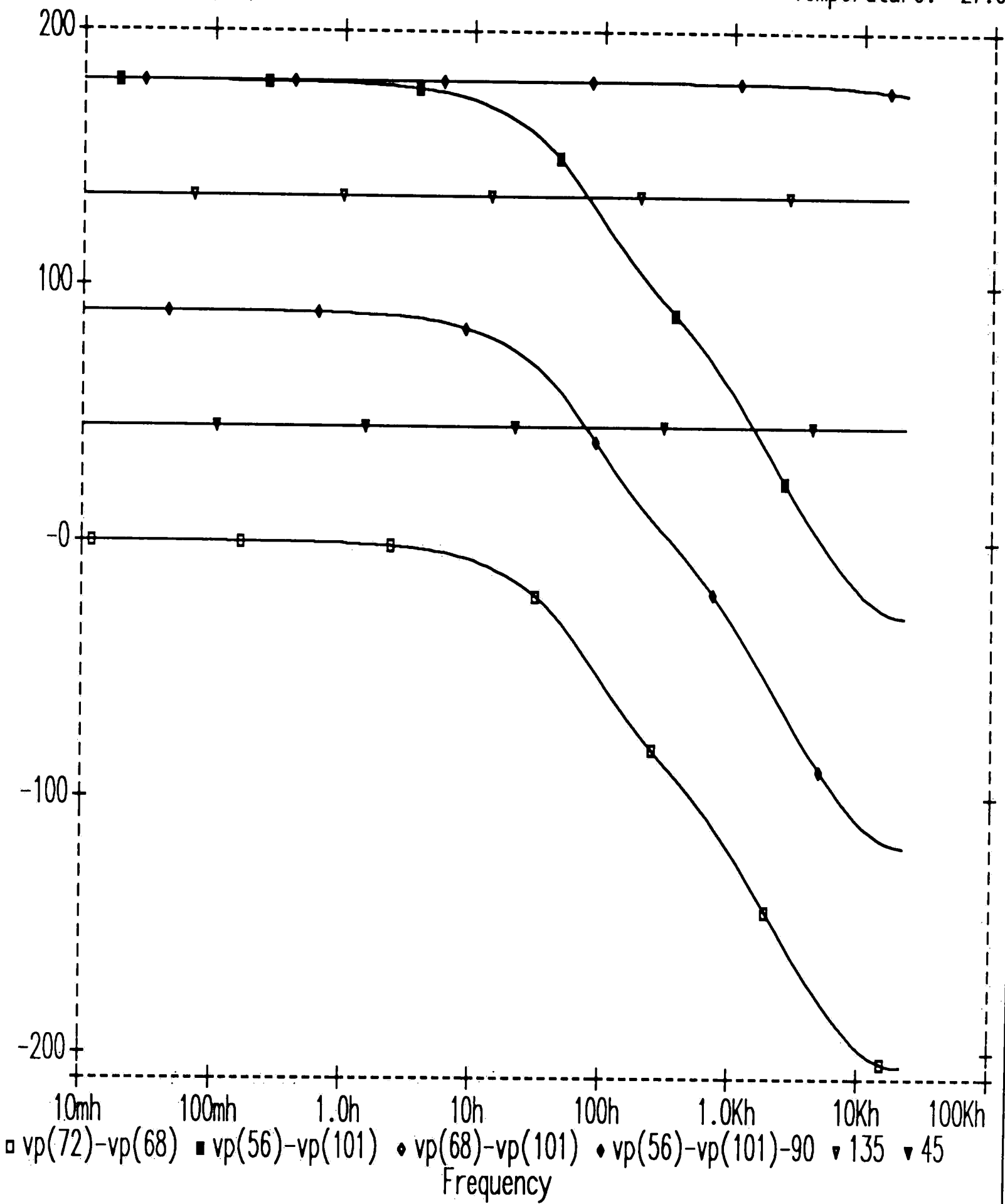
Figure 57 - 150 ohm Load Phase Plot With No Compensation.

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Compensation of the regulator was approached by a graphical method using the previous plots to compensate the error amplifier to yield a design goal of 45 degrees of phase margin for the regulator-error amplifier cascade. To accomplish this, the frequency at which there is a 135 degrees (90 + 45) of phase margin was located on the phase plot in figure 57 and transferred to the gain plot unity gain line in figure 56. If this frequency were to be used to implement a single dominate pole compensation network the unity gain crossing point would have 45 degrees of phase margin. To find the location of the dominate pole, the unity gain point is extended upward at a slope of negative one decade in gain per decade in frequency to where it crosses the gain of the error amp - regulator cascade. The intersection point is the location of dominate pole p1 which would provide a stable closed loop system. Since we are using a zero-pole compensating network, we can assume that a factor of ten improvement in unity gain cut off frequency can be obtained over the dominate pole network scheme due the phase lead of the zero. The pole p1 was moved a factor of ten higher to location p2 to reflect the use of such a scheme.

With the pole located, the location of the zero needs to be determined. The zero should be located at as low a frequency as possible to maintain the loop gain but not so

low that the unity gain cross over point is raised to where the system becomes unstable. This point is chosen from figures 56 and 57 to be 100Hz.

(A)

Error Amp
Transconductance

Error Amp
Gain

$GEA := 4400 \cdot 10^{-6}$ mhos

$AV := 800$

(B)

$REA := \left[\dfrac{AV}{GEA}\right]$

$REA = 1.82 \cdot 10^{5}$

Error amp ouput resistance in ohms calculated from data sheet GEA and AV

(C)

$P := 300000$

$CEA := \left[\dfrac{1}{2 \cdot P \cdot REA}\right]$

$CEA = 2.92 \cdot 10^{-12}$

Model Error amp pole at P hertz with capacitor CEA calculated from phase gain plot from data sheet.

(D) Zero Pole compensation network forms a zero pole dependent on external components CCMP and RCMP and internal output resistance REA.

$Zero := 100$ $Pole := .25$ $RCMP := 0$ $RCMP<<<REA$

$CCMP := \left[\dfrac{1}{2 \cdot (RCMP + REA) \cdot Pole}\right]$

$RCMP := \left[\dfrac{1}{2 \cdot (Zero) \cdot CCMP}\right]$

$Pbgain := \left[\dfrac{RCMP \cdot REA \cdot GEA}{RCMP + REA}\right]$

$CCMP = 3.5 \cdot 10^{-6}$ $RCMP = 4.55 \cdot 10^{2}$

$Pbgain = 2$

Figure 58 - Calculation of Component Values to Obtain Desired Pole Zero Location.

The calculation of the component values to set pole and zero is carried out in figure 58. To check the pole-zero location the calculated value of REA and CEA were entered into the model and the gain and phase were again plotted. It was observed that the phase margin was 70

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degrees so the pole was move up to raise the cut off
frequency and reduce the phase margin.

A check of the regulator compensation for the new
pole location was accomplished by simulating the gain and
phase for all four combinations of load and input voltage
(See figures 60 - 65). From these plots it can bee see
that the phase margin is the worst for minimum input
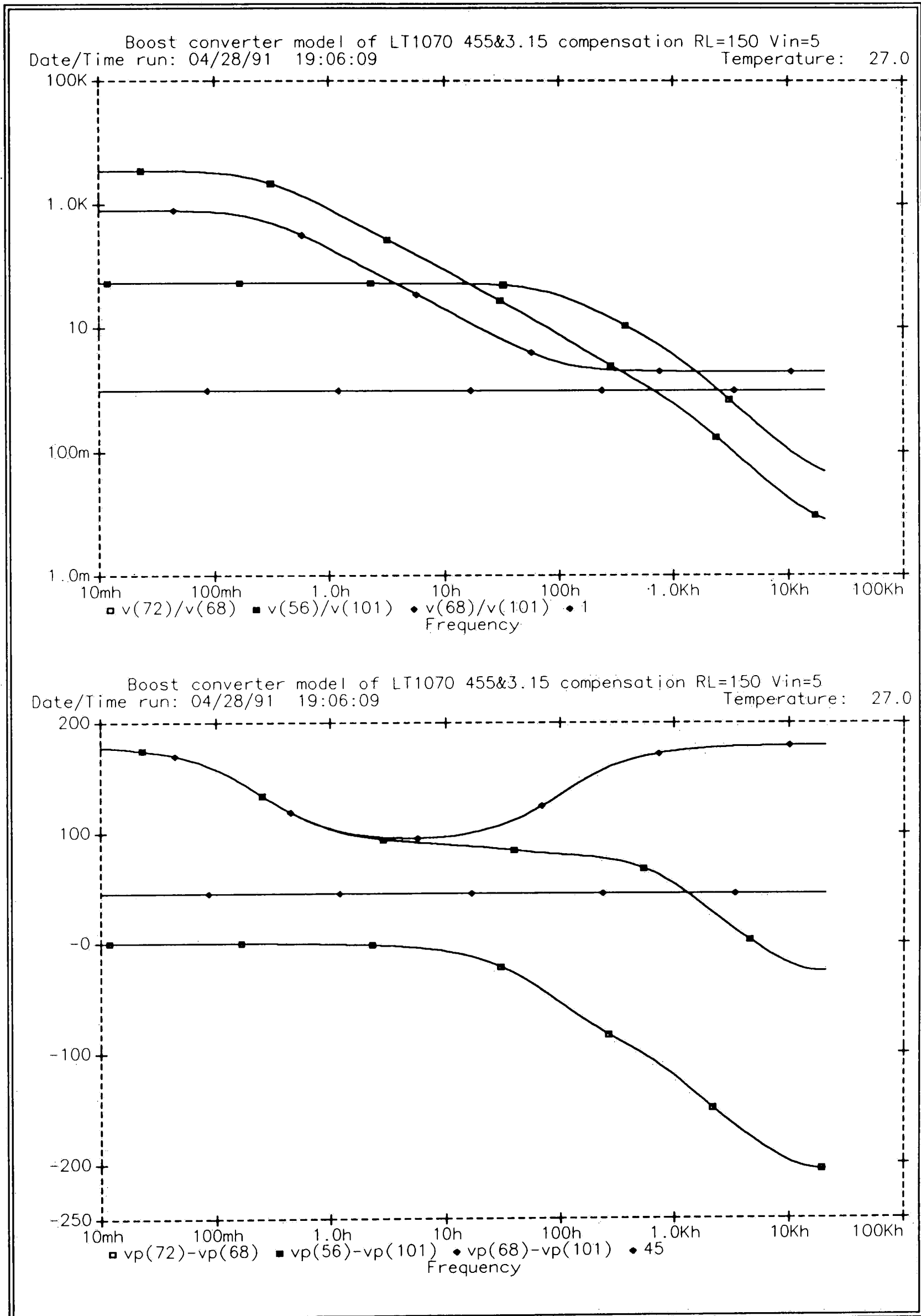voltage maximum load but all cases fall within the design
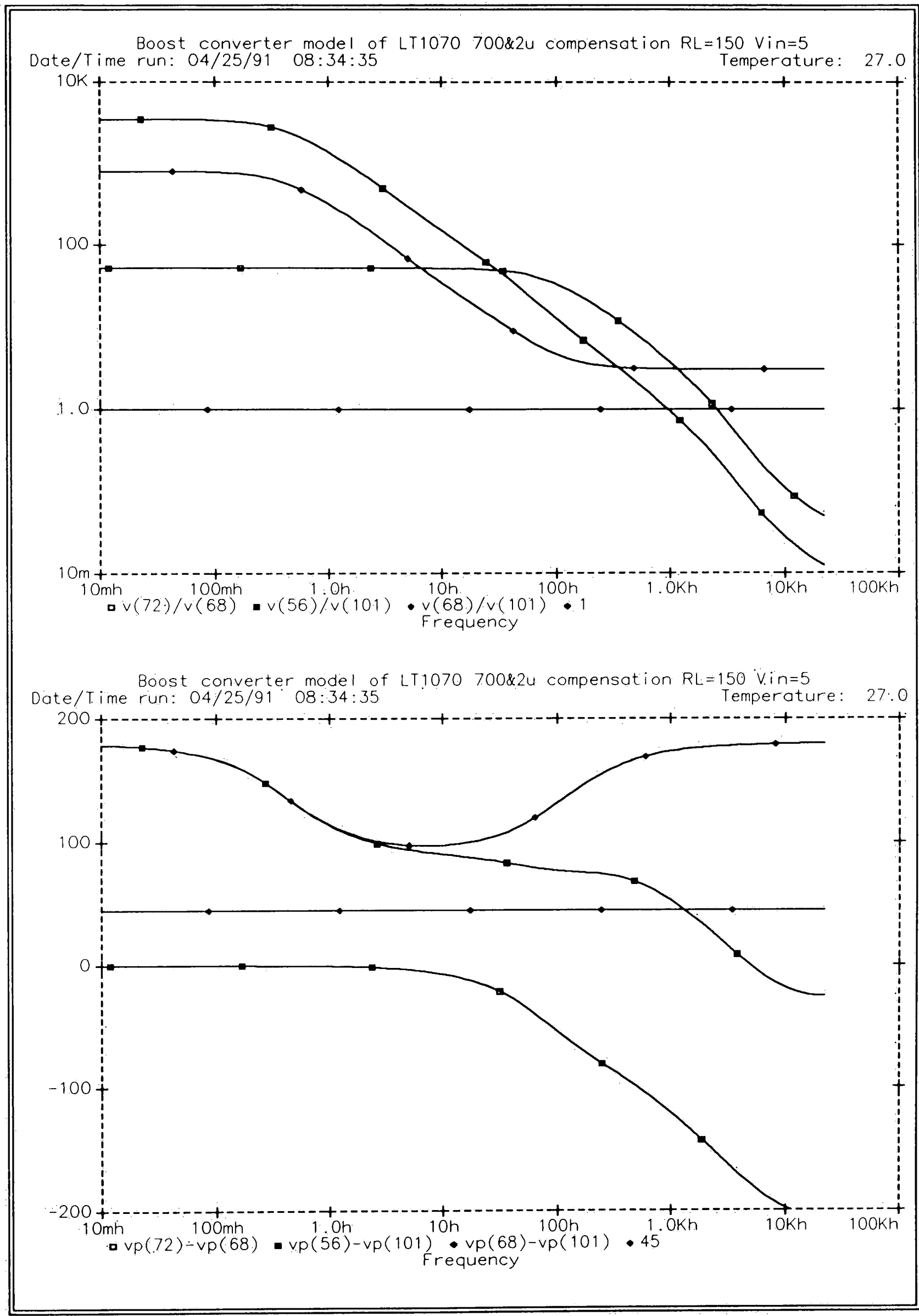goal of 45 degrees.

Figure 59 - Gain and Phase for Initial Pole Location.

Figure 60 - Gain and Phase for Pole Moved to 0.45 Hz.
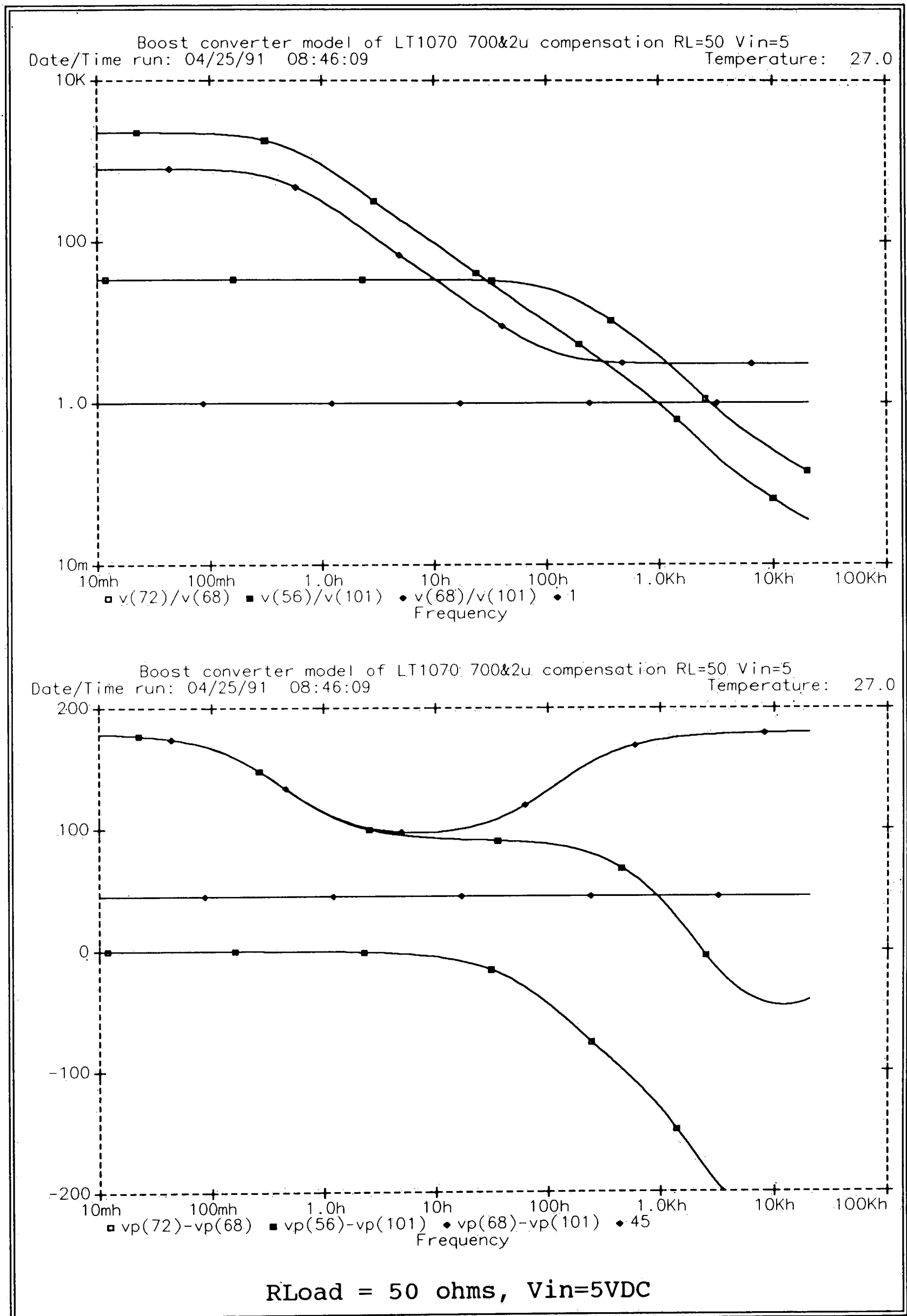
Figure 61 - 50 ohm Load Gain and Phase for Nominal Input.
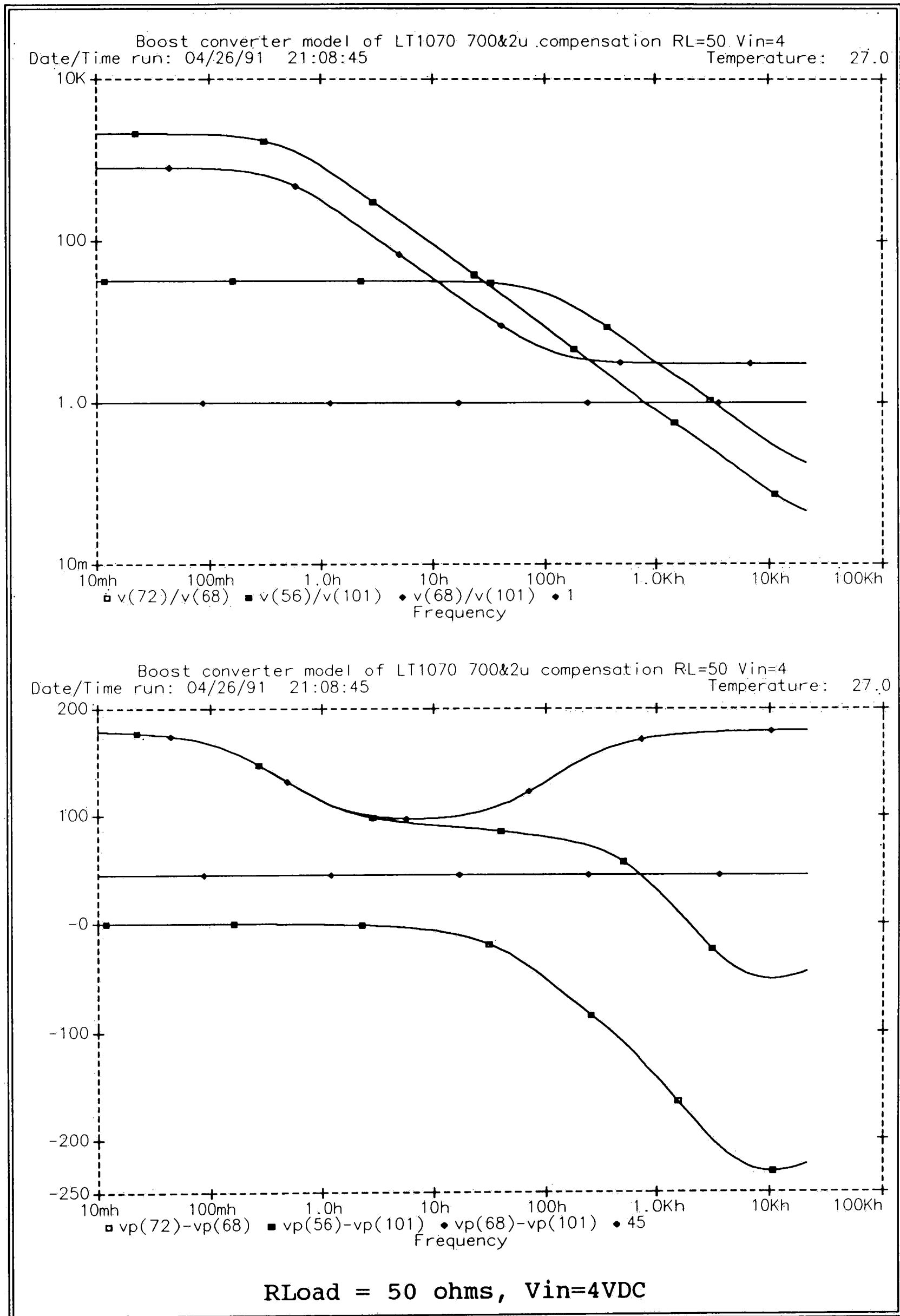
Figure 62 - 50 ohm Load Gain and Phase for Minimum Input.
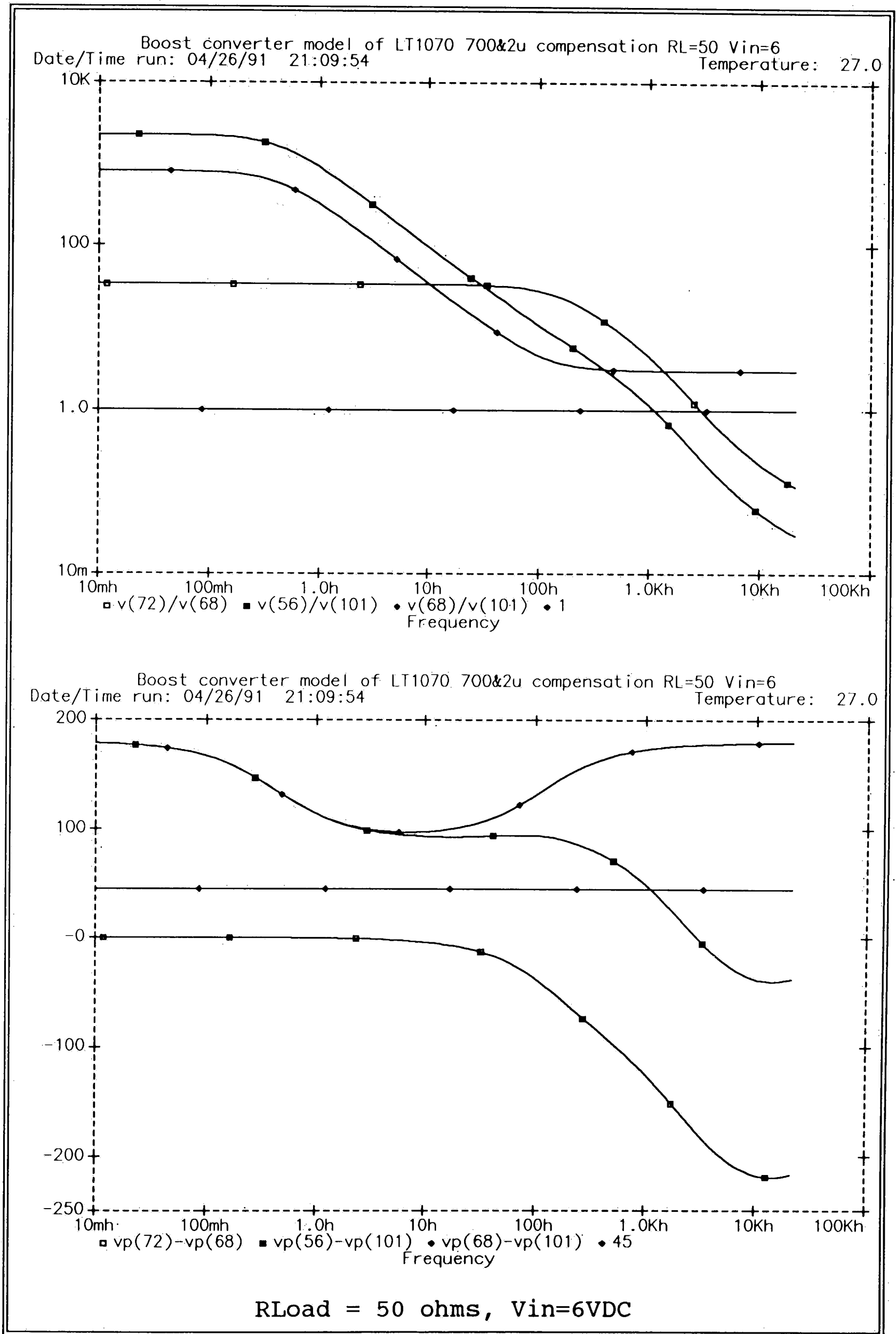
Figure 63 - 50 ohm Load Gain and Phase for Maximum Input.
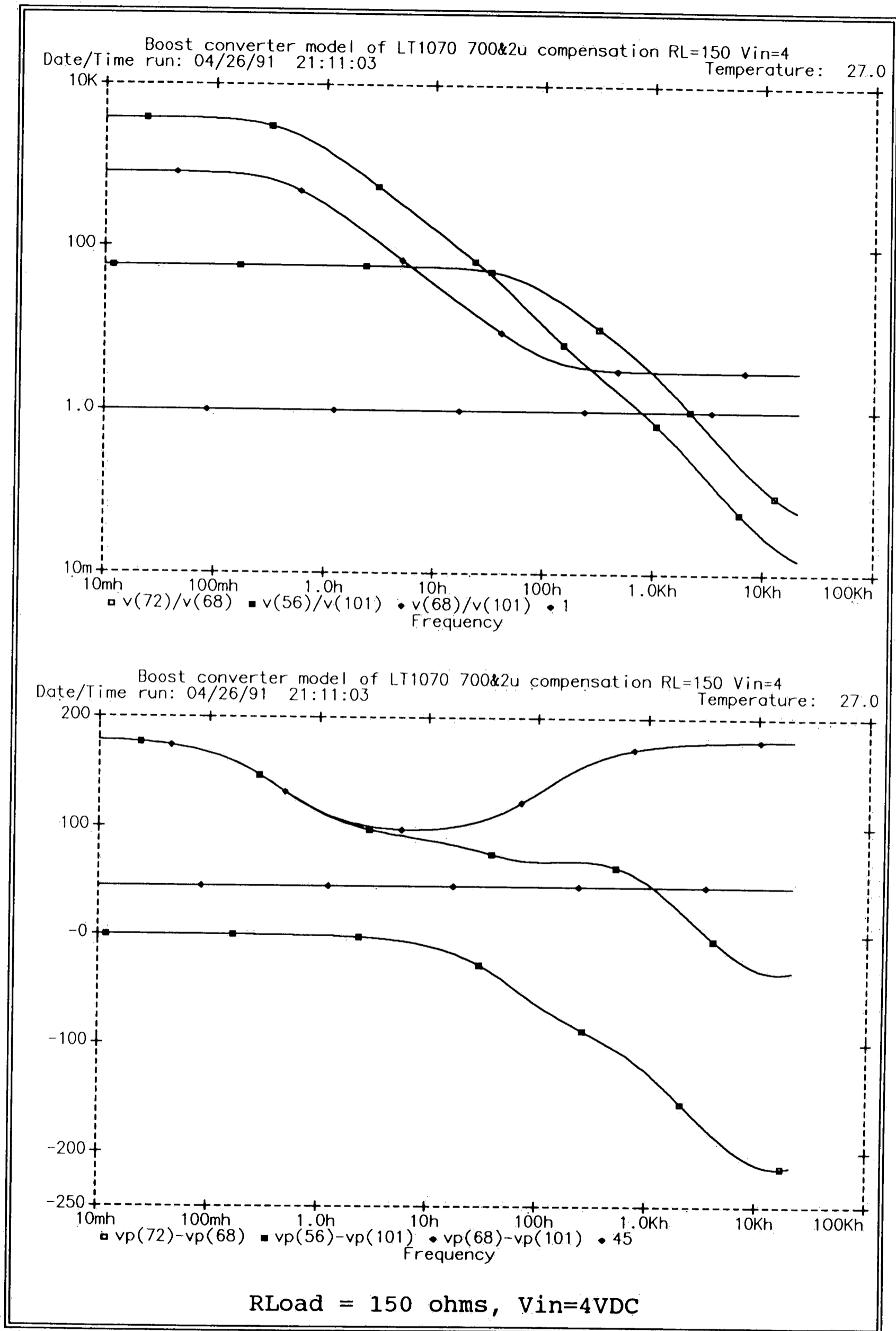
Figure 64 - 150 ohm Load Gain and Phase for Minimum Input.
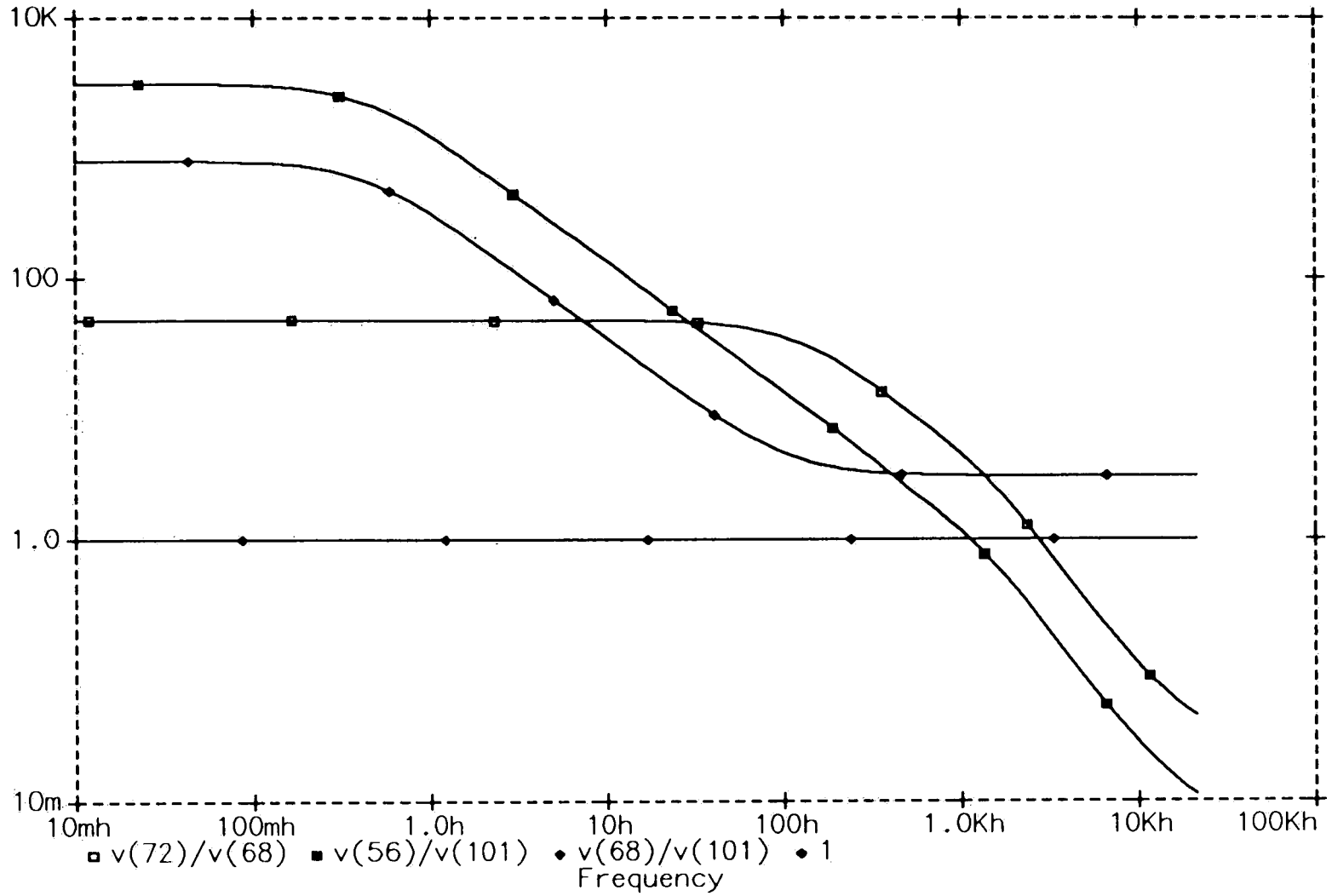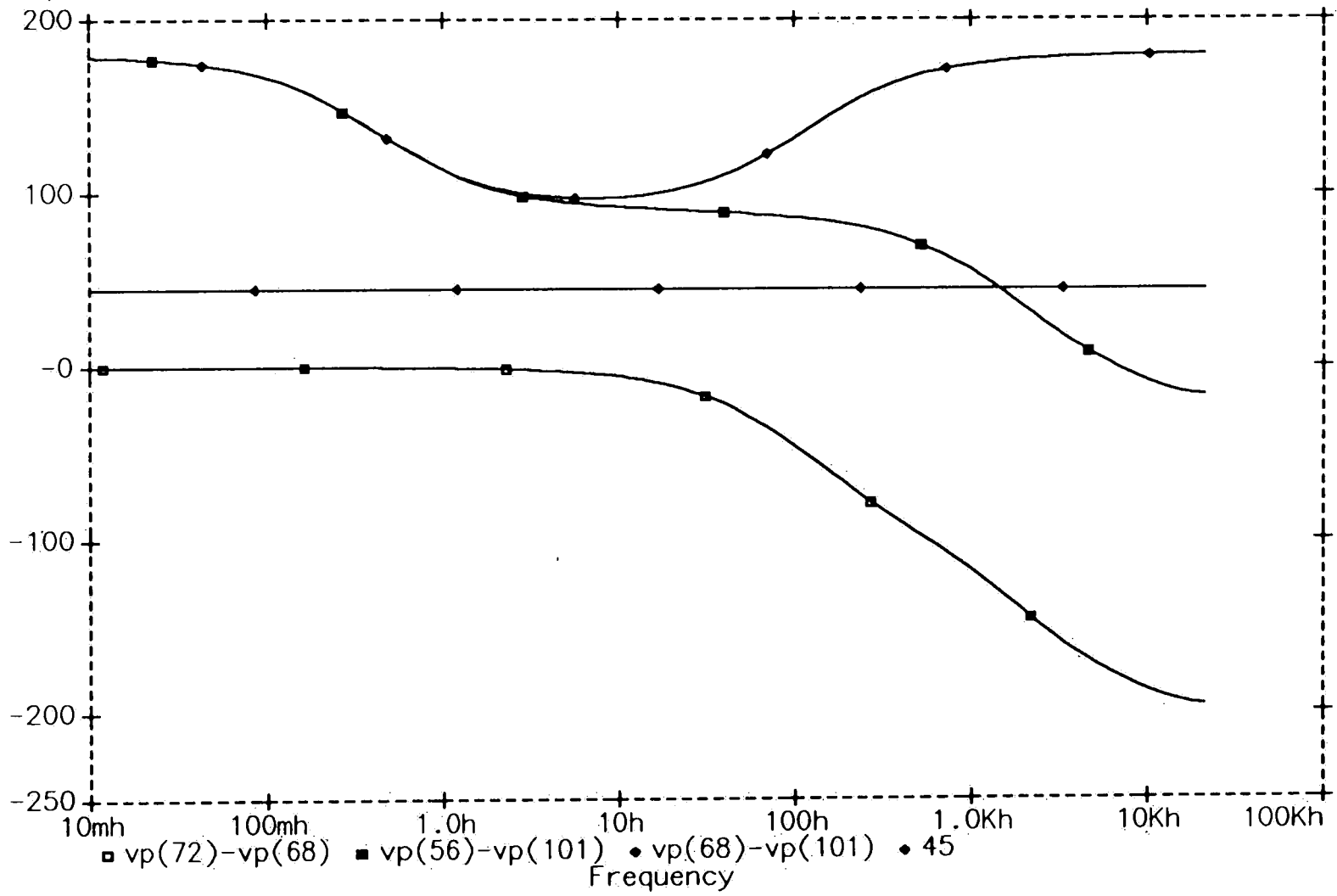
Figure 65 - 150 ohm Load Gain and Phase for Maximum Input.
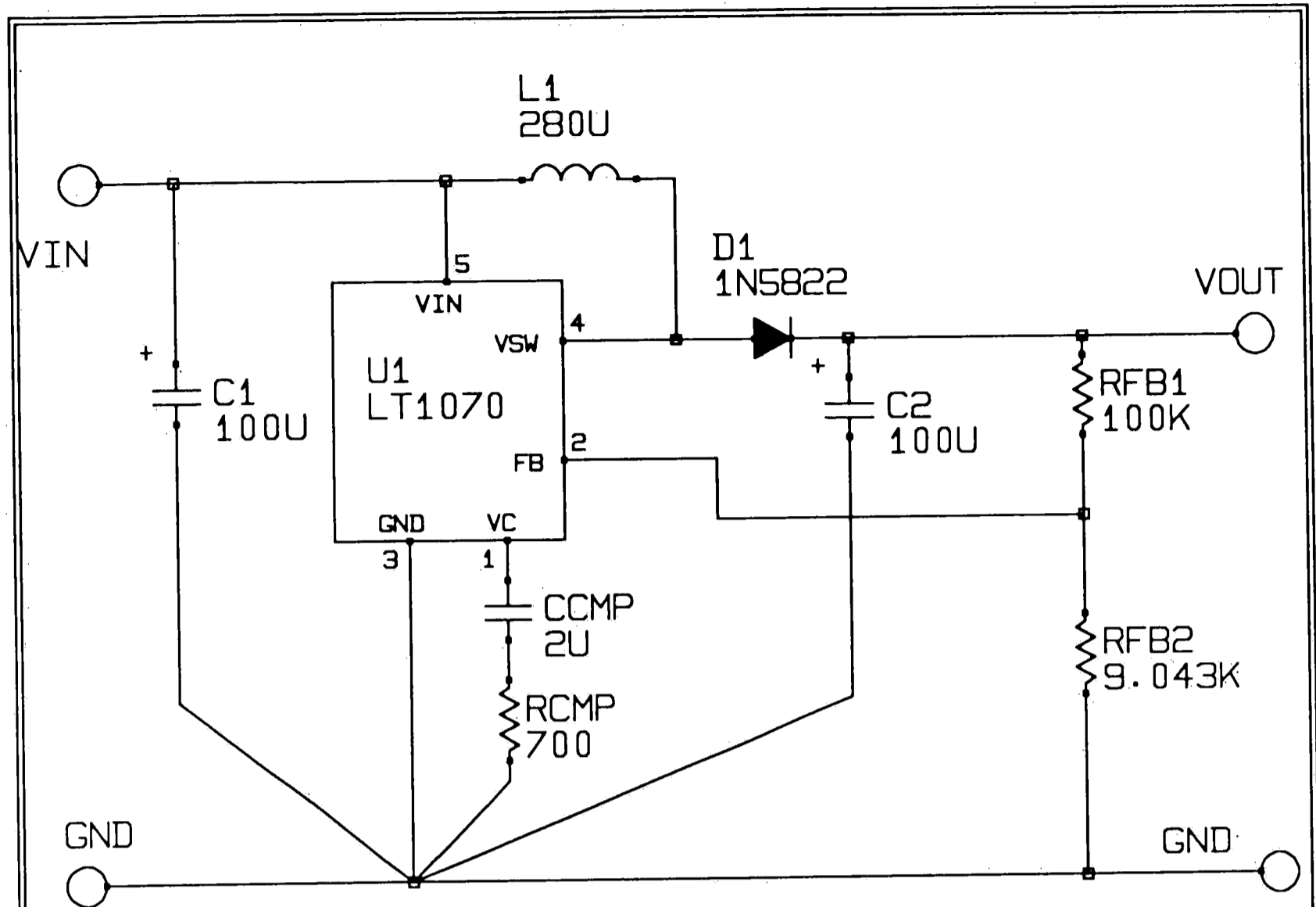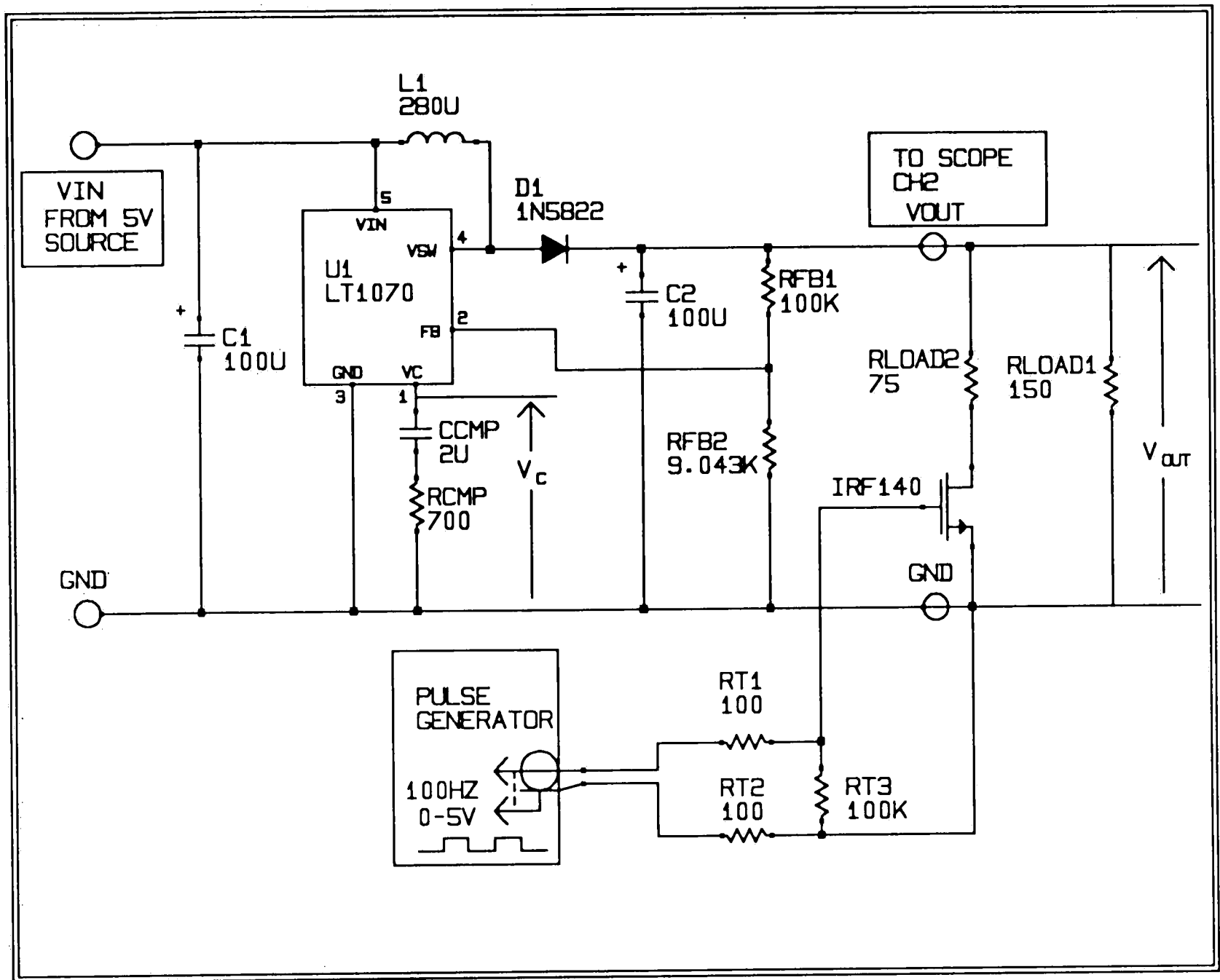
Figure 66 - Prototype Circuit With Component Values.

Figure 67 - Variable Load Test Circuit.

Design Verification

To check the model accuracy, the circuit was constructed per the schematic in figure 66. Although when powered up, the circuit appeared to be stable, the stability was further scrutinized by pulsing the output current between maximum output current I_{max} and the nominal output current I_{nom}, while monitoring the output for sustained ringing (See figure 67 for the test setup and figure 68 for output waveforms). The circuit was found to be stable as predicted by the simulations.
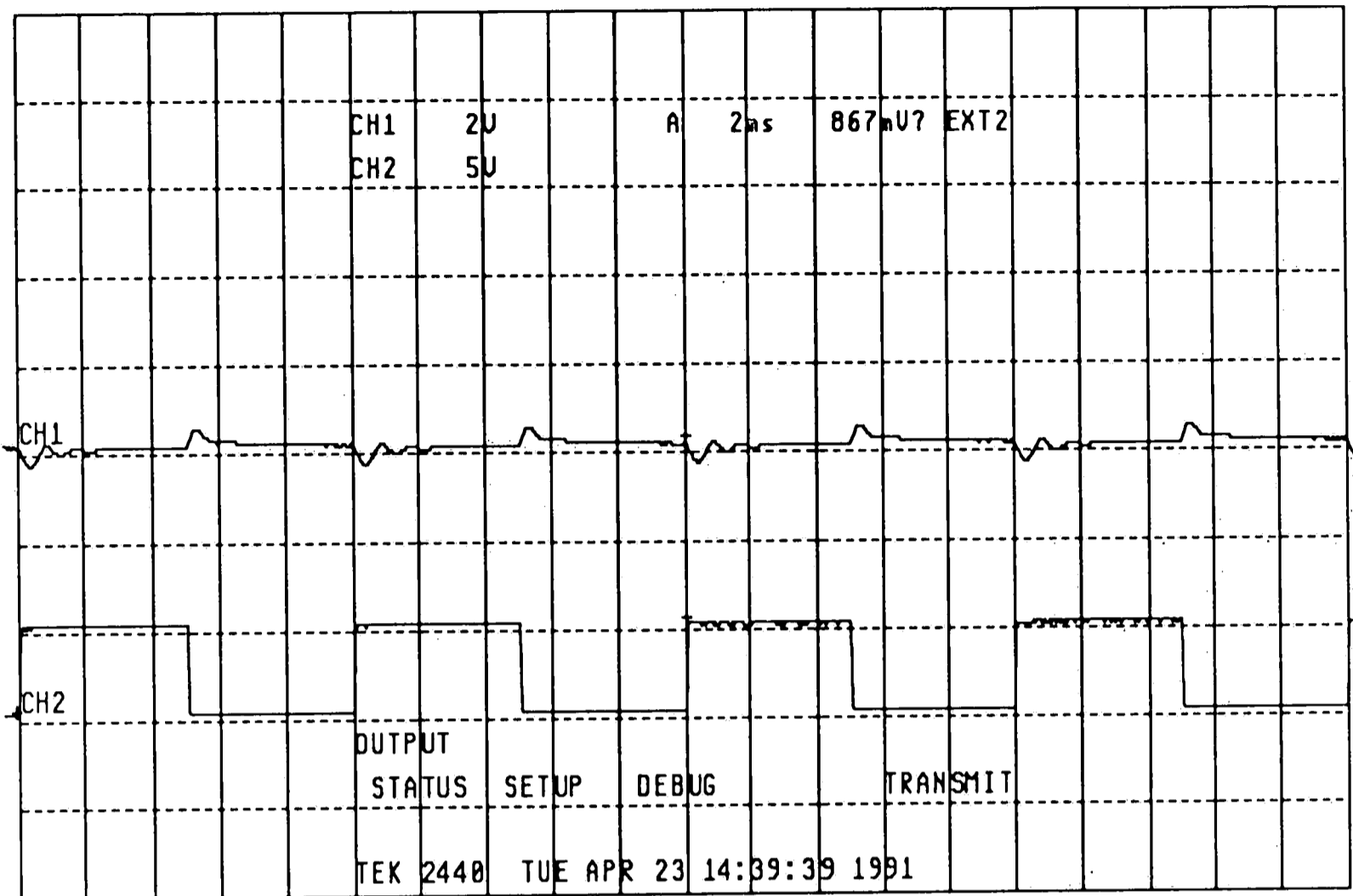
CH1 - Vout (DC coupled)
CH2 - Gate drive to IRF140 MFET (High= 50 ohm load).
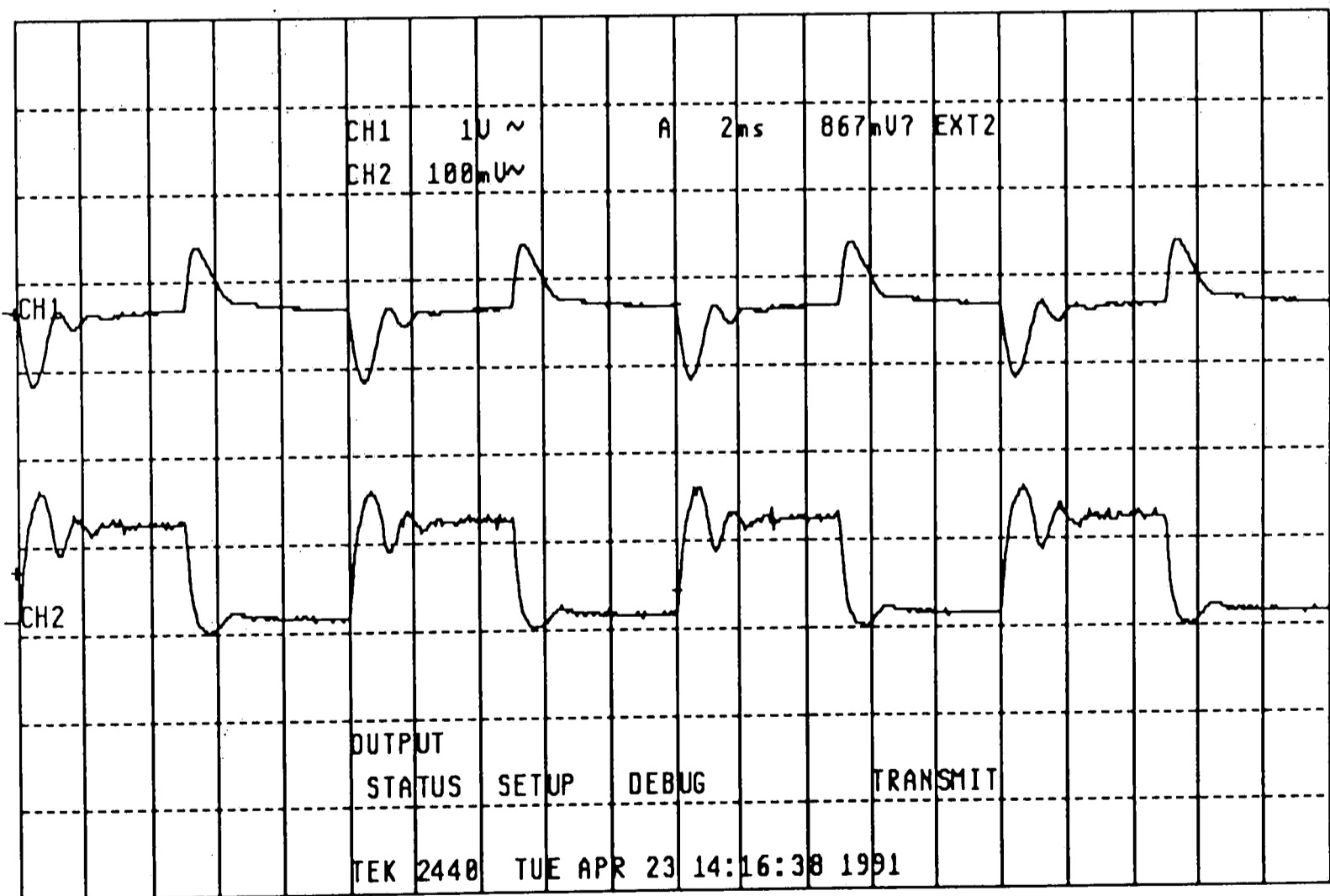
CH1 - Vout (AC coupled)
CH2 - Error amplifier output (VC).

Figure 68 - Transient Response.

Measurement of the open loop gain and phase for the purpose of checking the pspice model was accomplished using the test circuit shown in figure 69. Accurately measuring V_{out} in the presence of the output ripple signal proved to be troublesome. A scope with digital averaging was utilized to average out signals which were non-synchronous to the input test signal.

Plots of the measured gain and phase are shown in figure 70 where it can be seen that the gain and phase agree with the simulation for frequencies below 5KHZ, but the phase tends to be larger than that predicted by the model for higher frequencies. Causes of the disagreement in phase are most likely linked to the frequency limitations of the sampled data nature of the models as discussed in the state space averaging section of this paper. The model is ideally only usable for frequencies up to one half the switching frequency, (20KHZ in the case of this circuit) so it is not at all suspicious that the phase is going awry for frequencies within 2 octaves of the theoretical limit.
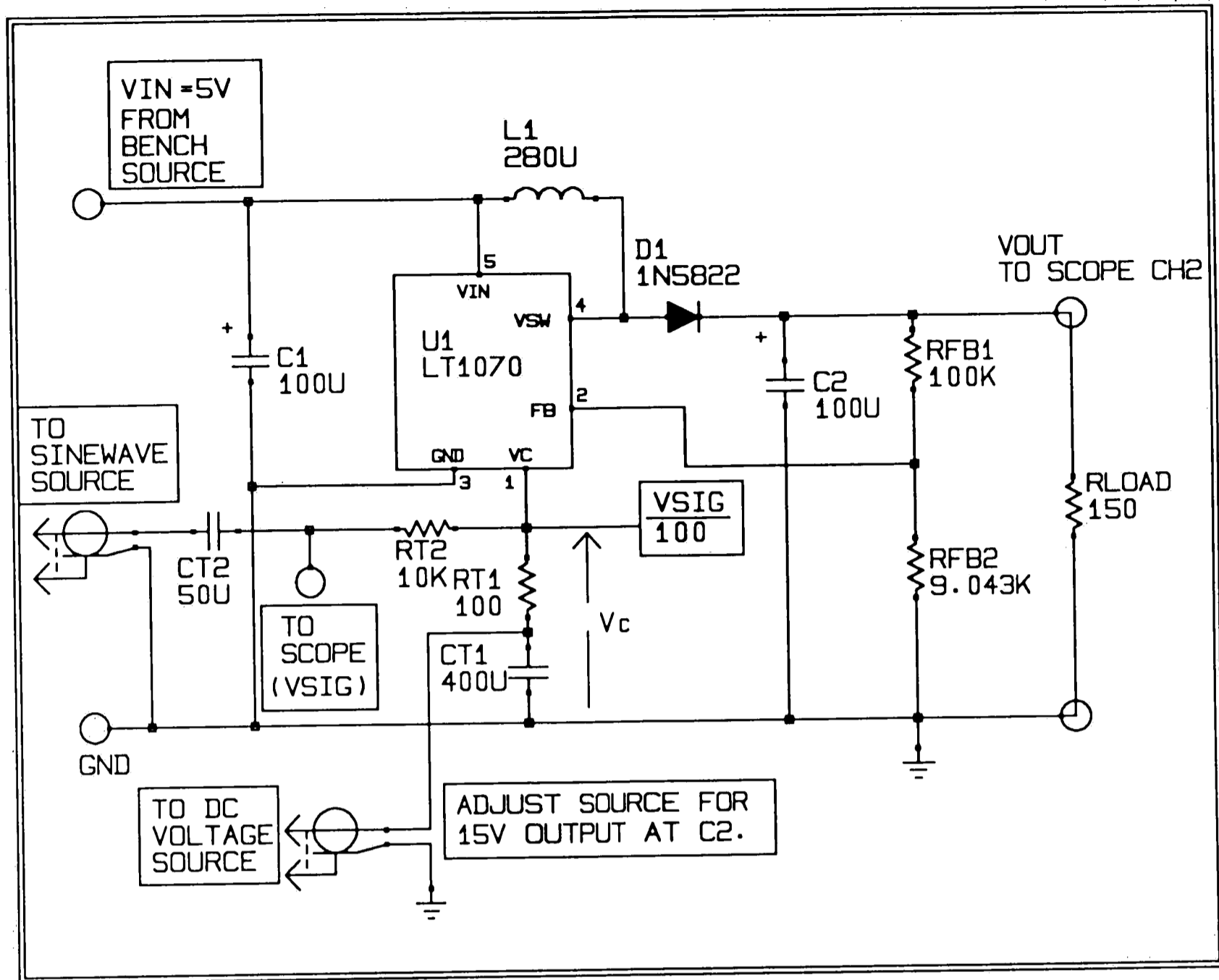
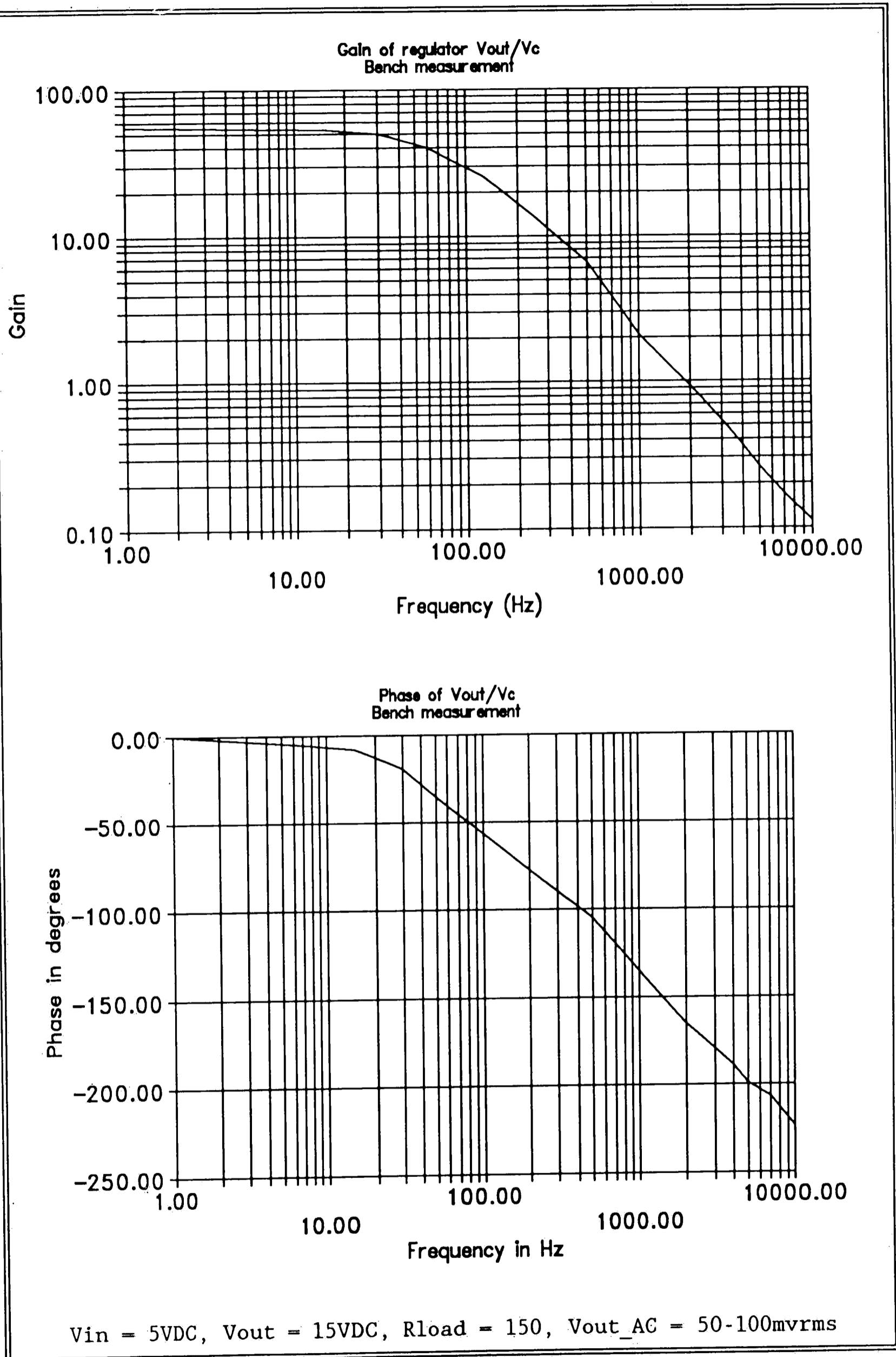Figure 69 - Phase and Gain Bench Test Circuit.

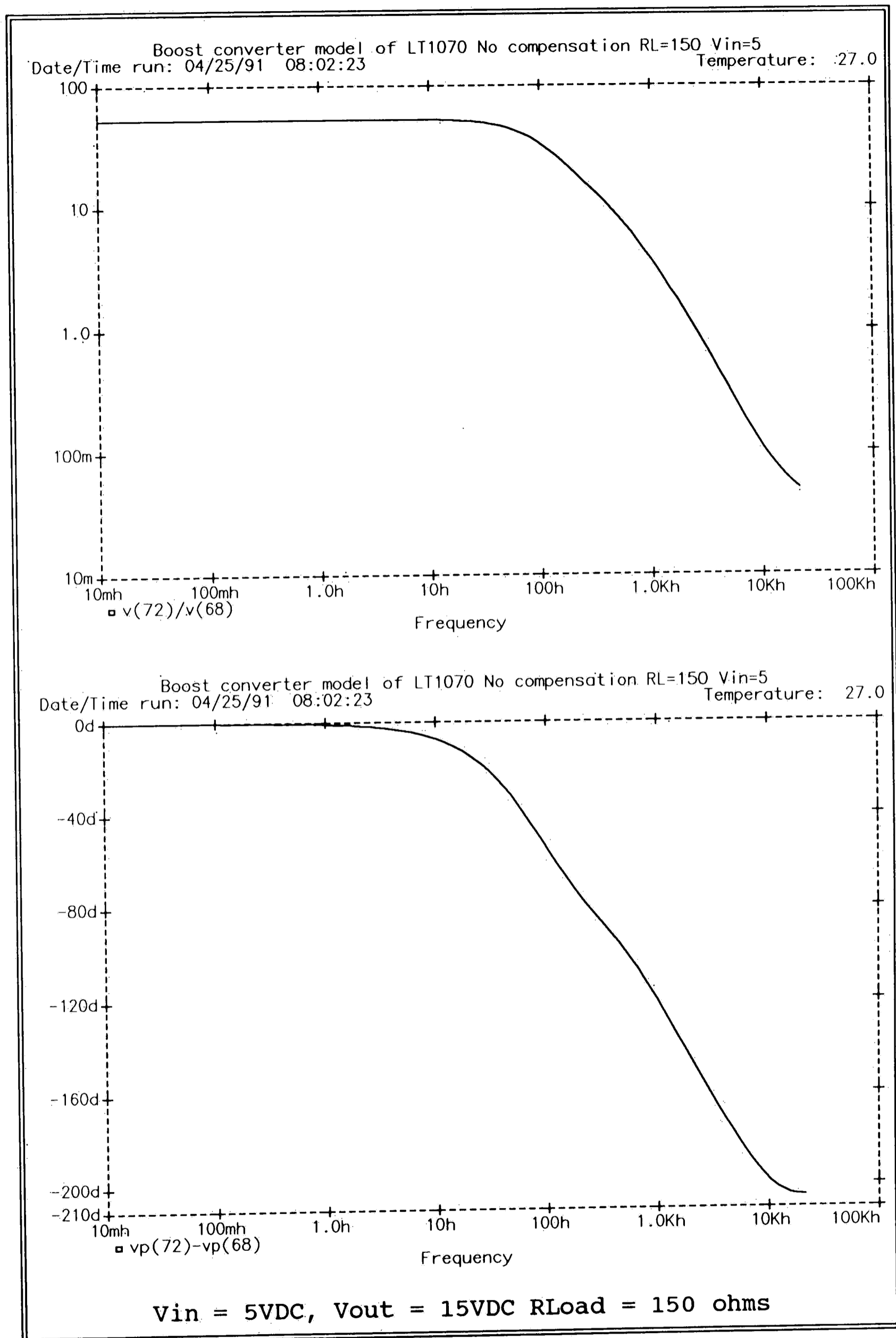Figure 70 - Measured Gain and Phase of Regulator for V_c to V_{out}.

Figure 71 - Simulated Gain and Phase of Regulator for V_c to V_{out}.

Conclusion

We have discussed basic converter topologies and their large and small signal behavior. Large signal analysis was used to gain an understanding of the basic operation of each converter type. State space averaging and linearization was introduced as a method of predicting small signal behavior of the circuit. Because of the laborious tasks required to use state space averaging and linearization, an average topology model was introduced using the concepts demonstrated by state space averaging. This non-linear model was linearized through the use of Pspice non-linear dependent sources. The Pspice average model was verified using a sample design of a current mode converter. It was found that the average model performs well as a design tool but tends to predict a phase shift less than reality.

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Vita

The author was born October 24, 1960 in Orange, New Jersey to Virginia A. Lebo, and James B. Lebo. At the Age of four he moved to LongIsland New York where he resided until 1983. He attended Lehigh University from August, 1979 to May, 1983 where he obtained a Bachelors of Science in Electrical Engineering. After graduating from Lehigh University, he became employed by AT&T Microelectronics in Reading, PA designing test systems and test applications for production testing of bipolar integrated circuits. In 1988 he was married to Ruth A. Klischer. He and his wife live in Birdsboro PA. While working at AT&T he pursued a Masters of Science in Electrical Engineering from Lehigh University for which this paper is a part of.