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THE DESIGN OF A 70 MHZ DIGITALLY CONTROLLED GAIN AMPLIFIER AND QUADRATURE DEMODULATOR FOR THE GSM EUROPEAN DIGITAL CELLULAR SYSTEM

by

Scott Leonard Forgues

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Approval

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Professor in Charge

CSEE Department Chairman

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Most importantly, a special thanks goes to my parents, Gerald and Mignonne Forgues. For without their support and encouragement, my many years of academic pursuits would not be possible.

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1. Abstract

The design of a 70 MHz Digitally Controlled Gain Amplifier and Quadrature Demodulator for the GSM European Digital Cellular System is described. This integrated circuit is used in the receive path for mobile terminals that comply with the GSM European Digital Cellular Standard.

The circuit provides digitally controlled amplification of a Gaussian-filtered Minimum Shift Keying (GMSK) modulated signal at an intermediate frequency of 70 MHz. The digitally controlled gain has a range of 0 to 45 dB as selected in 3 dB steps by four gain select signals. The gain error for any setting is less than ±3 dB over temperature and processing variations.

The circuit also provides GMSK demodulation by mixing two local oscillator signals that are 90° out of phase from each other with the amplified IF GMSK signal. The mixing is performed by two double balanced mixers that use Gilbert cell multipliers. The 90° out of phase local oscillator signals are derived from an external local oscillator of frequency equal to the IF frequency. An RC phase shifter with limiting amplifiers provides two 90° out of phase square wave outputs to drive the In-phase and Quadrature mixers.

A digitally controlled bandgap provides stable reference voltages and currents. The bandgap has a sleep mode that is enabled by a TTL compatible input. In the sleep mode, the entire circuit is turned off and draws less than 50 μA of supply current.

The integrated circuit is fabricated in AT&T's High Frequency Complementary Bipolar Integrated Circuit (CBIC-U) process on the ALA202 linear array. This 100 mW circuit requires a single +5 Volt power supply and has a chip area of 12.2 mm^2. The circuit is packaged in a 16 pin Small Outline Gull Wing (SOG) package and has 13 active pins.

The manufactured circuit has been tested for DC, gain and phase, noise, and switching speed characteristics. An analysis of the measured characteristics is presented. In addition, improvements are suggested and conclusions about the design and its performance are made.

2. Introduction

The Groupe Speciale Mobile (GSM) Digital Cellular Telephone System is a standard that has been developed for use by member countries of the European Economic Community as a common standard for digital cellular communications throughout Europe. The standard defines a system that will use Gaussian-filtered Minimum Shift Keying (GMSK) as a means of modulating the radio frequency (RF) signal that is transmitted and received between mobile terminals and base stations that are connected to the public telephone network.

This work presents the design and experimental results of an integrated circuit for mobile terminals that will amplify and demodulate a received GMSK signal that has been down-converted to an intermediate frequency (IF) of 70 MHz.

2.1 The GSM Digital Cellular Telephone System

The GSM Digital Cellular System uses RF transmit and receive frequencies in the 900 MHz to 1 GHz range [1]. The RF signal is modulated with 124 GMSK channels each separated by 200 kHz [1] within the RF band. In a mobile terminal, an RF circuit is used to down-convert one of the 124 channels that is received in the 935 MHz to 960 MHz [1] mobile receive band to an IF frequency of 70 MHz. The circuit described provides amplification and demodulation of the 70 MHz GMSK modulated IF signal. The demodulated signal is then filtered and processed by an external circuit so as to provide a data stream to a series of digital signal processors, microprocessors, and digital to analog converters.

A “ping-pong” receive/transmit approach for each multi-channel station is used, whereby the receiver and transmitter are alternately switched on for short bursts. The burst-mode operation presupposes a new approach to AGC which requires digital gain control. In a conventional radio system, the desired analog control voltage is stored on a capacitor. In GSM, it is stored in memory by a microprocessor so the receiver may start each burst of a series at the correct gain level. The gain is changed between bursts to avoid

the "clicks" of digital AGC. As required by the GSM system, digital control provides the ability to measure the absolute level of the received RF signal. The accuracy is limited by the tolerance of the gain, which is allocated to be ±3 dB for the IF amplifier/demodulator portion of the receiver path [2]. A hybrid analog / digital AGC may also be used as a gain control [12], but this approach requires the use of costly analog-to-digital converters so that the microprocessor may obtain data concerning the input signal level.

2.2 GSM Requirements for the IF Amplifier and Demodulator

The GSM system requirements together with the requirements of several mobile terminal manufacturers were used to determine some specifications and design constraints for the IF amplifier and demodulator. The following sections describe these issues with respect to the design.

2.2.1 Power Level Detection

The GSM specification requires that the received RF signal power level should be known to the microprocessors [3]. The method of power level detection is not described in the system requirements and is subject to the discretion of the mobile terminal manufacturer. The method that is used, when the circuit described is utilized in the signal path, is digital gain control. By maintaining a constant output level after demodulation by microprocessor control, the RF input level may be calculated by the microprocessor by software control. This is done by programming the microprocessor with the specified power level gains and losses through all stages that precede demodulation except for the digitally controlled IF amplifier. The input level may then be calculated using the programmed gains and losses, the value of the demodulated output power level, and the microprocessor controlled IF amplifier gain that is required to maintain the desired output power level.

2.2.2 Required Gain

The digitally controlled gain IF amplifier has a required maximum gain of 45 dB and a required minimum gain of 0 dB. The GMSK demodulator stage has a 6 dB conversion gain requirement. Through both the IF amplifier and the

GMSK demodulator, the total conversion gain error must be less than ±3 dB from the defined total conversion gain of 51 dB [3].

2.2.3 Noise Figure Requirements

The noise figure of the circuit must be as low as possible since this circuit is intended to amplify relatively low level signals that are only minimally amplified in the RF to IF down conversion stage. Since the circuit has a range of gain levels, the highest level of gain requires the lowest noise figure, while the lowest level of gain only does not require as low a noise figure. The design goal for this circuit is to have a noise figure of less than 10 dB for its highest gain setting and a maximum noise figure of 30 dB for the lowest gain setting.

2.2.4 Power Consumption

Since the described circuit is intended for use in a mobile terminal, the total power consumption must be kept as low as possible. This is to avoid an excessive power drain on the battery powered mobile terminals. A goal of less than 100 mW is desired with a nominal single supply voltage of +5 Volts. In addition, during the mobile transmit cycle of communication with the base station, the receive path must be able to be turned off by digital control. When the receive path is turned off, this is known as the sleep mode. The circuit described must be capable of drawing less than 50 μA during the sleep mode and the settling time when switching between modes should be less than 25 μs.

2.2.5 Input and Output Definition

The input to the IF amplifiers should be single-ended with an input impedance of greater than 300 Ω. The local oscillator (LO) input to the GMSK demodulator should also be single-ended with an input impedance of greater than 300 Ω.

Following the GMSK demodulation, the circuit should have In-phase (I) and Quadrature (Q) differential outputs. Each output should have a single ended

output impedance of 50 Ω or less and be capable of a baseband frequency range of DC to 1 MHz. Also, the output stage must be capable of driving a 1 Vpp differential signal with a 1 kΩ resistive load in parallel with a 30 pF capacitive load on each output.

2.2.6 GMSK Demodulator Requirements

GMSK demodulation is implemented by mixing the IF signal from the IF amplifier with two local oscillator (LO) signals that are equal in frequency to the IF signal, but phase shifted 90° with respect to each other. The local oscillator should be such that a +45° phase shifted LO signal is mixed with the IF signal in the I channel mixer and a -45° phase shifted LO signal is mixed with the IF signal in the Q channel mixer. The phase shifter requires an error of ±3° with respect to the 90° I and Q phase shift requirement.

2.2.7 Temperature and Supply Requirements

The IF amplifier and demodulator should meet all specifications for an ambient temperature range of -25 °C to +85 °C with a positive supply voltage range of +4.75 Volts to +5.25 Volts.

2.3 Circuit Implementation

Considering the requirements of section 2.2, AT&T's High Frequency Complementary Bipolar Integrated Circuit technology (CBIC-U) is suitable for the implementation of the circuit. The CBIC-U technology has an NPN transistor f_T of 4.0 GHz and a PNP transistor f_T of 2.5 GHz. The AT&T ALA202 linear array was used to fabricate the circuit. This enables a fast design turn around time with minimal cost of manufacture. With a design at this frequency, some gain penalties are paid due to increased layout parasitics in the array, but they may be accounted for in the design of the gain stages.

The circuit's block diagram is shown in figure 2.1. Note that the digitally controlled amplifier provides the desired 0 - 45 dB gain is 3 dB steps while the I and Q mixers with the phase shifter provide the GMSK demodulation.

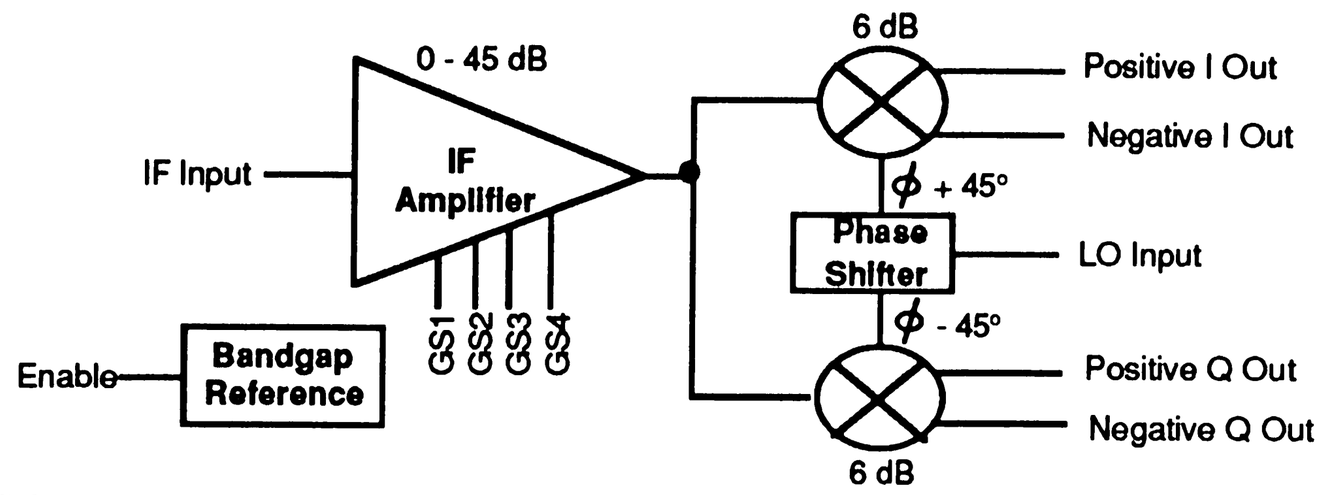

Figure 2.1: IF Amplifier and Demodulator Block Diagram

2.4 IF Amplifier Definition

The IF amplifier subcircuit is comprised of multiple digitally controlled gain amplifiers. To obtain the required 45 dB of gain switchable in 3 dB steps, the amplifiers are partitioned such that the gain steps may be selected with a N-bit binary word. To obtain a 3 dB resolution of gain steps over the range of 0 dB to 45 dB, N = 16 gain steps are needed. Therefore, four binary Gain Select control signals are required. The gain select truth table, shown in Table 2.1, shows the bit patterns that should be applied to the four Gain Select inputs to obtain the corresponding gain through the IF amplifier subcircuit. It is evident from Table 2.1 that the four amplifiers should be selected to provide switchable gains of 24 dB / 0 dB, 12 dB /0 dB, 6 dB / 0 dB, and 3 dB / 0 dB.

The selection of the circuit topology for the digitally controlled gain amplifiers is dictated by three main considerations. First, the total gain error through the chain of amplifiers and through the mixer stages must be less than ±3 dB regardless of the selected gain. Second, the number of available transistors for each amplifier must be kept to a minimum. This is required because the circuit is to be built on a linear array that has a limited number of transistors and resistors available. The last consideration is to minimize the allocated current consumption for the IF amplifier.

GS1	GS2	GS3	GS4	Gain
H	H	H	H	0 dB
H	H	H	L	3 dB
H	H	L	H	6 dB
H	H	L	L	9 dB
H	L	H	H	12 dB
H	L	H	L	15 dB
H	L	L	H	18 dB
H	L	L	L	21 dB
L	H	H	H	24 dB
L	H	H	L	27 dB
L	H	L	H	30 dB
L	H	L	L	33 dB
L	L	H	H	36 dB
L	L	H	L	39 dB
L	L	L	H	42 dB
L	L	L	L	45 dB

Table 2.1: Gain Select Truth Table

2.4.1 Gain Error Allocation

The gain error specification may be defined by allocating a fraction of the gain error to each of the gain stages. The simplest allocation is to divide the total required gain error by the number of stages in the signal path. Therefore, with a total required gain error of ±3 dB through four gain stages and a mixer, the gain error for each stage is allocated to be ±0.6 dB.

2.4.2 Linear Array Limitations

The AT&T ALA202 linear array consists of 9 "standard" tiles, 2 "power" tiles, and 1 "input" tile each containing a number of NPNs, PNPs, and resistors. Table 2.2 shows the component totals per tile for the ALA202 [4].

Component	Type	Standard	Input	Power
Transistors				
NPN	1/3X	-	2	-
NPN	1X	9	7	2
NPN	2X	2	2	2
NPN	5X	1	1	2
NPN	15X	-	-	2
PNP	1/3X	-	2	-
PNP	1X	5	3	2
PNP	2X	2	2	2
PNP	5X	-	-	2
PNP	15X	-	-	2
50 Ω/sq Resistors	50 Ω	8	8	-
	100 Ω	40	40	40
	200 Ω	8	8	-
1 kΩ/sq Resistors	1 kΩ	4	4	-
	2 kΩ	20	20	20
	4 kΩ	4	4	-
Capacitors	0.75 to 3.35 pF	1	1	-
	1.0 pF	2	2	-

Table 2.2: AT&T ALA202 Linear Array Component Totals

The design of each gain stage in the IF amplifier should be constrained to the components available to a single "standard" tile so as to minimize interconnect capacitance within each amplifier and for ease of layout, since

each amplifier will have similar topologies. The detailed design of the IF amplifier and each of its stages will be discussed in section 3.

2.5 Double Balanced Mixer and Output Stage Subcircuit Definition

The I and Q Double Balanced Mixers of the GMSK demodulation stage is required to have a conversion gain of 6 dB with a gain error of ±0.6 dB. In addition, the mixers should be capable of handling a 0.5 Vpp differential input and providing a 1 Vpp output without distortion. The output must have a 50 Ω output impedance and be able to drive a 1 kΩ load in parallel with 30 pF.

A Gilbert cell multiplier is well suited to the implementation of the demodulation and gain requirements of the GMSK demodulator since it provides for phase detection through alternate +1 and -1 switching. In addition, a push-pull output stage is also suitable to meet the load and output impedance requirements that have been stated. Figure 2.2 shows the block diagram of the mixer and output stages. In section 4, the mixer and output circuits will be discussed in more detail.

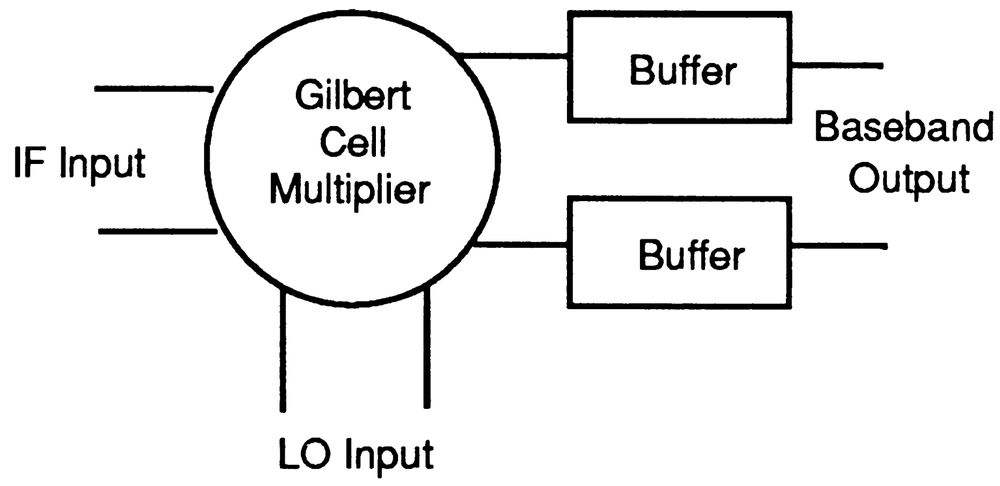

Figure 2.2: Mixer and Output Stage Block Diagram

2.6 Quadrature Phase Shifter Subcircuit Definition

The quadrature phase shifter, as part of the GMSK demodulator, is required to provide two 70 MHz local oscillator signals to the I and Q mixers, each of which are to be 90°±3° apart in phase. Given an externally provided LO signal, the circuit should provide the two signals such that they are phase shifted +45° and -45° from the external 70 MHz LO signal. To assure a

minimum mixer output gain error between channels, the outputs should be large enough so as to fully switch each of the mixer's LO inputs. Also, the minimum LO input level to the phase shifter should be approximately 100 mVpp. The block diagram of figure 2.3 shows the configuration needed to provide the desired phase shift while insuring full switching of the mixers.

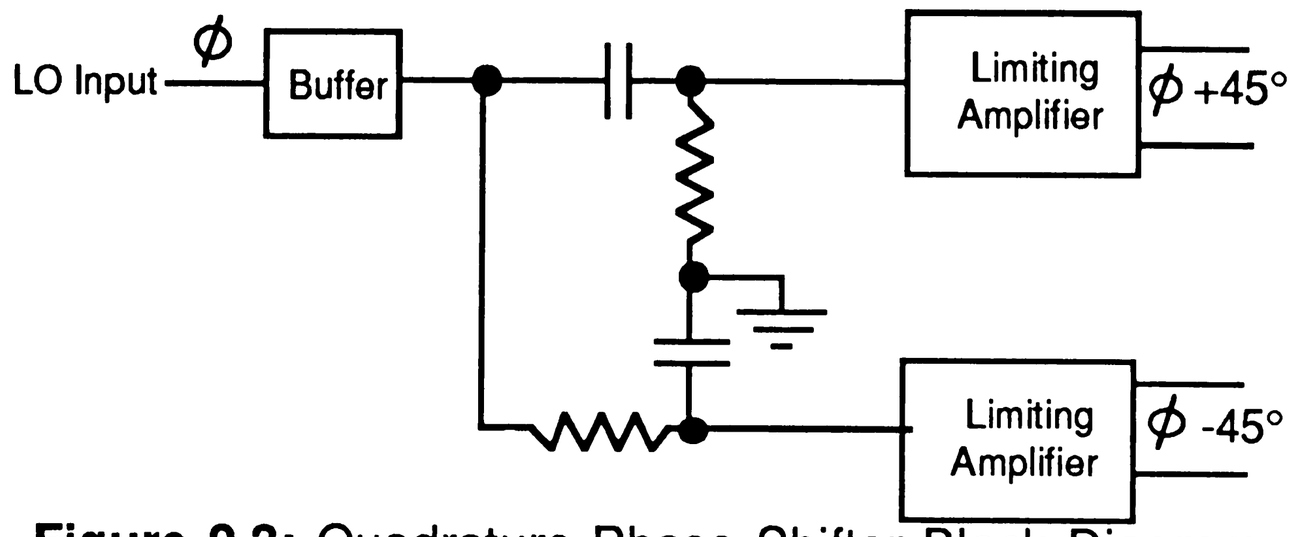

Figure 2.3: Quadrature Phase Shifter Block Diagram

The buffer provides the desired input impedance, while the RC network provides the two +45° and -45° phase shifter outputs. The RC network drives two limiting amplifiers that provide two equal, but 90° out of phase, square wave outputs to the I and Q mixers. Section 5 will present the design of the quadrature phase shifter.

2.7 Digitally Controlled Bandgap Reference Subcircuit Definition.

The digitally controlled bandgap must be able to provide stable voltage references so as to set up current mirrors and reference levels throughout the circuit. In addition, the bandgap must have the capability to be turned off by digital control such that all subcircuits that are drawing current will be turned off. Section 6 will discuss the design of the digitally controlled bandgap and the current mirrors it sets up.

3. Digitally Controlled Gain IF Amplifier

The Digitally Controlled Gain IF Amplifier consists of four Digitally Controlled Gain Differential Amplifiers (DCGDA). Each DCGDA has three distinct sections. First, two levels of amplification are provided by a Dual Gain State Differential Amplifier (DGSDA) whose gain is dependent upon the selection of tail current sources. Second, the selection of tail current sources is controlled by a Digitally Controlled Current Switch (DCCS). Lastly, the differential amplifier is buffered by a pair of emitter followers. Figure 3.1 shows a block diagram of the DCGDA subcircuit.

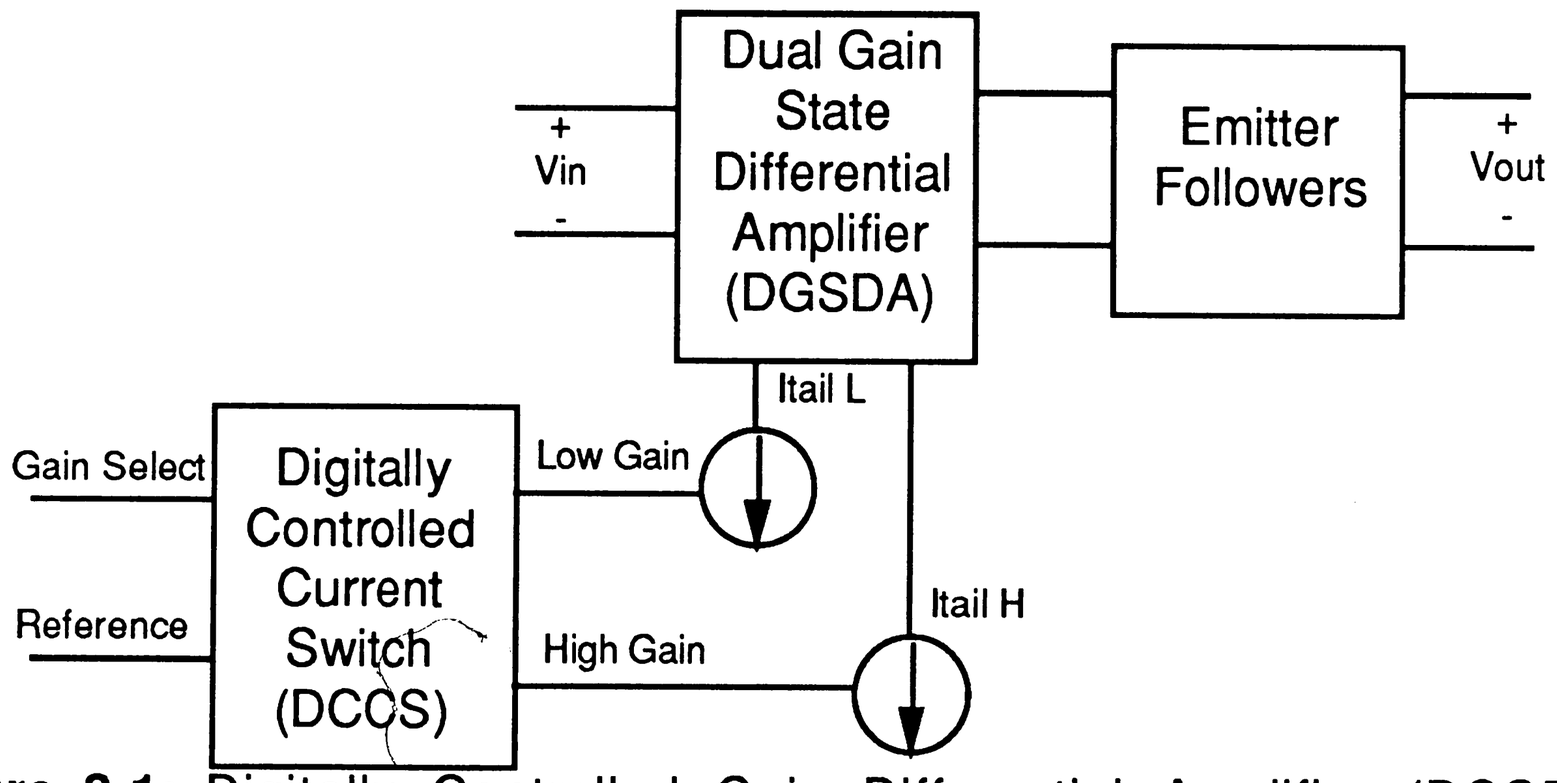

Figure 3.1: Digitally Controlled Gain Differential Amplifier (DCGDA) Subcircuit

The following sections describe the operation and design of the previously described subcircuits. In addition, issues such as gain error due to temperature and processing variations will also be discussed. Also, an example calculation for the important parameters of s DCGDA subcircuit will be presented. The chapter will conclude with a comparison of the calculated and simulated gains and gain errors.

3.1 Dual Gain State Differential Amplifier (DGSDA) Design

The Dual Gain State Differential Amplifier is, in effect, an emitter-coupled pair with emitter degeneration. This type of differential amplifier has a

voltage gain that is determined roughly by the formula [5] as found in equation 3.1.

$$A_v = \frac{R_c}{\frac{1}{g_m} + R_e} \qquad \text{(Eq. 3.1)}$$

To facilitate the required selection of two separate voltage gains in the DGSDA, R_e may be changed while $\frac{1}{g_m}$ and R_c is held constant. This is accomplished by splitting the emitters of the input transistors in the emitter-coupled pair and connecting two sets of emitter degeneration resistors to the split emitters. Switching between the two sets of R_e may be achieved by selecting either $I_{tail\ L}$ or $I_{tail\ H}$, each of which drive separate sets of emitter resistors. The Digitally Controlled Current Switch, to be described in section 3.2, performs the selection. The DGSDA is shown in figure 3.2.

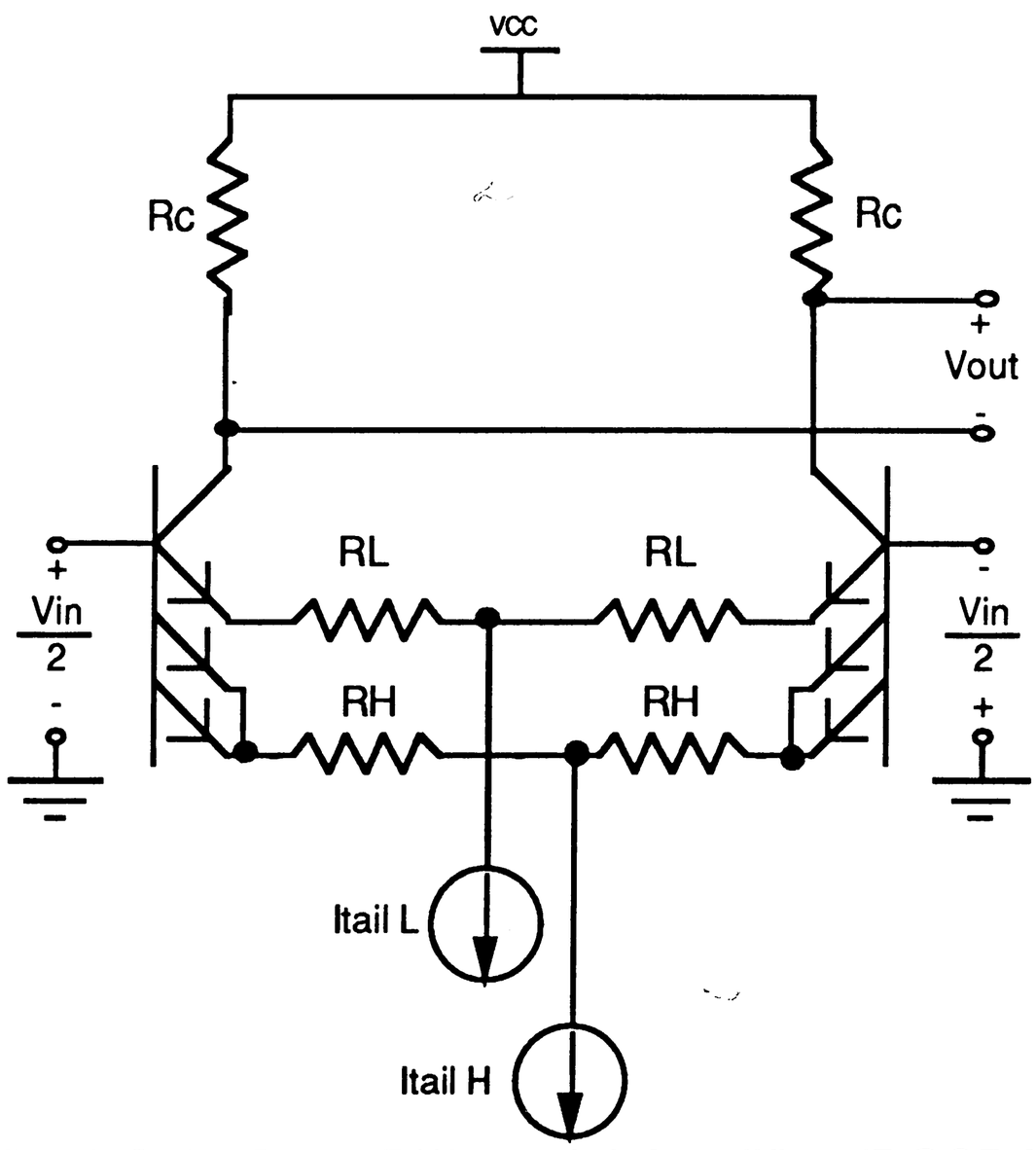

Figure 3.2: Dual Gain State Differential Amplifier (DGSDA) Subcircuit

In the DGSDA configuration, the differential amplifier acts as two separate emitter coupled pairs with a common collector, a common base, and a common load between them. A benefit of the common collector and common

load is the sharing of collector to substrate capacitance, layout parasitics, and resistor parasitic capacitance. This causes the overall capacitance to be lower at the collector. Therefore, the gain will roll off at a higher frequency due to a lower RC time constant. In addition, the sharing of transistors eliminates two devices from the transistor count. This is an important consideration when designing with a linear array.

3.1.1 Calculation of Gain, Input Impedance, and Output Impedance

Since the DGSDA may be considered as two separate emitter coupled pairs with emitter degeneration, the design equations may be found based on this property. The following will show how the design equations that primarily effect the performance of the circuit were found. They are the high frequency small-signal gain, the input impedance, and the output impedance.

The small-signal gain equation as used in Eq. 3.1 is appropriate for low frequency and low gain differential amplifier designs. Since this design is intended to operate at an IF frequency of 70 MHz and the highest gain setting for a DGSDA is 24 dB, a more detailed gain equation should be used. Using the half-circuit concept [5, 6] to determine the gain, input impedance, and output impedance of an emitter-coupled pair with emitter degeneration, the small-signal equivalent circuit of figure 3.3 may be used.

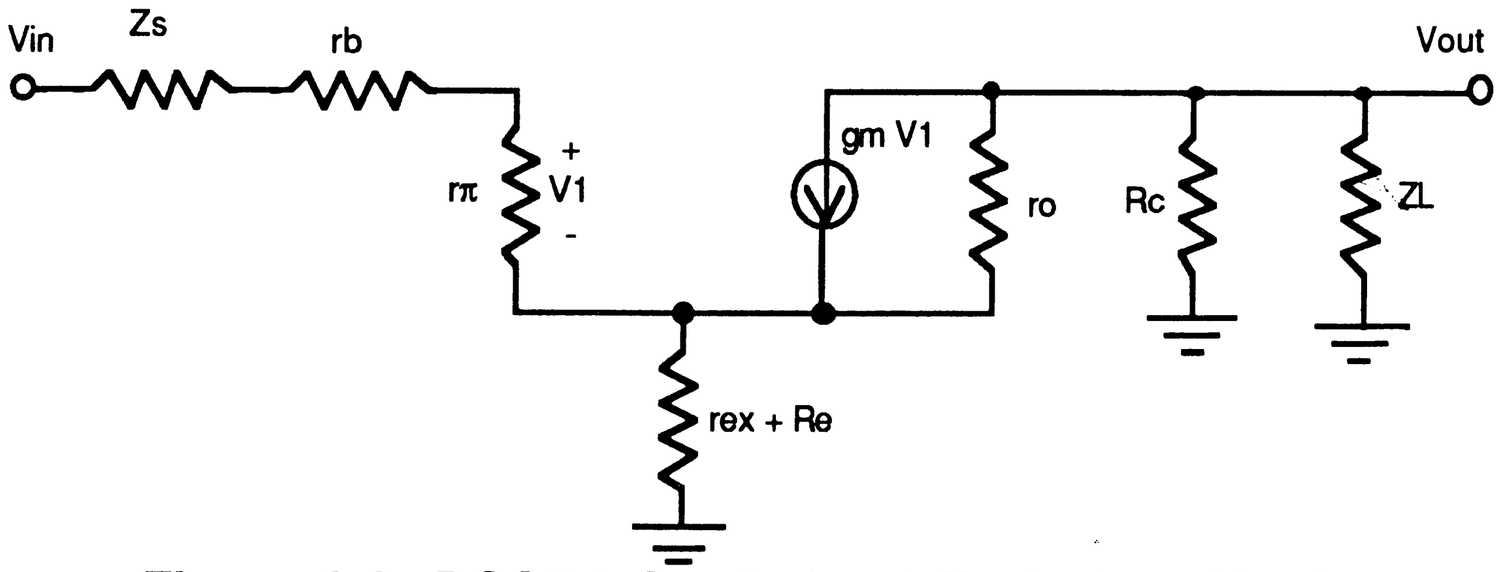

Figure 3.3: DGSDA Small-signal Equivalent Circuit

The small-signal equivalent circuit of figure 3.3 includes the source impedance, Z_s, as seen across one input of the emitter-coupled pair and the load impedance, Z_L, on each DGSDA output. The load impedance includes

the layout parasitic capacitance, the collector-to-base capacitance of the emitter follower, and the R_c resistor parasitic capacitance.

To simplify the design, a two-port equivalent circuit [6] may be found such as that shown in figure 3.4.

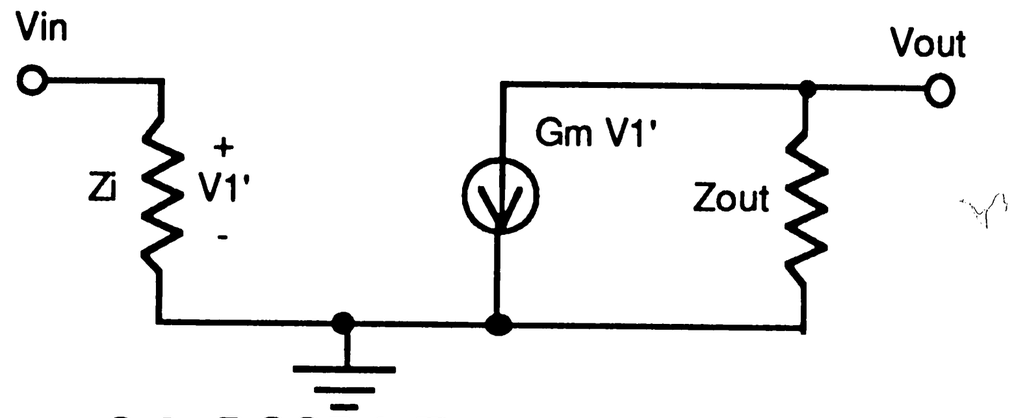

Figure 3.4: DGSDA Two-port Equivalent Circuit

Where $$Z_i = Z_s + r_b + r_\pi + (r_{ex} + R_e)(1 + \beta_o) \quad , \qquad \text{(Eq. 3.2)}$$

$$G_m \approx \frac{1}{\frac{Z_s + r_b + r_\pi}{\beta_o} + r_{ex} + R_e} \quad , \qquad \text{(Eq. 3.3)}$$

and $$Z_{out} = R_c \parallel Z_L \parallel r_o(g_m R_e + 1) \qquad \text{(Eq. 3.4)}$$

Since each DCGDA is preceded by a low source impedance, then Z_s may be neglected in equations 3.2 and 3.3. Also, r_b may be neglected since it is usually very small. Therefore, Equations 3.2 and 3.3 may be re-written as shown in equations 3.5 and 3.6, respectively.

$$Z_i \approx r_\pi + (r_{ex} + R_e)\beta_o \qquad \text{(Eq. 3.5)}$$

and $$G_m \approx \frac{1}{\frac{1}{g_m} + r_{ex} + R_e} \qquad \text{(Eq. 3.6)}$$

Furthermore, since $r_o(g_m R_e + 1)$ should be very large, then equation 3.4 may be approximated as shown in equation 3.7

$$Z_{out} \approx R_c \parallel Z_L \qquad \text{(Eq. 3.7)}$$

where Z_L includes C_{cs}, C_{layout}, C_{Rc}, and $C_{\mu ef}$.

Using the two-port equivalent circuit of figure 3.4, the differential input impedance [5] may be found directly from equation 3.8,

$$Z_{in} = 2\,Z_i \approx 2\left[r_\pi + (r_{ex} + R_e)\,\beta_o\right] \qquad \text{(Eq. 3.8)}$$

and the voltage gain may be found by equation 3.9.

$$A_v = G_m\,Z_{out} \approx \frac{R_c \parallel Z_L}{\frac{1}{g_m} + r_{ex} + R_e} \qquad \text{(Eq. 3.9)}$$

It is now evident that the gain, as determined by Equation 3.9, differs from Equation 3.1 by the addition of the parasitic capacitances of Z_L. This becomes significant at the 70 MHz frequency of operation.

3.1.2 Determination of Component Values and Tail Currents

To obtain a design for the DGSDA, the desired voltage gain (Eq. 3.9), the gain error requirement, and the output swing requirement may be used to find the desired values of R_c, R_e, and I_{tail}. This is accomplished by also keeping in mind the effects of the load capacitance, C_L, and the resistor tolerance, ε_R.

A portion of the gain error budget should be allocated so as to account for the gain rolloff error due to the R_cC_L time constant. Since the pole of the differential amplifier's transfer function is found at $f_{op}R_cC_L$, then the gain rolloff error may be found by equation 3.10.

$$\varepsilon_{AV_T} = 20 \log \sqrt{(f_{op}R_cC_L)^2 + 1} \qquad \text{(Eq. 3.10)}$$

The loading capacitance, C_L, consists of the collector to substrate capacitance (C_{cs}), the collector to base capacitance of the emitter follower ($C_{\mu ef}$), the estimated layout capacitance (C_{layout}), and the R_c resistor parasitic capacitance (C_{Rc}).

Using a rearranged equation 3.10, a nominal value for the collector resistor, R_c, may be found as shown in equation 3.11. The resistor tolerance, ε_R is used so as to insure that the maximum R_c will not cause the gain rolloff error to exceed its desired value.

$$R_c = \frac{\sqrt{10^{\frac{\varepsilon_{AV_T}}{10}} - 1}}{2\pi f_{op} C_L(1 + \varepsilon_R)} \qquad \text{(Eq. 3.11)}$$

To obtain the required output voltage swing, the value for I_{tail} may be found by using equation 3.12.

$$I_{tail} = \frac{V_{OUTmax\ p\text{-}p}}{(R_c)(1 + \varepsilon_R)} \qquad \text{(Eq. 3.12)}$$

Now, the gain setting resistor R_e may be found by rearranging equation 3.9 to that as shown in equation 3.13.

$$R_e = \frac{R_c \parallel Z_L}{A_v} - r_{ex} - \frac{1}{g_m} \qquad \text{(Eq. 3.13)}$$

The output and input impedances may then be calculated by using equations 3.7 and 3.8, respectively.

3.1.3 Errors Due to Temperature and Process Variations

Another important characteristic of the IF amplifier is it's requirement to maintain a relatively stable gain over variations of temperature and process parameters. Therefore, the following will address these issues as they effect the basic design equations.

To reduce temperature effects on the gain of the DGSDA, the tail currents should be proportional to temperature. This is evident when examining the approximate gain equation (Eq. 3.1). The equation shows that the gain is dependent on R_c, R_e, and g_m. One aspect of the gain equation's dependence on temperature is the inversely proportional to temperature

value of g_m. Since $g_m = \frac{I_c}{V_T}$ and $V_T = \frac{kT}{q}$, then it may be seen that for g_m to be independent of temperature, then I_c should be proportional to temperature. The temperature dependent current mirror, as described in section 6.3, provides the tail currents through the Digitally Controlled Current Switch so as to drive the DGSDA. Therefore, a major contributor to temperature dependent gain error is cancelled so that g_m is independent of temperature.

Examining the expanded gain equation of equation 3.9, it is apparent that variations in gain due to temperature are not solely due to changes in g_m Therefore, the variations with temperature for the remaining parameters should be considered. Since r_{ex} is small relative to $\frac{1}{g_m}$ and R_e, then the change with respect to temperature of the gain due to r_{ex} may be neglected. The effects of temperature on Z_L due to C_{cs}, C_{layout}, C_{Rc}, and $C_{\mu ef}$ may also be neglected since the temperature dependency of these capacitances is small. The remaining parameters in equation 3.9 are R_c and R_e. Since these two resistors are designed such that they are of the same type, the values should approximately track. Using equation 3.14, the temperature coefficient of A_v may be found.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx \left[\left(\frac{R_c \parallel Z_L}{R_c}\right)^2 - \frac{R_e}{\frac{1}{g_m} + r_{ex} + R_e}\right]\frac{1}{R}\frac{\partial R}{\partial T} \qquad \text{(Eq.3.14)}$$

Another major contributor to gain error is the error caused by the resistor tracking errors between R_c and R_e. This gain error maybe found by using equation 3.15.

$$\varepsilon_{AV_R} \approx 20 \log\left[1 + \frac{1}{2}\left(1 + A_{Vo}\frac{R_{eo}}{R_{co}}\right)\varepsilon_{Rtrack}\right] \qquad \text{(Eq.3.15)}$$

3.1.4 Example Calculation for the 24 / 0 dB DGSDA

As an example, the R_c, I_{tail}, and R_e may be found for the 24 / 0 dB gain stage. Using these parameters, the gain errors due to temperature and process variations may also be calculated.

For the 0 dB gain setting, a maximum output level of at least 0.5 Vpp is required with a total gain error ($\mathcal{E}_{AV}$) of ±0.6 dB. First, the load capacitance should be estimated. Therefore, the C_{cs} is approximately 0.20 pF, while the $C_{\mu ef}$ of the emitter follower may be estimated to be 0.15 pF. The C_{layout} and the C_{Rc} is approximately 0.15 pF and 0.1 pF, respectively. Therefore, the total estimated loading capacitance, C_L, is 0.60 pF. Thus, with a resistor tolerance of 20% and an allocated rolloff gain error of ±0.3 dB then equation 3.11 may be used to calculate R_c as found in equation 3.16.

$$R_c = \frac{\sqrt{10^{\frac{0.3\ dB}{10}} - 1}}{2\pi(70MHz)(0.60\ pF)(1 + 0.2)} = 845\ \Omega \qquad \text{(Eq.3.16)}$$

Now, I_{tail} may be found with equation 3.12 as shown in equation 3.17 with an output swing of 0.5 Vpp.

$$I_{tail} = \frac{0.5\ Vpp}{(845\ \Omega)(1 - 0.2)} = 740\ \mu A \qquad \text{(Eq. 3.17)}$$

and with equation 3.13, R_e may be calculated to be the value as found in equation 3.18.

$$R_e = \frac{\dfrac{1}{\sqrt{\left(\frac{1}{845\ \Omega}\right)^2 + \left(2\pi(70MHz)(0.60pF)\right)^2}}}{1} - 1\ \Omega - \frac{26\ mV}{\frac{740\ \mu A}{2}} = 753\ \Omega \qquad \text{(Eq. 3.18)}$$

When in the high gain state, 24 dB of gain is required. Since R_c is shared then the previously calculated value must be used. Due to the high gain of this setting, it is obvious that a small R_e will result. To decrease the dependence of gain on g_m, a larger tail current should be selected so that the $\frac{1}{g_m}$ term in the gain equation (Eq. 3.6) may be smaller Therefore, I_{tail} may be selected to be 2 mA so as to decrease $\frac{1}{g_m}$. Any more current would be too much considering the constraints of the power budget. Thus, the only

remaining parameter to be calculated is R_e. Using equation 3.13 R_e is found in equation 3.19.

$$R_e = \frac{\dfrac{1}{\sqrt{\left(\dfrac{1}{845\ \Omega}\right)^2+\left(2\pi(70\text{MHz})(0.60\ \text{pF})\right)^2}}}{15.85} - 1\ \Omega - \frac{26\ \text{mV}}{\frac{2\ \text{mA}}{2}} = 25\ \Omega \quad \text{(Eq. 3.19)}$$

Now, Z_{in} and Z_{out} may be found from equations 3.7 and 3.8, as calculated in equations 3.20 and 3.21, respectively.

$$Z_{out} = R_c \,||\, Z_L = \frac{1}{\sqrt{\left(\dfrac{1}{845\ \Omega}\right)^2+\left(2\pi(70\text{MHz})(0.60\text{pF})\right)^2}} \cong 825\ \Omega \quad \text{(Eq. 3.20)}$$

$$Z_{in} = 2\,Z_i \approx 2\left[\frac{57}{\frac{2\ \text{mA}}{2(26\text{mV})}} + (1\ \Omega + 25\ \Omega)57\right] = 5928\ \Omega \quad \text{(Eq. 3.21)}$$

Where Z_{in} is the minimum value as found in the high gain state and β_o is found by equation 3.21.

$$\beta_o = \frac{f_T}{f_{op}} = \frac{4.0\ \text{GHz}}{70\ \text{MHz}} = 57 \qquad \text{(Eq.3.21)}$$

where f_T is found from the AT&T ALA202 Data Sheet [4].

The errors due to temperature and resistor tracking errors may now be calculated. Using a temperature coefficient of 1300 ppm/°C [4] for 50 Ω/sq. implanted boron resistors in equation 3.14, the gain temperature coefficient for the low gain state is found to be that as calculated in equation 3.23,

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx \left[\left(\frac{825\ \Omega}{845\ \Omega}\right)^2 - \frac{753\ \Omega}{\frac{26\ \text{mV}}{370\ \mu\text{A}} + 1\ \Omega + 753\ \Omega}\right] 1300\ \frac{\text{ppm}}{\text{°C}} = 52\ \frac{\text{ppm}}{\text{°C}} \quad \text{(Eq.3.23)}$$

while, for the high gain state, the gain temperature coefficient is found by equation 3.24.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx \left[\left(\frac{825\ \Omega}{845\ \Omega}\right)^2 - \frac{25\ \Omega}{\frac{26\ mV}{1\ mA} + 1\ \Omega + 25\ \Omega}\right] 1300\ \frac{ppm}{°C} = 614\ \frac{ppm}{°C} \text{(Eq.3.24)}$$

Therefore, with a maximum temperature swing of ±60 °C from the nominal temperature, the maximum change in gain for the 0 dB and the 24 dB settings would be the changes as found by equations 3.25 and 3.26, respectively.

$$\varepsilon_{AV_T} = 20 \log\left[1 + \frac{(\pm 60\ °C)(52\ ppm/°C)}{10^6}\right] = \pm 0.027\ dB \text{ (Eq.3.25)}$$

$$\varepsilon_{AV_T} = 20 \log\left[1 + \frac{(\pm 60\ °C)(614\ ppm/°C)}{10^6}\right] = \pm 0.314\ dB \text{ (Eq.3.26)}$$

The gain error due to resistor tracking errors may be found with equation 3.15 using a resistor tracking error of approximately 1% [4]. The maximum error with the low gain selected is as found in equation 3.27,

$$\varepsilon_{AV_R} \approx 20 \log\left[1 + \frac{1}{2}\left(1 + 1\ \frac{753\ \Omega}{845\ \Omega}\right) 0.01\right] = \pm 0.082\ dB \text{(Eq.3.27)}$$

and for the high gain selected the maximum error is as found in equation 3.28.

$$\varepsilon_{AV_R} \approx 20 \log\left[1 + \frac{1}{2}\left(1 + 15.85\ \frac{25\ \Omega}{845\ \Omega}\right) 0.01\right] = \pm 0.064\ dB \text{ (Eq.3.28)}$$

The cumulative gain error is the sum of the errors due to the allocated rolloff error of -0.3 dB, the error due to temperature, and the error due to resistor tracking. This results in a total gain error of ±0.409 dB for the 0 dB gain setting and ±0.678 dB for the 24 dB setting. It is now evident that the upper limit for the total gain error occurs when the high gain mode is selected. The results for the 24 dB setting are found to be slightly outside the target value range of ±0.6 dB gain error. This shouldn't be a problem because the following three gain stages of the Digitally Controlled Gain IF Amplifier have maximum gains of 12 dB, 6 dB, and 3 dB. Each of these gain stages should

have a smaller maximum gain error such that the total gain error through the IF amplifier will result in the target of ±3 dB. Of course, the emitter follower stage will also contribute some gain error. Section 3.4 will show the total gain error through all four stages.

3.2 Digitally Controlled Current Switch (DCCS) Design

The operation of the Dual Gain State Differential Amplifier is dependent upon the circuitry that controls the selection of tail currents. This section will discuss the operation of the circuit that performs this task. The Digitally Controlled Current Switch (DCCS) subcircuit is shown in figure 3.5

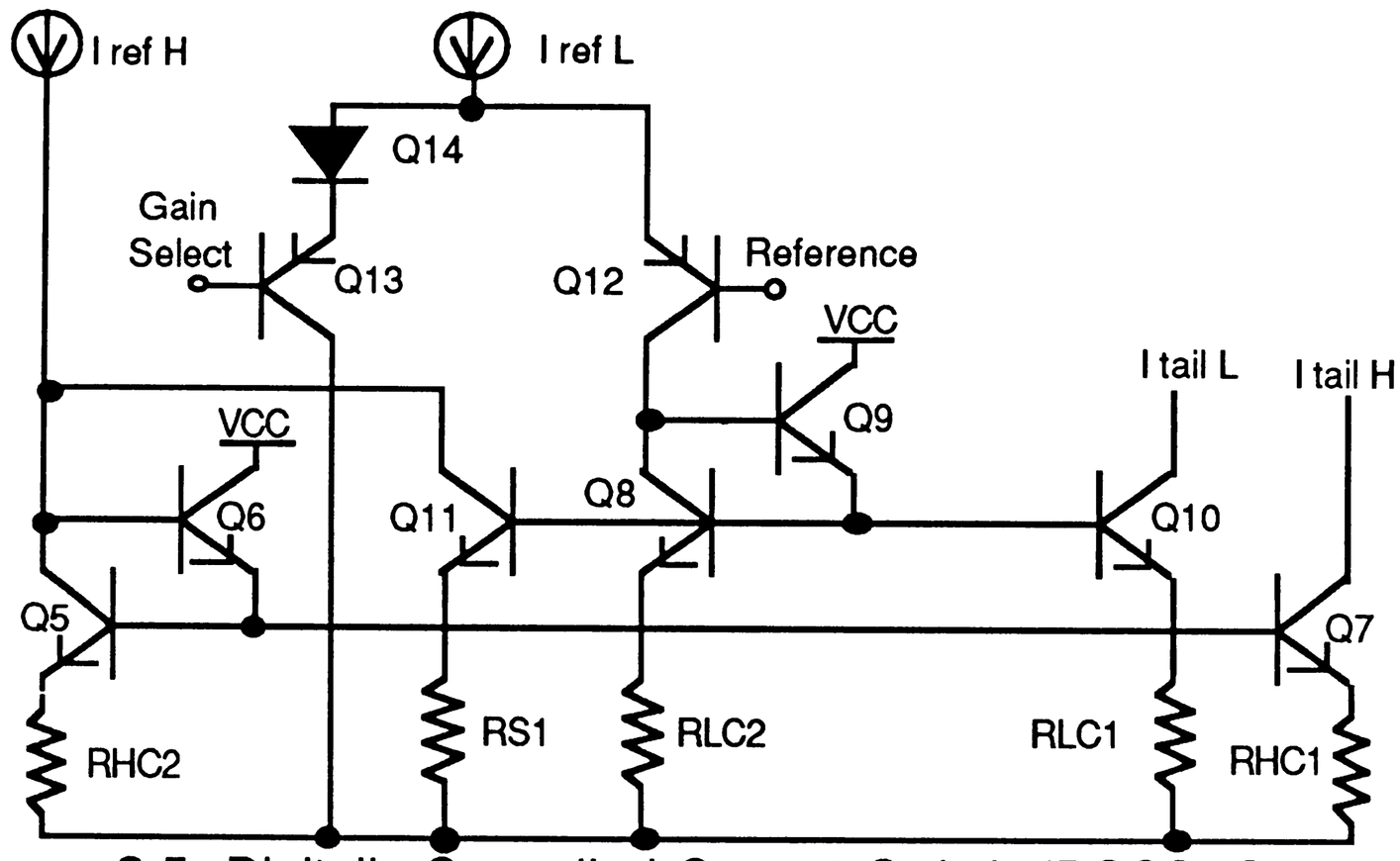

Figure 3.5: Digitally Controlled Current Switch (DCCS) Subcircuit

3.2.1 Digitally Controlled Current Switch Operation

Depending upon the state of the DCCS, the reference currents $I_{ref\,H}$ and $I_{ref\,L}$ ultimately drive the differential amplifier tail currents $I_{tail\,H}$ and $I_{tail\,L}$ through emitter degenerated current mirrors. Since $I_{ref\,H}$ and $I_{ref\,L}$ are derived from a proportional to absolute temperature (PTAT) current mirror that is described in section 6.3, then the currents $I_{tail\,H}$ and $I_{tail\,L}$ will also be proportional to absolute temperature. Therefore, the temperature dependency of g_m in the differential amplifiers, as mentioned in section 3.1.3, will be cancelled.

At the heart of the DCCS are transistors Q12, Q13, and Q14 that form a PNP differential pair. These transistors steer the current $I_{ref\ L}$ either to ground or to the low-state current mirror (Q8, Q9, and Q10) that provides the current $I_{tail\ L}$. The base rail of the low-state current mirror is connected to transistor Q11. If the signal Gain Select is above Reference so that Q12 conducts and Q13 and Q14 doesn't, then the current $I_{ref\ L}$ drives the low-state current mirror. This provides the tail current $I_{tail\ L}$ and also causes Q11 to begin conducting. When Q11 starts to conduct, the voltage across RHC2 decreases since Q11 is sinking some of the current from $I_{ref\ H}$. Therefore, the initially reverse-biased base-to-collector junction of Q11 begins to forward bias so that Q11 moves into the saturation region. With Q11 in saturation, all of the current $I_{ref\ H}$ is sunk to ground through Q11. Thus, the mirror that provides the current $I_{tail\ H}$ is turned off due to a lack of current. Figure 3.6 shows a simulation of the voltage across RHC2, the base-to-collector voltage of Q11, and the collector current of Q11 where it is seen how the saturation of Q11 occurs as the Gain Select voltage rises.

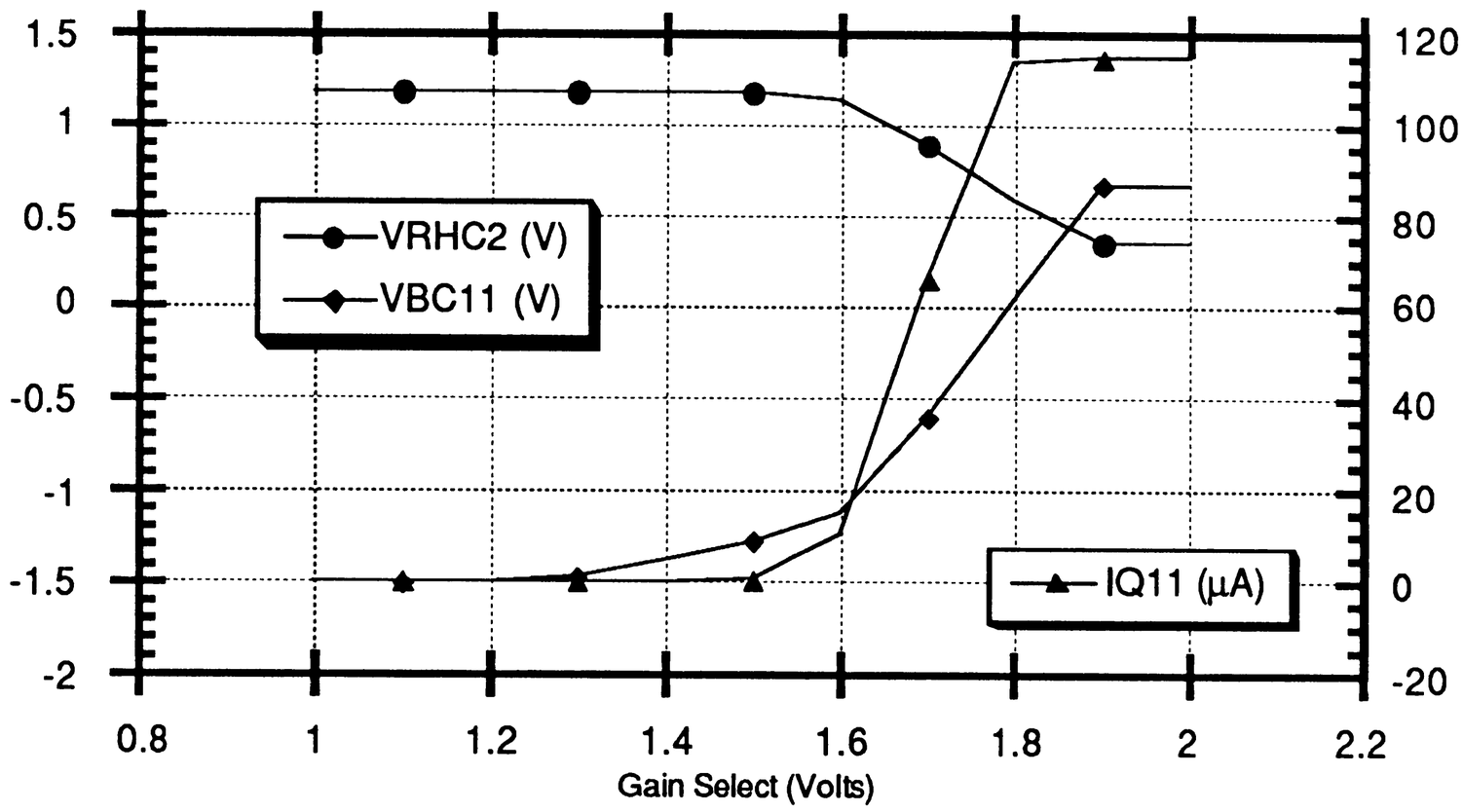

Figure 3.6:VRHC2, VBC11, and IQ11 During State Change

When Gain Select is below Reference so Q13 and Q14 conduct and Q12 is off, then the current $I_{ref\ L}$ is sunk to ground through Q13 and Q14. Therefore, the low-state current mirror is turned off, which also turns off Q11 so the high-state current mirror (Q5, Q6, Q7) may provide the current $I_{tail\ H}$ by mirroring

$I_{ref\ H}$. The switching of $I_{tail\ H}$ and $I_{tail\ L}$ is shown in figure 3.7 as Gain Select increases.

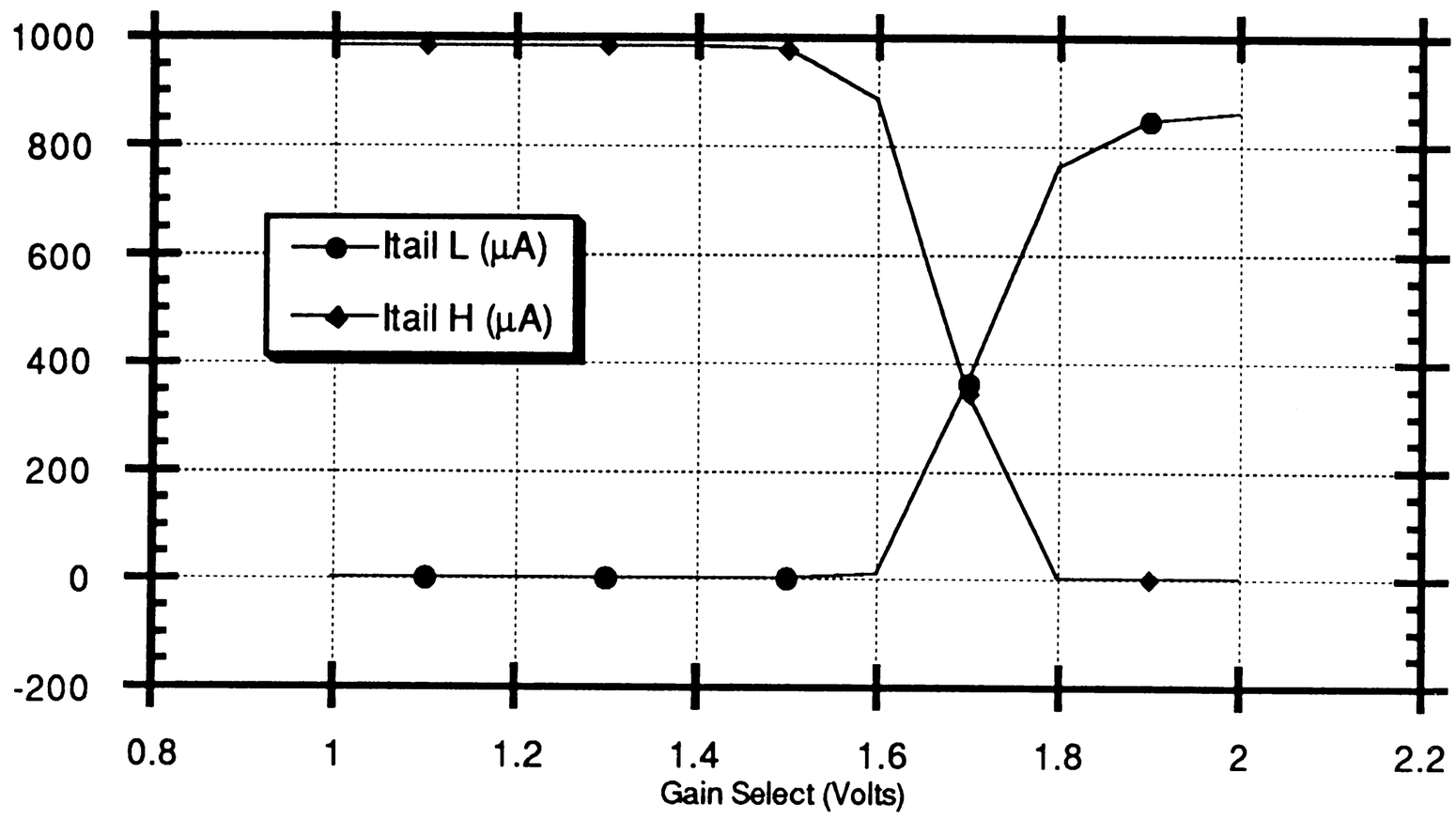

Figure 3.7: $I_{tail\ L}$ and $I_{tail\ H}$ During State Change

The transistors Q6 and Q9 of the high-state and low-state current mirrors are provided as "beta helpers" to reduce the effects of low β on the error of the current mirrors [6]. Also, for each of the current mirrors, the resistor values (RLC1, RLC2, RHC1, and RHC2) are selected so as to provide a high current gain between the reference currents and the tail current outputs. The high gain is needed to allow the use of small reference currents so that the low supply current target is met. Each pair of resistors sets the gain such that the tail currents are appropriate for each stage as defined in the previous discussion. The formula used to obtain the resistor values for the current mirrors is the transcendental equation 3.29 as shown below.

$$V_T \ln\left[\frac{I_{ref}}{I_{tail}} \frac{Size_{tail}}{Size_{ref}}\right] = I_{tail}R_{tail} - I_{ref}R_{ref} \qquad \text{(Eq.3.29)}$$

The Reference signal is a temperature independent voltage derived from the bandgap reference as described in section 6. Since this reference voltage is also used in the mixers and the phase shifter, the diode Q14 is required to lower the switch point so as to obtain near-TTL compatible logic levels.

3.3 Emitter Follower Design

The emitter follower subcircuit is shown in figure 3.8. This circuit was selected as a unity-gain buffer between the differential pair output and the next stage, whether it is another differential pair or coupling capacitors.

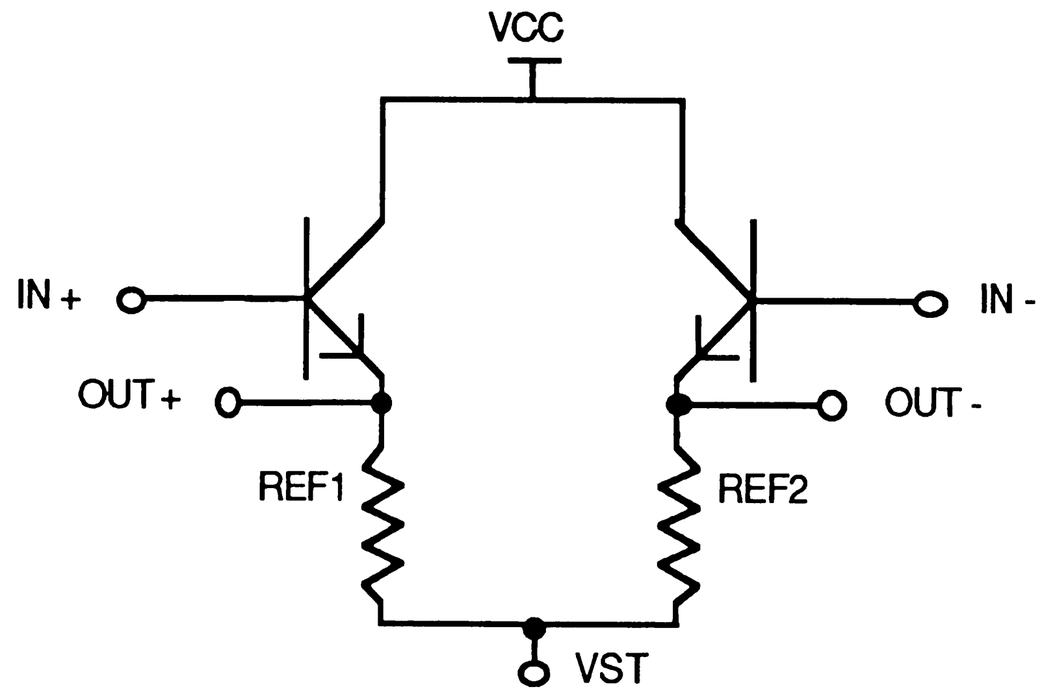

Figure 3.8: Emitter Follower Subcircuit

The node V_{ST} is connected to the collector of a large saturating transistor that is described in the bandgap description of section 6. With the bandgap circuit enabled, V_{ST} is equal to the V_{SAT} of a large NPN saturating transistor, while when the circuit is disabled, V_{ST} goes high so that only a minimum of current is drawn through the emitter followers. The emitter followers of each stage in the IF amp are connected to this node. This connection facilitates the low supply current requirement of the sleep mode whose implementation is to be described in section 6.

In selecting R_{EF}, a primary consideration is to avoid slew rate limiting when driving large capacitances such as the parasitic capacitance of the coupling capacitors between the first and second stages and following the last stage of the IF amplifier. Therefore, the current needed to drive the load capacitance may be found by equation 3.30,

$$I_{EF\ min} = C_L(f_{op})V_{peak\ s\text{-}e} \qquad \text{(Eq. 3.30)}$$

and to determine R_{EF}, worst case conditions must be considered as done in equation 3.31.

$$R_{EF} = \frac{V_{cc\ min} - \frac{I_{tail\ max}}{2} R_C(1 + \varepsilon_R) - V_{be\ max} - V_{st\ max}}{I_{EF\ min}(1 + \varepsilon_R)} \quad \text{(Eq. 3.31)}$$

The gain of the emitter follower may be determined by the formula [6] in equation 3.32.

$$A_{v\,EF} = 20 \log\left[\frac{1}{1 + \frac{R_c + \beta_o \frac{V_T}{I_{EF}}}{(\beta_o + 1)R_{EF}}}\right] \quad \text{(Eq. 3.32)}$$

The gain of an emitter follower has a temperature coefficient that is given by equation 3.33.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx -\frac{k}{qI_{EF}}\frac{1}{R_{EF}} \quad \text{(Eq. 3.33)}$$

In order to have a negligible loading effect on the load resistor of the differential pair, the emitter follower exhibits a high input impedance as shown by equation 3.34 [6]

$$R_i = \beta_o \frac{V_T}{I_{EF}} + R_{EF}(\beta_o + 1) \quad \text{(Eq.3.34)}$$

Also, the emitter follower has a low output impedance as shown by equation 3.35.

$$R_o = \left[\frac{1}{g_m} + \frac{R_c}{(1 + \beta_o)}\right] \| R_{EF} \quad \text{(Eq. 3.35)}$$

3.3.1 Example Calculations for 24 / 0 dB Emitter Follower

To continue the example as discussed before so as to obtain a design for the emitter follower stage for the 24 / 0 dB amplifier, the emitter follower current may be found using equation 3.30 as shown in equation 3.36. The load capacitance is equivalent to the bottom plate to substrate parasitic

capacitance of about 1 pF for the 32 pF coupling capacitor that follows the 24 / 0 dB amplifier and a layout capacitance of about 0.5 pF

$$I_{EF\,min} = (1.5\text{ pF})(2\pi)(70\text{ MHz})(0.30\text{ V}) = 198\ \mu\text{A} \qquad \text{(Eq. 3.36)}$$

Now, using this current, the emitter follower load resistor may be found with equation 3.31 as shown in equation 3.37.

$$R_{EF} = \frac{4.75\text{ V} - \frac{2\text{ mA}}{2}(845\ \Omega)(1 + 0.2) - 0.8\text{ V} - 0.3\text{ V}}{198\ \mu\text{A}(1 + 0.2)} = 11\ \text{k}\Omega \qquad \text{(Eq. 3.37)}$$

Given the calculated values of I_{EF} and R_{EF}, the gain through the emitter follower may be calculated using equation 3.32 as shown in equation 3.38.

$$A_{v\,EF} = 20\log\left[\frac{1}{1 + \frac{845\ \Omega + 57\frac{26\text{ mV}}{198\ \mu\text{A}}}{(57 + 1)11\ \text{k}\Omega}}\right] = -0.113\text{ dB} \qquad \text{(Eq. 3.38)}$$

Also, the gain error due to temperature may be found using equation 3.33, as shown in equation 3.39, and converting to decibels as found in equation 3.40.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx -\frac{1.38\text{ X }10^{-23}\frac{\text{J}}{\text{K}}}{(1.602\text{ X }10^{-19}\text{C})(198\ \mu\text{A})}\frac{1}{11\ \text{k}\Omega} = -40\frac{\text{ppm}}{^\circ\text{K}} \qquad \text{(Eq. 3.39)}$$

$$\varepsilon_{AV_T} = 20\log\left[1 + \frac{(\pm 60\ ^\circ\text{K})(-40\text{ ppm}/^\circ\text{K})}{10^6}\right] = \pm 0.021\text{ dB} \qquad \text{(Eq.3.40)}$$

The input and output impedances may now be found using the emitter follower current and load resistor as shown in equation 3.41 and 3.42, respectively.

$$R_i = 57\frac{26\text{ mV}}{198\ \mu\text{A}} + 11\ \text{k}\Omega(57 + 1) = 645\ \text{k}\Omega \qquad \text{(Eq.3.41)}$$

$$R_o = \left[\frac{26\text{ mV}}{198\ \mu\text{A}} + \frac{845\ \Omega}{(1 + 57)}\right] \| \ 11\ \text{k}\Omega = 144\ \Omega \qquad \text{(Eq. 3.42)}$$

With the calculated values as found above, it is evident that the input impedance of the emitter follower is much higher than the differential pair load resistor. Therefore, the conclusion made previously that it has a negligible effect may be considered to be true. Also, the gain loss as contributed by the emitter follower may be considered to be small, but since the specifications of each amplifier call for a ±0.6 dB error, a recalculation of the resistor may be considered. Since the ADVICE [7] simulator may be used to "fine tune" the design, the recalculation will, in effect, be made after performing worst case simulations and adjustments of the resistor values are found to meet the specifications.

3.4 Interconnection of Differential Amplifiers

The complete IF amplifier stage is made complete by the interconnection of the four Digitally Controlled Differential Amplifiers each with gains of 24 / 0, 12 / 0, 6 / 0, and 3 / 0 dB. This section will discuss how offset problems may be reduced, the overall calculated gain and error performance of the complete IF amplifier, and simulation results of the complete IF amplifier.

3.4.1 Using Coupling Capacitors to Reduce Offset Problems

With a total maximum gain of 45 dB, the IF amplifier could be susceptible to the amplification of the input offset voltage. If this occurs, with maximum gain, the output of the IF stage could be pinned to one of the supply rails. To reduce the possibility of this happening, capacitors should be placed between the 24 dB and the 12 dB amplifiers. The addition of coupling capacitors between these stages splits the possible gain of an offset into 24 dB and 21 dB maximum gain segments. Although these gains are still fairly large, with proper device placement in the layout of the differential pairs, the offsets shouldn't be large enough to cause latching of each segments outputs. The coupling capacitors should be as large as possible so as to reduce the voltage divider loss between the high frequency coupling capacitor impedance and the input impedance of the next stage. Therefore, the largest available capacitors on the ALA202 array were used. The 32 pF capacitance should be large enough at the 70 MHz operating frequency. A

block diagram of the four DCGDA stages is shown in figure 3.9 with the placement of the coupling capacitors.

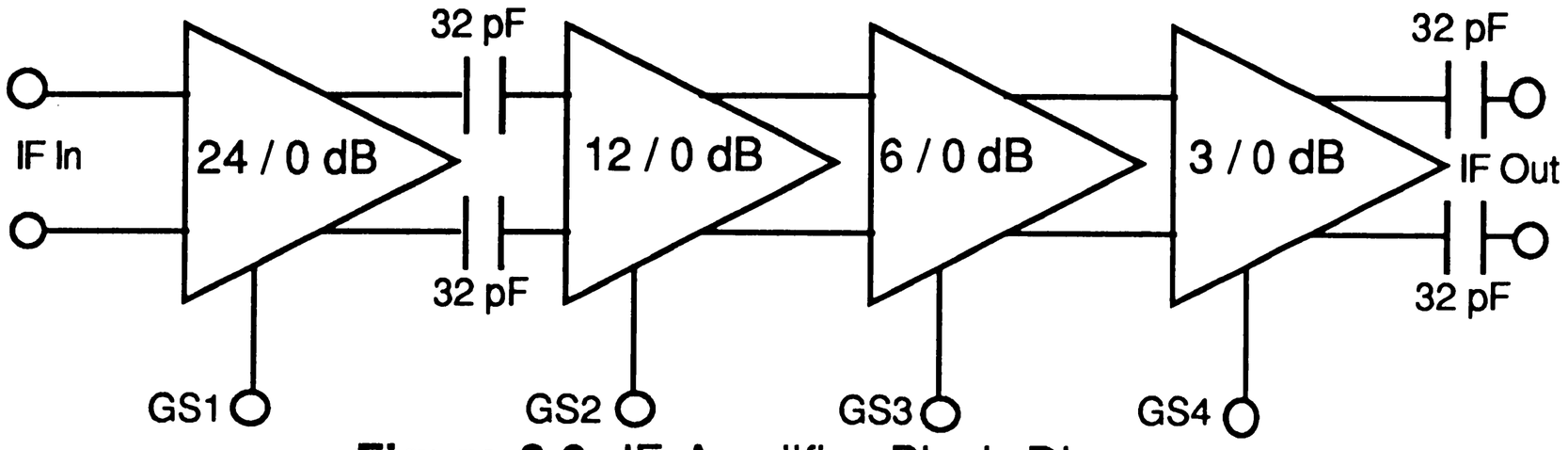

Figure 3.9: IF Amplifier Block Diagram

3.4.2 Calculated IF Amplifier Gain and Error Performance

In the previous sections, an example calculation for the 24 / 0 dB Digitally Controlled Gain Differential Amplifier was performed. The resistor values and the gain performance characteristics for examples of the remainder of the blocks is presented here. In addition, the total maximum gain error is also presented by finding the sum of the gains for each block in the IF amplifier stage. Table 3.1 shows the calculated values.

Stage	R_c	I_{tail}	R_e	I_{EF}	R_{EF}	$A_{V\ EF}$	$A_{V\ nom}$	$A_{V\ min}$	$A_{V\ max}$	ΔA_V
Units	Ω	*mA*	Ω	μA	$k\Omega$	*dB*	*dB*	*dB*	*dB*	*dB*
24/0 dB	845	0.74	753	198	11	-0.113	0.0	-0.501	+0.275	±0.388
		2	25				24.0	23.230	24.544	±0.657
12/0 dB	845	0.74	753	66	39	-0.091	0.0	-0.483	+0.301	±0.392
		0.74	136				12.0	11.356	12.462	±0.553
6/0 dB	845	0.74	753	66	39	-0.091	0.0	-0.483	+0.301	±0.392
		0.74	342				6.0	5.463	6.355	±0.446
3/0 dB	845	0.74	753	198	13	-0.097	0.0	-0.488	+0.294	±0.391
		0.74	512				3.0	2.490	3.316	±0.413

Table 3.1: Resistor Values and Gains for the DCGDA Amplifiers

The total maximum low-gain error due to DCGDA errors is equivalent to the difference between 45 dB and the sum of the $A_{V\ min}$ gains for the maximum gain settings of each stage, while the total maximum high-gain error is the same except the $A_{V\ max}$ gains are used. This results in a maximum low-gain error of -2.461 dB and a maximum high-gain error of +1.677 dB. Therefore,

the total gain error is close to the allocated ±2.4 dB error for the full IF amplifier stage.

An additional gain error may be due to the coupling capacitor between the 24 / 0 dB and 12 / 0 dB stages and the coupling capacitor at the output of the IF amplifier stage. Each coupling capacitor is 32 pF and the 12 / 0 dB amplifier has an input impedance of approximately 10 kΩ, while the two mixers connected to the output of the IF amplifier stage each has an approximate input impedance of 10 kΩ for a parallel impedance of 5 kΩ. It is evident, since the impedance of the 32 pF capacitor at 70 MHz is 71 Ω, that this voltage divider gain error is negligible.

3.4.3 IF Amplifier Simulation Results

The IF amplifier simulations are focused on determining the gain variation through the four DCGDA amplifier stages. Through the use of ADVICE [7], the full IF amplifier, including the coupling capacitors, was simulated. An approach was taken whereby two simulations were performed, one with all gains low and one with all gains high. By finding the gain through each stage for the two states, the two gains for each stage was determined. Simulations were performed at three junction temperatures, -25 °C, 25 °C, and 95 °C. Only the 95 °C temperature included a 10 °C increment above the maximum 85 °C ambient temperature to account for the thermal impedance of the package.

During the simulation phase of the design, resistor values, such as R_c and R_e, were changed slightly so as to center the gain variations within the ±0.6 dB gain error allowed for each amplifier. Also, the tail currents were changed slightly so as to achieve the desired performance while achieving the lowest supply current possible. In practice, none of the resistor values or tail currents were changed enough so as to warrant the re-calculation of the design parameters by hand. Table 3.2 shows a summary of the simulation results where the nominal values are at 25 °C and the minimum and maximum values are for the range of temperatures. The full set of simulation results for the IF amplifiers is shown in appendix 1.

Stage	$A_{V\ nom}$	$A_{V\ min}$	$A_{V\ max}$	ΔA_V
Units	*dB*	*dB*	*dB*	*dB*
24/0 dB	+0.325	-0.455	+0.395	±0.425
	+24.28	+22.96	+24.65	±0.845
12/0 dB	-0.026	-0.652	+0.167	±0.409
	+11.93	+11.12	+12.16	±0.520
6/0 dB	+0.141	-0.491	+0.369	±0.430
	+6.11	+5.43	+6.37	±0.470
3/0 dB	+0.072	-0.661	+0.193	±0.427
	+3.18	+2.53	+3.30	±0.385

Table 3.2: Simulated Gains for the DCGDA Amplifiers

By comparing the ΔA_V columns of tables 3.1 and 3.2, it may be seen that the calculations for the gain error in each amplifier was reasonably close. Some explanation for the discrepancies is that ADVICE [7] uses significantly more sophisticated models that those that were used to determine the design equations. Also, since some of the resistor values were modified slightly, this may also be offered as an explanation.

The simulations show that a total minimum gain error of -2.96 dB and a total maximum gain error of +1.48 dB results in a ±2.22 dB spread of the gain errors. This compares with the -2.606 dB minimum and +1.822 dB maximum gain errors that resulted in a ±2.214 dB spread. Due to the limited resistor selection in the use of a linear array, the centering of the spread was considerably difficult.

4. Double Balanced Mixer and Output Stage

The In-phase (I) and Quadrature (Q) mixers of the integrated circuit are shown as blocks in figure 2.1. Their function is to perform demodulation of a Gaussian-filtered Minimum Shift Keying (GMSK) signal at a frequency of 70 MHz, such that the I and Q outputs result in digital signals at frequencies up to 1 MHz. Output stages are included on the differential outputs of both the I and Q mixers. The output stages provide buffering to drive the output load as specified in section 2.2.5.

The following sections describe the operation and design of the double balanced mixer and output stages. Section 4.1 describes how GMSK demodulation is performed in this circuit. The design of the double balanced mixer and the output stage is described in sections 4.2 and 4.3, respectively. An example calculation of component values, gain, and gain errors for the mixer and output stages is presented in section 4.4, while section 4.5 discusses and presents the simulation results for the combined mixer and output stages.

4.1 GMSK Demodulation

GMSK signals are similar in nature to Quadrature Phase Shift Keying (QPSK) signals in that the information content of the signal is based on the relative phase of the modulated signal. A means of demodulation for this type of signal is by the multiplication of two equal frequency signals. The multiplication of the GMSK signal with a local oscillator (LO) signal of constant phase and a frequency equal to that of the input signal will result in the demodulation of the input signal's information content [9].

A GMSK input signal, s(t), is phase modulated such that the mathematical representation of the signal is as shown in equation 4.1.

$$s(t) = A_i \cos (2\pi f_o t + \theta_i(t)) \qquad \text{(Eq. 4.1)}$$

where $\theta_i(t) = \{\theta_1 , \theta_1 + 90°, \theta_1 + 180°, \theta_1 + 270°)\}$

This GMSK modulated signal, s(t), contains information that consists of two separate bit streams. Each of the four possible phase settings of θ_i represents two bits of information for a single data time frame.

The multiplication of the input signal, s(t), and the local oscillator signals, $LO_i(t)$ and $LO_q(t)$, produces the two bit stream outputs. The mathematical representations of the local oscillator I and Q mixer inputs are shown in equations 4.2 and 4.3, while the resulting output formulas are shown in equations 4.4 and 4.5 for the I and Q channels, respectively. The output equations assume that there is a low pass filtering circuit on the output of the mixers so as to remove a component equal to twice the carrier frequency that would remain in the output signal. The following sections will describe this filtering circuit.

$$LO_i(t) = A_{lo} \cos (2\pi f_o t + \theta_{lo}) \qquad \text{(Eq. 4.2)}$$

$$LO_q(t) = A_{lo} \sin (2\pi f_o t + \theta_{lo}) \qquad \text{(Eq. 4.3)}$$

$$out_i(t) = A_i A_{lo} \left[\frac{1}{2} \cos (\theta_i(t) - \theta_{lo})\right] \qquad \text{(Eq. 4.4)}$$

$$out_q(t) = A_i A_{lo} \left[-\frac{1}{2} \sin (\theta_i(t) - \theta_{lo})\right] \qquad \text{(Eq. 4.5)}$$

It can be seen from equations 4.4 and 4.5, that the phase, θ_i, may be changed so that, when demodulated, the I and Q output levels will represent either a binary 1 or 0. Table 4.1 shows an example of the possible decoding patterns that could result from the I and Q outputs in a single data time frame.

Input Phase	I Output	Q Output
θ_1	0	0
$\theta_1 + 90°$	0	1
$\theta_1 + 180°$	1	0
$\theta_1 + 270°$	1	1

Table 4.1: Phase Input Bit Representation

The bit representations of the I and Q outputs are determined by a decision circuit that is externally connected to the mixer outputs. An optimum

detectable output will result as long as $|\theta_{lo} - \theta_1|$ is equal to some multiple of 45°. If $|\theta_{lo} - \theta_1|$ is equal to 0°, 90°, 180°, or 270°, then the decision circuit may produce errors for some bits. Therefore, external circuitry should be used in the integrated circuit's application so as to change the local oscillator phase, θ_{lo}, such that the output is detectable and a low bit error rate will result [3].

The use of a double balanced Gilbert-cell mixer [6, 8] will implement the multiplication function that is required for GMSK demodulation. The design of this mixer circuit is discussed in the next section.

4.2 Double Balanced Mixer Design

The Gilbert-cell double balanced mixer [6, 8] of figure 4.1 performs the demodulation function as described in the previous section. The differential input signal, V_{if}, is applied to the bases of transistors Q5 and Q6, while the local oscillator signal, V_{lo}, is across the input of the cross coupled pair of transistors Q1 through Q4. The emitter degeneration resistor, R_g, is used to develop a conversion gain which is defined as the ratio of the output level to the IF input level, each at their respective frequencies. The output stage, to be described later, is differentially driven by the output V_{out}.

The following sections will describe the operation of the mixer, the determination of conversion gain, and the low pass output filtering circuit.

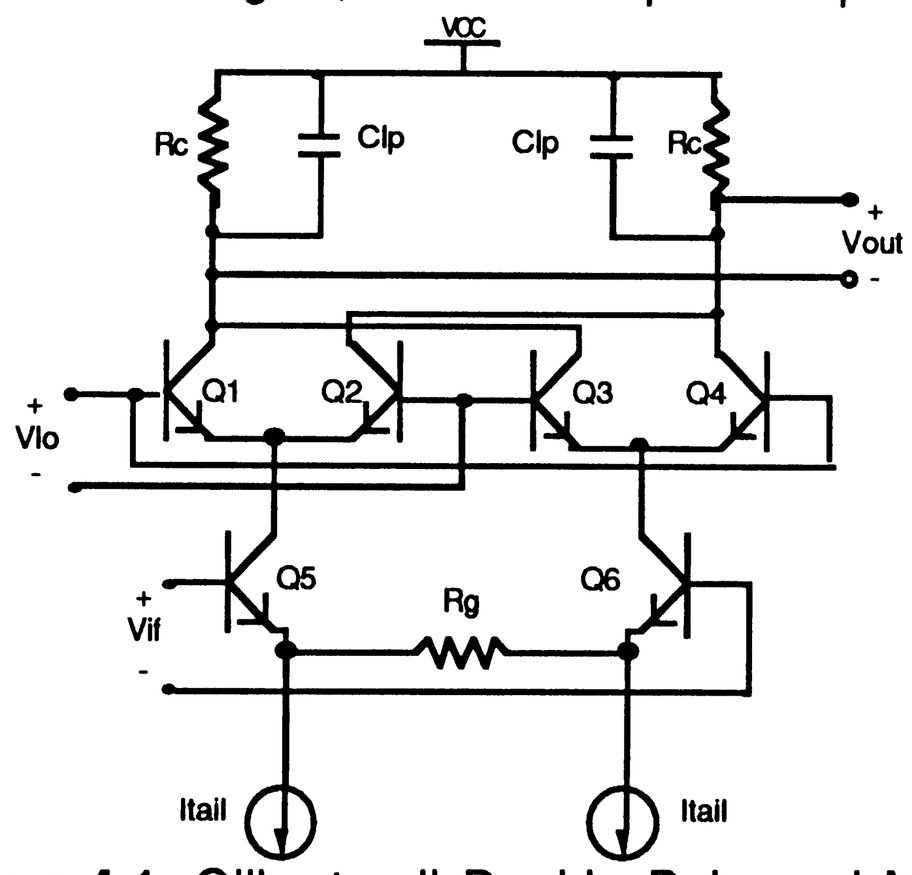

Figure 4.1: Gilbert-cell Double Balanced Mixer

4.2.1 Mixer Operation

The demodulation of the GMSK modulated signal in this circuit is performed somewhat differently than the simple multiplication as described in the previous section. The LO inputs of the mixer are designed so that the amplitude is much larger than $2 \cdot V_T$. As explained in Grey and Meyer [6], this causes the transistors Q1 through Q4 to behave like switches, so that the signals from the linearly operating devices Q5 and Q6 are multiplied by a +1 to -1 square wave. Therefore, the input signal, s(t), as shown in equation 4.1, is multiplied with the square wave functions as shown in equation 4.6 for the I channel and equation 4.7 for the Q channel.

$$LO_i(t) = \sum_{n=1}^{\infty} A_n \cos (2\pi n f_o t + n\theta_{lo}) \qquad \text{(Eq. 4.6)}$$

$$LO_q(t) = \sum_{n=1}^{\infty} A_n \sin (2\pi n f_o t + n\theta_{lo}) \qquad \text{(Eq. 4.7)}$$

where $$A_n = \frac{\sin n\frac{\pi}{2}}{\frac{\pi}{4}}$$

The resulting outputs for both the I and Q channels are shown in equations 4.8 and 4.9, where only the n=1 component is within the pass band of the low pass filter.

$$out_i(t) = \frac{2KA_i}{\pi} \left[\cos (\theta_i(t) - \theta_{lo})\right] \qquad \text{(Eq. 4.8)}$$

$$out_q(t) = -\frac{2KA_i}{\pi} \left[\sin (\theta_i(t) - \theta_{lo})\right] \qquad \text{(Eq. 4.9)}$$

where K = gain from transistors Q5 and Q6

From equations 4.8 and 4.9, it is seen that they are similar to equations 4.4 and 4.5 in that they result in output voltages that are proportional to the input phase $\theta_i(t)$. The advantage of using the square wave input is evident from

equations 4.8 and 4.9 in that the output level is independent of the LO input amplitude.

Since the specification of section 2.2.2 calls for a conversion gain of 6 dB through the mixers, the transistors Q5 and Q6 must exhibit a gain of K so that the factor in the output equations with yield the desired gain. As seen in the next section, the calculation of the gain factor is similar to the gain calculations as found in the IF amplifiers.

4.2.2 Gain Determination and Selection

The mixer gain factor may be found by simplifying the configuration of Q5, Q6, R_g, and I_{tail} such that it resembles the emitter degenerated emitter coupled pair of figure 3.2 in the IF amplifier section. This is done by assuming that the resistor R_g is split into two resistors each of value $R_g / 2$ that are driven at their common point by a current source equal to $2 \cdot I_{tail}$. Therefore, the gain of these transistors may be found by using equation 3.1 with the appropriate parameters, as shown in equation 4.10.

$$K = \frac{R_C}{\frac{V_T}{2 \cdot I_{tail}} + \frac{R_g}{2}} \qquad \text{(Eq. 4.10)}$$

With the combination of equations 4.8, 4,9, and 4.10, the overall mixer gain may be found for each channel by equations 4.11 and 4.12 .

$$out_i(t) = \frac{4A_i}{\pi} \cdot \frac{R_C}{\frac{V_T}{I_{tail}} + R_g} \left[\cos\left(\theta_i(t) - \theta_{lo}\right)\right] \qquad \text{(Eq. 4.11)}$$

$$out_q(t) = -\frac{4A_i}{\pi} \cdot \frac{R_C}{\frac{V_T}{I_{tail}} + R_g} \left[\sin\left(\theta_i(t) - \theta_{lo}\right)\right] \qquad \text{(Eq. 4.12)}$$

Assuming that the condition of optimum detection is achieved, as set forth at the end of section 4.1, the absolute value of the multiplier due to the cosine and sine terms in equations 4.11 and 4.12 will have a value of $1/\sqrt{2}$. Therefore, the mixer gain may be found by equation 4.13.

$$Av = \frac{4}{\pi} \cdot \frac{R_c}{\frac{V_T}{I_{tail}} + R_g} \cdot \frac{1}{\sqrt{2}} \qquad \text{(Eq. 4.13)}$$

Since the calculation of gain is similar to that of the IF amplifiers, then the calculation of gain errors will also be similar. The calculation of gain error may be simplified in that the effects of parasitic capacitances on the gain may be neglected, since at the load resistor, the output frequency is less than 1 MHz. Therefore, the 0.3 dB rolloff error allocation may be eliminated.

Equation 3.14 may be used for the gain temperature coefficient due to resistor temperature coefficient with some modifications as shown in equation 4.14.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx \frac{4}{\pi} \cdot \frac{1}{\sqrt{2}} \left[1 - \frac{R_g}{\frac{V_T}{I_{tail}} + R_g} \right] \frac{1}{R}\frac{\partial R}{\partial T} \qquad \text{(Eq.4.14)}$$

The gain error due to resistor tracking errors may be found with equation 4.15. This is similar to equation 3.15 as used for the IF amplifiers.

$$\varepsilon_{AV_R} \approx 20 \log \left[1 + \frac{1}{2} \left(1 + \frac{A_{Vo}}{2} \frac{R_{go}}{R_{co}} \right) \varepsilon_{Rtrack} \right] \qquad \text{(Eq.4.15)}$$

Since the tail current, I_{tail}, of the mixer stages is not proportional to absolute temperature, then an additional error factor due to temperature is introduced. This temperature coefficient may be found by equation 4.16.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} = -\frac{4}{\pi} \cdot \frac{1}{\sqrt{2}} \cdot \frac{1}{To} \cdot \frac{V_{To}}{V_{To} + R_g I_{tail}} \qquad \text{(Eq. 4.16)}$$

The formulas described to calculate the mixer gain and gain error will be used in an example calculation as shown in section 4.4. The example calculation will also include the gain and gain errors for the output stage.

4.2.3 Low Pass Output Filter

In order to remove the high frequency components of the mixed IF and LO signals from the output, capacitors were added in parallel with the collector resistors to act as a low pass filter. The output voltage transfer function has a one pole rolloff which is characterized by equation 4.17.

$$TF_{LP} = \left(\frac{1}{1 + j \frac{f_o}{f_{LP}}} \right) \qquad \text{(Eq. 4.17)}$$

where

$$f_{LP} = \frac{1}{2\pi R_c C_{lp}}$$

The pole of the transfer function should be set at least one decade below the lowest unwanted high frequency component that may result. This will achieve at least a 20 dB attenuation of all high frequency components. The lowest high frequency component that could result in the outputs of equations 4.11 and 4.12 without filtering is at the operating frequency of 70 MHz. Therefore, the low pass frequency, f_{LP}, should be set at no less than 7 MHz.

4.3 Output Stage Design

As stated in section 2.2.5, the differential output stage of each mixer must be able to drive a 1 kΩ resistive load in parallel with a 30 pF capacitive load, exhibit an output impedance of no more than 50 Ω, and be capable of a 1 Vpp differential signal swing at frequencies of 1 MHz or less without distortion. In order to adhere to the goal of a low overall power dissipation for the circuit, a class AB complementary push-pull output stage was selected. The circuit diagram for each side of the mixer's differential output is shown in figure 4.2

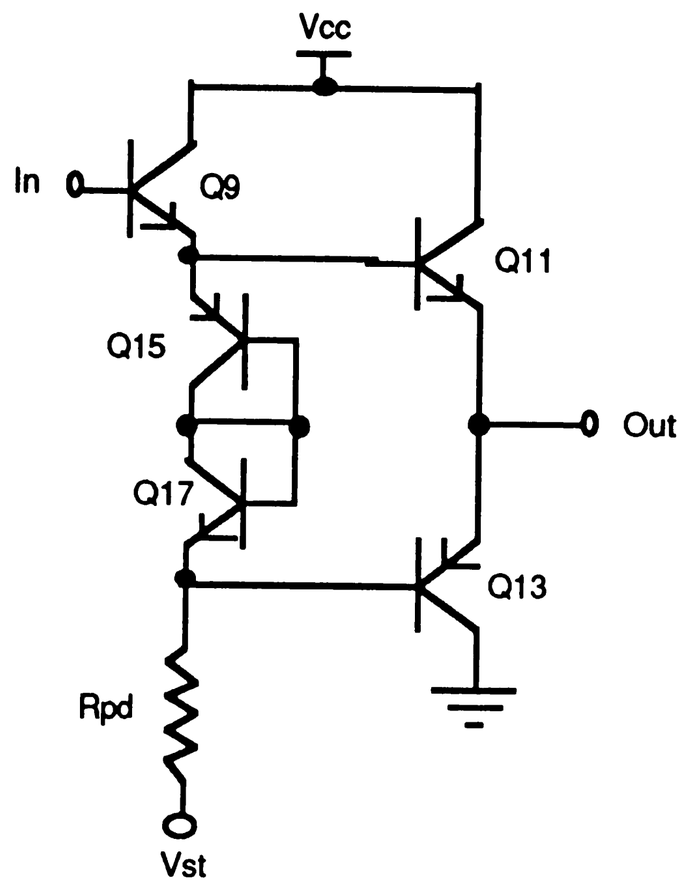

Figure 4.2: Class AB Complementary Push-pull Output Stage

The base of transistor Q9 is connected to one of the differential outputs of the mixer stage as shown in figure 4.1. This transistor acts as an emitter follower buffer that exhibits a high input impedance and a low output impedance. Therefore, the signal is driven by the emitter follower at the junction of transistors Q15 and Q11.

Transistors Q11 and Q13 form the complementary push-pull output driver. Since these transistors act as emitter followers when connected to the output load, the output drive capability is more than sufficient for the required load. In addition, the output impedance of the push-pull stage is essentially equal to $\frac{1}{2 \cdot g_{m\ 11\text{-}13}}$. This is found by reducing the output impedance formula of equation 3.35 for the emitter follower given that the source impedance is small and divided by β, as is seen looking into Q9 - Q15 and Q17 - R_{pd}. Therefore, the output impedance requirement may be achieved by setting $g_{m\ 11\text{-}13}$ appropriately.

The diode connected transistors, Q15 and Q17, provide the operating point for the push-pull stage so that the output stage operates as a class AB amplifier. Class AB operation is accomplished when the transfer function of the amplifier is such that there is no cross over distortion or "dead zone" that occurs when the input voltage is within the range $\pm V_{BE}$. The operating point

of transistors Q15 and Q17 also sets the operating point of transistors Q11 and Q13. This is evident by identifying the loop of V_{BE} drops around the four transistors. The bias current of transistors Q11 and Q13 may be determined by equation 4.18, where I_{tail} and R_c is from the mixer stage and V_{ST} is the saturating transistor's voltage as mentioned in section 3.3 and to be further described in section 6.5.

$$I_{c\ 11\text{-}13} = \sqrt{\frac{A_{11}\cdot A_{13}}{A_{15}\cdot A_{17}}}\left[\frac{V_{cc}-I_{tail}\cdot R_c-3V_{BE}-V_{ST}}{R_{pd}}\right] \qquad \text{(Eq. 4.18)}$$

The output swing capability of the complementary push-pull output stage is limited only by the power supply rails. Thus, the 1 Vpp differential output swing will be easily obtained since the push-pull's output is approximately $2\cdot V_{BE}$ (or about 1.5 V) below it's input.

The calculation of gain and gain error for the output stage is the same as found in section 3.3 for the emitter follower design of the IF amplifiers. This is because the output stage is essentially two emitter followers consisting of transistors Q9 and either Q11 or Q13. Therefore, by using equations 3.32 through 3.35, the gain and the gain error due to temperature may be found for the output stage. The next section will present an example calculation of the output stage's operating points and gain characteristics together with the previously described characteristics of the mixer stage.

4.4 Example Calculation for Mixer and Output Stages

The selection of components for the design of the mixer and output stages is determined by the requirements as set forth in section 2.5. The differential output swing should be capable of 1 Vpp with an output impedance of 50 Ω, while the conversion gain must nominally be 6 dB with a gain error of ±0.6 dB. Therefore, the mixer input should handle 0.5 Vpp without distortion.

The design of the mixer's R_c and I_{tail} will be found first, with the output stage design following. The gain setting resistor, R_g, in the mixer will then be designed to compensate for the loss in the output stage that will result.

Finally, the low pass filter will be designed so as to meet the requirements as discussed earlier.

The first parameter in the mixer to be chosen is the tail current, I_{tail}. Keeping in mind the need for a low overall supply current, I_{tail} is chosen to be 150 μA. With this, the collector resistor, R_c, may be chosen so as to obtain the desired output swing of 1 Vpp. The swing requirement dictates that at least 500 mV should be able to be dropped across R_c on each side of the amplifier without distortion. Therefore, the R_c voltage drop is chosen as 600 mV so that a margin of safety is present. This results in a value for R_c of 4 kΩ.

With the R_c and I_{tail} selected for the mixer, the output stage design may now be completed. The output impedance of the output stage, as discussed in section 4.3, is determined by the formula $\frac{1}{2 \cdot g_{m\ 11\text{-}13}}$. Therefore, to obtain an output impedance of less than 50 Ω, the value of $I_{c\ 11\text{-}13}$ must be greater than 260 μA. From equation 4.18, the values of R_{pd} and the emitter areas of transistors Q11, Q13, Q15, and Q17 may be set to meet the requirement. Using 300 μA for $I_{c\ 11\text{-}13}$ will provide a margin of error and result in a nominal output impedance of 43 Ω. With the term $\sqrt{\frac{A_{11} \cdot A_{13}}{A_{15} \cdot A_{17}}}$ set equal to 4, the value of R_{pd} is calculated in equation 4.19.

$$R_{pd} = 4\left[\frac{5.0\ V - 150\ \mu A \cdot 4\ k\Omega - 3(0.75\ V) - 0.2\ V}{300\ \mu A}\right] = 26\ k\Omega \quad \text{(Eq. 4.19)}$$

As mentioned in section 4.3, the output stage gain may be calculated with equation 3.32 as applied to transistors Q9 and either Q11 or Q13. Therefore, the calculations for output stage gain are found in equations 4.20 and 4.21 for Q9 and Q11, respectively.

$$A_{v\ EF\ 9} = 20 \log\left[\frac{1}{1 + \frac{4\ k\Omega + 110\ \frac{4(26\ mV)}{300\ \mu A}}{(110 + 1)21.8\ k\Omega}}\right] = -0.150\ dB \quad \text{(Eq. 4.20)}$$

$$A_{v\,EF\,11} = 20 \log\left[\frac{1}{1 + \dfrac{377\ \Omega + 110\,\dfrac{26\ mV}{300\ \mu A}}{(110 + 1)1\ k\Omega}}\right] = -0.743\ dB \qquad \text{(Eq. 4.21)}$$

Equations 4.20 and 4.21 show that a total loss of 0.893 dB results due to the emitter followers of the output stage. Therefore, the mixer gain should be set so that this loss is compensated for. This results in the need for a mixer gain of 6.893 dB.

Now, the mixer gain setting resistor, R_g, may be found by rearranging equation 4.13 and using the values of R_c, I_{tail}, and the corrected mixer gain. The calculation is shown in equation 4.22.

$$R_g = 4\ k\Omega \cdot \frac{4}{\pi} \cdot \frac{1}{\sqrt{2}} \cdot 10^{-\frac{6.893\ dB}{20}} - \frac{26\ mV}{150\ \mu A} = 1455\ \Omega \qquad \text{(Eq. 4.22)}$$

The capacitor of the low pass filter may now be selected to obtain the 7 MHz pole as recommended in section 4.2.3. From equation 4.17, the value of C_{lp} is found in equation 4.23.

$$C_{lp} = \frac{1}{2\pi \cdot 4\ k\Omega \cdot 7\ MHz} = 5.7\ pF \qquad \text{(Eq. 4.23)}$$

With the components values now designed for the mixer and output stages, the gain errors may be found. For the mixer, the gain temperature coefficient due to resistor temperature coefficient is found with equation 4.14 as shown in equation 4.24. The resulting gain error is shown in equation 4.25.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} \approx \frac{4}{\pi} \cdot \frac{1}{\sqrt{2}}\left[1 - \frac{1455\ \Omega}{\dfrac{26\ mV}{150\ \mu A} + 1455\ \Omega}\right] 1300\ \frac{ppm}{°C} = 125\ \frac{ppm}{°C} \qquad \text{(Eq.4.24)}$$

$$\varepsilon_{AV_{TR}} = 20 \log\left[1 + \frac{(\pm 60\ °C)(125\ ppm/°C)}{10^6}\right] = \pm 0.065\ dB \qquad \text{(Eq. 4.25)}$$

The mixer gain error due to resistor tracking errors, as found with equation 4.15, is calculated in equation 4.26.

$$\varepsilon_{AV_R} \approx 20 \log\left[1+\frac{1}{2}\left(1+\frac{10^{\frac{6.893\ dB}{20}}}{2}\frac{1455\ \Omega}{4\ k\Omega}\right)0.01\right] = \pm 0.061\ dB \quad \text{(Eq.4.26)}$$

The temperature coefficient due to the mixer tail current, as found by equation 4.16, is calculated in equation 4.27, while the error is found in equation 4.28.

$$\frac{1}{A_v}\frac{\partial A_v}{\partial T} = -\frac{4}{\pi\sqrt{2}} \cdot \frac{1}{298\ °K} \cdot \frac{26\ mV}{26\ mV + 1455\ \Omega \cdot 150\ \mu A} = -322\ \frac{ppm}{°K} \quad \text{(Eq. 4.27)}$$

$$\varepsilon_{AV_{TI}} = 20 \log\left[1 + \frac{(\pm 60\ °K)(-322\ ppm/°K)}{10^6}\right] = \mp 0.169\ dB \quad \text{(Eq. 4.28)}$$

The output stage gain temperature coefficient may found by using equation 3.33 as determined for the emitter follower circuit. Equation 4.29 and 4.30 show the calculations for transistors Q9 and Q11, respectively.

$$\frac{1}{A_{v\,9}}\frac{\partial A_{v\,9}}{\partial T} \approx -\frac{1.38 \times 10^{-23}\ \frac{J}{K}}{1.602 \times 10^{-19}\ C \cdot \frac{300\ \mu A}{4}}\frac{1}{21.8\ k\Omega} = -53\ \frac{ppm}{°K} \quad \text{(Eq. 4.29)}$$

$$\frac{1}{A_{v\,11}}\frac{\partial A_{v\,11}}{\partial T} \approx -\frac{1.38 \times 10^{-23}\ \frac{J}{K}}{1.602 \times 10^{-19}\ C \cdot 300\ \mu A}\frac{1}{1\ k\Omega} = -287\ \frac{ppm}{°K} \quad \text{(Eq. 4.30)}$$

Using the results of equations 4.29 and 4.30, the output stage gain errors may be found respectively in equations 4.31 and 4.32 for transistors Q9 and Q11.

$$\varepsilon_{AV_9} = 20 \log\left[1 + \frac{(\pm 60\ °K)(-53\ ppm/°K)}{10^6}\right] = \mp 0.027\ dB \quad \text{(Eq. 4.31)}$$

$$\varepsilon_{AV_{11}} = 20 \log\left[1 + \frac{(\pm 60\ °K)(-287\ ppm/°K)}{10^6}\right] = \mp 0.148\ dB \quad \text{(Eq. 4.32)}$$

The total mixer and output stage gain error may now be found by taking the sum of the results from equations 4.25, 4.26, 4.28, 4.31, and 4.32. The resulting gain error is $\mp$0.218 dB.

4.5 Simulation Results

The simulation of the output stage with ADVICE [7] was performed in conjunction with the phase shifter portion of the circuit. This was done to reflect the effects of the actual output amplitude from the phase shifter on the mixer and output stage results. Since the mixing function is non linear in nature, the results obtained from ADVICE [7] were not considered to be completely accurate. In addition, to perform simulations of gain results over temperature and processing variations, several simulations were required. As a result, simulation time had to be reduced significantly from the simulation time that would be required if full speed signals were used. Therefore, the mixer gain results were obtained by using an 11 MHz sine wave voltage on the mixer signal input, while a 10 MHz sine wave was applied to the phase shifter input. At these lower frequencies, the gain results are expected to be higher than desired primarily because of the reduced effect that parasitic capacitances will have. The results were determined by ADVICE's Fourier analysis command [7] at a frequency of 1 MHz. ADVICE [7] predicted a nominal gain of 7.09 dB, while the minimum was found to be 6.27 dB and the maximum was 7.40 dB. The result is a gain spread of ±0.565 dB, which is significantly greater than the previously calculated gain spread of ±0.218. The complete results for temperature and processing variations are shown in appendix 2.

5. Quadrature Phase Shifter

The quadrature phase shifter, as defined in section 2.6, provides two signals.that are 90° out of phase with each other to the LO inputs of the I and Q mixers. The maximum allowable phase error is defined to be ±3°. The phase shifter outputs are derived from an externally provided local oscillator signal that has a minimum amplitude of 100 mVpp and is equal in frequency to the input signal of the IF amplifiers. As described in section 4.2.1, the phase shifter outputs should be square waves that are equal in amplitude and much greater than $2 \cdot V_T$ so that equal output levels will result from the mixers .

In figure 2.3, the block diagram of the quadrature phase shifter shows an RC network driven by a buffered LO input with the outputs of the RC network driving two limiting amplifiers. This chapter will describe each of these blocks in more detail. Section 5.1 describes the buffer design, while section 5.2 shows the design of the RC phase shifter network. The next section discusses the design of the limiting amplifier. The final section, section 5.4, will present the simulation results that were obtained from ADVICE [7].

5.1 Buffer Design

The buffer that drives the input of the RC phase shifter network is a simple push-pull configuration that is driven by up-down emitter followers. The buffer provides near unity gain, has high input impedance, and low output impedance [6]. The circuit diagram of the buffer is shown in figure 5.1.

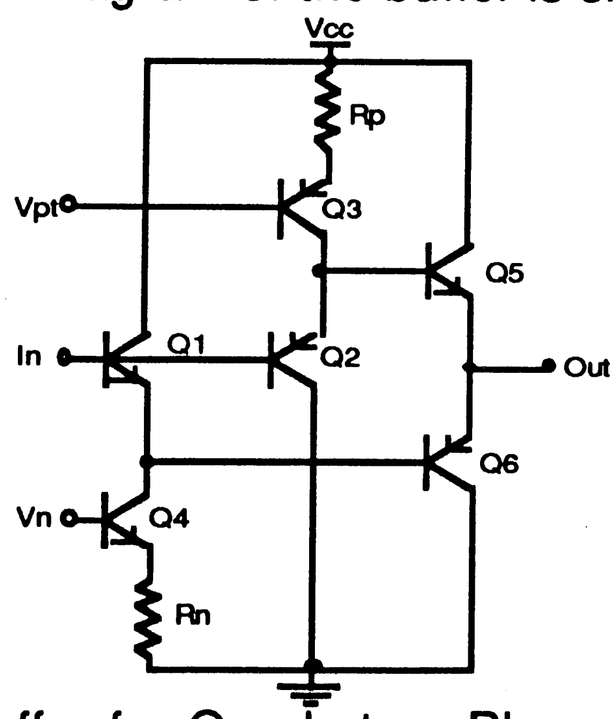

Figure 5.1: Buffer for Quadrature Phase Shifter Circuit

In figure 5.1, transistors Q3 and Q4 act as current sources for the emitter follower transistors Q1 and Q2. The bias levels of Q3 and Q4 are set with the voltages V_{pt} and V_n. These voltages are obtained from the bandgap circuit to be discussed in section 6. Transistors Q5 and Q6 form the push-pull stage of the buffer.

With a minimum LO input of 100 mVpp, as defined in section 2.6, the gain of the buffer may be considered to be unity and the gain errors neglected. This is practical since the required input to the mixers need only be greater than $2 \cdot V_T$ and the quadrature phase shifter block diagram shows limiting amplifiers to amplify and square the RC phase shifter outputs. If it were desirable to calculate the gain and gain errors of figure 5.1, then the gain and gain error through the buffer could be calculated similarly to the methods used for the IF amplifier emitter followers (section 3.3) and the mixer output stage emitter followers (section 4.3).

5.2 Phase Shifter Design

As stated in section 2.6, the phase shifter should provide two outputs that are 90°±3° out of phase with each other. To obtain equal amplitudes from the outputs that drive the I and Q mixers, the I output, V_i, should be +45° phase shifted from the V_{lo} phase while the Q output, V_q, should be -45° phase shifted from the V_{lo} phase [10]. These requirements are implemented with the phase shifter circuit as shown in figure 5.2.

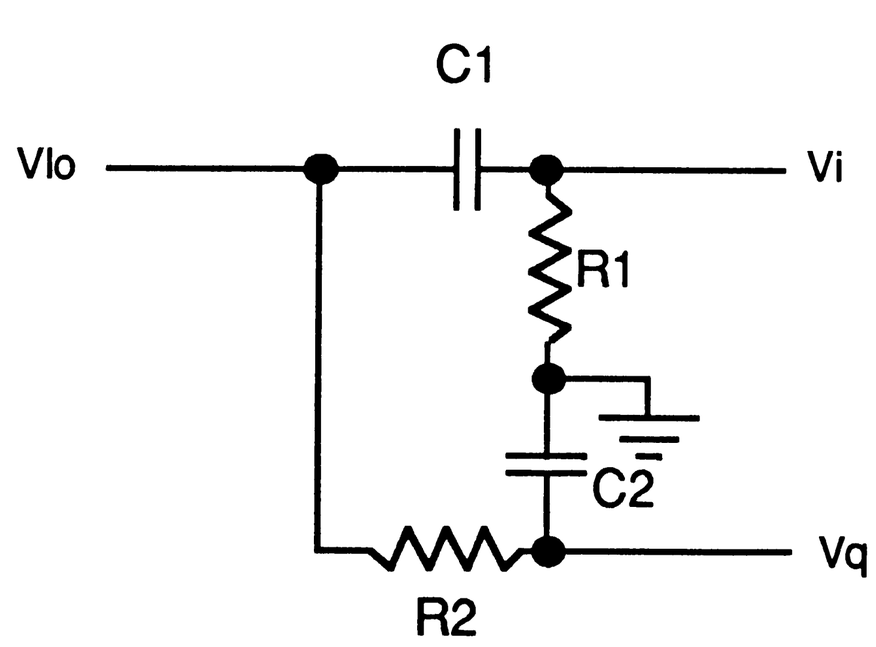

Figure 5.2: Phase Shifter Circuit

The phase of the I output, V_i, may be calculated with equation 5.1, while the phase of the Q output, V_q, is found with equation 5.2.

$$\phi_i = \tan^{-1}\left[\frac{1}{\omega C_1 R_1}\right] \qquad \text{(Eq. 5.1)}$$

$$\phi_q = \tan^{-1}\left[-\omega C_2 R_2\right] \qquad \text{(Eq. 5.2)}$$

The RC time constants in equations 5.1 and 5.2 are set so that ϕ_i and ϕ_q are equal to +45° and -45°, respectively, at the operating frequency of 70 MHz. This will result in both C_1R_1 and C_2R_2 equalling 2.274 ns.

The requirements of section 2.6 indicate that it is necessary that the phase between the I and Q outputs be equal to 90°. The equations for calculating the phase difference between the I and Q outputs are shown in equations 5.3a, b.

$$\Delta\phi = \tan^{-1}\left[\frac{\frac{1}{\omega C_1 R_1} + \omega C_2 R_2}{1 - \frac{C_2 R_2}{C_1 R_1}}\right] \qquad \text{for } C_1R_1 > C_2R_2 \text{ (Eq. 5.3a)}$$

$$\Delta\phi = \tan^{-1}\left[\frac{\frac{1}{\omega C_1 R_1} + \omega C_2 R_2}{1 - \frac{C_2 R_2}{C_1 R_1}}\right] + 180° \qquad \text{for } C_2R_2 > C_1R_1 \text{ (Eq. 5.3b)}$$

It is evident from equations 5.3a,b that the phase difference of 90° is achieved as long as the ratio of the two time constants is very close to 1. Therefore, the tracking of R's and C's is critical to insuring that the 90° phase shift is within the desired ±3° error. The graph of figure 5.3 shows the phase difference between the I and Q outputs calculated as a function of the time constant mismatch, $\Delta\tau/\tau$. Since the mismatch between Rs and Cs are each around ±1%, then it is evident that the time constant mismatch is approximately ±1%. Therefore, the graph indicates that time constant

mismatch can cause around ±0.3° of error from the nominal 90° phase difference.

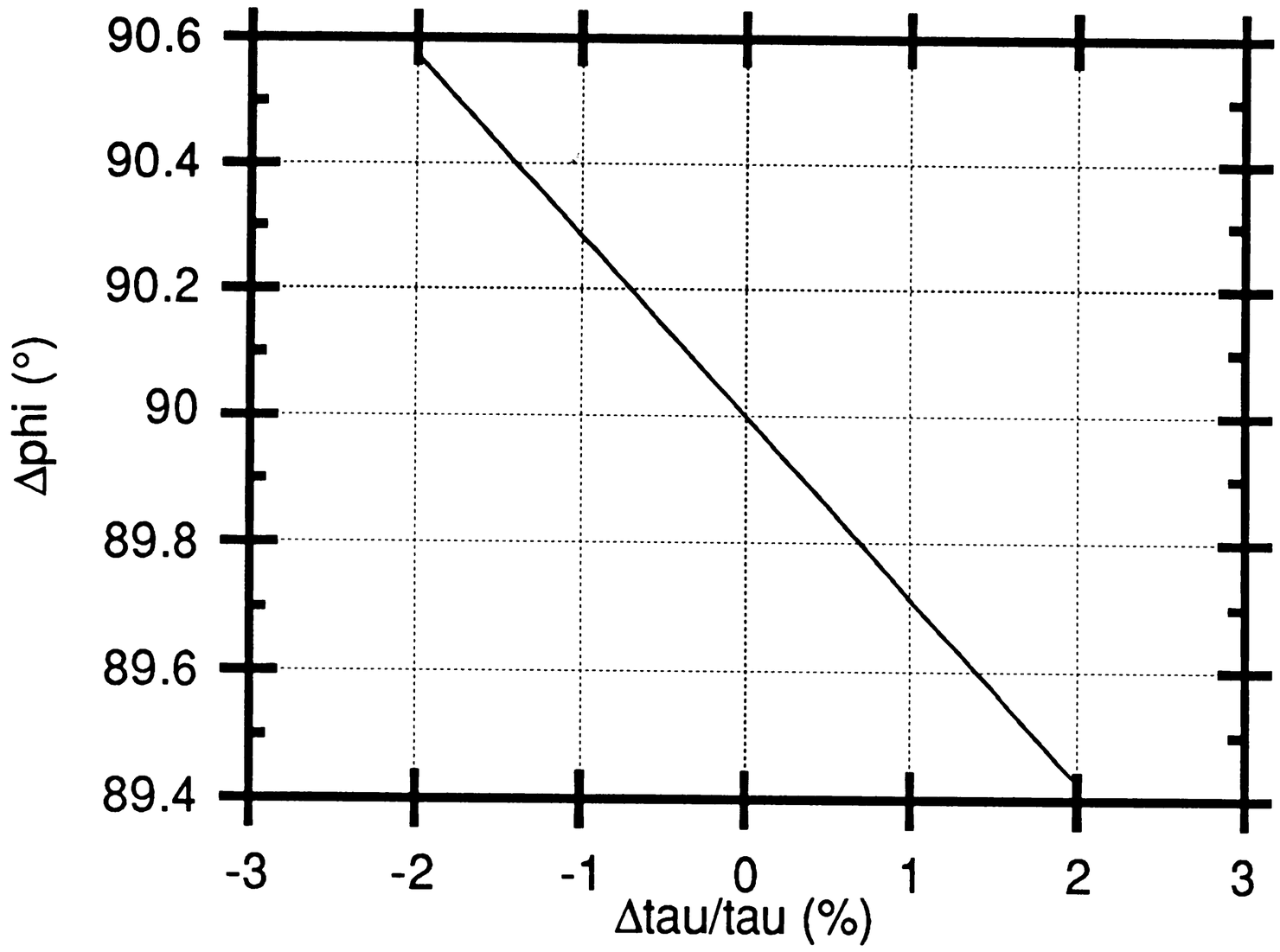

Figure 5.3: Phase Shifter Phase vs. Time Constant Error

The graph of figure 5.4 shows the phase of the I and Q outputs versus frequency, as found from equations 5.1 and 5.2, as well as the phase difference between I and Q. The graph demonstrates the ability of the phase shifter circuit to maintain a constant 90° phase difference over a wide band of frequencies. Since the magnitude of the phase shifter outputs are also a function of frequency, it is not realistic for the phase shifter to be operated over such a wide band. This is so because the amplitude imbalance between the I and Q outputs increases as the operating frequency deviates from the nominal operating frequency that was used to calculate the RC values of the phase shifter. An amplitude imbalance can cause the mixer output levels to be imbalanced if the phase shifter circuit is used without some amplitude compensation. The limiting amplifier, to be discussed in the next section, provides the needed compensation by amplifying and clipping the I and Q outputs.

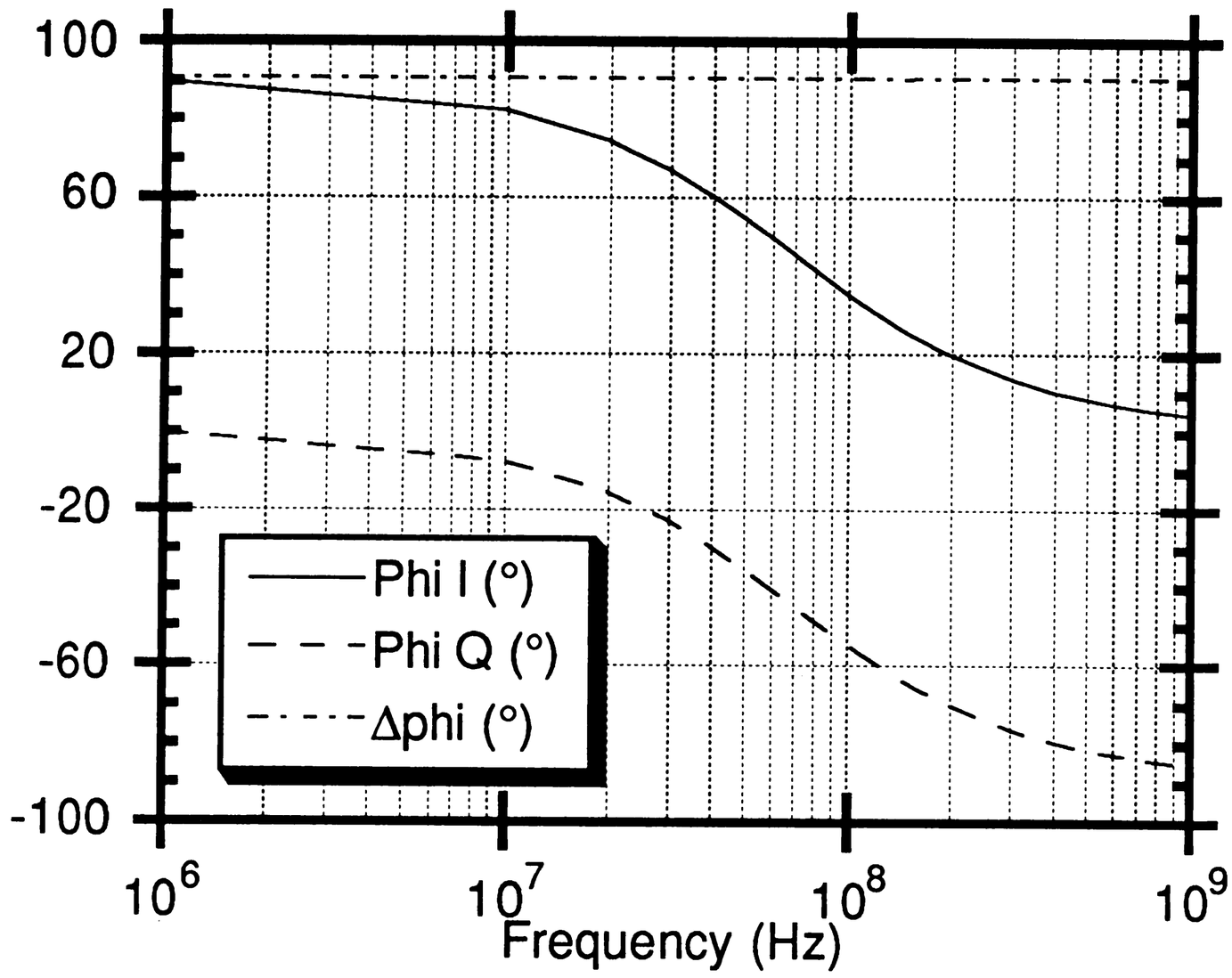

Figure 5.4: Phase Shifter Output Phase vs. Frequency

The temperature dependence of the RC time constants should also be considered in calculating the phase shifter error. However, data does not exist for the temperature coefficient of the tracking error for resistors and capacitors in the CBIC-U process being used. Therefore, phase shifter errors due to temperature may be neglected [10].

Parasitic resistances and capacitances on the I and Q phase shifter outputs can result in deviations from the desired 45° phase shift for each output. However, if the circuit layout is symmetrical, then the parasitics should be approximately equal. It can be shown that, with equal parasitics, the phase difference between the I and Q outputs will remain at 90° [10]. Thus, no phase difference error is contributed by layout parasitics. The deviation from the I and Q nominal phase shifts is not a problem, since the most important requirement is the 90° phase difference that is required for quadrature demodulation.

5.3 Limiting Amplifier Design

A limiting amplifier is connected on each of the I and Q outputs of the RC phase shifter circuit as shown in figure 2.3. As discussed previously, the limiting amplifier is intended to provide a constant amplitude signal to the switching inputs of the two mixers in the circuit. Therefore, each limiting amplifier should provide a square wave signal whose amplitude is significantly greater than $2 \cdot V_T$ to the switching inputs of the I and Q mixers. This signal will cause the mixers to switch as if a square wave signal was applied to the mixer with an amplitude swing of +1 to -1. As described in section 4.2.1, the mixer gain will, therefore, be independent of phase shifter amplitude.

The limiting amplifier circuit, as shown in figure 5.5, consists of a differential amplifier with cascode transistors and a limited output swing and two emitter follower output stages.

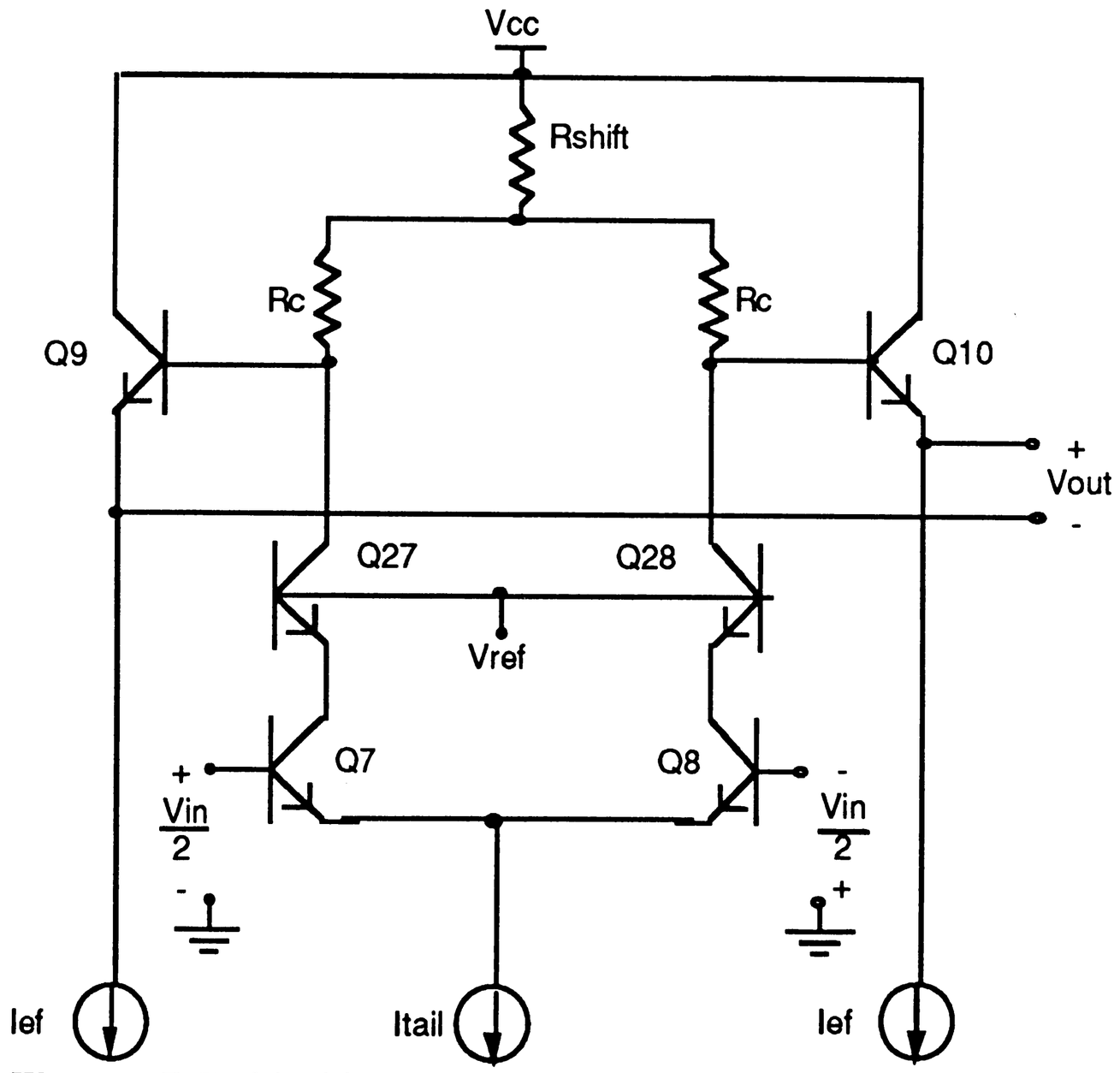

Figure 5.5: Limiting Amplifier for Phase Shifter Circuit

The differential pair, Q7 and Q8, of the limiting amplifier operates in the same manner as the differential pairs of the IF amplifiers. The difference lies in the limited differential voltage swing that is set by the voltage drops across the R_C resistors, which is equal to $I_{tail} \cdot R_C$. With a gain of $g_m \cdot R_C$, the differential pair amplifies the minimum LO input signal of 100 mVpp that is ultimately applied to the inputs of the limiting amplifier. To achieve limiting, the differential voltage swing limit must always be less than the differential pair gain multiplied by the minimum LO input signal.

As mentioned previously, for full switching to occur in the mixer, the output of the limiting amplifiers must be much greater than $2 \cdot V_T$. Since $2 \cdot V_T$ is approximately 52 mV, then setting the nominal voltage swing limit to 300 mV should be sufficient to provide a square wave output and to fully switch the mixers under all conditions. Now, given the desired voltage swing limit of 300 mV, the amplifier's gain may be found to be equal to 5.8 V/V. Therefore, limiting will occur since the voltage swing limit of 300 mV is less than the gain-minimum input signal product of 580 mV.

The level shifting resistor, R_{shift}, shifts the limited voltage swing of the differential pair down by a voltage equal to $I_{tail} \cdot R_{shift}$. This is done to set the DC component of the limiting amplifier output so that the Gilbert cell transistors of the mixer stage won't go into saturation.

Transistors Q27 and Q28 make the differential pair into a cascoded differential amplifier. The cascode transistors were added to minimize the effects at high frequency of Miller multiplication on the base-collector capacitor, C_μ. Since the value of C_μ is modulated with the voltage across the base-collector junction and the Miller multiplication effect pronounces this modulation, then the parasitic capacitances due to C_μ on each side of the RC phase shifter circuit may be different as a result of the differing voltage due to the phase shifting. Therefore, by reducing the Miller effect, the effects of the modulating capacitance will be reduced. Since, as mentioned previously, only equal parasitics on the output of the phase shifter are cancelled, then this circuit addition reduces the parasitics due to C_μ and is

critical in maintaining the 90° phase shift between the I and Q outputs of the phase shifter.

5.4 Simulation Results

The phase shifter simulations, as mentioned in section 4.5, were performed in conjunction with the mixer circuits. Taking into consideration that the simulations performed were on a non-linear circuit (mixer) and that the signals used in the simulations were significantly lower in frequency than the actual operating signals, then the ADVICE [7] simulations for these results are also considered to be somewhat inaccurate. As determined from the raw data of simulations over temperature and processing variation cases as shown in appendix 2, the final output phase difference was found to be 87.2° for the nominal and minimum values, while the maximum phase difference was found to be 93.4°. This results in a phase difference spread of ±3.1°. This is close to the desired phase variation limit of ±3°, but since the accuracy of ADVICE [7] for these simulations is in question, then the results are essentially inconclusive.

6. Digitally Controlled Bandgap Voltage Reference

The bandgap reference, as stated in section 2.7, must provide stable voltages for setting up current mirrors and reference levels throughout the integrated circuit. In addition, the bandgap must be capable of being switched by digital control. This feature is needed to have the ability to switch the entire circuit's power dissipation to zero on demand.

The first section will discuss the bandgap design and it's enable/disable mechanism. Section 6.2 will show the reference voltages that were required and how they were designed. Sections 6.3 and 6.4 will discuss the temperature dependant and independent current mirrors, respectively. Section 6.5 will present the saturating transistor circuit that was used to switch off the emitter followers of the circuit. The final section will discuss the simulation results that were obtained for the bandgap's operation.

The circuit shown in figure 6.1 consists of the digitally controlled bandgap circuit with it's voltage and current reference outputs.

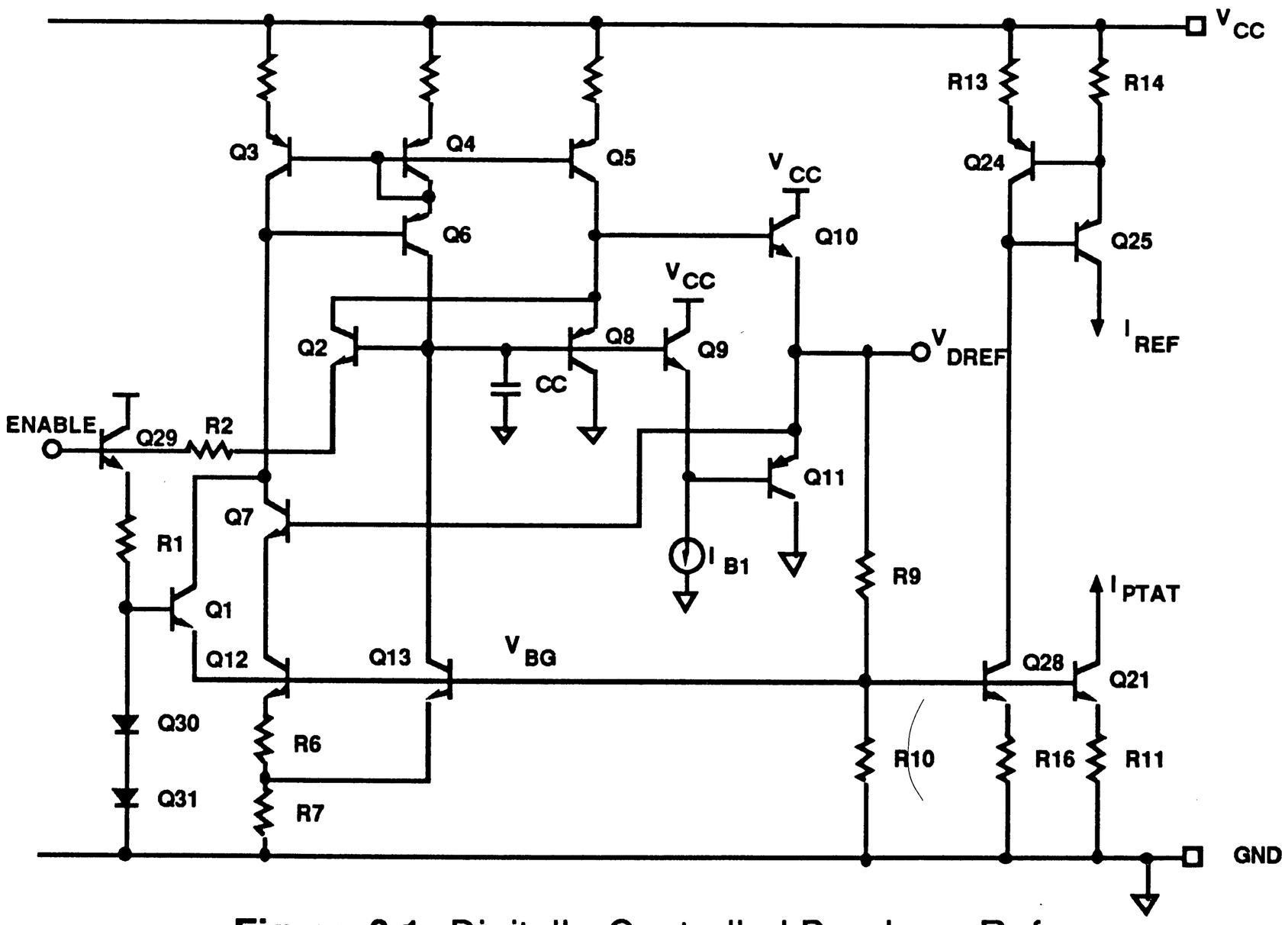

Figure 6.1: Digitally Controlled Bandgap Reference

6.1 Digitally Controlled Bandgap Design

The core bandgap circuit is essentially a Brokaw bandgap reference circuit [11] consisting of transistors Q12 and Q13 with resistors R6 and R7. The Wilson current mirror [13], consisting of transistors Q3, Q4, and Q6, causes the collector currents of Q12 and Q13 to be equal to each other. Since the emitter areas of transistors Q12 and Q13 are different and the collector currents are equal, then a voltage difference between the two V_{be}'s of Q12 and Q13 will exist across resistor R6. Therefore, a current, which is set up by the V_{be} difference and is proportional to V_T, will flow through R6. This current, added to the current flowing through Q13, will cause a voltage drop across R7. The sum of the voltage drop across R7 and the V_{be} of Q13 will equal the bandgap voltage, V_{bg}. This voltage is set to be approximately 1.25 V, which is close to the bandgap of silicon. From the analysis of the basic bandgap circuit shown in Grey & Meyer [6], it is seen that this type of circuit, whose voltage is the sum of a V_{be} and a term proportional to V_T, provides a reference that is relatively constant over a wide range of operating temperatures.

The switching circuitry consists of some of the other transistors shown in figure 6.1. In the start-up circuit, transistors Q8 through Q11 make up a unity gain buffer whose output helps to set up a reference voltage and is also fed back to transistor Q7. In addition, transistor Q1 acts as the catalyst of the start up circuitry. When turning on the bandgap, if the ENABLE input is high, then Q1 will turn on. As Q1 turns on, the bandgap reference will also begin to turn on as voltage is dropped across R6 and R7 and current is drawn through Q1 from the Wilson current mirror. As this occurs, the unity gain buffer will cause Q7 to fully turn on. When the startup is completed, the transistor Q1 is starved of current and will turn off. Transistors Q30 and Q31 and resistor R1 determine the level at which Q1 will turn on the bandgap.

To turn off the bandgap reference, the ENABLE input is brought low and transistor Q2 turns on. With Q2 on, the current that was previously driving Q8 of the unity gain buffer is shunted through Q2. This causes the output of the

buffer to fall, which in turn, causes Q7 to start turning off. As Q7 turns off, the Wilson current mirror is starved of current and causes the bandgap reference to turn off while, at the same time, the current through Q2 is turned off. Thus, when the turn off process is complete, the bandgap is completely shut down and no current is drawn from the supplies.

6.2 Reference Voltage Design

Although not mentioned specifically in the previous sections, the design required two reference voltages primarily to set the DC levels for capacitively coupled inputs. For instance, the input to the first stage of the IF amplifier is capacitively coupled and requires a DC level of approximately 2.5 V that is fairly constant over temperature. This reference voltage is shown as V_{DREF} in the circuit of figure 6.1 and the remaining connections to V_{DREF} are shown in the complete schematics of appendix 7. An additional voltage, V_{REF}, is required to set the DC level of the input to the second IF amplifier stage. V_{REF} should be equal to approximately 3.25 V.

V_{DREF} is determined by using V_{bg} to set up a current in resistors Q10 and Q9. The values of R9 and R10 are set so the voltage at node V_{DREF} will be equal to 2.5 V. Since the bandgap voltage, V_{bg}, is constant with temperature, the only temperature variation of V_{DREF} will be due to the temperature coefficient of the resistors.

The reference voltage V_{REF}, is set up with a buffer that provides an upward level shift equal to one V_{be} from the voltage V_{DREF}. Therefore, the output is approximately 3.25 V. This simple buffer circuit is only shown in the complete schematics of appendix 7.

6.3 Temperature Dependent Current Mirror Design

The temperature dependent current mirror is designed to have an output current that is proportional to absolute temperature (PTAT). This temperature dependency is obtained by deriving the I_{PTAT} current from the temperature dependency of a transistor's V_{be}, which is commonly known to be approximately -2 mV/°C [6]. The circuit of figure 6.1 shows the I_{PTAT} output,

which is obtained by applying the constant-with-temperature bandgap voltage, V_{bg}, across the V_{be} junction of transistor Q21 and resistor R11. The negative temperature coefficient of the V_{be} voltage and the assumed constant temperature coefficient of the resistor yields a current through Q21 that has a positive temperature coefficient and is also proportional to absolute temperature.

6.4 Temperature Independent Current Mirror Design

The temperature independent current mirror, whose output is shown in figure 6.1 as I_{ref}, uses the same principle as the PTAT current mirror, but with an additional V_{be} in the loop. As may be seen from figure 6.1, a PTAT current drives transistor Q24 and resistor R13. The voltage across R14 and the V_{be} junction of Q24 will yield a net zero volt per degree Celsius temperature coefficient since the positive temperature coefficient of the PTAT current is cancelled by the negative temperature coefficient of the V_{be} junction of Q24. Thus, with this voltage across R14, the current I_{ref} is obtained with a zero temperature coefficient. This also assumes a zero resistor temperature coefficient along with equal V_{be} temperature coefficients for NPNs and PNPs.

6.5 Saturating Transistor Design

The saturating transistor, as shown in figure 6.2, provides a low voltage, that is equal to approximately 0.2 V, to the "grounded" end of the load resistors in the emitter follower circuits that are found in the IF amplifiers and mixers. When the bandgap is on, the node V_{ST} provides a near ground voltage and a current sink for normal operation of the emitter follower load. When the bandgap is off, the voltage V_{ST} is disabled and current is no longer sunk from the emitter followers.

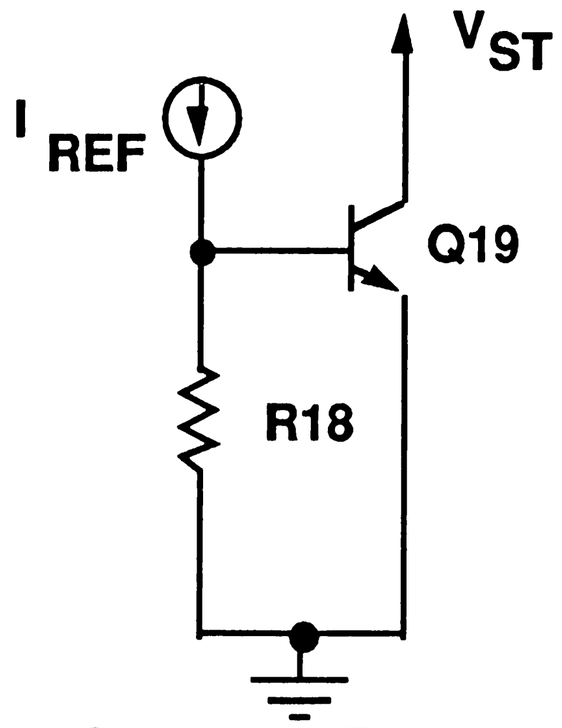

Figure 6.2: Saturating Transistor Schematic

With the bandgap voltage active, the current I_{ref} is mirrored and drives resistor R18. This resistor is large enough so that when I_{ref} is on, the voltage across the V_{be} junction of transistor Q19 is also large. This causes Q19 to go into saturation and as a result the V_{ce} voltage across Q19 drops to about 0.2 V. When the bandgap reference is turned off, the current I_{ref} is also turned off. Therefore, the transistor Q19 is also turned off, leaving no place for the emitter followers' current to sink.

6.6 Simulation Results

A graph of the bandgap reference's voltages and currents versus temperature is shown in figure 6.3.

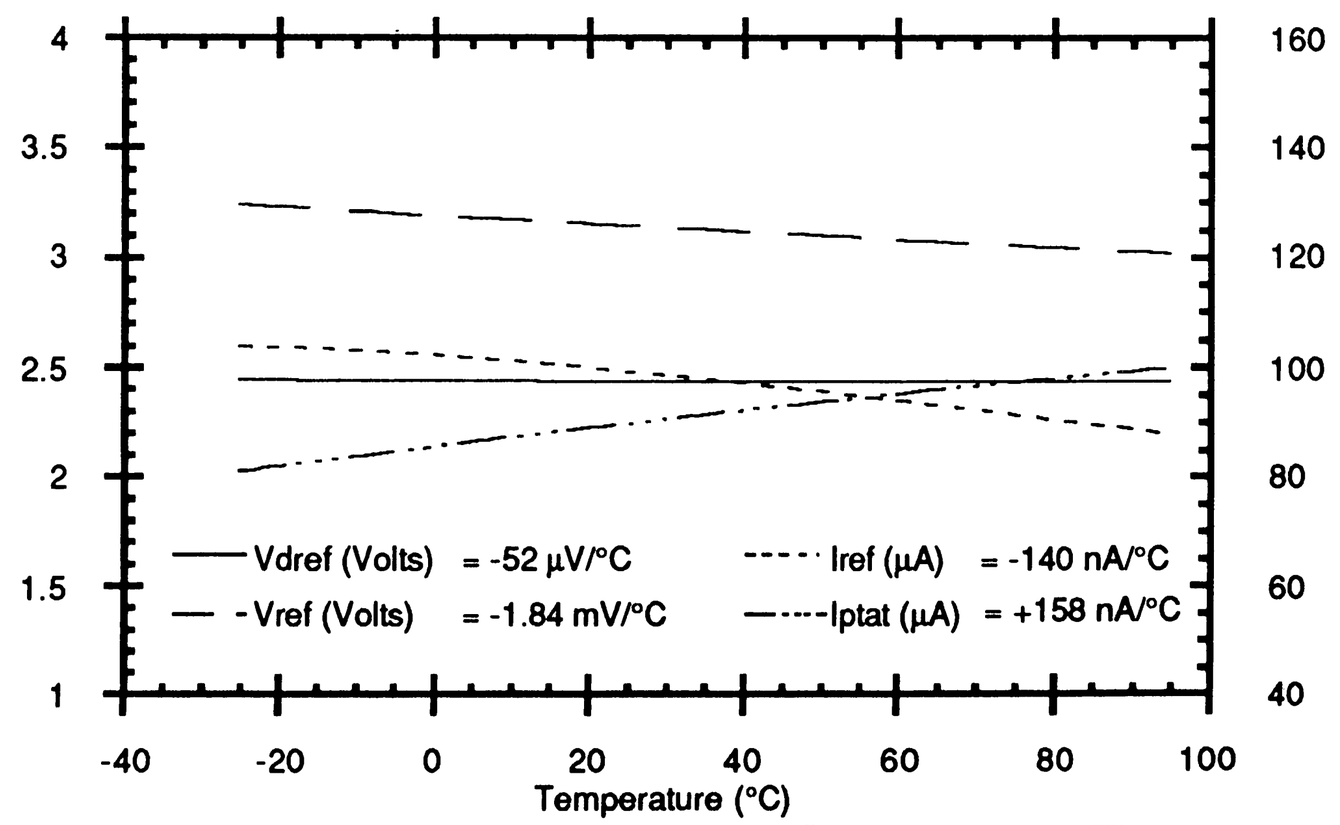

Figure 6.3: Bandgap Voltages and Currents vs. Temperature

The graph indicates that the voltage V_{dref} is nearly constant over temperature with a temperature coefficient of only -52 μV/°C. This slight coefficient may be attributed to resistor temperature coefficients in the circuit. The voltage V_{ref} demonstrates a temperature coefficient of -1.84 mV/°C. This coefficient is due to the temperature coefficient of a V_{be} junction in the buffer that was previously mentioned.

The proportional to absolute temperature reference current, I_{PTAT}, demonstrates a +158 nA/°C temperature coefficient that appears to linearly increase with temperature. Thus, this current is performing as intended. The current I_{ref}, on the other hand, appears to exhibit a temperature coefficient of -140 nA/°C that is somewhat unexpected. As noted previously, the goal of obtaining a zero temperature coefficient is dependent upon a zero resistor temperature coefficient and V_{be} temperature coefficient matching between NPNs and PNPs. Thus, the simulated results indicate that these assumptions may not necessarily be valid. It appears that the V_{be} temperature coefficient of PNPs is somewhat more negative than the temperature coefficient for the NPNs. Also, the positive temperature coefficients of the resistors may be adding some excess negative slope.

Simulations of the bandgap reference in the off (or sleep) mode were also performed. It was found that total sleep mode supply current was no higher than 273 nA and as low as 15.3 nA. The complete results of these simulations may be found in appendix 3.

7. Implementation and Experimental Results

The process of finalizing the design of the IF Amplifier / Demodulator and realizing the circuit in silicon involves several tasks. This chapter will address this process. Section 7.1 will explain some additions to the circuit that were needed to interconnect the blocks of the circuit. The layout of the circuit will be presented in section 7.2 while the selection of packaging will be discussed in section 7.3. DC simulation results of the full chip will be presented in section 7.4. Section 7.5 will present the experimental results and will also discuss the circuit required to test the integrated circuit at it's operating frequency The experimental results will include DC results, gain and phase, noise, and switching speed. Also, the circuit problems that were discovered as a result of the testing of the manufactured silicon will be discussed in section 7.6.

7.1 Implementation of Block Diagram

The construction of the full circuit from each of the block diagrams required some additional components. In addition, two components were added to the design so that low frequency wafer probe testing would be possible. A set of complete circuit schematics are shown in appendix 7.

In order to provide a voltage reference at the inputs of capacitively coupled amplifiers, resistors were added between the inputs and a reference voltage from the bandgap. The differential inputs of the 24 dB/0 dB amplifier were connected to the DREF reference voltage through 4 kΩ resistors. In addition, since the input of the 24 dB/0 dB amplifier is designed to be single ended, the negative input of the DGSDA subcircuit (figure 3.2) is connected to ground through a 32 pF capacitor, thus providing an AC ground on this side of the amplifier. The 12 dB/0 dB amplifier and the two mixers also have 10 kΩ resistors connecting their inputs to the DREF reference voltage. This is required due to the 32 pF coupling capacitors before these inputs.

The need to determine functionality at the wafer testing stage requires the ability to test for signal gain through the IF amplifier stages. Therefore, a method was found to measure an AC signal at the quadrature mixer inputs.

This was accomplished by connecting the base of a PNP transistor to each of the differential mixer inputs. The collectors of the transistors were connected to ground while the emitters each went to separate bond pads. This addition to the circuit provides the ability to design an emitter follower by adding a resistor from the bond pad to Vcc. The emitter follower outputs may then be used to measure the signal levels at the mixer inputs. This technique provides a method of measuring a low frequency signal without adding the large bond pad capacitance as a parasitic directly on the mixer inputs. If the mixer inputs were tied directly to bond pads for testing, the parasitic capacitance may have provided a significant loss in the signal path when the circuit was used at it's normal operating frequency.

7.2 Layout

The layout of the circuit is one of the most important portions of the circuit design process for a high speed integrated circuit. Thus, care was taken to minimize layout problems wherever possible. The use of a linear array causes some problems to be inevitable. Increased parasitic capacitance and less than optimal device matching are traded off for the low-cost and fast processing benefits that a linear array allows.

With this design, efforts were taken to minimize the number of components so that each block would fit in a tile of the linear array. This was not always possible. Some components of each functional block had to be connected from adjacent tiles. As a result, some nodes had higher layout capacitance than desired.

Where thermally matched devices were required, components were found adjacent to each other as much as possible. This was not a real problem for this design since each of the IF amplifiers and each mixer were designed to require only the components available on a single tile.

A chip photomicrograph of the manufactured circuit is shown in appendix 5.

7.2.1 Floor Plan

The layout floor plan is shown in figure 7.1. The IF signal flow through the chain of amplifiers and to the mixer is such that the output of one stage feeds the input of the next on adjacent tiles. This minimizes the parasitic capacitance and crosstalk. The large coupling capacitors that were used in the IF amplifier / mixer chain were obtained from the left edge of the array (not shown in figure 7.1). Also, the large bypass capacitors used at the negative side of the IF input and in the phase shifter buffers were taken from the right edge of the array (also not shown in figure 7.1).

The mixer output stages were placed on tiles in the right hand corners of the layout. These tiles are "power tiles" which contain some of the larger transistors in the array. Since the signals from the mixers to the mixer output stages are at low frequencies, then parasitic effects shouldn't be a problem. The experimental results indicate that crosstalk between these connections and the power supply lines may be a problem, but avoiding this was impossible given the limitations of the array.

The phase shifter needed to be separated between two tiles due to it's large number of components. The placement was selected so that the mixers would be adjacent to outputs of it's corresponding side of the phase shifter. The remaining two tiles were used for the bandgap circuitry.

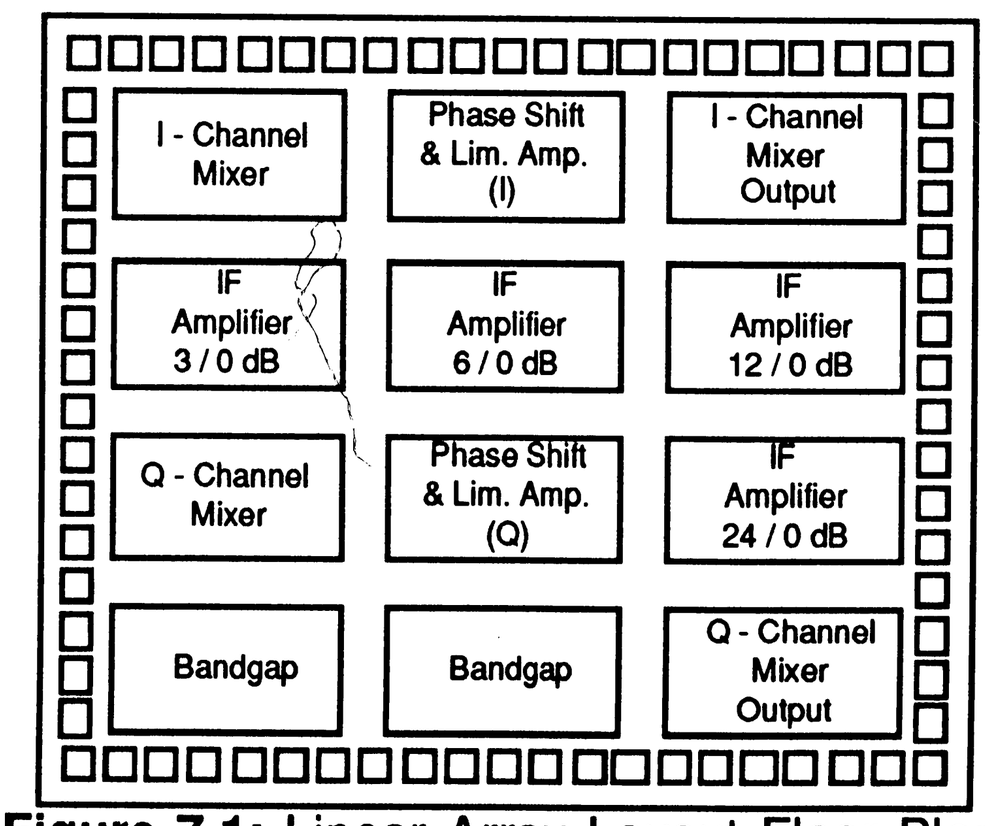

Figure 7.1: Linear Array Layout Floor Plan

7.2.2 Pad and Pin Selection

The selection of the pads on the layout and the pinout of the package were defined by two major factors, the layout of the array and the marketing needs of the device. Since the use of the linear array restricted the placement of tiles to only a few options, the selection of pad placement was somewhat fixed once the floor plan had been selected.

For the high frequency IF and LO inputs, the pads were placed as close to the input transistors as possible. For the Vcc and Ground pads, they were placed so as to minimize lead inductance and to meet the marketing needs of the package pinout. The I channel output pads were placed as close as possible to the output transistors, while the Q channel output pads were required to cross the chip vertically so as to keep the I and Q channel outputs together on the same side as the package pinout.. The gain select pad placement was chosen to accommodate the desired pinout of the package. The pinout of the package is shown in figure 7.2.

7.3 Packaging

The package selected to house the chip was a plastic small outline gull wing (SOG) package. The package was selected because of it's low lead inductance, low vertical profile and small footprint The low lead inductance is important because of the circuit's high frequency operation, while the low vertical profile and small footprint is desired since this circuit may be used in hand held portable cellular telephones, where board space is at a premium.

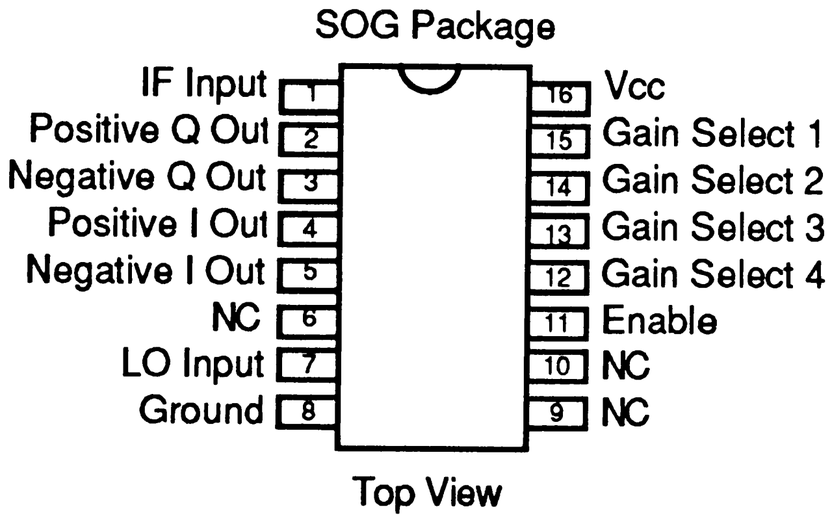

Figure 7.2: Pin Configuration

7.4 DC Simulation Results

This section presents the simulation results that were not covered in the previous discussions of the individual circuit blocks. The results shown here

are for the relevant DC parameters that were discussed in section 2.2 as requirements for the circuit's proper operation in the GSM digital cellular system.

Table 7.1 shows the simulated active and sleep mode supply currents, gain select and enable input currents, IF and LO input impedances, output impedances, and the common mode output voltage. The nominal parameters are determined from nominal component models at nominal supply voltage and room temperature. The minimum and maximum results are derived from worst case supply voltage conditions over a temperature range of -25 °C to +85 °C. The models used to obtain these results were found from seven different worst case processing conditions that were determined from combinations of high and low parameter extremes for each type of component (e.g. one condition may be high NPN, low PNP, and high resistor characteristics). The complete listing of DC and impedance simulation results may be found in appendices 3 and 6.

Parameter	Symbol	Nom	Min	Max	Units
Active Supply Current	$I_{Vcc\ a}$	18.8	14.2	24.5	mA
Sleep Supply Current	$I_{Vcc\ s}$	0.083	0.015	0.145	µA
Gain Select Current	I_{gs}	2.5	0.84	7.8	µA
Enable Current	I_{enb}	0.62	0.21	2.5	µA
IFIN Input Impedance	Z_{ifin}	1540	581	1613	kΩ
LOIN Input Impedance	Z_{loin}	2226	1642	3107	Ω
Output Impedance	Z_{out}	24.6	16.4	40.4	Ω
Common Mode Output Voltage	V_{cm}	2.87	2.70	3.14	V

Table 7.1: Simulated DC Results

The simulated results of Table 7.1 indicate that the goals as defined in section 2.2 were met for most of the DC parameters. One exception is the active supply current. The maximum active supply current is somewhat higher than it should be to meet the 100 mW power dissipation goal. Since the maximum value is determined at the circuit's extreme worst case operating condition and the nominal supply current is well below the 20 mA level, then it is not unreasonable to expect that for most operating conditions,

the circuit will dissipate less than 100 mW. The sleep mode current is shown to be well below the 50 μA goal as defined in section 2.2.4.

The IF and LO input simulated impedances are well above the 300 Ω level required by section 2.2.4. Also, the simulated output impedance is below the 50 Ω specification as outlined in section 2.2.4.

The remaining DC simulation results, such as gain select and enable input currents and common mode output voltage, were not defined in earlier sections but do have requirements that may be mentioned here. The gain select and enable input currents needed to be as low as possible so that they may be driven without any type of external buffering. Therefore, the simulation results indicate that the current level needed to drive these inputs is in the range of a few microamps or less, which is small enough to meet the low drive current objective. The common mode output voltage needed to be at least 0.5 V from the power supply rails so as to meet the 1 Vpp output requirement without distortion as stated in section 2.2.5. Therefore, the simulated common mode output voltage indicates that this parameter is well within the requirement.

Simulated results for AC parameters, such as amplifier and mixer gain, were presented previously in the sections pertaining to each subcircuit.

Noise figure simulations of the entire circuit were performed so as to determine if the goals of section 2.2.3 would be met. The simulations showed maximum noise figures of 7.23 dB and 27.38 dB for the maximum and minimum gain settings, respectively. This is within the 10 dB and 30 dB goals of section 2.2.3.

Settling time for switching between active and sleep modes was required in section 2.2.4 to be less than 25 μs. Nominal simulation results indicated a settling time of 5 μs at room temperature. No further simulations were performed because the measurement of settling time required extremely long simulations and because the nominal 5 μs result is well below the required time.

7.5 Experimental Results

The experimental results of the manufactured and packaged integrated circuit is described in this section. First, the DC testing results are presented with average, minimum, maximum, and 1 σ values for each parameter. Also included are histograms for each of the DC parameters. Section 7.5.2 discusses the evaluation board used for RF testing of gain, phase, and other parameters. The next section presents the results of the RF testing. Figures are shown and discussed for measurements of gain (and in some cases phase) versus several different variables such as selected gain, IF input, LO amplitude, power supply, temperature, and frequency. In addition, gain and phase deviation histograms are presented and discussed. Sections 7.5.4 and 7.5.5 present data and discuss noise and switching speed experimental results.

7.5.1 DC Results

The DC testing results were obtained using an automatic test set that is commonly in use at AT&T for wafer probe testing. Simple test circuits were built to facilitate the testing through the use of a computer program. The testing was initially performed on the wafer level so as to screen bad parts before they were packaged. The results presented here were performed on packaged parts at room temperature and nominal supply voltage (25 °C and +5.0 V). The data presented was obtained from a sample size of 16 parts with the exception of the common mode output voltage which was obtained from 10 parts. The sample parts were manufactured from three different diffusion lots so as to obtain a reasonable prediction of normal production device parameter deviations. Table 7.2 lists the results for each of the tests. These results may be compared to the simulated DC results of Table 7.1.

Parameter	Symbol	Avg	Min	Max	1 σ	Units
Active Supply Current	$I_{Vcc\ a}$	18.4	17.65	19.45	0.75	mA
Sleep Supply Current	$I_{Vcc\ s}$	0.003	0 †	0.01	0.005	μA
Gain Select Current	I_{gs}	0.26	0.2	0.32	0.036	μA
Enable Current	I_{enb}	0.13	0.11	0.18	0.02	μA
IFIN Input Impedance	Z_{ifin}	3771	3503	4008	154	Ω
LOIN Input Impedance	Z_{loin}	2464	2255	2603	117	Ω
Output Impedance	Z_{out}	43.2	35.89	49.47	3	Ω
Common Mode Output Voltage	V_{cm}	2.89	2.86	2.91	0.17	V

† Below resolution of test equipment

Table 7.2: Measured DC Results

The active supply current, LO input impedance, and common mode voltage average values are very close to the simulated nominal values as shown in Table 7.1 and their measured minimums and maximums are well within the simulated limits. Therefore, for these parameters it is evident that the circuit is operating within it's defined specifications.

For the sleep mode supply current and the IF and LO input currents, the measured results were below the simulated predictions. This is not a problem since for each of these parameters, the lowest current level possible was desired. The differences may be explained by assuming that low current levels such as these may be difficult for ADVICE [7] to predict accurately and that the automatic test equipment's ability to test such low currents are somewhat inadequate. In addition, the measured IF input impedance is significantly higher than the simulated results. This error is because simulations were performed at the operating frequency of 70 MHz so as to account for parasitic capacitive effects, while the measurements were taken at DC with the automatic test equipment. Also, the measured output impedance is somewhat higher than simulated. This may be due to the numerous difficulties that were encountered in making this measurement.

The following five figures show histograms of the DC measurement data. Figures 7.3, 7.4, 7.5, 7.6, and 7.7 show the histograms for the active supply

current, IF and LO input impedances, gain select and enable input currents, output impedances, and common mode output voltage, respectively.

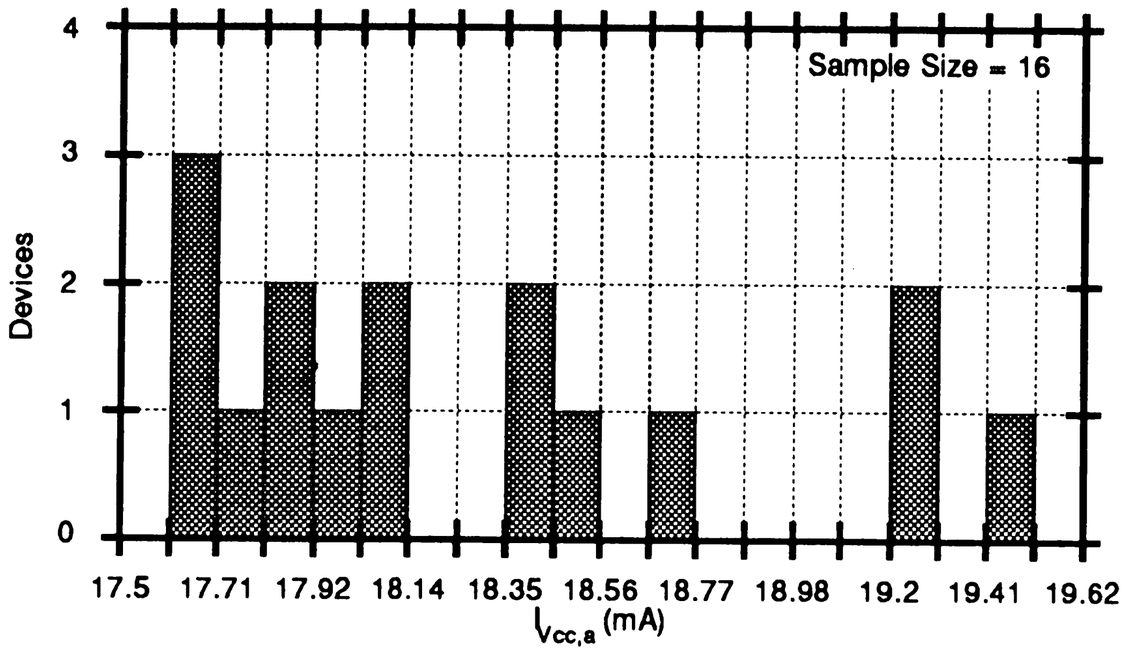

Figure 7.3: Active Supply Current Histogram

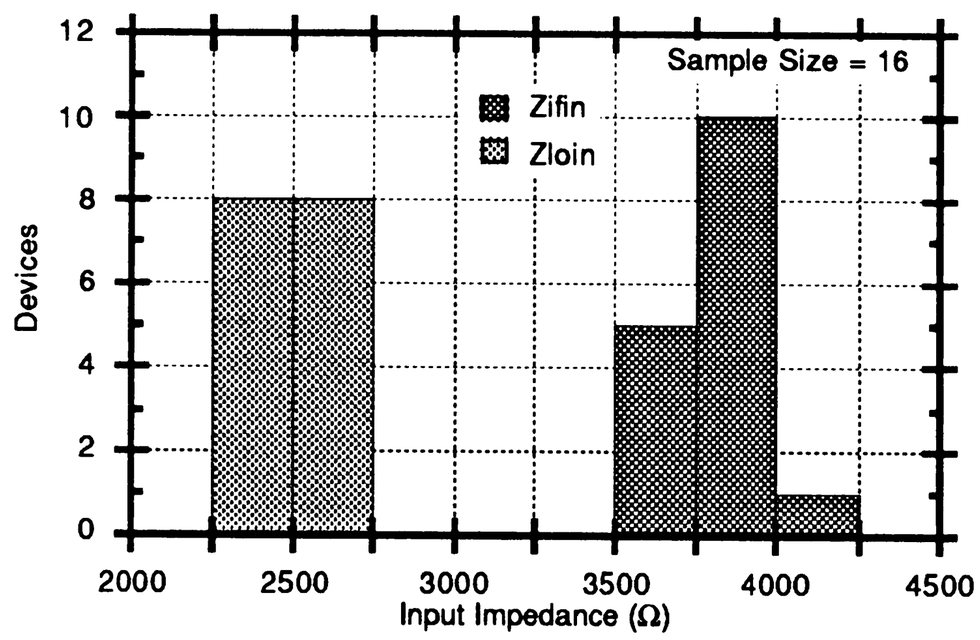

Figure 7.4: IF and LO Input Impedance Histogram

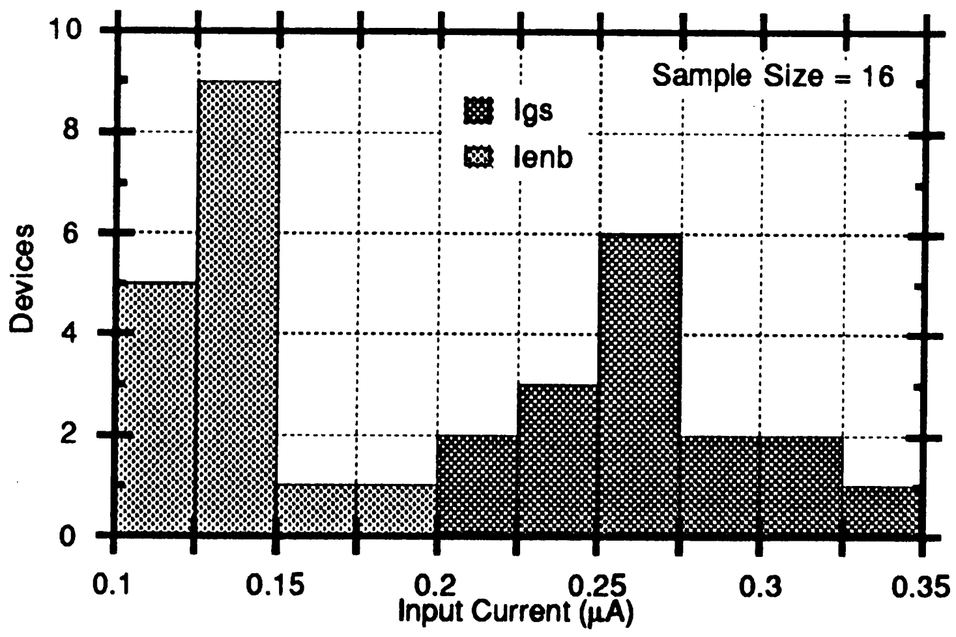

Figure 7.5: Gain Select and Enable Input Current Histogram

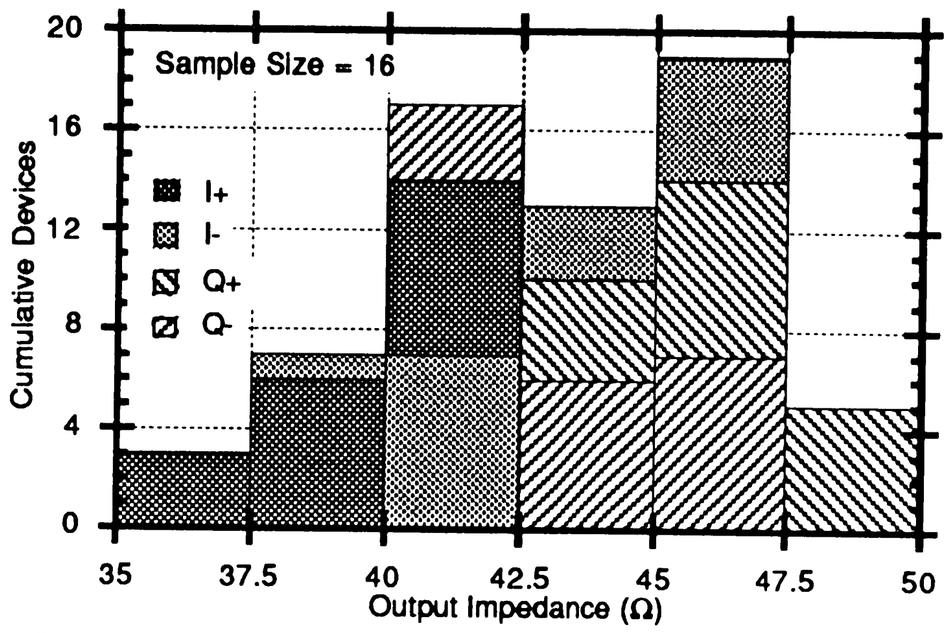

Figure 7.6: Output Impedance Histogram

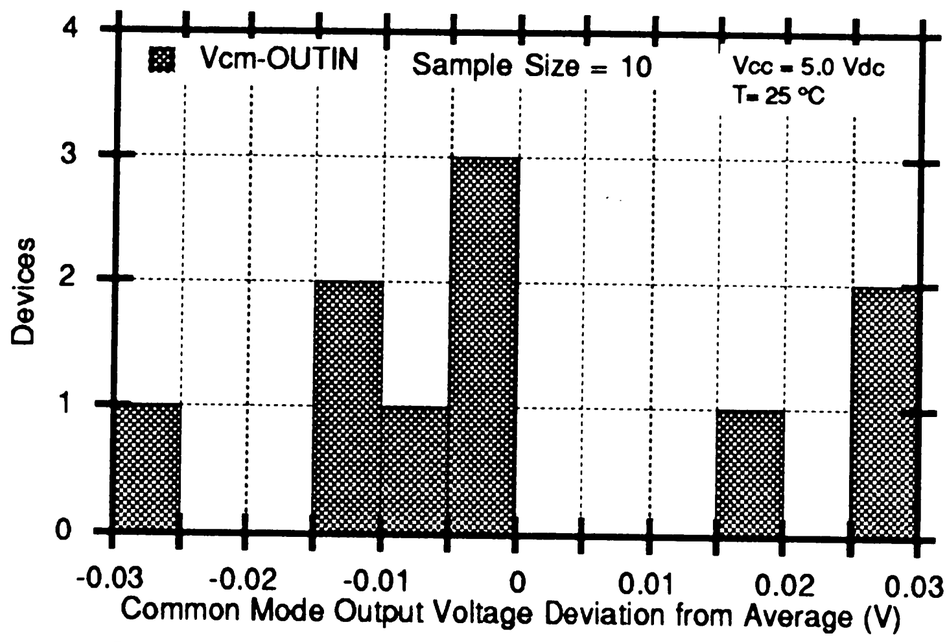

Figure 7.7: Common Mode Voltage Deviation Histogram

7.5.2 RF Evaluation Board Design

The circuit used to test RF performance and it's board layout is important, since it could effect the measurements that are being performed at the 70 MHz operating frequency. Therefore, care was taken in selecting the circuit and minimizing detrimental effects due to board layout, such as parasitic capacitances and crosstalk. The circuit used has on board 50 Ω terminations and AC coupling to the IF and LO inputs. The Vcc board connection has a ferrite bead inductor with large capacitors to ground so as to filter out any high frequency signals from the supply input to the chip. These inputs and the Ground connection were placed as close as possible to the chip in the board layout. In addition, a ground plane was provided on all unused areas of the RF evaluation board.

The I and Q mixer differential outputs drive two separate wide bandwidth op amps configured in a unity gain circuit. The I and Q outputs drive the unity gain circuits through capacitors so as to remove the DC components of the mixer outputs. Two sets of switches were used to provide the switching levels to the gain select and enable inputs of the chip. One set of switches selects between a pin input, where a switching signal from a function generator may be applied, and a switch that selects either a high or low input as derived from the Vcc and Ground connections. Figure 7.8 shows the component layout of the RF evaluation board and appendix 4 shows the schematic for the RF test circuit.

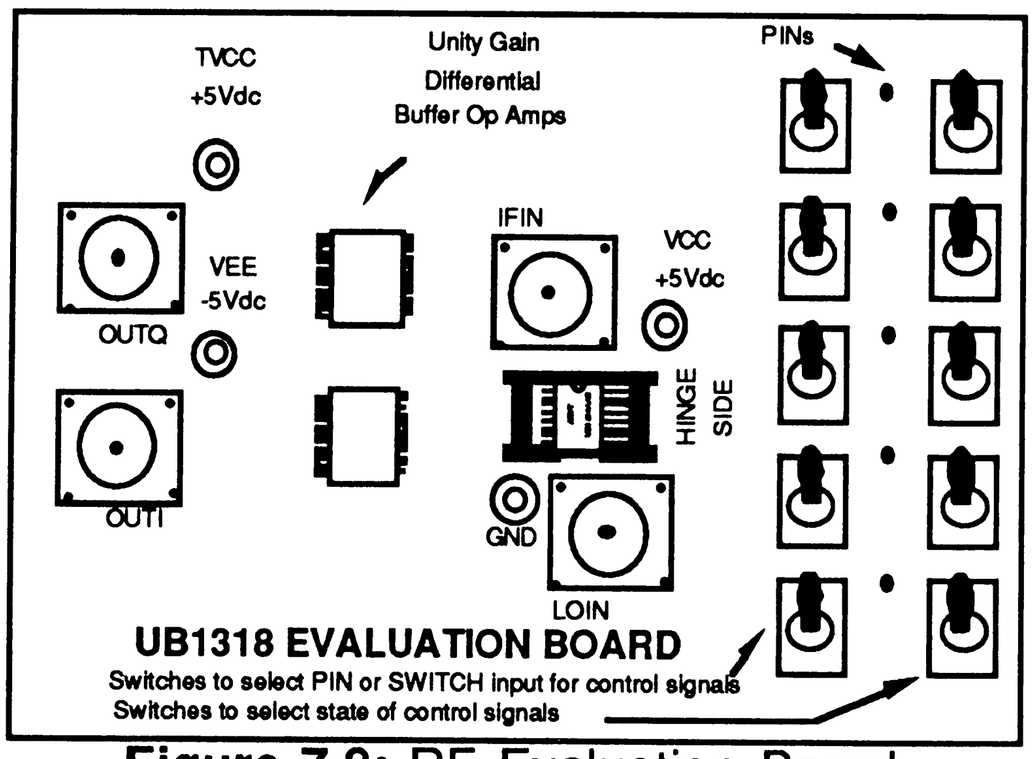

Figure 7.8: RF Evaluation Board

7.5.3 Gain and Phase Results

The measured gain error versus the selected gain setting is shown in figure 7.9. The figure indicates that the maximum absolute gain error is approximately ±0.8 dB under nominal operating conditions. This is well within the ±3 dB gain error that is required in section 2.2.2 and is also within the calculations of gain error due to processing as found in the example of section 3.1.4. A one σ band is also shown to indicate the gain error variation from samples over three separate diffusion processing lots.

The negative slope of the gain error graph may be attributed to gains above the desired level for the low gain states of each amplifier which is

cumulatively cancelled by below desired gain levels for each of the high gain states.

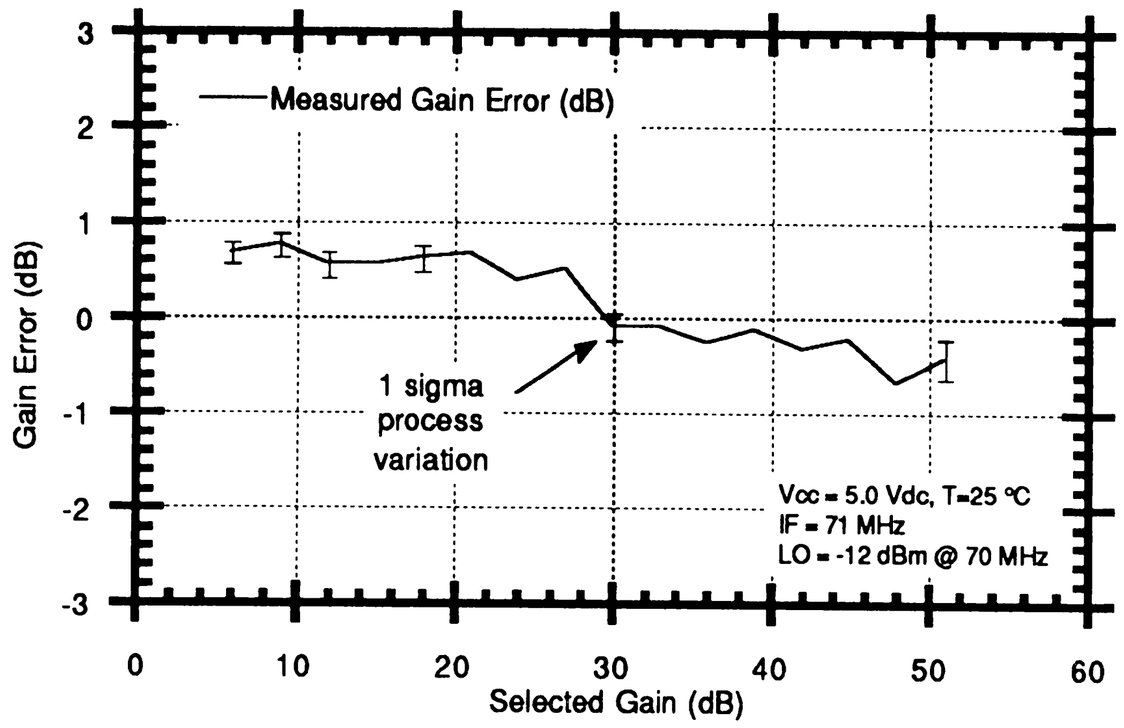

Figure 7.9: Measured Gain Error vs. Selected Gain

Figure 7.10 shows the measured gain and phase vs. temperature. This indicates that the gain is high by about 0.2 dB for low temperatures, while the gain is low by about 0.7 dB for high temperatures. The slope of the gain versus temperature curve indicates a negative temperature coefficient for the gain. Although the negative temperature coefficient due to g_m was cancelled in the IF amplifiers (section 3.1.3), there are several other temperature dependencies throughout the signal path. Negative temperature coefficients for gain are exhibited by each emitter follower stage in the IF chain, the mixer gain stage, and the limiting amplifiers. Therefore, the cumulative effects of these negative temperature coefficients can explain for the negative slope of the gain curve.

If the gain errors associated with processing from figure 7.9 and the errors associated due to temperature from figure 7.10 are taken together, then it is evident that the total gain error is within the ±2.0 dB total error as calculated using the total IF amplifier gain error of ±2.2 dB from section 3.4 and the mixer gain error of ±0.218 dB as found in section 4.4.

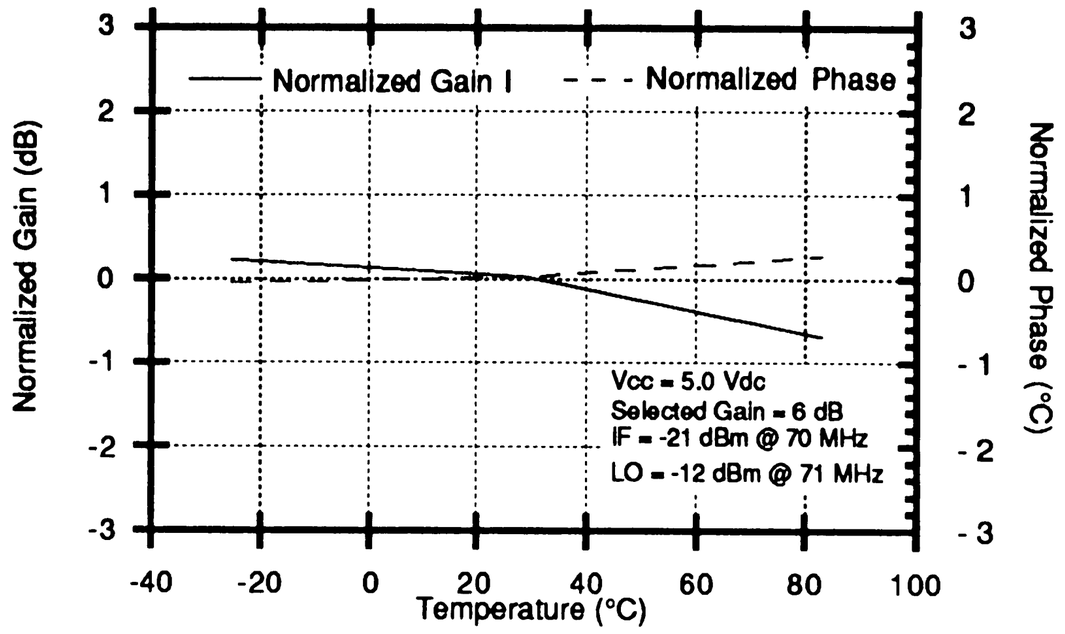

Figure 7.10: Normalized Gain and Phase vs. Temperature

The phase error vs. temperature curve of figure 7.10 shows only a slight drop in phase for low temperatures and about a 0.25 ° increase in phase for high temperatures. This is likely due to changes in the thermal matching between the Rs and Cs of the phase shifter as described in section 5.1.

The graph of figure 7.11 demonstrates the changes in gain as a function of supply voltage. The graph shows that within the specified +4.75 V to +5.25 V power supply operating range, the gain is within ±0.4 dB and the phase is within ±0.3 ° of their nominal gain and phase, respectively.

The gain errors are likely due to the voltage level shifts that are present across the emitter follower resistors in each gain stage. This causes a change in the emitter follower current. Since the emitter follower gain is proportional to the current, it follows that the gain will be proportional to the supply voltage as is shown in the measured results.

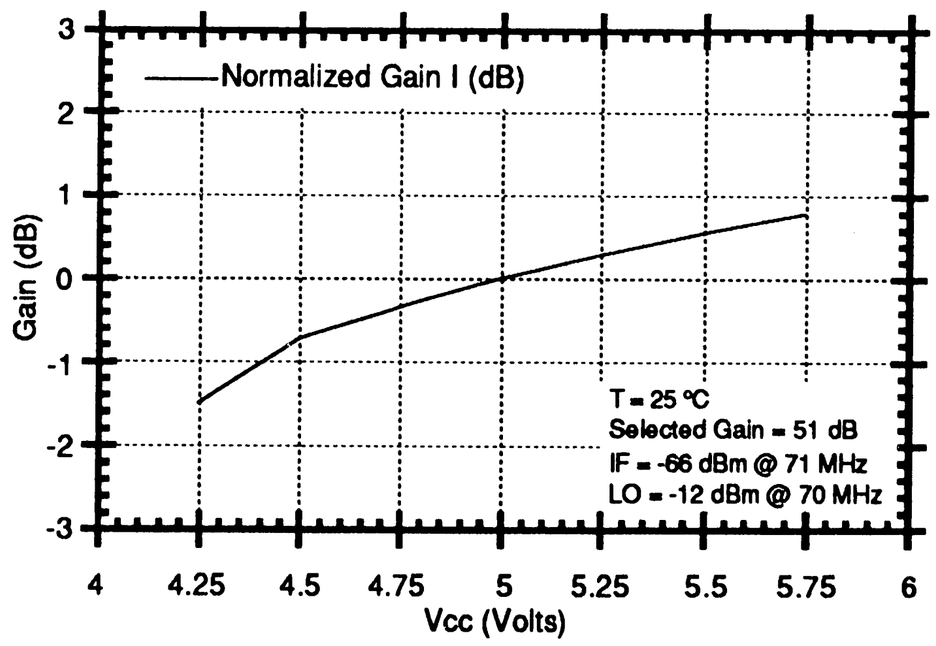

Figure 7.11: Normalized Gain vs. Vcc

Figure 7.12 shows the normalized gain and phase versus the local oscillator (LO) amplitude. This graph demonstrates the ability of the circuit to maintain it's gain level and phase difference over a range of LO amplitudes. It can be seen that the normalized gain stays within approximately 0.5 dB over a range of LO amplitudes from -15 dBm to 0 dBm. This indicates that the limiting amplifier is performing such that the gain level is only a slight function of the LO amplitude.

The phase vs. LO amplitude graph of figure 7.12 indicates a somewhat stable phase difference within a range of LO amplitudes from -15 to -5 dBm. The increase in phase for higher amplitudes is probably due to distortion from over driving the limiting amplifiers.

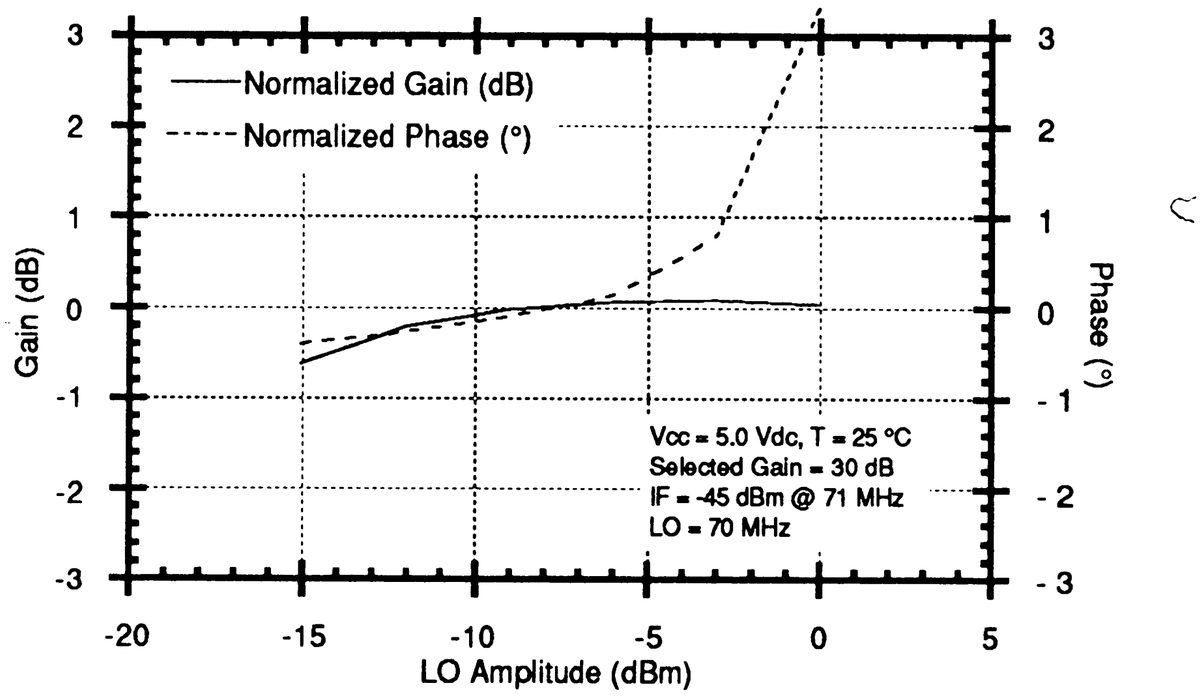

Figure 7.12: Normalized Gain and Phase vs. LO Amplitude

The normalized gain of both the I and Q channel outputs versus operating frequency is shown in figure 7.13. This graph shows that the circuit is capable of operating properly at frequencies other than the frequency at which the circuit was designed to operate. It is evident that the circuit will give adequate levels of gain at frequencies between approximately 30 MHz and 100 MHz. Above 100 MHz the gain drops off sharply due to bandwidth limitations of the IF amplifiers and below 30 MHz the gain drops off due to the increasing impedances of the coupling capacitors. The gain difference between the I and Q channels increase significantly at lower frequencies. This is a result of the change in phase from the RC phase shifters. Although the phase difference between the two phase shifters should remain close to

90 °, the amplitudes of the outputs will differ at frequencies other than the frequency at which the circuit is designed for. As a result, the input to one of the limiting amplifiers will be lower in amplitude than the other input. This eventually causes a decrease in one limiting amplifier output such that it no longer fully switches its side of the mixer. This ultimately causes a difference in output amplitudes between the I and Q channels.

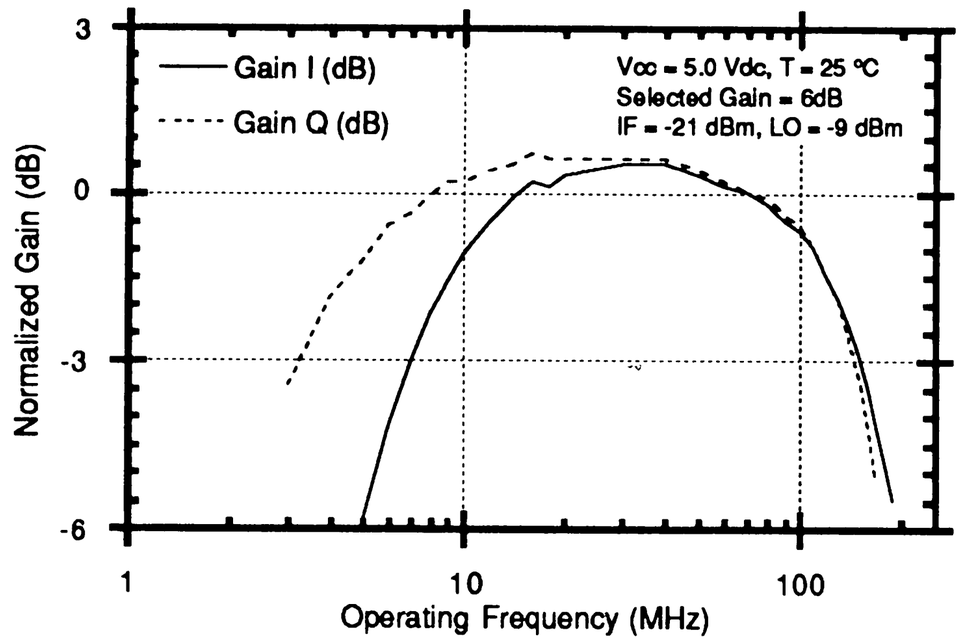

Figure 7.13: Normalized Gain vs. Operating Frequency

The normalized gains for the 6 and 51 dB settings vs. the IF input level is shown in figure 7.14. The graph demonstrates the dynamic range of the amplifiers. At the 51 dB gain level, the amplifiers are able to amplify signals down to at least -80 dBm (lowest amplitude level of the signal generator) without noise problems, while the input can go up to about -50 dBm before distortion occurs and gain drops off. For the 6 dB gain setting, IF signals are amplified without distortion with levels between approximately -35 and -5 dBm. Thus, the dynamic range of the circuit is at least 75 dB. The upper limit of the input amplitude is a function of the first gain stage output level at which distortion occurs, whereas the lower limit is determined by the noise at the amplifier's inputs.

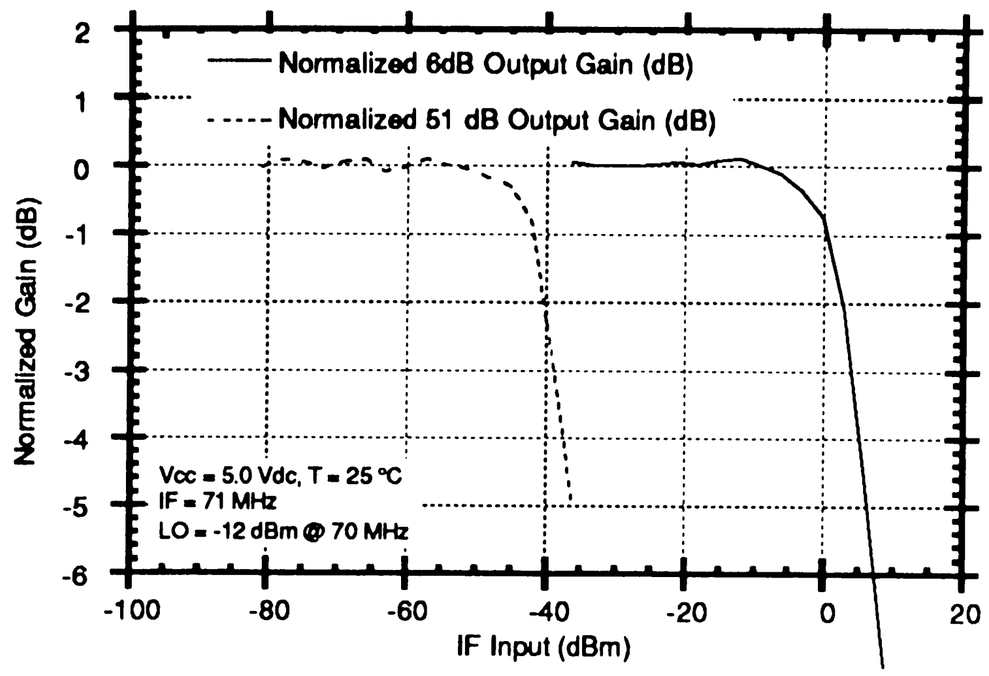

Figure 7.14: 6 dB and 51 dB Normalized Gain vs. IF Input

The gain and phase deviation histograms of figures 7.15 and 7.16, show how the deviations from average values occurred for a sample size of 10 devices that were manufactured from 3 separate diffusion lots. It is seen that the distributions are reasonably tight where the gain has a spread of about 0.7 dB around the average while the phase's distribution from average is around 1.1 °.

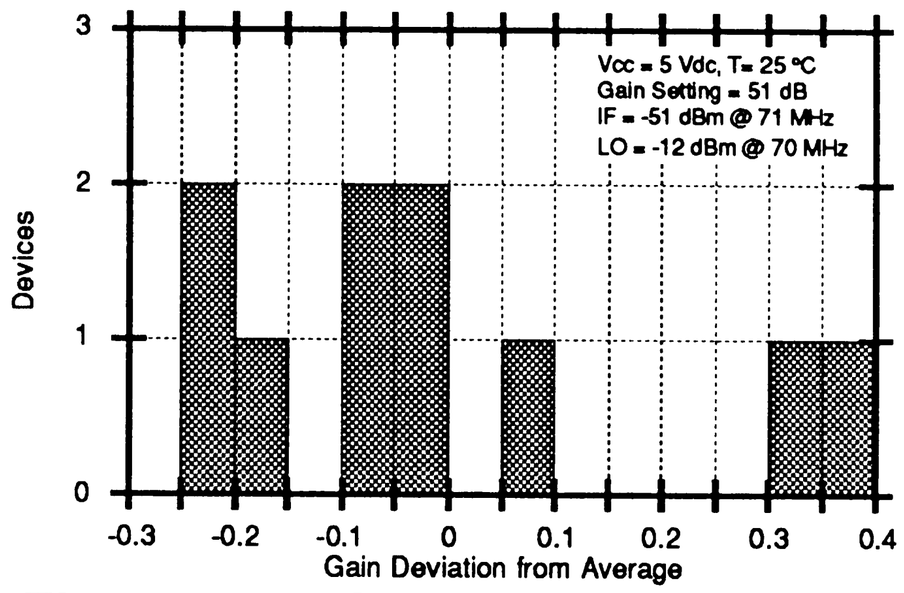

Figure 7.15: Gain Deviation Histogram

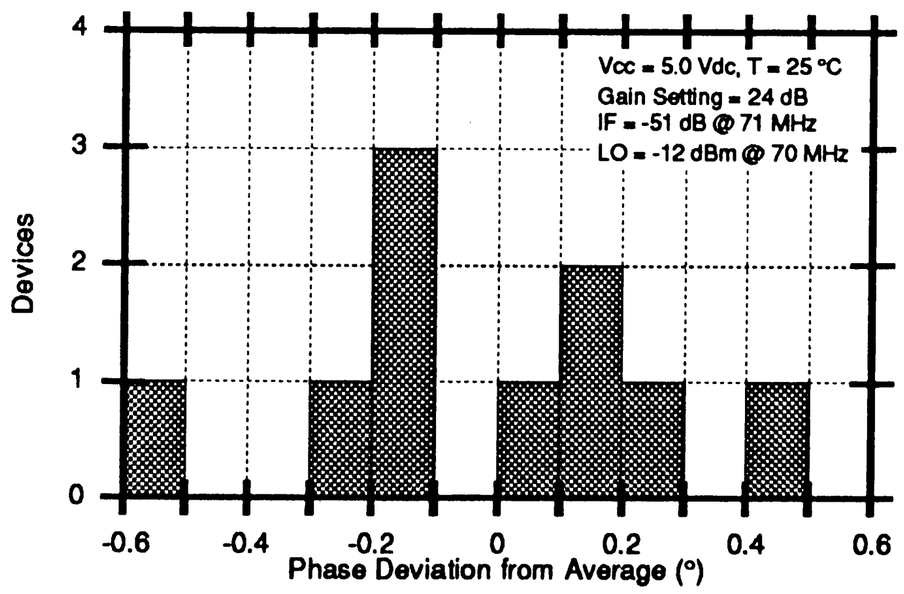

Figure 7.16: Phase Deviation Histogram

7.5.4 Noise Resuits

The noise figure of the circuit was determined experimentally by applying a 70 MHz signal to the local oscillator and no signal at the IF input. Measurements of the mixed output noise at 100 kHz were taken with a spectrum analyzer. This output noise was divided by the measured gain for each of the amplifier's sixteen gain settings so as to obtain the noise figure. This data was translated to figure 7.17 which shows the noise figure versus the gain setting. The figure shows that the noise decreases as gain increases. At the lowest gain setting, the noise figure was approximately 30 dB, while the noise figure was approximately 11 dB for the 51 dB gain setting. These values are higher than the simulated noise figures of 27.38 dB and 7.23 dB as reported in section 7.4 for the lowest and highest gain settings, respectively. In addition, the graph shows a significant drop in noise figure when the gain changes from 27 dB to 30 dB. This drop is due the switching of the first gain stage from low to high gain. The lower noise figure for the high gain setting is due to the drop in R_e of the first amplifier when the gain changes from low to high.

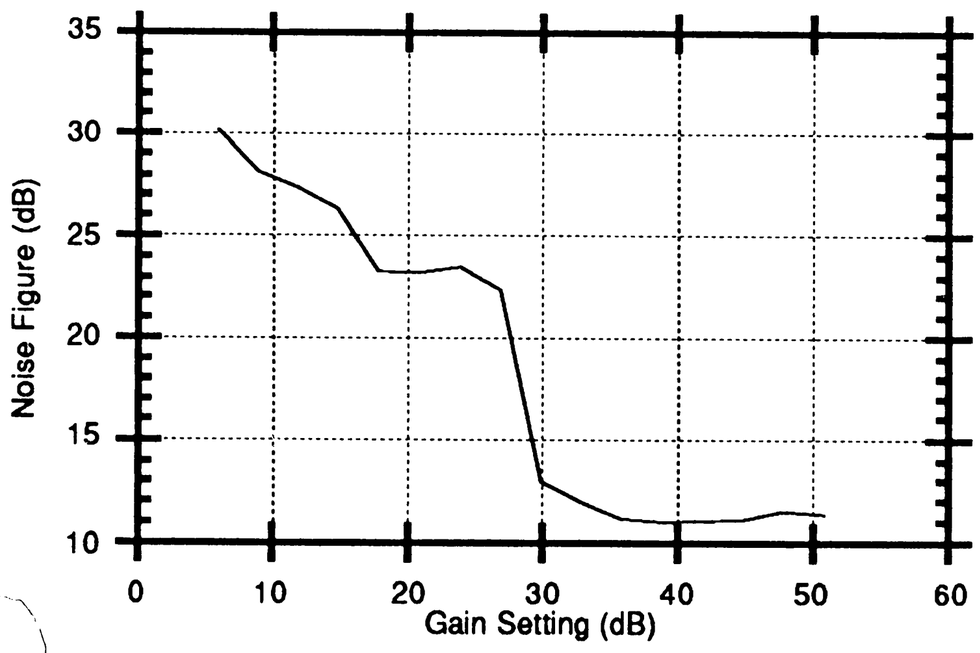

Figure 7.17: Noise Figure vs. Gain Setting

7.5.5 Switching Speed Results

The average enable switching speed was measured to be 10.36 µs. This compares with the simulated value of 5 µs. The difference is likely because the simulated values did not include parasitic capacitances that were

present in the packaged devices. The major parasitics are from the bonding pad, package pin, and measurement cable capacitances.

7.6 Experimental Problems

In the first attempts at obtaining experimental results, there were some unexpected results which led to the discovery of some problems with the final manufactured circuit. This section discusses some of these difficulties with the circuit.

During initial gain measurements of the circuit, the gain for the two highest gain settings, 48 dB and 51 dB, were found to be significantly lower than expected. Since the lower gain settings seemed to be within the desired gain error for each setting, a feedback problem was suspected. With the removal of the 30 pF load capacitances on the RF evaluation board that were placed on the outputs, the gain for the two highest gain settings improved significantly and were within the desired gain error.

The problem appeared to be the development of an oscillation when the two highest gain settings were selected. Since the removal of the load capacitor removed the oscillation, it became evident that the output was feeding back to the input through the power supply and a divider effect was present between the power supply lead inductance and the load capacitance. When the gain of the circuit exceeded the loss from the divider effect, an unstable system would be present and oscillations occurred. The removal of the load capacitance causes the transfer function of the feedback path to increase the loss significantly and the system then becomes stable for the highest gain settings.

The graph shown in figure 7.18 demonstrates another side effect of the feedback problem. The differential output offset voltage is shown to increase almost exponentially as the gain setting increases from 6 dB to 51 dB. This increase in offset voltage is caused by the mixing of the fed-back local oscillator signal with the original LO signal. Since the LO and it's feedback signal are of identical frequency, but shifted in phase due to a delay, the

output would then produce a DC level. It is evident from the increasing DC offset level as gain increases that the LO is feeding back to the IF input.

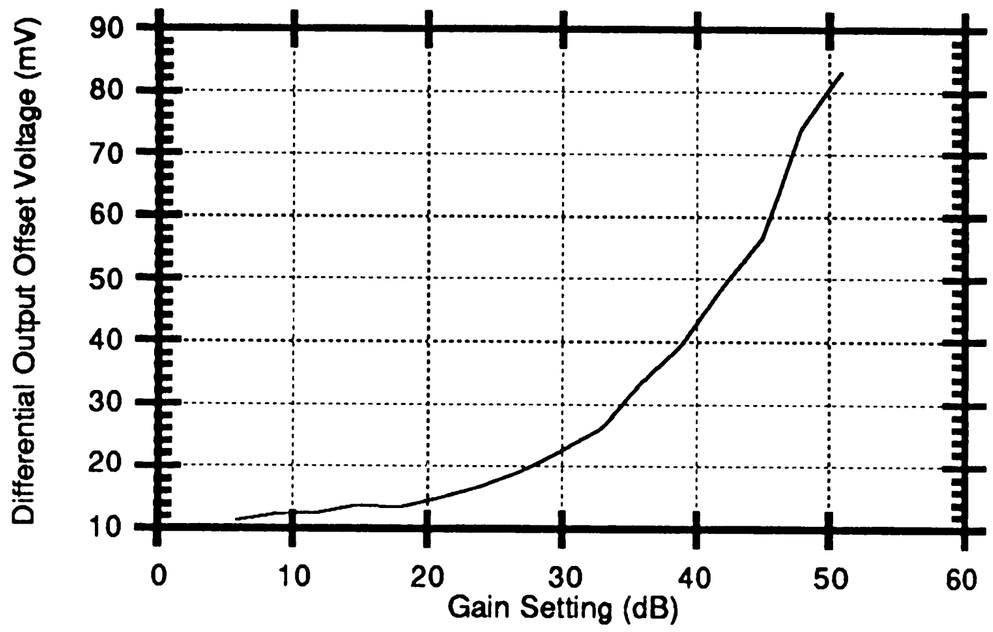

Figure 7.18: Output Offset Voltage vs. Gain Setting

Other factors could have attributed to this feedback problem, including the placement of the LO input pin next to one of the output pins (pinout of figure 7.2), a layout which found two output leads crossing over the IF input lead, and a single pin power supply (Vcc) connecting all blocks together. The pinout and the layout problems are attributed to the inability to pick an optimum floor plan because of the limitations of a linear array and a need to have a pinout that could be marketable to customers.

One assumption that was taken caused these problems to be over looked in the design before manufacture. The assumption that the mixer outputs would be strictly low frequency was incorrect. The filtering capacitors that were added to the mixer outputs didn't provide enough filtering because of a low pass frequency that was set too high. In addition, the path through the mixer's load resistors was not the only potential feedback path. Another path was present though the collectors of the push-pull output transistors.

A new layout of the power supply distribution and a new pinout would help to correct these problems. Also, the use of separate supplies for the amplifier, mixer, and output stages would also improve performance.

8. Conclusions

A 70 MHz Digitally Controlled Gain Amplifier and Quadrature Demodulator integrated circuit has been described and experimental results of the fabricated circuit have been presented. The circuit achieves the desired objectives for use as a circuit block in the receiver section of mobile radio terminals that comply with the Groupe Speciale Mobile (GSM) standard for European digital cellular radio.

The GSM digital cellular telephone system has been described as a means for high quality mobile communications that will be implemented in member countries of the European Economic Community. In addition, the requirements for IF amplification and demodulation, as they apply to the described circuit, have been presented. The means by which these requirements were implemented was initially discussed as an overview of the integrated circuit that was designed.

The circuit, consisting in an IF amplifier stage and a quadrature demodulation stage, provides digitally controlled amplification and demodulation of 70 MHz Gaussian Minimum Shift Keying (GMSK) modulated radio signals. The circuit is also capable of being switched off so as to draw zero power from the supplies.

The four digitally controlled gain IF amplifiers were designed to provide a gain range of 0 dB to 45 dB. The 16 separate gain levels are selected by four digital inputs that control the gain in 3 dB steps. The maximum gain error for any one gain level is ±3 dB. Design equations were presented for the circuit and an example calculation was demonstrated.

The quadrature demodulation stage was discussed in two parts. First, the double balanced mixer and output stage was presented, where it was shown how GMSK demodulation is implemented with a Gilbert cell multiplier. The mixer stage provides for demodulation of GMSK signals by multiplying a 70 MHz IF signal with two orthogonal 70 MHz square wave LO signals that is provided by a phase shifter circuit. The resulting output signal is filtered and operates in a band of DC to 1 MHz. Design equations and

examples were presented to discuss the operation and the 6 dB conversion gain of the mixer and output stages.

The phase shifter was designed to provide the required orthogonal inputs to the In-phase and Quadrature local oscillator inputs of the mixer stages. The outputs of the phase shifter circuit provided two signals that were phase shifted from each other by 90° with an error of less than ±3°. In addition, it was shown how limiting amplifiers on the outputs could provide mixer output levels that were independent of local oscillator input levels.

To properly operate the circuit, a bandgap voltage and current reference circuit was designed to provide temperature independent and proportional to absolute temperature outputs for various stages in the overall circuit. The bandgap was also designed to be switchable by a digital enable input.

Finally, the implementation of the circuit blocks and the experimental results were presented. The layout of the circuit on AT&T's ALA202 linear array was described along with the selected packaging. In addition, some of the full chip simulation results were presented and discussed. The 100 mW circuit, having been manufactured in AT&T's High Frequency Complementary Bipolar Integrated Circuit (CBIC-U) process, was tested for DC and high frequency parameters. Some of the results demonstrated the predicted variations in parameters that were presented in the design discussions. Overall, the experimental results confirmed the predictions that were made by design equations and simulation results.

The experimental results also revealed some problems and pitfalls that are generally associated with high frequency integrated circuit design. The discussion of the problems leads to some suggestions for future improvements of this circuit.

In general, this thesis demonstrates that a high frequency circuit may be designed successfully as an integrated circuit on a linear array. The common limitations of high frequency integrated circuit design are somewhat accentuated when using a linear array, but in some cases, these limitations need not be barriers to successful design.

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Appendices

Appendix 1 - IF Amplifer Gain Test Simulation Results

Amplifier AC Gain Test **T=25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
gain24ln	+0.325 dB	-0.348 dB (c6)	+0.359 dB (c2)
gain12ln	-0.025 dB	-0.620 dB (c6)	+0.097 dB (c2)
gain6ln	+0.140 dB	-0.473 dB (c6)	+0.304 dB (c2)
gain3ln	+0.072 dB	-0.570 dB (c6)	+0.151 dB (c2)
bndwdthln	+119.1 MHz	+79.4 MHz (c1)	+181.2 MHz (c2)
gain24hn	+24.2 dB	+23.0 dB (c5)	+24.3 dB (c4)
gain12hn	+11.9 dB	+11.1 dB (c1)	+11.9 dB (c2)
gain6hn	+6.11 dB	+5.46 dB (c1)	+6.26 dB (c2)
gain3hn	+3.17 dB	+2.61 dB (c1)	+3.25 dB (c2)
bndwdthhn	+109.5 MHz	+74.6 MHz (c3)	+163.5 MHz (c2)

Amplifier AC Gain Test **T=-25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
gain24ll	+0.296 dB	-0.455 dB (c6)	+0.394 dB (c2)
gain12ll	+0.022 dB	-0.587 dB (c6)	+0.166 dB (c2)
gain6ll	+0.179 dB	-0.426 dB (c6)	+0.368 dB (c2)
gain3ll	+0.067 dB	-0.660 dB (c6)	+0.192 dB (c2)
bndwdthll	+119.9 MHz	+78.4 MHz (c6)	+182.8 MHz (c2)
gain24hl	+24.5 dB	+23.5 dB (c5)	+24.6 dB (c4)
gain12hl	+12.0 dB	+11.3 dB (c6)	+12.1 dB (c2)
gain6hl	+6.20 dB	+5.62 dB (c6)	+6.37 dB (c2)
gain3hl	+3.19 dB	+2.54 dB (c6)	+3.30 dB (c2)
bndwdthhl	+111.5 MHz	+74.9 MHz (c3)	+166.3 MHz (c2)

Amplifier AC Gain Test **T=95 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
gain24lh	+0.147 dB	-0.316 dB (c1)	+0.221 dB (c2)
gain12lh	-0.162 dB	-0.652 dB (c6)	-0.029 dB (c2)
gain6lh	+0.005 dB	-0.490 dB (c6)	+0.186 dB (c2)
gain3lh	-0.105 dB	-0.570 dB (c1)	+0.024 dB (c2)
bndwdthlh	+108.8 MHz	+74.6 MHz (c1)	+166.1 MHz (c2)
gain24hh	+23.5 dB	+22.9 dB (c5)	+23.5 dB (c0)
gain12hh	+11.5 dB	+11.1 dB (c6)	+11.6 dB (c2)
gain6hh	+5.89 dB	+5.43 dB (c3)	+6.05 dB (c2)
gain3hh	+2.96 dB	+2.52 dB (c3)	+3.08 dB (c2)
bndwdthhh	+98.9 MHz	+68.9 MHz (c1)	+147.6 MHz (c2)

Appendix 2 - Mixer Gain & Phase Test Simulation Results

Case	Temp (°C)	Gain (dB)	Phase (°)	Case	Temp (°C)	Gain (dB)	Phase (°)
c0	25.000	7.08	87.2	c4	25.000	7.01	88.5
		6.79				6.97	
	-25.000	7.12	90.6		-25.000	7.04	91.1
		6.93				6.83	
	95.000	6.64	89.4		95.000	6.63	91.4
		6.65				6.69	
c1	25.000	6.80	89.1	c5	25.000	6.48	88.8
		6.70				6.60	
	-25.000	6.68	90.7		-25.000	6.64	88.3
		6.63				6.50	
	95.000	6.43	91.6		95.000	5.70	90.6
		6.52				6.29	
c2	25.000	6.98	87.9	c6	25.000	7.13	89.2
		7.39				7.17	
	-25.000	7.21	93.4		-25.000	7.25	80.5
		6.96				6.90	
	95.000	6.27	88.7		95.000	6.64	92.1
		6.85				6.65	
c3	25.000	6.82	88.7				
		6.71					
	-25.000	6.85	87.8				
		6.81					
	95.000	6.37	91.5				
		6.46					

Appendix 3 - DC Operating Point Test Simulation Results

DC Operating Point Test		**T=25 deg.C**	
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivccln	+17.5 mA	+14.0 mA (c1)	+22.2 mA (c2)
igs1ln	-10.6 pA	-10.8 pA (c2)	-10.6 pA (c1)
igs2ln	-10.6 pA	-10.8 pA (c2)	-10.6 pA (c1)
igs3ln	-10.6 pA	-10.8 pA (c2)	-10.6 pA (c1)
igs4ln	-10.6 pA	-10.8 pA (c2)	-10.6 pA (c1)
ienbln	+623 nA	+335 nA (c4)	+1.58 uA (c6)
voutipln	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutinln	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutqpln	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutqnln	+2.86 V	+2.81 V (c5)	+2.91 V (c4)

DC Operating Point Test		**T=25 deg.C**	
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivcchn	+18.7 mA	+15.1 mA (c1)	+23.9 mA (c2)
igs1hn	+2.45 uA	+1.18 uA (c3)	+6.09 uA (c5)
igs2hn	+2.45 uA	+1.18 uA (c3)	+6.09 uA (c5)
igs3hn	+2.45 uA	+1.18 uA (c3)	+6.09 uA (c5)
igs4hn	+2.45 uA	+1.18 uA (c3)	+6.09 uA (c5)
ienbhn	+623 nA	+335 nA (c4)	+1.58 uA (c6)
voutiphn	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutinhn	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutqphn	+2.86 V	+2.81 V (c5)	+2.91 V (c4)
voutqnhn	+2.86 V	+2.81 V (c5)	+2.91 V (c4)

DC Operating Point Test		**T=25 deg.C**	
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivccsn	+82.5 nA	+24.6 nA (c1)	+273 nA (c2)
igs1sn	-11.5 pA	-11.9 pA (c2)	-11.5 pA (c6)
igs2sn	-11.5 pA	-11.9 pA (c2)	-11.5 pA (c1)
igs3sn	-11.5 pA	-11.9 pA (c2)	-11.5 pA (c6)
igs4sn	-11.5 pA	-11.9 pA (c2)	-11.5 pA (c6)
ienbsn	-15.7 nA	-52.7 nA (c2)	-2.92 nA (c1)
voutipsn	+4.68 V	+4.65 V (c3)	+4.70 V (c4)
voutinsn	+4.68 V	+4.65 V (c3)	+4.70 V (c4)
voutqpsn	+4.68 V	+4.65 V (c3)	+4.70 V (c4)
voutqnsn	+4.68 V	+4.65 V (c3)	+4.70 V (c4)

DC Operating Point Test		**T=-25 deg.C**	
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivccll	+16.7 mA	+13.1 mA (c1)	+21.4 mA (c2)
igs1ll	-10.5 pA	-10.8 pA (c2)	-10.5 pA (c6)
igs2ll	-10.5 pA	-10.8 pA (c2)	-10.5 pA (c6)
igs3ll	-10.5 pA	-10.8 pA (c2)	-10.5 pA (c6)
igs4ll	-10.5 pA	-10.8 pA (c2)	-10.5 pA (c6)
ienbll	+985 nA	+537 nA (c4)	+2.47 uA (c6)
voutipll	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutinll	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutqpll	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutqnll	+2.72 V	+2.70 V (c5)	+2.77 V (c4)

DC Operating Point Test **T=-25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivcchl	+18.0 mA	+14.2 mA (c1)	+23.0 mA (c2)
igs1hl	+3.45 uA	+1.68 uA (c3)	+7.81 uA (c5)
igs2hl	+3.45 uA	+1.68 uA (c3)	+7.81 uA (c5)
igs3hl	+3.45 uA	+1.68 uA (c3)	+7.81 uA (c5)
igs4hl	+3.45 uA	+1.68 uA (c3)	+7.81 uA (c5)
ienbhl	+985 nA	+537 nA (c4)	+2.47 uA (c6)
voutiphl	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutinhl	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutqphl	+2.72 V	+2.70 V (c5)	+2.77 V (c4)
voutqnhl	+2.72 V	+2.70 V (c5)	+2.77 V (c4)

DC Operating Point Test **T=-25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivccsl	+48.1 nA	+15.3 nA (c5)	+144 nA (c2)
igs1sl	-11.5 pA	-11.6 pA (c1)	-11.4 pA (c3)
igs2sl	-11.5 pA	-11.6 pA (c1)	-11.4 pA (c3)
igs3sl	-11.5 pA	-11.6 pA (c1)	-11.4 pA (c3)
igs4sl	-11.5 pA	-11.6 pA (c1)	-11.4 pA (c3)
ienbsl	-8.37 nA	-25.8 nA (c2)	-1.08 nA (c1)
voutipsl	+4.53 V	+4.51 V (c1)	+4.56 V (c2)
voutinsl	+4.53 V	+4.51 V (c1)	+4.56 V (c2)
voutqpsl	+4.53 V	+4.51 V (c1)	+4.56 V (c2)
voutqnsl	+4.53 V	+4.51 V (c1)	+4.56 V (c2)

DC Operating Point Test **T=95 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivcclh	+17.7 mA	+14.3 mA (c1)	+22.5 mA (c2)
igs1lh	-12.0 pA	-14.8 pA (c2)	-12.0 pA (c0)
igs2lh	-13.6 pA	-14.8 pA (c2)	-13.1 pA (c6)
igs3lh	-13.6 pA	-14.8 pA (c2)	-13.1 pA (c6)
igs4lh	-13.6 pA	-14.8 pA (c2)	-13.1 pA (c6)
ienblh	+398 nA	+210 nA (c4)	+1.03 uA (c6)
voutiplh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutinlh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutqplh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutqnlh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)

DC Operating Point Test **T=95 deg.C**

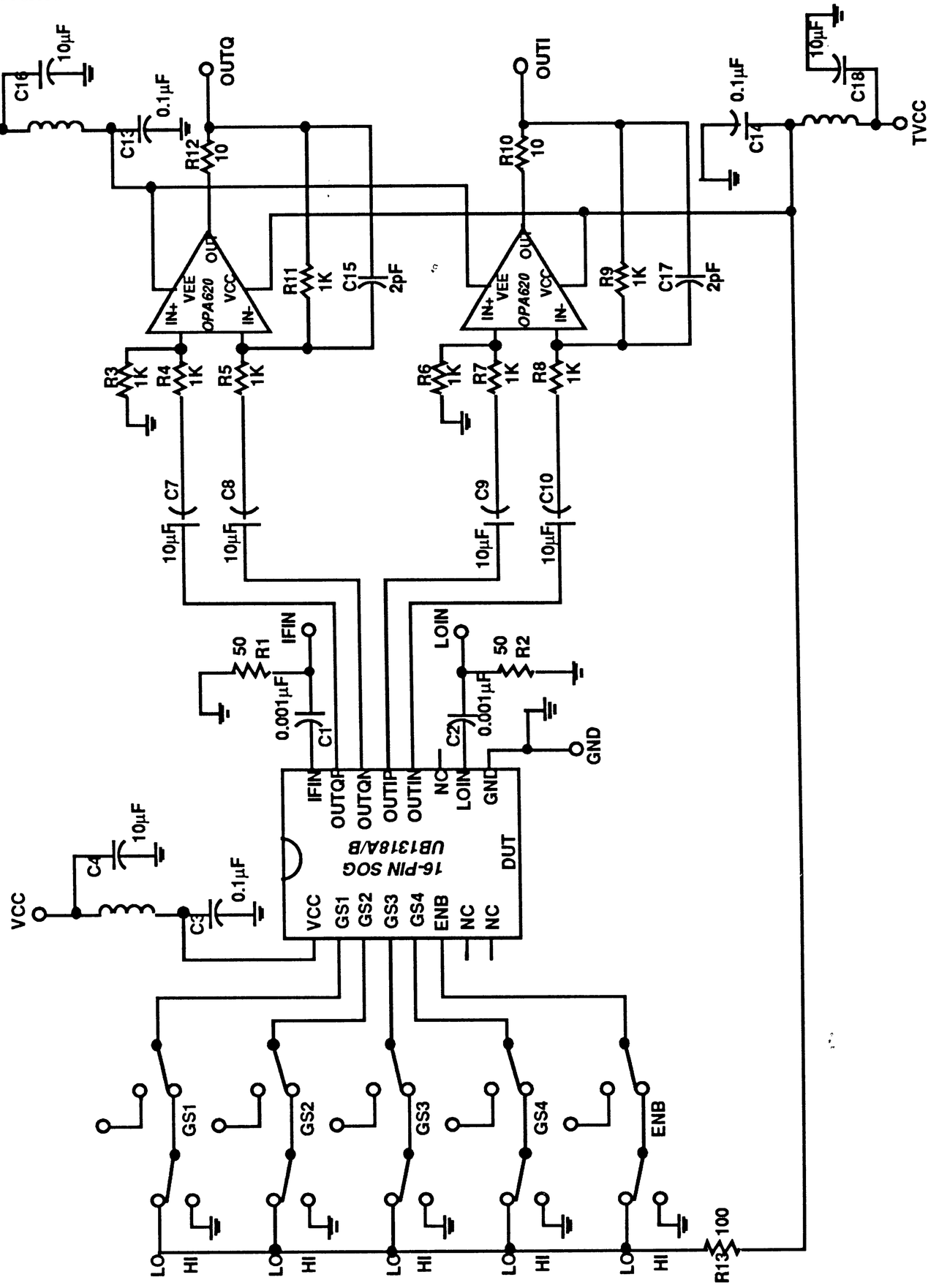
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivcchh	+19.0 mA	+15.4 mA (c1)	+24.4 mA (c2)
igs1hh	+1.79 uA	+842 nA (c3)	+4.76 uA (c5)
igs2hh	+1.79 uA	+842 nA (c3)	+4.76 uA (c5)
igs3hh	+1.79 uA	+842 nA (c3)	+4.76 uA (c5)
igs4hh	+1.79 uA	+842 nA (c3)	+4.76 uA (c5)
ienbhh	+398 nA	+210 nA (c4)	+1.03 uA (c6)
voutiphh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutinhh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutqphh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)
voutqnhh	+3.08 V	+3.01 V (c5)	+3.13 V (c4)

DC Operating Point Test **T=95 deg.C**

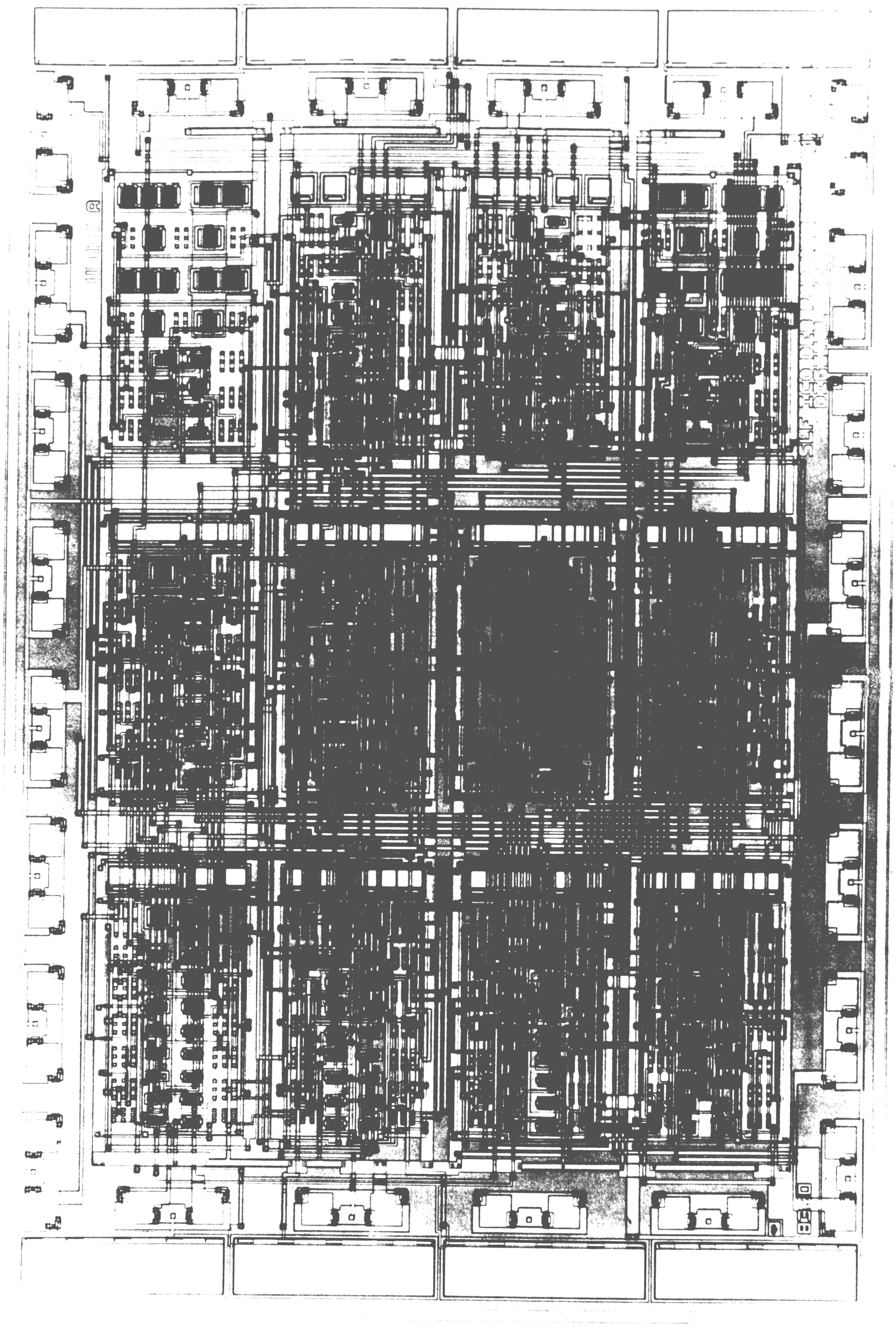
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
ivccsh	+64.7 nA	+30.1 nA (c6)	+144 nA (c2)
igs1sh	-15.4 pA	-17.3 pA (c2)	-15.1 pA (c1)

igs2sh	-15.4 pA	-17.3 pA (c2)	-15.1 pA (c5)
igs3sh	-15.4 pA	-17.3 pA (c2)	-15.1 pA (c1)
igs4sh	-15.4 pA	-17.3 pA (c2)	-15.1 pA (c5)
ienbsh	-9.71 nA	-18.3 nA (c2)	-3.86 nA (c6)
voutipsh	+4.88 V	+4.77 V (c3)	+4.92 V (c4)
voutinsh	+4.88 V	+4.77 V (c3)	+4.92 V (c4)
voutqpsh	+4.88 V	+4.77 V (c3)	+4.92 V (c4)
voutqnsh	+4.88 V	+4.77 V (c3)	+4.92 V (c4)

Appendix 4 - RF Test Board Circuit Schematic



Appendix 5 - Chip Photomicrograph



Appendix 6 - Impedance Test Simulation Results

Impedence Test **T=25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimpln	1.53 kOhms	1.41 kOhms (c6)	1.58 kOhms (c4)
loinpln	2.22 kOhms	1.77 kOhms (c2)	2.70 kOhms (c1)
imppiln	24.6 Ohms	16.9 Ohms (c2)	38.0 Ohms (c5)
impniln	24.6 Ohms	16.9 Ohms (c2)	38.0 Ohms (c5)
imppqln	24.6 Ohms	16.9 Ohms (c2)	38.0 Ohms (c5)
impnqln	24.6 Ohms	16.9 Ohms (c2)	38.0 Ohms (c5)

Impedence Test **T=25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimphn	665 Ohms	580 Ohms (c5)	747 Ohms (c4)
loinphn	2.22 kOhms	1.77 kOhms (c2)	2.70 kOhms (c1)
imppihn	24.6 Ohms	16.8 Ohms (c2)	38.0 Ohms (c5)
impnihn	24.6 Ohms	16.8 Ohms (c2)	38.0 Ohms (c5)
imppqhn	24.6 Ohms	16.8 Ohms (c2)	38.0 Ohms (c5)
impnqhn	24.6 Ohms	16.8 Ohms (c2)	38.0 Ohms (c5)

Impedence Test **T=-25 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimpll	1.53 kOhms	1.39 kOhms (c6)	1.61 kOhms (c4)
loinpll	2.06 kOhms	1.64 kOhms (c2)	2.52 kOhms (c1)
imppill	24.6 Ohms	16.4 Ohms (c2)	40.4 Ohms (c5)
impnill	24.6 Ohms	16.4 Ohms (c2)	40.4 Ohms (c5)
imppqll	24.6 Ohms	16.4 Ohms (c2)	40.4 Ohms (c5)
impnqll	24.6 Ohms	16.4 Ohms (c2)	40.4 Ohms (c5)

Impedence Test **T=-25 deg.C**

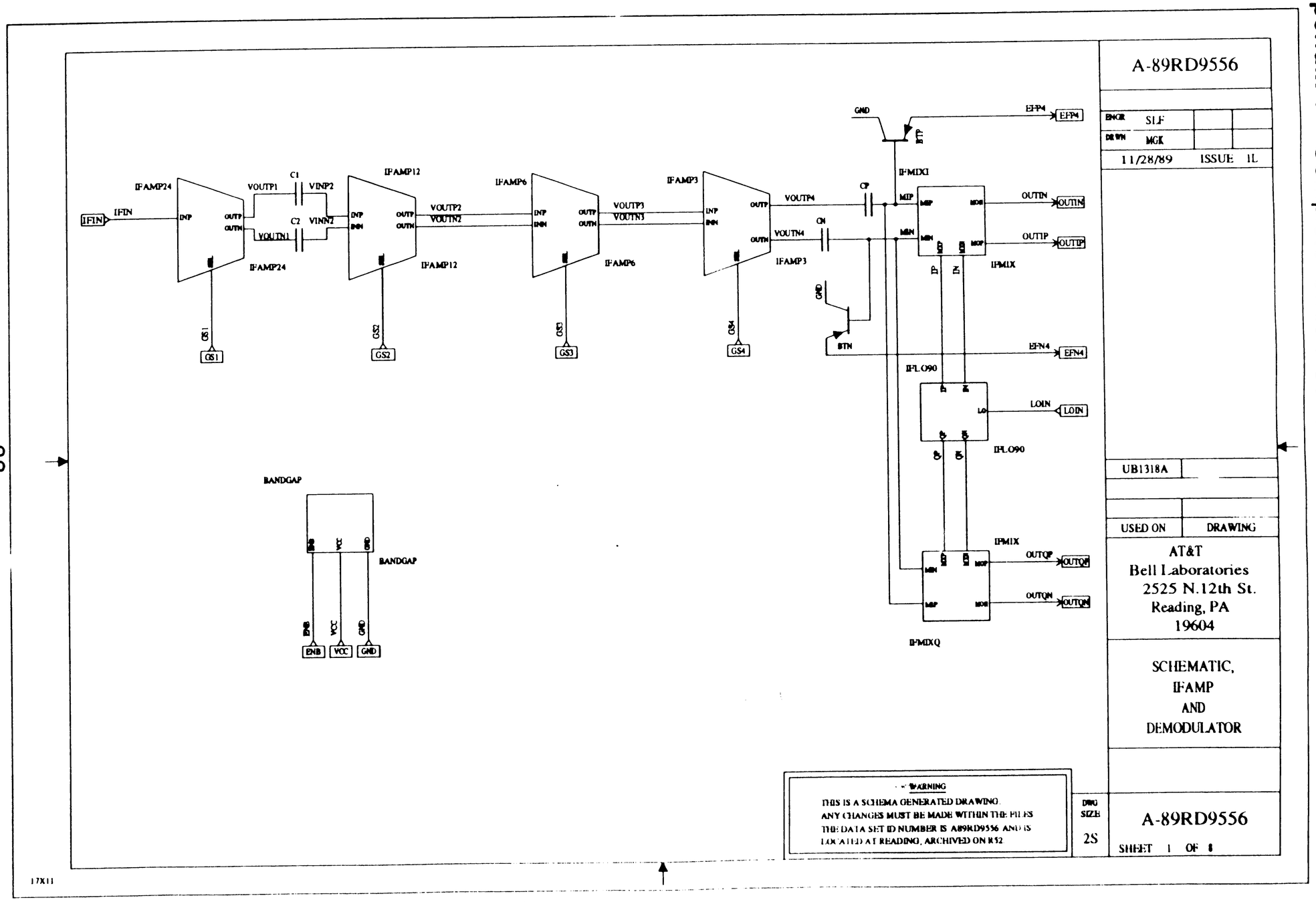
Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimphl	664 Ohms	583 Ohms (c5)	757 Ohms (c4)
loinphl	2.06 kOhms	1.64 kOhms (c2)	2.52 kOhms (c1)
imppihl	24.6 Ohms	16.4 Ohms (c2)	40.3 Ohms (c5)
impnihl	24.6 Ohms	16.4 Ohms (c2)	40.3 Ohms (c5)
imppqhl	24.6 Ohms	16.4 Ohms (c2)	40.3 Ohms (c5)
impnqhl	24.6 Ohms	16.4 Ohms (c2)	40.3 Ohms (c5)

Impedence Test **T=95 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimplh	1.51 kOhms	1.38 kOhms (c6)	1.59 kOhms (c4)
loinplh	2.55 kOhms	2.03 kOhms (c2)	3.10 kOhms (c1)
imppilh	27.2 Ohms	18.9 Ohms (c2)	40.6 Ohms (c5)
impnilh	27.2 Ohms	18.9 Ohms (c2)	40.6 Ohms (c5)
imppqlh	27.2 Ohms	18.9 Ohms (c2)	40.6 Ohms (c5)
impnqlh	27.2 Ohms	18.9 Ohms (c2)	40.6 Ohms (c5)

Impedence Test **T=95 deg.C**

Param	Nominal Value	Lower Limit (case)	Upper Limit (case)
inimphh	661 Ohms	554 Ohms (c5)	743 Ohms (c4)
loinphh	2.56 kOhms	2.03 kOhms (c2)	3.10 kOhms (c1)
imppihh	27.2 Ohms	18.9 Ohms (c2)	40.5 Ohms (c5)
impnihh	27.2 Ohms	18.9 Ohms (c2)	40.5 Ohms (c5)
imppqhh	27.2 Ohms	18.9 Ohms (c2)	40.5 Ohms (c5)
impnqhh	27.2 Ohms	18.9 Ohms (c2)	40.5 Ohms (c5)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VOUTP3
VOUTN3
VOUTP4
VOUTN4
CP
CN
GND
EFP4
EFN4
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OUTIN
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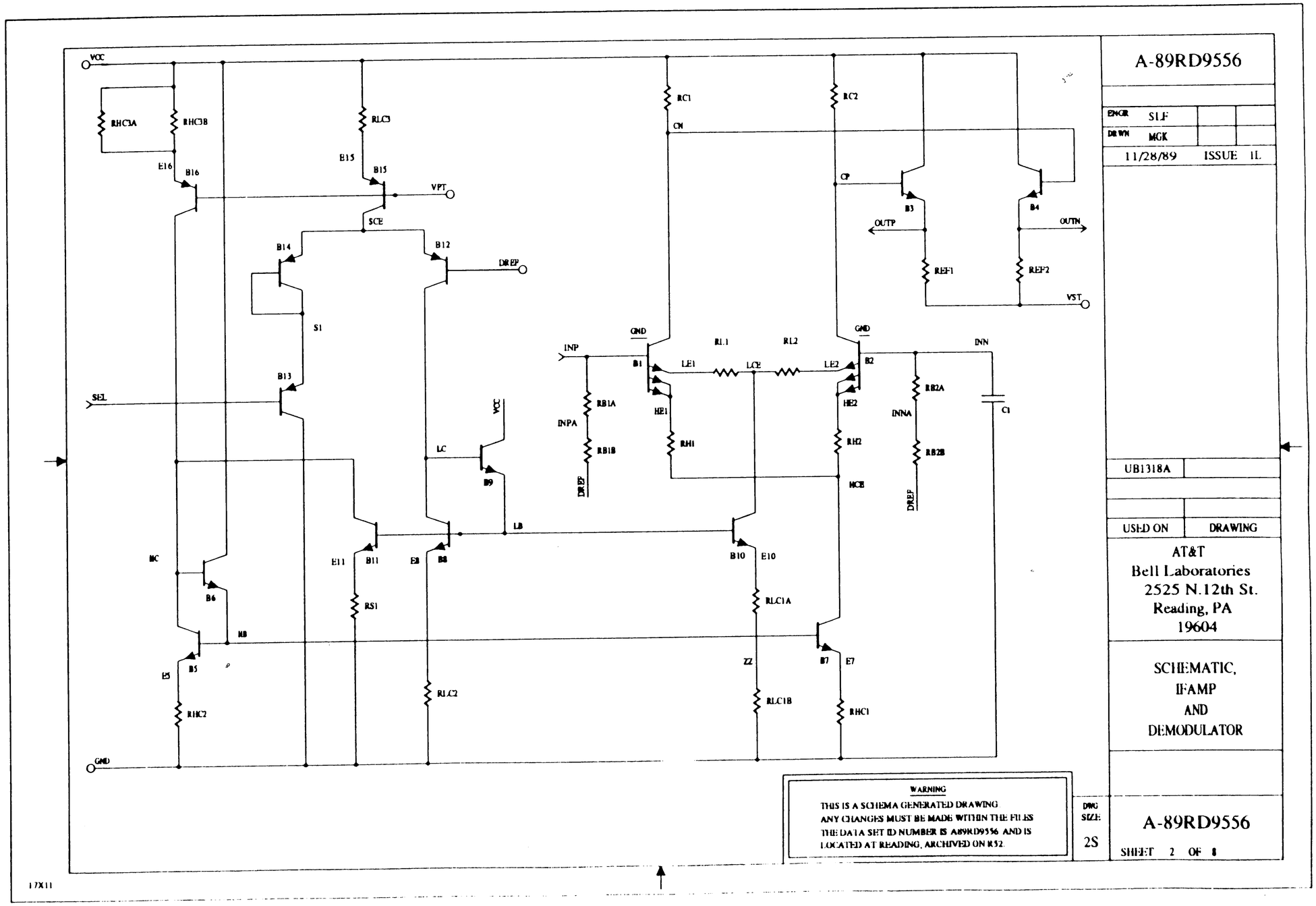

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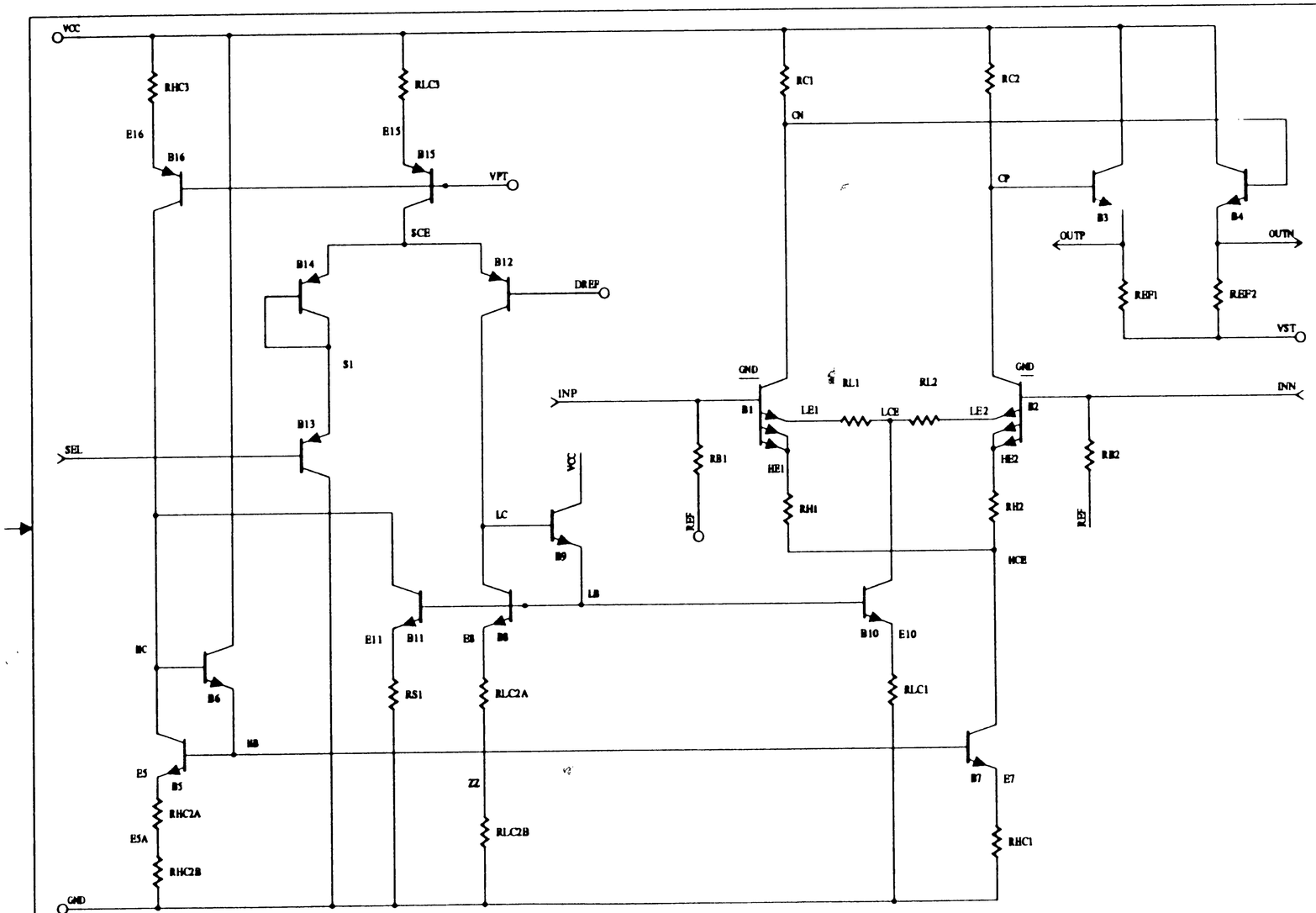

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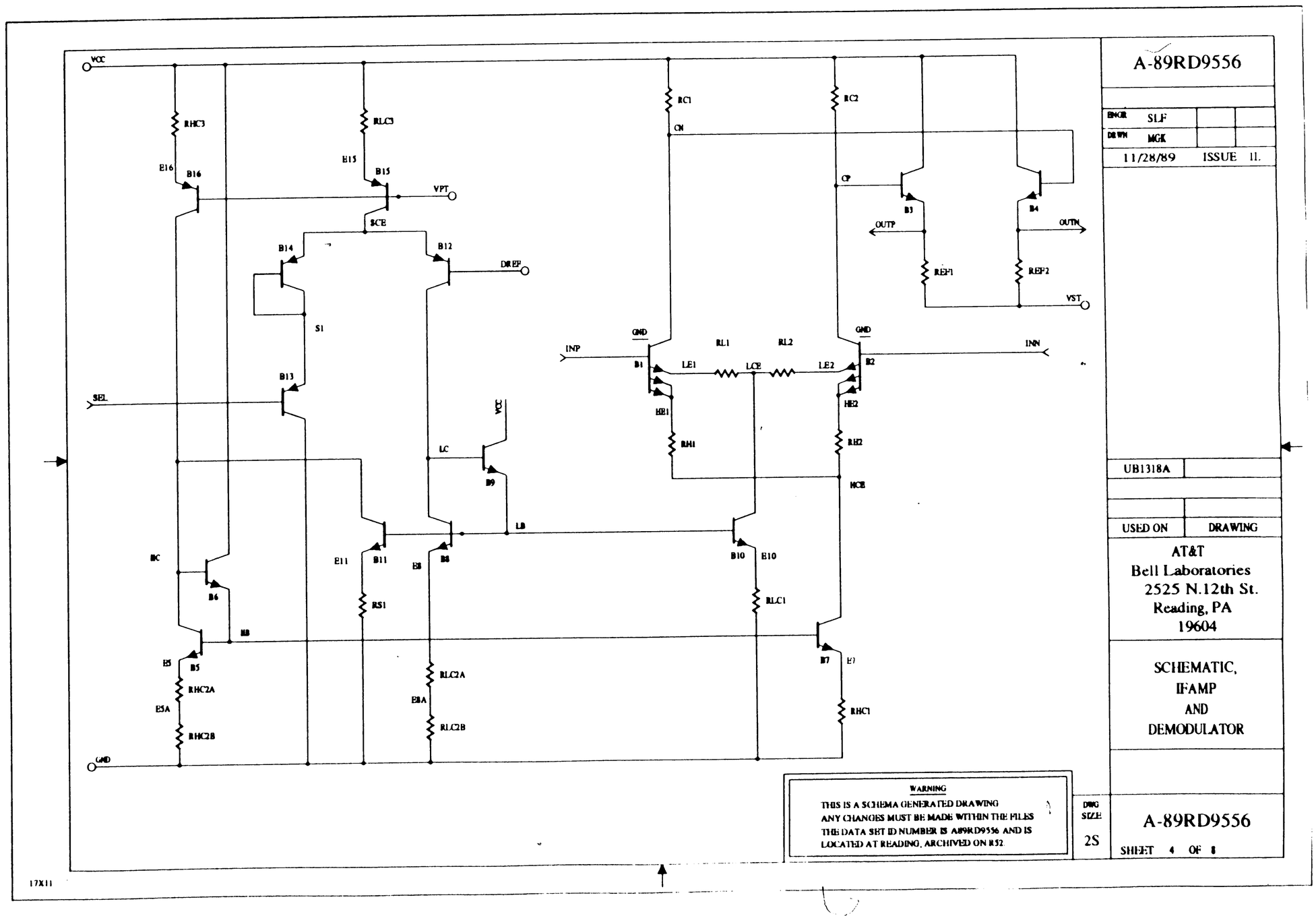

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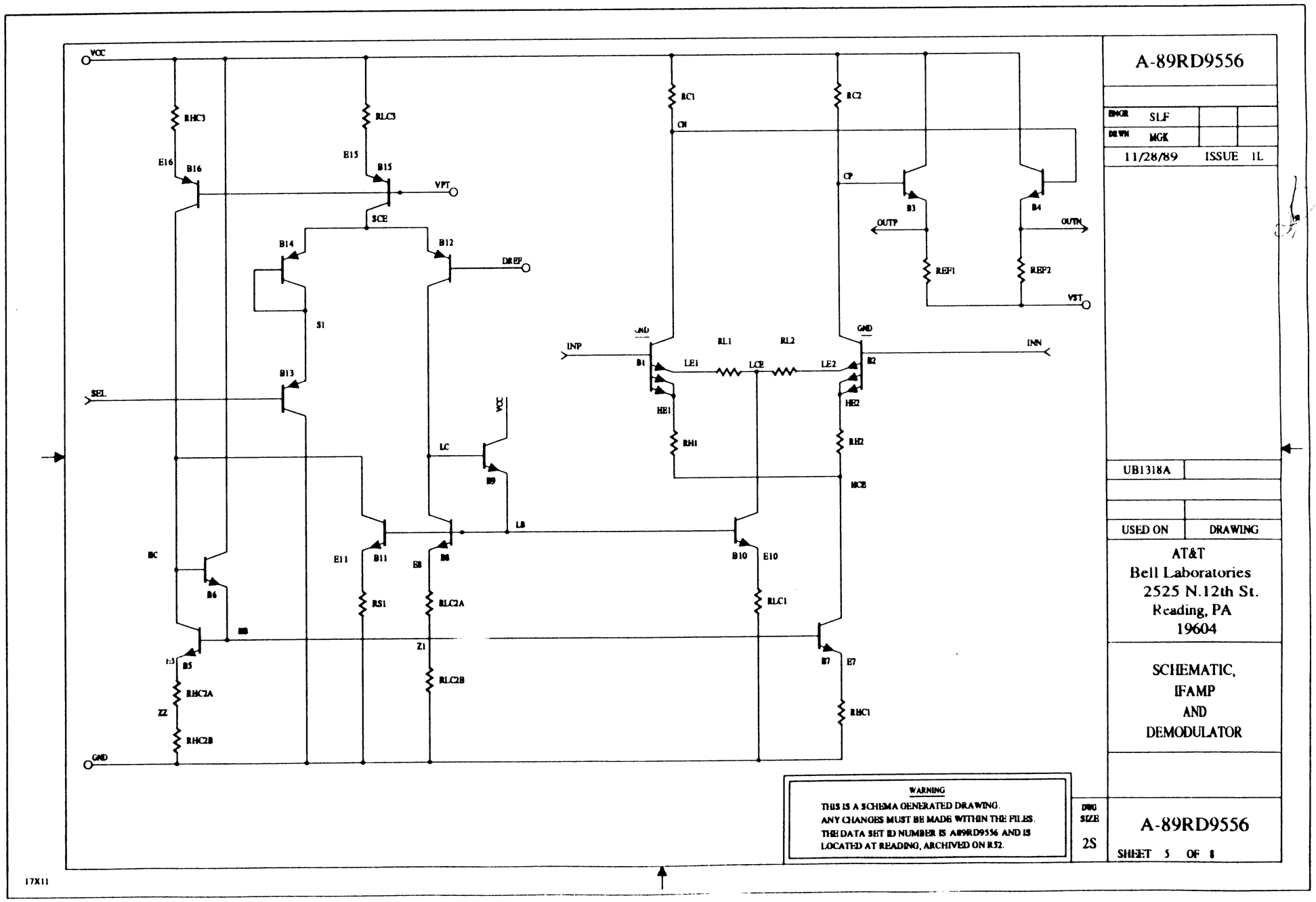
SHEET 4 OF 8



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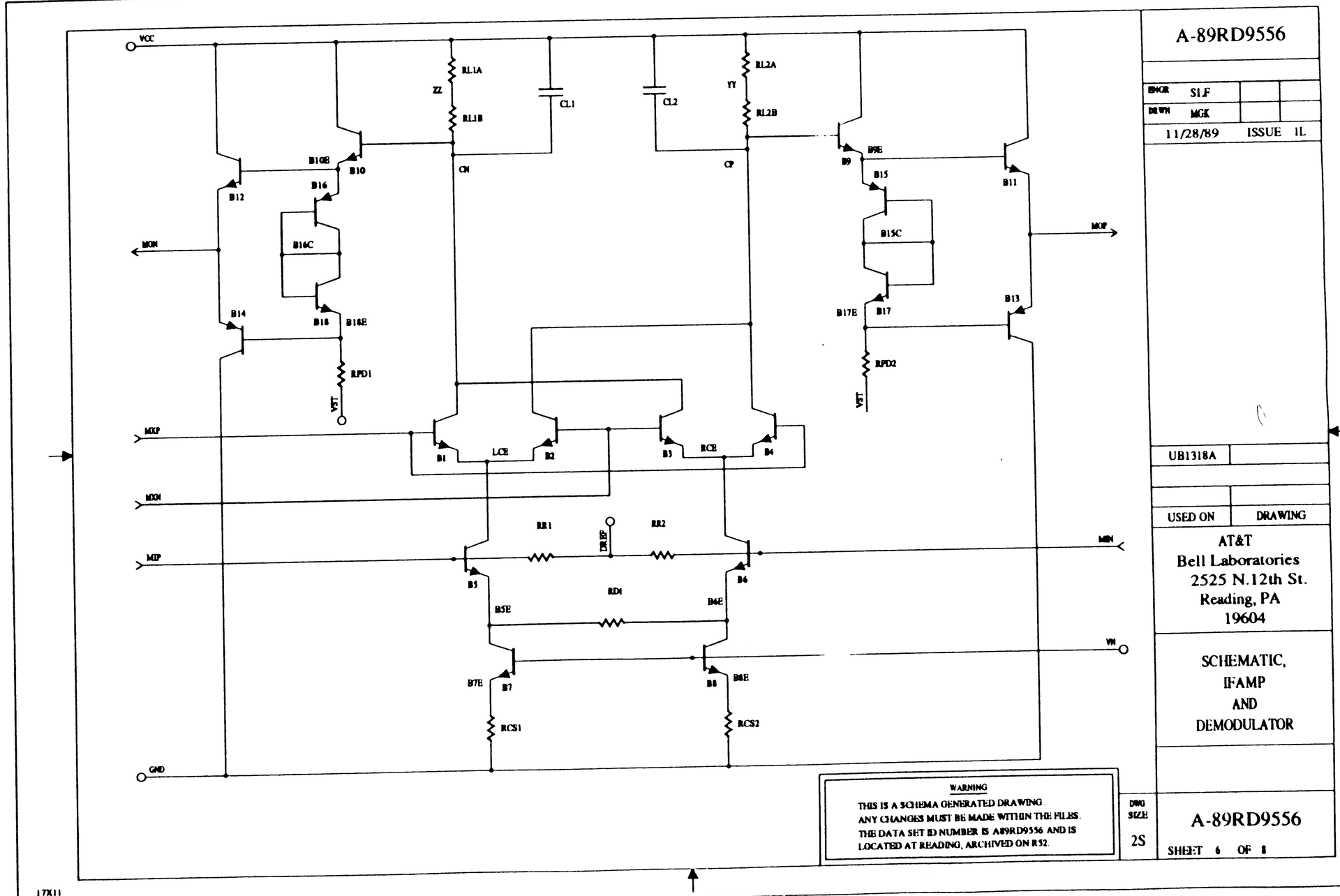

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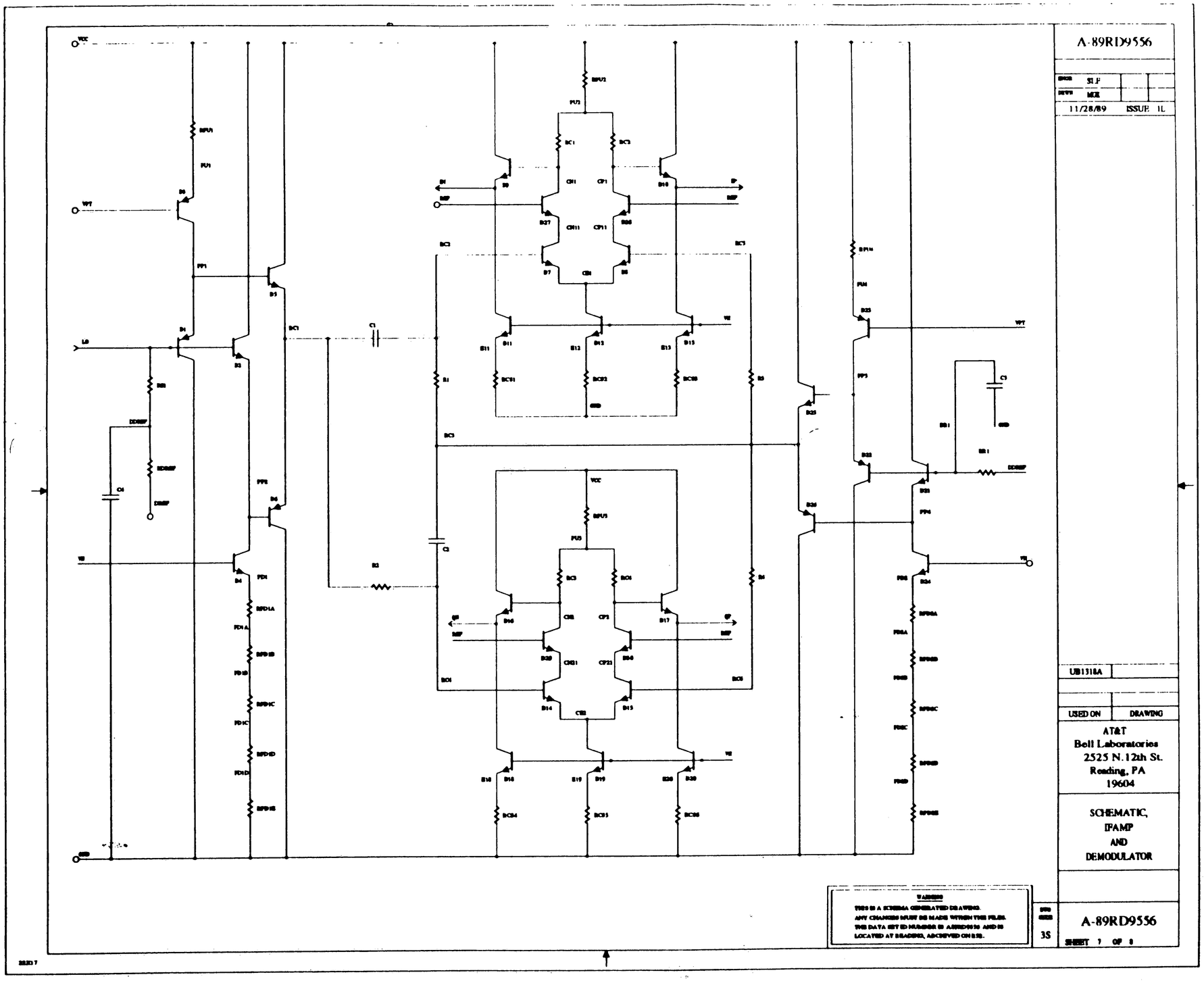
SHEET 6 OF 8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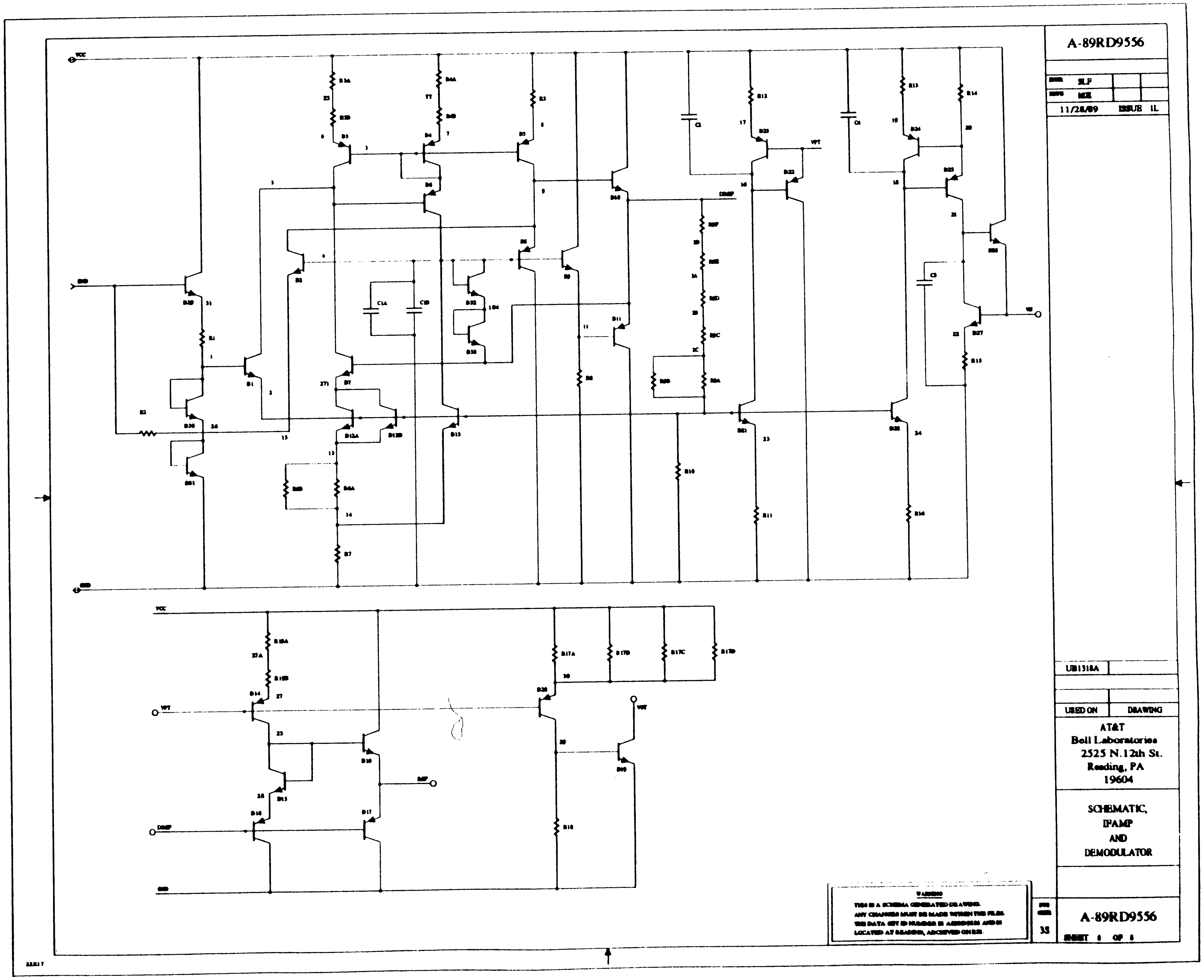
SHEET 7 OF 8
3S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DEMODULATOR
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Vita

Scott Leonard Forgues was born on February 21, 1966 to Gerald A. and Mignonne B. Forgues in New Bedford, Massachusetts. Scott earned the degree of Bachelor of Science in Electrical Engineering - Magna Cum Laude in June of 1988 from the University of Lowell, Lowell, Massachusetts. While an undergraduate student, Scott was employed as a CMOS Digital Circuit Design Technician by Custom Silicon, Inc., Lowell, Massachusetts from 1986 to 1988. In June of 1988, he began employment as a Member of Technical Staff in the Analog Bipolar Design Department with AT&T Bell Laboratories in Reading, Pennsylvania. While employed at AT&T Bell Laboratories, Scott began work on the degree of Master of Science in Electrical Engineering at Lehigh University, Bethlehem, Pennsylvania in September of 1988. Scott co-authored a paper titled "A 100 MHz IF Amplifier/Quadrature Demodulator for GSM Cellular Radio Mobile Terminals" that was presented at the 1990 IEEE Bipolar Circuits and Technology Meeting in Minneapolis, MN.