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A STUDY OF THE EFFECTS ON GATE OXIDE QUALITY OF NITRIDE THICKNESS AND POLYSILICON REMOVAL METHOD IN THE POLY-BUFFER LOCOS PROCESS

by

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in

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ACCEPTANCE

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science in Material Science.

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1. Abstract

Electrical isolation of active devices in integrated circuits is accomplished using a partially or fully recessed oxide in the "field" regions between devices. Most modern integrated circuit technologies use LOCOS (LOCal Oxidation of Silicon) for this device isolation. The major drawback of LOCOS is the lateral oxidation or "bird's beak" that occurs underneath the oxidation mask. For a typical 5,000 - 6000 Å field oxide, the "bird's beak" measures ~ 0.5μm per side and is independent of the field oxide area. Poly-buffer LOCOS is a semirecessed LOCOS process which exploits the fact that a thinner pad oxide and/or a thicker nitride results in a shorter "bird's beak". This is accomplished by introducing a polysilicon buffer layer underneath the nitride. Poly-buffer LOCOS has been used sucessfully as device isolation method for several submicron technologies. The objective of this work is to investigate two areas of the poly-buffer LOCOS process; a) the effect of various silicon nitride thicknesses (1600 Å - 2800 Å) on "bird's beak" encroachment and silicon defects and b) the effect of the polysilicon removal method on the quality of the active device regions.

The results show that the "bird's beak" lateral encroachment decreased with increasing nitride thickness. There was no statistical difference in the defect density due to nitride thickness and the average gate oxide defect density of experimental groups were less than the standard LOCOS group. No process-induced stacking faults were found on any wafer. Plasma removal of the polysilicon buffer layer with SF_6 and NF_3 resulted in significantly lower gate oxide defect density than the standard LOCOS group. An increase in gate oxide defect density was observed when the polysilicon buffer layer was removed thru oxidation.

2. *Background*

2.1 *Rationale*

Electrical isolation of active devices in integrated circuits is accomplished using a partially or fully recessed oxide in the "field" regions between devices. Most modern integrated circuit technologies use LOCOS (LOCal Oxidation of Silicon) for this device isolation.

The LOCOS process was introduced by Appels and Kooi in 1970 . In this process a thermally grown pad oxide is covered by a deposited layer of Si_3N_4, which will act as an oxidation mask. The nitride layer is patterned, etched to remove the nitride over selected areas, and then oxidized to grow a thick field oxide of 3,000 to 10,000 Å in the exposed silicon regions, as illustrated in Figure 1. This process has become the most common isolation technology for Metal Oxide Semiconductor (MOS) integrated devices down to 0.9 µm geometries. [1]

Silicon nitride films are known to have very high tensile stress when deposited by Chemical Vapor Deposition (CVD) on silicon (on the order of 10^{10} dynes/cm^2). [1] The termination of intrinsic stresses at the edge of the nitride films results in a horizontal force that acts on the silicon substrate. Under some conditions, this stress can exceed the critical stress for dislocation generation in silicon. In the LOCOS process a pad oxide layer is used to reduce the force transmitted to the silicon at the nitride edge, relieving the stress of the nitride through the viscous flow of the pad oxide. [2]

The major drawback of LOCOS is the lateral oxidation or "bird's beak" that occurs underneath the nitride oxidation mask. The "bird's beak", as shown in Figure 2, is caused by the lateral diffusion of oxidizing species during selective field oxidation. Its length, X, varies depending on the nitride and pad oxide thicknesses ratio and the selective oxidation conditions. For a typical 5,000 - 6000 Å field oxide, the "bird's beak" measures ~ 0.5µm per side and is independent of the field oxide area. [3] Due to the 0.5µm "bird's beak" encroachment it was thought that LOCOS would have to be replaced for device dimensions smaller than 2 µm ; however, optimization of process steps have allowed use of LOCOS for device fabrication with active device regions of ~ 1.00 µm. [4] [5] [6] For linewidths of active device regions of < 1 µm , the standard LOCOS isolation must be modified while maintaining its desirable attributes : absence of edge defects, low diode leakage, gate oxide integrity and process simplicity. Various methods of obtaining active device isolations in submicron devices have been published. [7] [8] [9] [10] [11] One method, which will be the focus of my work, Poly-buffer LOCOS has been used sucessfully as the active device isolation scheme for several submicron technologies.

2.2 Poly-Buffer LOCOS Isolation

2.2.1 Process Description The poly-buffer LOCOS is a semirecessed LOCOS isolation method which exploits the fact that a thinner pad oxide and/or a thicker nitride will result in a shorter "bird's beak". This is accomplished by introducing a polycrystalline silicon (polysilicon) buffer layer between the silicon nitride layer and the underlying oxide. The polysilicon is effective in absorbing the tensile stress from the nitride allowing the pad oxide to be thinned and the nitride thickened to reduce the "bird's beak" encroachment without generating stress induced defects in the active regions.

In 1985, Robert Havemann and Gordan Pollack at Texas Instruments Incorporated, Dallas Texas, were awarded the patent for this invention. [12] The poly-buffer LOCOS process sequence is illustrated in Figure 3. The thicknesses of the pad oxide, polysilicon and silicon nitride films can be tailored to give desired "bird's beak" encroachment length and profile. After resist patterning, the stack is etched to remove the nitride and polysilicon layers, stopping in or on the pad oxide layer. Alternatively, the pad oxide and some of the silicon substrate maybe etched during patterning of the stack below the bottom level of the pad oxide layer. The exposed region is then oxidized to form the field oxide regions by any standard oxidation method resulting in a partially recessed field oxide. Next, the silicon nitride layer is removed using a hot phosphoric acid etch preceded by a short HF etch to remove any oxynitride which forms during field oxidation. The polysilicon buffer layer is then removed using a selective etch or oxidizing the polysilicon and then etching.

2.2.2 Poly-Buffer LOCOS in VLSI Technologies There are many VLSI technologies using Poly-Buffer LOCOS for device isolation. The process features of some of these technologies are summarized in Table 1.

In 1986, N.Hoski and associates, from Sony Corporation in Japan, reported using poly-buffer LOCOS isolation in their 1.0 μm CMOS process for a 1 megabit SRAM. [13] They obtained a "bird's beak" length of less than 0.2 μm per side without sacrificing junction leakage current characteristics.

Richard Chapman and associates, from Texas Instruments Incorporated , Dallas, Texas, reported the use of TI's invention as the isolation scheme for a 0.8 μm CMOS technology in 1987. [14] Silicon nitride, polysilicon and oxide thicknesses were chosen to give a final "bird's beak" encroachment of only 0.1 μm per side into the active regions.

In 1988, Sony Corporation published the use of Advanced Poly Silicon Pad LOCOS for the 0.5 μm Isolation Technology. [8] This isolation method was an adaptation of their 1.0 μm SRAM process reported in 1986. One modification was the addition of a boron implant after field oxidation. The boron implant serves as a punch-through implant in the active regions.

TABLE 1. Poly-buffer LOCOS Processes

Poly-buffer LOCOS Process Summary					
Tech.	Oxide Tk.	Poly Tk.	Nitride Tk.	Field OX. Tk.	Bird's Beak
Sony 1μm	50 Å	550 Å	1000 Å	4000 Å	0.2μm
T.I 0.8μm	100 Å	500 Å	2400 Å	900°C steam	0.1μm *
Sony 0.5μm	50 Å	500 Å	not reported	2200 Å	0.1μm
G.E. 0.8μm	200 Å	550 Å	1500 Å	6000 Å	0.3 μm
T.I. 1.0μm	120 Å	500 Å	2400 Å	8000 Å	0.37 μm

* All bird's beak sizes reported are after field oxidation from cross-sectional SEM micrographs, except T.I. 0.8μm technology this bird's beak size is after HF etches prior to gate oxidation

boron implant after field oxidation. The field oxide thickness was only 2200 Å and "bird's beak" encroachment was reported to be 0.1 μm per side

In 1989, M. Ghezzo and associates from General Electric Co., Schenectady, New York, reported use of LOPOS (Local Oxidation of Polysilicon Over Silicon) for a 0.8 μm CMOS Technology. [9] They discussed the effect of pad oxide and silicon nitride thicknesses on "bird's beak" encroachment and process - induced silicon defects. A summary of measured "bird's beak" lengths are listed in Table 2. For the 0.8 μm CMOS process, they chose a stack comprised of a 200 Å oxide, 550 Å polysilicon and 1500 Å nitride. A 6000 Å field oxide is grown at 1000°C, for a "bird's beak" encroachment of 0.3 μm per side without generation of silicon defects. No silicon defects were observed in samples where the oxide to silicon nitride ratio was less than 10:1. There was also an absence of low-voltage breakdown during MOS capacitor voltage stressing up to 8MV/cm, and low junction leakage .

2.3 Poly-Buffer LOCOS Processing Issues

The choice of oxide, polysilicon, and nitride thicknesses depends on the processing capabilities of the manufacturing line and the technology. The objective is to obtain the smallest "bird's beak" encroachment possible without degrading the electrical characteristics of the devices. In the following section, the Poly-buffer LOCOS process steps from various technologies are discussed in more detail.

TABLE 2. LOPOS : Bird's Beak size

LOPOS : Bird's beak size			
Nitride	Buffer oxide thickness		
Thickness	100Å	200Å	300Å
1000Å	0.315μm	0.35μm	0.4μm
1500Å	0.246μm	0.305μm	0.315μm
2000Å	0.175μm	0.245μm	0.263μm

* Bird's Beak encroachment was measured on SEM micrographs as the distance between the encroachment point and the masking nitride edge vertical projection.

2.3.1 Stack Composition The pad oxide serves two distinct purposes: it relieves the stress from the silicon nitride layer on the silicon substrate and it serves as an etch stop during pattern transfer and stack removal after field oxidation. M.Ghezzo from General Electric studied three pad oxide thicknesses: 100 Å, 200 Å and 300 Å. They found that, for a given polysilicon and nitride thickness, the "bird's beak' encroachment increased with increasing pad oxide thickness. This same study also looked at three nitride thicknesses : 1000 Å, 1500 Å and 2000 Å. The results show that, for a given oxide and polysilicon thickness the "bird's beak" encroachment decreased with increasing nitride thickness. The generation of process-induced stacking faults was also monitored and found to be a function of the nitride/oxide ratio. No defects were observed for samples where this ratio was less than 10:1. [9]

The polysilicon layer thickness reported was consistently 500 - 550 Å for technologies using poly-buffer LOCOS isolation. General Electric and Texas Instruments both use LPCVD (Low Pressure Chemical Vapor Deposition) at 620°C for polysilicon deposition. General Electric reported that they found the "bird's beak" encroachment to be independent of the polysilicon thickness .

In a report by Y.Han and B.Ma, thicker polysilicon layers were evaluated. [15] Their experiments looked at a) 270 Å pad oxide and 2300 Å polysilicon, b) 270 Å pad oxide and 1700 Å polysilicon and c) 700 Å pad oxide and 1700 Å polysilicon. Nitride thickness was 1000 Å for each experiment. The "bird's beak" profiles obtained after an 8200 Å field oxidation are shown in Figure 4a. As the polysilicon thickness is reduced, the reentrant corner of the polysilicon is reduced. Han and Ma further optimized their stack to 260 Å pad oxide, 1000 Å polysilicon and 1000 Å nitride. This combination, with the same field oxide thickness of 8200 Å, eliminated the reentrant angle and resulted in a very small bird's beak,

as shown in Figure 4b.

2.3.2 Stack Etch and Field Oxidation In Han and Ma's study the polysilicon was not totally removed during stack etch and the remaining polysilicon - pad oxide was incorporated into the field oxide. This technique of oxidizing the polysilicon layer during the field oxidation process was also reported by Sony and Texas Instruments. [10] [13] The resulting field oxide profile, shown in Figure 5, is less planar with a sharp field oxide to active device region transition. Han and Ma claim two reasons for this profile and its shortened "bird's beak" : a) the lateral diffusion of oxidant is consumed by the polysilicon to form oxide, and b) the remaining lateral diffusion of oxidant is limited by the thin buffer oxide and is consumed by two silicon surfaces instead of one.

Texas Instruments discussed the need to minimize the oxidation of the polysilicon layer prior to silicon nitride deposition. They found that the presence of such an intermediate oxide inhibits the removal of the polysilicon layer after field oxidation, leaving residues in the active device regions. If this intermediate oxide is thick enough, a smaller secondary "bird's beak" will be formed during field oxidation. [10]

The choice of stack etch and field oxidation conditions used in the poly-buffer isolation scheme is dependent on the technology. In the technologies reported here the field oxide along with a channel-stop implant provided the isolation between PMOS and NMOS devices. Two stack etches were reported: a) etching both the nitride and polysilicon layers stopping in/on the pad oxide and b) etching only the nitride layer stopping in/on the polysilicon layer. The field oxide profiles obtained following each etch are also shown in Figure 5.

Texas Instruments reports using a single wafer plasma etcher to etch the nitride. The etch chemistry is C_2F_6 - CHF_3 - He at 140 Watts. A 15% overetch leaves ~ 250 Å of unetched polysilicon . Field oxide was grown at 900°C for ~ 10 hrs to grow a nominal 8000 Å oxide. Texas Instruments also looked at using HIPOX (HIgh Pressure Oxidation) for field oxide growth and found the gradient of the field oxide transition region to be independent of oxide growth method. They reported that the advantage of HIPOX was better corner sharpness.

General Electric reported removing the nitride and polysilicon layers with reactive ion etching (RIE) in two steps. The nitride was removed in a chemistry of 4:1 CHF_3 and CO_2, and then the polysilicon layer was removed with a 6:1 gaseous mixture of CCl_2F_2 and N_2 stopping in/on the pad oxide layer. A 6000 Å field oxide was grown at 1000 °C in steam.

2.3.3 Stack Removal After field oxidation the poly-buffer LOCOS stack must be removed without damage to the active device regions. In all technologies an HF oxide etch was used to remove the oxynitride layer prior to a nitride strip in HOT Phosphoric acid (H_3PO_4). This step was not found to be critical due to the high selectivity of hot phosphoric acid to oxide

and silicon as shown in Figure 6.

In a second step polysilicon was removed with a selective etch stopping in/on the pad oxide layer without pitting the active device regions. Here again only Texas Instruments and General Electric reported their method of polysilicon removal. Texas Instruments strips the polysilicon layer in a single wafer plasma reactor using a chemistry of SF_6 and He to achieve a > 40:1 selectivity of polysilicon to oxide giving them considerable process latitude. General Electric strips the polysilicon layer in an aqueous solution of KOH/isopropyl alcohol at 55 °C. Both companies report using a HF etch to remove the pad oxide layer and "bird's beak" oxide. This etch removed ~ 1000 Å of field oxide.

3. Experimental

3.1 Objective

Two evaluations were done using test devices which gave both structural and electrical characterization. For comparison devices were also fabricated with the standard LOCOS process. [4].

Gate oxide breakdown is caused by process-induced defects of all types. Poly-buffer LOCOS process is prone to process-induced defects due to process complexity. The studies discussed earlier contradict each other on the formation of process-induced stacking faults with thick nitride films, >1500 Å. The objective of this work is to investigate two areas of the poly-buffer LOCOS process; a) the effect of various silicon nitride thicknesses (1600 Å - 2800 Å) on "bird's beak" encroachment and silicon defects and b) the effect of polysilicon removal method on the surface quality of the active device regions.

3.2 Process Sequence

The poly-buffer LOCOS process used for the control cell is listed in Table 3 and described below.

P-type silicon wafers were used as the starting material. After tub formation and implantation the tub oxide was stripped using a HF etch. This was followed by a 150 Å oxide grown at 850°C an in O_2 - HCl ambient. The 500 Å poly-buffer layer was deposited by LPCVD (Low Pressure Chemical Vapor Deposition). No effort was made to minimize the oxide formation on the polysilicon layer prior to silicon nitride deposition. Four thicknesses of nitride were evaluated; 1600 Å, 2000 Å, 2400 Å and 2800 Å. All nitrides were deposited using LPCVD at 800°C. Only the deposition time was adjusted to obtain the desired thickness.

The poly-buffer LOCOS stack was then patterned using 1.2 μm of resist and etched in a single wafer plasma reactor. A three step etch was used to remove both the nitride and polysilicon layers stopped in the underlying pad oxide, leaving ~ 100 Å of oxide. The nitride was etched in a plasma of CHF_3 - Ar - CF_4 - O_2 at 600 W, followed by a polysilicon etch in Cl_2 at 100 W and a polysilicon overetch step in Cl_2 - He - O_2 at 80 W. The nitride etch time was adjusted for each nitride thickness.

After resist strip, the wafers received a 100:1 HF etch for 1 minute prior to a 6300 Å field oxidation . The field oxidation conditions were the same as the standard LOCOS process referenced earlier. Wafers from each split were pulled after field oxidation for SEM (Scanning Electron Microscopy) cross-sections to determine the length of the "bird's beak" encroachment. A blanket layer of TEOS (Tetraethyl orthosilicate) glass was deposited on the wafers to allow decoration of the field oxide profiles.

TABLE 3. Poly-buffer LOCOS Process Sequence

- 150 Å Oxide (850 ° C)
- 500 Å Poly Buffer Layer (LPCVD)
- 2400 Å Nitride Layer (LPCVD)
- Active Device Region Patterning
- Plasma Etch of nitride and polysilicon layers
- Resist Strip
- 100:1 HF (1 minute.)
- 6300 Å Oxide (HIPOX)
- 15:1 HF (2 minutes)
- Nitride Etch (Hot Phosphoric Acid)
- Plasma Etch of polysilicon layer
- 15:1 HF (2 minutes)
- 600 Å Oxide (900 ° C, steam)
- 15:1 HF (3.5 minutes)

The poly-buffer stack removal over the active device regions was done layer by layer. After field oxidation the oxynitride film was removed by a 15:1 HF etch followed by a Hot Phosphoric etch of the nitride layer. Hot Phosphoric acid has excellent selectivity to Si and SiO_2 as shown in Figure 6. The etch time of each group was adjusted to give a 50% overetch of the nitride layer. The polysilicon layer was removed in a plasma reactor using a two step etch. The first step in CHF_3 - O_2 removed any oxide present on the polysilicon layer and etched ~ 300 Å of field oxide. This was followed with a in-situ polysilicon etch in NF_3. The conditions were adjusted to give a 15:1 selectivity of polysilicon to oxide . The polysilicon etch endpoint was detected and a 100% overetch was added. The remaining pad oxide measured ~ 100 Å. The polysilicon etch was followed by a 15:1 HF etch for 2 minutes to strip the pad oxide and "bird's beak" oxide prior to a 600 Å sacrificial oxide grown at 900°C in steam. This sacrificial oxide was stripped prior to a 150 Å gate oxide immediately followed by a 3600 Å polysilicon deposition.

In a second experiment, wafers fabricated with the poly-buffer LOCOS process , listed in Table 3, were used to evaluate two other methods of polysilicon removal, that are described in detail below.

NF_3 is an anisotropic etchant and is commonly used for gate patterning and etching polysilicon at a rate of ~ 1500 Å/minute. SF_6 is a highly isotropic etchant with a much higher polysilicon etch rate ~ 4000 Å/minute and under similar conditions to the NF_3 etch process has a > 30:1 selectivity to oxide. [16] [17] Both polysilicon etch chemistries were evaluated.

The removal of the polysilicon layer through oxidation was also evaluated. After the nitride layer was removed in hot phosphoric acid, the polysilicon layer was oxidized in two steps using a grow / strip / grow methodology. First, the polysilicon layer was oxidized at 900 °C in steam for a time equivalent to a 600 Å oxide growth on a bare silicon control wafer. This oxide was stripped using 15:1 HF for 3.5 minutes followed by a megasonic ammonium hydroxide peroxide clean. The wafers were then oxidized for a second time (also at 900 °C) in steam for a time equivalent to a 450 Å oxide growth on a bare silicon control wafer. This second oxide was also stripped in 15:1 HF for 2.5 minutes prior to the 150 Å gate oxidation and polysilicon deposition.

All plasma polysilicon removal cells received a sacrificial oxide after the field oxide and active device region formation. The sacrificial oxide is stripped in HF and a 150 Å gate oxide is grown at 900°C. A 3600 Å LPCVD polysilicon layer is then immediately deposited on the oxide surface. The gate electrode was patterned with reactive ion etching (RIE) and devices continued through to window etch before being tested.

Wafers from all experimental groups were pulled immediately prior to gate oxidation for surface SEM evaluation. The remaining wafers were processed through window etching and then electrically tested to calculate defect density by evaluation of gate oxide quality.

After testing, one wafer from each nitride experimental group was etched to decorate process-induced stacking faults. The wafers were etched in buffered HF for 6.5 minutes to remove the oxide and expose the polysilicon gate electrode. The polysilicon was then removed in 2.5 minutes of KOH at 65°C. An area .0014 cm^2 was inspected. The sites inspected did show some gate oxide defects, indicating point of gate oxide breakdown. The wafers were then SECCO etched for 4 minute, with an inspection after 2 minutes and 4 minutes.

3.3 Test Structures

Devices fabricated using the poly-buffer LOCOS process have a large area gate level electrode which covered an array of small active device regions. The electrode terminated up

on field oxide to eliminate leakage current paths at the electrode edge. The array is 5 x 11 major blocks. Each major block is subdivided into a 5 x 5 array, a diagram is given in Figure 7. These secondary arrays are divided into three regions each containing a 10 x 10 array of 2.25 x 11.75 μm sized active device regions on 1.75 μm minimum spacings, a diagram is given in Figure 8. The total active area was 0.101 cm^2 with a field oxide to active device region perimeter of 106.96 cm. [18]

3.3.1 Test Conditions High quality SiO_2 films will typically give breakdown at electric fields of 5 - 10 MV/cm . The exact value is a function of oxidation and annealing conditions, oxide charges, surface crystallographic orientation, and surface preparation. For this study gate oxide break down was used as a measure of the surface quality after the poly-buffer LOCOS isolation process. All other factors were held constant .

All devices on a wafer were probed. To be considered for evaluation of gate oxide quality a die must pass both probe and scratch test. The probe test checks contact resistance of every probe. If a probe does not make contact or exhibits too high a contact resistance the die fails probe test. The scratch test checks for severe mechanical damage of the alumimun and silicide levels, which every test structure depends on. If a die fails either test it is disqualified from further analysis.

The defect density is calculated at three applied voltages; 2, 5.5, and 10 volts. The criterion for failure is a current density in excess of 100 $\mu A/cm^2$. The defect densities are computed from the simple Poisson model.

$$D_0 = -ln\ (Y)\ /\ A$$

where D_0 is the defect density, Y is the yield and A is the active device area evaluated.

A confidence limits analysis was done at 5.5 volts. Low and high confidence limits are computed for a 95% level of confidence. These limits indicate that the true defect density lies somewhere between the low and high limit, and were used to compare defect densities of experimental groups.

Results of electrical testing were normalized with the LOCOS group processed with each experimental group. This was done due to the proprietary nature of the exact values. The 95% confidence values are reported as the delta from the average defect density for that experimental group.

4. Results

The test devices were evaluated both structurally and electrically. Structural evaluation was by top view and cross-sectional SEM micrographs. Electrical evaluation was made in comparison to a standard LOCOS cells fabricated with the experimental wafers

4.1 Nitride Thickness Evaluation

Wafers were pulled after the 6300 Å field oxidation for "bird's beak" encroachment measurements. Bird's beaks were measured on several SEM micrographs as the distance between the encroachment point and the masking nitride edge vertical projection. The results are listed in Table 4 and SEM cross-sections are shown in Figures 9 and 10.

TABLE 4. Bird's Beak Size Dependence on Nitride Thickness

	Bird's beak size Nitride thickness Splits			
	1600Å	2000Å	2400Å	2800Å
Bird's beak size	0.414μm	0.345μm	0.313μm	0.300μm

The fully processed device wafers were tested to electrically measure defect density as a function of gate oxide leakage current. The failure criteria was a measured leakage of 100 $\mu m/cm^2$ amperes. The result of the defect density per cm^2 of the active device area were normalized with the measured defect density per cm^2 for the standard LOCOS group. The results are listed in Table 5, and the 95% confidence limits of defect density for the 5.5 volt measurement are given in Table 6.

TABLE 5. Defect Density Dependence on Nitride Thickness

Normalized Defect Density per cm^2				
Stress	Nitride thickness Splits			
Voltage	1600Å	2000Å	2400Å	2800Å
2 volts	0.27	0.24	0.22	0.22
5.5volts	0.24	0.22	0.17	0.20
10 volts	0.90	0.96	0.93	0.91

The results show that the "bird's beak" lateral encroachment decreased with increasing nitride thickness, but were larger than those reported by M. Ghezzo for the 0.8 μm LOPOS process (Table 2). The average defect density of all experimental groups were less than the standard LOCOS group, and there was no statistical difference in the defect density due to nitride

TABLE 6. Nitride Splits : 95 % Confidence Limits at 5.5 volts

Nitride Splits 5.5 volt 95 % Confidence Limits			
Nitride Tk.	# of sites	Delta	
1600 Å	392	-0.29	+0.46
2000 Å	392	-0.24	+0.36
2400 Å	336	-0.22	+0.37
2800 Å	336	-0.25	+0.43

Delta values are the difference from the average defect density for a given group.

thickness.

4.2 Polysilicon Removal Method Evaluation

Wafers for this study were processed with a poly-buffer LOCOS stack of a 150 Å oxide, 500 Å polysilicon and 2400 Å nitride as described in Table 3. Wafers were pulled after polysilicon removal and prior to gate oxide growth for SEM evaluation. Electrical measurement of gate oxide breakdown was again used as an assessment of active device surface quality.

Wafers were etched to remove the polysilicon buffer layer with a two step etch in a batch plasma reactor. The first step in CHF_3 - O_2 was the same for both plasma etches evaluated. For the NF_3 and SF_6 cells, a 1 minute. etch was evaluated. This etch time was optimized for maximum polysilicon removal and no visible pad oxide break - through SEM micrographs of active device regions after polysilicon removal are shown in Figures 11. Although the surface is not smooth no visible pitting of the active device regions is observed. Figures 12 and 13 show close ups of the active device region's surface prior to gate oxidation. The surfaces show no pitting but the edges and corners, in particular, show scalloping.

A group of wafers were used to evaluate the removal of the polysilicon layer through oxidation. A grow / strip / grow methodology was used, as discussed in section 3.2. Figure 14 shows SEM micrographs of active device regions after removal of the polysilicon buffer layer oxidation prior to gate oxidation. The surface is much rougher with a pattern which suggest memory of the polysilicon grain structure. The edges are much worse, but even inside areas show a non-uniform surface. For comparison, Figure 15 shows the active device

regions prior to gate oxidation of the standard LOCOS group. Electrical defect density measurements are given in Table 7, and the 95% confidence limits for the 5.5 volt test are given in Table 8.

TABLE 7. Defect Density Dependence on Polysilicon Removal Method

Normalized Defect Density per cm^2			
Poly removal Method	Stress Voltage		
	2 Volts	5.5 volts	10 volts
Plasma (NF_3)	0.43	0.31	0.68
Plasma (SF_6)	0.11	0.10	0.95
Oxidized	1.02	0.99	26.81

* The defect density was again normalized to the standard LOCOS cell fabricated with the experimental wafers.

TABLE 8. Polysilicon Removal Splits : 95% Confidence Limits at 5.5 volts volts 95 % confidence limits"

Polysilicon Removal Methods 5.5 volt 95 % Confidence Limits			
Method	# of sites	Delta	
Plasma NF_3	392	-0.32	+0.42
Plasma SF_6	336	-0.17	+0.28
Oxidized	168	-0.33	+0.95

Delta values are the difference from the average defect density for a given group.

Defect densities for the two groups which had the polysilicon removed using NF_3 or SF_6 plasma are significantly lower than the group which had the polysilicon removed by oxidation. This was expected from comparison of the surfaces of the active device areas prior to gate oxidation. From the SEMs, the oxidized group shows a rough surface texture. A non-uniform surface will cause small localized areas of increased electric field under gate bias resulting in a oxide breakdown. Both the SF_6 and NF_3 groups resulted in significantly lower defect densities than the standard LOCOS group, with the SF_6 group measuring slightly better.

5. Discussion

5.1 Nitride Thickness Split Evaluation

The experiment investigating the effect of the nitride thickness on the length of the "bird's beak" encroachment agreed with the work of M. Ghezzo at General Electric. A decrease in the length of the "bird's beak" was observed with an increase in nitride thickness, but no adverse effects on the quality of the active device area were measured . A comparison of measured "bird's beak" lengths verses nitride thickness is given in Figure 16.

The length of the "bird's beak" encroachment was significantly longer than those measured by M. Ghezzo at General Electric. There could be several reasons; a) differences in the way the "bird's beak" encroachment was measured, b) differences in pad oxide thicknesses, and c) differences in the field oxidation conditions. For my measurements I used the same method reported by M. Ghezzo which should minimize the difference due to measurement technique. The pad oxide used for my experiments was 150 Å. This thickness was between two of Ghezzo groups, allowing correlation of experiments. The major difference was field oxidation conditions ; I grew 6300 Å of oxide in HIPOX (HIgh Pressure OXidation) at a temperature less than 1000 ° C, Ghezzo grew 6000 Å of oxide at 1000 ° C (other growth conditions not reported).

The silicon oxidation process has three stages; a) the transport of the oxidizing species to the vicinity of, and adsorption into the oxide surface, b) the transport of the oxidizing species through the existing oxide layer , and c) the reaction of the oxidant at the Si/SiO_2 surface. The equation relating the growth time to the oxide thickness is

$$x_0^2 + A_{x_0} = B\ (t = \tau)$$

where:

1. x_0 = the oxide thickness
2. B = the parabolic rate constant
3. B/A = the linear rate constant
4. t = the oxidation time
5. τ = initialization parameter

In characterizing the oxidation process, the parabolic rate constant, B, is a function of the diffusivity of the oxidant in the oxide, its solubility in the oxide, and its partial pressure and predominates for thicker oxides. As shown in Figure 17, the linear rate constant, B/A, is most influential for shorter oxidation times and lower temperatures. [19] In work done by Wu and

Stacy, it was found that, for a fixed field oxide thickness, most of the reaction in High Pressure Oxidations takes place in the initial growth regime where the linear rate constant, B/A, is dominant and results in a slightly longer "bird's beak". [2] In their study, which looked at the effect of different field oxidation conditions on the length of the "bird's beak" encroachment, they found that the length of the "bird's beak" encroachment was very dependent on the temperature of the field oxidation and slightly dependent on the pressure . Their results are shown in Figure 18. Therefore the differences in the field oxidation conditions, predominately temperature, would explain the large difference in measured "bird's beak" encroachment.

A major difference from the study by M. Ghezzo was in the observance of process - induced stacking faults. Ghezzo reported the presence of process - induced stacking faults for all groups where the nitride to pad oxide ratio was greater than 10:1. In this study I looked at nitride to pad oxide ratios of 10:1, 13:1, 16:1, and 20:1, and no stacking faults were found . My results agree with the results from Sony and Texas Instruments. Both report finding no process - induced stacking faults with their poly - buffer LOCOS isolation schemes, which have nitride to pad oxide ratios greater than 20:1. This difference may be due to the deposition conditions of the nitride and polysilicon layers. These deposition conditions will have an effect on the amount of stress induced by the nitride and the amount of stress relieved by the polysilicon layers.

5.2 Polysilicon Removal Split Evaluation

The polysilicon removal step is critical to obtaining a smooth active device region. During field oxidation the "bird's beak" is forming, and a portion of the polysilicon buffer layer is being oxidized. Cross-Sectional SEM micrographs, Figure 19, show the existence of a small secondary bird's beak at the polysilicon/nitride interface. This secondary "birds beak" is due to the presence of an oxide layer on top of the polysilicon buffer layer prior to nitride deposition. The oxide layer permits lateral diffusion of the oxidant during field oxidation as does the pad oxide and as a result, the polysilicon buffer layer is oxidized from both top and bottom. The oxidation of the polysilicon buffer layer is also enhanced by the exposure of the polysilicon sidewall surface by the stack definition etch. During the field oxidation the polysilicon edges are partially oxidized to form a polysilicon oxide, SiO_x. SEM micrographs of the active device regions after selective polysilicon removal show the effects of this oxidation. Figure 20 shows residual polysilicon/oxide left in the corners and small active device regions. The presence of this polysilicon/oxide creates a problem with polysilicon removal. An etch with very high selectivity of polysilicon to oxide will not remove the polysilicon encased in a thin oxide layer and an etch with low selectivity of polysilicon to oxide will breakthrough the thin pad oxide layer protecting the active device regions.

Pitting of active device areas by the polysilicon removal etch is illustrated in Figure 21. The pitting is located at approximately the point of the extension of the major bird's beak indicating that the polysilicon layer may be discontinuous either through oxidation along grain boundaries or breakup from stress induced by the double bird's beak formation. This pitting of active device regions is only observed intermittently.

SF_6 is known to be a very isotropic etch with a selectivity of polysilicon to oxide on the order of 40:1 . Therefore it will be very effective in removing polysilicon which may be encased in a SiO_2 coating as long as the SiO_2 film is thin. The isotropic nature of this etchant makes SF_6 ideal for a cleaning out type etch. The difficulty with SF_6 is its high etch rate of silicon ~ 4000 Å/minute. It will drill holes in the silicon surface if it breaks through the underlying pad oxide. Figure 22 shows the effect of a 1 minute 40 seconds SF_6 etch of the polysilicon buffer layer. Breakthrough of the pad oxide is very evident.

NF_3 has a lower etch rate to silicon, ~ 1500 Å/minute, a selectivity of Si to SiO_2, ~ 15:1. If we assume that both SF_6 and NF_3 can remove the thin oxide, then the more iostropic etch in SF_6 would be more effective at removing any residual polysilicon.

The SEM micrographs of active device regions after polysilicon removal etch shown in Figure 11 display little difference between NF_3 and SF_6. The corner areas, which due to oxidation from two sides are more prone to the formation of SiO_x, both exhibit ragged field oxide to active device area edges. The electrical measurements of gate oxide defect density indicate that the SF_6 etch may be slightly superior to NF_3 with a lower defect density and tighter distribution. The increase in the measured defect density for both the SF_6 and NF_3 plasma etch at 10 volts may be due to corner roughness.

The effect of a very rough surface is seen with the experimental group in which the polysilicon was removed by oxidation. SEM micrographs of active device regions prior to gate oxidation show a very textured surface . This texture is most likely caused by the non-uniform oxidation of the polysilicon buffer layer at the top and bottom interface. A non uniform surface will cause small localized areas of increased electric field under gate bias resulting in a greater probability of gate oxide breakdown. Interestingly , the 2 and 5.5 volt measurements of gate oxide defect density show only a slight increase as compared to the standard LOCOS group, but at 10 volts a 26 x greater density of defects is measured. This indicates that the 2 and 5.5 volt measurements are not sensitive to slight irregularities of the active device region, but 10 volts is. This supports the idea that the increase in measured gate oxide defects at 10 volts of the plasma polysilicon groups is due to the scalloping around the edges.

Another possible reason for this increase in gate oxide defect density at 10 volts may be the final active device region profile. Cross sectional SEM micrographs of active device regions

after polysilicon gate deposition show the field oxide edge is below the active device region. This profile, shown in Figure 23, if steep enough, will result in a higher electric field concentration at this edge and subsequently a lower gate oxide breakdown. This profile was commom in all experimental groups . For my study the amount of HF etch, after active device region formation, was held constant and not optimized for final active device region profile.

5.3 General Processing Issues

The increase in the gate oxide defect density at 10 volts shows that the poly - buffer LOCOS process as performed in this study is not optimized for gate oxide quality. An improvement may come from changing the stack etch to leave some or all of the polysilicon buffer layer behind prior to field oxidation. The major advantage of this method is that vertical oxidation of the exposed polysilicon layer may limit the amount of oxidant available for lateral diffusion and oxidation of the underlying polysilicon. A second improvement could come from a change in the field oxidation conditions to a higher temperature and different pressure or using a high temperature steam oxidation to limit lateral diffusion of the oxidant. Also, work is needed to determine the optimum cleaning and sacrifical oxidation process prior to gate oxidation.

The small secondary "bird's beak" which can form at the nitride polysilicon interface should be minimized, but it is not clear how much of an effect it has on the amount of polysilicon/oxide formed during field oxidation. Texas Instruments[10] reported that they observed a polysilicon/oxide residue in the active device regions after their polysilicon removal etch, (plasma SF_6). A cleaning sequence of a 12 minute megasonic cleaning performed in 1:1:5 NH_4OH, H_2O_2, H_2O was found effective in removing the residues remaining from the plasma etch. But, they also report that a small amount of scalloping is observed along the field oxide transition region in narrow inside corners. They attribute this scalloping to enhanced stress effects and non-uniform oxidation of the polysilicon along its grain boundaries.

Another factor in this problem is the variability in the poly removal itself. Using a batch plasma reactor requires a considerable overetch (100 %) to ensure that all 18 positions are cleared . A single wafer etcher is being evaluated.

6. Conclusions

The use of Poly-buffer LOCOS as a method of electrical isolation of active devices in integrated circuits has been evaluated for its effect on gate oxide quality. Two studies were conducted: 1) an evaluation of the "bird's beak" length and generation of process - induced stacking faults as a function of nitride thickness, and 2) an evaluation of active device surface quality as a function of the polysilicon removal method. The results are summerized below.

1. The "bird's beak" length decreased with an increase in nitride thickness.
2. No process - induced stacking faults were observed in active device areas on any wafer.
3. Low gate oxide defect densities were measured on all nitride thickness groups.
4. Low gate oxide defect densities were measured for groups using plasma etch removal of the polysilicon buffer layer after field oxidation.
5. A large increase in gate oxide defect density was measured at 10 volts when the polysilicon buffer layer was removed through oxidation due to surface roughness.
6. All devices fabricated with the poly - buffer LOCOS process listed in Table 3 resulted in a lower gate oxide defect density than standard LOCO S for 2 and 5 volt bias, with comparable yield at 10 volt bias..

7. Acknowledgements

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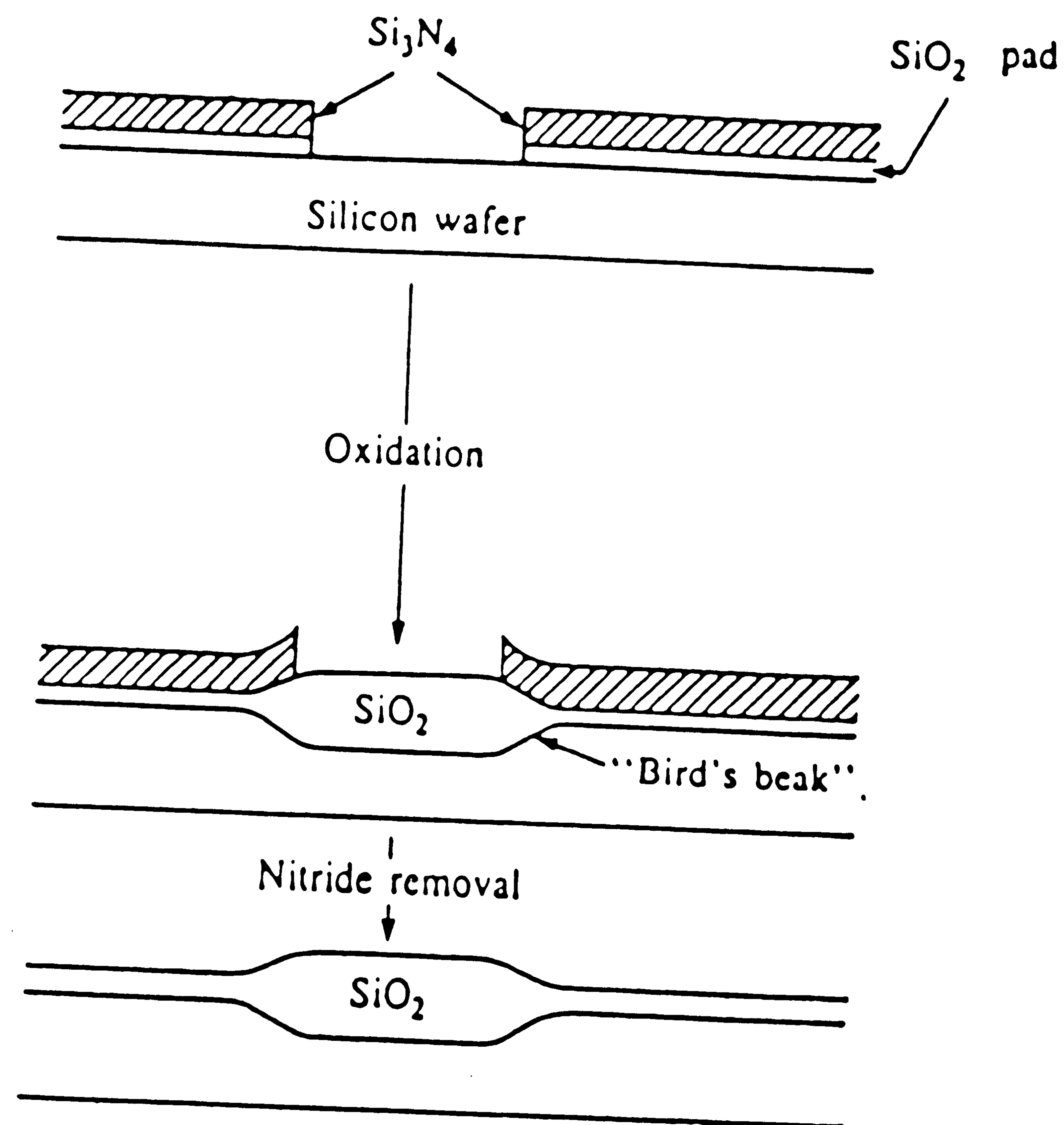
Most importantly the author wishes to thank her husband, John, for his love and support throughout these years of study.

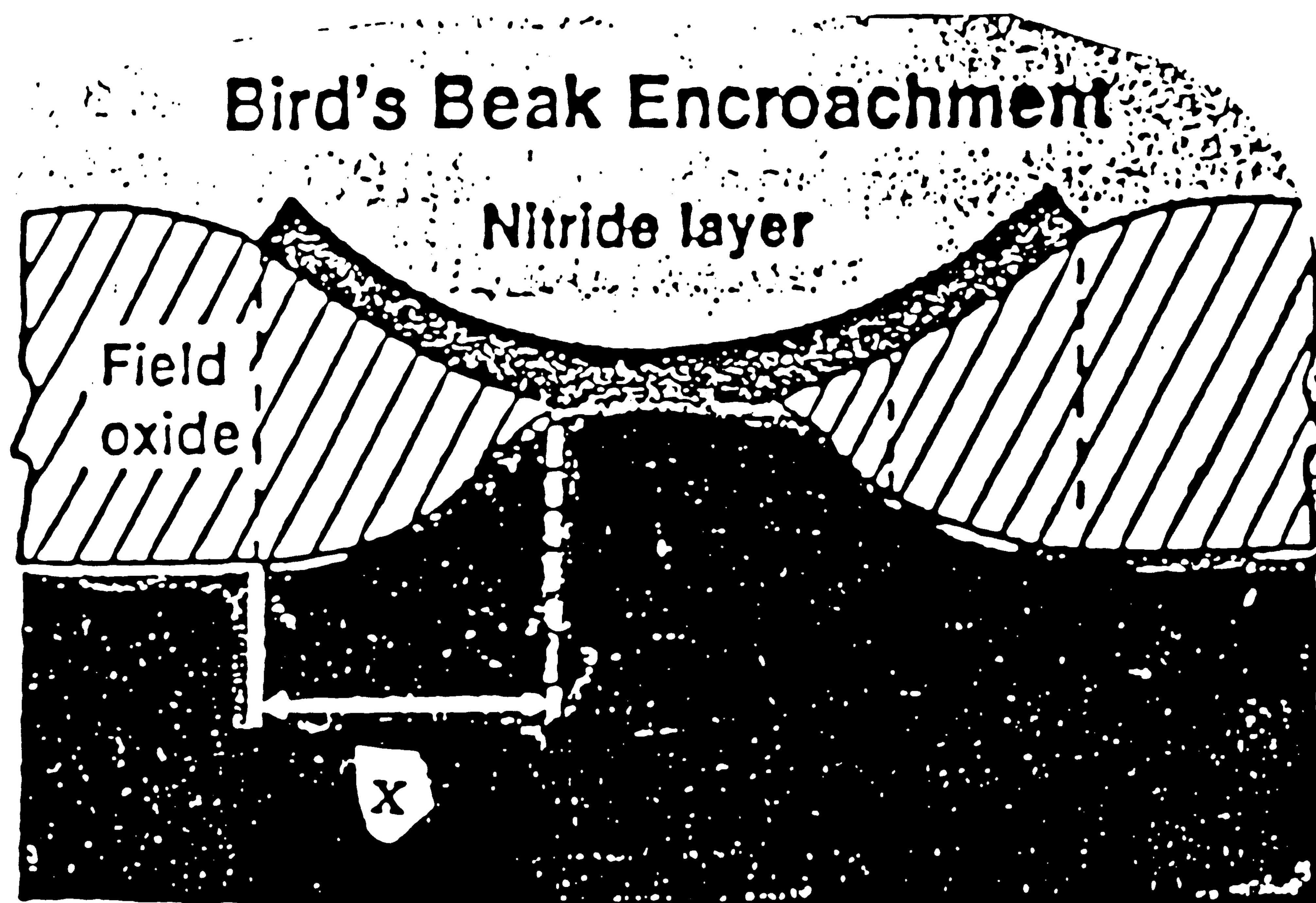
8. Figures

Figure 1. Standard LOCOS Processing Sequence



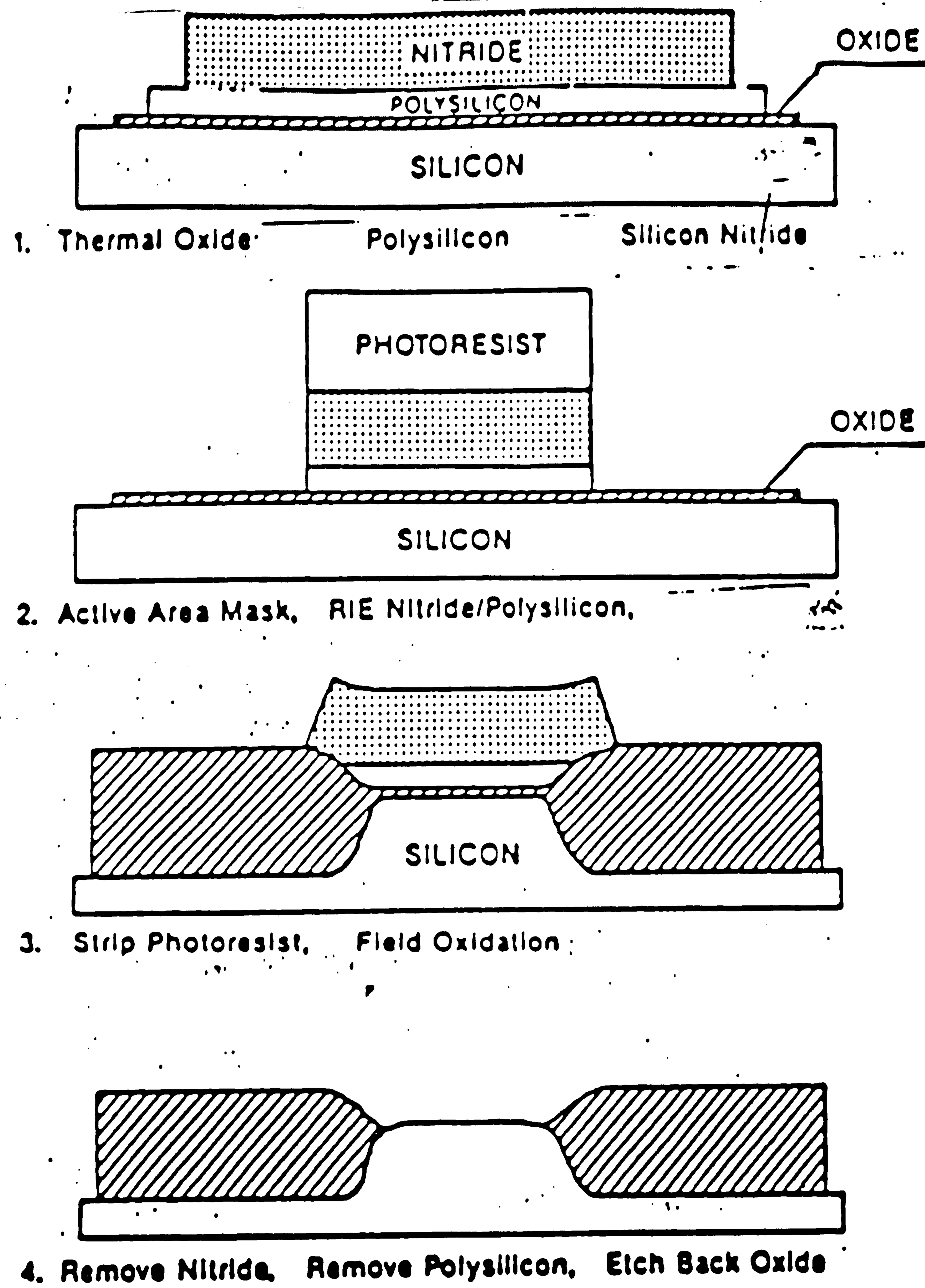
Cross section depicting process sequence for standard LOCOS a semirecessed isolation scheme. Reprinted from "Silicon Processing for the VLSI Era, vol 2" p 20.

Figure 2. Diagram of LOCOS Bird's Beak



X is the "Bird's Beak" Encroachment after field oxidation.

Figure 3. Patented Poly-buffer LOCOS Sequence

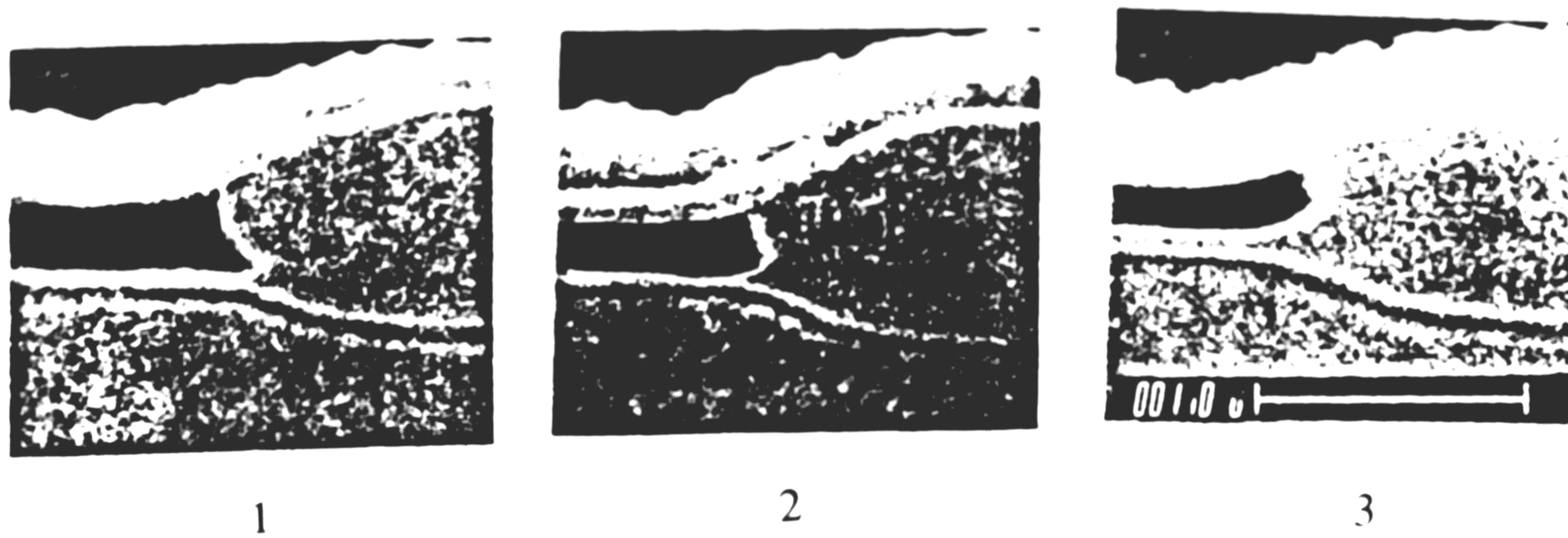


1. Stack Formation
2. Active Area Patterning
3. Selective Field Oxidation
4. Active Area Cleaning

Reprinted from M.Ghezzo "Journal of Electrochemical Society" July 1989.

Figure 4

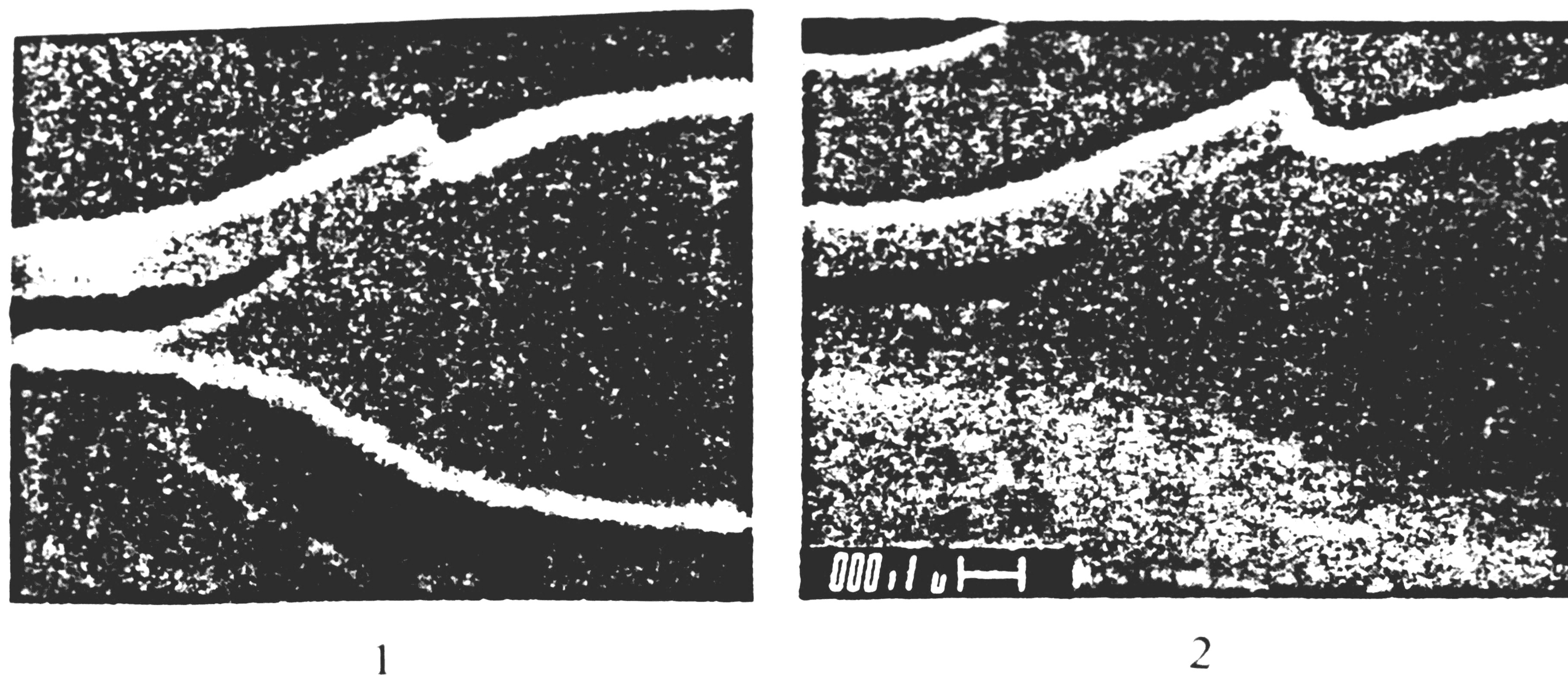
Effects of Polysilicon and Pad Oxide Thicknesses on Bird's Beak profile



1 2 3

1. 270 Å pad oxide and 2300 Å polysilicon
2. 270 Å pad oxide and 1700 Å polysilicon
3. 700 Å pad oxide and 1700 Å polysilicon

with 1000 Å nitride



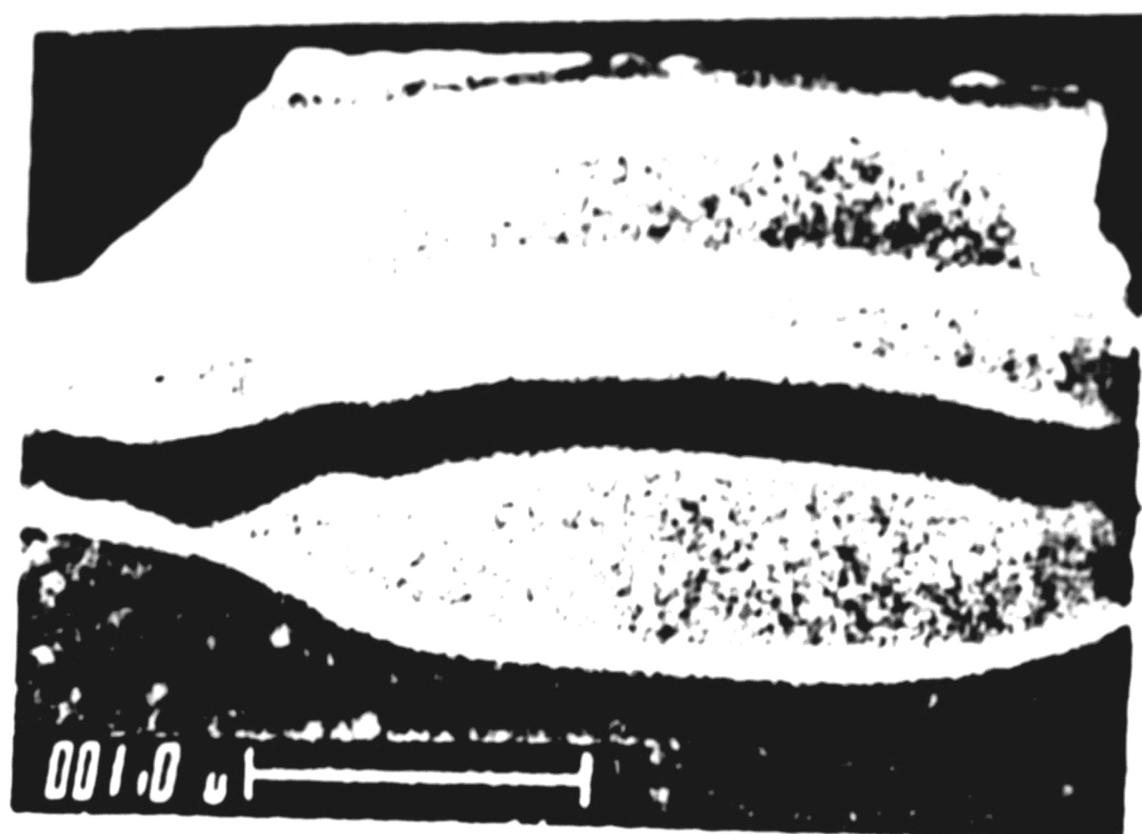
1 2

1. 260 Å pad oxide
2. 710 Å pad oxide

with 1000 Å polysilicon and 1000 Å nitride

Reprinted from Han and Ma "VLSI Science and Technology Electrochemical Society" May,1984.

Figure 5. Field Oxide Profiles : Prior to Gate Oxidation



1

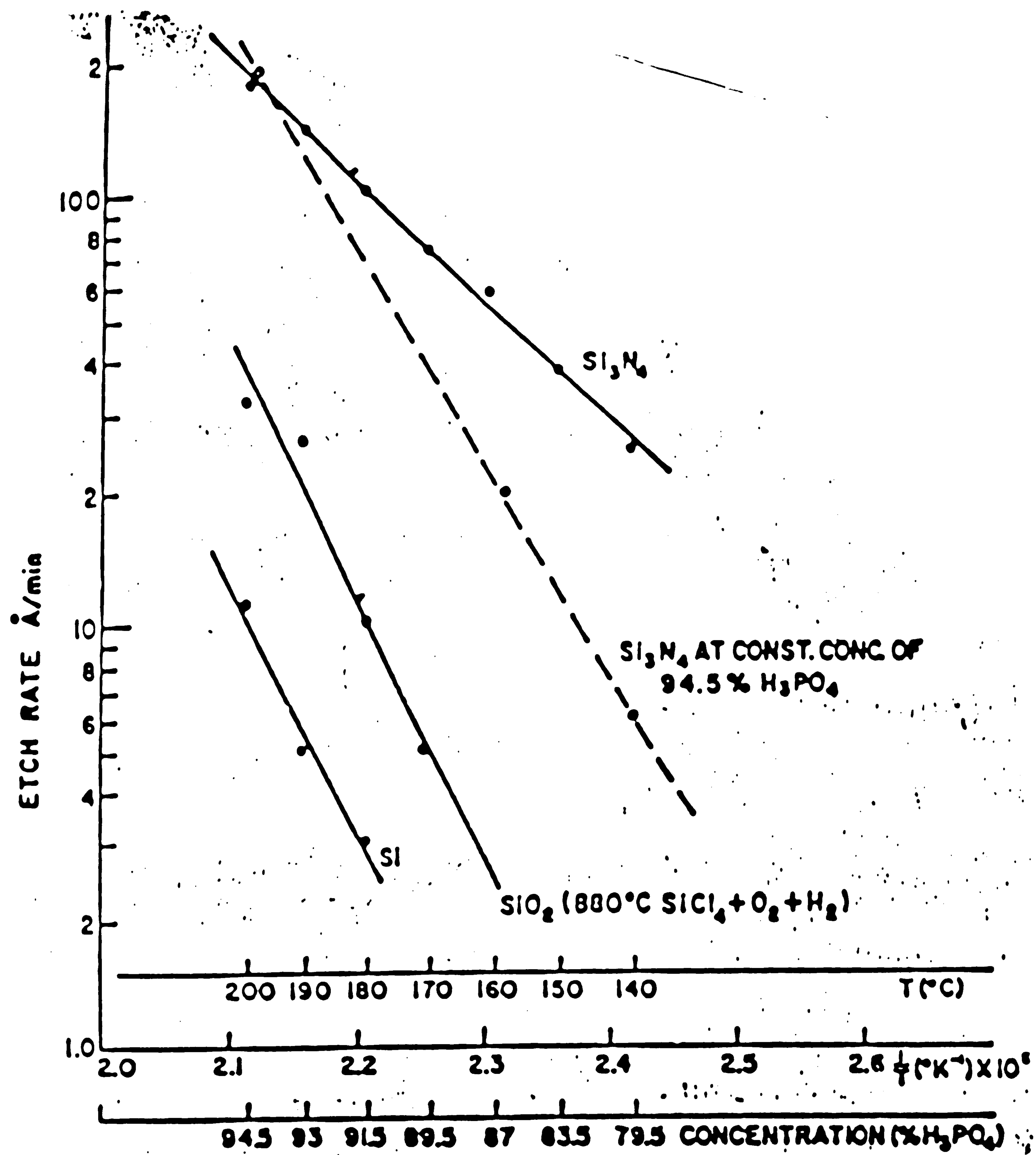
2

1. conventional LOCOS
2. 1500 Å polysilicon incorporated into 8000 Å field oxide.

Reprinted from Han and Ma "VLSI Science and Technology Electrochemical Society" May,1984.

3. Polysilicon removed prior to Field Oxidation

Figure 6. Etch Rates In Hot Phosphoric Acid



Solid lines: etch rate of Si_3N_4, SiO_2, and Si in refluxed boiling phosphoric acid at atmospheric pressure as a function of boiling temperature and acid concentration. Dashed line: etch rate of Si_3N_4 at a constant concentration of 94.5% H_3PO_4 as a function of temperature only (from Van Gelder and Hauser, The Electrochemical Society Inc.)

Figure 7. Test Structure

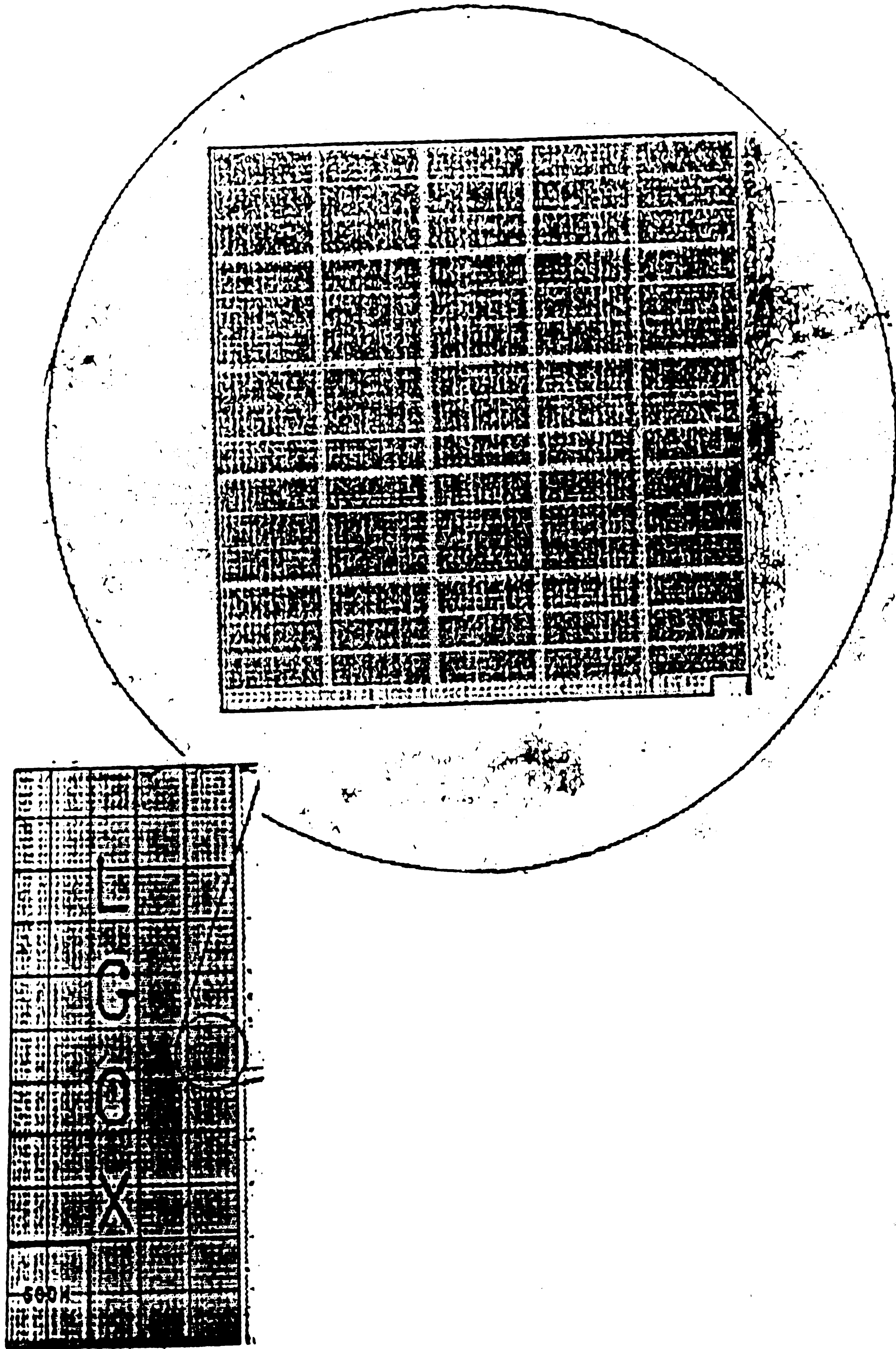


Figure 8. Test Structure Blowup

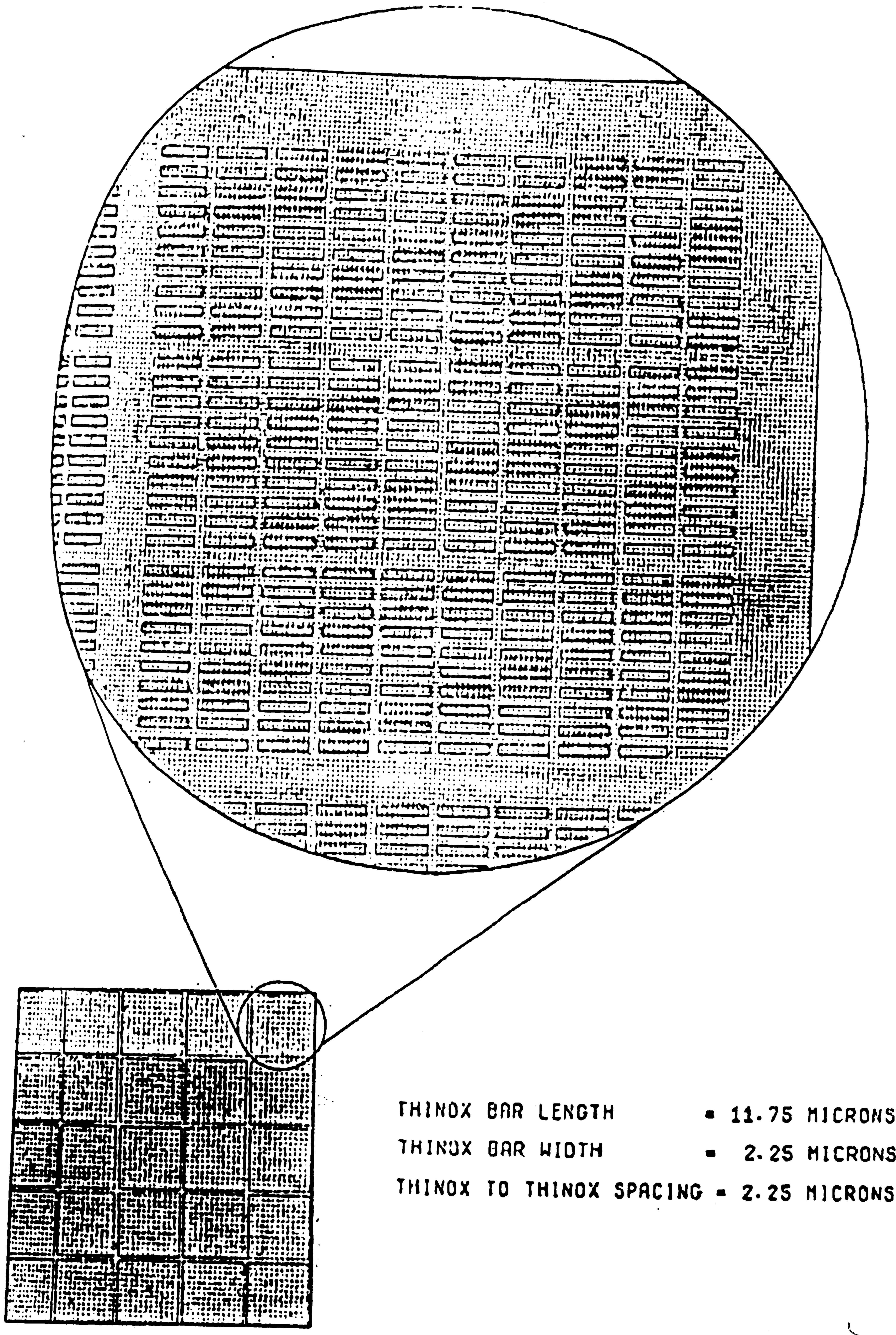


Figure 9. SEM cross-sections Nitride Splits 2800 and 2400 Å

2800 Å Nitride

2400 Å Nitride

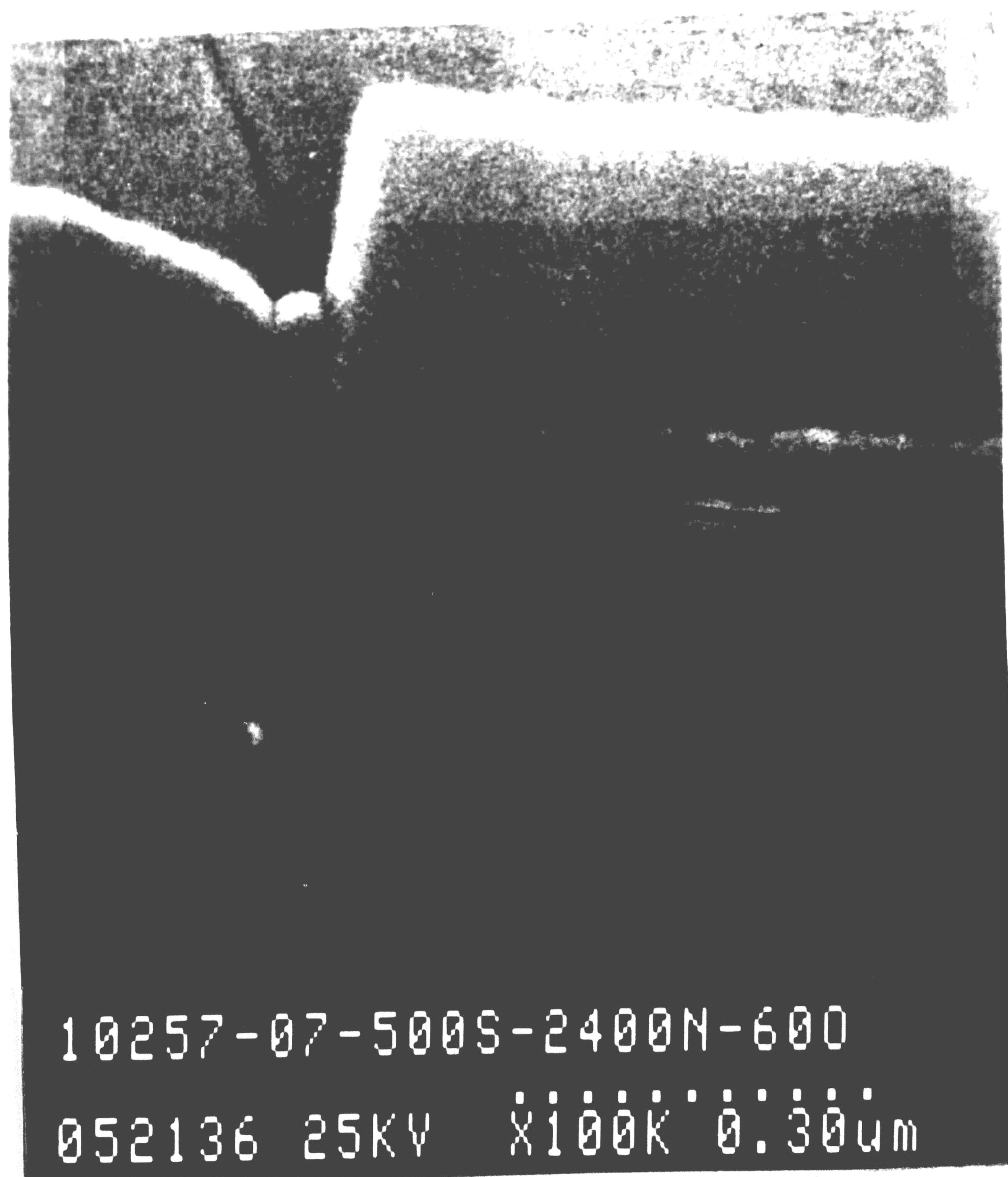


Figure 10. SEM cross-sections Nitride Splits 2000 and 1600 Å

2000 Å Nitride

1600 Å Nitride

Figure 11. SEM of Active Device Regions After Plasma Polysilicon Removal

NF_3 1 minute.

SF_6 1 minute.

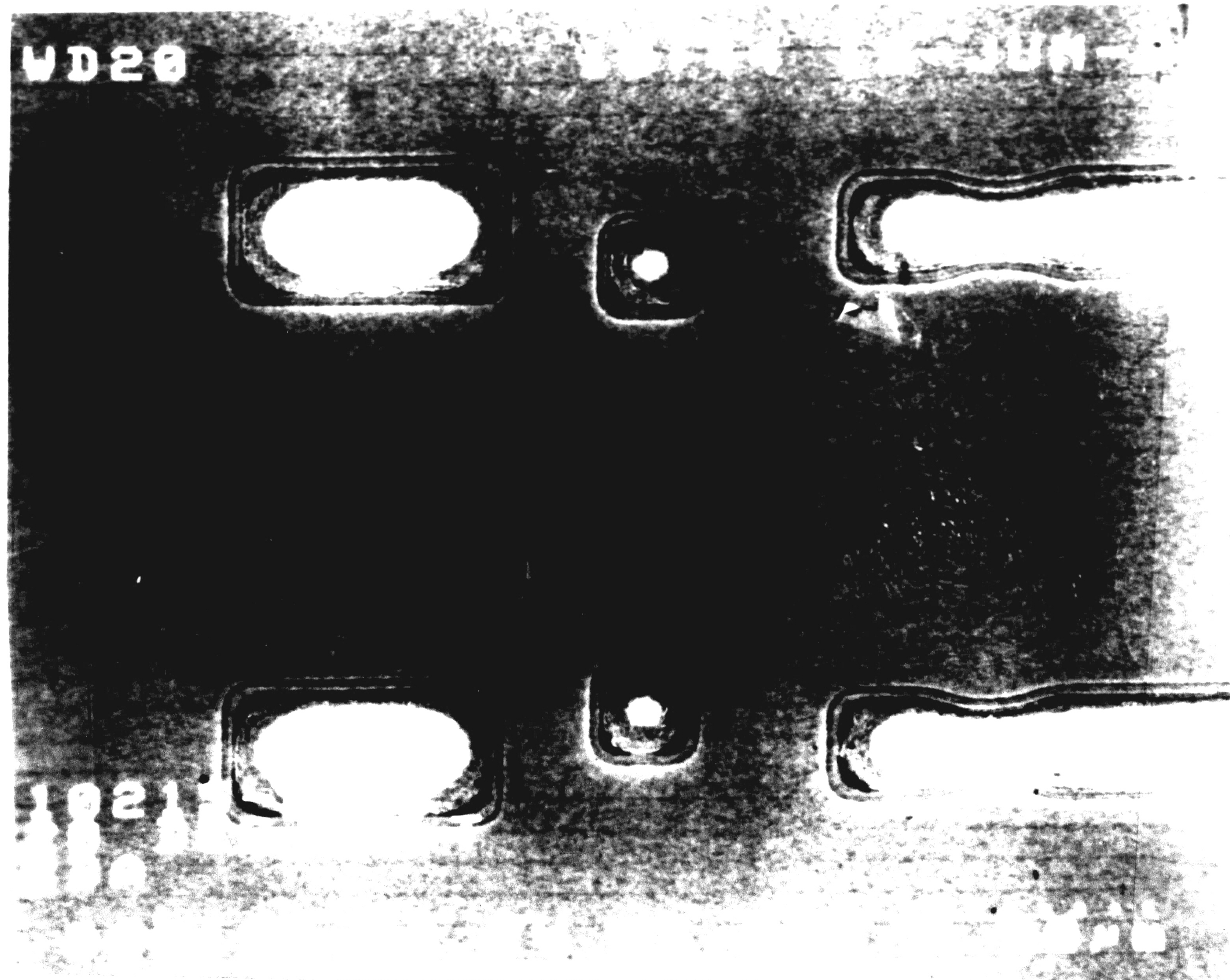


Figure 12. SEM of Active Areas prior to Gate Oxidation : NF_3

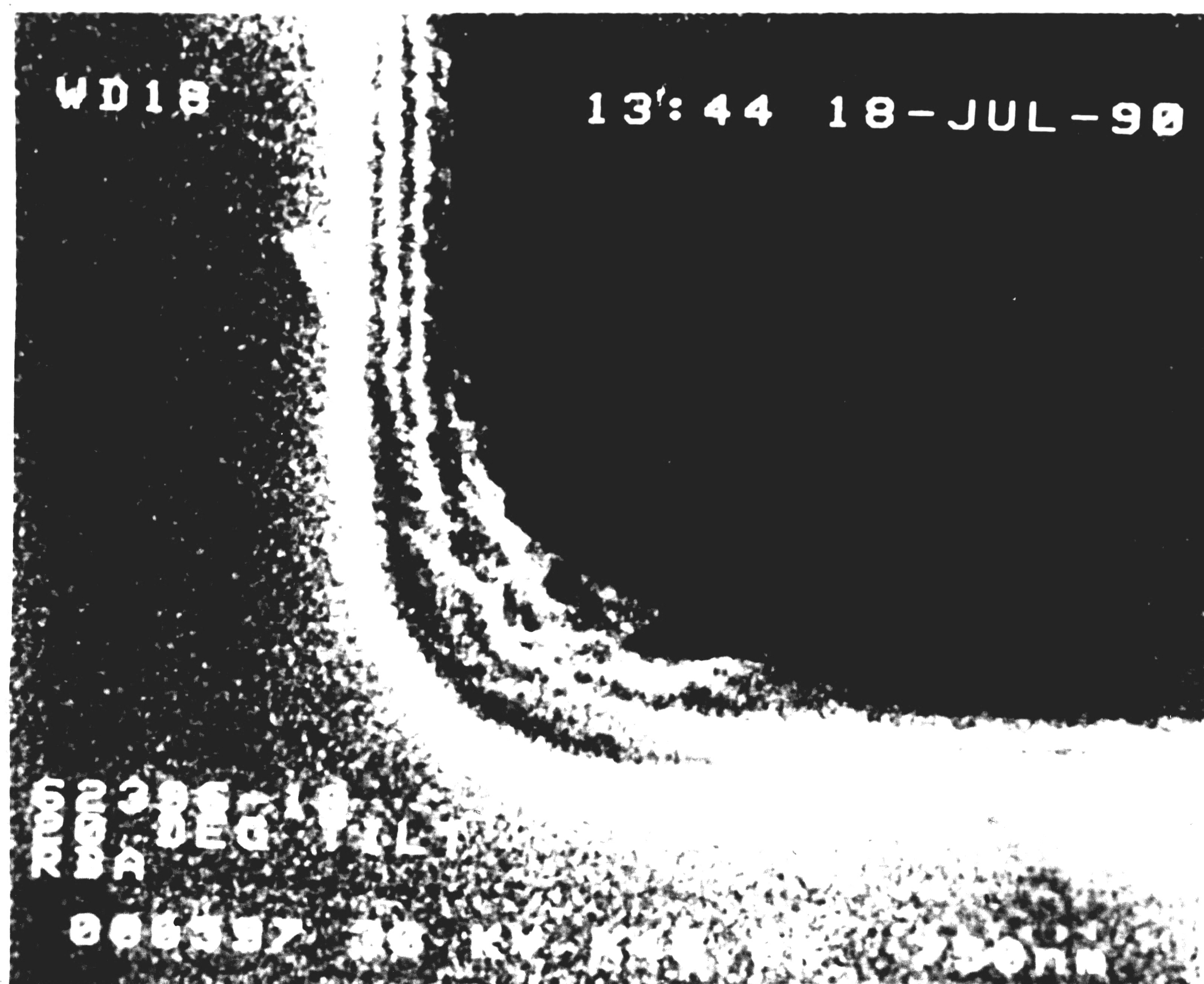


Figure 13. SEM of Active Areas prior to Gate Oxidation : SF_6

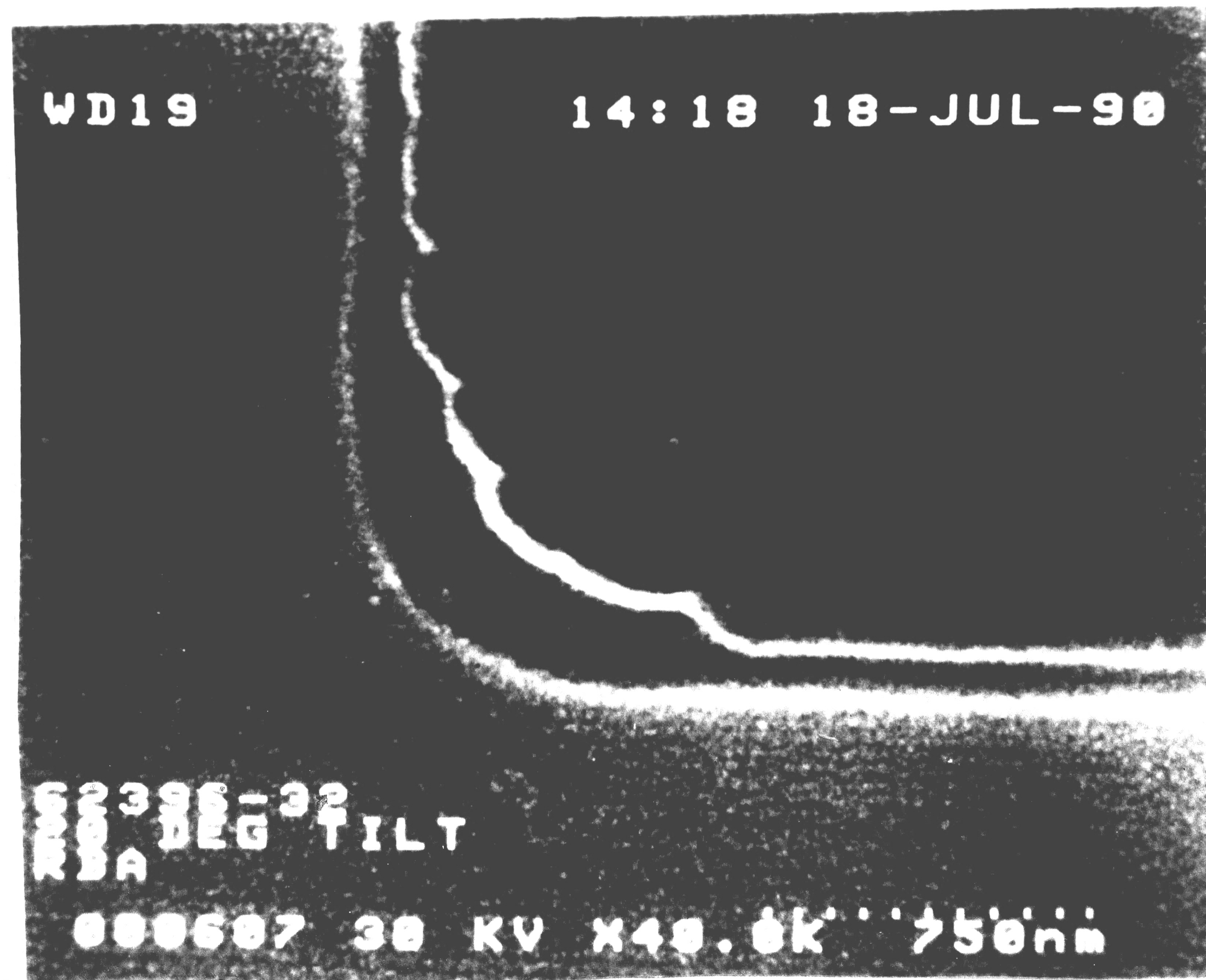


Figure 14. SEM of Active Areas prior to Gate Oxidation : **Oxidized**

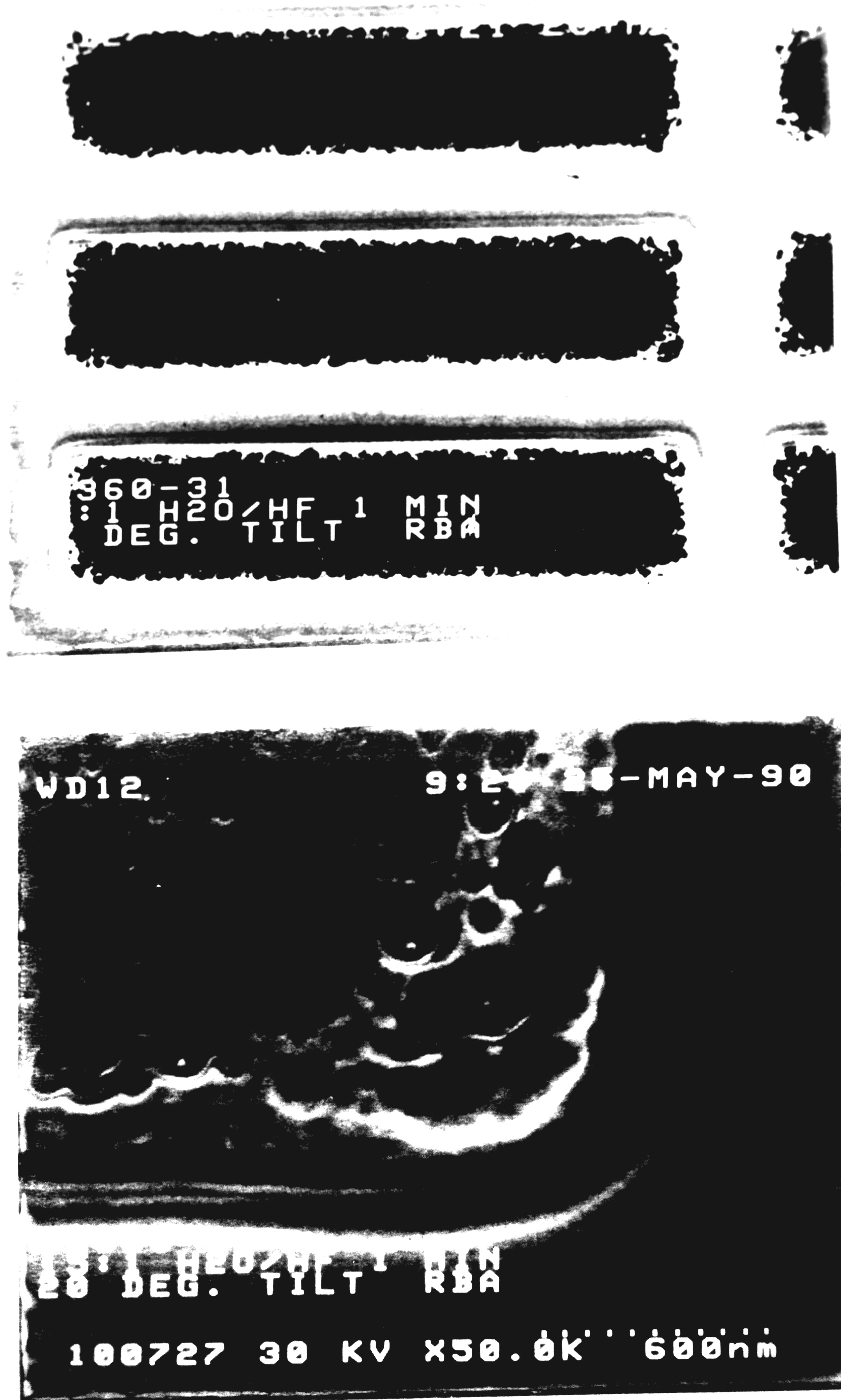
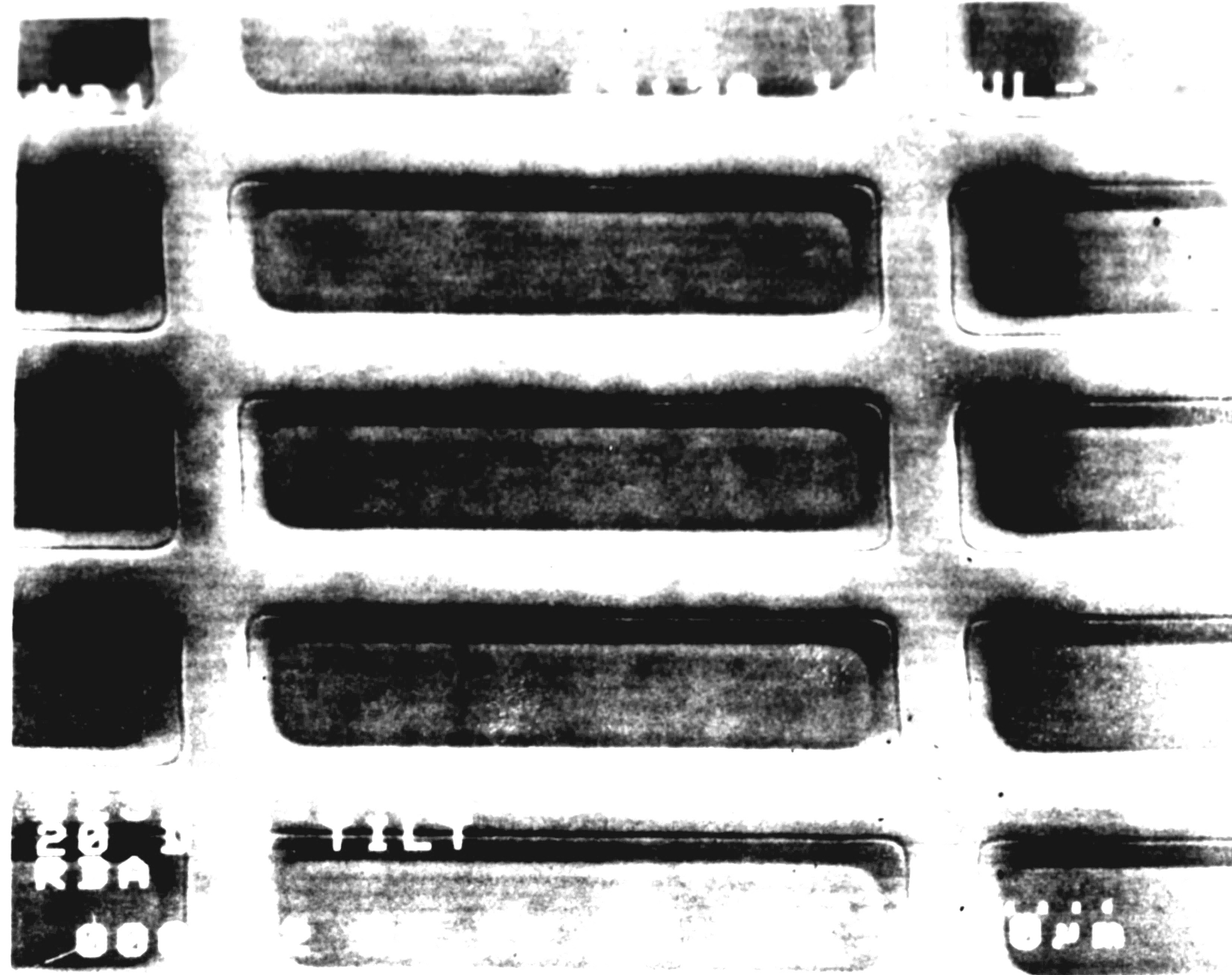


Figure 15. SEM of Active Areas prior to Gate Oxidation : Standard LOCOS



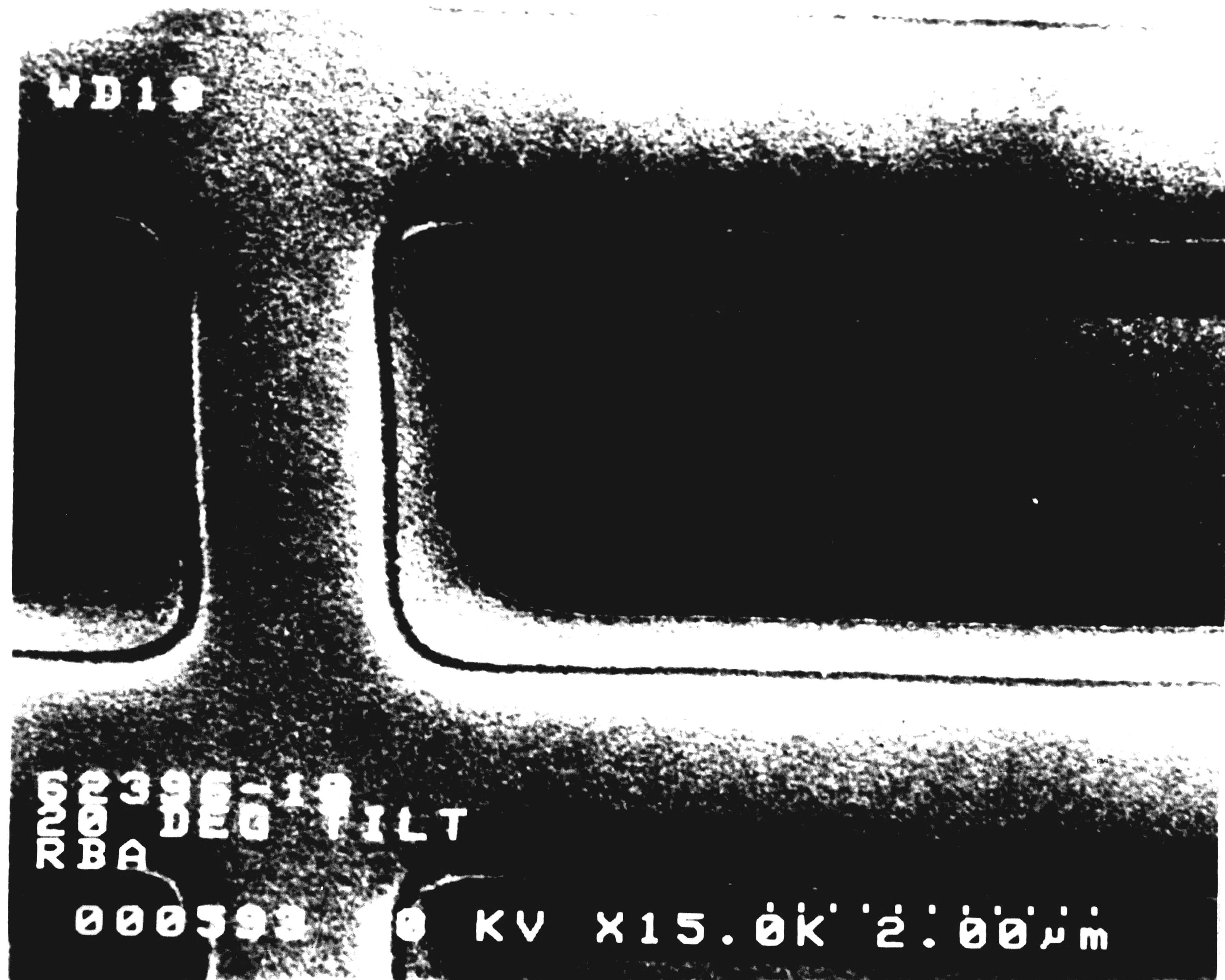
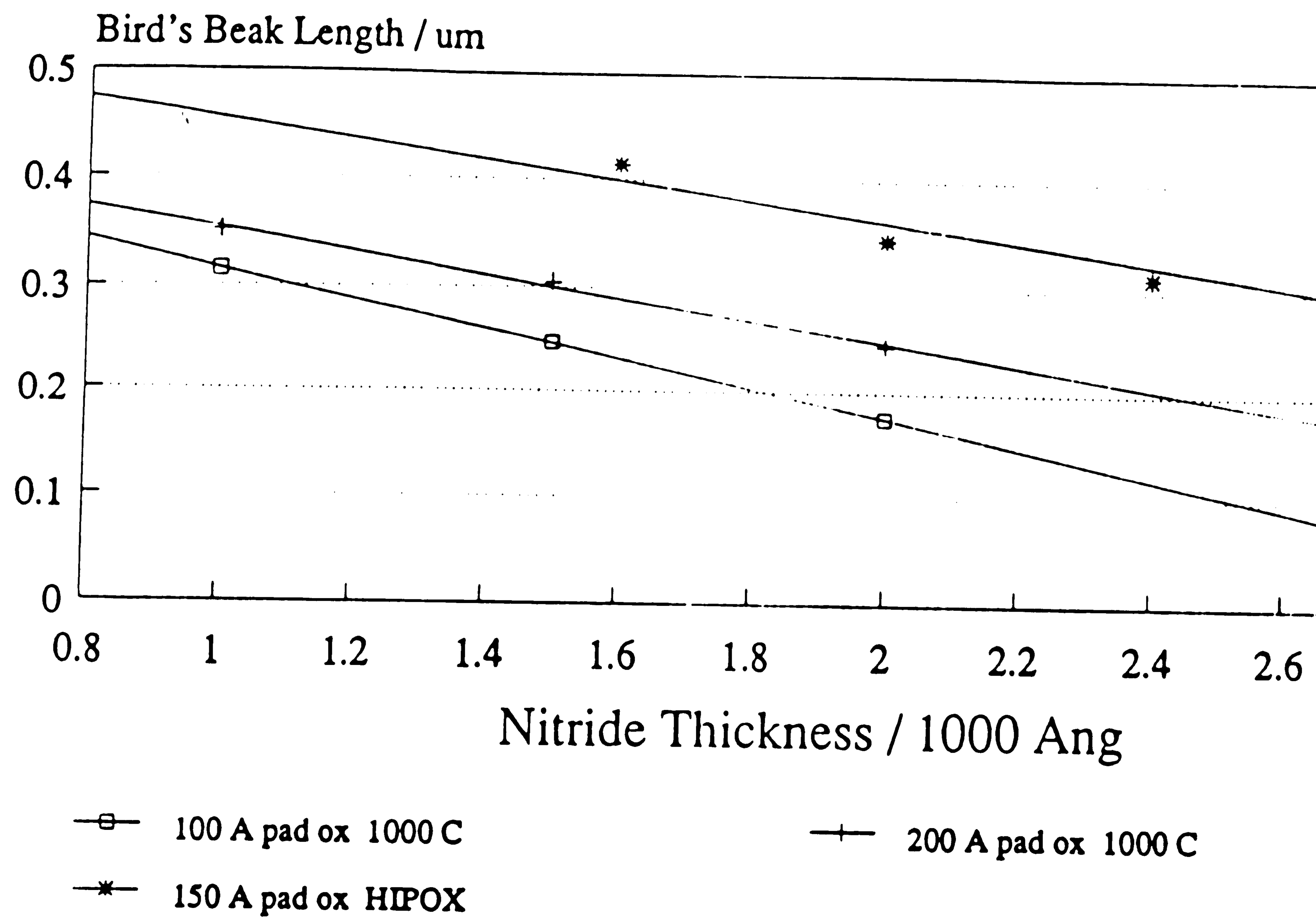
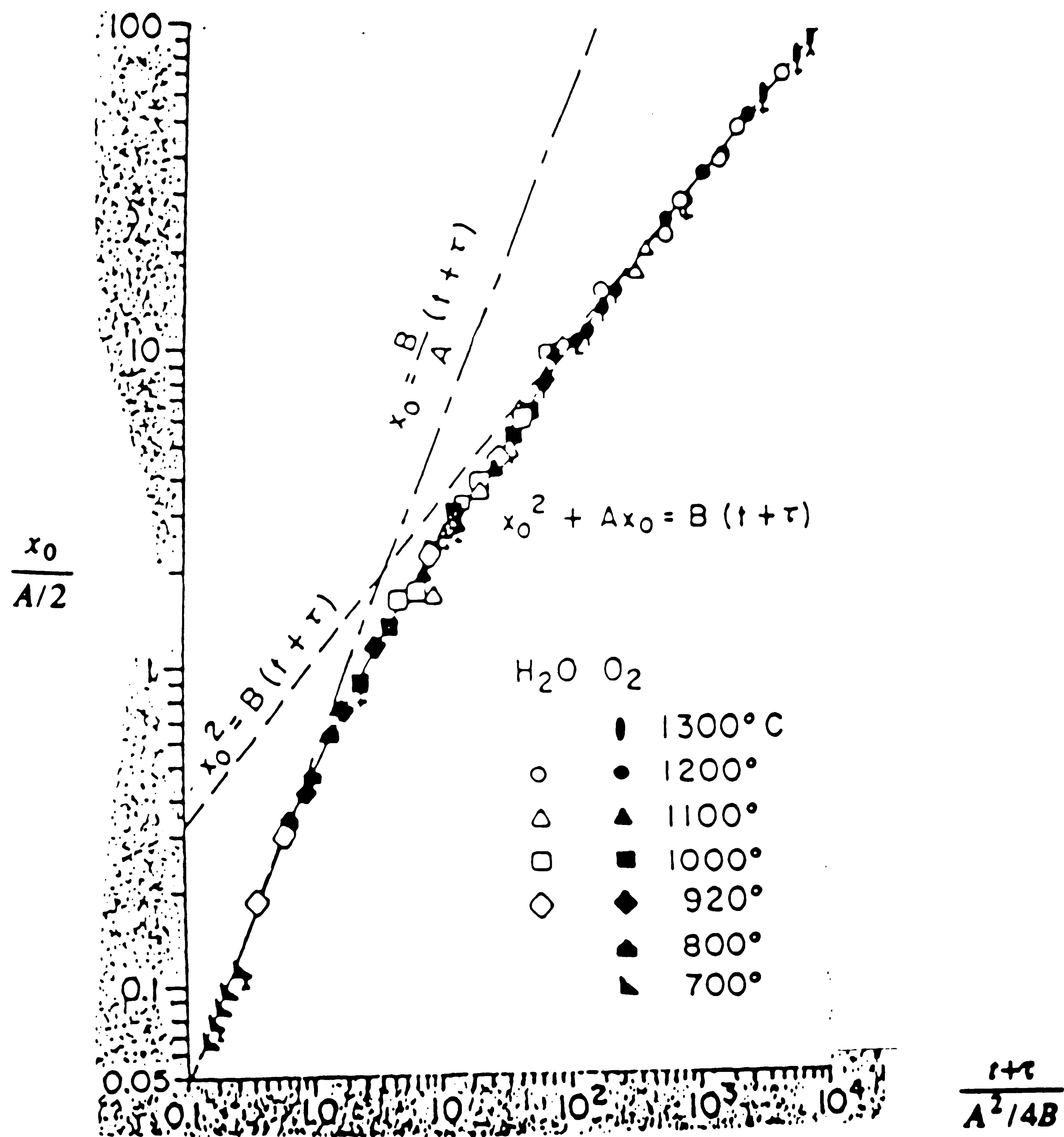


Figure 16. Comparison of Measured Bird's Beak lengths



JAS 8/90

Figure 17. General Relationships for Thermal Oxidation of Silicon



Plotted are the results for various oxidation conditions on the normalized axis of:

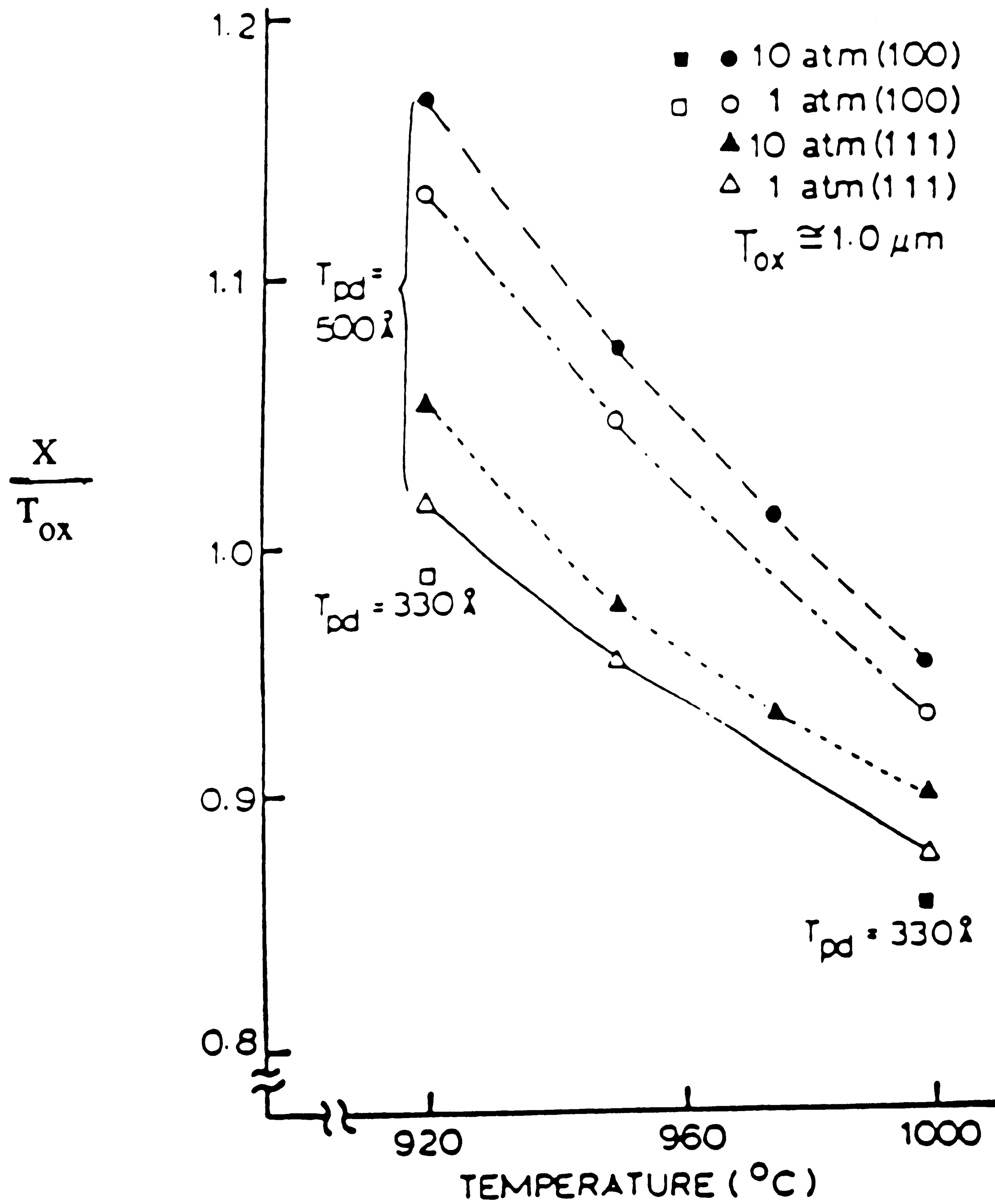
$$\frac{t+\tau}{A^2/4B}$$

vs.

$$\frac{x_0}{A/2}$$

Figure 18. Wu and Stacy's results

Bird's Beak Length vs. Field Oxide Growth Conditions



where X is the measured "bird's beak" length, and T_{ox} is the field oxide thickness.

Figure 19. SEM cross-section Showing Secondary Bird's Beak

Figure 20. Polysilicon/Oxide Residues

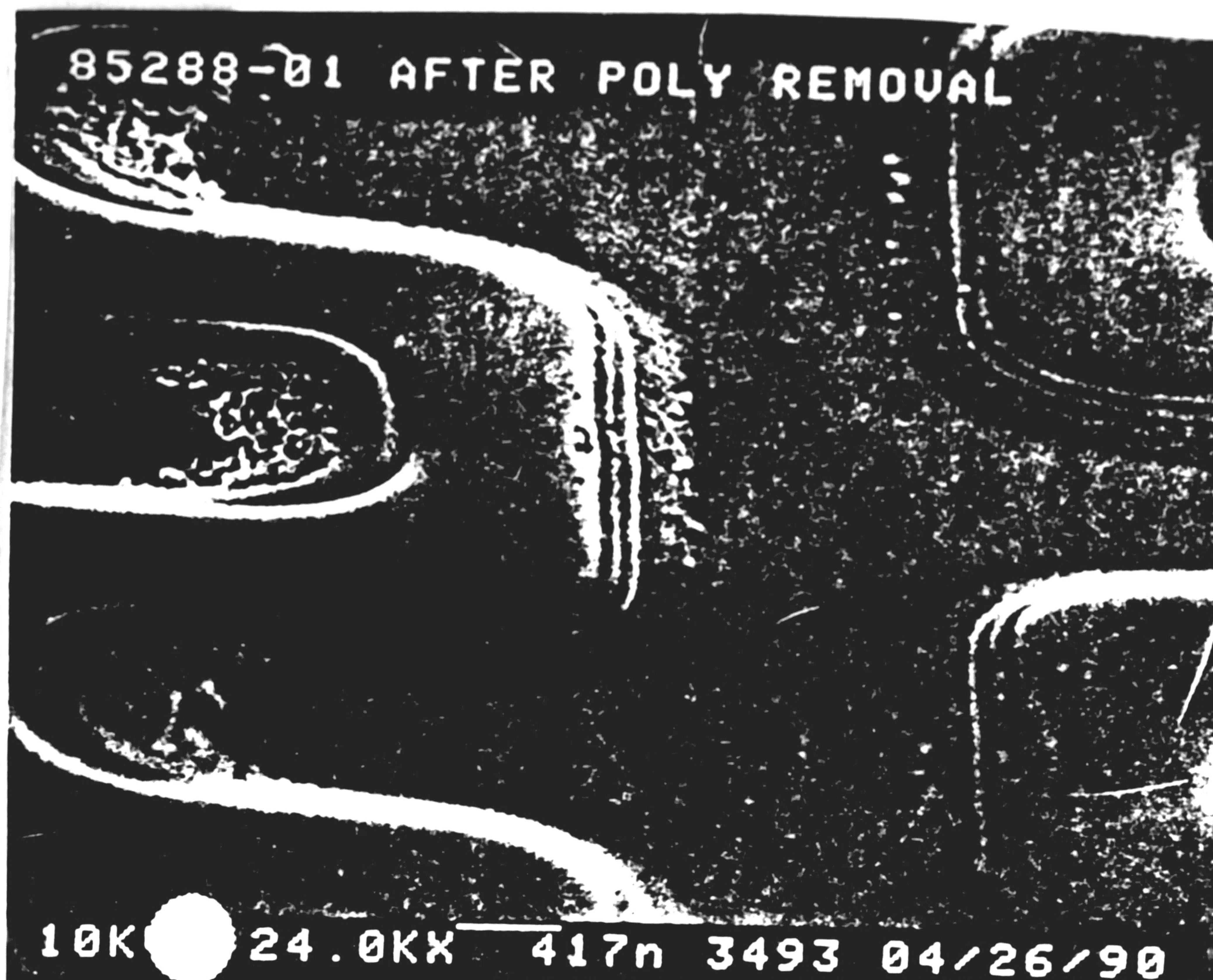


Figure 21. Pitting of Active Areas

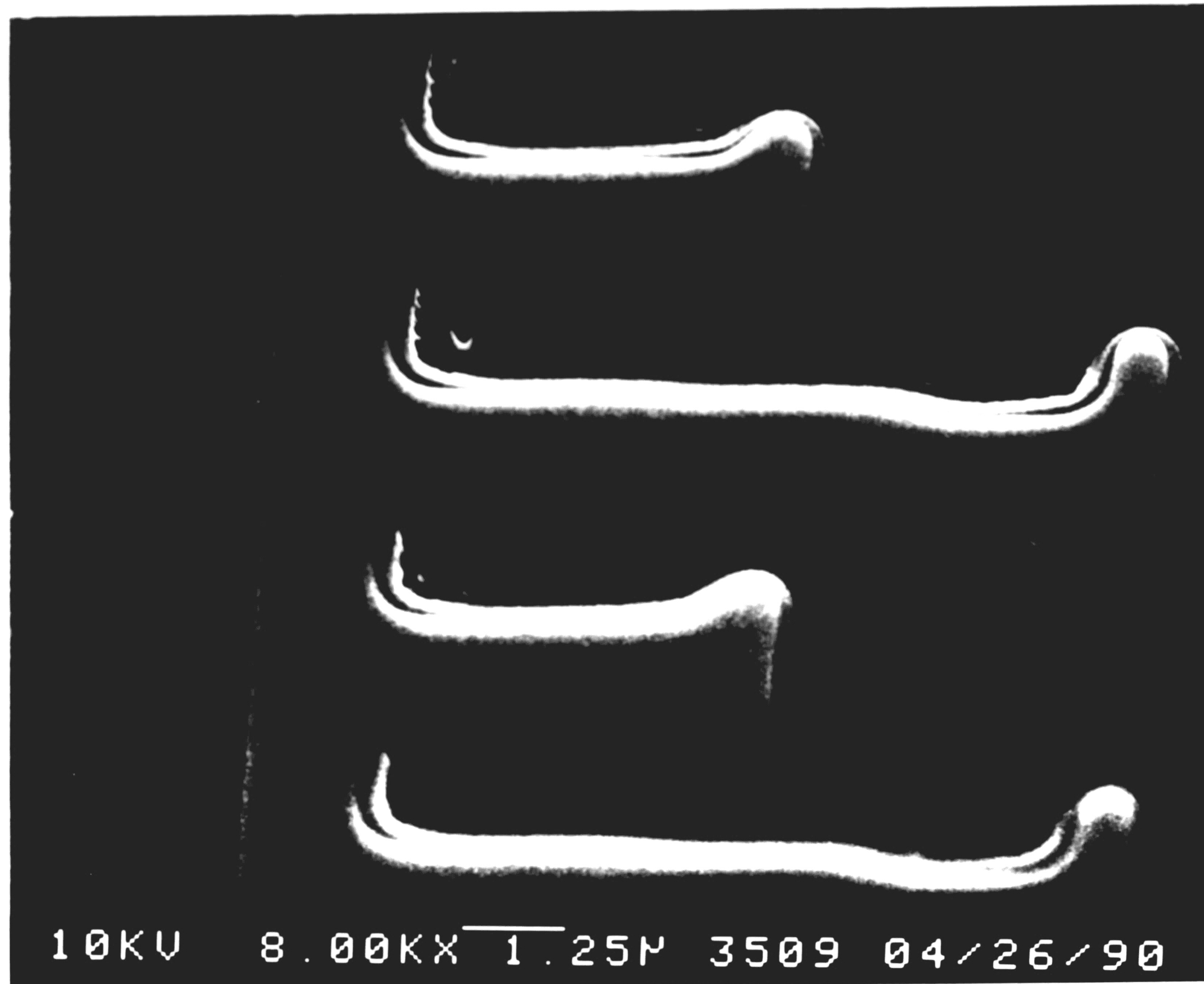


Figure 22

Pitting of Active Device Areas with 1 minute 40 seconds S_6 Plasma Etch"

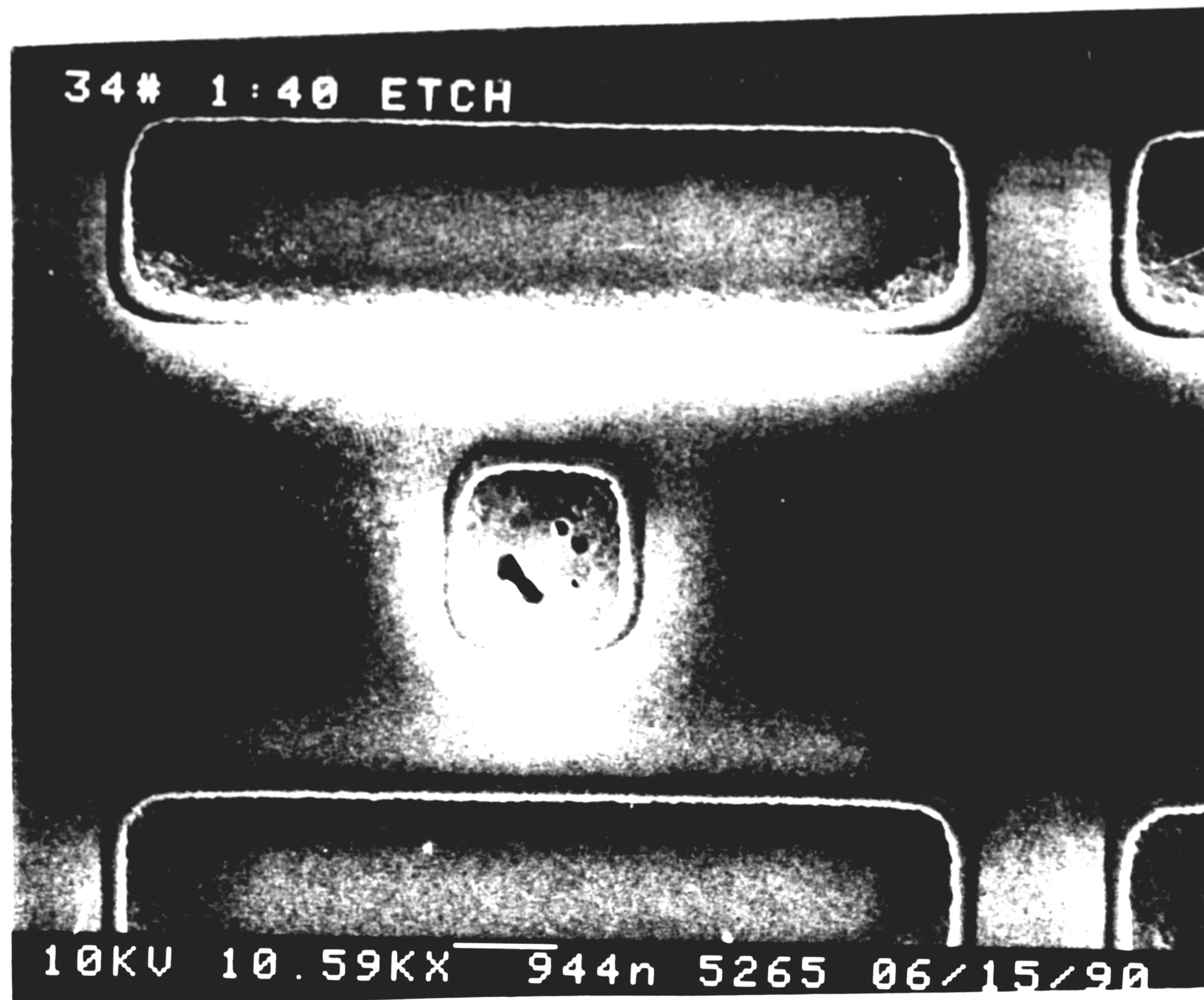


Figure 23. Final Active Device Area cross sectional Profile

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9. Vita

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Jane joined Bell Telephone Laboratories in September 1981, starting as a Senior Technical Associate in the Silicon Processing Technology Laboratory. At AT&T Bell Laboratories, she is presently a Member of the Technical Staff in the VLSI Technology Laboratory, working on the 0.5 μm Technology Development.