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Analog comparator design and testing techniques in a linear array fabricated using a complementary bipolar technology

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ANALOG COMPARATOR DESIGN AND TESTING TECHNIQUES IN A LINEAR ARRAY FABRICATED USING A COMPLEMENTARY BIPOLAR TECHNOLOGY

by

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I dedicate this thesis to my wife Cynthia and son Anthony. Their love, patience, and sacrifice enabled me to concentrate on my work and studies.

I also dedicate this thesis to my parents Anthony and Evdokia Koullias for doing everything necessary so that I have become a useful member of society.

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ABSTRACT

An analog comparator has been designed, fabricated using a complementary bipolar linear array, and tested. On-chip thin film resistors allow the input offset voltage to be trimmed to within less than ±50 μV. The voltage gain is calculated to be 6,400 (76.1 dB). The measured average value of the input bias current is 3.3 μA while the ±3σ value of the input offset current is ±173 nA. Vertical PNP transistors, as opposed to commonly used Zener diodes, perform the level shifting with high speed while allowing the use of a 5-to-10 V power supply. In addition, a modified emitter-coupled pair amplifier design has been used to achieve a 2.1 ns typical propagation delay. The power dissipation is 247 mW with ±5V power supplies.

PREFACE

There is a growing trend of performing the signal processing using digital techniques regardless whether the input signal is of the analog or digital form. The conversion of the analog signals to the digital form has been greatly facilitated by the development of high-performance data converters that are either stand-alone (hybrid or monolithic) or integrated with the rest of the digital processing circuitry. An important and basic block of the data converters is the comparator.

Generally, the resolution and the sampling rate of the converter is strongly dependent on the precision and time response of the comparator(s) employed. Therefore, the ability to convert analog signals to the digital form is contingent upon the ability to realize comparators that combine precision and speed.

This thesis explores the advantages derived from the use of an advanced complementary bipolar process for the design of a high performance comparator.In Chapter 1, a brief description of the comparator function and applications is made and the most important specification parameters are defined. In addition, the performance achieved by some recently introduced comparators is presented.

In Chapter 2, the comparator specifications are derived from a typical A/D converter requirement. Given the overall gain, the optimum number of gain stages is calculated from a simplified amplifier model. In Chapter 3 , the device characteristics of the complementary bipolar process are presented. The comparator transistor-level circuit design is discussed in Chapter 4. The experimental results are presented in Chapter 5 and discussed in Chapter 6.

CHAPTER 1

General Introduction

1.1. Introduction

A comparator compares two analog input signals and provides a digital output that is a function of their difference. Therefore, since it is in effect a 1-bit A/D converter, the comparator is one of the most important elements of the A/D converters. The comparators are also the basic element of pulse-width modulators, peak detectors, delay generators, switch drivers, etc.

A comparator is essentially a fast, high-gain amplifier whose digital output is either "high" or "low", except when switching. When the comparator is in the switching region, the voltage gain is large, and the device is said to be in the linear region. The comparator is designed to be used in an open-loop configuration , and therefore, it does not require frequency compensation.

However, most practical comparators have a small amount of input hysteresis to help keep noise from causing the output to "chatter" [1]. Also, most comparators have a latch input, which makes it possible to freeze the output at a state it has at a given instant of time, in response to a logic signal. Since the comparator is producing a digital decision, its outputs are compatible with either TTL or ECL. Generally, the comparators with ECL compatible outputs have faster response time than those with TTL.

The comparator circuit configuration and the fabrication process used depends on the performance requirements. For very fast response, the comparators are usually designed in advanced all-NPN processes. These circuits use zener diodes for voltage level shifting [2]. Since the device breakdown is low and the zener breakdown is over 5 V, the allowed supply

range is limited. However, comparators have also been designed in processes that include JFET's or vertical PNP transistors [3,4].

The JFET, when used at the input stage, provides high input impedance and level shifting. However, their transconductance is low, and their large mismatch results in large input offset voltage. Comparators that use the vertical PNP's have been reported, but the best propagation delay reported was as high as 20 ns. It is the purpose of this work to investigate circuit techniques with which a total propagation delay of under 3 ns is achieved while the comparator can produce a valid output digital logic level even when the difference between the two input signals is as low as 1.221 mV and as high as 5 V (required precision for a 12-bit system).

1.2. Definition of Comparator Performance Parameters

The precision of a comparator is measured with parameters that are similar to those of an op amp. The voltage gain A_V and the input offset voltage V_{IO} provide a measure of the input voltage window outside of which the digital outputs are at valid digital levels. Thus, no digital information can be obtained when the input voltage has values that fall within this uncertainty window. Note that the voltage gain does not have any meaning for comparators that have built-in hysteresis. Also, the other DC parameters are many times difficult to extract from the transfer function of these comparators.

It is therefore natural to propose a new comparator performance parameter, called input uncertainty window, that is universally applicable to all comparators, with or without hysteresis.In addition, the input referred error voltage, due to the input offset voltage being a function of the source impedance, input common-mode, and power supply variations, could also be added to the uncertainty window. A formal definition of this new comparator parameter would be

> *Input Uncertainty Window (V_U)* is the range of values of the input voltage values within which

the digital information at the output are unspecified.

The units of this can be Volts or, as in A/D converters, fractions of a least significant bit (LSB). For example, an LSB/4 of input uncertainty window would mean that the comparator can effectively compare two signals that have a magnitude difference as small as one LSB/4.

The most important figure of merit that describes the speed performance of a comparator is the input to output propagation delay τ_D. It is the measure of the time that the comparator takes to provide a digital output signal in response to an analog threshold crossing at the input. Depending on the application, the variation of the propagation delay with input over-drive level is desired to be as small as possible. This is because the absolute value of the propagation delay can be calibrated out but it is very difficult to do that for its dispersion.

The definition of the most important comparator performance parameters are listed bellow

Input Offset Voltage (V_{IO})

The differential input DC voltage required to null the output voltage. The ECL output is considered nulled when the differential output voltage is zero.

Input Bias Current (I_B)

The average of the currents flowing into the input terminals when the differential output voltage is nulled.

Input Offset Current (I_{OS})

The difference in the currents flowing into the two input terminals when the differential output voltage is nulled.

Voltage Gain (A_V)

The ratio of the change in differential output voltage to the change in differential input voltage.

Input Resistance (R_{IN})
The ratio of the change in input voltage to the change in input current at either terminal with the other grounded.

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in common-mode voltage to the corresponding change in input offset voltage.

Power Supply Rejection Ratio (PSRR)
The ratio of the change in either supply voltage to the corresponding change in input offset voltage.

Common-Mode Voltage Range (V_{CM})
The range of common-mode voltage at the input for which operation within specifications is guaranteed.

Input Overdrive (V_{OD})
The applied differential input voltage in excess of the comparator input offset voltage.

Input to Output Propagation Delay (τ_D)
The propagation delay measured from the time the differential input signal equals the input offset voltage to the 50% point of the output transition.

Latch Setup Time (τ_S)
The minimum time before the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output.

Latch Hold Time (τ_H)
The minimum time after the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output.

Latch Pulse Width (τ_{PW})

The minimum time that the latch enable signal must be in the compare mode in order to acquire and subsequently hold an input signal change.

Latch Disable Propagation Delay (τ_{LD})

The propagation delay measured between the 50% point of the latch-to-compare transition of the latch enable signal and 50% point of the output transition.

1.3. State of the Art

Table 1.1 lists some examples of high-speed comparators reported and/or are commercially available [5]. Only the stand-alone comparators are listed. The comparators used as part of monolithic A/D converters have less stringent output load drive requirements so that meaningful performance comparison is not valid.

TABLE 1.1

Representative High-Speed Comparators

Manufacturer	Model	τ_D/V_{OD} (ns,max/mV)	V_{IO} (mV,max)	I_B (μA,max)	A_V (V/V)	V_{CM} (V)
Analog Dev.	AD96687	3.5/10	2	10	-	+5/-2.5
Elantec	EL2018	30/5	3	0.3	15,000	+12/-12
Harris	HF-0003	3.4/5 (4.3/1)	5	12	----	+4.8/-2.9
VTC	VC7690	1.8/10	5	20	400	+2.5/-2.5
Honeywell	HCM96870A	2.3/10	3	20	4000	+2.5/-2.5
Plessey	SP93802	1/10	3.5	9	20	+2.6/-2.1
PMI	CMP-08	9.5/5	2.5	13	800	+2.7/-3.0

CHAPTER 2

Block-Level Requirements

2.1. Precision Performance Requirements

2.1.1. Comparator DC Block-Level Model

The DC error sources of the comparator, in a similar fashion to the op amp, can be modeled as simple current and voltage generators. A model that includes DC errors due to the input offset voltage and current, input bias current, input resistance, and voltage gain is shown in Figure 2.1. The model is valid only when the comparator is in the linear region. It is also assumed that the differential output is F100K ECL compatible and there is no built-in hysteresis.

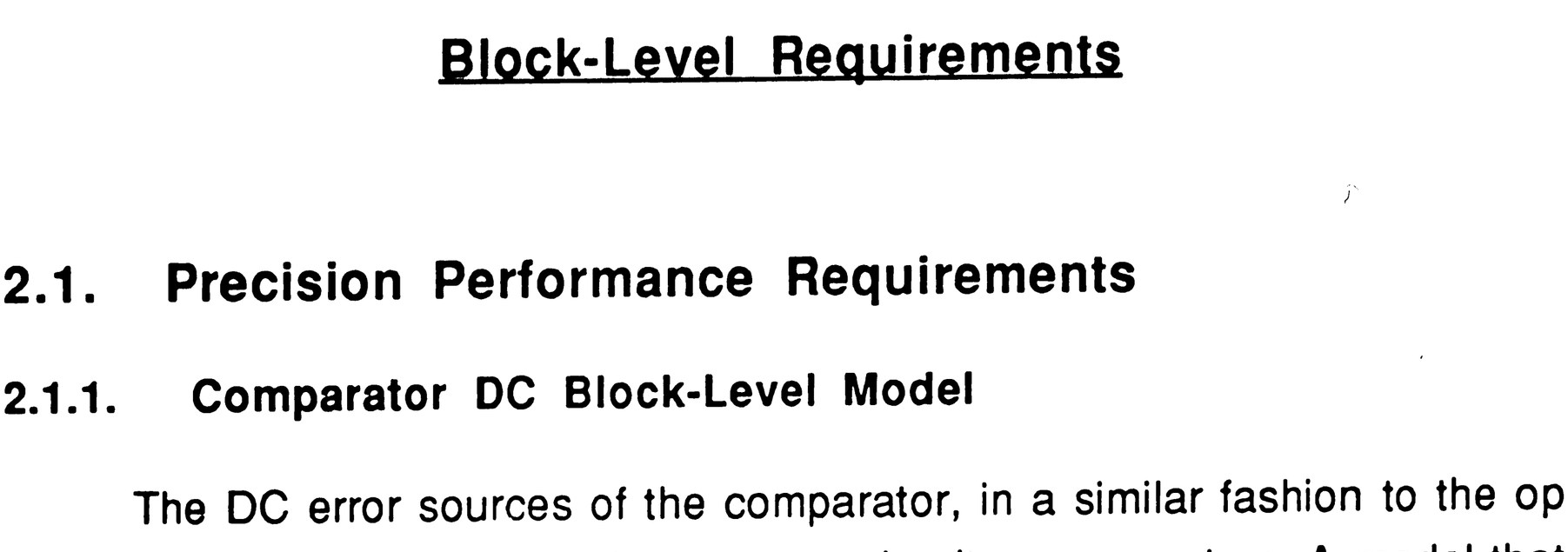


Figure 2.1. Equivalent circuit for the comparator including input offset voltage and current, input bias current, and input resistance.

The range within which the linear model is valid can be deduced by first considering the ideal DC transfer function of the comparator shown in Figures 2.2 and 2.3. The DC level of each output is plotted in (a) while the differential output versus the (differential) input is shown in (b). For a given value of gain A_V, the linear differrential input range is

$$v_{id} = \frac{v_{od}}{A_V} \quad => \quad (V_{IH} - V_{IL}) = \frac{2(V_{OH} - V_{OL})}{A_V} \tag{2.1}$$

Table 2.1 lists the differential input linear voltage range for different values of gain. Assuming zero offset voltage and current, the minimum value of the differential input voltage has to be larger than this input linear voltage range so that the output can produce a valid logic level. Outside this range the gain of the comparator is zero. Therefore, the ideal comparator transfer function is given by

$$H = \begin{cases} 0 & \text{for} \quad |v_{id}| > \dfrac{V_{OH} - V_{OL}}{A_V} \\ A_V & \text{for} \quad |v_{id}| \leq \dfrac{V_{OH} - V_{OL}}{A_V} \end{cases} \tag{2.2}$$

TABLE 2.1

Linear differential input range as a function of gain

A_V (V/V)	$(V_{IH}-V_{IL})/2$ (typ, uV)	$(V_{IH}-V_{IL})/2$ (max, uV)	$(V_{IH}-V_{IL})/2$ (min, uV)
256 (2^8)	2,980	3,633	2,324
512 (2^9)	1,490	1,816	1,162
1,024 (2^{10})	745	908	581
2,048 (2^{11})	373	454	290
4,096 (2^{12})	186	227	145
8,192 (2^{13})	93	113	73
16,384 (2^{14})	47	57	36
32,768 (2^{15})	23	28	18
65,536 (2^{16})	12	14	9
131,072 (2^{17})	6	7	4

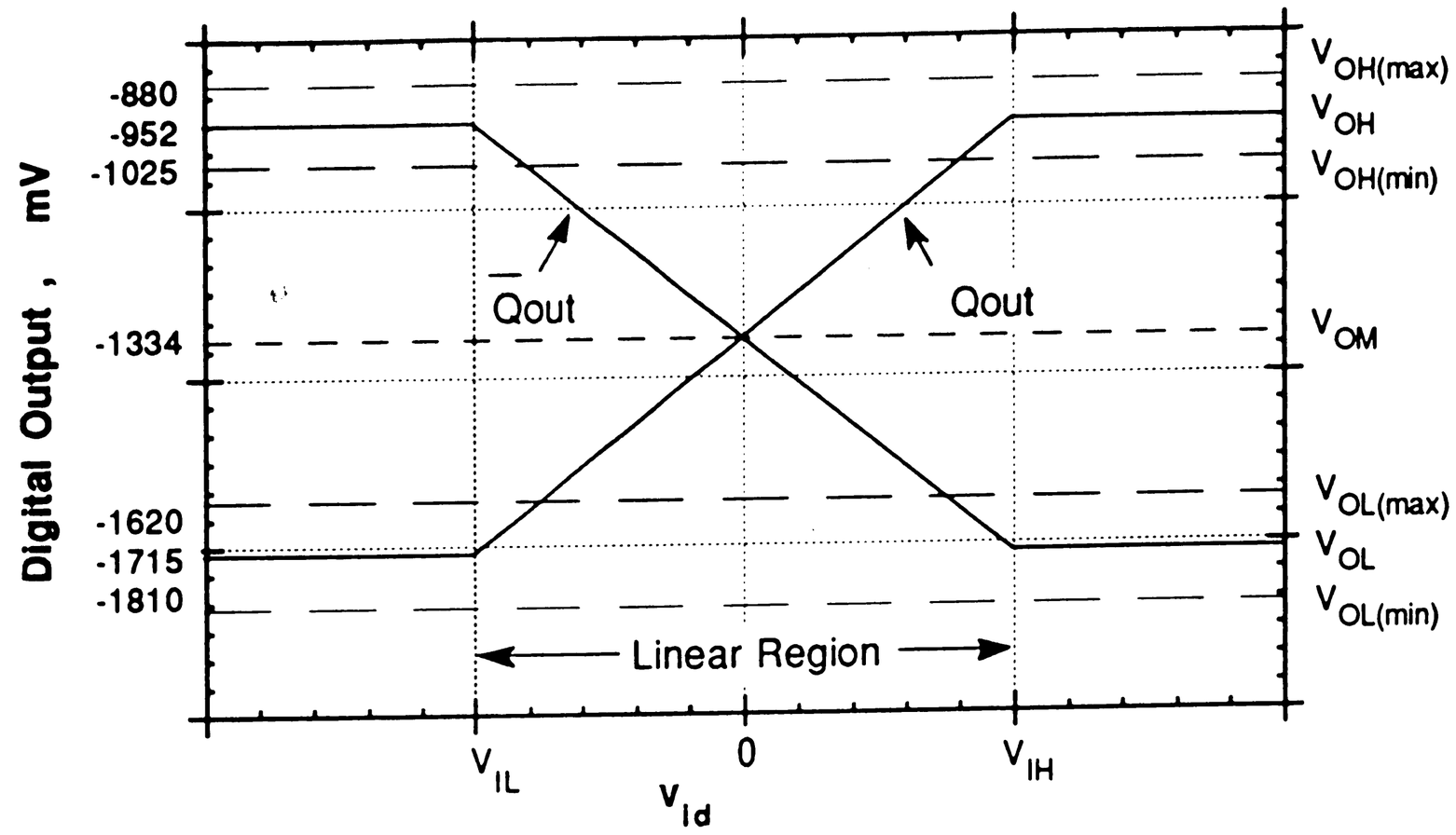


Figure 2.2. Ideal DC transfer characteristics for each of the outputs of an F100K ECL compatible comparator

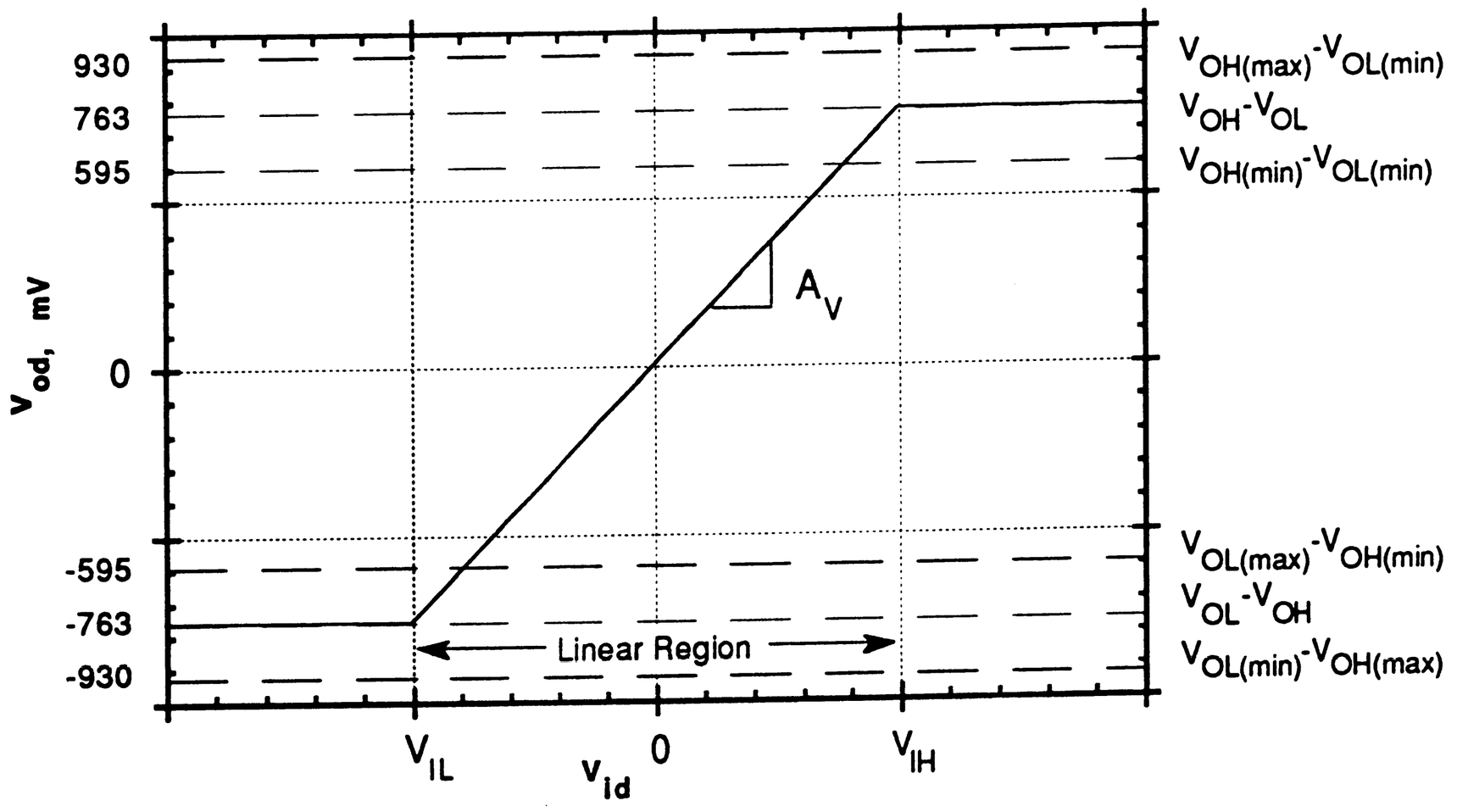


Figure 2.3. Ideal differential-output transfer characteristics of an F100K ECL compatible comparator

2.1.2 DC Error Budget Analysis

The DC error contributions of the input resistance, bias and offset currents become finite when the comparator is driven by finite impedance sources. The error contributions are calculated when the comparator is connected as shown in Figure 2.4 based on the model of Figure 2.1. In the linear range, the output signal is

$$v_{od} = \frac{A_V}{1 + \frac{2R_S}{R_{IN}}} \left[V_S + (V_{IO} - I_B \Delta R_S - I_{OS} R_S)\right] \qquad (2.3)$$

where, $R_S = \frac{R_{SP} + R_{SN}}{2}$, $\Delta R_S = R_{SP} - R_{SN}$

The effect of the input resistance is to decrease the voltage gain. However, the decrease can be neglected since the source impedance is usually much lower than the input resistance. Since the input bias current contributes an offset term that is proportional to the source impedance mismatch, then this term can be nulled by making both impedances equal. The offset current error contribution can only be reduced by decreasing the average value of the input impedances.

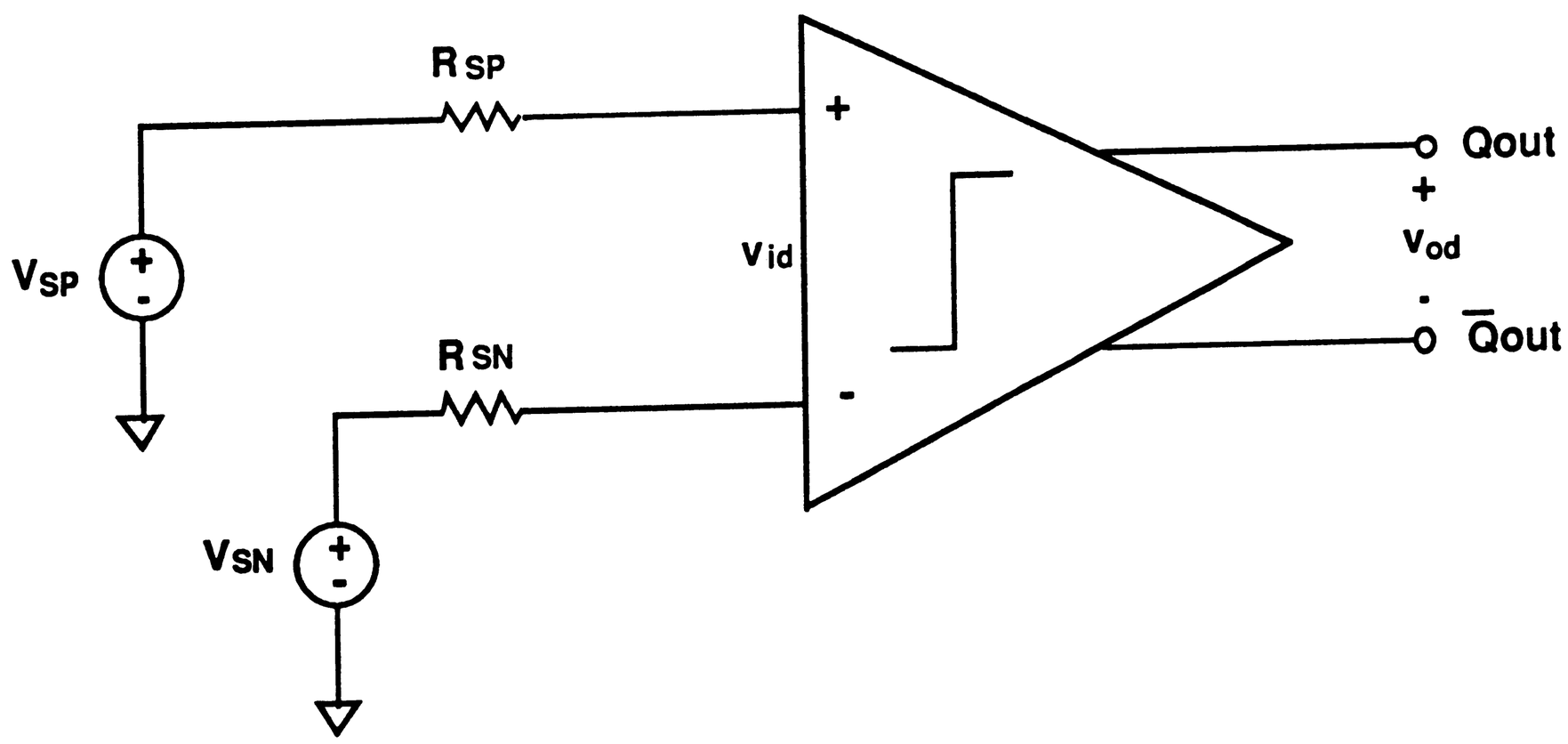


Figure 2.4. Comparator connection used for the error budget calculation

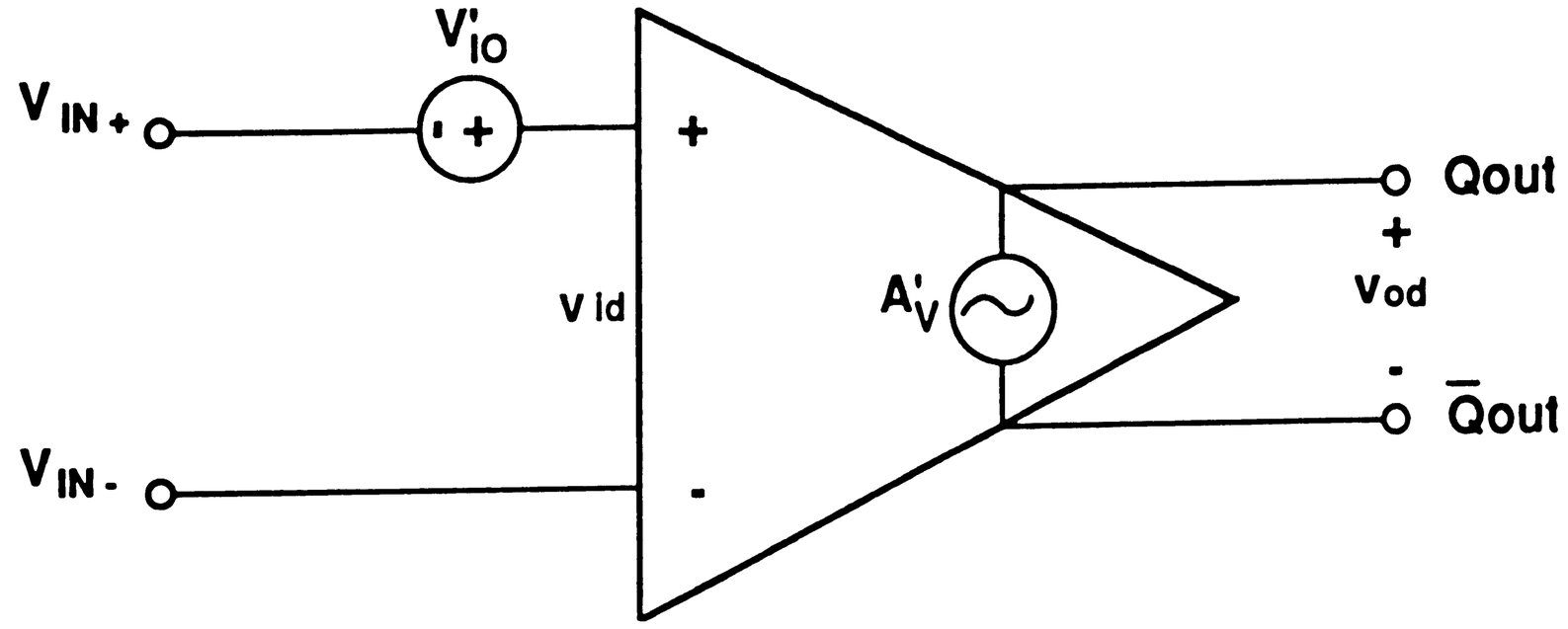


Figure 2.5. Equivalent circuit for the comparator including the source impedance error contributions.

Therefore, as far as the application is concerned, the mismach between the bias currents is more important than their absolute values. This has serious implications for the design of the comparator. It means that the addition of circuitry to reduce the input bias currents is useless since their mismatch can actually get worse. Furthermore, the input shot noise, and input capacitance more than doubles. It is for these reasons that the comparator configuration described in this thesis does not include any input bias current cancellation cicuitry.

Based on equation (2.3), the comparator model of Figure 2.1 can be merged with the circuit of Figure 2.4 to produce a simpler but complete model shown in Figure 2.5. The input offset, input bias and offset currents error contributions are modeled with a single offset voltage source given by

$$V'_{IO} = V_{IO} - I_B \Delta R_S - I_{OS} R_S \tag{2.4}$$

and the gain is modified by the input resistance as

$$A'_V = \frac{A_V}{1 + \frac{2R_S}{R_{IN}}} \quad (\approx A_V) \tag{2.5}$$

Note that the quantities of Equation (2.4) are statistical variables. Therefore, assuming they are statistically independent, the maximum value of V'_{IO} is the root-mean-square sum of the individual maximum errors.

Since,

$$v_{id} = V'_{IO} + (V_{IN+} - V_{IN-}) \tag{2.6}$$

then the complete DC transfer of the comparator that includes the input error sources is given by

$$H = \begin{cases} 0 \quad \text{for } |V_{IN+} - V_{IN-}| > \dfrac{V_{OH} - V_{OL}}{A'_V} + |V'_{IO}| \\ A'_V \quad \text{for } |V_{IN+} - V_{IN-}| \leq \dfrac{V_{OH} - V_{OL}}{A'_V} + |V'_{IO}| \end{cases} \tag{2.7}$$

Note: It is implicitly assumed that the V'_{IO} in equation (2.7) is a random number with a mean value of zero.

According to equation (2.7), the output of the comparator has valid digital levels when the transfer function is zero. The region, within which the gain is A'_V, is also the region where the output has no valid digital information i.e. the input uncertainty window. Therfore from (2.7)

$$V_u = \frac{V_{OH} - V_{OL}}{A'_V} + |V'_{IO}| \tag{2.8}$$

which is the mathematical definition of the input uncertainty window. Note that equation (2.8) actually gives half the window value. It is assumed that the portion of the window with negative values is the same with with the one for positive values. It is like saying that the input offset voltage is 2 mV; what we really mean is that the offset voltage can take values anywhere between -2 mV and +2mV.

2.1.3. Calculation of the Input Uncertainty Window

The uncertainty window can be calculated from the comparator application requirements. For an A/D converter, the LSB is found from the number of bits and the nominal full-scale range according to

$$1\ \text{LSB} = \frac{V_{FS}}{2^N} \tag{2.9}$$

where, N is the number of bit precision required. Table 2.2 lists the LSB size for certain bit precision and nominal full-scale range.

TABLE 2.2

LSB size versus bit precision and nominal full-scale range

	1 LSB, mV				
Bit Precision	VFS=2 V	VFS=4 V	VFS=5 V	VFS=7 V	VFS=10 V
8	7.813	15.625	19.531	27.344	39.063
9	3.906	7.813	9.766	13.672	19.531
10	1.953	3.906	4.883	6.836	9.766
11	0.977	1.953	2.441	3.418	4.883
12	0.488	0.977	1.221	1.709	2.441
13	0.244	0.488	0.610	0.854	1.221
14	0.122	0.244	0.305	0.427	0.610
15	0.061	0.122	0.153	0.214	0.305
16	0.030	0.061	0.076	0.107	0.153
17	0.015	0.030	0.038	0.053	0.076

The total error contributed by the comparator is usually equivalent to one fourth or one fifth of the 1 LSB size. This error is equivalent to the total length of the comparator uncertainty window or twice the value as given by (2.8). Let's define the fraction of the LSB error contributed by the comparator as

$$\text{comparator error as a fraction of 1 LSB} = \frac{\text{total uncertainty window width}}{\text{1 LSB size}}$$

or

$$f_\varepsilon = \frac{1}{2^\varepsilon} = \frac{2V_u}{1\ LSB} \tag{2.10}$$

Combining (2.9) with (2.10)

$$V_u = \frac{1}{2}LSB\, f_\varepsilon = \frac{V_{FS}}{2^{(N+1)+\varepsilon}} = \frac{V_{FS}}{2^{Nc+1}} \tag{2.11}$$

The quantity Nc is the bit accuracy of the comparator. Note that ε does not have to be a whole number. Equations (2.8) and (2.11) can be used for the design or the analysis of a comparator. When designing, the value of V_u is found from the system requirements by using (2.11); afterwards the value of A_V' and V_{IO}' are found so that (2.8) is satisfied.

When the comparator performance is given, one can work backwards to calculate the total error contributed by the comparator. As a point of reference, the required values of A_V' are plotted in Figure 2.6 as a function of V_{IO}' for a given level of comparator bit accuracy. A 5 V nominal full-scale range is assumed.

The value of A_V' is constant when the uncertainty window is much less than the value of V_{IO}'. When V_u becomes comparable with V_{IO}' then the gain increases rapidly to keep the width of the uncerainty window constant. Perhaps, the gain exponential increase is best illustrated by re-arranging Equation (2.8) for A_V'

$$A_V' = \frac{V_{OH} - V_{OL}}{V_u - |V_{IO}'|} = \frac{V_{OH} - V_{OL}}{\frac{V_{FS}}{2^{Nc+1}} - |V_{IO}'|} \tag{2.12}$$

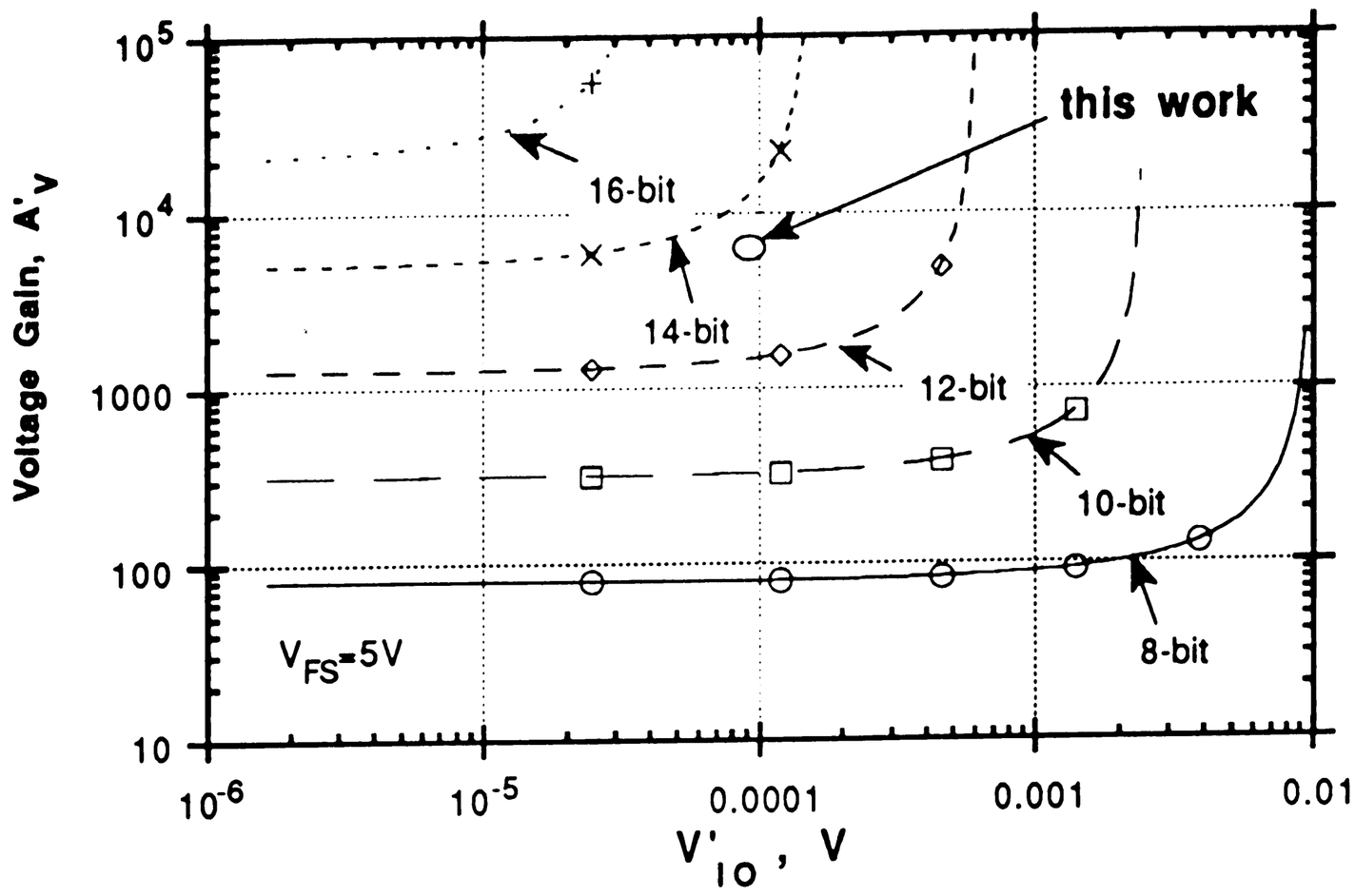


Figure 2.6. A'_V vs V'_{IO} for different compararator precision levels Nc.

Note that the required gain is decreased by increasing full-scale range value. Also, the required gain is fairly reasonable even for fairly high comparator precision levels assuming the V'_{IO} contributors are kept low compared with the uncertainty window. For example, a 12-bit A/D converter will probably require a 15-bit comparator precision. Assuming the V'_{IO} is under 100 μV, then the required gain will be about 3,719. For a 5 V full-scale range and the same offset, the required gain will be 14,506; a factor of almost four increase. Since high gain means slow frequency response, particular care should be taken to decrease V'_{IO}.

2.2 Optimization of the Time-Domain Response

The DC block characteristics of the comparator were determined from the analysis in section 2.1. Now this question arises; for a given DC precision, what is the optimum type and number of sub-blocks such that the time domain response is optimized? To be more specific one may ask; how many gain stages and what is the gain of each stage such that, for a given overall voltage gain, the input-to-output propagation delay is minimized?

In addition to the required DC precision, an additional variable, that may be imposed to constrain the answer to this question, is maximum allowed power dissipation. Naturally, the ultimate speed that can be achieved is with no such constraint; however in realistic circuits power dissipation is a very important parameter and should not be iqnored. Most of the block optimization analysis reported in the literature includes no power constraint; therefore, the following discussion includes the derivation of the optimum number of stages with or without power constraints [6,7].

2.2.1 Simplified Linear AC Model

Let's assume that the comparator consists of an amplifier chain with an n-number of identical non-interacting stages as shown in Figure 2.7. The reason for identical stages is that it has been shown that the minimumm over-all rise time for a given gain is achieved by making all stages the same. This rule is not as important for propagation delay but it does make the analysis and design simpler. The amplifier stages are non-interacting when their input impedance is infinite and their output impedance is zero; a reasonable approximation for this level of analysis.

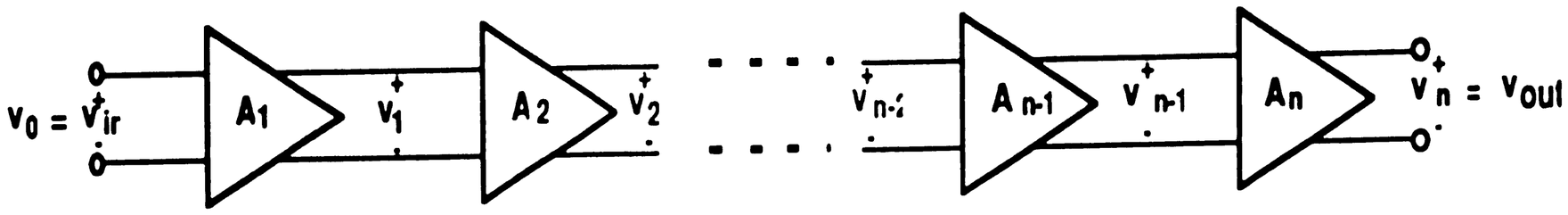


Figure 2.7. Sub-block AC model of the comparator.

Another assumption is that the each amplifier stage is linear. This is due to the fact that the propagation delay is usually worse for small values of input overdrive at which usually only the last stage is in the non-linear region. The total gain A_V is given by the product of the individual gains; thus the required gain of each amplifier A_i is found from

$$A_V = A_1 \cdot A_2 \cdot A_3 \ldots\ldots A_i^n \quad \Rightarrow \quad A_i \ldots = \ldots A_V^{1/n} \tag{2.13}$$

Also, each individual gain can be written in the form of a product of a transconductance Gmi that is proportional to the amplifier power supply current Ii (1/VK is the proportionality constant), and a resistance Ri as shown below

$$A_{Vi} = Gm_i R_i = \frac{I_i}{V_K} R_i \tag{2.14}$$

As a first order approximation, let's assume that the frequency response of each individual amplifier is determined by a single dominant pole or, in otherwords, a single time constant τ_{Di} which is proportional to the resistance Ri and some lumped capacitance Ci. as shown below

$$\tau_{Di} = R_i C_i \tag{2.15}$$

This form is justified because Ri, as shown in Equation (2.14), determines the amplifier gain and, therefore is usually the largest impedance on the signal path. Combining Equations (2.14) and (2.15) we derive the relationship between the time constant τ_{Di}, the supply current Ii, and the stage gain to be

$$\tau_{Di} = \frac{Gm_i}{Gm_i} R_i C_i = \frac{A_{Vi}}{Gm_i} C_i \quad \Rightarrow$$

$$\tau_{Di} = \frac{A_{Vi}}{I_i} C_i V_K \tag{2.16}$$

Note that the total supply current Icc of the comparator is approximatelly

$$I_{CC} = n I_i \quad \Rightarrow \quad I_i = \frac{I_{CC}}{n} \tag{2.17}$$

Therefore, Equation (2.16), when combined with (2.13) and (2.17) can be written as

$$\tau_{Di} = \frac{A_V^{1/n}}{I_i} C_i V_K = \tau_{io} A_V^{1/n} \tag{2.18.a}$$

or

$$\tau_{Di} = \frac{n A_V^{1/n}}{I_{CC}} C_i V_K = \tau_{no} n A_V^{1/n} \tag{2.18.b}$$

where,

$$\tau_{io} = \frac{C_i V_K}{I_i} = n \tau_{no} \tag{2.18.c}$$

and

$$\tau_{no} = \frac{C_i V_K}{I_{CC}} \tag{2.18.d}$$

are proportionality constants indendent of the number of stages n. The choise of which equation to use depend on whether there is (use (2.18.b)) or there is not (use (2.28.a)) a power supply current constraint.

2.2.2 Time Response of n-Cascaded Gain Stages

The Laplace transfer function [8] of n-cascaded identical linear gain stages that are characterized by a dominant pole pi=$1/\tau_{Di}$ is

$$A_V(s) = \frac{Vn(s)}{V_{IN}(s)} = \frac{A_{Vi}^n}{(1 + s\tau_{Di})^n} \tag{2.19}$$

Both the time and the frequency response of the sytem can be derived from (2.19). We consider first the time response to a unity step input. Vin(s)=1/s. Then (2.19) becomes

$$\frac{vn(s)}{A_{Vo}} = \frac{1}{s\,(1 + s\tau_{Di})^n} \tag{2.20}$$

By taking the inverse Laplace transform of (2.20) the time response at the output of the n_{th} amplifier due to a unity step input is found to be

$$\frac{vn(t)}{A_{Vo}} = 1 - e^{-t/\tau_{Di}} \sum_{r=0}^{r=n-1} \frac{(t/\tau_{Di},)^r}{r!} \tag{2.21}$$

The time delay of the whole system tDn can be found by setting the second term of (2.21) to 0.5 and solving for the normalized time

$$\frac{\tau_{Dn}}{\tau_{Di}} = \frac{t\,(\frac{v_n(t)}{A_V} = 0.5)}{\tau_{Di}} \tag{2.22}$$

Unfortunately an analytical solution is not possible so a numerical solution is performed for systems that have up to ten identical stages. The solution is tabulated on Table 2.3.. Also shown is the delay normalized to the number of stages.

TABLE 2.3

Time Delay Through n-Gain Stages

n	τ_{Dn}/τ_{Di}	$(\tau_{Dn}/\tau_{Di})/n$
1	0.693	0.693
2	1.678	0.839
3	2.674	0.891
4	3.672	0.918
5	4.670	0.934
6	5.670	0.945
7	6.670	0.953
8	7.669	0.959
9	8.669	0.963
10	9.668	0.967

Examining the results of Table 2.3 one can approximate the total propagation delay through n-stages as the sum of all the individual time constants

$$\tau_{Dn} \approx n\,\tau_{Di} \tag{2.23}$$

This approximation is quite good for larger number of gain stages. For example, the total error is 3% for ten gain stages and 8% for four. The maximum error is 31% for one gain stage. A better approximation seems to be

$$\tau_{Dn} \approx (n - 0.31)\,\tau_{Di} \tag{2.24}$$

In this case the errors for ten, four, and one gain stages are 0.2%, 0.5%, and 0.4% respectively. Equation (2.24) can be used to obtain almost exact solutions. However, the Equation (2.23) gives a better intuitive understanding, an accurate enough solution for multiple gain stages, and is mathematically more tractable.

2.2.3 Frequency Response of n-Cascaded Gain Stages

The most important frequency response parameter of n-cascaded gain stages is the -3 dB bandwidth which can be found by substituting $s=j\,\omega$ in Equation (2.19) and finding the frequency at which the magnitude of the overall gain decreases by a factor of 0.707. Therefore (2.19) can be written as

$$A_V(j\omega) = = \frac{A_{Vi}^n}{(1 + j\omega\tau_{Di})^n} \quad =>$$

$$A_V(j\omega) = = \frac{A_{Vi}^n\,(1 - j\omega\tau_{Di})^n}{[1 + (\omega\tau_{Di})^2]^n} \tag{2.25}$$

And its magnitude is

$$|A_V(j\omega)| = = \frac{A_{Vi}^n}{[1 + (\omega\tau_{Di})^2]^{n/2}} \tag{2.26}$$

Therefore, the -3 dB bandwidth is found by equating the denominator of (2.26) to the square root of two and solving for the frequency [9,10]

$$[1 + (\omega\tau_{Di})^2]^{n/2} = \sqrt{2} \quad =>$$

$$\omega_{-3dB} = \frac{\sqrt{2^{\,1/n} - 1}}{\tau_{Di}} \tag{2.27}$$

Figure 2.8 shows graphically the variation of the normalized bandwidth as a function of the number of gain stages.

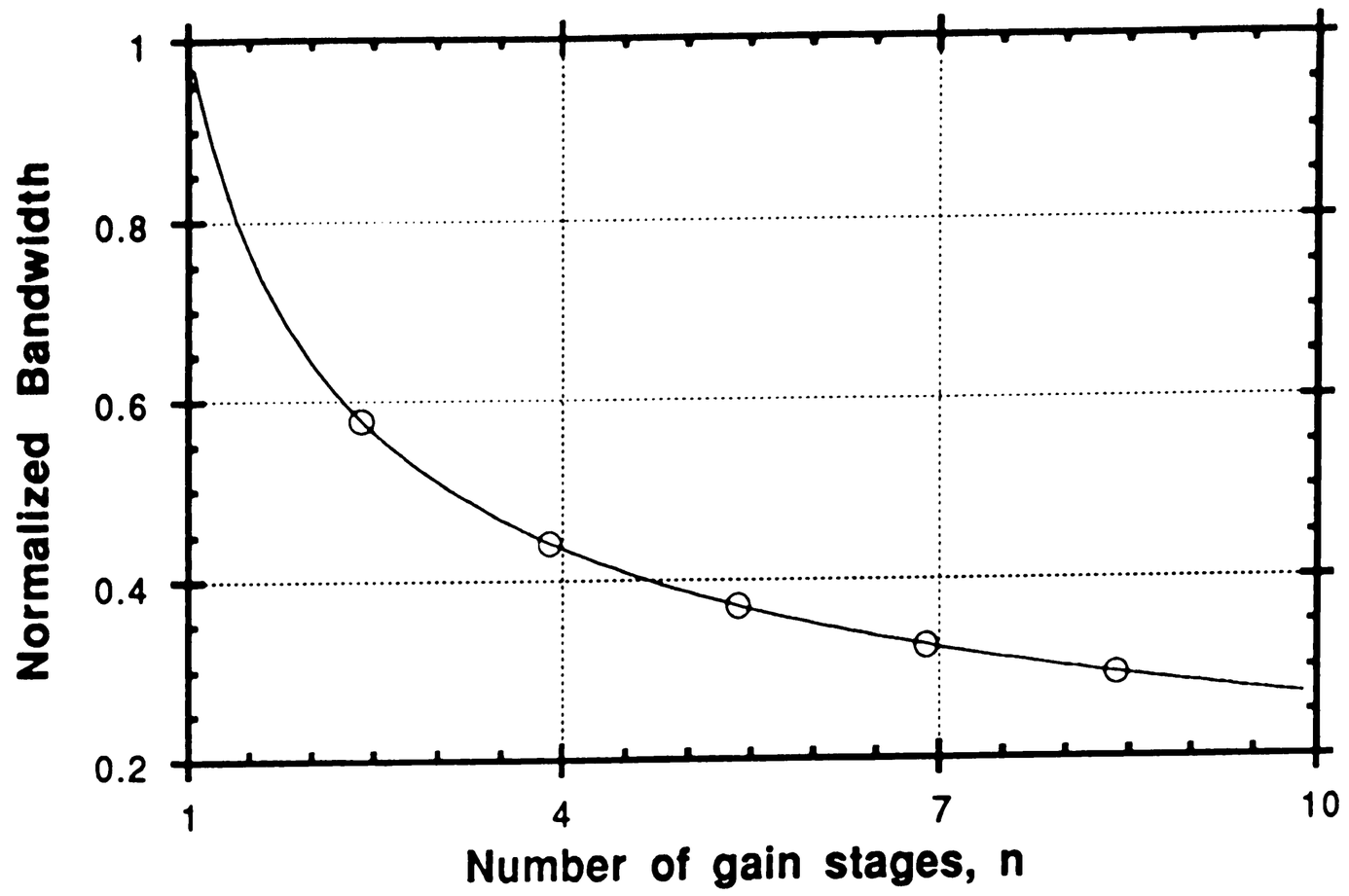


Figure 2.8. Normalized bandwidth of an n-stage cascaded amplifier

2.2.4 Optimum Number of Stages for Minimum Propagation Delay

In sections 2.2.1 and 2.2.2 we have derived a model for the propagation delay of one gain stage and, knowing this, of an n-number of identical stages. We are in the position now to answer the question put earlier as to what is the optimum number of gain stages so that the propagation delay through the comparator can be minimized. For this purpose we use Equations (2.18) and (2.23) to derive the overall analytical expression for the propagation delay. With no power supply limitations the propagation delay is

$$\tau_{Dn} \approx n\,\tau_{Di} = n\,A_V^{1/n}\,\tau_{io} \qquad (2.28.a)$$

When there is a maximum power supply specification, the propagation delay expression is of the form

$$\tau_{Dn} \approx n\,\tau_{Di} = n^2\,A_V^{1/n}\,\tau_{no} \qquad (2.28.b)$$

Equations (2.28.a) and (2.28.b) are plotted in figures 2.9 and 2.10 respectivelly as a function of the number of stages n for different values of DC gain. Note that in both graphs the propagation delay decreases to a minimum value and increases for very small or very large number of gain stages. The main differnce between the two graphs is that the minimum propagation delay value occurs for a smaller number of n when the supply current is fixed, and that minimum is more defined.

The number of stages at which the minimum propagation delay occurs is found by differentiating (2.28) with respect to n , setting the differential equal to zero, and then solving fon n as a function the gain Avo. Differentiating (2.28.a) we find

$$\frac{d\tau_{Dn}}{dn} = \tau_{io}\left(A_V^{1/n} - \frac{n\, A_V^{1/n} \ln (A_V)}{n^2} \right) \quad \Rightarrow$$

$$\frac{d\tau_{Dn}}{dn} = \tau_{io}\, A_V^{1/n}\left(1 - \frac{\ln (A_V)}{n} \right) \tag{2.29}$$

Setting (2.29) equal to zero and solving for the optimum value of n we find

$$n_{opt} = \ln A_V \tag{2.30}$$

The above equation is simple enough so that only the overall gain is needed to decide how many gain stages are required for minimum propagation delay.. Since the numver of stages and the overall gain is known we can also derive the gain of each stage to achieve minimum propagation delay. From (2.13) and (2.30) we solve for A_i to find

$$A_{i,opt} = A_V^{1/n_{opt}} = A_V^{1/\ln(A_V)} \quad \Rightarrow$$

$$\ln(A_{i,opt}) = \frac{\ln A_V}{\ln A_V} = 1 \quad \Rightarrow$$

$$A_{i,opt} = e^1 = 2.718 \tag{2.31}$$

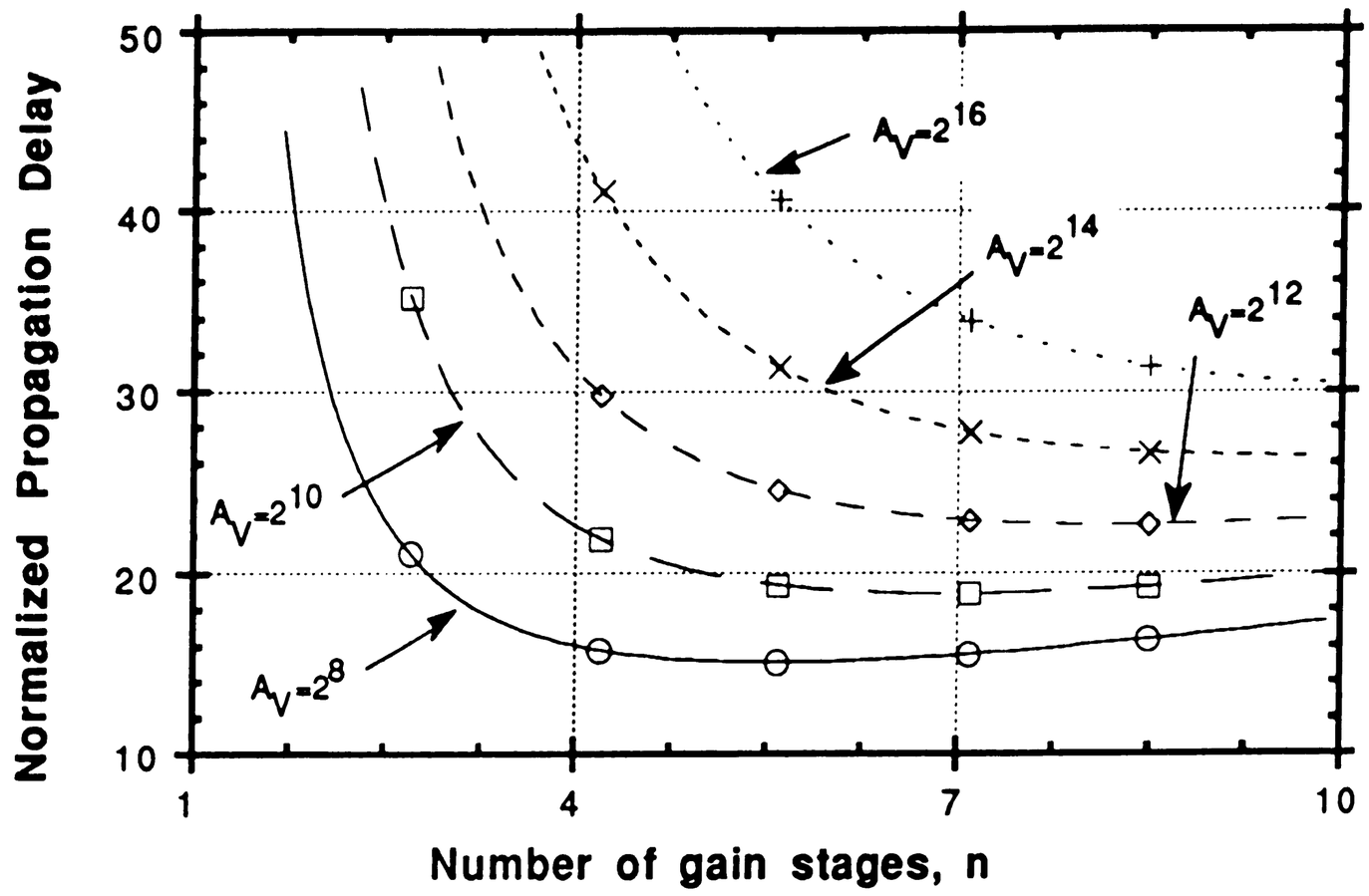


Figure 2.9. Propagation delay vs number of stages with no power supply current limitations.

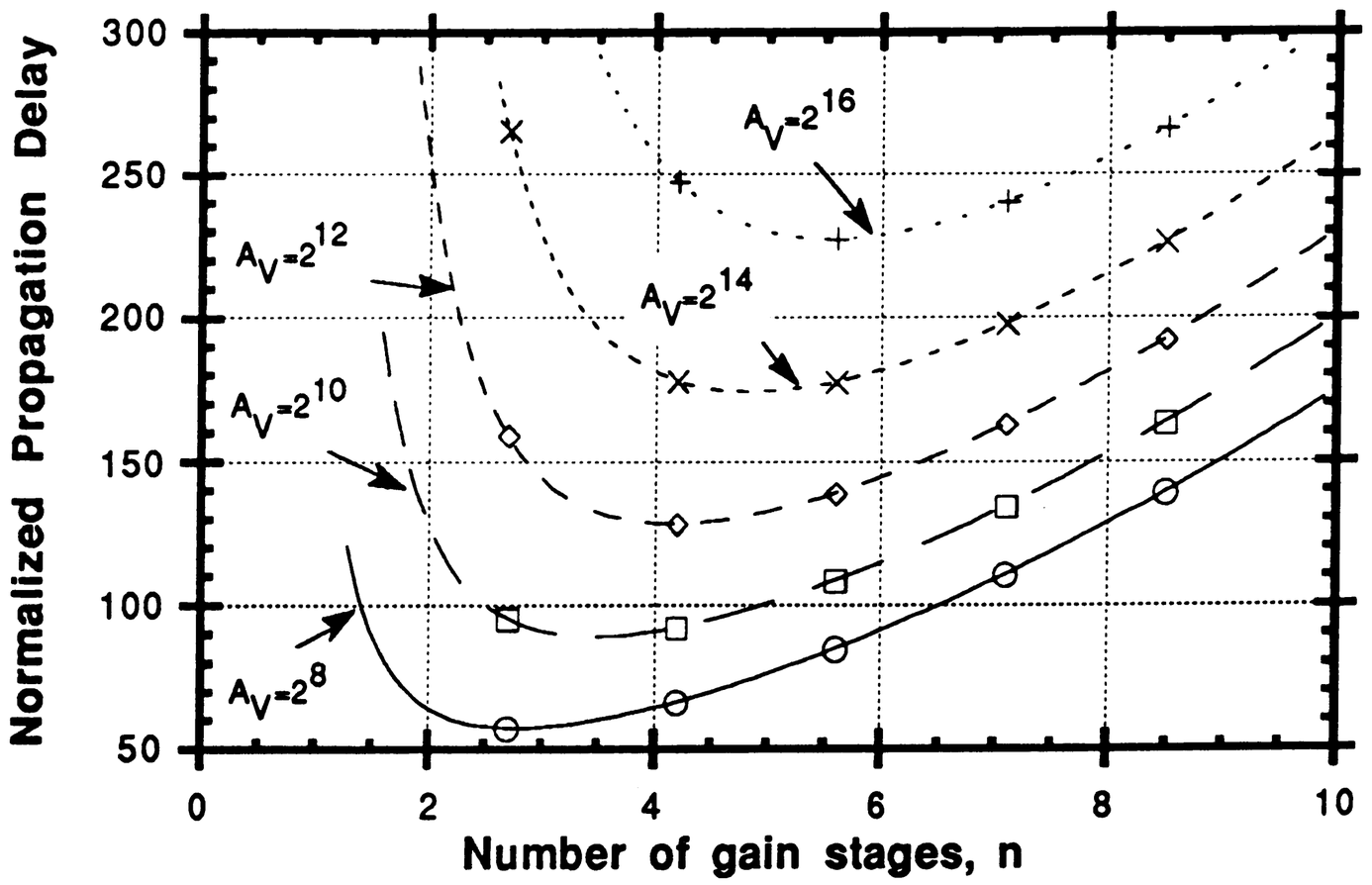


Figure 2.10. Propagation delay vs number of stages for a fixed gain and maximumsupply current.

Again a pleasant suprise; the optimum gain of each stage is a fixed number independent of any other quantity. This is important since, in principle, one need not know the final gain specification to start designing each individual gain stage. This approach can be useful in standard cell design when the final application is unknown. For analysis purposes, the minimum value of the propagation delay can also be found to be

$$\tau_{Dn,opt} = e^1 \tau_{io} \ln(A_V) \tag{2.32}$$

Therefore, the optimum propagation delay varies logarithmically with the overall gain of the comparator.

As mentioned before the more practical case is that which the power supply current is fixed to a maximum allowable value. Following the same method the diffrerential of equation (2.28.b) with respect to n is found to be

$$\frac{d\tau_{Dn}}{dn} = \tau_{no}\left(2n\, A_V^{1/n} - \frac{n^2\, A_V^{1/n} \ln (A_V)}{n^2} \right) \quad \Rightarrow$$

$$\frac{d\tau_{Dn}}{dn} = \tau_{no}\, A_V^{1/n} \left(2n - \ln (A_V) \right) \tag{2.33}$$

Setting the differential equal to zero and solving for n we find

$$n_{opt} = \frac{\ln A_V}{2} \tag{2.34}$$

Equation (2.34), graphed on Figure 2.10, shows that the optimum number of gain stages for fixed power supply current is half the number required when there are no restrictions as shown by equation (2.30). Similarly the optimum gain for this case is

$$A_{i,opt} = A_V^{1/n_{opt}} = A_V^{2/\ln(A_V)} \quad \Rightarrow$$

$$\ln(A_{i,opt}) = \frac{2 \ln A_V}{\ln A_V} = 2 \quad \Rightarrow$$

$$A_{i,opt} = e^2 = 7.389 \tag{2.35}$$

which equals to the square of the previous case (equation (2.31)). Also, the minimum value of the propagation delay is found to be

$$\tau_{Dn,opt} = \frac{e^2}{2} \tau_{io} \ln(A_V) \tag{2.36}$$

The formulas developed in this chapter so far are adequate for the block level design of the comparator based on the system application requirements. These formulas were derived based on a simple model of the comparator. Next, some refinements of the model are made to help increase the accuracy of the block level design.

The first assumption made was that the the propagation delay of a single stage is proportional to a time constant that decreases with power dissipation and increases with gain (equation (2.16). In reality, there are two more time constants that should be considered [11]. One, τ_O, is a constant and is only a function of the particular technology used. An example of such a time constant is the base transit time of a transistor that depends only on the width of the base and the minority carrier diffusivity.

The other time constant increases linearly with supply current and, if there is a limit on the power supply current, is inversely proportional to the number of gain stages comprising the comparator. This type of time constant is usually associated with the time needed to build up the minority carrier charge in the base of a transistor. The sum of all three time constants is the propagation delay through a single gain stage. For identical gain stages, the propagation delay through the whole comparator is

$$\tau_{Dn} = n\left(\tau_o + \frac{\tau_p}{n} + n\, A_V^{1/n}\tau_{no}\right) \tag{2.37}$$

Again we assumed that the propagation delay of the cascaded stages is equivalent to the propagation delay of each stage multiplied by the number of stages. Differentiating with respect to the number of stages

$$\frac{d\tau_{Dn}}{d\,n} = \tau_o + \tau_{no}\, A_V^{1/n}\left(2n - \ln\left(A_V\right)\right) \tag{2.38}$$

It is interesting to note that the time constant that increases with supply current does not play a part in determining the optimum number of stages. Seting (2.38) to zero and solving for the optimum number of gain stages we find

$$n_{opt} = \frac{\ln A_V}{2} - \frac{\tau_o}{2\tau_{no}A_V^{1/n_{opt}}} \quad \Rightarrow$$

$$n_{opt} = \frac{\ln A_V}{2} - \frac{\tau_o}{2\tau_{no}A_{Vi}} \tag{2.39}$$

Unfortunately, this equation can only be solved numerically, assuming τ_o and τ_{no} are known. That necessitates knowledge of the technology and the particular design used. However, examining (2.39), some useful conclusions can be drawn. The first term is exactly the one derived when a single time constant was assumed. Thus, the second term is a correction factor to the simple case. It shows that the number of gain stages is less than one would expect if the independent time constant is appreciable. Also, it becomes important when the number of stages is large.

CHAPTER 3

Process Description

3.1. Introduction

The major advantage of the Complementary Bipolar Integrated Circuit (CBIC) process over a conventional all-npn process is that the one can design circuits that perform voltage level shifting and high output load drive capability and still maintain high frequency operation, large input and output voltage swing, and low power supply voltages. Another advantage is the reduced amount of time and experience needed to achieve a given level of electrical performance performance The only disadvantage is that the wafer fabrication ost is higher because more masks and diffusion steps are required.

Recently, several manufacturers have recognized these advantages and responded by CBIC processes based on either junction-isolation or dielectric isolation technologies. As a result, the speed of linear circuits such as op amps has increased by about an order of magnitude to 300 MHz unity-gain stable bandwidth.

These processes have been made available for semi-custom IC designs by the introduction of linear arrays. The main advantage of designing analog circuits in linear arrays is reduced fabrication cost and time. The device sizes and location are fixed so that the designer can only decide the connectivity between devices and the top plate area of MOS capacitors. Sometimes, the designer can also determine the layout of metal thin film resistors (if available). The disadvantages include increased layout parasitics, non-ideally matched components, and large die size.

The AT&T-ALA210 linear array [12,13] has been used for the design of this comparator. The array is fabricate using a process called CBIC-U that

features complementary vertical NPN and PNP transistors with 4 GHz and 2.5 GHz f_T respectively. Also included are metal-programmable MOS capacitors, diffused resistors, and electrostatic discharge protection (ESD) diodes, 16 bonding pads, and three areas for optional laser-trimmable Ta_2N thin film resistors. The array has 74 transistors on a 2.1 mm x 1.4 mm chip.

3.2. CBIC-U Process/Device Description

The transistors in the CBIC-U process, as shown by their cross-sections in Figure 3.1, are isolated from each other by using reverse biased junctions. Both the NPN and the PNP are true vertical devices. An n-type epitaxial layer is grown on top of the p-type substrate after the buried layers for the NPN (n-type) and PNP (p-type) are implanted. The low resistivity buried layers are used to reduce the collector parasitic resistance.

The n-type epitaxial (n-epi) layer forms the collector region of the NPN with a p-type diffusion ring isolating the devices. The collector of the PNP is formed by a deep p-type ion implantation in the epitaxial layer. Since the n-epi acts as the substrate for the PNP transistors, it should be connected to the most positive potential of the circuit to ensure device isolation. For the same reason the p-substrate should be connected to the most negative potential. Note that the p-substrate is common to the whole chip while the n-epi "wells" are independent from each other. The n-epi in CBIC-U is therefore analogous to the n-well of a CMOS process.

The critical step in the process is the formation of the NPN and PNP emitters. The emitter length for both transistors is 1.5 µm so that the base width can be made narrow while keeping low parasitic base resistance.

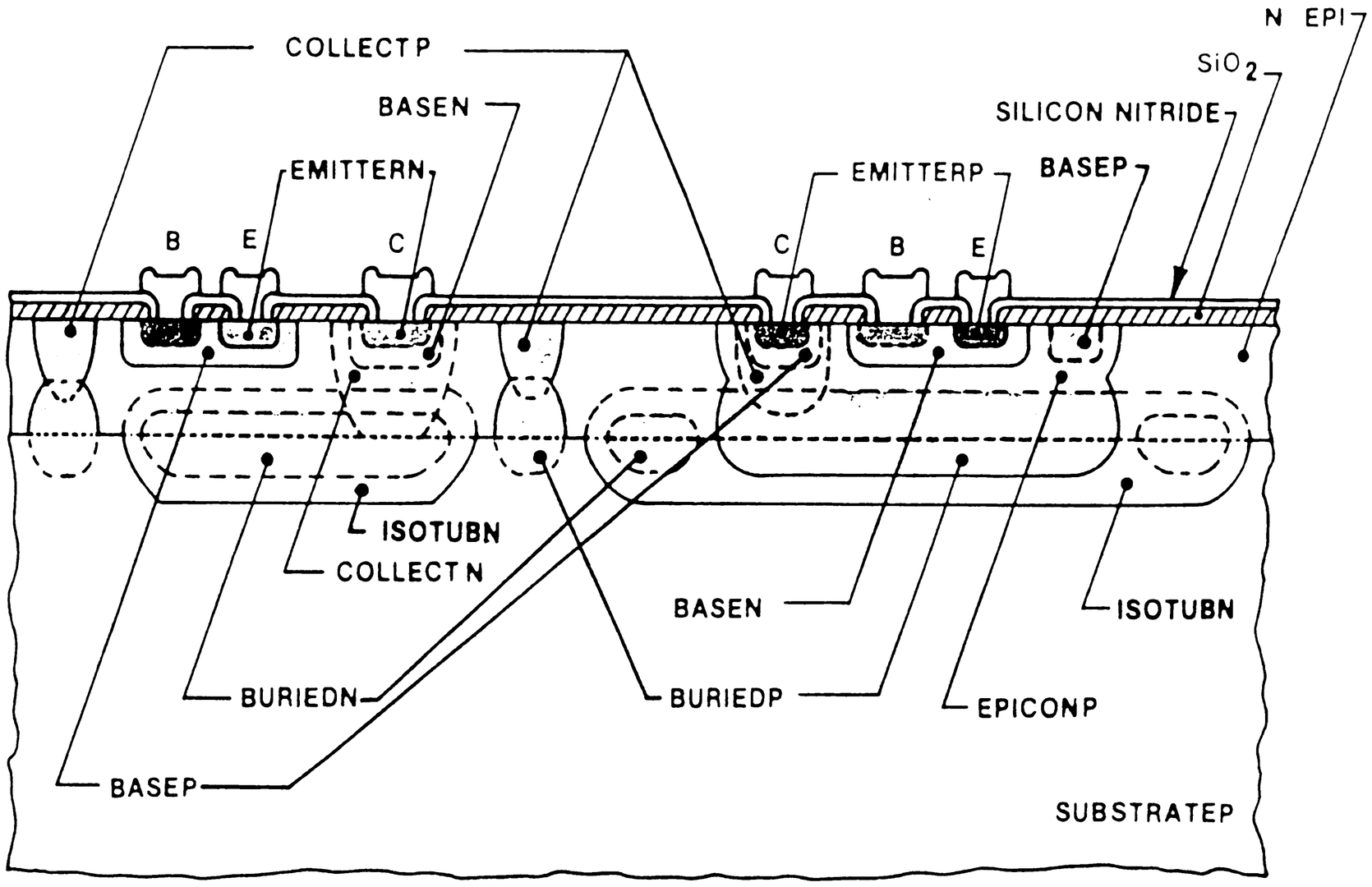


Figure 3.1. CBIC-U transistor cross-section.

3.2.1 Transistor Electrical Characteristics

The smallest device available in the CBIC-U technology has a single emitter stripe with a length of 5 µm. However the smallest NPN and PNP devices available in the AT&T-ALA210 linear array have two emitter stripes with a length of 15 µm each. The name of the NPN follows the AT&T nomenclature, and is called NU231A01, while the PNP is called PU231A01. The explanation for the AT&T nomenclature follows:

N	=>	transistor type (N for NPN's, P for PNP's)
U	=>	technology (U for CBIC-U)
2	=>	number of emitter stripes per device
3	=>	length of each emitter stripe divided by 5 µm
1	=>	number of collector contacts
A	=>	version (A)
0	=>	layout style (0 for standard device)
1	=>	number of devices within same isolation

EXAMPLES:

PU432A01 - A PNP transistor in the CBIC-U technology with four emitter stripes each 15 µm in length and two collector contacts. The layout is one PU432A device in a single isolation.

NU663A02 - An NPN transistor in the CBIC-U technology with twelve emitter stripes each 30 µm in length and six collector contacts. The layout architecture is two NU663A devices side-by-side in a single isolation.

Tables 3.1 lists the electrical characteristics for the NU231A01 and the PU231A01 transistors.

TABLE 3.1

Typical CBIC-U Transistor Electrical Characteristics (T_A=25 °C)

Parameter	Condition	NU231A01	PU231A01	Units
f_T	I_E=1mA, V_{CE}=3V	3.5	2.7	GHz
h_{FE}	I_E=1mA, V_{CE}=2V	125	35	-
V_A	I_E=1mA,V_{CE}=2, 4V	40	14	V
$V_{CE(sat)}$	I_C=1mA, I_B=0.1mA	0.13	0.13	V
V_{BE}	I_E=1mA, V_{CB}=2V	0.785	0.795	V
BV_{CEX}, typ/min	I_C=100μA, I_B=0.1μA	18/12	18/11	V
BV_{CBO}, typ/min	I_C=1μA	40/20	24/15	V
BV_{CSO}, typ/min	I_C=1μA	72/50	40/20	V
BV_{EBO}, typ/min	I_E=10μA	5.3/4.7	5.4/5.0	V
BV_{EBS}, typ/min	I_C=1μA	4.7/2.0	2.8/0.5	V
I_{EBO}, typ/max	I_C=0, V_{BE}=2V	0.02/1	0.01/1	μA
I_{CES}	V_{CE}=5V	1		nA
I_{CBO}	V_{CB}=10V, I_E=0	1		nA
$r_{BX}+r_{BI}$	-	20+70	26+46	Ω
$r_{CX}+r_{CI}$	-	31+170	38+110	Ω
t_F	V_{CB}=0	25	23	ps
C_{JEo}	V_{BE}=0	120	120	fF
C_{JCo}	V_{CB}=0	166	317	fF
C_{JCSo}	V_{CS}=0	368	769	fF

The physical mechanisms contributing to the breakdown voltage of the NPN is different from that of the PNP. The NPN collector-to-emitter breakdown is attributed to the avalanche breakdown of the collector-to-base junction (BV_{CBO}). If the impedance of the circuit connected to the base is high, the

transistor breaks down in the BV_{CEX} mode due to beta multiplication of the avalanche generated carriers, and it can be as low as 12 V. If the impedance at the base is low, then the transistor breaks down in the BV_{CBO} mode which is much higher (20.8 V minimum).

The breakdown mechanism of the PNP is attributed to base punchthrough. In the BV_{CEX} mode, the base width is depleted and the collector is effectively shorted to the emitter. If the circuit at the emitter is high impedance the breakdown is increased by the additional voltage required to zener the emitter-to-base diode (about 5 V). These mechanisms are illustrated by the fact that the difference between BV_{CBO} and BV_{CEX} is typically 22 V for the NPN and only 6 V for the PNP; a big difference considering the NPN has about four times higher h_{FE} than the PNP.

Shown in Figures 3.2 and 3.3 are the I_C-V_{CE} transistor characteristics. The non-linearity of the Early Voltage is more apparent for the PNP than the NPN. The transistor Gummel plots are shown in Figures 3.4 and 3.5. Figures 3.6 and 3.7 show the unity-gain frequency (f_T) variation as a function of the collector current. The interesting fact is that not only the PNP f_T peaks at about the same current as the NPN but also its rolloff at higher currents is actually less steep.

PSPICE transistor models are supplied by AT&T for its linear array customers. There are three sets of models; one is for the typical device performance case and the other two are for the most pessimistic and most optimistic cases. The typical case PSPICE models for all the transistor types that are available in the AT&T-ALA210 linear array are listed in Appendix A3.1. The PSPICE models are similar to the conventional three-terminal SPICE models with a diode modeling the fourth terminal (substrate) node.

However, since CBIC-U uses junction isolation, there is an isolation junction associated with each transistor, and its parasitic effect must be included in the transistor model. This junction is actually the collector-base junction of the parasitic transistor. Its emitter-base junction is the collector-base junction of the desired transistor. When the collector-base junction of the desired transistor is

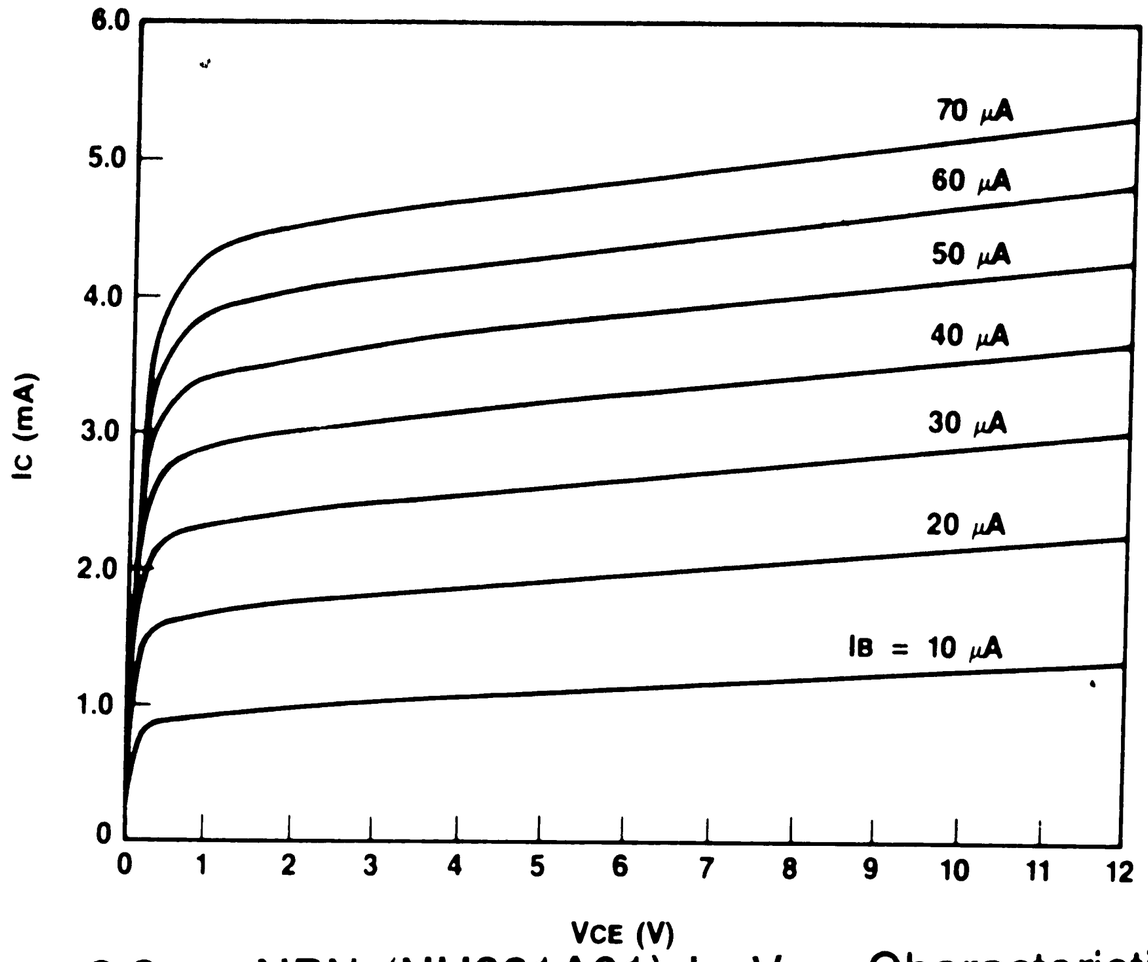


Figure 3.2. NPN (NU231A01) I_C-V_{CE} Characteristics

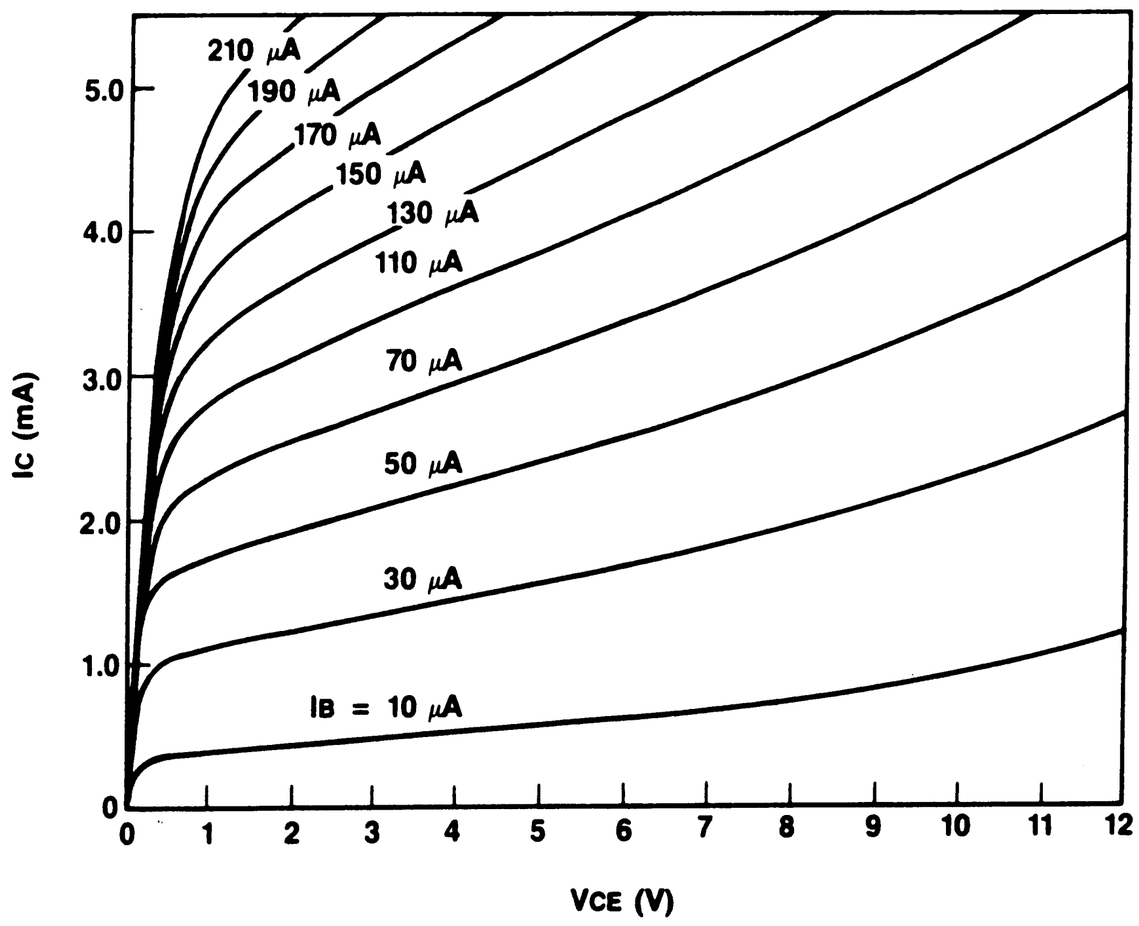


Figure 3.3. PNP (PU231A01) I_C-V_{CE} Characteristics

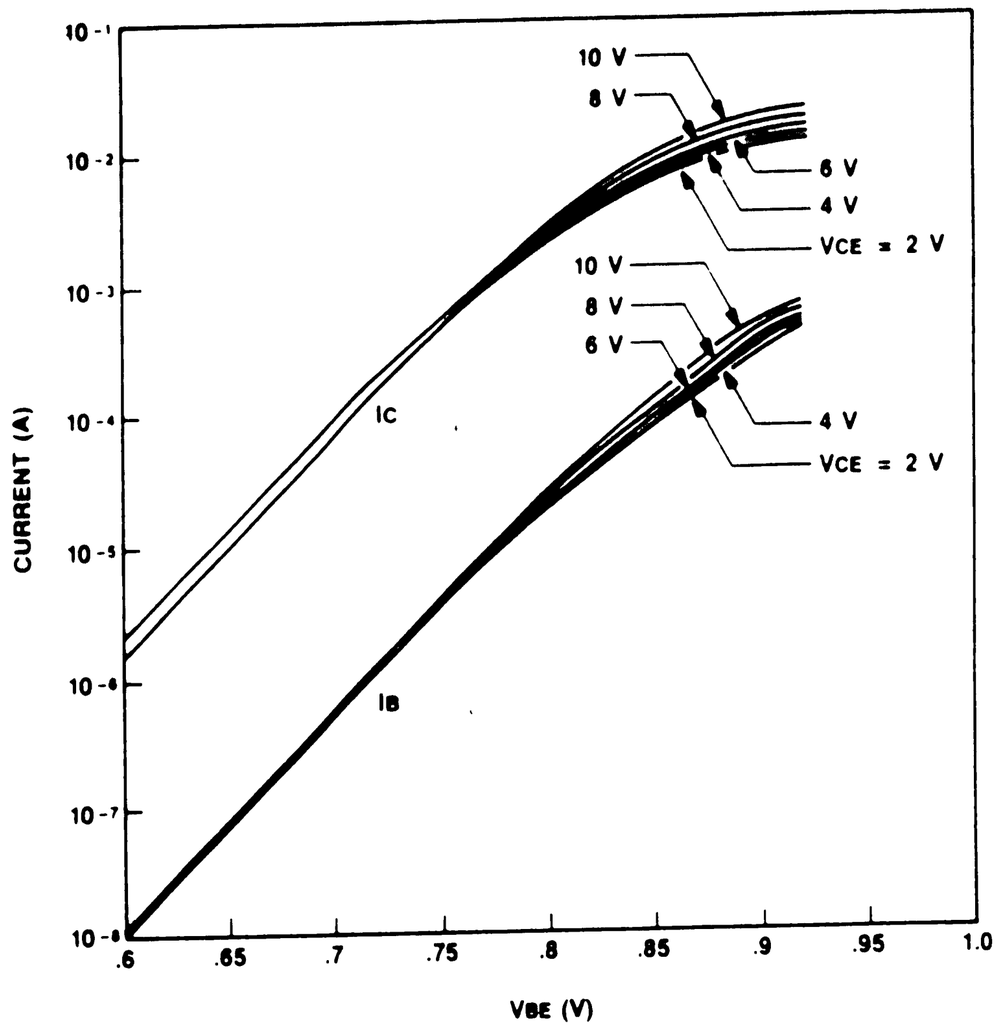


Figure 3.4. NPN (NU231A01) Gummel Plot

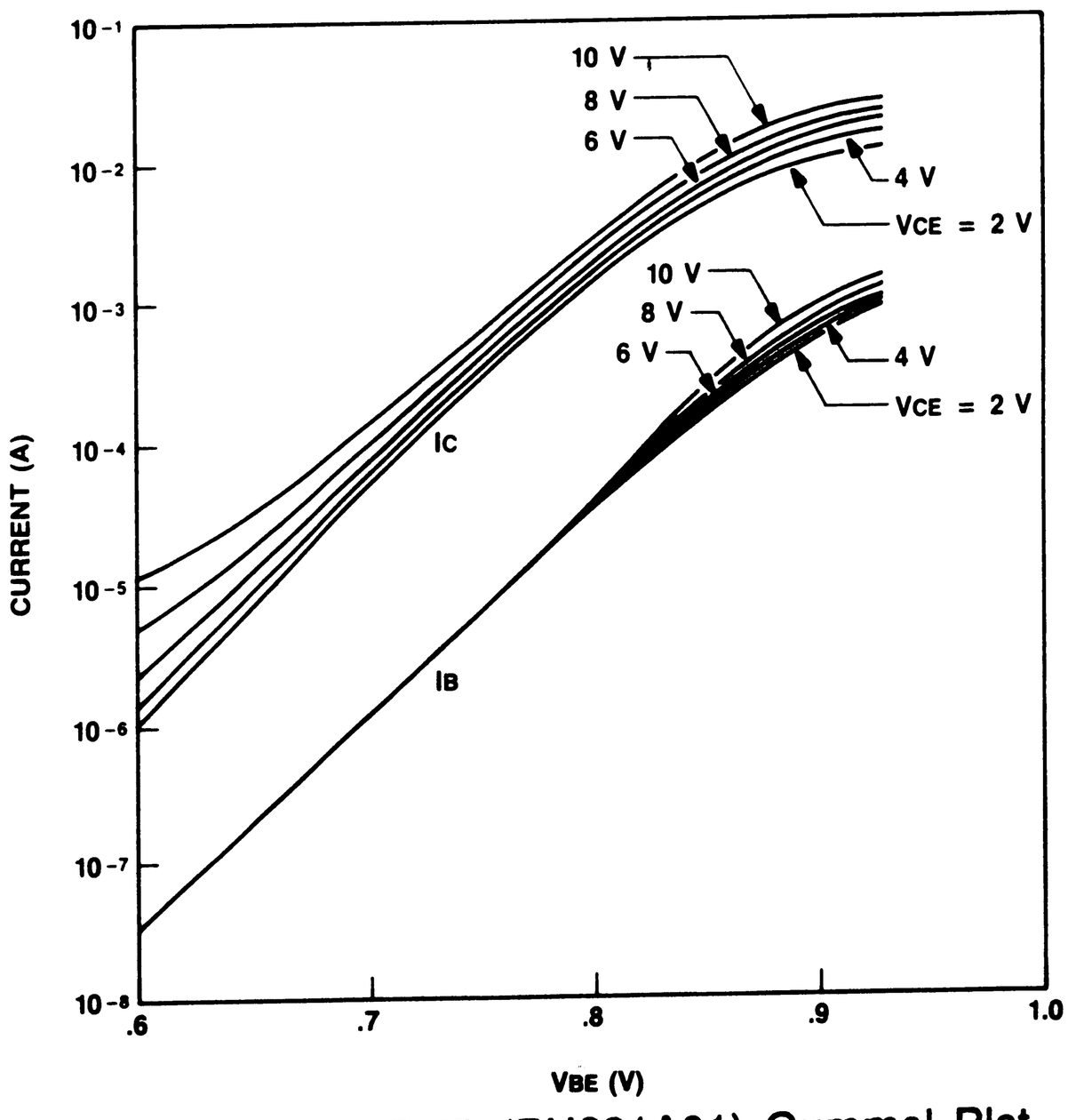


Figure 3.5. PNP (PU231A01) Gummel Plot

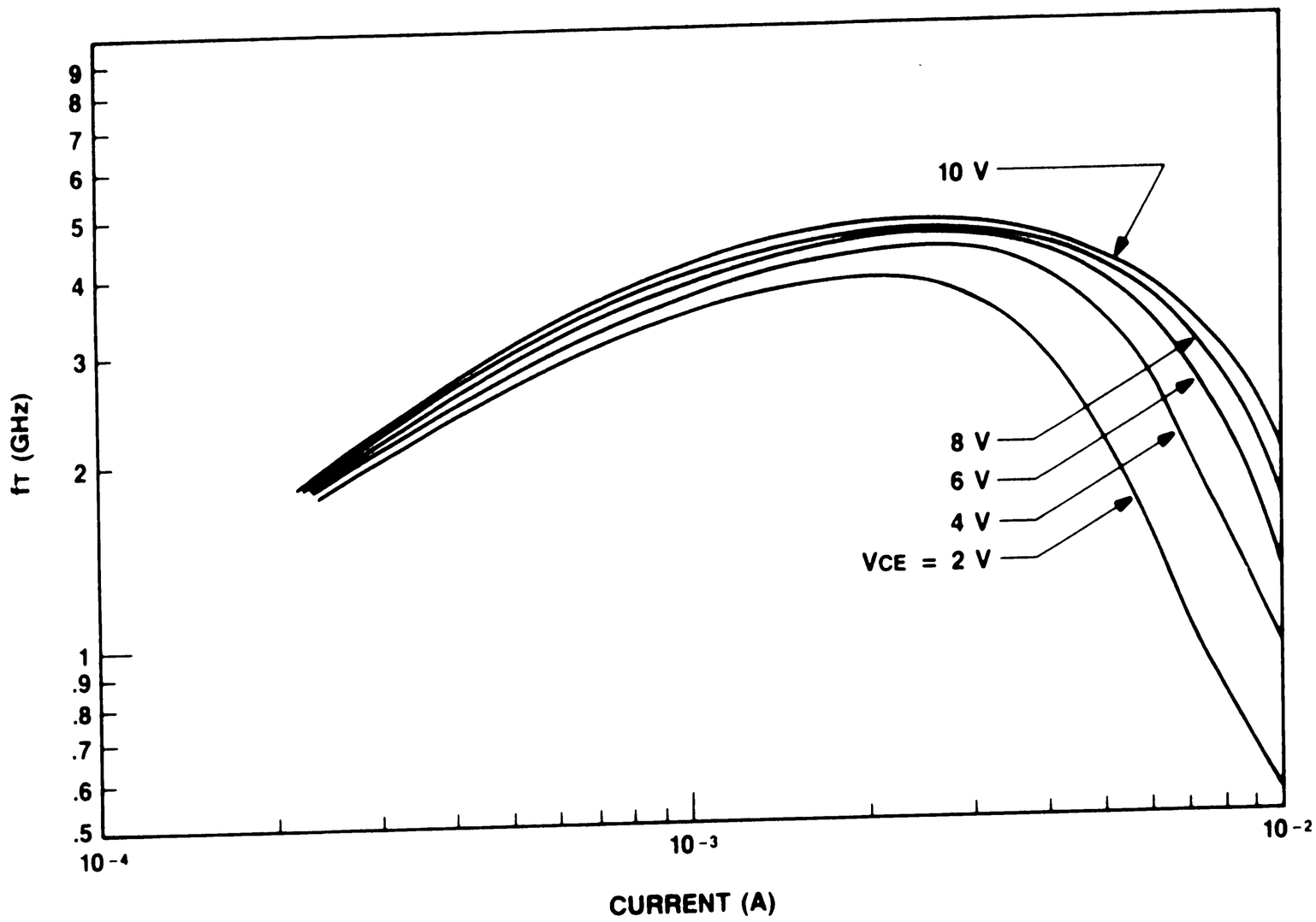


Figure 3.6. NPN (NU231A01) Unity-gain frequency response

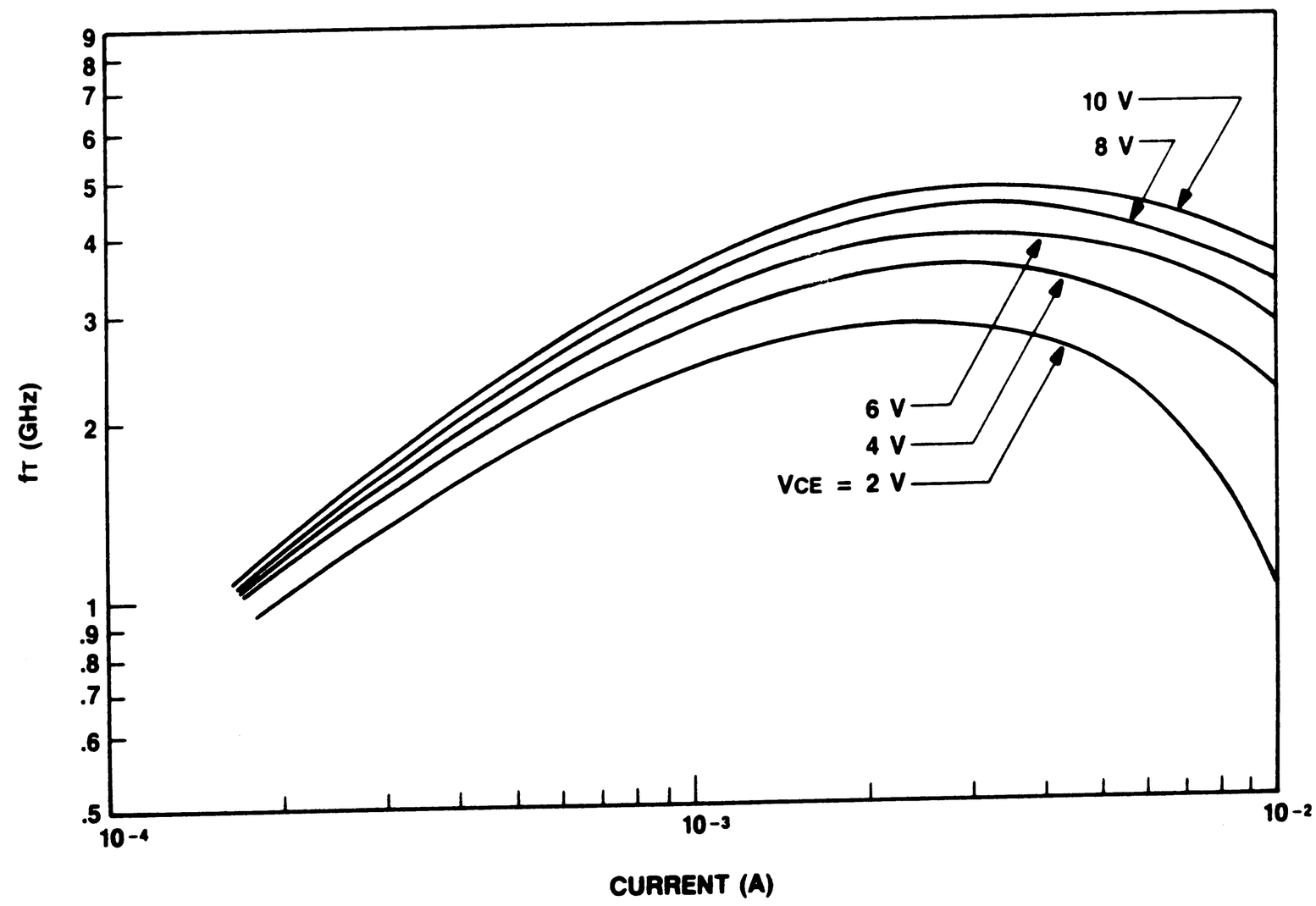


Figure 3.7. PNP (PU231A01) Unity-gain frequency response

forward biased, current is shunted from the base of the transistor to the isolation region via transistor action of the parasitic transistor. Therefore a true four-terminal model is needed for a transistor that operates in the quasi-saturation and saturation region.

AT&T's internal ADVICE simulator uses an Extended Gummel-Poon bipolar transistor model which includes terms to model collector resistance modulation in quasi-saturation operation and the parasitic transistor to isolation. For more accuracy, ADVICE has been used to simulate the comparator circuit.. However, the simulation results should be very similar with the ones that would have been obtained if PSPICE was used. This is because the comparator devices do not operate in the saturation region.

3.2.2 Resistors

There are three standard resistor types available in the CBIC-U process; two diffused and one thin film.The diffused resistors are formed by separate boron implants in the n-epi. RUL and RUH , as they are called by AT&T, have sheet resistances of 50 Ω/sq and 1080 Ω/sq respectively.

The thin film resistors are made of sputtered Ta_2N stabilized to 300 Ω/sq sheet resistance. The thin film resistors, called STIC (the acronym for Silicon Tantalum Integrated Circuit) are deposited on top of the dielectric that covers the bottom level metal. Then, the top level metal is deposited and forms the ohmic connection to the STIC resistors. The STIC can be selectively trimmed by a laser beam and therefore its resistance value can be adjusted to a very high accuracy. We used this feature to design the resistors of the comparator so that the input offset voltage can be accurately nulled. Listed below on Table 3.2 are the characteristics of the three resistor types.

TABLE 3.2

Resistor Characteristics (T_A = 25 °C)

Parameter	RUL	RUH	STIC	Units
Sheet Resistance	50	1080	300	Ω/sq
Tolerance	±20	±20	+30,-20	%
Mismatch	±1	±1	-	%
TCR	1380	1770	-200	ppm/°C

3.2.3 Capacitors

There are two types of capacitors available in the CBIC-U process. One, called MNOS (for Metal-Nitride-Oxide-Silicon), is formed by growing two thin films of SiO_2 and Si_3N_4 on top of low sheet resistivity silicon. The top plate is made of the bottom layer metal Thus the value of the capacitor can be programmed by changing the area of the metal.

For very small capacitor values a Metal-on-Metal (MOM) capacitor can be used. This is formed by the top and bottom layer metal. Table 3.3 lists the characteristics of the two types of capacitors. The mismatch refers to the ratio error between two capacitors of the same type as a function of the center-to-center distance. The leakage parameters apply to MNOS capacitors of less than 30 pF and MOM capacitors of less than 4 pF.

TABLE 3.3

Capacitor Characteristics (T_A = 25 °C)

Parameter	MNOS	MOM	Units
Capacitance Density	3.413E-4	4.413E-5	pF/(μm²)
Area/pF	2930	22660	(μm²)/pF
Absolute Tolerance	±15	±35	%
Mismatch	±1E-4	±3E-4	%/μm
Minimum Value	0.75	0.005	pF
Max. Leakage at 10 V	500	500	pA
Breakdown Voltage	35	-	V

3.2.4 Metallization

A sandwitch of Au-Ti-Pt forms the first and second level metal with vias connecting the two levels. Both levels have 0.04 Ω/sq sheet resistance and can carry 2 mA/μm reliably. An otional thick Au metal may be plated on the top level metal that reduces its sheet resistance to 0.004 Ω/sq and increases its current handling capability to 14 mA/μm. Also, there are Ti-Pt links that are used as fusible links for trimming. Table 3.4 list the metalization characteristics. The metal parasitics per unit length are based on 5 μm and 10 μm wide bottom and top level metal respectively.

TABLE 3.4

Metalization Characteristics (T_A = 25 °C)

Parameter	Bottom Metal	Top Metal	Units
Sheet Resistance	0.04	0.04	Ω/sq
Min. Width	5	10	μm
Min. Spacing	5	10	μm
Thickness	0.4	0.4	μm
Max. Curr. Density	2	2	mA/μm
Max. Resistance	8	4	Ω/mm
Inductance	1.28	1.15	nH/mm
Capacitance to Si	0.17	0.21	pF/mm
Parallel Path Capac.	0.02	0.03	pF/mm

CHAPTER 4

Circuit Design

4.1. Introduction

As discussed in Chapter 2, the system in which the comparator is used determines the block level characteristics of the comparator. In this chapter we investigate circuits that meet these block level requirements.

The circuit is partitioned into four stages. The input stage primarily determines the DC precision characteristics of the comparator. The second stage performs the voltage level shift and determines the minimum power supply voltage that can be used. It is this stage that utilizes the vertical PNP transistors to perform the voltage level shift while maintaining high frequency operation.

The third stage simply provides more voltage gain.The output not only drives the load but also determines the digital output level compatibility with 100K ECL logic. A bandgap reference generates the currents needed to bias the circuit and minimizes the variations of the comparator gain and output logic levels as a function of perturbation in operating ambient temperature and power supply voltage.

After the design of the cicuit is completed, the layout and package parasitics effects on the comparator performance are investigated. This is important since the high frequency operation can be greatly reduced by parasitics. Finally, the predicted performance of the comparator, based on simulation results, is presented.

4.2. Input Stage

As pointed out previously, the design of the first stage determines the precision performance that can be attained by the comparator. The reason for this is that the errors, such as offset voltage, induced by the first stage are multiplied by the total comparator gain and show up as a large error at the output. However , the errors induced by the later stages are multiplied by a smaller gain and, therefore are not as important as the first stage. An alternative way of saying the same statement is that the errors of the first stage add directly to the input-referred comparator error while the error contribution of the later stages is divided by the gain preceding each stage.

High precision and high speed operation of a given circuit are mutually exclusive. Therefore, in trying to optimize the precision of the input stage, the speed performance of the comparator can be severely degraded. To optimize both high precision and high speed operation, the limitations of the commonly used emitter-coupled pair differential amplifiers are investigated and an improved design is proposed. The same basic topology is used for the first three gain stages. The biasing requirements are then calculated with the purpose of maintaining constant gain as a function of temperature. The input offset voltage is calculated with the purpose of designing a circuit and an algorithm to laser trim it. The rest of the input stage precision parameters are subsequently calculated.

4.2.1 Conventional Diferential Amplifier

The emitter-coupled pair differential amplifier, shown in Figure 4.1, is the most often used circuit in high speed comparators. It is useful as an input stage because it has low offset voltage and high frequency response.

There are many variations of the basic topology [14]. For example: a common-base (cascode) stage is often connected on top of the input transistors to help reduce the Miller multiplication of the collector-to-base junction

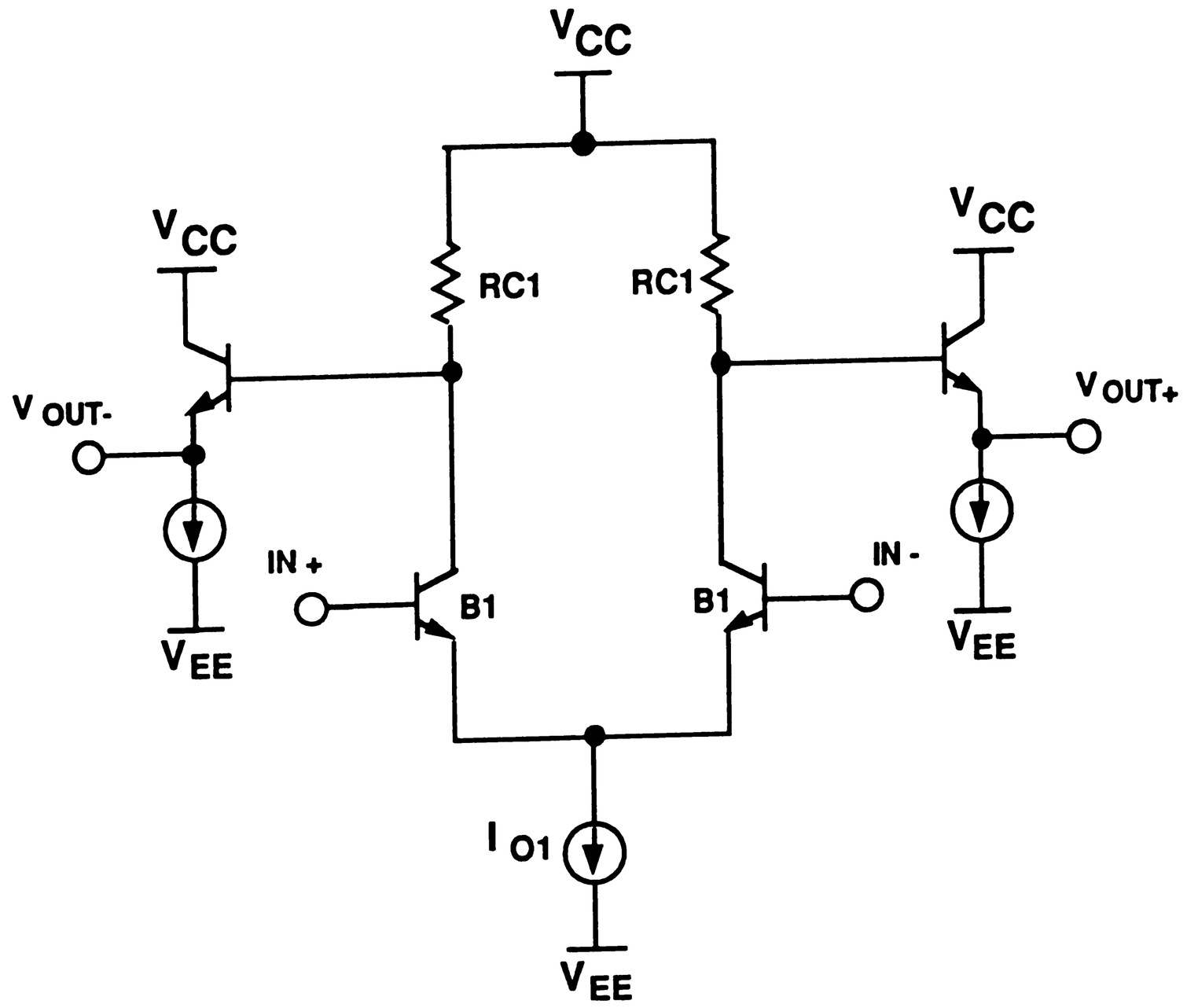


Figure 4.1. Emitter-coupled pair differential amplifier

capacitance. Often, emiter followers are used to drive the input so that high input impedance and low input bias current can be achieved.

The fundamental performance limitations of the basic differential amplifier can be investigated by calculating the propagation delay based on the simplified AC model [15] shown in Figure 4.2. This model is a single-ended approximation of the differential amplifier that includes the parasitic metal capacitance and the collector-base junction capacitance of the emitter follower Q2 lumped into a single capacitor CC1. Using the Miller approximation, the propagation delay can be found to be

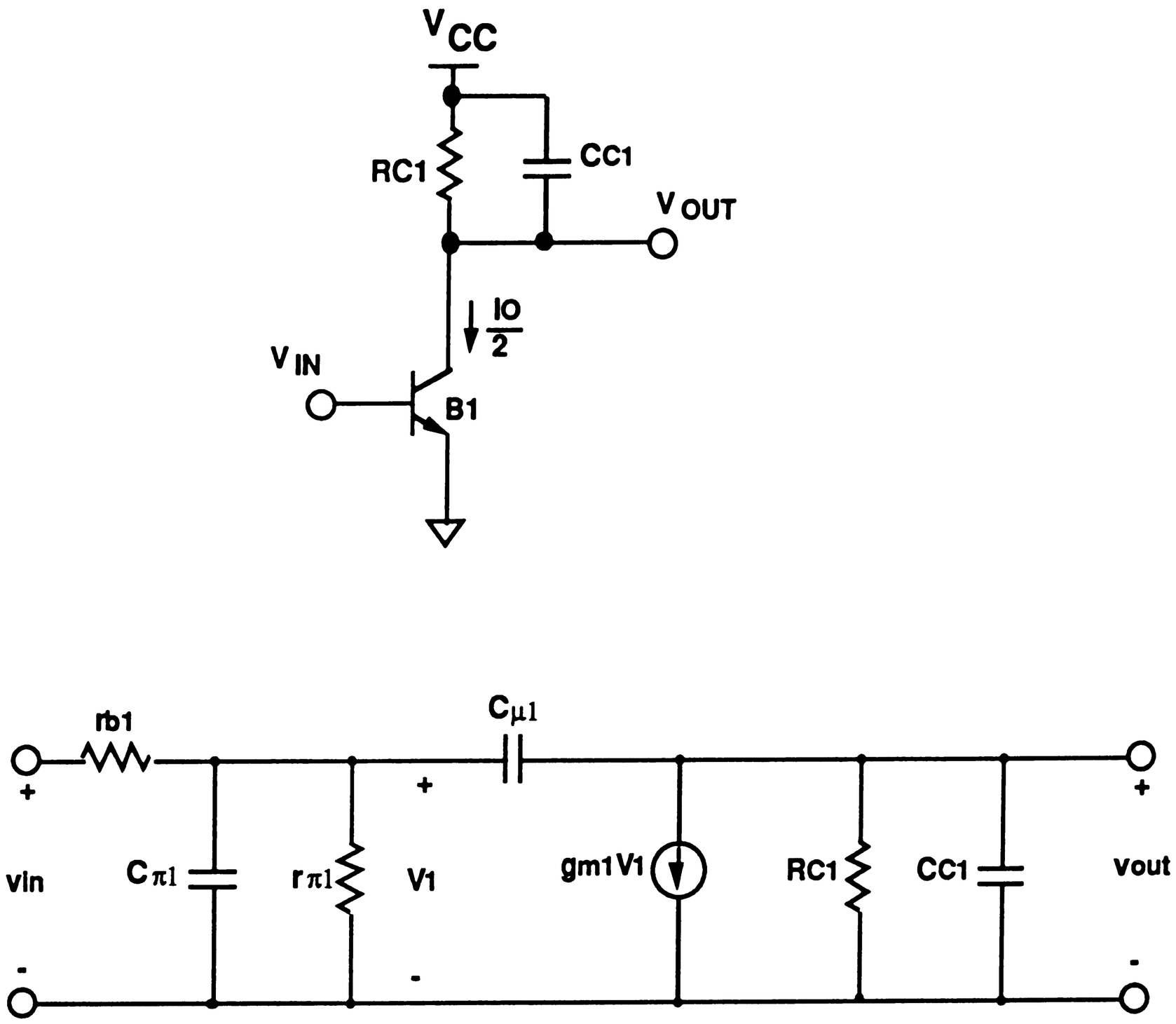


Figure 4.2. Simplified AC model of the differential amplifier

$$\tau_{BW} = r_{b1} C_{\pi 1} + r_{b1} C_{\mu 1} (1 + g_{m1} R_{C1}) + R_{C1} C_{C1} \qquad (4.1)$$

where:

r_{b1}	=>	base resistance (including source impedance)
$C_{\pi 1}$	=>	base-emitter junction and diffusion capacitance
g_{m1}	=>	transconductance of the input transistor Q1
$C_{\mu 1}$	=>	collector-base junction capacitance
C_{C1}	=>	total collector capacitance

Noting that

$$C\pi = C_{je} + g_m \tau_F \tag{4.2}$$

and

$$C_{C1} = 2\,C\mu_1 + C_{CS1} + C_{M1} \tag{4.3}$$

where:

C_{je}	=>	base-emitter junction capacitance
τ_F	=>	base transit time
C_{CS1}	=>	collector-substrate capacitance
C_{M1}	=>	metal parasitic capacitance

we can rewrite (4.1) as follows

$$\tau_{BW} = r_{b1}\,(C_{je1} + C\mu_1) + g_{m1}\,\tau_F\,r_{b1} + A_{Vi}\,(r_{b1}\,C\mu_1 + \frac{C_{C1}}{g_{m1}}) \tag{4.4}$$

where, A_{Vi} is the DC gain of the amplifier given approximatelly by

$$A_{Vi} \approx g_{m1}\,R_{C1} \tag{4.5}$$

The performance limitations of the simple differential amplifier can be illustrated by examining Equation (4.4) closely. The first right-half term depends only on the device process parameters and, to a first order, does not scale with device size. The value of the second term is proportional to the transistor bias current since

$$g_{m1} \approx \frac{I_{C1}}{V_T} \tag{4.6}$$

where V_T is the thermal voltage constant (about 26 mV at room temperature). The third time constant is due to the time required to charge the collector parasitic capacitances. The significant result is that this term increases in proportion to the required DC voltage gain and decreases with increased bias current. Also, note that the comparator input bias current is equivalent to the transistor base current. This is important because if an attempt is made to

increase the DC gain and reduce the input bias current then the third term, which is usually the dominant, will increase; thus limiting the amplifier speed.

The best performance that can be achieved by this stage can be found by noting that the second term increases and the third term decreases with bias currentt. Therefore, there is an optimum bias point for which the propagation delay is maximized. Differentiating (4.4) with respect to g_{m1}, we find the its optimum value to be

$$g_{m1} = \sqrt{\frac{A_{Vi}\, C_{C1}}{\tau_F\, r_{b1}}} \tag{4.7}$$

and the minimum value of the propagation delay to be

$$\tau_{BW,min} = r_{b1}\,(C_{je1} + C_{\mu 1}) + A_{Vi}\, r_{b1}\, C_{\mu 1} + 2\sqrt{A_{Vi}\, C_{C1}\, \tau_F\, r_{b1}} \tag{4.8}$$

Note that even the optimum gain can be found from the system requirements. This was found in Chapter 2 (Equation (2.35)) to be 7.389. Thus, Equation (4.4) has been reduced to a sum of time constants that depend on process parameters only. To get an empirical feeling for the magnitude of the time constants involved we assume the following process parameter values:

$r_{b1} = 115\ \Omega$	$C_{je1} = 540$ fF	$C_{\mu 1} = 100$ fF
$C_{cs1} = 170$ fF	$C_{M1} = 300$ fF	$\tau_{F1} = 25$ ps

then the minimum propagation delay is

$$\tau_{BW,min} = (74 + 85 + 239)\ \text{ps} = 398\ \text{ps} \tag{4.9}$$

It is obvious that the bigest term is the one associated with the parasitic collector capacitance which makes up 60 % of the total value of the propagation delay. It is the purpose of the proposed circuit described in the next section to reduce this time constant.

The optimum transistor bias current can be found from (4.6) and (4.7) to be

$$I_{C,opt} = 1.1 \text{ mA}$$

which is about a factor of two higher than what is required to keep the comparator input bias current low. Reducing this bias current will result in an increase of the propagation delay. It is, therefore, important that the modified circuit achieve the minimum propagation delay with a low bias current of the input transistors.

4.2.2 Differential Amplifier with Active Load

The simplified schematic diagram of the modified differential amplifier is shown in Figure 4.3 [15,16]. The simple resistive load is replaced by a feedback circuit that forces the impedance at the node connected to the collectors of the input stage devices to be low. Threfore, the parasitic capacitance CC1 has less of an effect on the amplifier speed. For this reason versions of this basic circuit have been used in a variety of high speed circuits, such as frequency dividers. The object of this investigation is to see the applicability of this cicuit technique for the design of fast high precision comparators.

As in the previous section, the performance of this circuit can be demonstrated by analysing its simplified single-sided AC model shown in Figure 4.4. Again using the Miller approximation, the propagation delay is found to be

$$\tau_{BW} = r_{b1} C\pi_1 + r_{b1} C\mu_1 \left(1 + \frac{g_{m1} R_{C1}}{1 + g_{m2} R_{C2}}\right)$$

$$+ \frac{R_{C1} C_{C1}}{1 + g_{m2} R_{C2}} + \frac{r_{b2} C_{IN2} + R_{C2} C_{C2}}{1 + g_{m2} R_{C2}} \qquad (4.10)$$

The terms are the same as the previous section with the addition of

$$C_{IN2} = C\pi_2 + C\mu_2 (1 + g_{m2} R_{C2}) \qquad (4.11)$$

and

$$C_{C2} = 2 C\mu_2 + C_{CS2} + C_{M2} \qquad (4.12)$$

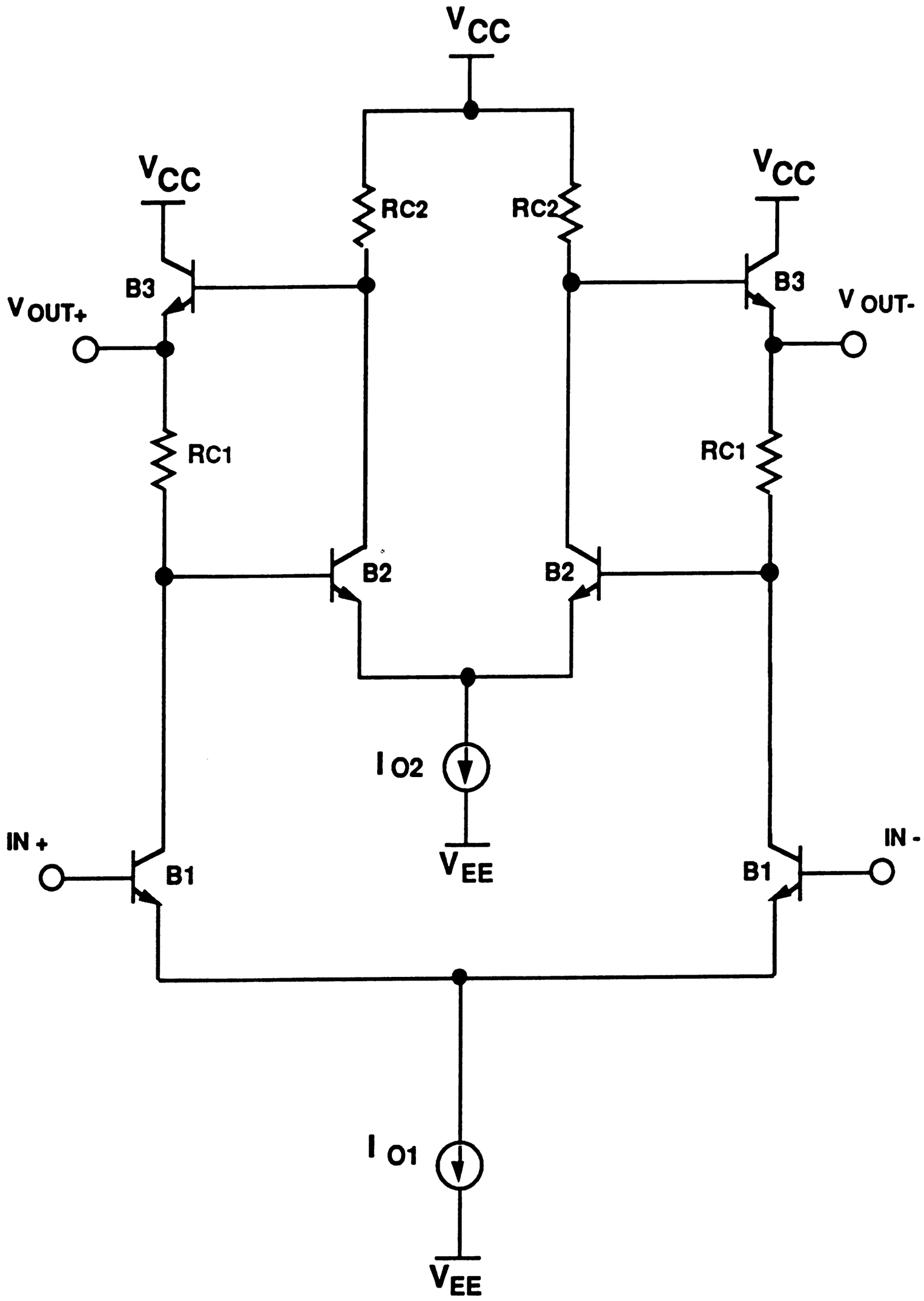
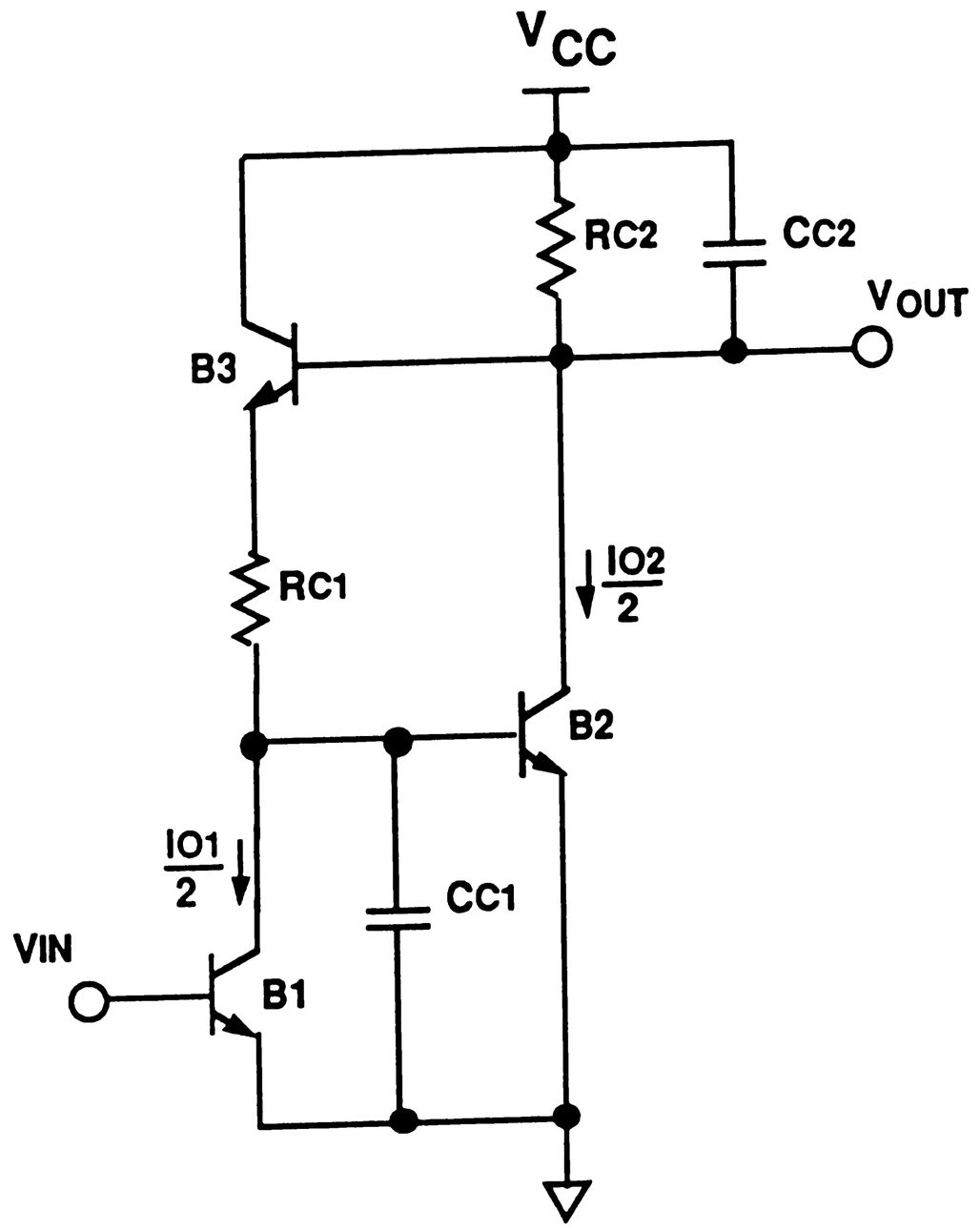


Figure 4.3. Differential amplifier with active load



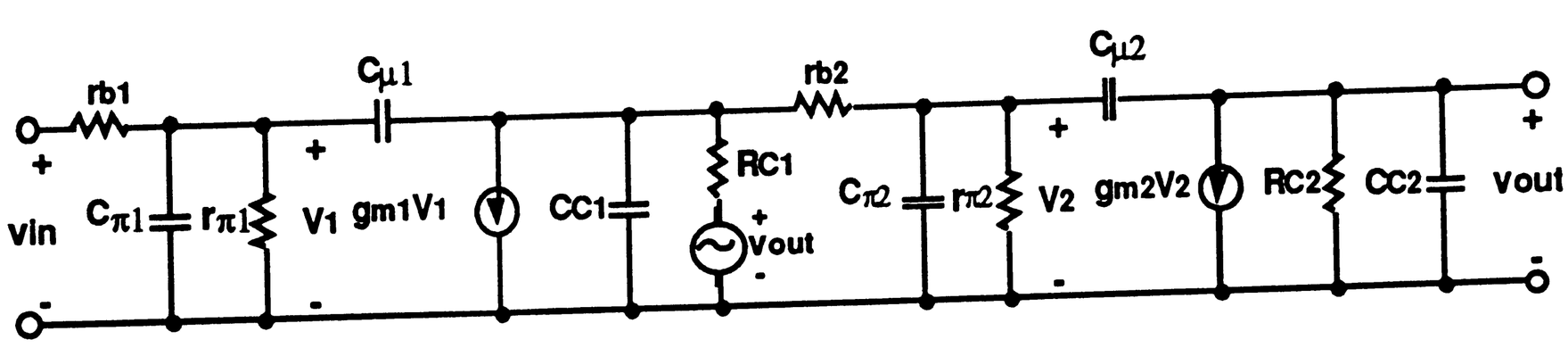


Figure 4.4. Simplified AC model of the modified differential amplifier

It is important to recognize that the open-loop gain of the feedback amplifier is approximatelly given by

$$A_{Vi} \approx g_{m2} R_{C2} \tag{4.13}$$

Combining equations (4.2), (4.5), (4.10), (4.11), (4.13) and assuming that A_{V2} is much larger than unity we find

$$\tau_{BW} = r_{b1}(C_{je1} + C\mu_1) + g_{m1}\tau_F r_{b1} + \frac{A_{Vi}}{A_{V2}}(r_{b1} C\mu_1 + \frac{C_{C1}}{g_{m1}})$$

$$+ r_{b2}(C\mu_2 + \frac{C_{je2}}{A_{V2}}) + \frac{g_{m2}\tau_F r_{b2}}{A_{V2}} + \frac{C_{C2}}{g_{m2}} \tag{4.14}$$

Note that the first three terms are the same as the ones in Equation (4.4) with the exception of the third term which is divided by the gain of the feedback amplifier. Since this used to be the dominant time constant, it can be decreased by simply increasing the gain Av2. There are three more time constants introduced but those are lelatively small. As in the previous section, the optimum bias of the input transistors is

$$g_{m1,opt} = \sqrt{\frac{A_{Vi} C_{C1}}{A_{V2}\tau_F r_{b1}}} \tag{4.15}$$

This is a very important result since it indicates that the required current and therefore the comparator input bias current decreases with the square root of the feedback amplifier gain. Thus, in designing the circuit, one can compute the required feedback amplifier gain from the input bias current requirements by simly solving Equation (4.15) for A_{V2}. Similarly, the optimum bias current of the feedback amplifier transistors is

$$g_{m2,opt} = \sqrt{\frac{A_{V2} C_{C2}}{\tau_F r_{b2}}} \tag{4.16}$$

with A_{V2} defined by (4.15). Therefore, from (4.15)

$$A_{V2} = \frac{A_{Vi} C_{C1}}{g^2_{m1opt} r_{b1} \tau_F} \tag{4.17}$$

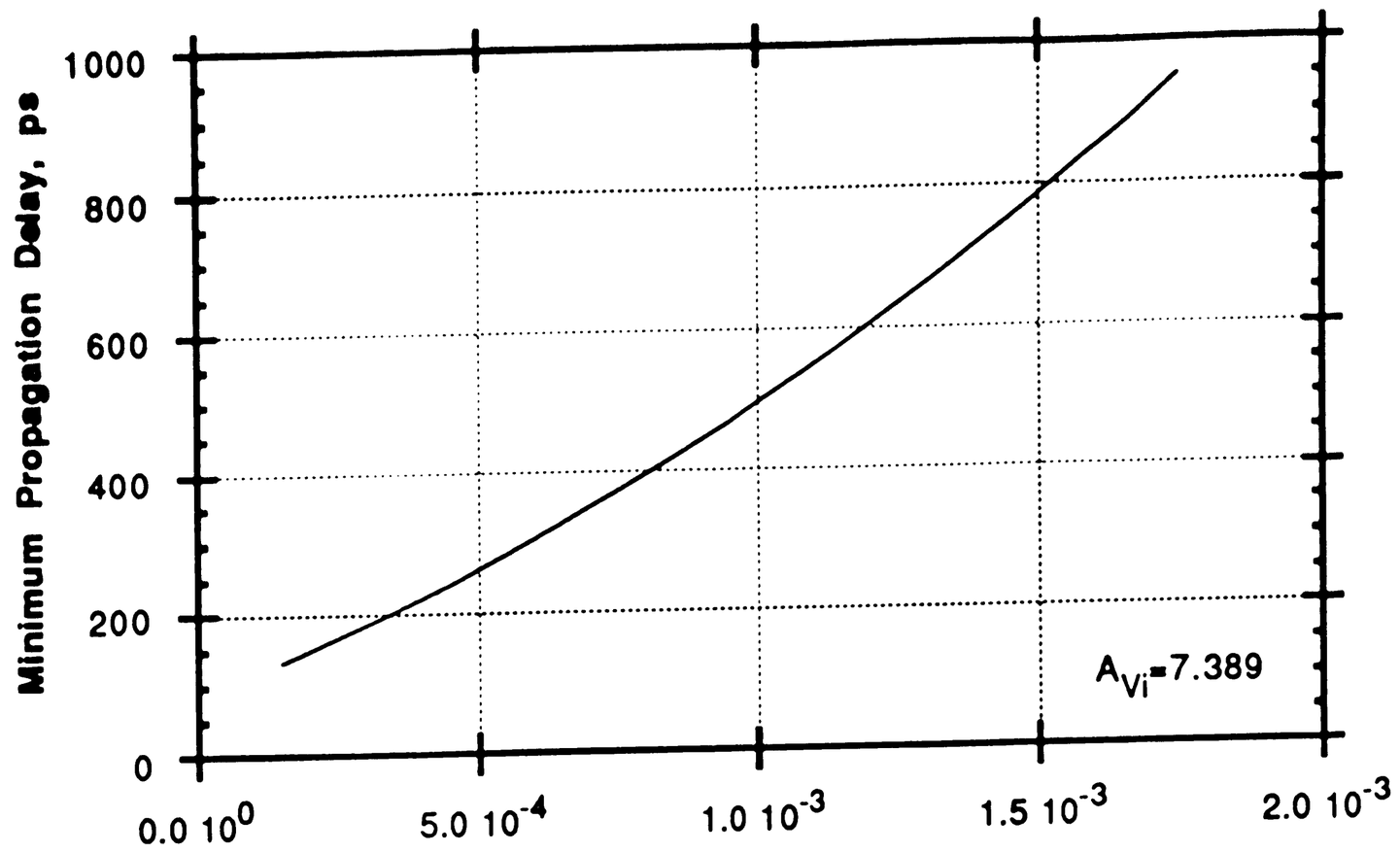


Figure 4.5. Modified differential amplifier propagation delay

we find

$$g_{m2,opt} = \frac{\sqrt{A_{Vi}}}{\tau_F\, g_{m1opt}} \sqrt{\frac{C_{C1}\, C_{C2}}{r_{b1}\, r_{b2}}} \tag{4.18}$$

Then, combining the last equation with (4.14), the optimum propagation delay is

$$\tau_{BW,min} = r_{b1}\,(C_{je1} + C_{\mu 1}) + r_{b2}\, C_{\mu 2} + g_{m1,opt}\, \tau_F\, r_{b1} \left[2 + g_{m1,opt}\, r_{b1} \left(\frac{C_{\mu 1} + \frac{C_{je2}\, r_{b2}}{A_{Vi}\, r_{b1}}}{C_{C1}}\right) + \frac{2}{\sqrt{A_{Vi}}} \sqrt{\frac{r_{b2}\, C_{C2}}{r_{b1}\, C_{C1}}}\right] \tag{4.19}$$

It is interesting to find what is the numerical result of (4.19) based on the process parameters given in the previous section. Also, assume that

$r_{b2} = 90\ \Omega$ $\quad C_{je2} = 540$ fF $\quad C_{\mu 2} = 100$ fF

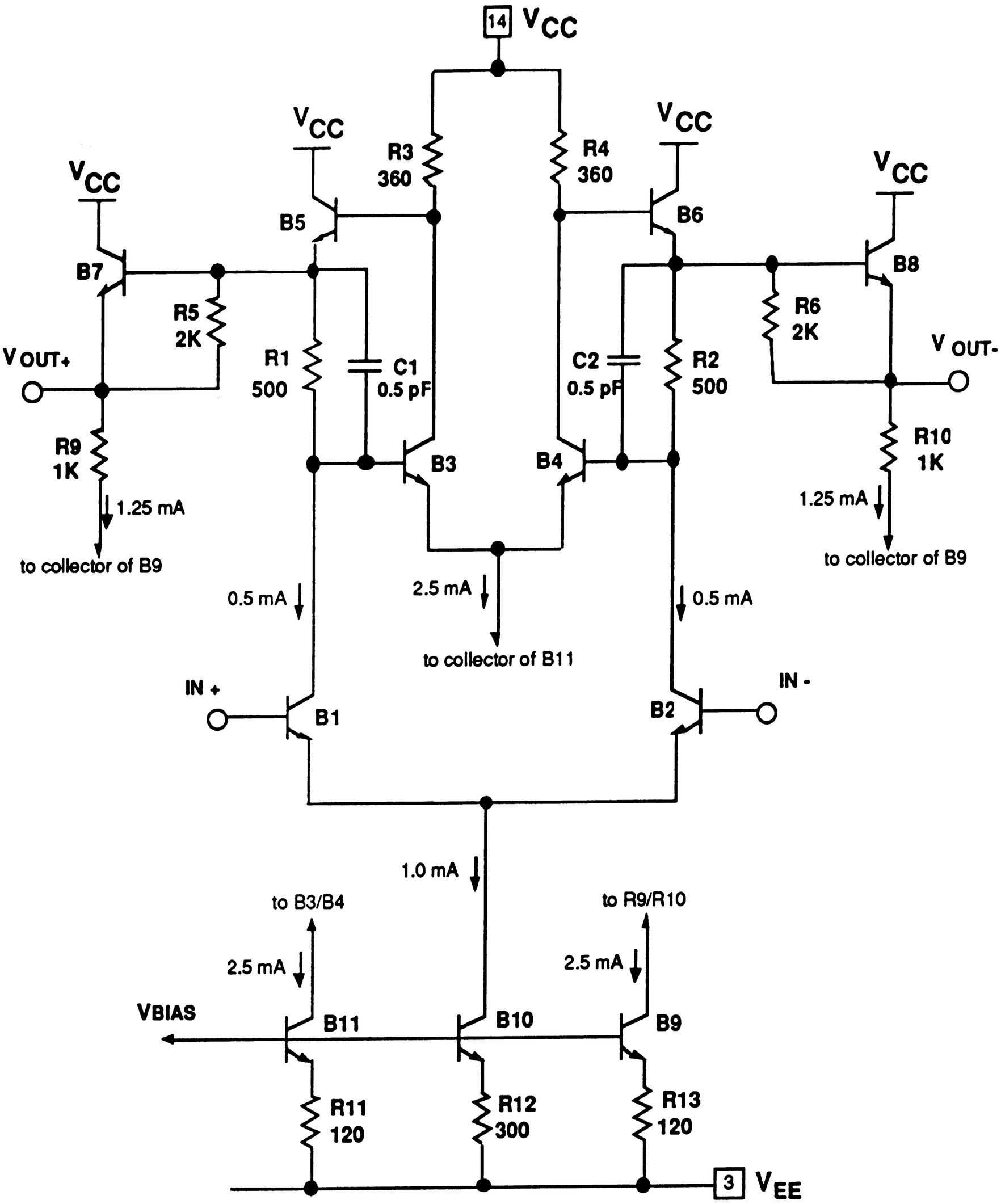
$C_{CS2} = 170$ fF $\quad C_{M2} = 300$ fF

The minimum propagation delay is plotted in Figure 4.5 as a function of the current biasing the input transistors (B1). It is evident that the propagation delay

is lower that the one for the simple differential pair with very low input bias currents. For example, 0.5 mA of collector current the propagation delay is reduced to 255 ps; a 36 % improvement.

Based on the results of the above investigation, it is evident that the modified differential pair with active feedback, if used, results in the reduction of the propagation delay and, at the same time, in the reduction of the input bias current.

The complete input stage schematic is shown in Figure 4.6. Transistors B9, B10, and B11 serve as curreent sources and are biased by a bandgap reference to be described later. The emitter follower buffer the output from the input of the next stage. The capacitors C1 and C2 are necessary to reduce the gain peaking caused by parasitic metal capacitances connected to the collector of the input transistors B1 and B2.



Note: All transistor sizes are 1X (NU231A01)
unless labeled otherwise

Figure 4.6. First (input) gain stage

4.2.3 Gain Temperature Coefficient

Since the comparator is to operate over a wide temperature range, it is important to minimize the temperature coefficient of the voltage gain. The approximate value of the DC gain is given by Equatiion (4.5) and is repeated here (see Figure 4.6)

$$A_{Vi} = g_{m1} R1 \tag{4.20}$$

expanding g_{m1}

$$A_{Vi} = \frac{I_{C1} R1}{V_T} = \frac{I_{C1} R1}{KT/q} \tag{4.21}$$

The temperature coefficient of the gain is found to be

$$TC(A_{Vi}) = \frac{1}{A_{Vi}} \frac{dA_{Vi}}{dT} = \frac{1}{I_{C1}} \frac{dI_{C1}}{dT} - \frac{1}{T} \tag{4.22}$$

where it has been assumed that the temperature coefficient of the resistor R1 is zero. This is a good assumption since its finite TCR is cancelled by the TCR of the resistor located in the bandgap reference that generates the bias currents (assuming it is a resistor of the same type, which it is). For zero gain temperature coefficient, the required bias current TC is found from (4.22) to be

$$\frac{1}{I_{C1}} \frac{dI_{C1}}{dT} = \frac{1}{T} \qquad \text{, for } TC(A_{Vi}) = 0 \tag{4.23}$$

which is nominally about 3,000 ppm/°C. It is the objective of the bandgap reference design to generate a bias current with such a temperature coefficient.

4.2.4 Input Offset Voltage Trim

The input offset voltage depends on mismatch between devices in the input stage. The offset voltage is calculated so that by predicting its worst case value, a resistor circuitry can be devised to null it. This is done by a laser cutting off parts of the thin film resistor.

Assuming the the various component mismatches are statistically independent , then the total offset is the root-mean-square sum of all these mismatches. Using variational analysis, the total offset is found to be

$$V_{IO}^2 = \left(-V_T \frac{\Delta I_{S1,2}}{I_{S1,2}}\right)^2 + \left(\frac{V_T}{A_{Vi}} \frac{\Delta I_{S3,4}}{I_{S3,4}}\right)^2 + \left(V_T \frac{\Delta R_{1,2}}{R_{1,2}}\right)^2$$

$$+ \left(\frac{V_T}{\beta_{3,4}} \frac{I_{C11}}{I_{C10}} \frac{\Delta \beta_{3,4}}{\beta_{3,4}}\right)^2 + \left(-\frac{V_T}{A_{Vi}} \frac{\Delta R_{3,4}}{R_{3,4}}\right)^2 \qquad (4.24)$$

The first two terms are due to the saturation current density mismatch between the transistors at the comparator input (B1, B2) and that of the feedback amplifier input (B3, B4). The third and fourth terms are due to the load resistor mismatches of the two amplifiers. The last term is due to the current gain mismatch of the feedback amplifier input transistors.

Note that the contribution of the feedback amplifier mismatches is divided by the overall gain of the first stage, and is therefore negligible. The numerical value of the total offset can be calculated based on the following assumptions: the worst-case saturation current density mismatch between transistors is ±8 %, between resistors is ±1 %, and between transistor current gains is ±5 %. Then the total input offset voltage is

$$V_{IO,max} = \sqrt{4.33 + 0.08 + 0.07 + 0.00 + 0.01} \quad mV$$

$$V_{IO,max} = 2.12 \text{ mV} \qquad \text{(untrimmed)} \qquad (4.25)$$

It is evident that the dominant term is the first one, which is 98 % of the total value. Therefore the addition of the feedback amplifier did not degrade the input offset voltage.

The temperature coefficient of the input offset voltage can be computed by taking the derivative of the first term of (4.24) with respect to temperature.

$$\frac{dV_{IO}}{dT} = \frac{V_{IO}}{T} = 7.1 \ \mu V/°C \qquad (4.26)$$

which can be reduced by simply trimming the offset voltage.

The design of the trim circuit takes advantage of the offset voltage variability with the mismatch between gain setting resistors R1, R2 and between R3, R4 described by Equation (4.24). The design of these resistors is shown in Figure 4.7. Resistors R1, R2 are for the gross trim and R3, R4 for the fine trim. Each resistor link is intended to be cut open by the laser beam so that there will be no thin film annealing effects after packaging. Only links C and D are designed to be cut Each resistor can acquire the following values (in Ohms):

TABLE 4.1

Possible Trim Resistor Values

Link Cut	Difference from Nominal Value	R1,R2	R3,R4
None	0	500	360
D	10	510	370
C	24.69	524.69	384.69
C,D	40	540	400

The offset change due to the resistors trim is given by

$$\Delta V_{IO_{TRIM}} = V_T \left[\frac{\Delta R_{1,2}}{R_{1,2}} - \frac{1}{A_{Vi}} \frac{\Delta R_{3,4}}{R_{3,4}} \right] \qquad (4.27)$$

Assuming the gain of the first stage is 7.389 and V_T is 26 mV, then the offset change due to R1, R2 and R3, R4 trim can take the following values

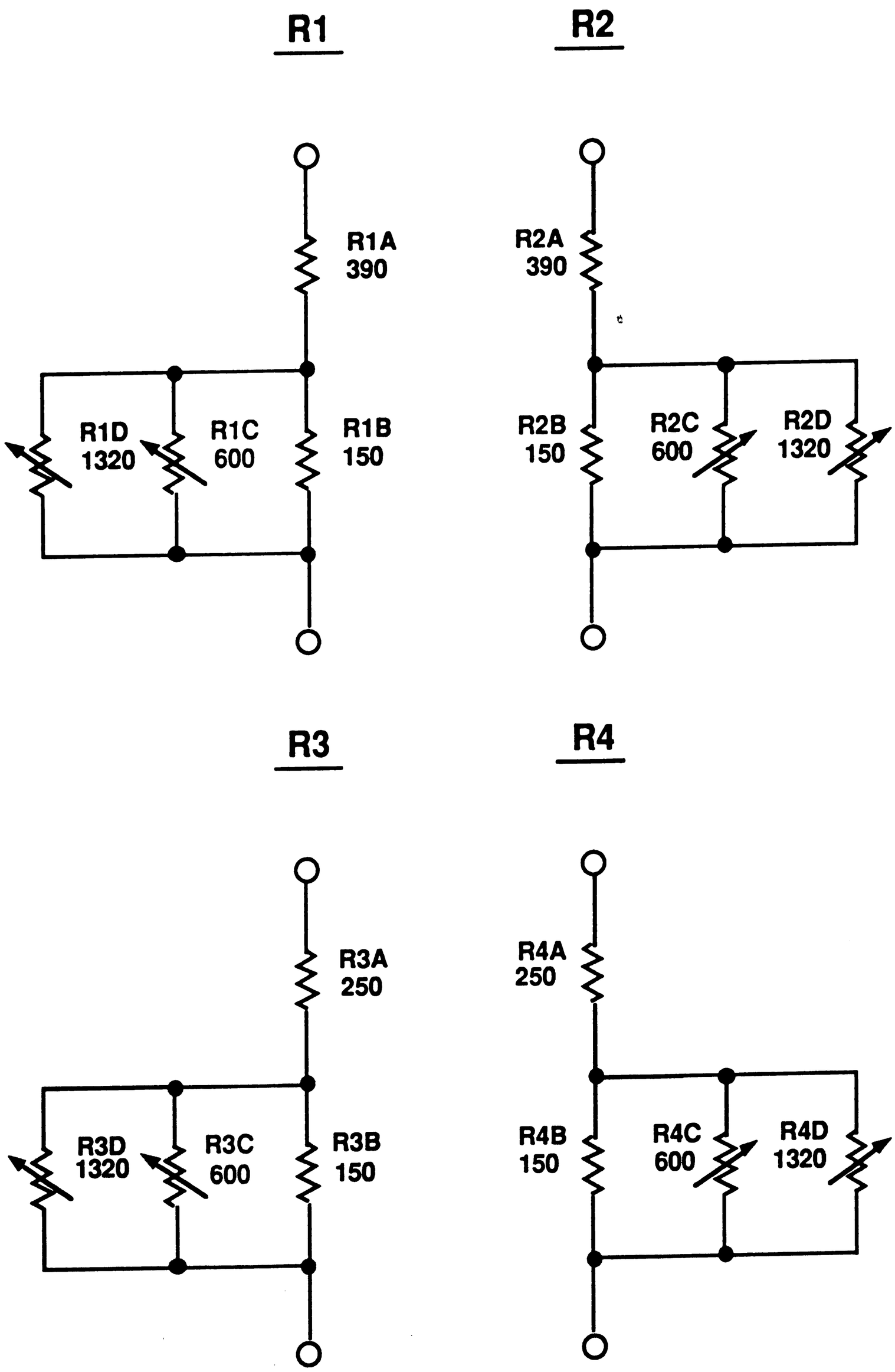


Figure 4.7. Trim resistors

TABLE 4.2

Offset Voltage Change Due to R1, R2 Trim

Link Cut	R1 (Ω)	R2 (Ω)	$\Delta R_{1,2}/R_{1,2}$ (%)	ΔV_{IO} (mV)
R2D,R2C	500	540	-7.69	-2.00
R1D, R2D, R2C	510	540	-5.71	-1.49
R2C	500	524.69	-4.82	-1.25
R1D, R2C	510	524.69	-2.84	-0.74
R2D	500	510	-1.98	-0.51
R1D	510	500	+1.98	+0.51
R1C, R2D	524.69	510	+2.84	+0.74
R1C	524.69	500	+4.82	+1.25
R1D, R1C, R2D	540	510	+5.71	+1.49
R1D, R1C	540	500	+7.69	+2.00

TABLE 4.3

Offset Voltage Change Due to R3, R4 Trim

Link Cut	R3 (Ω)	R4 (Ω)	$\Delta R_{3,4}/R_{3,4}$ (%)	ΔV_{IO} (mV)
R4D,R4C	360	400	-1.42	-0.37
R3D, R4D, R4C	370	400	-1.05	-0.27
R4C	360	384.69	-0.90	-0.23
R3D, R4C	370	384.69	-0.53	-0.14
R4D	360	370	-0.37	-0.10
R3D	370	360	+1.98	+0.10
R3C, R4D	384.69	370	+2.84	+0.14
R3C	384.69	360	+4.82	+0.23
R3D, R3C, R4D	400	370	+5.71	+0.27
R3D, R3C	400	360	+7.69	+0.37

From the results of the above tables, we conclude that the offset can be trimmed to a resolution of about ±50 μV and a range of ±2.37 mV.

4.2.5 I_B, I_{OS} Calculation

The comparator input bias current is equivalent to the base current of the input satge transistors B1, B2. It is given by

$$I_B = \frac{I_{C1,2}}{\beta_{1,2}} \approx \frac{0.5\ mA}{125} = 4\ \mu A \qquad (4.28)$$

The offset current is equivalent to the difference between the base currents of B1 and B2. It is caused by the β mismatches of these two devices.

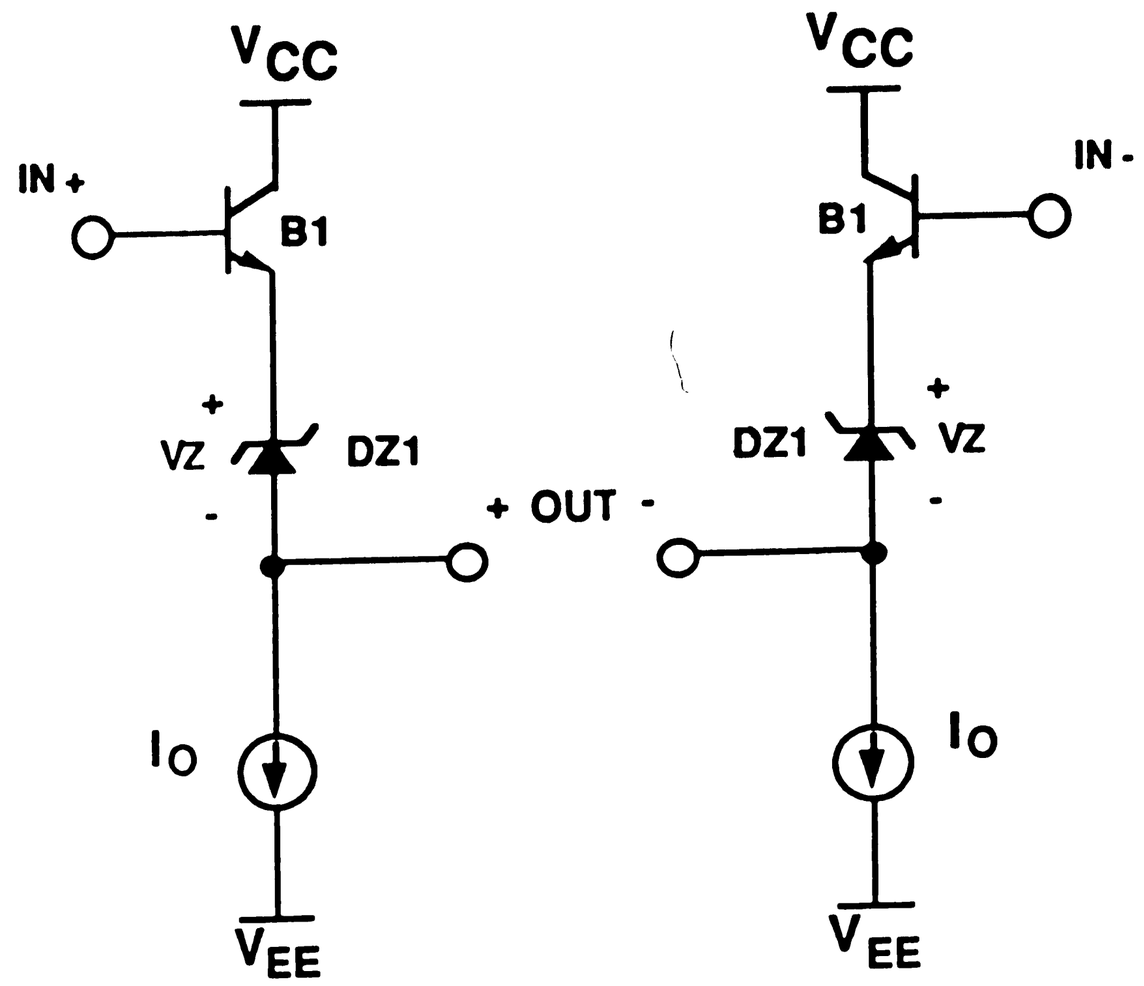


Figure 4.8. Zener diode level shift circuit

Thus,

$$I_{OS} = \frac{I_{C1,2}}{\beta_{1,2}} \frac{\Delta\beta_{1,2}}{\beta_{1,2}} = 4\,\mu A\ 5\,\% = 200\ nA \tag{4.29}$$

Since both the input offset voltage and input offset current depend primarily on the mismatch between the input devices B1 and B2, particular care should be taken to locate these devices at the proper place during the chip layout.

4.3. Level Shift Stage

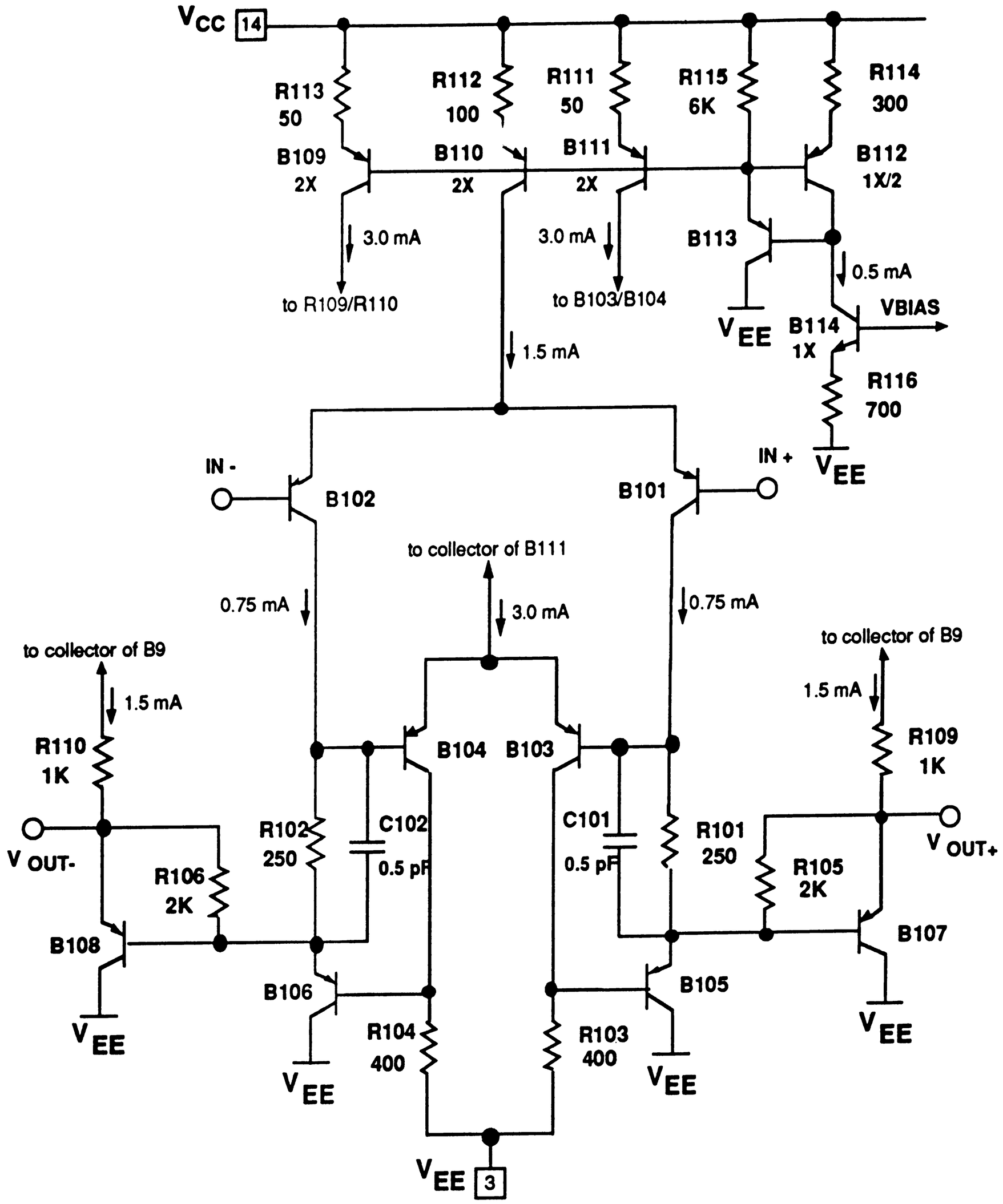
The second stage performs the voltage level shift. This is important as to allow the output to be a negative voltage (required by ECL compatibility), while the common-mode input can swing positive or negative.

In conventional all-NPN technologies, the most feasible way of level shifting is with a Zener diode as shown in Figure 4.8. The diodes are driven by the first stage with emitter follower (B1). The current sources Io force the diodes

into the low impedance breakdown mode.If ±5 V supplies are used, then the common-mode output voltage is negative, since the breakdown of the Zener diodes is usually about 5.5 V.

There are several problems with Zener level shifting, including long term drift, large mismatch, and noise. These problems can cause input-reflected DC errors and ecsessive noise but with careful design they can be neutralized. The difficult problem to get around is that the total power supply voltage has to be greater than the Zener breakdown voltage. This requirement hinders the flexibility in selecting power supply voltages; a disadvantage for a general building-block device.

These problems are overcome by using the vertical PNP transistors available in the complementary bipolar process CBIC-U as shown in Figure 4.9. It is basically identical to the first stage except the NPN has been replaced by PNPs. The bias currents are higher to account for the higher parasitic capacitances of the PNPs.



Note: All transistor sizes are 1X (PU231A01) unless labeled otherwise

Figure 4.9. Second (level shift) gain stage

4.4. Third Stage Amplifier

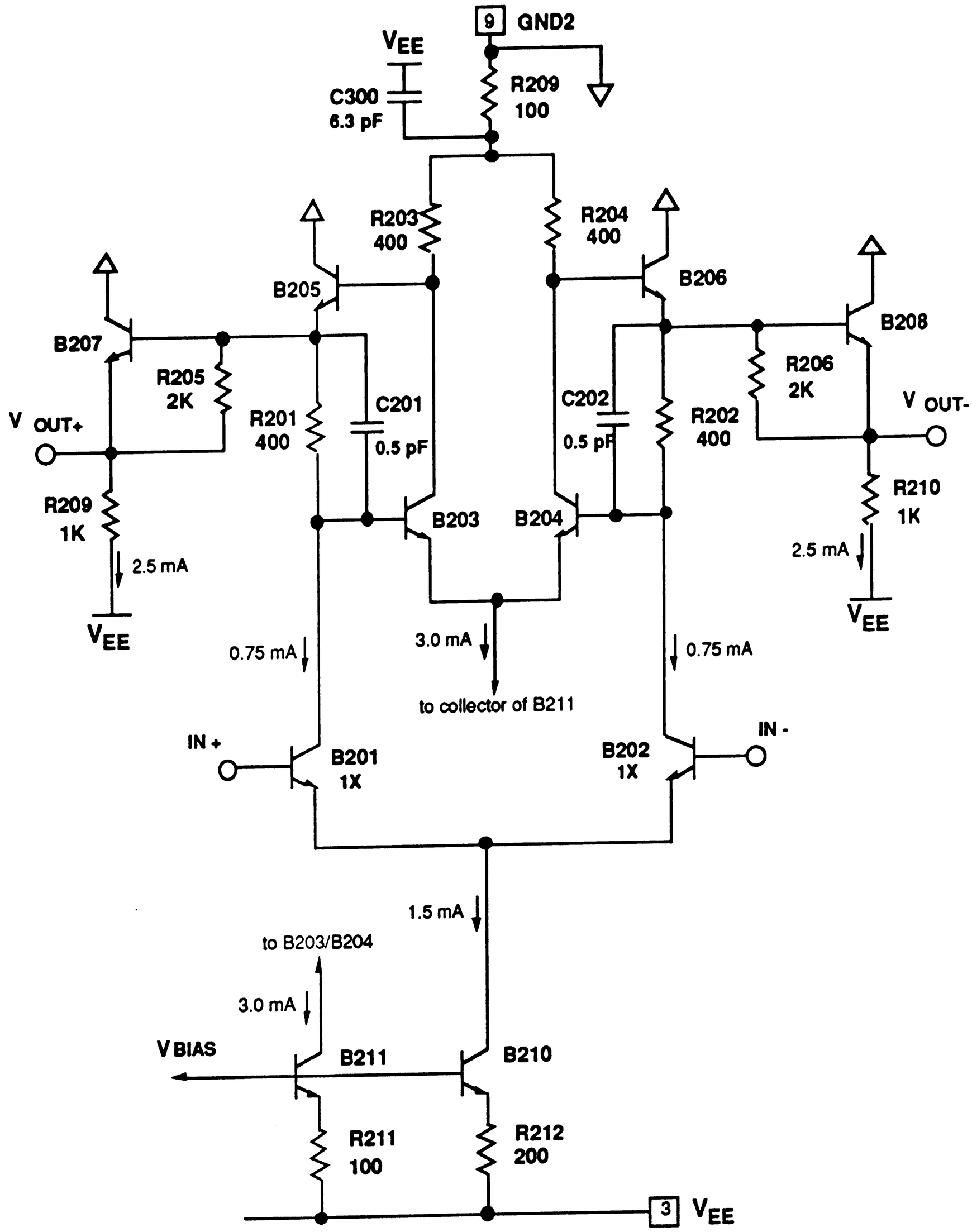
The schematic diagram of the third stage is shown in Figure 4.10. Its topology is the same as the first stage amplifier. The bias currents are larger to maintain high speed with the larger gain needed by the overall comparator requirements.

The bias resistors R213, R214 of the output emitter followers are connected to VEE for the lack of more NPN transistors in the linear array. The purpose of resistor R209 is to lower the output common-mode voltage so that the input transistors of the next stage will not enter the saturation region. Capacitor C300 lowers the impedance of the node that R209 is connected to. This stage is connected to the ground through it own bonding pad GND2, separate from the ECL output emitter followers.

4.5. F100K ECL-Compatible Output Stage

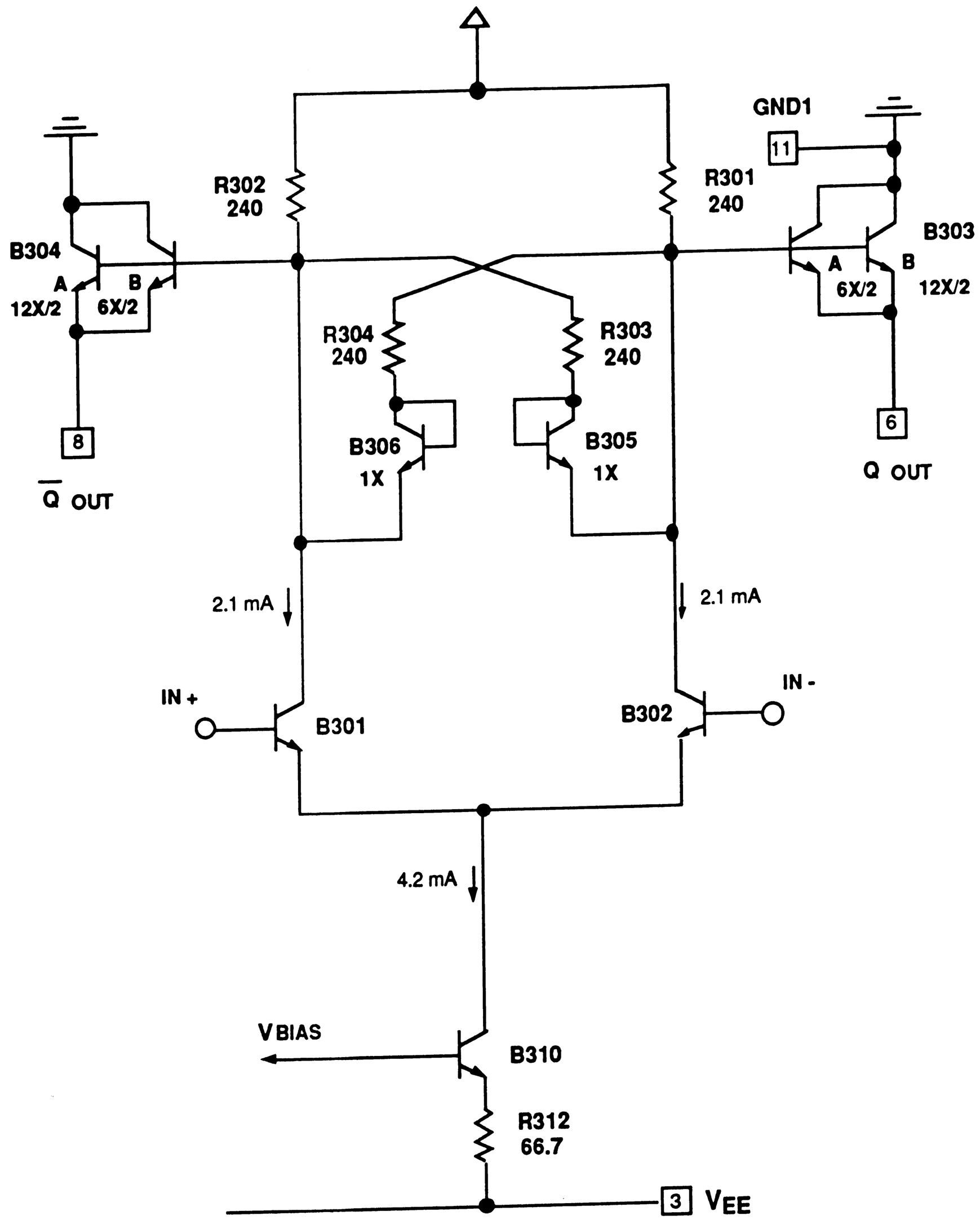
The complete schematic diagram of the output stage is shown in Figure 4.11. The amplifier topology is standard for an F100K ECL-compatible output buffer. It consists of a simple differential stage (B301, B302) amplifier and open-emitter buffers driving the external 50 Ω loads. The other terminal of the load resistor is supposed to be connected to a -2 V power supply.

What is different about this logic family are the two diodes (B305, B306) and resistors (R303, R304) connected across the gain setting resistors (R301, R302). Their function is to control the output voltage levels accuratelly over the whole temperature range. During the switching period both diodes turn off, so that the stage gain is still high. The specified output voltage levels of this ECL logic family are shown below.



Note: All transistor sizes are 2X (NU431A01)
unless labeled otherwise

Figure 4.10. Third gain stage



Note: All transistor sizes are 2X (NU431A01)
unless labeled otherwise

Figure 4.11. Fourth (ECL output) gain stage

TABLE 4.4

F100K ECL-compatible logic voltage levels

Logic Level	Min	Typ	Max	Units
High (V_{OH})	-1025	-952	-880	mV
Low (V_{OL})	-1810	-1715	-1620	mV
$V_{OH} - V_{OL}$	595	763	930	mV

In order to calculate the output voltage logic levels we assume that the voltage drop across the diodes and the base-emitter voltage of the transistors are equal while in the forward active region (V_{BEon} = 0.785 V), and

$$R301 = R302 = R1$$

$$R303 = R304 = R2 \qquad (4.30)$$

$$I_{C310} = I_0$$

Then, the low logic level is found to be

$$V_{OL} = - \frac{V_{BEon}\left(3 + \frac{R2}{R1}\right) + I_0 R1 \left(1 + \frac{R2}{R1}\right)}{2 + \frac{R2}{R1}} \qquad (4.31)$$

and the high logic level

$$V_{OH} = - \frac{V_{BEon}\left(1 + \frac{R2}{R1}\right) + I_0 R1}{2 + \frac{R2}{R1}} \qquad (4.32)$$

while the difference between the levels is given by

$$V_{OH} - V_{OL} = - \frac{V_{BEon} + \frac{I_0 R2}{2}}{2 + \frac{1}{2}\frac{R2}{R1}} \qquad (4.33)$$

A small deviation from the above calculated values should be expected due to the change of the emitter follower base-emitter voltage as a function of the output level. The find the exact solution is difficult because a degenarate equation would have to be solved.

Note from the above equations that the temperature coefficient of the output levels can be nulled by forcing Io to have a positive temperature coefficient so that it will cancell the negative temperature coefficient of the VBEon. Thus, the bias current temperature coefficient required to maintain constant gain and logic levels can be generated by one reference circuit.

4.6. Bandgap Reference

The Bandgap reference schematic diagram is shown in Figure 4.12. A reference voltage is produced by an inverted Brokaw bandgap cell (BR1, BR2) that is connected to the positive power supply. The bandgap voltage is regulated by an amplifier that provides current feedback, as opposed to the conventional voltage feedback. The feedback current comes from the collector of BR7 and has a value equal to the bandgap voltage (about 1.2 V) minus the voltage drop across the diode BR14 divided by the resistance of RR3. This current is mirrored to the rest of the comparator bias circuitry.

The current of the bandgap reference transistors is set by their emitter area ratio and the resistance value of RR1. Since the emitter area ratio is eight, then

$$I_{E1} = I_E(BR1) = I_E(BR2) = \frac{1}{RR1}\frac{KT}{q}\ln\frac{A_{E1}}{A_{E2}} \quad \Rightarrow \quad (4.34)$$

$$I_{E1} \approx \frac{26\ mV}{400\ \Omega}\ln 8 = 135.2\ \mu A \qquad (T=25\ ^\circ C)$$

Therefore, the bandgap reference voltage can be calculated as follows

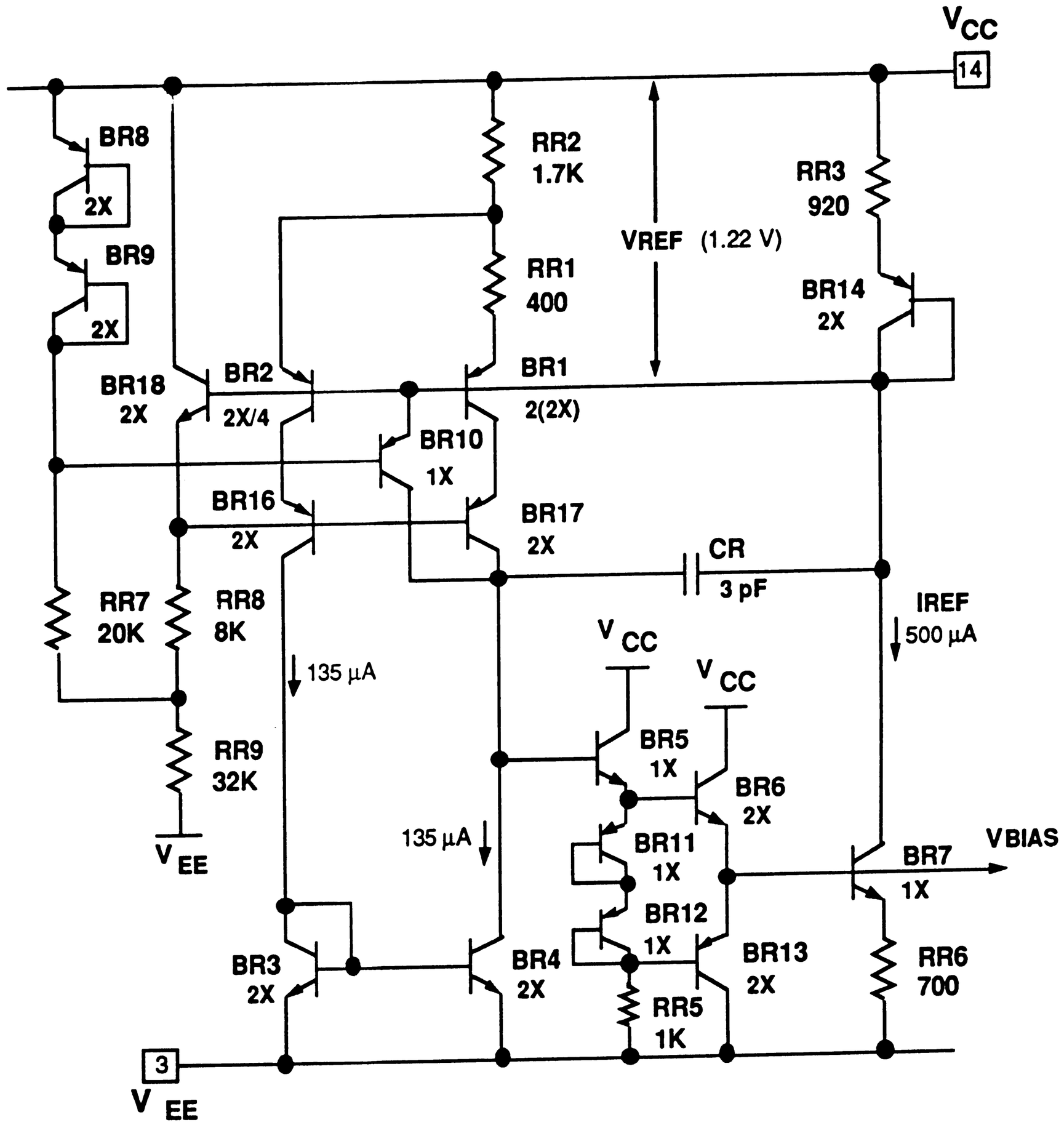


Figure 4.12. Bandgap current reference

$$V_{REF} = (I_{E1} + I_{E2})\,RR2 + V_{BE}(BR2) \quad \Rightarrow$$

$$V_{REF} = 2\,I_{E1}\,RR2 + \frac{KT}{q}\ln\frac{I_{E2}}{A_{E2}\,J_{SP}} \quad \Rightarrow \qquad (7.35)$$

$$V_{REF} \approx (2 \cdot 135.2 \cdot 1.7)\,mV + 760\,mV = 1.220\,V \quad (T=25\,^{\circ}C)$$

Once, the reference voltage is known, the refence current can be calculated from

$$I_{REF} = \frac{V_{REF} - V_{BE}(BR14)}{RR3} \qquad (7.36)$$

Combining Equations (7.34), (7.35), and (7.36) we find

$$I_{REF} = \frac{2\,I_{E2}\,RR2 + V_{BE}(BR2) - V_{BE}(BR14)}{RR3} \quad \Rightarrow$$

$$I_{REF} \approx 2\,I_{E2}\frac{RR2}{RR3} = 2\frac{RR2}{RR3}\frac{1}{RR1}\frac{KT}{q}\ln\frac{A_{E1}}{A_{E2}} \quad \Rightarrow \qquad (7.37)$$

$$I_{REF} \approx 2\frac{1700}{920}\,135.2\,\mu A = 500\,\mu A \quad (T=25\,^{\circ}C)$$

The temperature coefficient of the reference current is found by taking the derivative of the above equation to find

$$\frac{dI_{REF}}{dT} = 2\frac{RR2}{RR3}\frac{1}{RR1}\frac{KT}{q}\ln\frac{A_{E1}}{A_{E2}} \quad \Rightarrow$$

$$TC(I_{REF}) = \frac{1}{R_{REF}}\frac{dI_{REF}}{dT} = \frac{1}{T} \qquad (8.38)$$

which is exactly equal to Equation (4.23); Therefore, the bandgap reference generates the bias currents necessary to maintain constant voltage gain over temperature. Also, approxiamatelly the same temperaure coefficient is used to maintain constant output logic levels.

CHAPTER 5

Experimental Results

5.1 Introduction

This chapter sumarizes the comparator performance obtained from the simulation and the experimental results. Once the circuit design was competed, the majority of the chip layout was done using a software tool called ICED (Graphics Editor for IC Design) written by IC Editors Inc..The hardware used was an IBM PC6386 compatible personal computer manufactured by AT&T. The ICED layout of the linear array was also provided by AT&T.

The layout task involved connecting the transistors and diffused resistors with top and bottom level metal. Also, the layout of the thin-film resistors was performed to comply with the laser beam tolerance requirements of most commercially available laser trimmers. The finishing layout details and connectivity verifications were performed in cooperation with the AT&T layout department (DES). In addition, the metal layout parasitics were extracted so that the final circuit simulations could be performed.

5.2. Simulation Results

Advice, the AT&T proprietary IC circuit simulator, was used to verify the comparator design. The Advice file that included the circuit description, the layout metal parasitics, and the package parasitics was used for simulations.

The schematic of the test circuit is shown in Figure 5.1. Resistors R_{SP}/R_{SN} and R_{TP}/R_{TN} simulate the 50 Ω source and termination impedances.

Resistors R_{E1}/R_{E2} are used for the pull-down of the ECL output (fourth gain) stage. An external voltage source V_T (-2V) provides the pull-down.

The circuit performance presented here is based on the nominall device models at room temperature. Worst-case simulations were also performed during the circuit design phase but are not included. The "room" junction temperature at which the simulations were performed was found from

$$T_{J(room)} = T_{room} + P_D \Theta_{JA} = T_{room} + (I_{CC} V_{CC} + I_{EE} V_{EE} + I_T V_T) \Theta_{JA} \qquad (5.1)$$

$$T_{J(room)} \approx 17 + (87.2 + 160.1 + 52.6)\, 10^{-3}\, 100\ ^\circ C = 47.0\ ^\circ C$$

5.2.1 Simulated DC Performance

Since the circuit is balanced, the nominal input offset voltage and offset current are zero. The typical values of the DC parameters simulated are shown below on Table 5.1.

TABLE 5.1

Simulated DC parameter values

Parameter	Value	Units
Pos. Supply Current, I_{CC}	17.43	mA
Neg. Supply Current, I_{EE}	32.01	mA
Input Bias Current, I_B	3.773	µA
Power Dissipation, P_D	247	mW
Output Digital High, V_{OH}	-0.942	V
Output Digital Low, V_{OL}	-1.742	V
Voltage Gain, A_V	6,400 (76.1)	V/V (dB)

Figure 5.2 shows the transfer function of each of the digital outputs and Figure 5.3 shows the differential output versus the differential input. It is evident that the DC gain is high enough to reduce the uncertainty window under 1 mV.

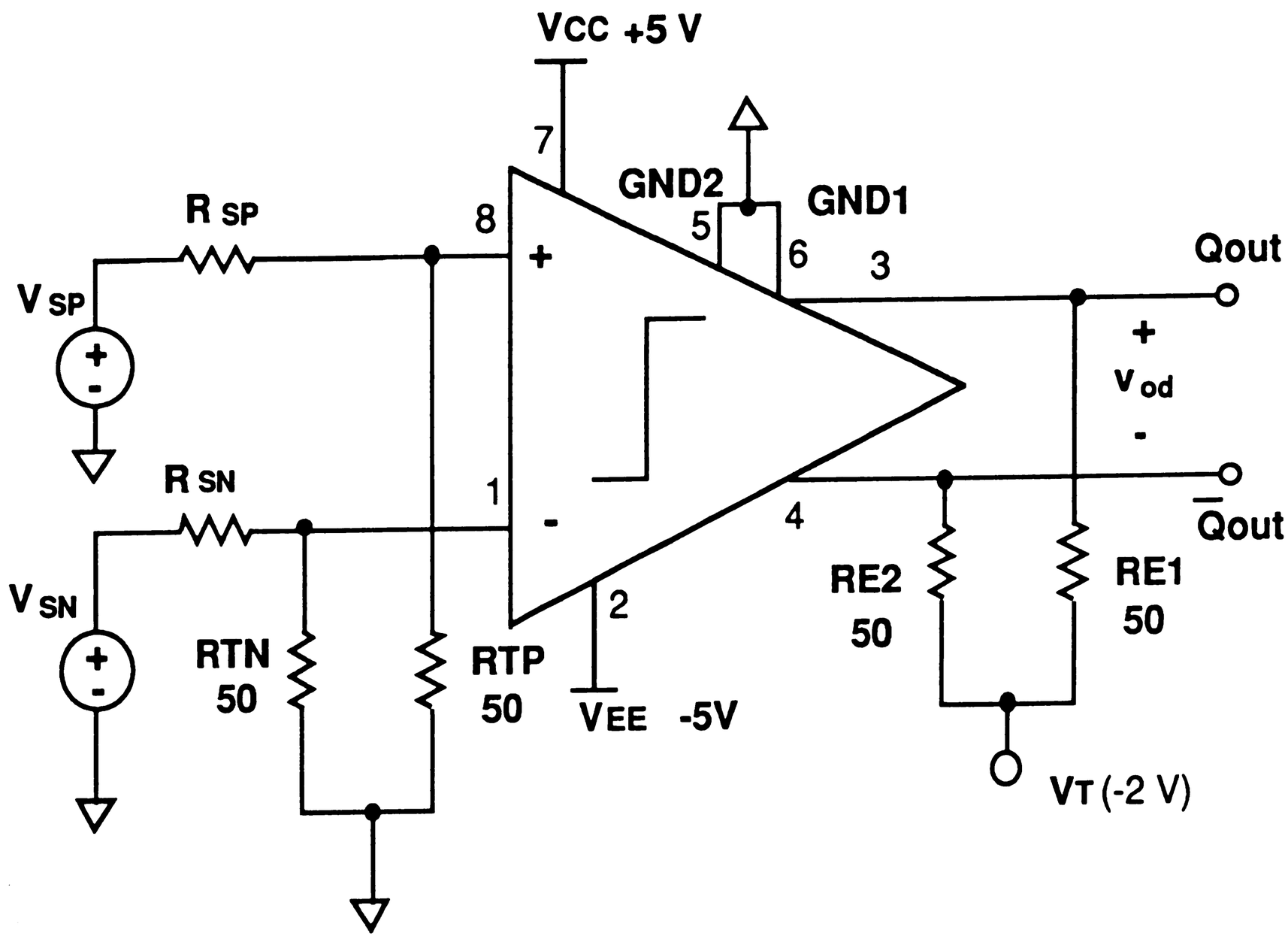


Figure 5.1. Comparator test circuit schematic diagram

It is important that the output digital voltage level remain constant with variations of temperature. Figures 5.4 and 5.5 show the variation of the digital output levels with temperature. Even under the worst-case military temperature range (-55 °C to 125 °C ambient) the digital outputs remain within the window of compatibility with the F100K ECL logic requirements.

5.2.2 Simulated AC and Transient Response

The AC frequency response of the comparator in the linear region is shown in Figure 5.6. Also shown are the AC characteristics of the intermediate stages.The overall bandwidth of the comparator appears to be dominated by the response of the output stage. This is due to the requirement that the output swing is set by the digital logic levels. Large swing necesitates large gain setting resistor values and therefore large RC time constants. Of course, since the output stage never operates in the linear region, the bandwidth is not directly indicative of the comparator response.

The transient response of the four gain stages to a ±100 mV input signal V_{ID1} is shown in Figure 5.7. Also, the digital output level transient response is shown in Figure 5.8. The total propagation delay τ_D is found to be 2.20 ns. Therefore, the maximum frequency that the comparator can be operated is given by the ring oscillator frequency given by

$$f_{max} = \frac{1}{2\,\tau_D} = \frac{1}{2\,(2.20\text{ ns})} = 227\text{ MHz} \qquad (5.2)$$

The transient performance of each gain stage and the overall comparator is summarized on Table 5.2 below.

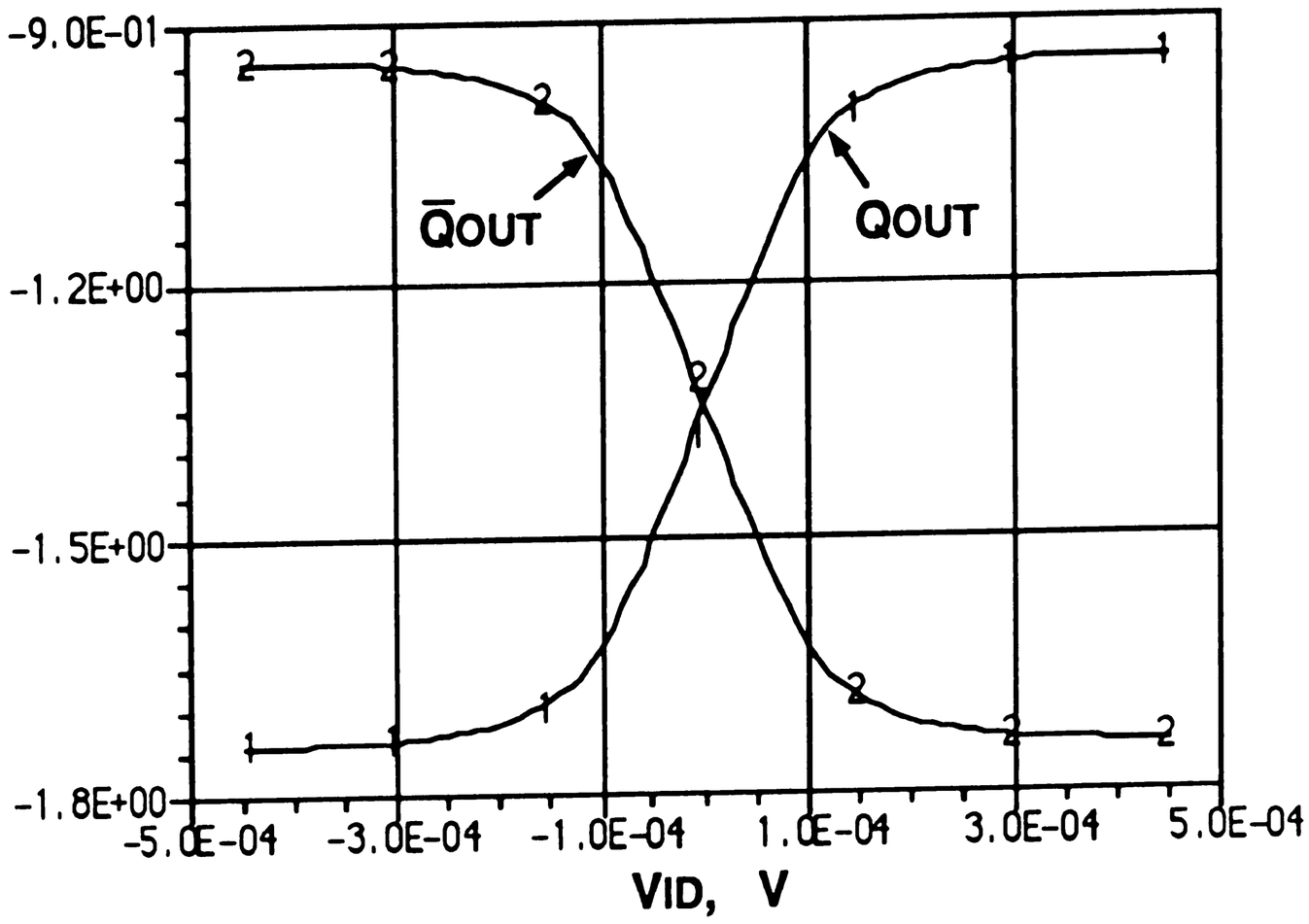


Figure 5.2. Digital output levels vs differential input

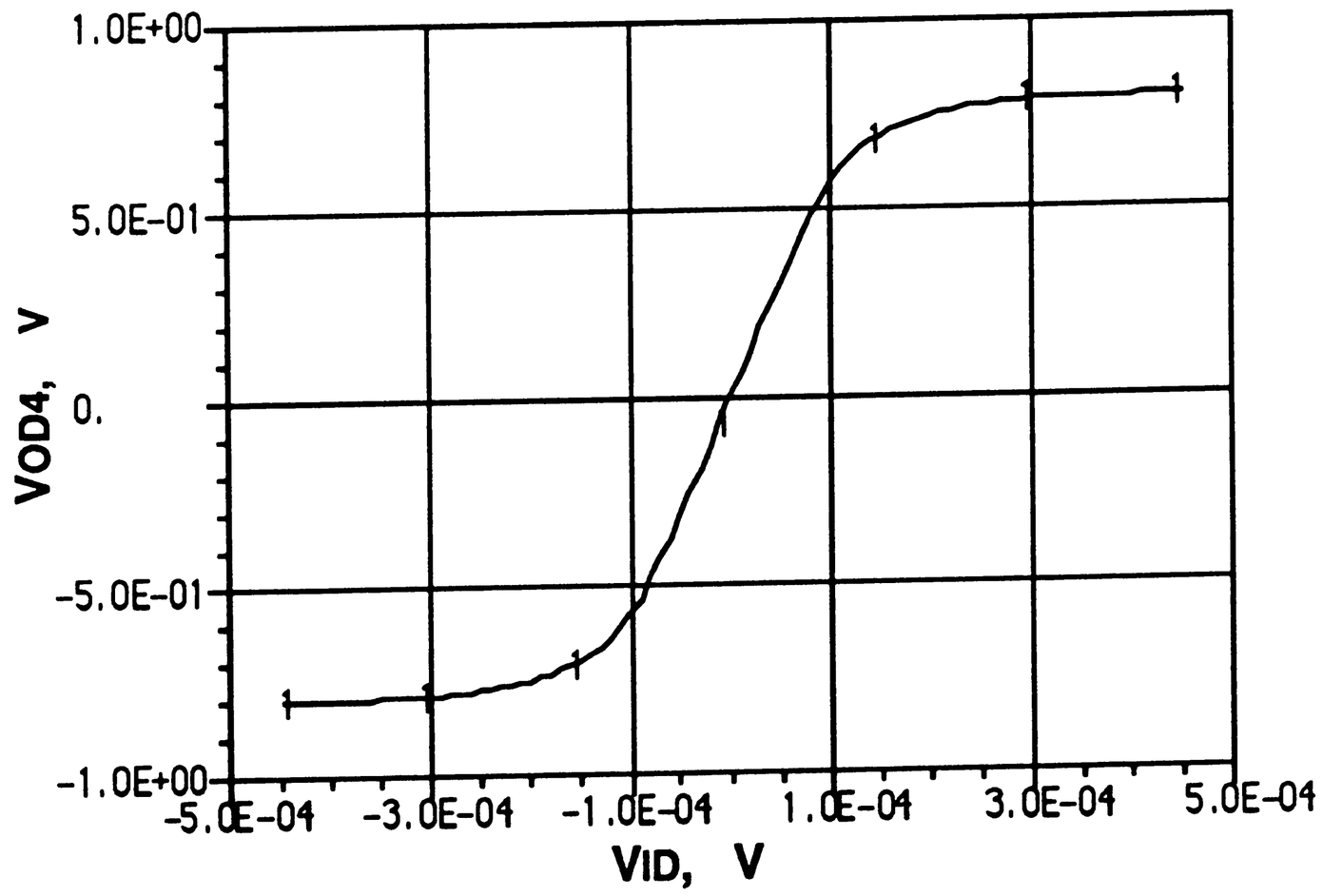


Figure 5.3. Differential output vs differential input

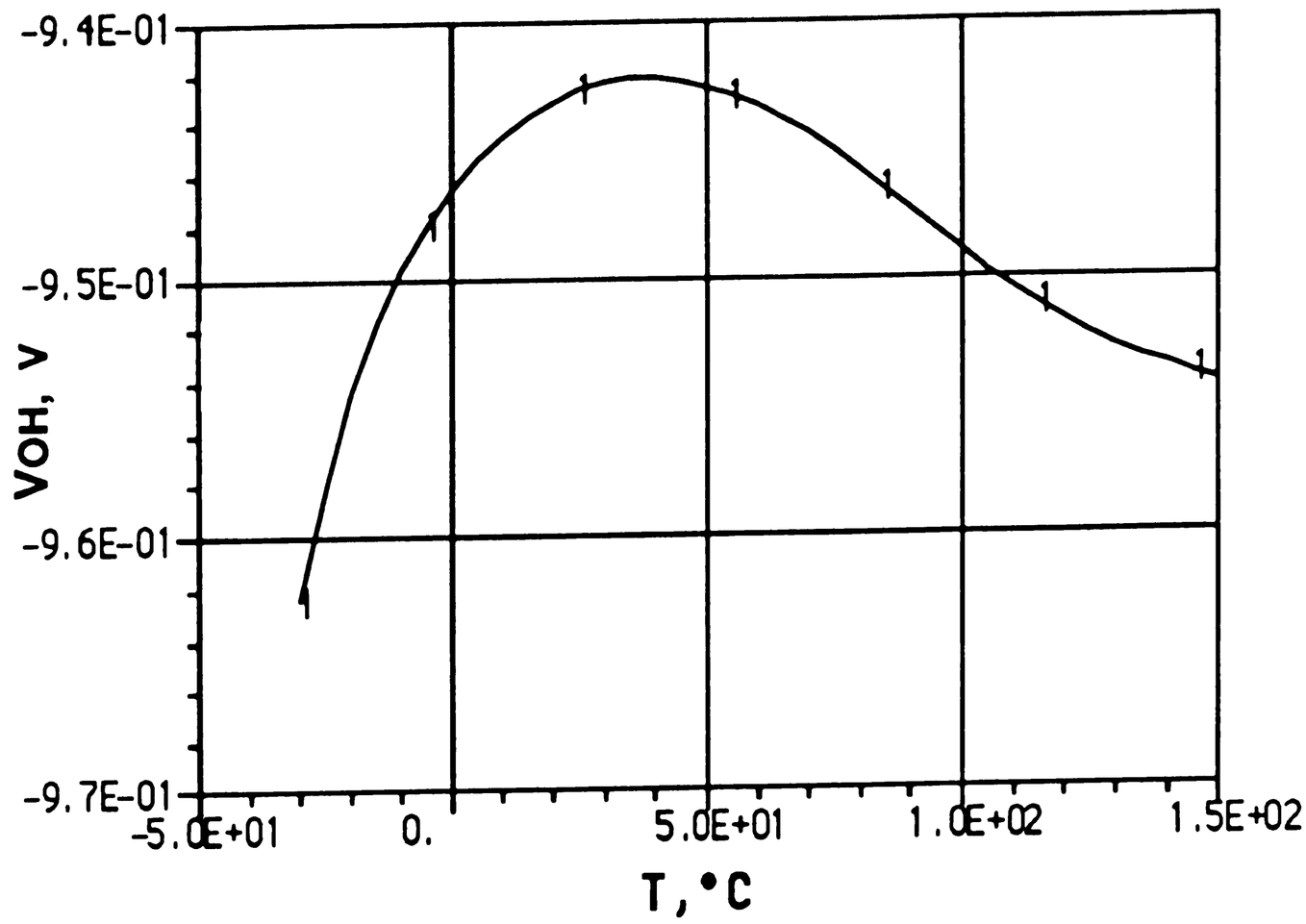


Figure 5.4. Digital "High" voltage level vs temperature

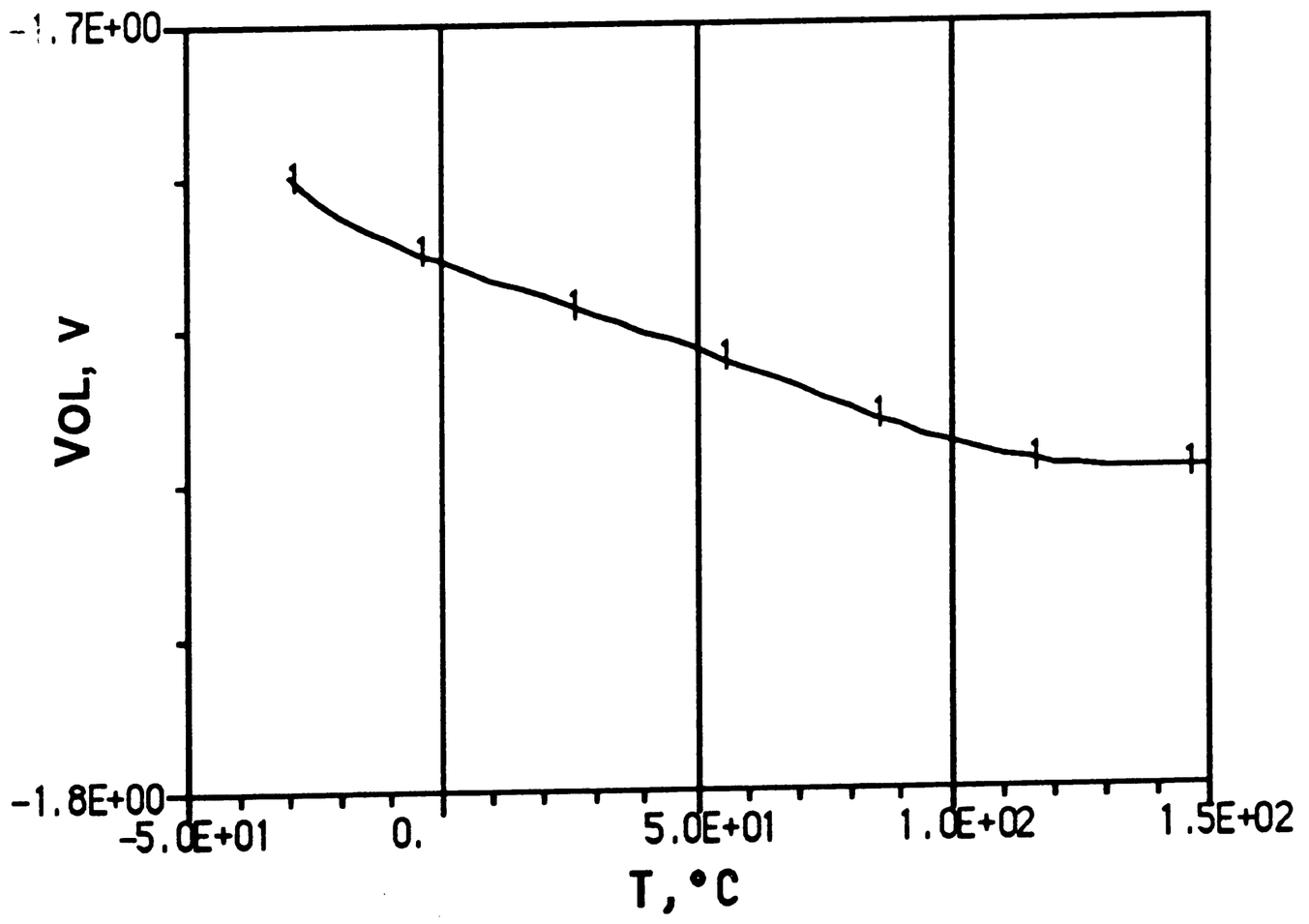


Figure 5.5. Digital "Low" voltage level vs temperature

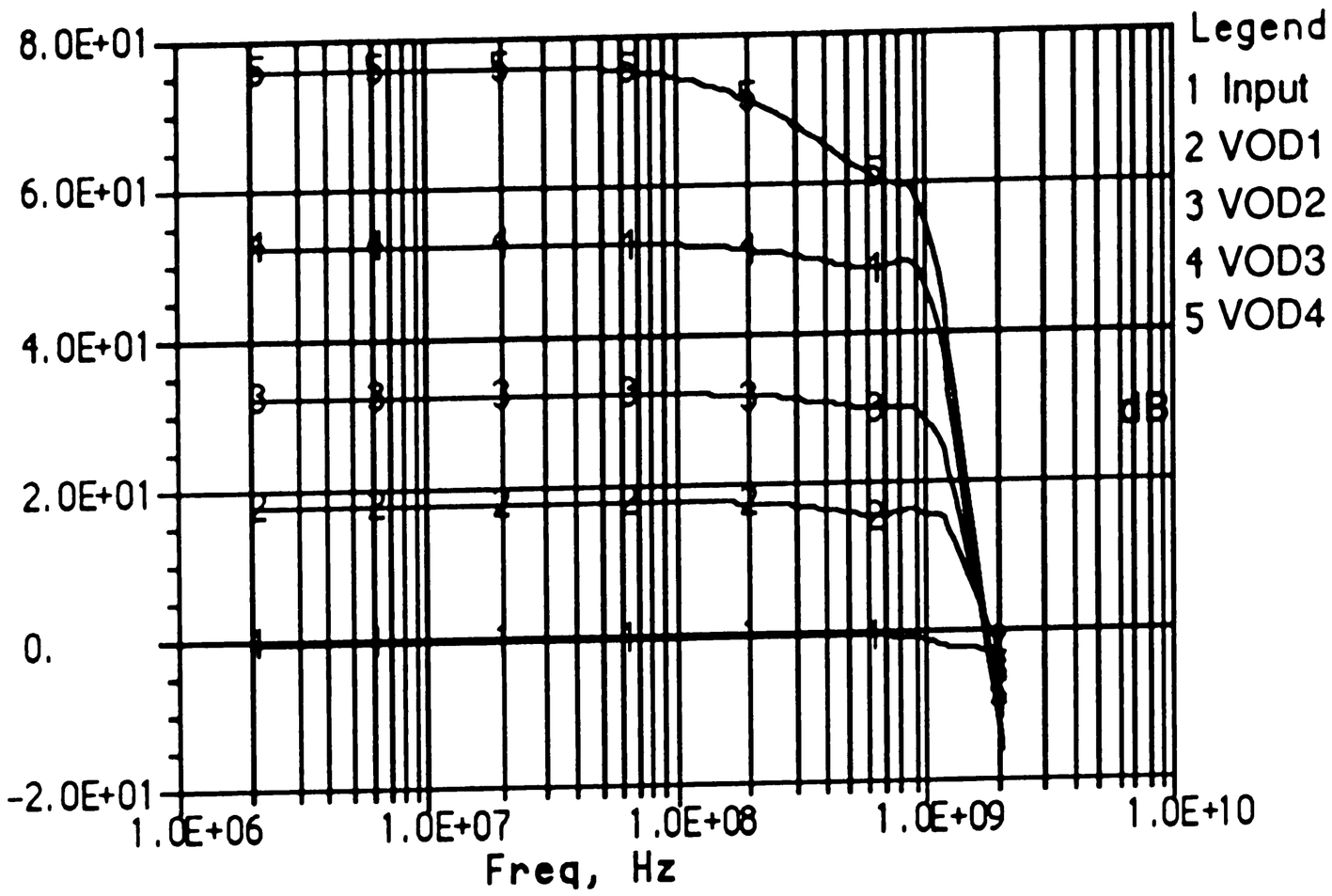


Figure 5.6. AC frequency response

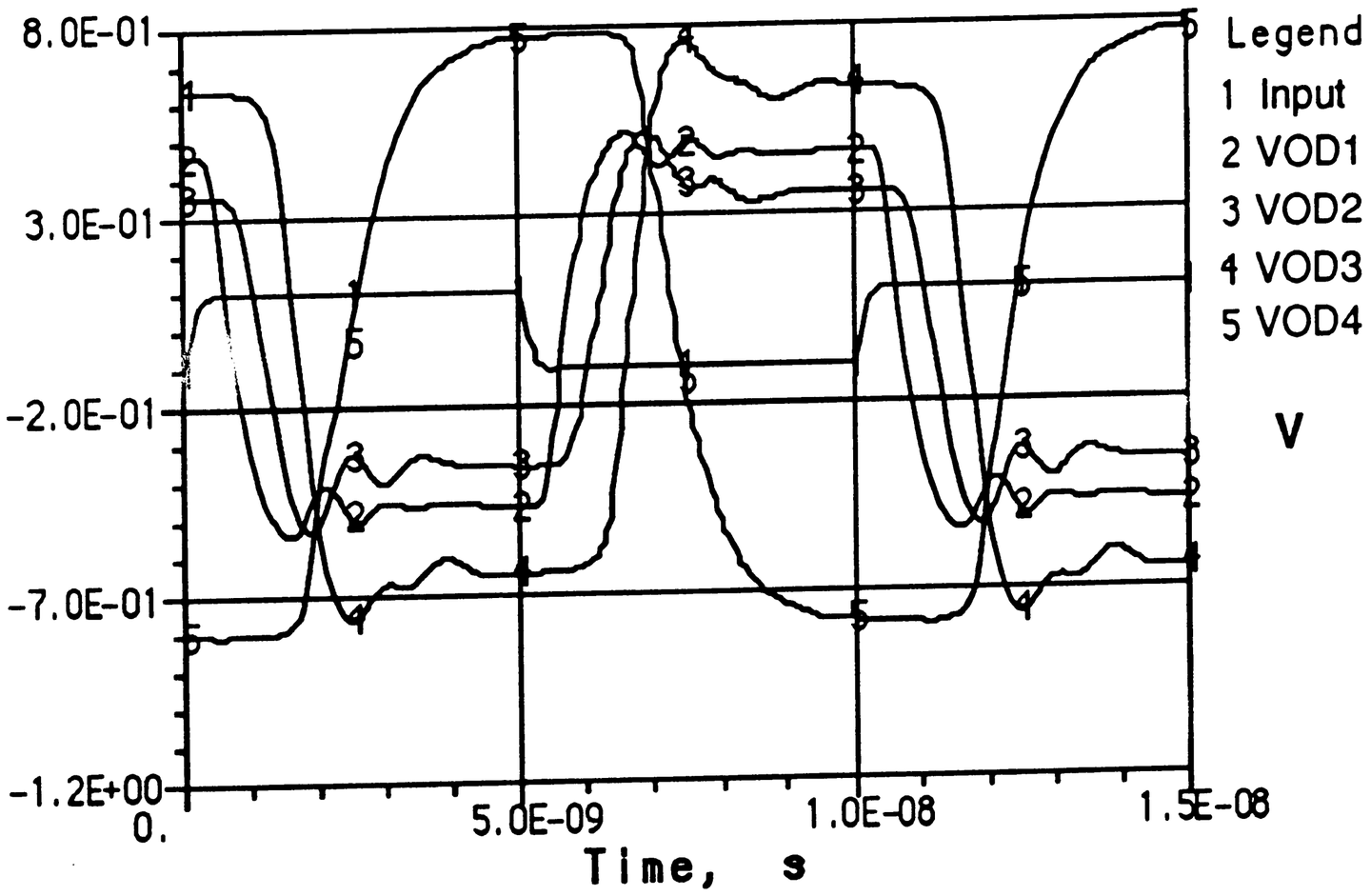


Figure 5.7. Transient response

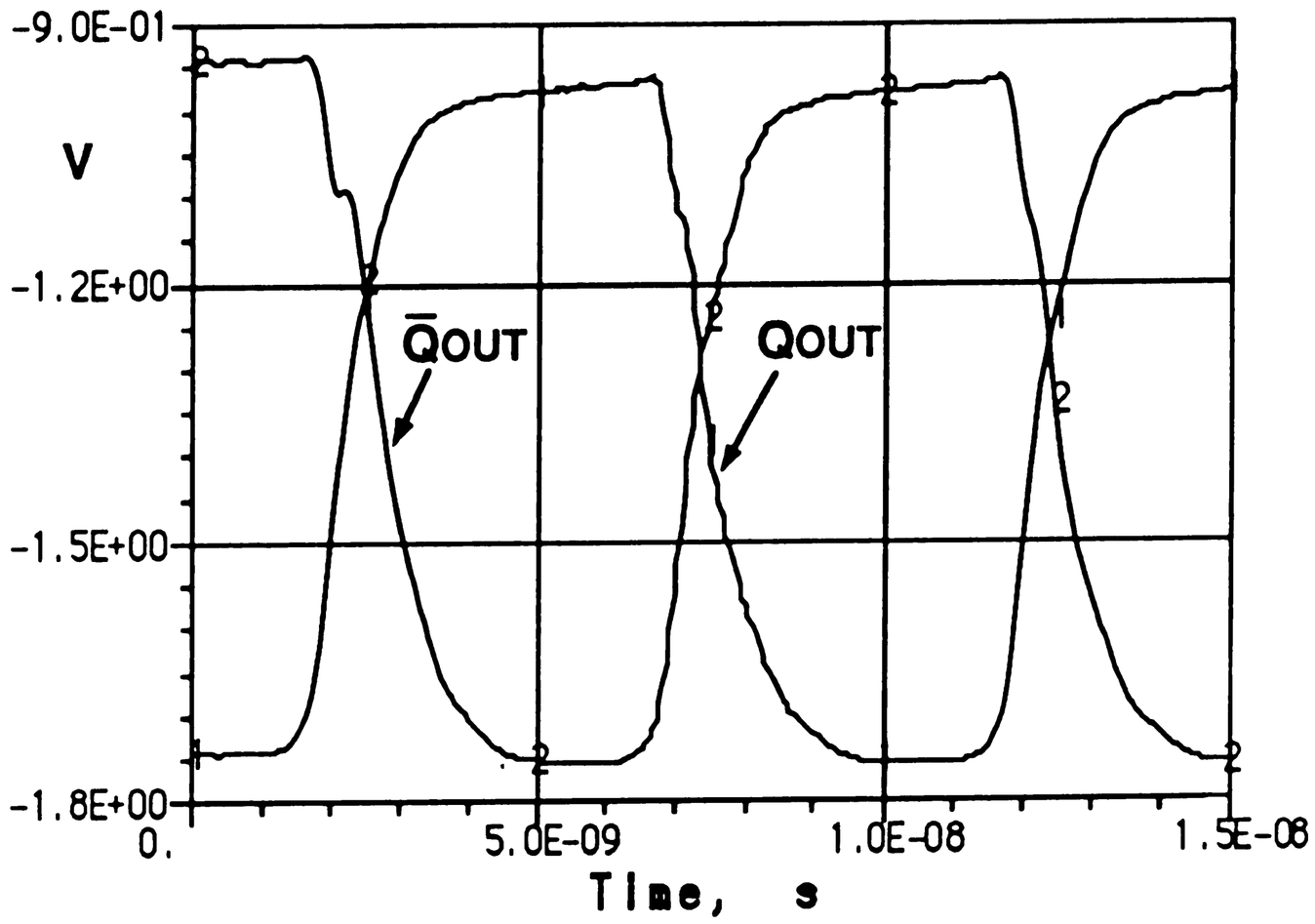


Figure 5.8. Output digital level time response

Table 5.2

Comparator transient performance results

Parameter	1st Stage	2nd Stage	3rd Stage	4th Stage	Total	Units
AC Gain, A_V	18.0	14.4	20.0	23.7	76.1	dB
Propagation Delay, t_D	550	450	500	700	2,200	ps
f_{max}	910	1,110	1,000	710	230	MHz

5.3. Experimental Results

The mask generation and the wafer fabrication were both performed by AT&T Microelectronics (Reading, Pennsylvania) using their standard CBIC-U linear array processing. Two finished wafers were provided. One wafer included a low temperature deposited Silicon Oxide and Silicon Nitride film sandwich to protect against scratching and humidity, while the second wafer did not.

The second wafer was used to verify the circuit functionality by probing not only the probe pads but also the top level metal in verious parts of the circuit. Once the electrical results were found to be satisfactory, twenty chips were chosen in random from the wafer with the protection film and were packaged in 8-pin sidebrazed ceramic packages.

5.3.1 DC Performance

A printed-circuit board was constructed with two copper metal planes with the same electrical connections as shown in Figure 5.1. The supply currents and the digital output levels were measured while a large (about 100 mV) differential input voltage was applied.

All the available units were tested. The distribution of the supply current values are shown in Figures 5.9 and 5.10. The distribution of the digital levels are shown in Figures 5.11 and 5.12. All the values are agree with the predictions. The values of the supply currents are slightly on the positive side. The distribution of the digital levels is tight. enough to meet the logic compatibility requiremets under worst case.

Figures 5.13 through 5.18 show the supply current and digital levels variation with positive and negative power supply. It is shown that the positive supply can be reduced to as much as 1V while the negative supply can be reduced to about 3.5V. The larger negative supply current variation with V_{EE} is due to the current through the resistors that bias the output emitter followers of the third stage.

Figure 5.19 shows the output logic level variation with the total supply voltage value. The total supply voltage can be reduced to as much as 4.5 V and still maintain functionality. The objective of being able to operate the comparator with a large supply voltage range has therefore being achieved.

Figure 5.20 the variation of the digital levels with the pulled-down voltage V_T. For small values of V_T there is not enough bias current to drive the output emitter followers "low" and, therefore, the voltage error of V_{OL} is larger than that of V_{OH}.

The measurement of the voltage gain, offset voltage, input bias, and offset currents requires the comparator to operate in the linear region. Attempts to force the comparator to work in the linear region have failed. It has been observed that when the differential voltage across the inputs is less than about ±10 mV (as low as 4 mV has been achieved) the comparator starts oscillating at at a frequency of about 900 MHz that makes the DC parameter measurement impossible.

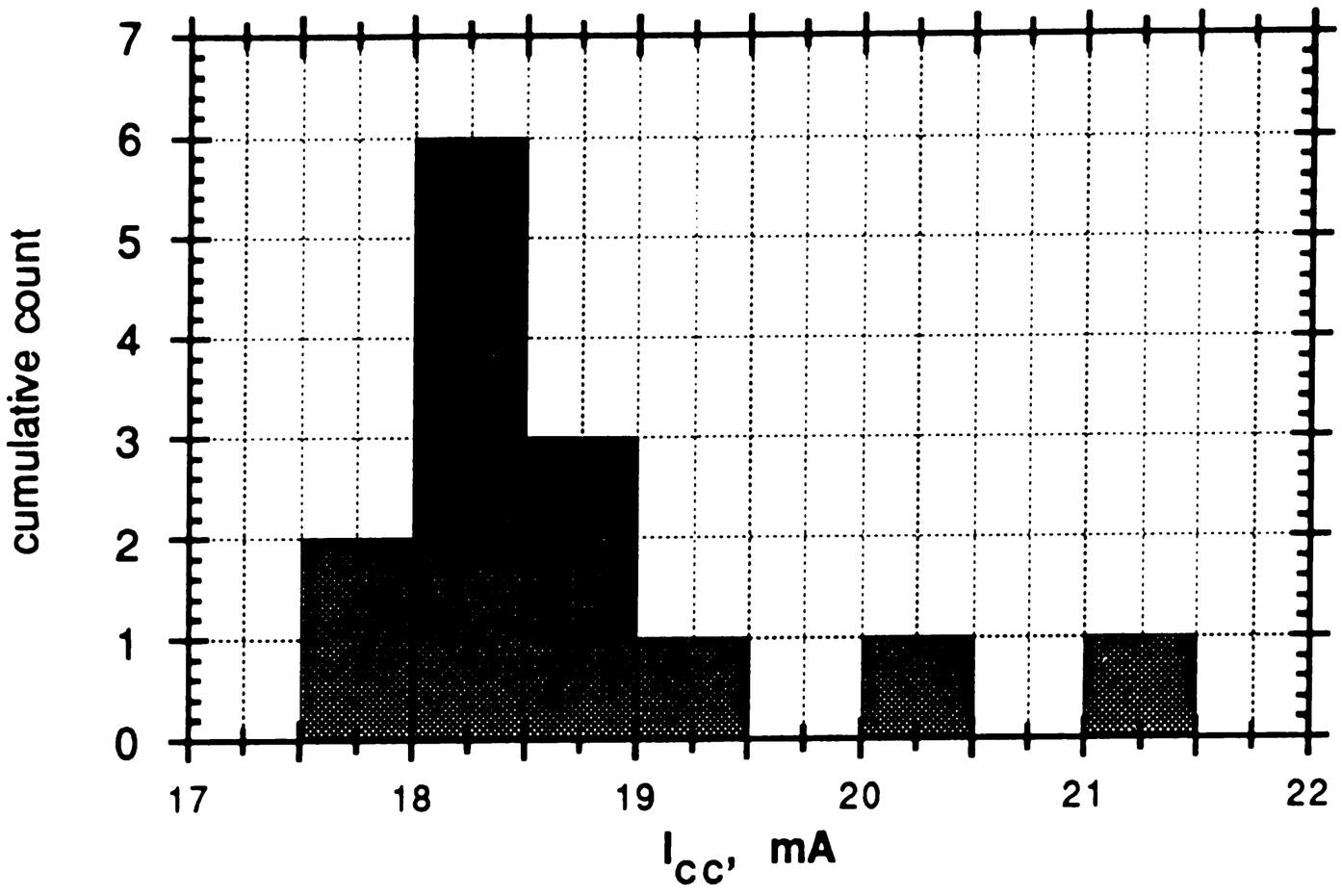


Figure 5.9. Positive supply current distribution

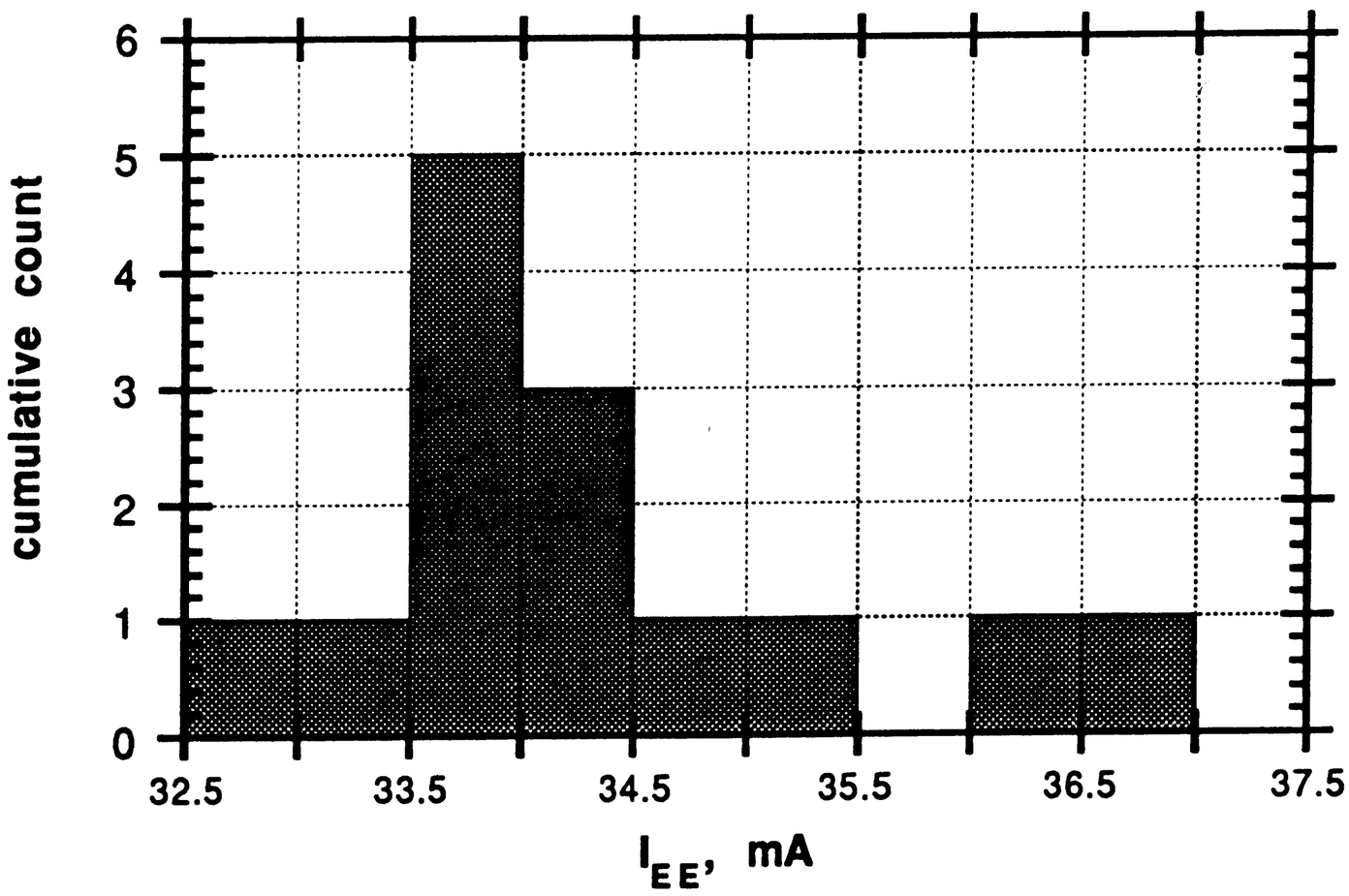


Figure 5.10. Negative supply current distribution

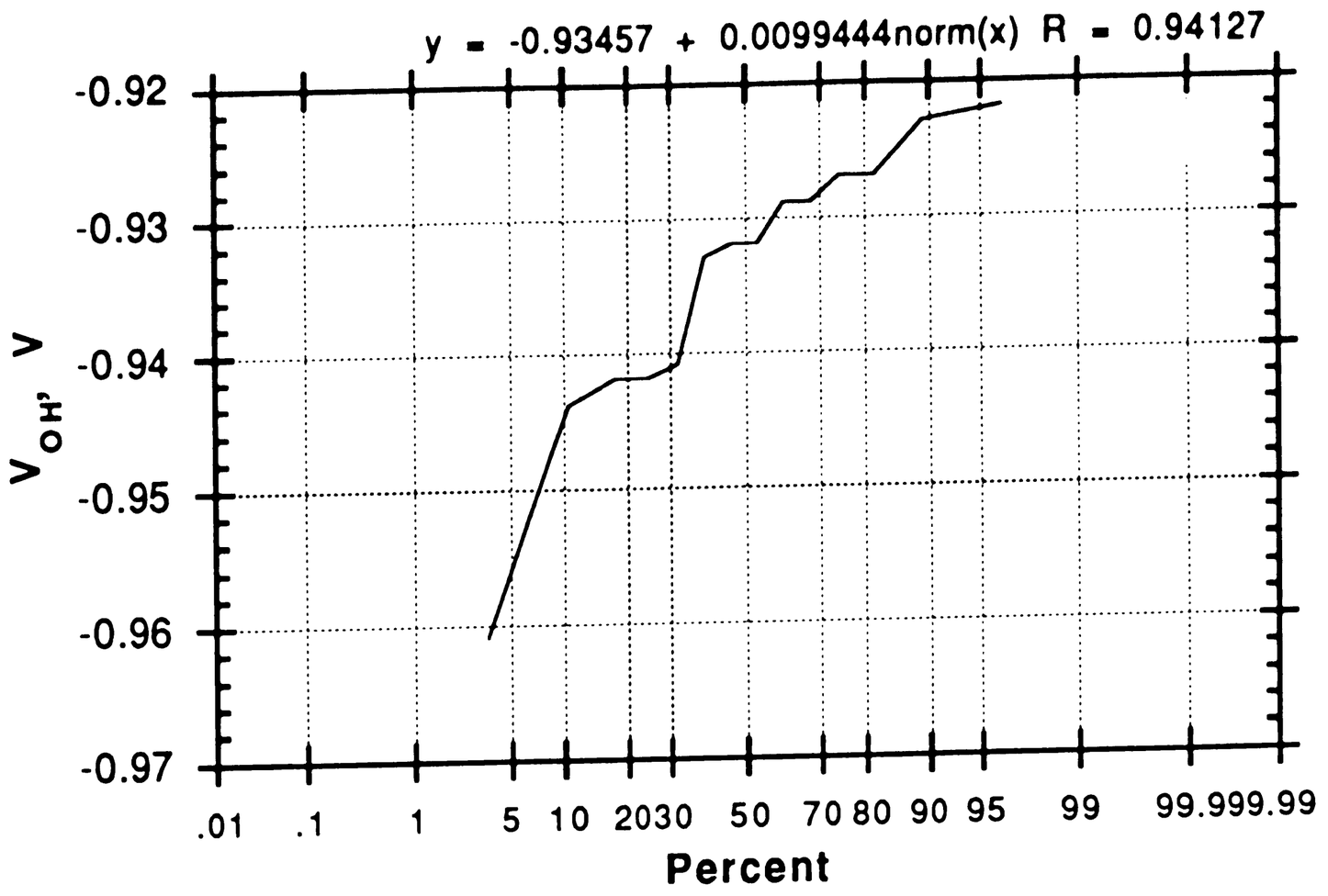


Figure 5.11. Digital "High" voltage level distribution

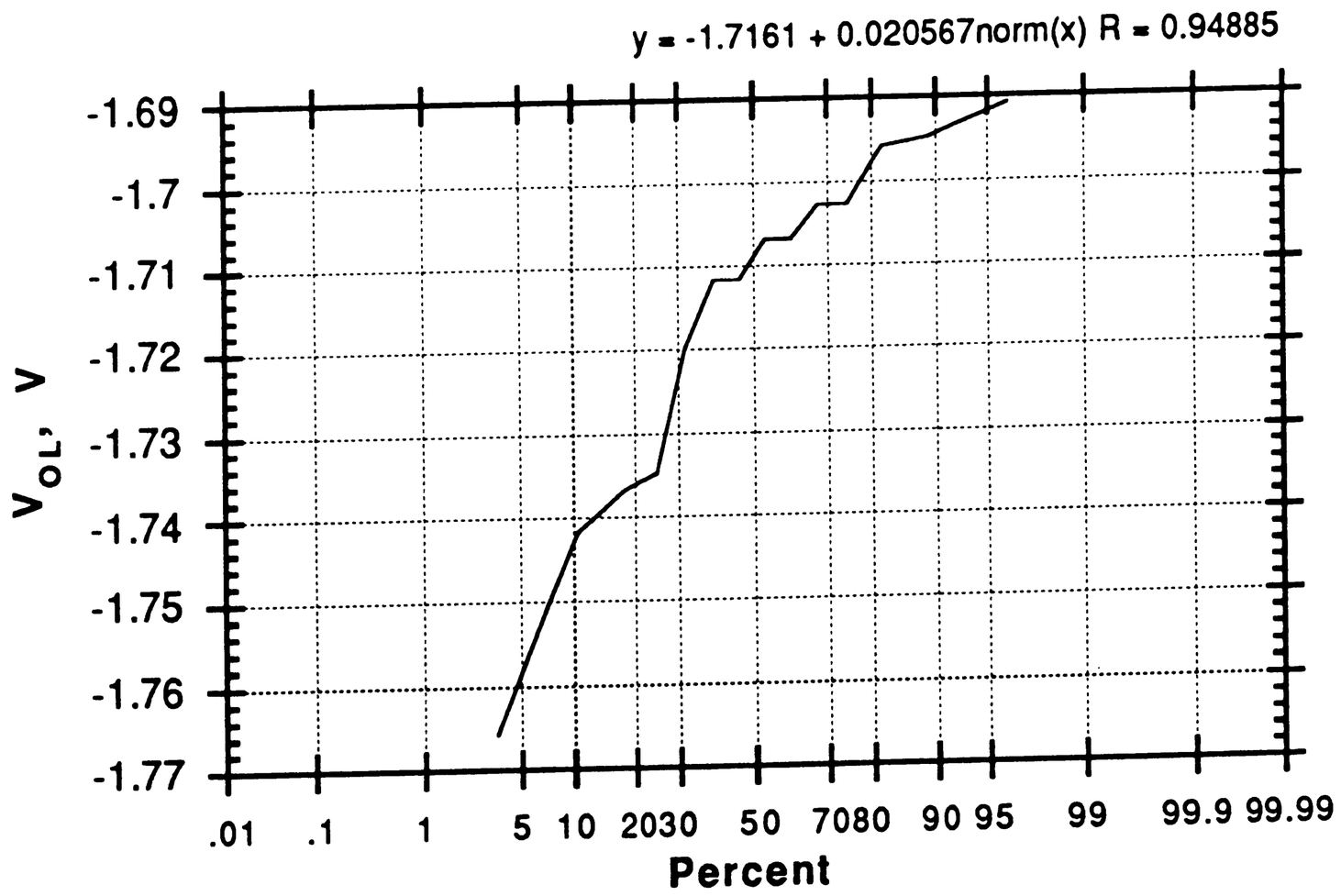


Figure 5.12. Digital "Low" voltage level distribution

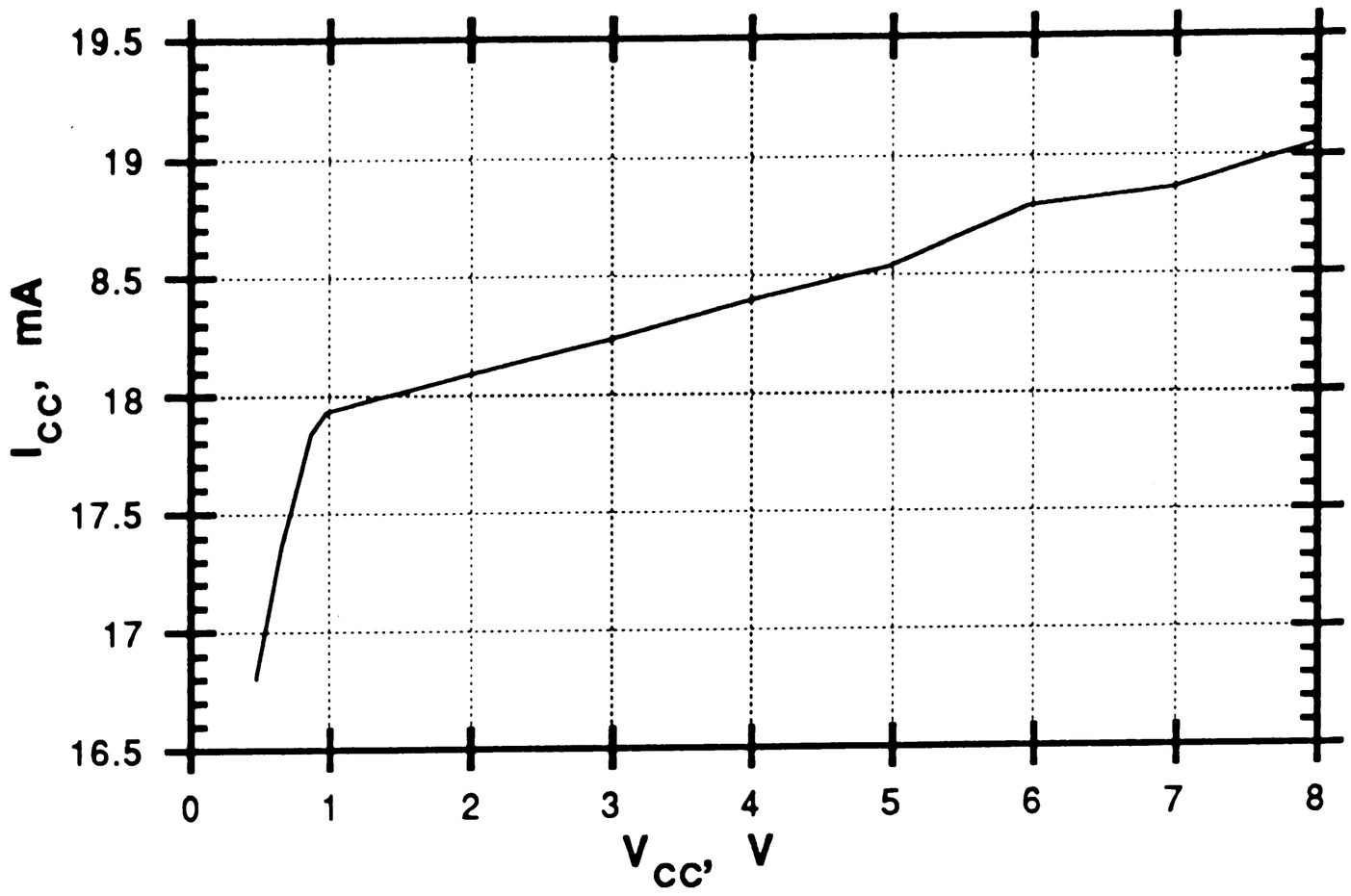


Figure 5.13. Positive supply Current vs positive supply voltage

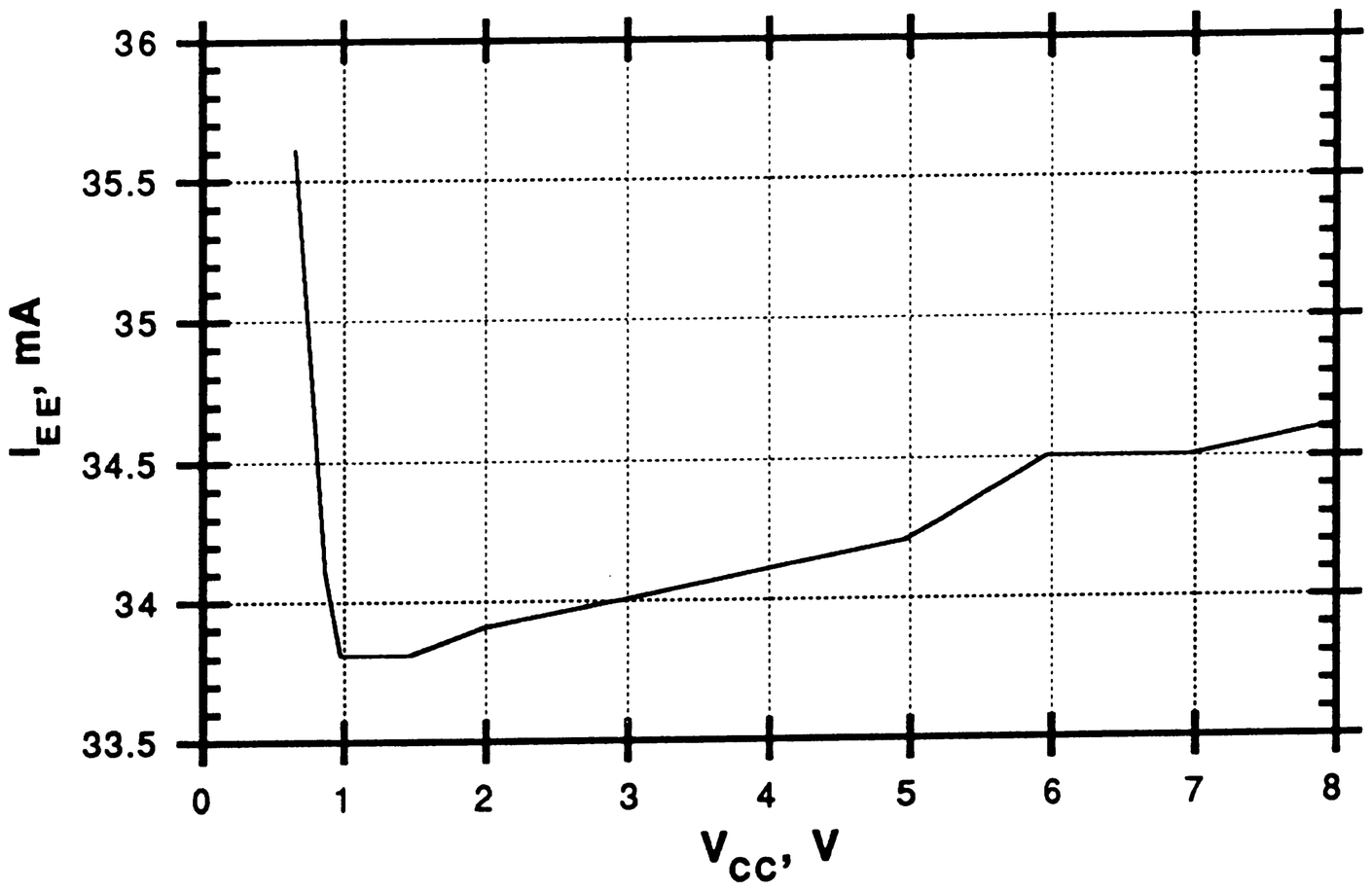


Figure 5.14. Negative supply current vs positive supply voltage

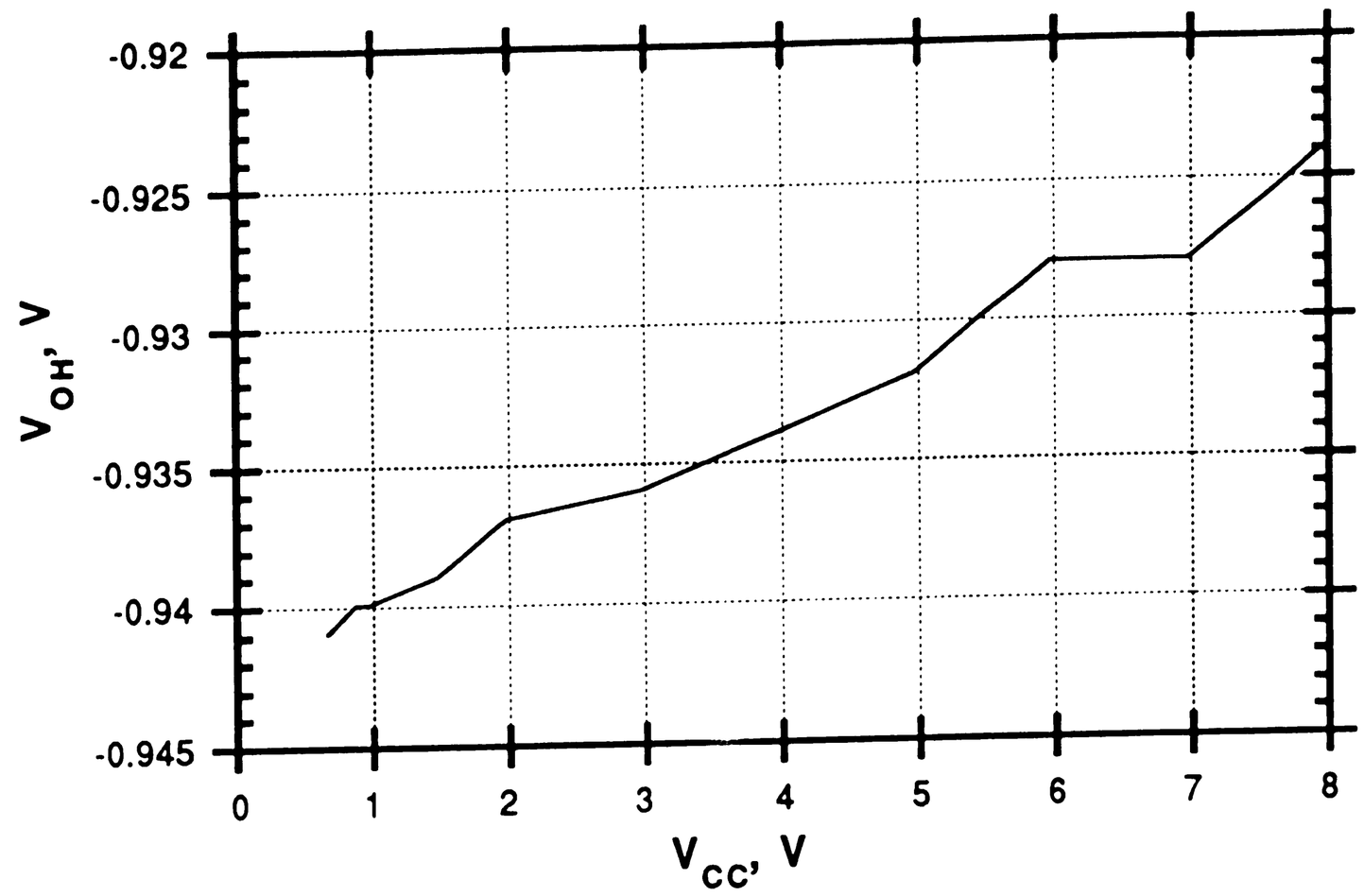


Figure 5.15. Digital "High" voltage level vs positive supply voltage

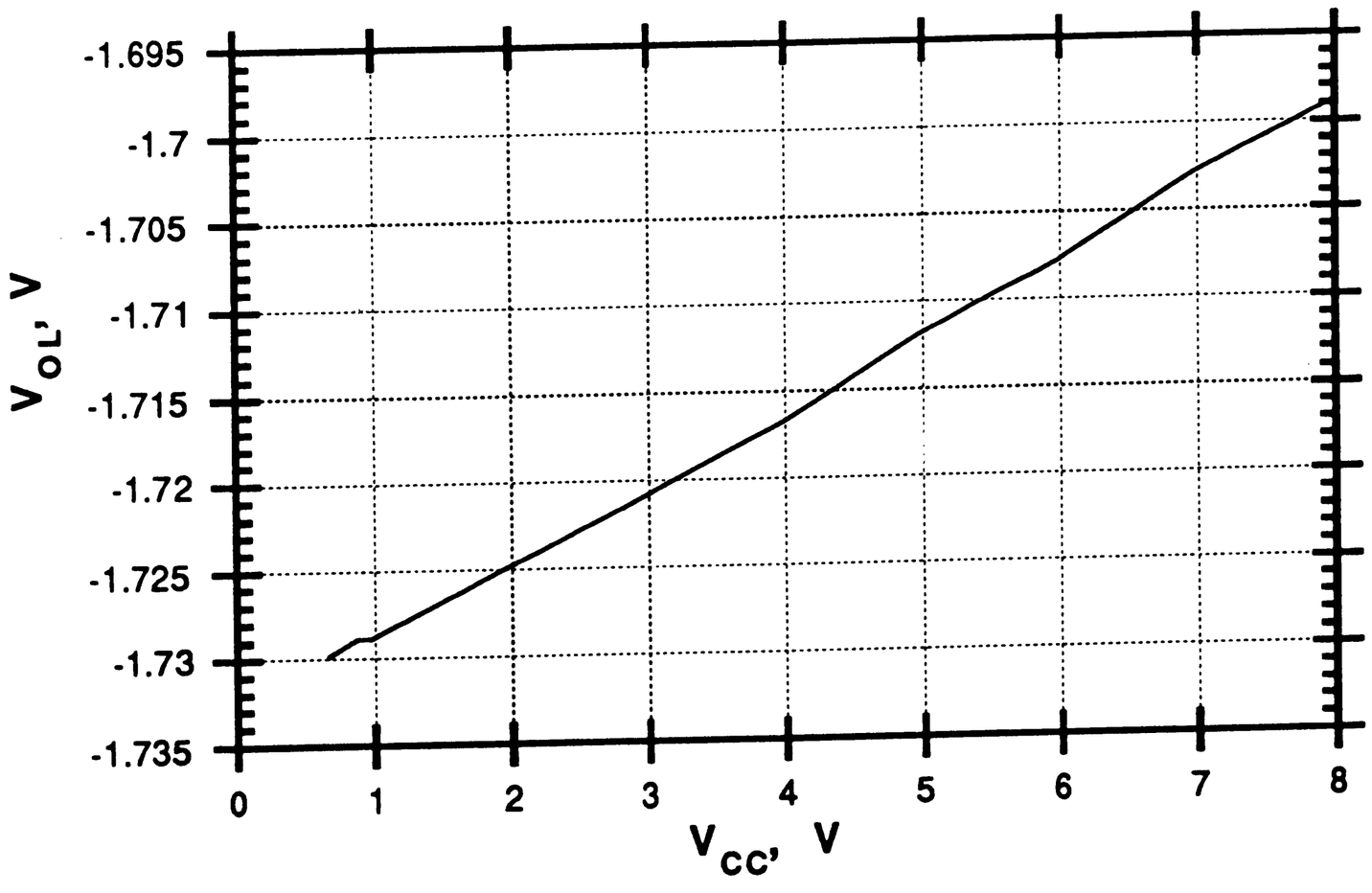


Figure 5.16. Digital "Low" voltage level vs positive supply voltage

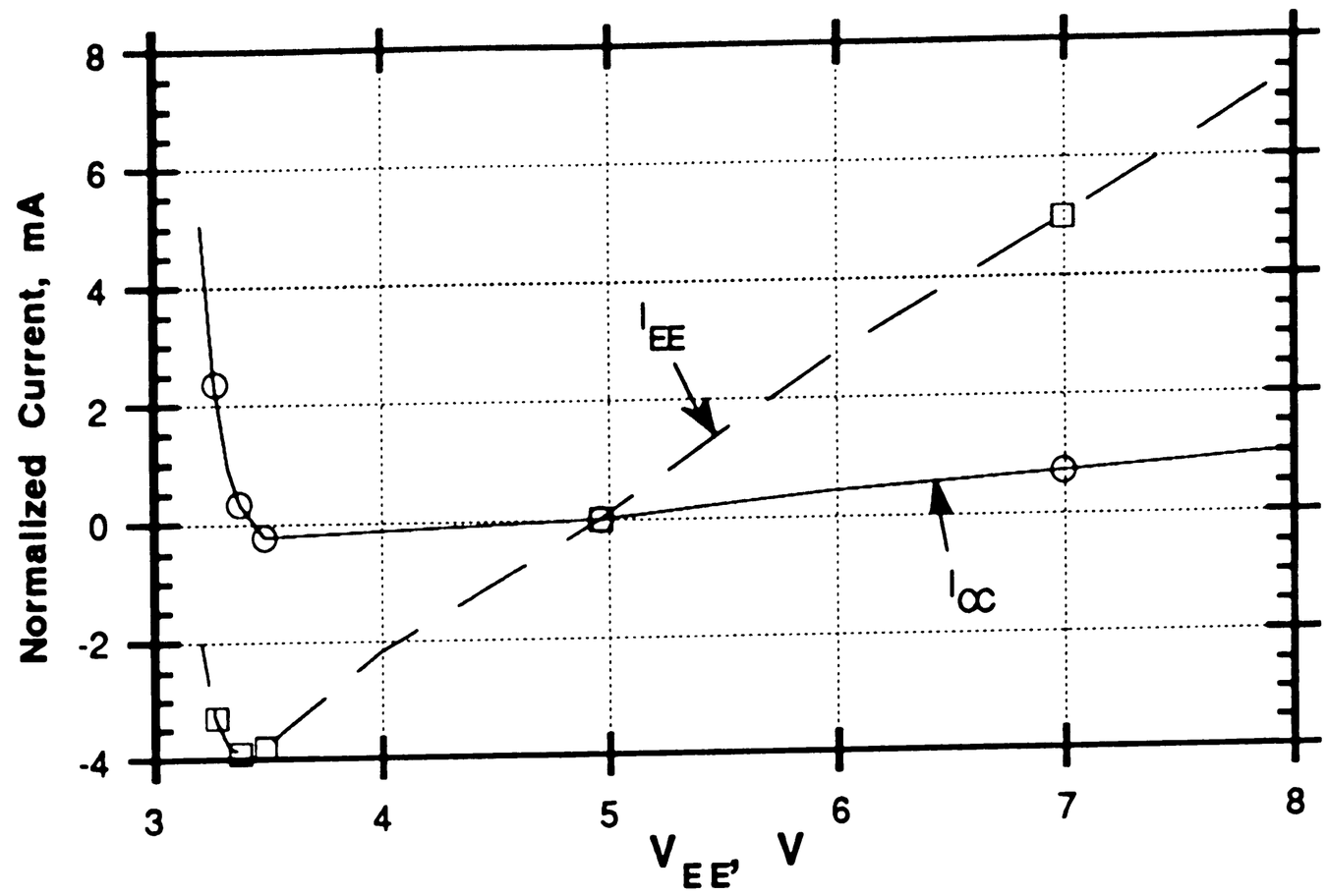


Figure 5.17. Normalized supply current vs negative supply voltage

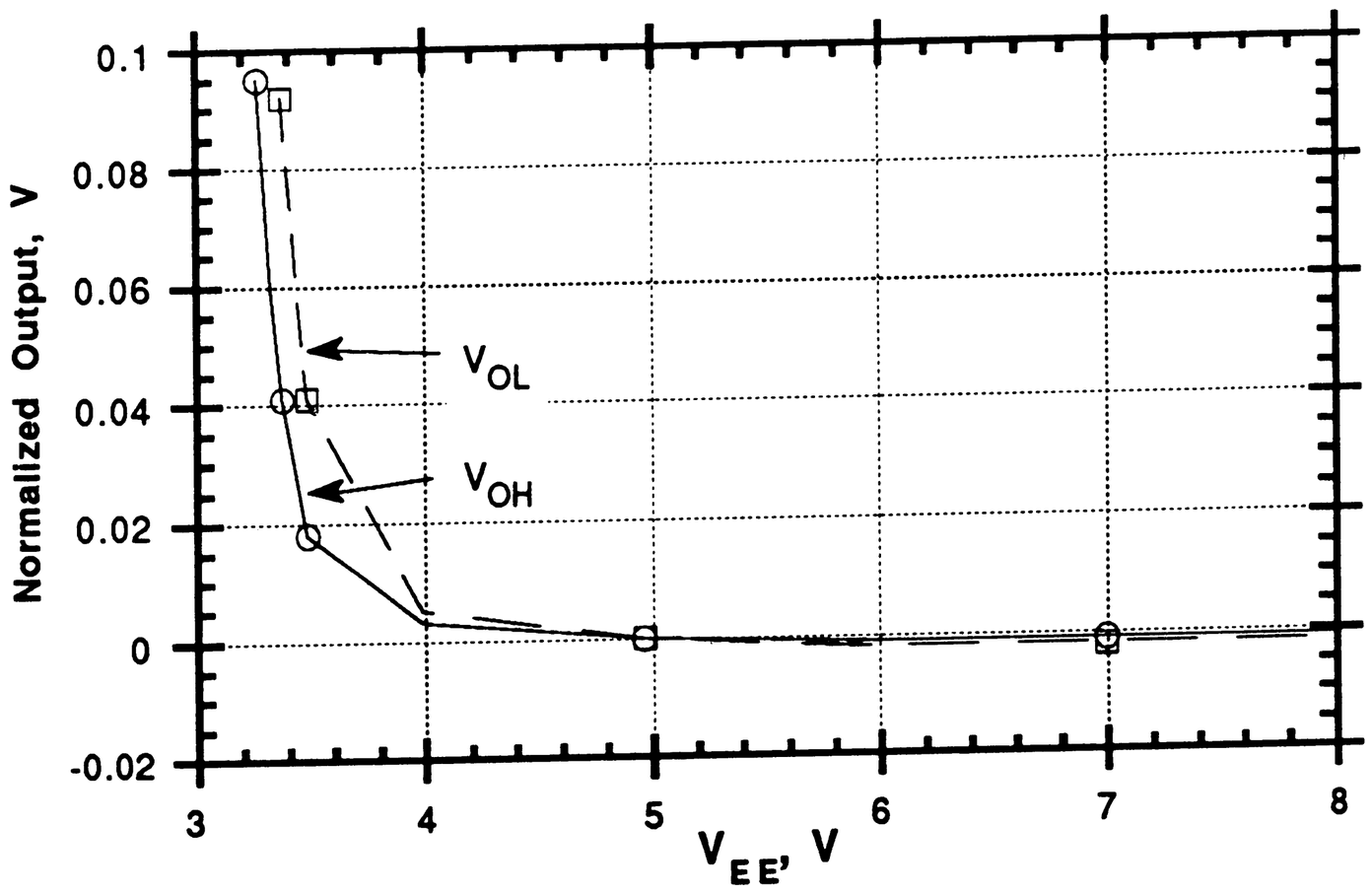


Figure 5.18. Output logic levels vs negative supply voltage

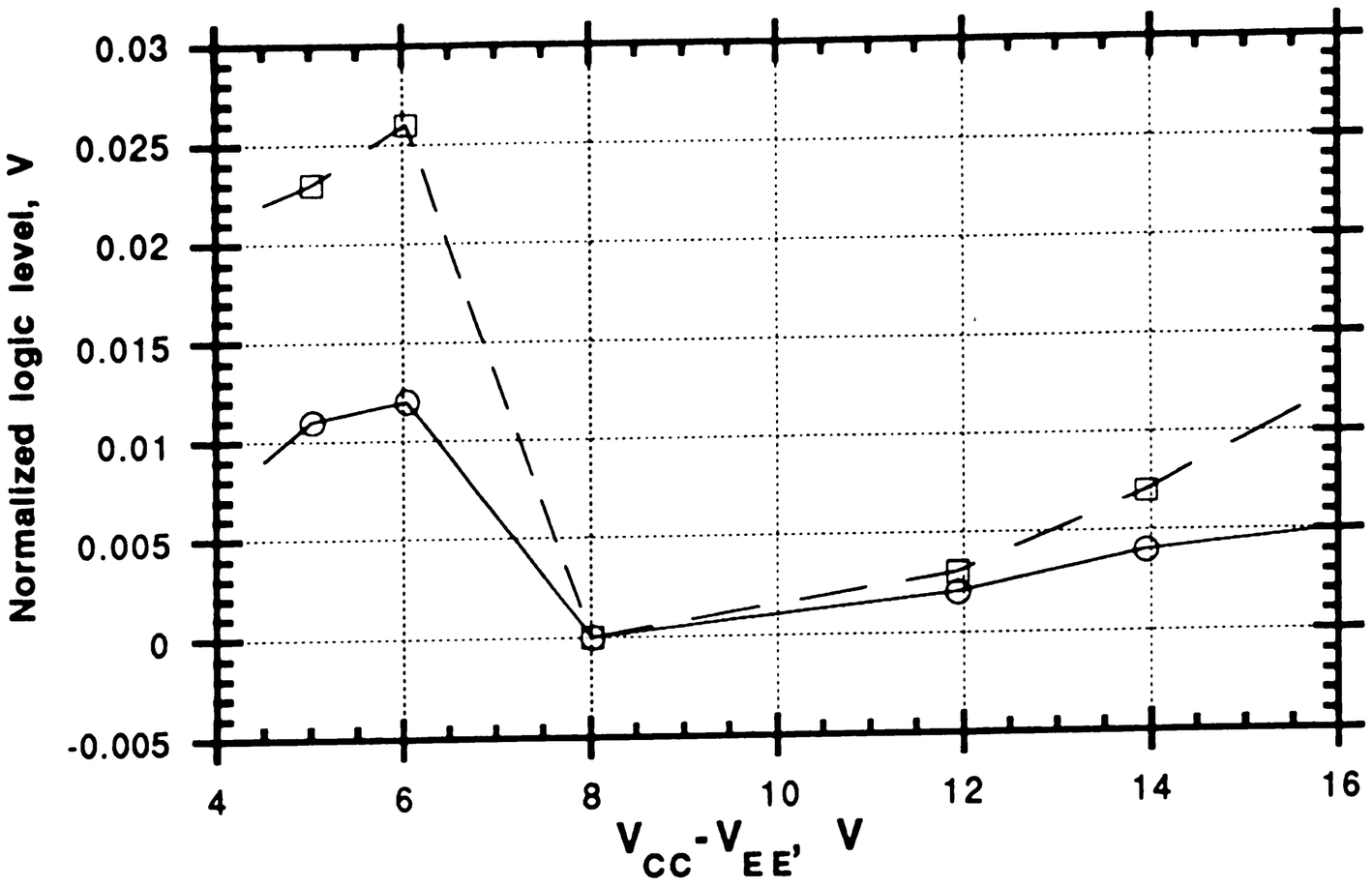


Figure 5.19. Output logic levels vs total power supply voltage

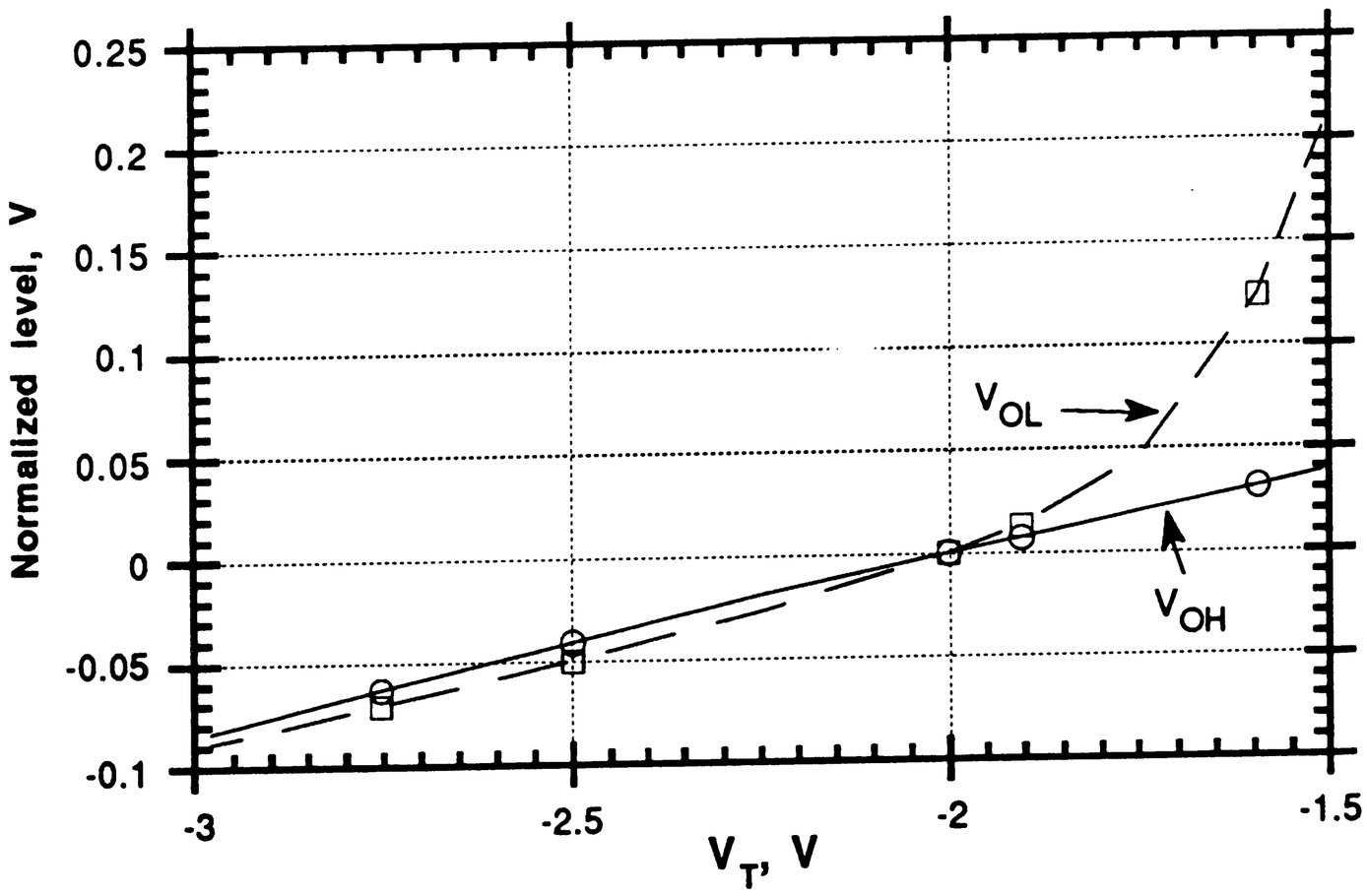


Figure 5.20. Output logic levels vs pull-down voltage V_T

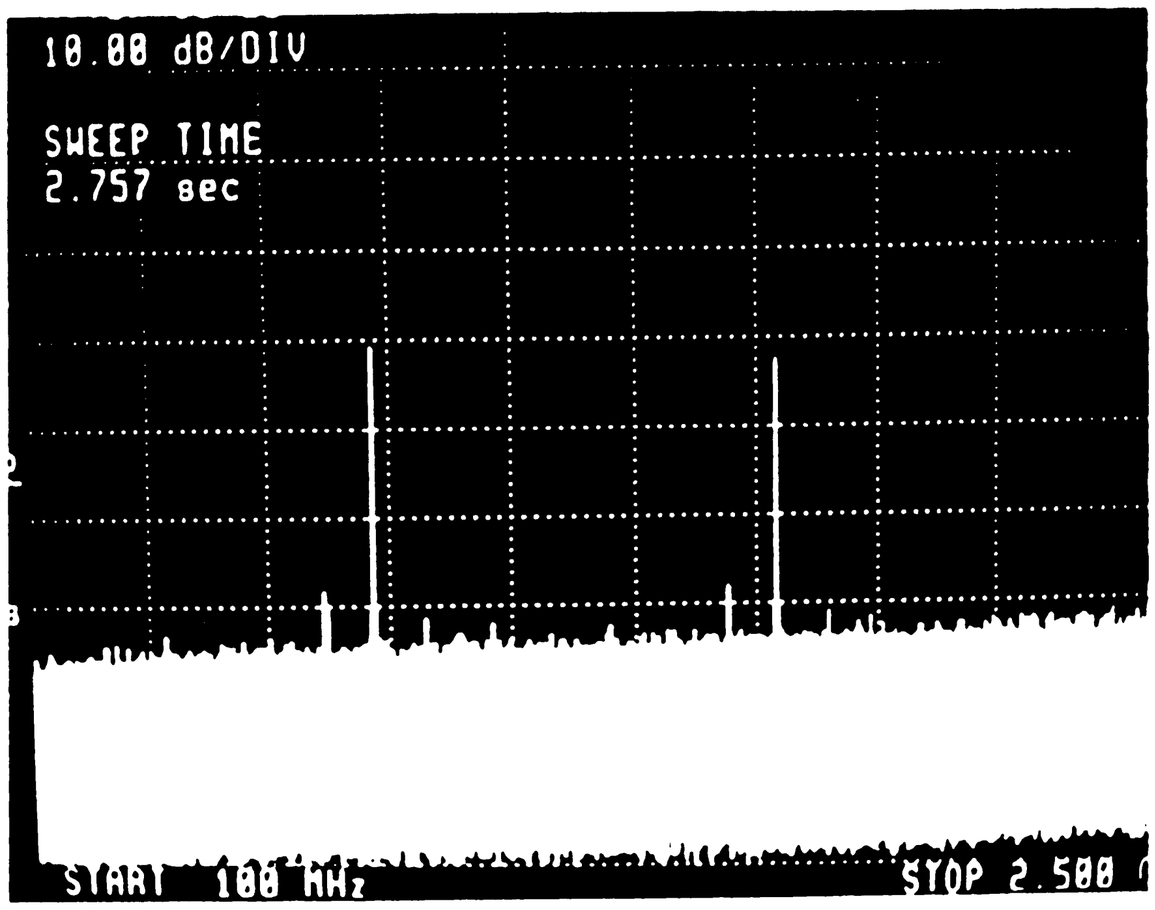


Figure 5.21. Comparator oscillation displayed on a spectrum analyzer

Figure 5.21 is a picture of a spectrum analyzer showing the resonance exhibited by the comparator in the linear region. The oscillation is detected using an RF coil at one end of a coaxial cable connected to the spectrum analyzer. The same oscillation was detected by circuit probing. The oscillation goes away when the differential input voltage is greater than about ±10 mV. This value tends to be a strong function of the particular test set-up used.

It has been possible to measure the comparator input bias current I_B, and input offset current I_{OS} indirectly. A relatively large differential input voltage was applied (about 480 mV) first such that it forced the comparator to go into the non-linear region in which it is stable. With a positive input signal polarity, the current flowing into the positive input terminal was measured. Then the input signal polarity was reversed and the current going into the negative input terminal was measured.

This technique uses the fact that the collector current of each of the input transistors in the linear region is half the value when the circuit operates in the non-linear region. It is assummed that the transistor current gain and its

mismatch does not change appreciably with changing current density. At worse, since the transistor current gain is reduced with current density, the measured experimental results are pessimistic. Figure 5.22 shows the distribution of the input bias current. Its value is found by taking one fourth the sum of the two input bias measured currents. Its value is very close to the simulation results. Figure 5.23 shows the distribution of the input offset current which has been found by taking half the value of the difference between the measured currents. Its 3σ value is ±173 nA. That means that the current gains of the two input transistors have a 3σ mismatch of ±5.3 %, which agrees with the manufacturer's data sheet value of ±5 %.

5.3.2 Transient Performance

The propagation delay of the comparator was measured by applying a pulse at the input and measuring with a probe the time difference between the input and the output pulse. First the input signal was probed and the waveform of the incoming signal was displayed along with the waveform of the probe signal. The coaxial cable cable legth of the incoming signal was adjusted until the two waveforms seem to have zero delay as shown in Figure 5.24.

Then the probe was removed from the input comparator pin and was placed at the output. The propagation delay was measured directly as the time difference between the two waveforms shown in Figure 5.25. Eigth devices were measured. The measured propagation delay values ranged from 1.9 ns to 2.3 ns with an average value of 2.1 ns. Assuming a measurement error of about ±0.1 ns, then the measured results agree with the simulation results.

Figure 5.26 shows the comparator response to a square wave with slow rise and fall times. The ripples are attributed to the probe impedance mismatches. Figure 5.27 shows the comparator response to a 100 MHz sinewave. It can been seen that the output waveform is still fairly square. The chip photomicrograph is shown in Figure 5.28.

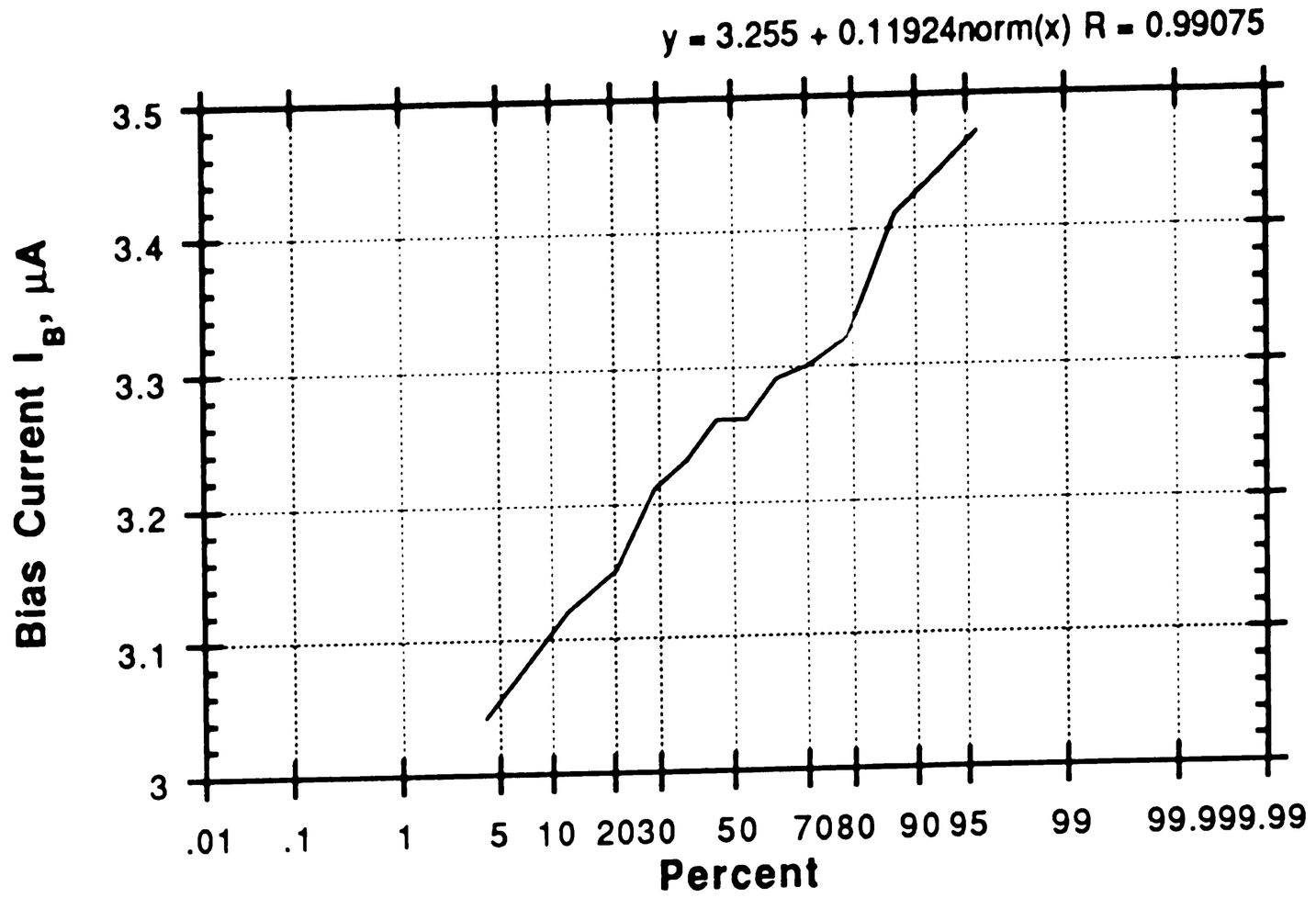


Figure 5.22. Input bias current distribution

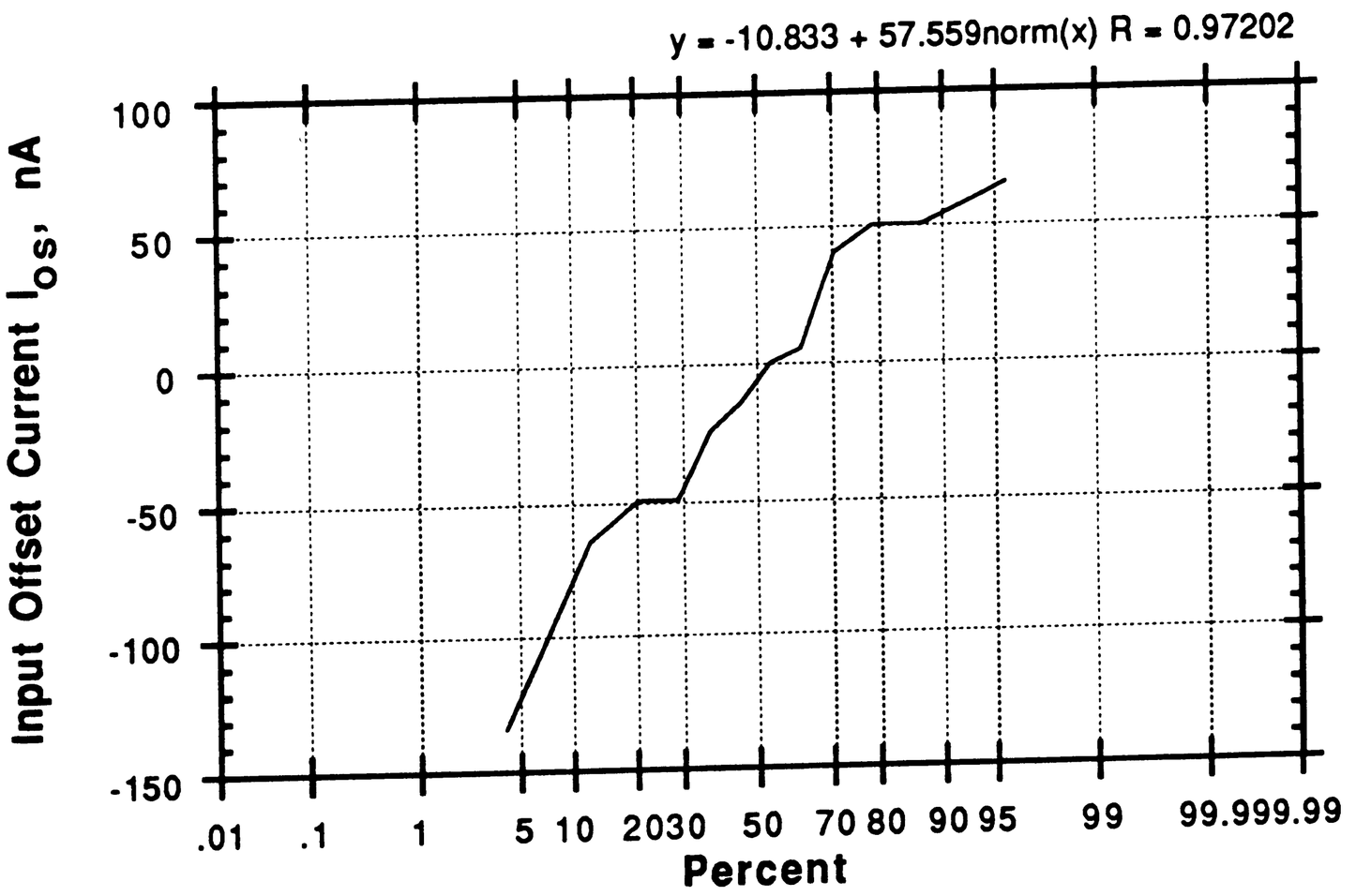


Figure 5.23. Input offset current distribution

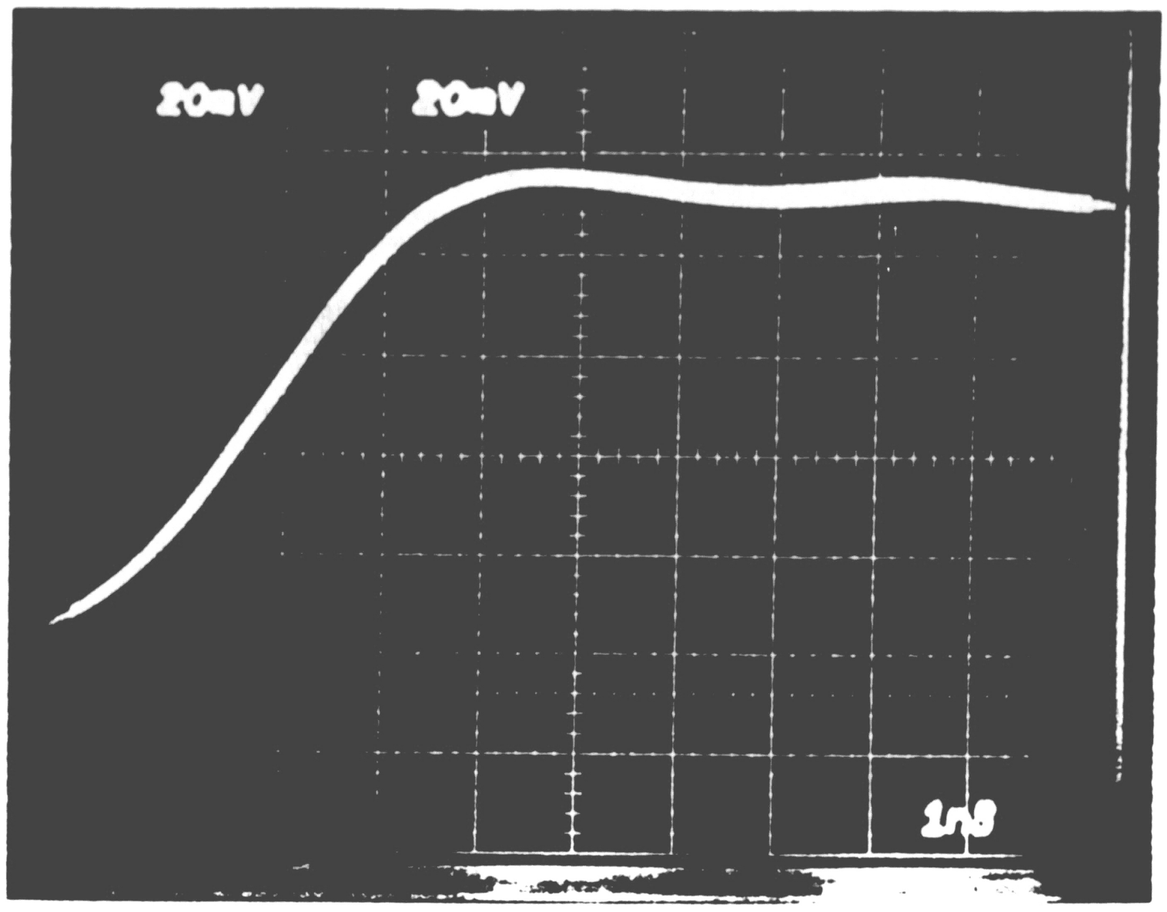


Figure 5.24. Nulling the difference of the input signal and probe propagation delays

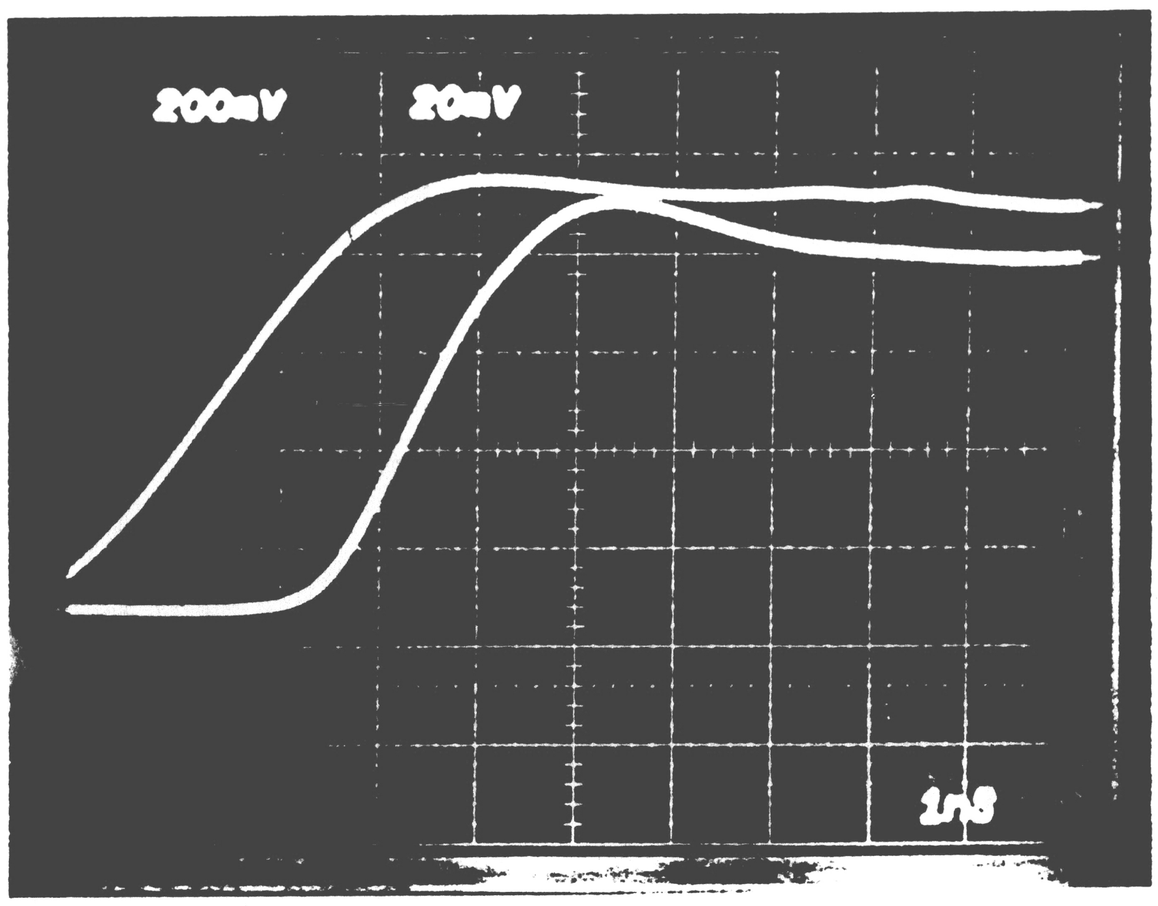


Figure 5.25. Input and output waveforms used to measure the propagation delays

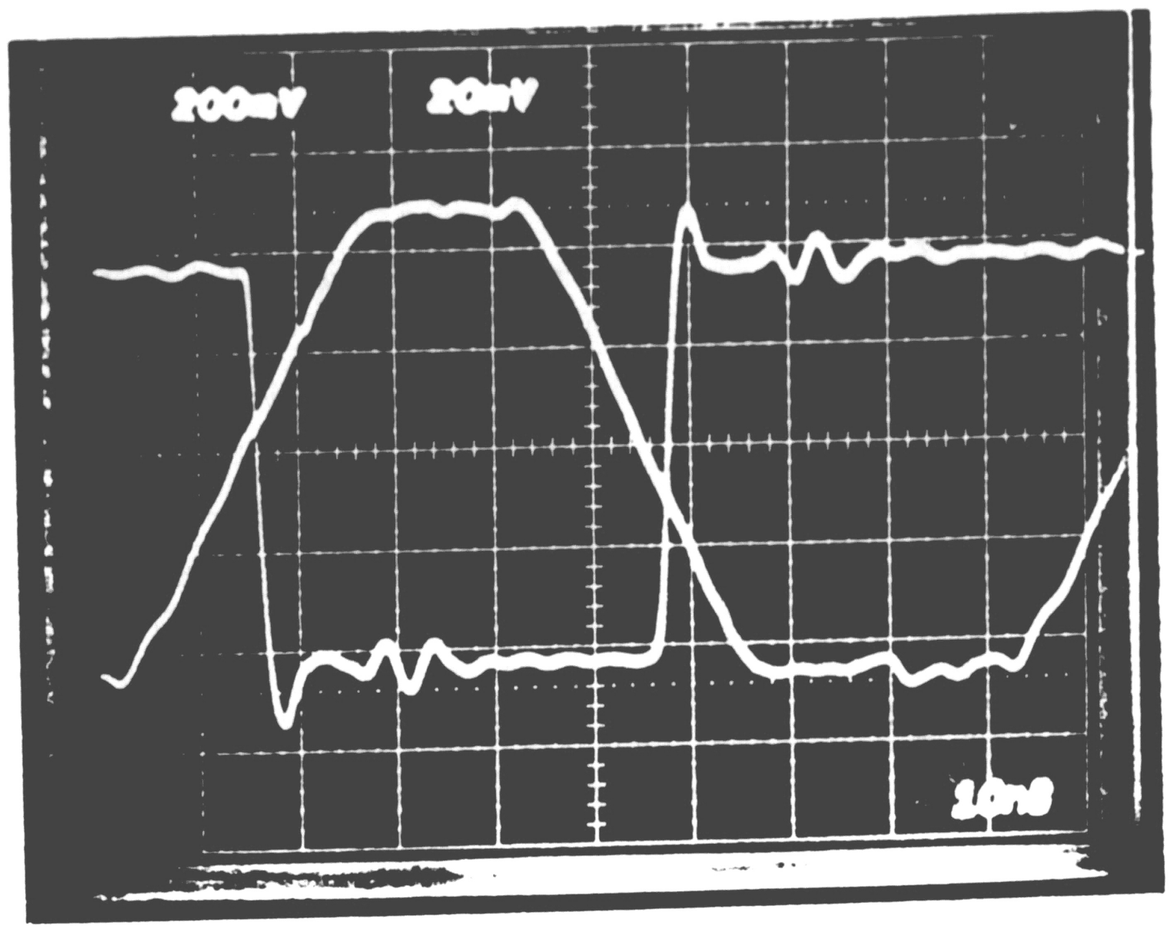


Figure 5.26. Comparator response to a square wave

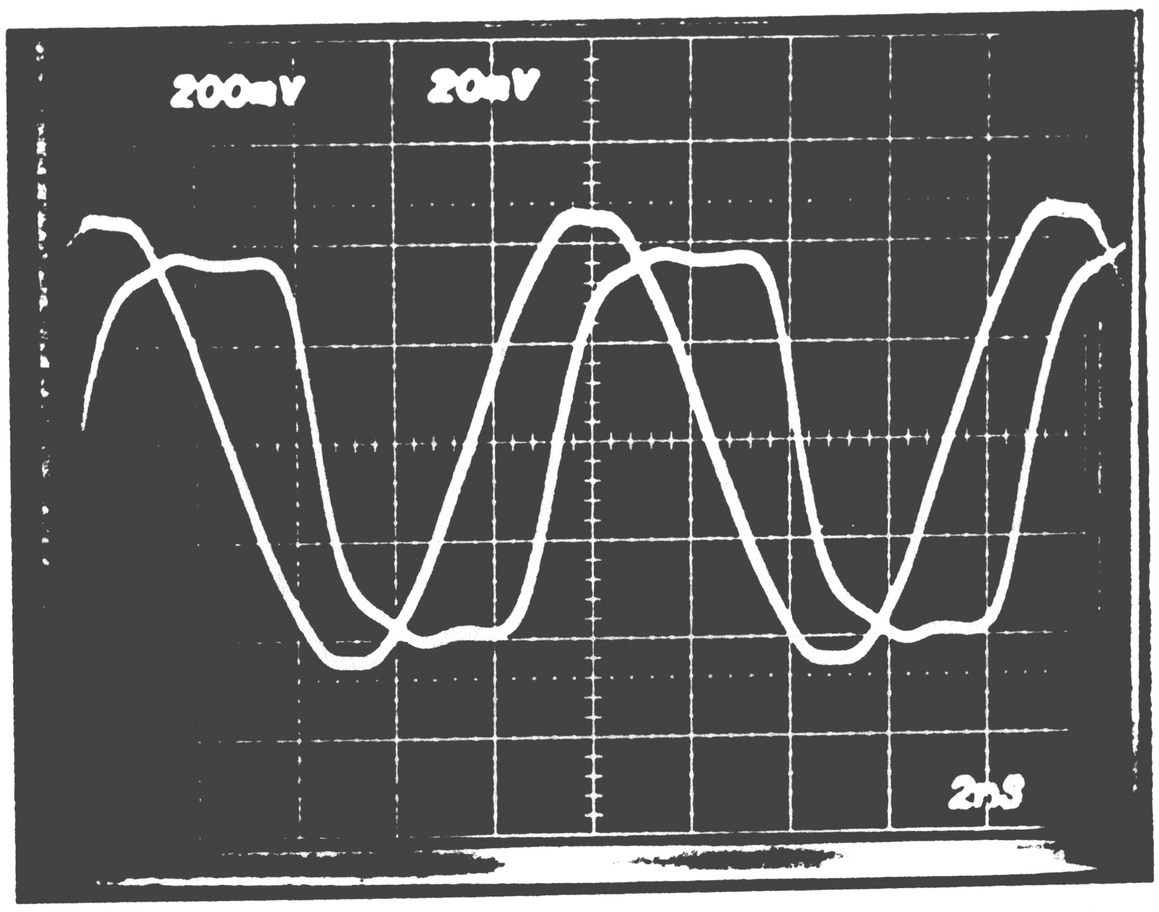


Figure 5.27. Comparator response to a 100 MHz sinewave

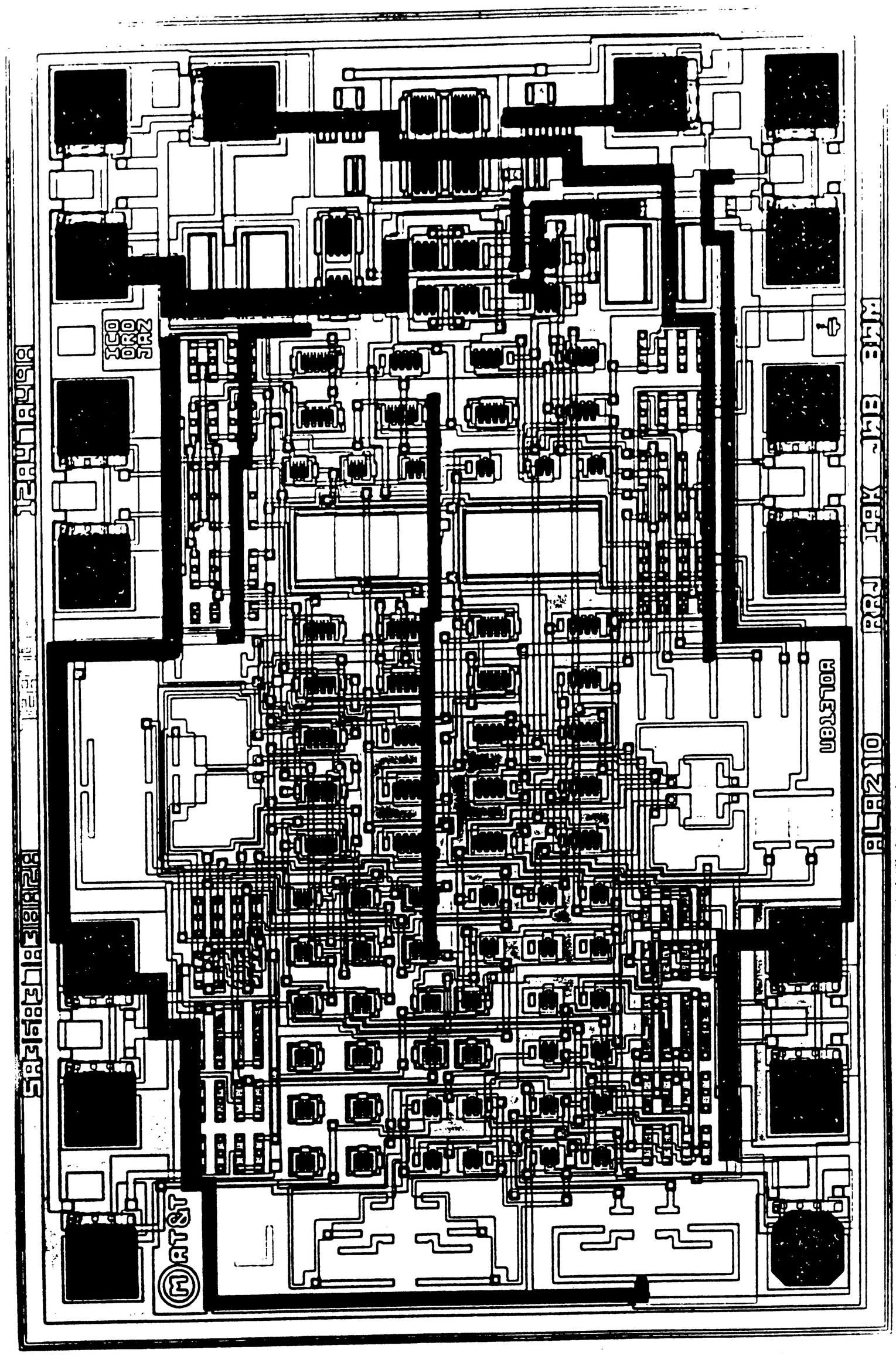


Figure 5.28. Chip photomicrograph

CHAPTER 6

Discussion of Results and Conclusion

6.1 Discussion of Results

Based on the experimental results, it appears that the comparator described here functions according to the predictions made based on calculations and/or simulations. However, two important parameters, namely the voltage gain and the input offset voltage, were not measured because of the high frequency oscillation problem.

According to various industry sources [17,18,19] this oscillation problem with comparators is the rule rather than the exception. In fact, it has been named comparator chatter. It is attributed to the fact that the comparator, being a very fast device with high gain, is particularly susceptible to AC feedback originating mostly from package and test fixture parasitics. According to this theory, the comparator described here is expected to be more susceptible to these parasitic effects since it has the uprecedented combination of gain and speed.

The effects of the feedback on the stability of an amplifier are well known. An amplifier, with open loop gain of $A_V(\omega)$ and negative feedback attenuation of β, will oscillate if the magnitude of the the loop gain is higher than unity and its phase shift is larger than 180°. Therefore, the comparator described here is potentially unstable if the isolation from the output to the input pins is less than the comparator gain, which is as much as 76.1 dB. This isolation magnitude is very large and can only be achieved by using specialized packages.

The calculation of the isolation between pins is very difficult. However we can do order-of-magnitude calculations to test the validity of this theory by assuming that the test circuit of Figure 6.1 has a package parasitic capacitance C_P connected from Q_{OUT} (pin#3) to the inverting input (pin#1). Note that the

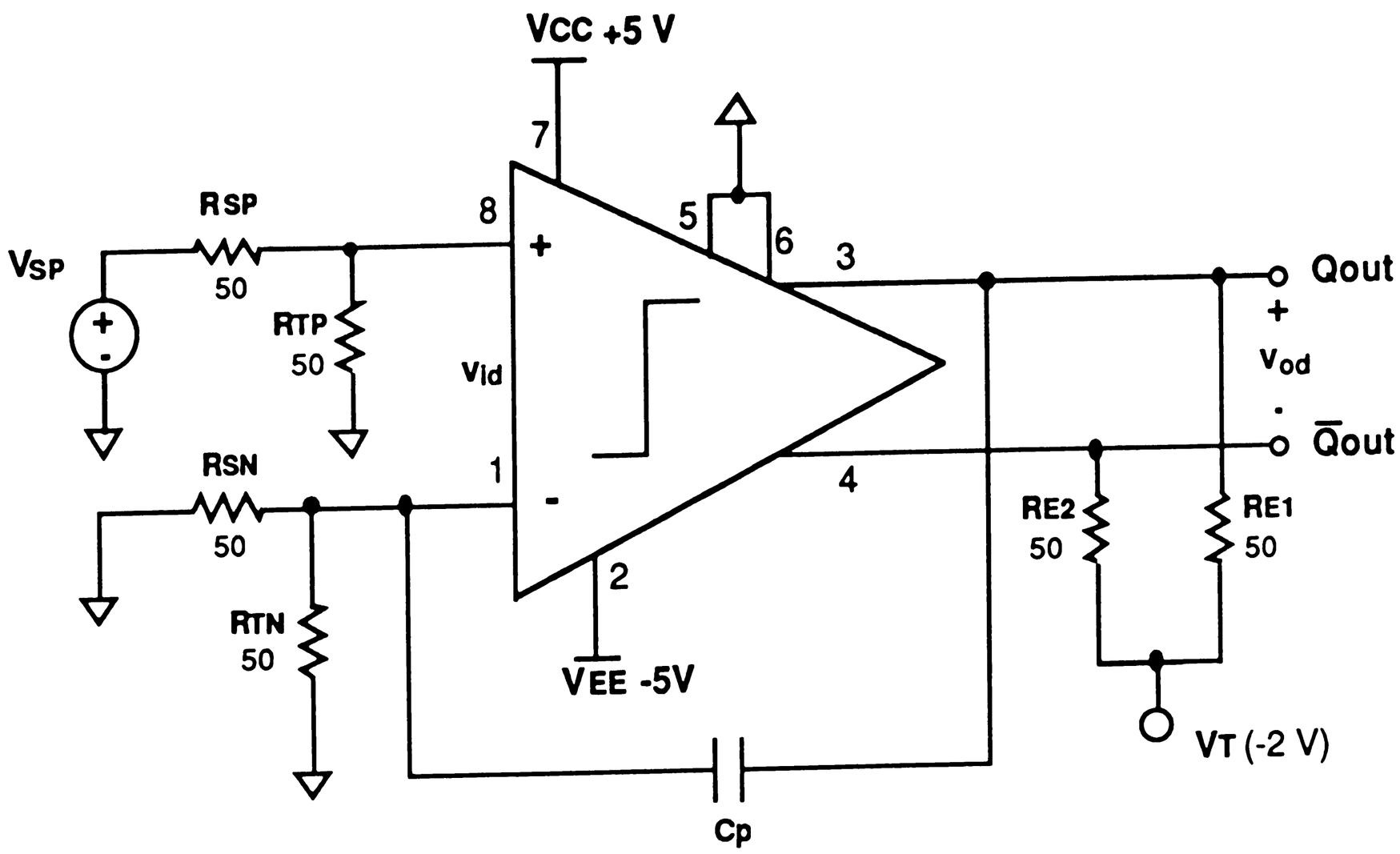


Figure 6.1. Comparator test circuit schematic diagram with package parasitic feedback capacitor.

effective impedance Rs at each input terminal is 25 Ω (R_{SN}//RSP). The value of the capacitor necessary such that an oscillatory condition occurs is calculated from the fact that the inverse of the feedback gain has to be less or equal to the open-loop gain of the comparator $A_V(f)$ at frequencies higher than the bandwidth f_{-3dB}. Therefore the minimum capacitance value necessary for oscillation is given by

$$C_{P,min} \approx \frac{1}{2\,\pi\, f_{-3dB}\, A_V\, R_S} = \frac{1}{6.28\ 227\ 10^6\ 6400\ 25} = 4.4\,fF \qquad (6.1)$$

The magnitude of this parasitic capacitance is small compared to the package parasitic capacitance. The parasitic capacitance values reported in the literature vary usually from a few hundred fempto-Farads to a few pico-Farads [20]. As an example, if the pin-to-pin capacitance of the DIP packages is in the order of 0.22 pF, then the capacitance from pin#1 (V_{IN-}) to pin#3 (Q_{OUT}) is in the

order of 110 fF. Even this relatively low value is 25 times higher than the value calculated using Equation (6.1).

Using this value of parasitic capacitance, the maximum gain that can be achieved while maintaining the same bandwidth is 25 times smaller; which is calculated to be $A_{V,max} = 256$. Therefore, the minimum signal that can be applied without oscillation is ±3.0 mV which is very close to the value that has been observed experimentally (±4 mV).

If the voltage gain is to be maintained then the bandwidth has to be decreased 25 times to 9.1 MHz (if oscillations are to be avoided). In otherwords, the propagation delay will increase to 55 ns. From (6.1) we can calculate the maximum gain-bandwidth product GBW for a comparator packaged in a DIP package to be

$$GBW_{max} = f_{-3dB}\, A_V \approx \frac{1}{2\ \pi\ Cp\ Rs} = \frac{1}{6.28\ 110\ 10^{-15}\ 25} = 58\ GHz \qquad (6.1)$$

Examining Figure 5.6 we observe that the GBW of 58 GHz occurs at a little less than 1 GHz which is almost the same frequency of the experimentally observed oscillation shown in Figure 5.21.

Based on the above discussion, its is obvious that in order to be able to measure the gain of the comparator a package with very low parasitics has to be used. The preferred package should have very high isolation from input to the output pins. Another feature is that it should have low pin inductance so that fast transient signals would not disturb common power supplies and grounds.

On the chip level, each gain stage has been laid out separately from each other so that crosstalk between stages is minimized. Perhaps, the oscillation problem could be reduced by using a non-standard pinout which includes multiple supply and ground pins. This comparator has all four stages sharing the same negative power supply and the first two stages sharing the positive power supply.

If the oscillation problem is eliminated, the input offset voltage is expected to be as low as was predicted. This is due to the fact that the input offset voltage and offset current both depend on the mismatch of the input stage transistors and the fact that the experimentally measured values of the input offset current are almost exactly the same as the values predicted. Once the offset voltage is within the trim range, it can be trimmed to within ±50 μV as predicted in Chapter 4. No attempt has been made to trim the offset.

The comparator bit accuracy can now be calculated based on the measured and predicted parameter values. Assuming 1 KΩ DC source impedances, the input uncertainty window can be calculated from (2.4) and (2.8) to be

$$V_u \approx \frac{763\ mV}{6400} + \sqrt{(50\ \mu V)^2 + (1K\ 173\ nV)^2} = \pm 300\ \mu V$$

Therefore, for a 5V full-scale input voltage the comparator bit accuracy is found from Equation (2.11) to be

$$N_C = \frac{\ln \frac{V_{FS}}{V_u}}{\ln 2} - 1 = 13.0 \text{ bits} \qquad (6.2)$$

Thus for a 12-bit system the comparator contributes half the error since

$$f_\varepsilon = \frac{2\ (300\ \mu V)}{1.221\ mV} \approx 0.5 \quad (\text{or} \quad \varepsilon = 1) \qquad (6.3)$$

which is reasonable. The comparator bit precision can be improved by reducing the source impedance.

6.2 Conclusion

An analog comparator has been designed, fabricated using a complementary bipolar linear array, and tested. Both block and transistor level design techniques have been developed so that the comparator can achieve performance necessary for 12-bit accurate A/D converter systems.

On-chip thin film resistors allow the input offset voltage be trimmed to less than ±50 μV. The voltage gain is calculated to be 6,400 (76.1 dB). The measured typical value of the input bias current is 3.3 μA while the 3σ value of the input offset current is 173 nA. Thus, the maximum error contributed by the comparator to the A/D system is calculated to be ±300 μV, or half the LSB size (assuming a 5 V full-scale input voltage and 1 KΩ source impedance).

Vertical PNP transistors, as opposed to commonly used Zener diodes, perform the level shifting with high speed while allowing the use of a 5-to-10 V power supply. In addition, a modified emitter-coupled pair amplifier design has been used to achieve a 2.1 ns typical propagation delay.

It has been shown both high speed and high accuracy can be achieved simultaneously only if a package with low parasitic capacitances and inductances, and excellent (>80 dB) output to input isolation is used. If an 8-pin ceramic DIP package is used, the comparator can oscillate at a frequency of about 900 MHz in the linear range which prohibits the voltage gain from reaching its maximum value and limits its input linear range.

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APPENDIX

CBIC-U Transistor PSPICE Model Values

TRANSISTOR NU231A01

SIZE = 46 x 71 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 1.0E-05A TO 2.0E-03A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 6.0E-04A TO 3.0E-03A
MAXIMUM CURRENT HANDLING CAPABILITY 8.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	53.6	89.8	143.2
IRB	0	0	0
RBM	25.3	19.9	12.2
RC	36.2	30.7	25.2
RE	1.4	1.4	1.4
IS	5.25E-17	1.58E-16	2.93E-16
EG	1.206	1.206	1.206
XTI	2	2	2
XTB	2.363	2.363	2.363
BF	100	220	380
IKF	12E-3	6E-3	8E-3
NF	1	1	1
VAF	84	66	30
ISE	1.19E-15	1.19E-15	1.19E-15
NE	1.7	1.7	1.8
BR	4	4	4
IKR	1E6	1E6	1E5
NR	1	1	1
VAR	3	3	3
ISC	1.92E-20	1.92E-20	1.92E-20
NC	1.7	1.7	1.7
TF	28P	25P	20P
TR	5.3N	3.8N	1.8N
CJE	181E-15	120E-15	89E-15
VJE	1.105	1.105	1.105
MJE	0.495	0.495	0.495
CJC	196E-15	166E-15	136E-15
VJC	0.615	0.615	0.615
MJC	0.335	0.335	0.335
XCJC	0.144	0.144	0.144
CJS	412E-15	368.4E-15	332.8E-15
VJS	0.5	0.5	0.5
MJS	0.318	0.318	0.318
FC	0.5	0.5	0.5
ITF	45E-3	45E-3	45E-3
VTF	10	10	10
XTF	30	15	10

TRANSISTOR NU431A01

SIZE = 46 x 93 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 2.0E-05A TO 4.0E-03A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 1.2E-03 TO 6.0E-03A
MAXIMUM CURRENT HANDLING CAPABILITY 16.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	26.8	44.9	71.6
IRB	0	0	0
RBM	12.65	9.95	6.1
RC	36.2	30.7	25.2
RE	0.7	0.7	0.7
IS	1.05E-16	3.16E-16	5.86E-16
EG	1.206	1.206	1.206
XTI	2	2	2
XTB	2.363	2.363	2.363
BF	100	220	380
IKF	24E-3	12E-3	16E-3
NF	1	1	1
VAF	84	66	30
ISE	2.39E-15	2.39E-15	2.39E-15
NE	1.7	1.7	1.8
BR	4	4	4
IKR	2E6	2E6	2E6
NR	1	1	1
VAR	3	3	3
ISC	3.84E-20	3.84E-20	3.84E-20
NC	1.7	1.7	1.7
TF	P	25P	20P
TR	6.3N	4.3N	2N
CJE	362E-15	240E-15	178E-15
VJE	1.105	1.105	1.105
MJE	0.495	0.495	0.495
CJC	340.4E-15	288.44E-15	237.2E-15
VJC	0.615	0.615	0.615
MJC	0.335	0.335	0.335
XCJC	0.166	0.166	0.166
CJS	538.2E-15	481.2E-15	434.7E-15
VJS	0.5	0.5	0.5
MJS	0.318	0.318	0.318
FC	0.5	0.5	0.5
ITF	90E-3	90E-3	90E-3
VTF	10	10	10
XTF	30	15	10

TRANSISTOR NU362A02

SIZE = 123.5 x 98 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 6.0E-05A TO 1.2E-02A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 3.6E-03A TO 1.8E-02A
MAXIMUM CURRENT HANDLING CAPABILITY 30.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	8.934	14.967	23.863
IRB	0	0	0
RBM	4.217	3.317	2.033
RC	4.704	3.989	3.274
RE	0.233	0.233	0.233
IS	3.15E-16	9.48E-16	1.758E-15
EG	1.206	1.206	1.206
XTI	2	2	2
XTB	2.363	2.363	2.363
BF	100	220	380
IKF	72E-3	36E-3	48E-3
NF	1	1	1
VAF	84	66	30
ISE	7.16E-15	7.16E-15	7.16E-15
NE	1.7	1.7	1.8
BR	4	4	4
IKR	6E6	6E6	6E6
NR	1	1	1
VAR	3	3	3
ISC	1.15E-19	1.15E-19	1.15E-19
NC	1.7	1.7	1.7
TF	28P	25P	20P
TR	8.3N	6.4N	2.5N
CJE	1.086E-12	720E-15	534E-15
VJE	1.105	1.105	1.105
MJE	0.495	0.495	0.495
CJC	921E-15	780.5E-15	642.1E-15
VJC	0.615	0.615	0.615
MJC	0.335	0.335	0.335
XCJC	0.183	0.183	0.183
CJS	800.7E-15	715.8E-15	646.6E-15
VJS	0.5	0.5	0.5
MJS	0.318	0.318	0.318
FC	0.5	0.5	0.5
ITF	270E-3	270E-3	270E-3
VTF	10	10	10
XTF	30	15	10

TRANSISTOR NU663A02

SIZE = 146 x 160
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 1.2E-04A TO 2.4E-02A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 7.2E-03A TO 3.6E-02A
MAXIMUM CURRENT HANDLING CAPABILITY 60.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	4.466	7.483	11.937
IRB	0	0	0
RBM	2.108	1.658	1.017
RC	2.352	1.995	1.637
RE	0.1167	0.1167	0.1167
IS	6.3E-16	1.896E-15	3.51E-15
EG	1.206	1.206	1.206
XTI	2	2	2
XTB	2.363	2.363	2.363
BF	100	220	380
IKF	144E-3	72E-3	96E-3
NF	1	1	1
VAF	84	66	30
ISE	1.43E-14	1.43E-14	1.43E-14
NE	1.7	1.7	1.8
BR	4	4	4
IKR	12E6	12E6	12E6
NR	1	1	1
VAR	3	3	3
ISC	2.31E-19	2.31E-19	2.31E-19
NC	1.7	1.7	1.7
TF	28P	25P	20P
TR	10.8N	7.3N	3.5N
CJE	2.172E-12	1.44E-12	1.068E-12
VJE	1.105	1.105	1.105
MJE	0.495	0.495	0.495
CJC	1.665E-12	1.41E-12	1.161E-12
VJC	0.615	0.615	0.615
MJC	0.335	0.335	0.335
XCJC	0.203	0.203	0.203
CJS	1.065E-12	951.6E-15	859.7E-15
VJS	0.5	0.5	0.5
MJS	0.318	0.318	0.318
FC	0.5	0.5	0.5
ITF	540E-3	540E-3	540E-3
VTF	10	10	10
XTF	30	15	10

TRANSISTOR PU231A01

SIZE = 52.5 x 72.5 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 1.0E-05A TO 2.2E-03A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 6.0E-04A TO 3.6E-03A
MAXIMUM CURRENT HANDLING CAPABILITY 8.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	52.61	71.36	98.8
IRB	0	0	0
RBM	33.81	25.66	16.8
RC	45.97	37.8	29.56
RE	0.6	0.6	0.6
IS	5.32E-17	1.21E-16	2.18E-16
EG	1.206	1.206	1.206
XTI	1.5	1.5	1.5
XTB	2.053	2.053	2.053
BF	64	115	190
IKF	15E-3	15E-3	20E-3
NF	1	1	1
VAF	50	30	21
ISE	1.3E-14	6.1E-15	5.7E-15
NE	1.557	1.557	1.6
BR	4	4	4
IKR	1E6	1E6	1E6
NR	1	1	1
VAR	1.4	1.4	1.4
ISC	2.49E-18	2.49E-18	2.49E-18
NC	1.634	1.634	1.634
TF	50P	33P	29P
TR	10.8N	4.3N	1.3N
CJE	163E-15	120E-15	89E-15
VJE	0.8939	0.8939	0.8939
MJE	0.493	0.493	0.493
CJC	365.45E-15	316.73E-15	267.6E-15
VJC	0.53	0.53	0.53
MJC	0.19	0.19	0.19
XCJC	0.144	0.144	0.144
CJS	807.1E-15	769E-15	730.6E-15
VJS	0.6	0.6	0.6
MJS	0.348	0.348	0.348
FC	0.8	0.8	0.8
ITF	150E-3	150E-3	150E-3
VTF	10	10	10
XTF	24	18	13

TRANSISTOR PU432A01

SIZE = 52.5 x 105.5 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 2.0E-05A TO 4.5E-03A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 1.2E-03A TO 7.2E-03A
MAXIMUM CURRENT HANDLING CAPABILITY 16.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	26.31	35.68	49.4
IRB	0	0	0
RBM	16.91	12.83	8.4
RC	22.99	18.88	14.78
RE	0.3	0.3	0.3
IS	1.064E-16	2.42E-16	4.36E-16
EG	1.206	1.206	1.206
XTI	1.5	1.5	1.5
XTB	2.053	2.053	2.053
BF	64	115	190
IKF	30E-3	30E-3	40E-3
NF	1	1	1
VAF	50	30	21
ISE	2.6E-14	1.22E-14	1.14E-14
NE	1.557	1.557	1.6
BR	4	4	4
IKR	2E6	2E6	2E6
NR	1	1	1
VAR	1.4	1.4	1.4
ISC	4.98E-18	4.98E-18	4.98E-18
NC	1.634	1.634	1.634
TF	50P	33P	29P
TR	12.3N	5.3N	1.3N
CJE	326E-15	240E-15	178E-15
VJE	0.8939	0.8939	0.8939
MJE	0.493	0.493	0.493
CJC	635.1E-15	550.4E-15	465E-15
VJC	0.53	0.53	0.53
MJC	0.19	0.19	0.19
XCJC	0.165	0.165	0.165
CJS	1.201E-12	1.145E-12	1.088E-12
VJS	0.6	0.6	0.6
MJS	0.348	0.348	0.348
FC	0.8	0.8	0.8
ITF	300E-3	300E-3	300E-3
VTF	10	10	10
XTF	24	18	13

TRANSISTOR PU392A02

SIZE = 172.5 x 94.5 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 9.0E-05A TO 2.0E-02A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 5.4E-03A TO 3.2E-02A
MAXIMUM CURRENT HANDLING CAPABILITY 30.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	5.846	7.929	10.978
IRB	0	0	
RBM	3.757	2.851	1.867
RC	5.317	4.368	3.419
RE	0.067	0.067	0.067
IS	4.788E-16	1.089E-15	1.962E-15
EG	1.206	1.206	1.206
XTI	1.5	1.5	1.5
XTB	2.053	2.053	2.053
BF	64	115	190
IKF	135E-3	135E-3	180E-3
NF	1	1	1
VAF	50	30	21
ISE	1.17E-13	5.49E-14	5.13E-14
NE	1.557	1.557	1.6
BR	4	4	4
IKR	9E6	9E6	9E6
NR	1	1	1
VAR	1.4	1.4	1.4
ISC	2.24E-17	2.24E-17	2.24E-17
NC	1.634	1.634	1.634
TF	50P	33P	29P
TR	15N	6.3N	1.5N
CJE	1.467E-12	1.08E-12	801E-15
VJE	0.8939	0.8939	0.8939
MJE	0.493	0.493	0.493
CJC	2.437E-12	2.112E-12	1.784E-12
VJC	0.53	0.53	0.53
MJC	0.19	0.19	0.19
XCJC	0.194	0.194	0.194
CJS	3.372E-12	3.212E-12	3.052E-12
VJS	0.6	0.6	0.6
MJS	0.348	0.348	0.348
FC	0.8	0.8	0.8
ITF	1.35	1.35	1.35
VTF	10	10	10
XTF	24	18	13

TRANSISTOR PU693A02

SIZE = 202.5 x 156.5 MICRONS
RECOMMENDED Ic RANGE FOR >80% PEAK DC GAIN 1.8E-04A TO 4.1E-02A
RECOMMENDED Ic RANGE FOR >80% PEAK SPEED 1.1E-02A TO 6.5E-02A
MAXIMUM CURRENT HANDLING CAPABILITY 60.0E-03A

VARIABLE	SLOW	NOMINAL	FAST
RB	2.922	3.965	5.489
IRB	0	0	0
RBM	1.878	1.426	0.933
RC	2.659	2.184	1.71
RE	0.033	0.033	0.033
IS	9.576E-16	2.178E-15	3.924E-15
EG	1.206	1.206	1.206
XTI	1.5	1.5	1.5
XTB	2.053	2.053	2.053
BF	64	115	190
IKF	270E-3	270E-3	360E-3
NF	1	1	1
VAF	50	30	21
ISE	2.34E-13	1.1E-13	1.03E-13
NE	1.557	1.557	1.6
BR	4	4	4
IKR	18E6	18E6	18E6
NR	1	1	1
VAR	1.4	1.4	1.4
ISC	4.48E-17	4.48E-17	4.48E-17
NC	1.634	1.634	1.634
TF	50P	33P	29P
TR	19N	7.6N	1.5N
CJE	2.934E-12	2.16E-12	1.602E-12
VJE	0.8939	0.8939	0.8939
MJE	0.493	0.493	0.493
CJC	4.402E-12	3.815E-12	3.222E-12
VJC	0.53	0.53	0.53
MJC	0.19	0.19	0.19
XCJC	0.214	0.214	0.214
CJS	6.051E-12	5.765E-12	5.477E-12
VJS	0.6	0.6	0.6
MJS	0.348	0.348	0.348
FC	0.8	0.8	0.8
ITF	2.7	2.7	2.7
VTF	10	10	10
XTF	24	18	13

Vita

Iconomos (Ico) Antonios Koullias was born on August 28th, 1959 in the Greek island of Kalymnos, located in the southeastern part of the Aegean sea. His father, Antonios Iconomos Koullias, and mother, Evdokia (the daughter of Mikhail and Helen Marangos), both came from families of fishermen and spongedivers.

In the summer of 1977, right after finishing high school, Ico Koullias immigrated in the United States, settling in the town of Tarpon Springs, Florida. While handling various odd jobs, including plumber, dishwasher, and busboy, he attended St. Petersburg Junior College and received his Associate in Arts degree in the summer of 1979. He then transferred to the University of Florida where he received his Bachelor in Electrical Engineering degree in May, 1982.

After graduation, he worked for Burr-Brown Corp. located in Tucson, Arizona as a product engineer. He dealt primarily with the manufacturing issues of high-precision amplifiers. At the same time, he attended classes at the University of Arizona towards a Master's degree and taught an electronics course at Pima College. In December 1983, he returned to Florida, and worked for the Semiconductor Division of the Harris Corporation as an analog integrated circuit design engineer. He designed mainly high-speed circuits, including the world's fastest (as of this writing) unity-gain stable operational amplifier in production. He also studied, competed, and taught under Master Pok Sik Yun the Korean martial art of Tae Kwon Do in which he earned a second degree black belt. In December 1986 he got married to former Cynthia Madelline, the daughter of William and Joan Lee.

In May 1988, he moved to Reading Pennsylvania where he started working as an MTS for AT&T Bell Laboratories. Also, he started attending classes at Lehigh University in the fall semester of the same year. His first child, Anthony William, was born in February 1989. Ico is scheduled to receive his MS degree in October of this year (1990).