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The design and fabrication of a UHF voltage-controlled oscillator bipolar integrated circuit and a study of chip-level interconnects

Douglas Alan Williams
Lehigh University

THE DESIGN AND FABRICATION OF A UHF VOLTAGE-CONTROLLED OSCILLATOR BIPOLAR INTEGRATED CIRCUIT AND A STUDY OF CHIP-LEVEL INTERCONNECTS

by

Douglas Alan Williams

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(date)

M Hatab

Professor in Charge

Lawrence J Vanneni

Chairman of Department

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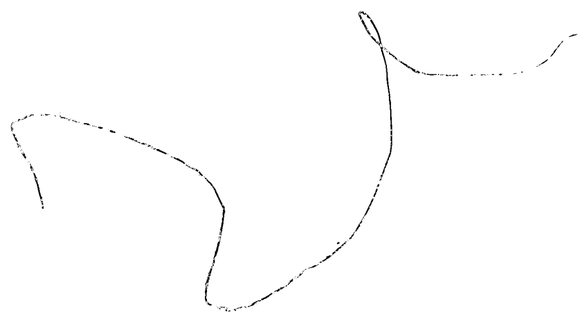
ABSTRACT

This research explores the design and fabrication of a bipolar voltage-controlled oscillator (VCO) integrated circuit that has an operating frequency of 1.2 GHz. This VCO circuit employs the emitter-coupled architecture and has been optimized for maximum operating frequency. It requires a single 10 volt power supply and 37 mA supply current. The temperature coefficient of the on-chip current reference has been adjusted to nominally zero over the range 0 to 100 °C.

To verify the performance of this design, the circuit has been fabricated on an AT&T ALA201 semicustom linear array in the CBIC-U (Complementary Bipolar Integrated Circuit) technology. In this technology the NPN transistors typically have a beta of 100 and an f_T of 4.5 GHz, and the PNP transistors have a beta of 40 and an f_T of 3.7 GHz.

Additionally, the effects of interconnects for circuits operating at frequencies about 1 GHz are investigated. First, the effects of "long-distance" on-chip interconnects are evaluated. Then chip-to-chip wire interconnects are studied and guidelines for their proper application are developed within the context of wafer-scale integration.



1. INTRODUCTION

1.1 OSCILLATOR OVERVIEW

The functions of electronic circuits can be divided into two general classifications: (1) signal-processing circuits which operate on an existing signal; and (2) signal-generating circuits which produce their own signals[1]. Circuits such as amplifiers, comparators, integrators, differentiators and active filters fall into the former category. Oscillators fall into the second category. Aside from amplifiers, oscillators are probably the most common analog building block used in electronic circuits today.

An oscillator is a key subcircuit used in the design of many complex electronic systems. Its sole function is to generate a stable and periodic waveform to then be used by other circuits. Depending on the application, this AC output signal can be a waveform of any type: sinusoidal, square, triangular, ramp, pulse, etc. The applications include communications systems (AM and FM broadcast and reception, telephony, etc.); analog circuits (frequency synthesizers, phase-locked loops, detectors, function generators, etc.); and digital systems (clock signals and data transmission).

There are two basic categories of oscillators[1]: The tuned oscillators, generally consisting of an amplifier and feedback network, most often use an LC tank circuit or piezoelectric resonator (either a quartz crystal or ceramic resonator) as the frequency-setting components. The relaxation oscillators, also called multivibrators, generally use an RC combination to set the frequency of operation. The tuned oscillators offer excellent frequency stability and can operate at frequencies up to several hundred MHz[2]. With a high-Q tank circuit the frequency stability is directly related to and primarily dependent on the reactive elements, and insensitive to the characteristics of the circuit's other components[3, 4, 5]. By

replacing the LC tank circuit with either a quartz crystal or a ceramic resonator, which have a Q of up to 3 orders of magnitude greater, an even more stable oscillator can be designed. However, since the mechanical frequency of the fundamental vibration of the piezoelectric element is inversely proportional to crystal dimension, this type of oscillator is in practice usually limited to operating frequencies of less than 20MHz[6]. To overcome the processing limitations during manufacture of the crystal[7], overtone crystals are sometimes used. These circuits usually have an operating range up to 50MHz[8]. Disadvantages for the tuned oscillator include requiring the use of bulky and costly external components (inductors and capacitors or a piezoelectric resonator) and a very narrow, non-linear tuning range.

On the other hand, the relaxation or multivibrator type oscillators are most common in monolithic integrated circuit design because an inductor or crystal is not required. A timing capacitor is alternately charged and discharged between two internal thresholds by constant-current sources. Periodic waveforms are then generated as the circuit switches back and forth between two astable states. Since the frequency of operation is inversely proportional to the timing capacitor value and proportional to the current source, the center frequency can easily be adjusted over many orders of magnitude. There are several approaches to implementing this type of configuration. One method is known as the grounded capacitor oscillator. This circuit uses a detector that senses the voltage on a timing capacitor and switches the capacitor charge and discharge current sources. It is usually implemented using comparators and a flip-flop. As a consequence, the oscillation frequency is usually limited to several MHz due to the switching delays induced by the comparator and flip-flop. A refinement of the grounded capacitor oscillator technique replaces the comparator and flip-flop with a single-stage Schmitt trigger. Above 20 MHz, however, the switching delay becomes a significant part of the

oscillation period for this method, too[2]. The best refinement of the relaxation oscillator can be found in the method known as the emitter-coupled oscillator. This still employs the constant-current charge and discharge technique, but the configuration of the circuit is such that there is only one high-speed switching section. In addition, the charge and discharge paths for the timing capacitor are topologically and electrically symmetrical. Therefore, it is preferred over the grounded capacitor circuits in most applications because of its inherent output waveform symmetry and higher output frequency capability. Furthermore, for any monolithic IC design that operates at frequencies greater that 20 MHz the emitter coupled architecture is preferred because the Schmitt trigger-type oscillator requires very critical accuracy and stability for the threshold levels.

An extra dimension can be added to the function of an oscillator when the ability to change the frequency with an applied control voltage is added. The basic concept of a voltage-controlled oscillator (VCO) first appeared in the form of a cross-coupled trigger circuit in 1919[9], and by the 1970s VCOs were used in many monolithic IC applications[10,11]. In the 1980s VCOs reached operating frequencies up to several hundred MHz[12,13], and much effort has been spent in optimizing the frequency stability and other performance specifications of these circuits[14].

1.2 MOTIVATION FOR THESIS

With recent advances in complementary bipolar IC fabrication technology providing transistors with f_T values of several GHz, a challenging task to implement an emitter-coupled oscillator that operates at frequencies over 1 GHz presented itself. In order to attain this operating frequency for a monolithic bipolar IC oscillator, the AT&T CBIC-U (Complementary Bipolar Integrated Circuit) technology[15] was used to fabricate this prototype circuit. The circuit and IC chip resulting from this research was optimized to enhance the high frequency capability. Hence the circuit

is designed to operate with low voltage swings and large dc bias currents.

The increased operating speed demonstrated by this circuit requires that the interconnects be carefully investigated for two reasons. First, the models that are currently used for "long-distance" on-chip interconnects in this fabrication technology (e.g., lumped resistance and capacitance) may not be adequate at these higher operating frequencies. Second, the semicustom linear array integrated circuit offers a unique opportunity for wafer-scale integration of analog systems: One can quickly and economically fabricate several different subcircuits simultaneously on a single wafer, and then interconnect only the good chip sites to realize a complex analog function. In this thesis guidelines for the proper application of such interconnections are presented.

1.3 OUTLINE OF THESIS

Presented in Chapter 2 is an overview of the CBIC-U process technology, including component characteristics and models. Chapter 3 reviews the design of the three subcircuits that comprise the VCO circuit, and contains computer simulations of the nominal circuit. An overview of the semicustom linear array used to layout this IC and the actual chip layouts are contained in Chapter 4. The results of full-chip simulations over the range of processing variables are also presented in Chapter 4. Chapter 5 presents the experimental results obtained from the fabricated IC. Chapter 6 describes the study of "long-distance" on-chip interconnections and chip-to-chip wire interconnects. The thesis is concluded with Chapter 7 which summarizes the results of this research and offers suggestions for future topics.

2. IC PROCESS TECHNOLOGY OVERVIEW

2.1 THE CBIC-U TECHNOLOGY

The solid-state electronics field was revolutionized with the invention of the planar process in 1959. Since then microelectronics has been dominated by two process technologies - bipolar and MOS. For digital applications where systems of enormous complexity are integrated into one chip, die size and power consumption are of major concern. In these cases an MOS realization is required. The increased complexity of these digital systems has required that some analog functions (e.g., analog multiplexers, D-A and A-D converters, etc.) be combined on the same chip to reduce cost and increase performance and reliability. This necessity has resulted in the increased use of MOS technology for analog circuit design. However, for the wide range of applications that require high current drive capability and precision analog performance, bipolar will continue to be the technology of choice.

In the early 1970s, activities in bipolar analog integrated circuit design began to be hampered by the limitations[15] imposed by the then current SBC (Standard Buried Collector) technology. In order to understand these limitations, typical device structures will be discussed. The schematic cross-section of a typical SBC NPN transistor is shown in Figure 2.1.

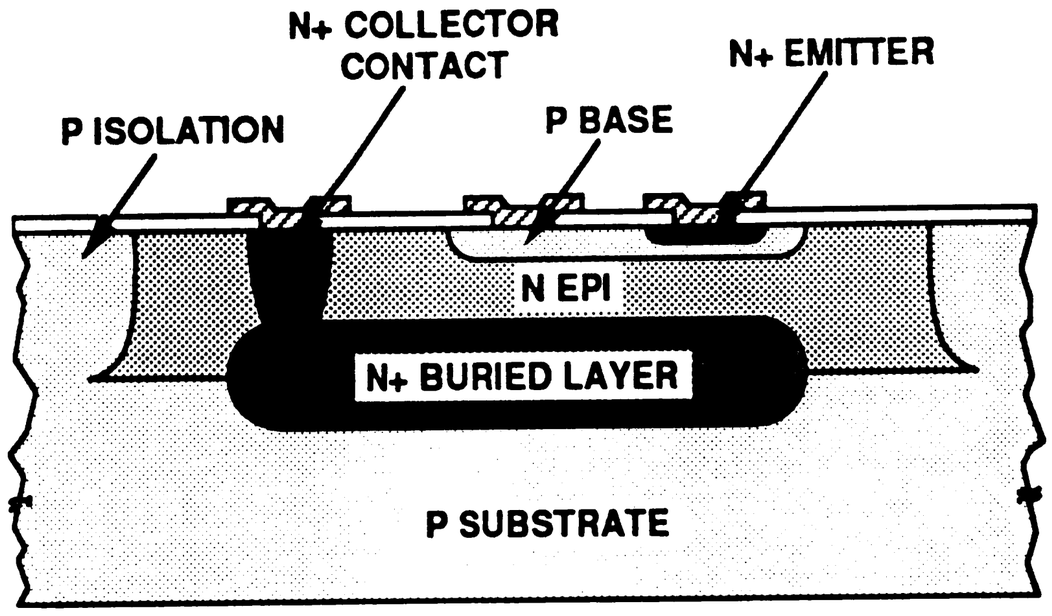


Figure 2.1 Typical SBC NPN Transistor Structure

The analysis of this structure is covered exhaustively in the literature and will not be discussed here, except to note that the minority carriers flow vertically through the base region. To complement this device there are two PNP transistor structures possible in the SBC technology. Both of these structures can be realized without any additions to the SBC processing steps. A cross-section of a lateral PNP structure is illustrated in Figure 2.2.

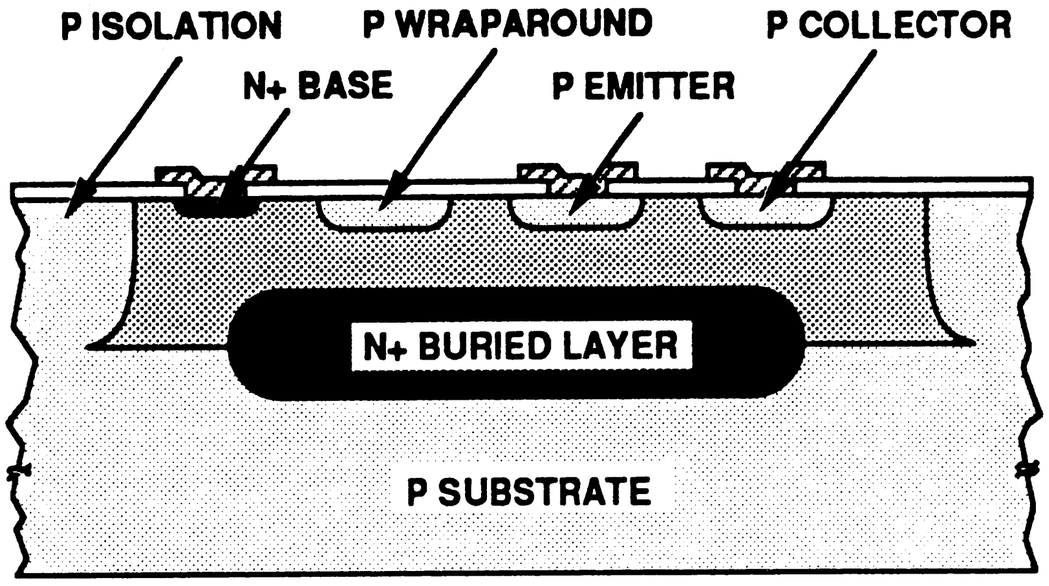


Figure 2.2 SBC Lateral PNP Transistor Structure

It is so-named because the minority carriers flow laterally through the base region as shown in Figure 2.3.

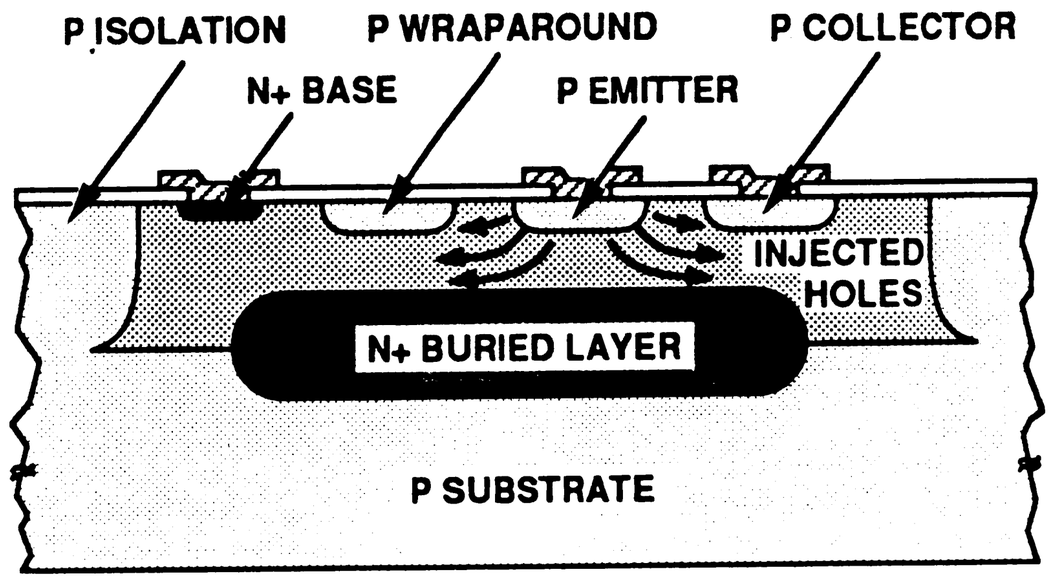


Figure 2.3 Lateral PNP Minority Carrier Flow

The light doping of the n-epi material that acts as the base (compared to the collector doping) requires that the base region be made wide to increase the breakdown voltage. The minimum base transit times exhibited for such a structure are typically 10 to 100 times greater than that of a corresponding NPN transistor. Thus the typical SBC lateral PNP has an f_T which is a factor of 10 to 100 times lower than the NPN. Another drawback to the lateral PNP structure is lower current gain, which is due to several causes[16]: First, some of the holes injected into the base are collected by the substrate which degrades β_F. Also, the wide base region results in a low emitter injection efficiency. Finally, the low base doping results in an earlier onset of the effects of high-level injection and its inherent degradation of current gain as collector current is increased.

An SBC structure that overcomes the poor high-current performance of the lateral device is known as the substrate PNP and is shown in Figure 2.4.

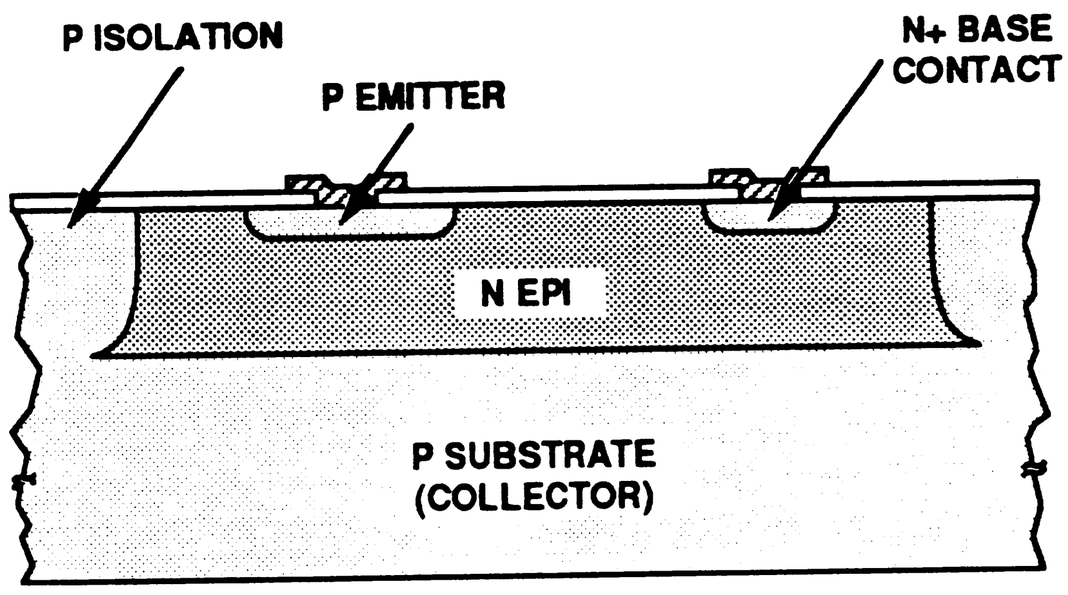


Figure 2.4 SBC Substrate, or Vertical, PNP Transistor Structure

As can be seen in Figure 2.5 the minority carrier flow is vertical, which results in an increase in the effective emitter area when compared to the lateral PNP.

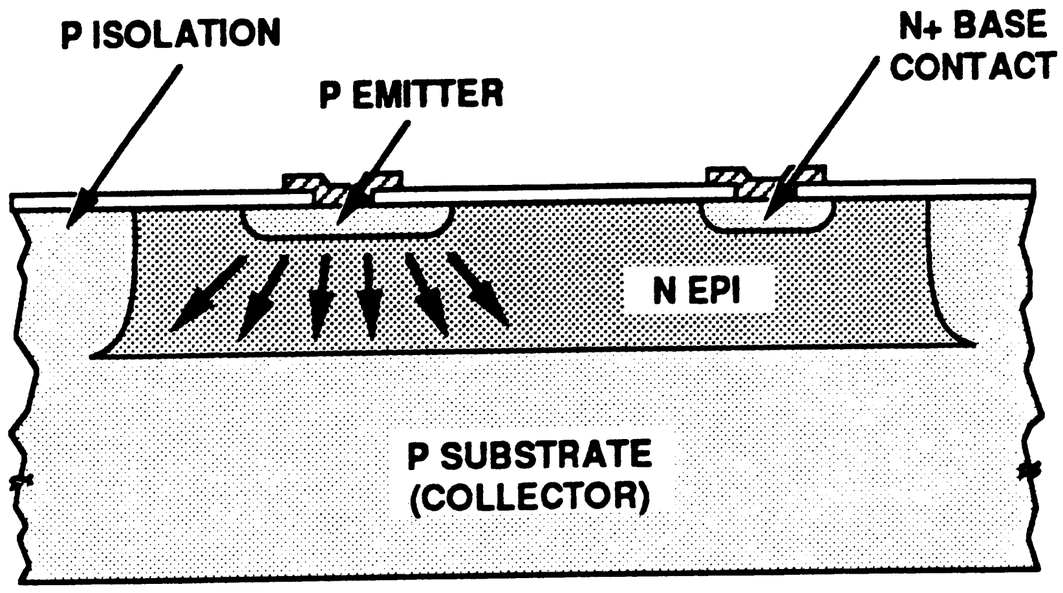


Figure 2.5 Substrate PNP Minority Carrier Flow

Although this structure provides improved β_F performance, the high resistivity of the substrate material can introduce two additional problems: First, the voltage drop in this region can cause the catastrophic effect of forward-biasing other PN junctions on the chip. Secondly, the Miller effect may multiply the already relatively large epi-to-substrate junction capacitance to unacceptable levels. Finally, it should be noted that by having the substrate function as the collector meant that the vertical PNP device was limited to applications within a circuit where its collector connection was defined to be the most-negative voltage applied to the chip.

Due to these drawbacks affecting the PNP devices, the evolution of IC fabrication processes was such that the performance of the NPN transistors was optimized. Therefore the PNP transistor was either entirely avoided in bipolar circuit designs, or relegated to non-critical functions. This on-going optimization of the PNP transistor continues to this day. Indeed, an NPN-only bipolar process with an f_T of 30 GHz has recently been reported[17].

However, many applications require a truly complementary technology where the characteristics of the PNPs and NPNs are closely matched. Examples of such applications include: push-pull output stages with low quiescent power

consumption; symmetric current sources; and, power-efficient level-shifting. As the value of these applications became more apparent, a new fabrication technology evolved at AT&T known as CBIC. The advent of ion implantation[18] as an alternative to diffusion for electronic device fabrication provided the necessary control over doping concentration and geometrical tolerances to make CBIC possible. This fabrication technology offers the vertical structure and closely-matched characteristics for both the NPN and PNP transistors, without the disadvantages associated with the SBC vertical PNP.

A cross-section of typical CBIC npn and pnp transistors is shown in Figure 2.6. Beginning with a p-type substrate, ISOTUB N isolates the pnp collector from the substrate and reduces the npn collector-substrate capacitance. The BURIED N and COLLECT N form the collectors of the npn transistors, while the BURIED P and COLLECT P form the collectors of the pnp transistors. For the pnp and npn transistors the bases are formed by the BASE N and BASE P regions, respectively. The transistor fabrication is completed with the emitters being formed by the EMITTER P and EMITTER N regions for the pnp and npn transistors, respectively. The resistors are fabricated during either the BASE P or EMITTER P process step, depending on the desired sheet resistance. Finally, the junction passivation consists of an SiO_2 - Si_3N_4 layer.

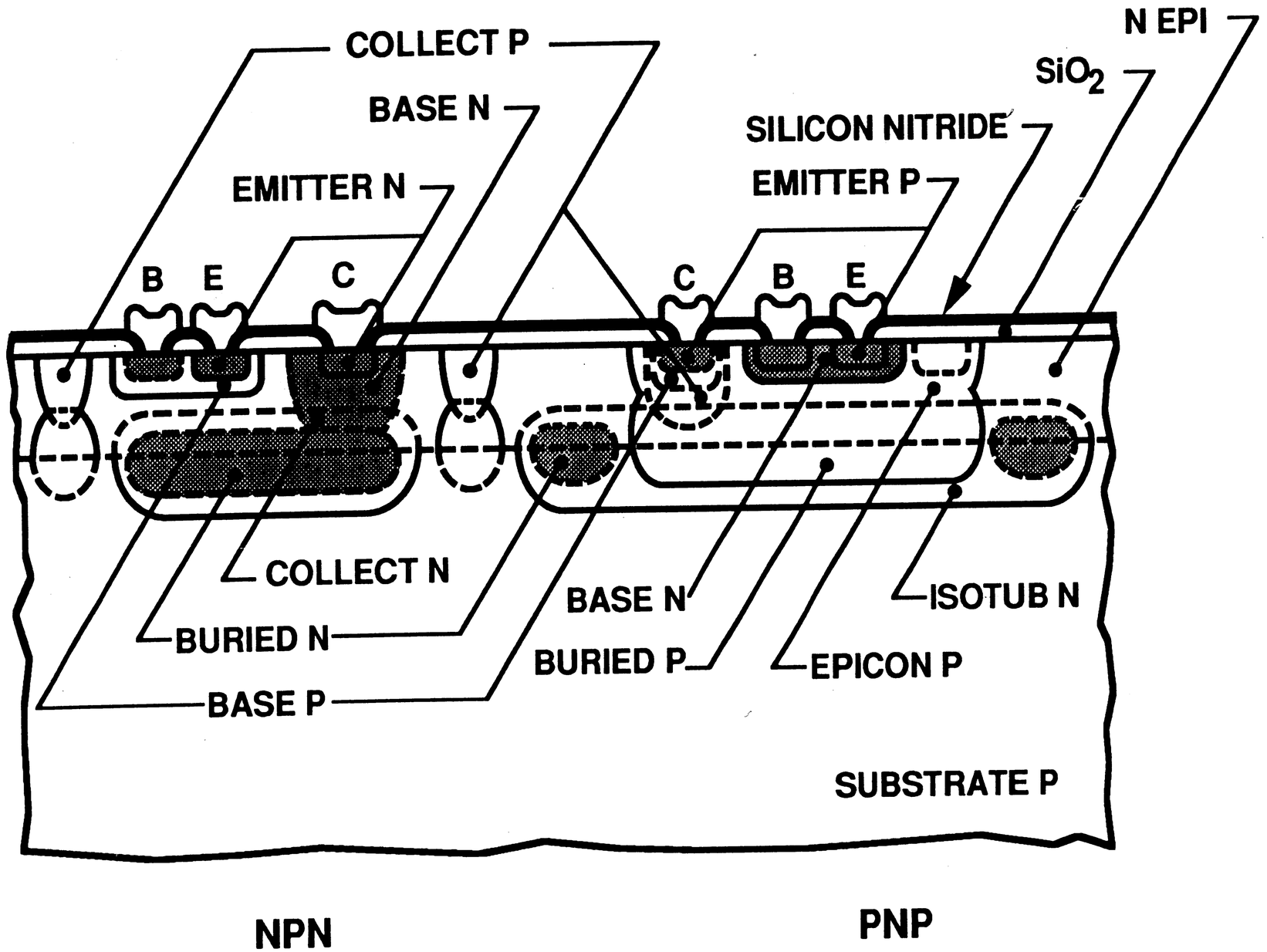


Figure 2.6 Typical CBIC Transistor Structures

The needs for improved telecommunications circuits spawned a variety of technological enhancements to the basic CBIC process. Included are: I^2L (integrated injection logic) gates; high-voltage capability; laser trimmable thin-film resistors; precision JFETs; and, two-level metalization.

The most recent enhancements have been spawned by the need for higher operating frequencies, and have resulted in greatly improved speed capability. The latest generation CBIC-U technology that is employed in the research for this thesis is a fabrication process which provides NPN transistors typically having a beta of 100 and an f_T of 4.5 GHz, and the PNP transistors having a beta of 40 and an f_T of 3.7 GHz.

2.2 COMPONENT CHARACTERISTICS

The task of designing a high-performance integrated circuit involves addressing two areas to achieve a prescribed behavior: (1) circuit (electrical) design; and (2) layout (physical) design. The methodology of IC design is such that these two phases are intimately meshed. Indeed, the salient performance characteristics of analog circuits can be optimized only by consideration of both aspects.

The design and analysis of the VCO circuit for this thesis is presented in detail in a later chapter. Typically the synthesis and "hand analysis" precede computer simulations. In order to achieve success during the early design phase, it is necessary to adhere to a principal of using the simplest model required that will result in the required accuracy. In addition, it is during the hand analysis that the greatest intuitive understanding of the circuit's function is gained. And it is this intuitive understanding of the circuit's function that allows subsequent iterative design revisions to be carried out and result in optimized performance.

In the design and analysis presented in later chapters, various component

parameters will be used as necessary. The most meaningful characteristics for the synthesis and hand analysis are presented in Appendix A.

2.3 ADVICE SIMULATION MODELS

An integral part of the design process is the use of computer simulations. At any point in the cycle, performance of the circuit can be precisely determined when necessary. And in later stages of the design cycle when subcircuits are connected to create higher-level functions, computer simulation is essential for verifying a circuit's behavior.

The circuit simulator used throughout this work is ADVICE[19] (Aid in Design Verification for Integrated Circuit Engineering). It is AT&T's version of the popular SPICE program, and it provides accurate device-level simulations of the electrical characteristics of analog and digital circuits. ADVICE performs dc steady-state analysis, transient time-domain analysis and small-signal frequency domain analysis. For primary input the program requires two things. The first is a "netlist," which defines the circuit of interest as an interconnection of circuit elements. Each element type (e.g., resistors, transistors, capacitors, etc.) has electrical characteristics that are determined by its model. The second input requirement for ADVICE is a library of device models. These inputs then allow the highly accurate solution of the matrix equations relating circuit voltages, currents and resistances.

The accurate characterization of the silicon devices and the extraction of the model parameters[20,21] is an on-going task carried out by process and manufacturing engineers[22]. This ensures that the designer has access to the models that accurately reflect the range of manufacturing capability of the factory. Thus in addition to device models that represent the nominal manufacturing process, worst-case variations of each parameter must be provided. The manufacturing tolerances of the various process parameters depend primarily on

two factors. The first is variation due to implant and diffusion effects, and the second is variation due to photolithographic and etching effects. By simulating the design over the expected range of process variations, the integrated circuit design can be guaranteed robust.

While the process "recipe" for the fabrication of the CBIC-U technology is proprietary information, the model parameters are available for use by designers. A comprehensive tabulation of the model parameter definitions and their nominal and worst-case variations are available in Appendix B.

3. DESIGN OF THE VCO CIRCUIT

This chapter will describe the design of the voltage-controlled oscillator circuit. As explained in Chapter 1, the emitter-coupled architecture was found to be the best choice for implementing an oscillator in a high-frequency bipolar technology. Shown in Figure 3.1 is a functional representation of the UHF VCO circuit.

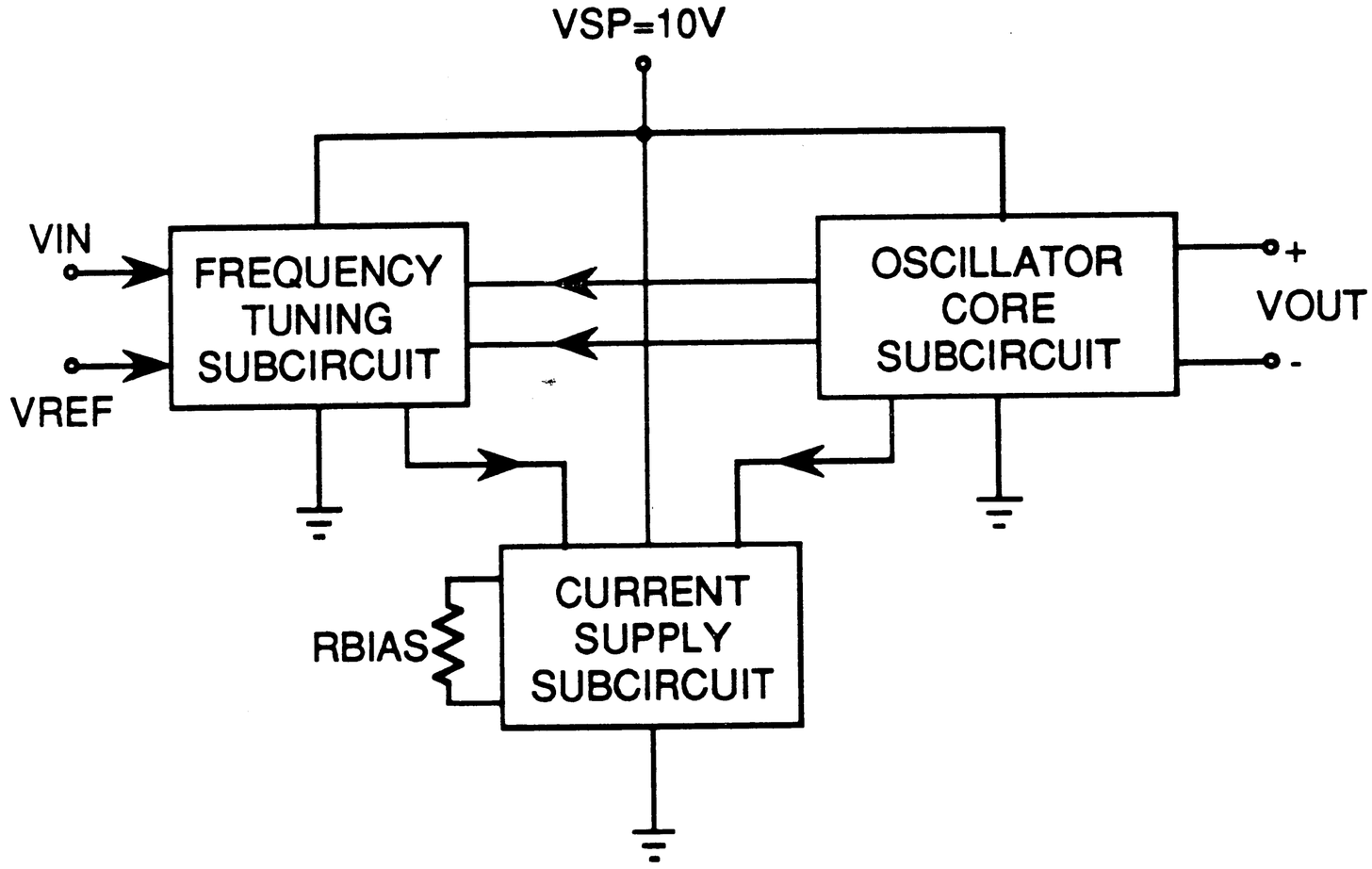


Figure 3.1 Voltage-Controlled Oscillator Block Diagram

The VCO consists of three subcircuits and operates from a single 10V power supply. It optionally requires only one external component, the bias-setting resistor. The use of an external bias resistor allows the center frequency to be accurately trimmed to compensate for process variations. The oscillator core subcircuit contains the emitter-coupled multivibrator and provides the output waveform. Adjustment of the oscillation frequency is accomplished by means of a differential DC control voltage applied to the frequency tuning subcircuit. The

current supply subcircuit uses a zener reference to provide a stable bias current to the other subcircuits. The operation of the complete circuit was optimized for the highest possible oscillating frequency for the CBIC-U technology. The design considerations to accomplish this will be described on a subcircuit basis in the next several sections of this chapter, and operation of the complete voltage-controlled oscillator will be presented in the last section of this chapter.

3.1 OSCILLATOR CORE SUBCIRCUIT

The architecture chosen to implement the oscillator core subcircuit is the emitter-coupled multivibrator. As explained in Chapter 1, this circuit type has the best attributes for implementation in a high-frequency bipolar technology. The schematic shown in Figure 3.2 is a simplified version of the circuit that forms the core of the UHF VCO circuit.

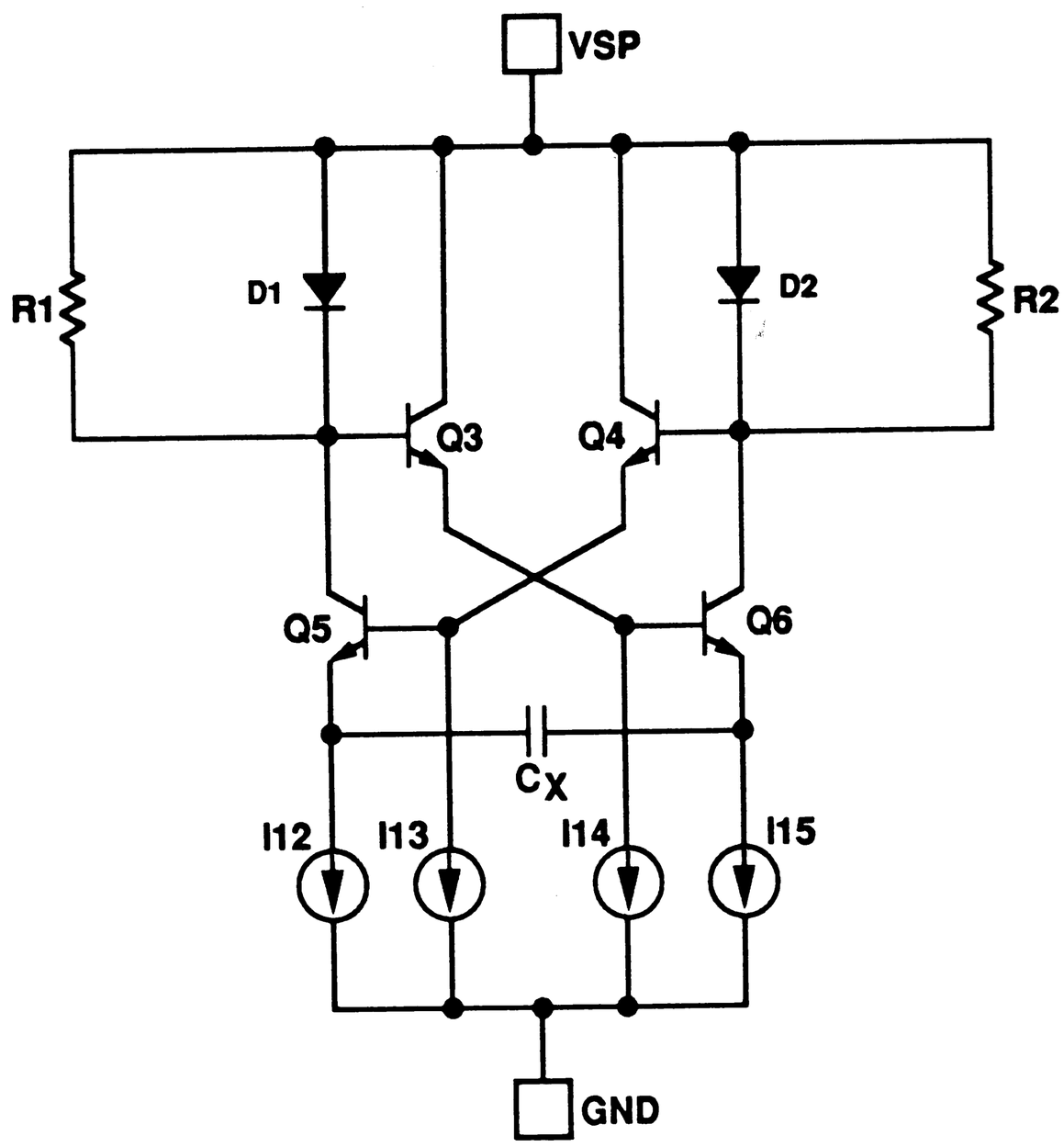


Figure 3.2 Basic Oscillator Core Subcircuit

In Figure 3.3 the circuit is shown in its first half-cycle state where Q5 is off and Q6 is on.

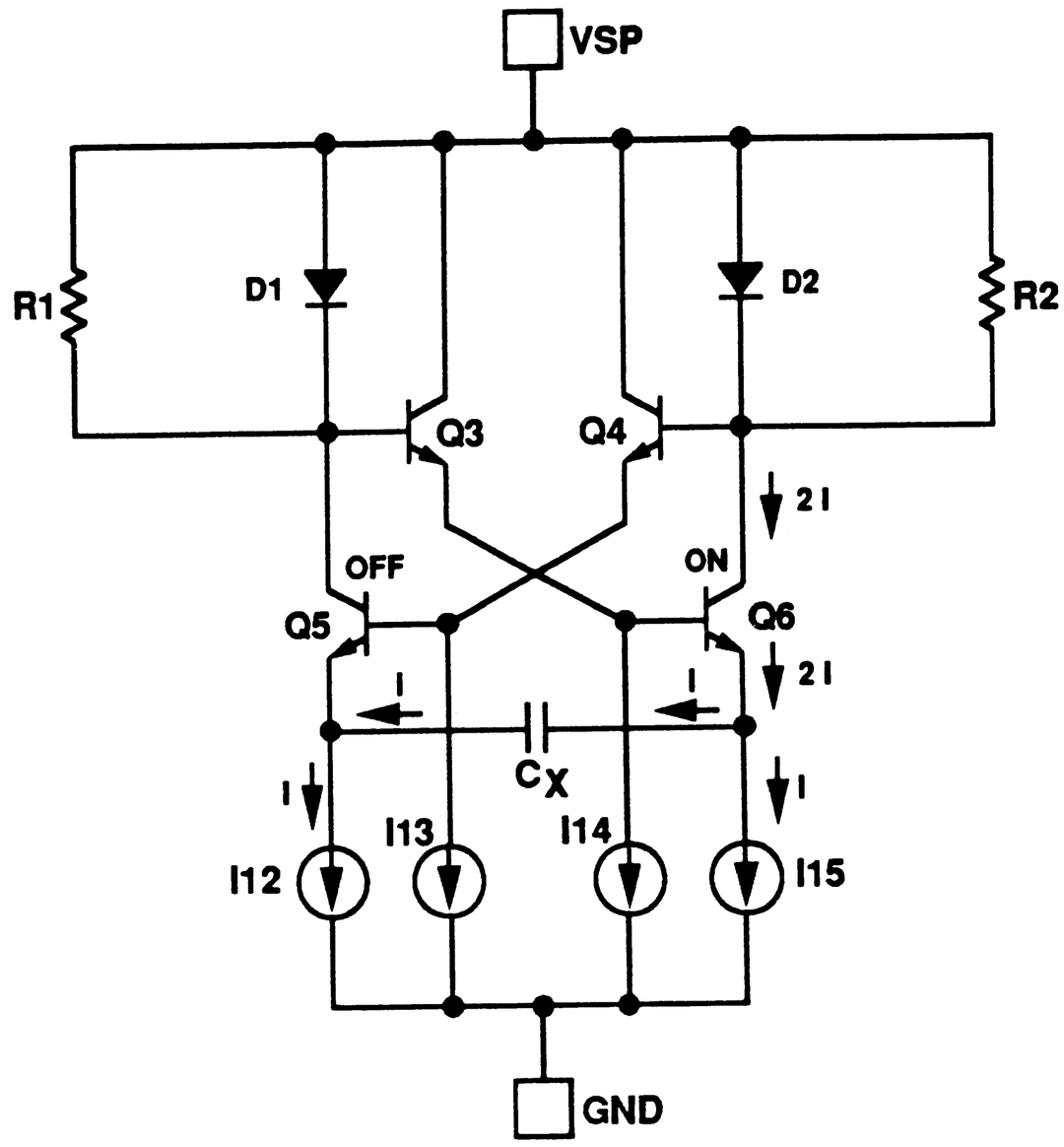


Figure 3.3 First Half-Cycle of Oscillation

Constant-current sources I12-I15 are sinking the timing current I. The base of Q3 is pulled up to VSP through R1 and thus the base of Q6 is at VSP-V_{BE} volts and the right-hand side of the timing capacitor Cx is at VSP-2V_{BE} volts. The voltage drop across R2 is clamped by diode D2, so the base of Q4 is at VSP-V_{BE} volts. Thus the base of Q5 is at VSP-2V_{BE} volts. Current source I12 is sinking the timing current I which begins to slew the emitter voltage of Q5 in a negative direction. When the voltage at the left-hand side of timing capacitor Cx drops to VSP-3V_{BE} volts, Q5 begins to conduct. As Q5 turns on, the resulting voltage drop across R1 acts through Q3 to remove the base drive from Q6. As Q6 is turned off by this action, its collector voltage rapidly rises one V_{BE} through the pull-up action of R2. Appearing

through the base-emitter junctions of Q4 and Q5, this one-V_{BE} step appears at the emitter of Q6 after being transmitted through Cx. Resistors R1 and R2 are both 2k Ω, a value chosen to meet two criteria: It must be small enough to act as a reliable pull-up for the transistor base when the diode is off. Also, it must divert a only small percentage (< 10%) of the current when the diode is on.

At this point begins its second half-cycle state as shown in Figure 3.4.

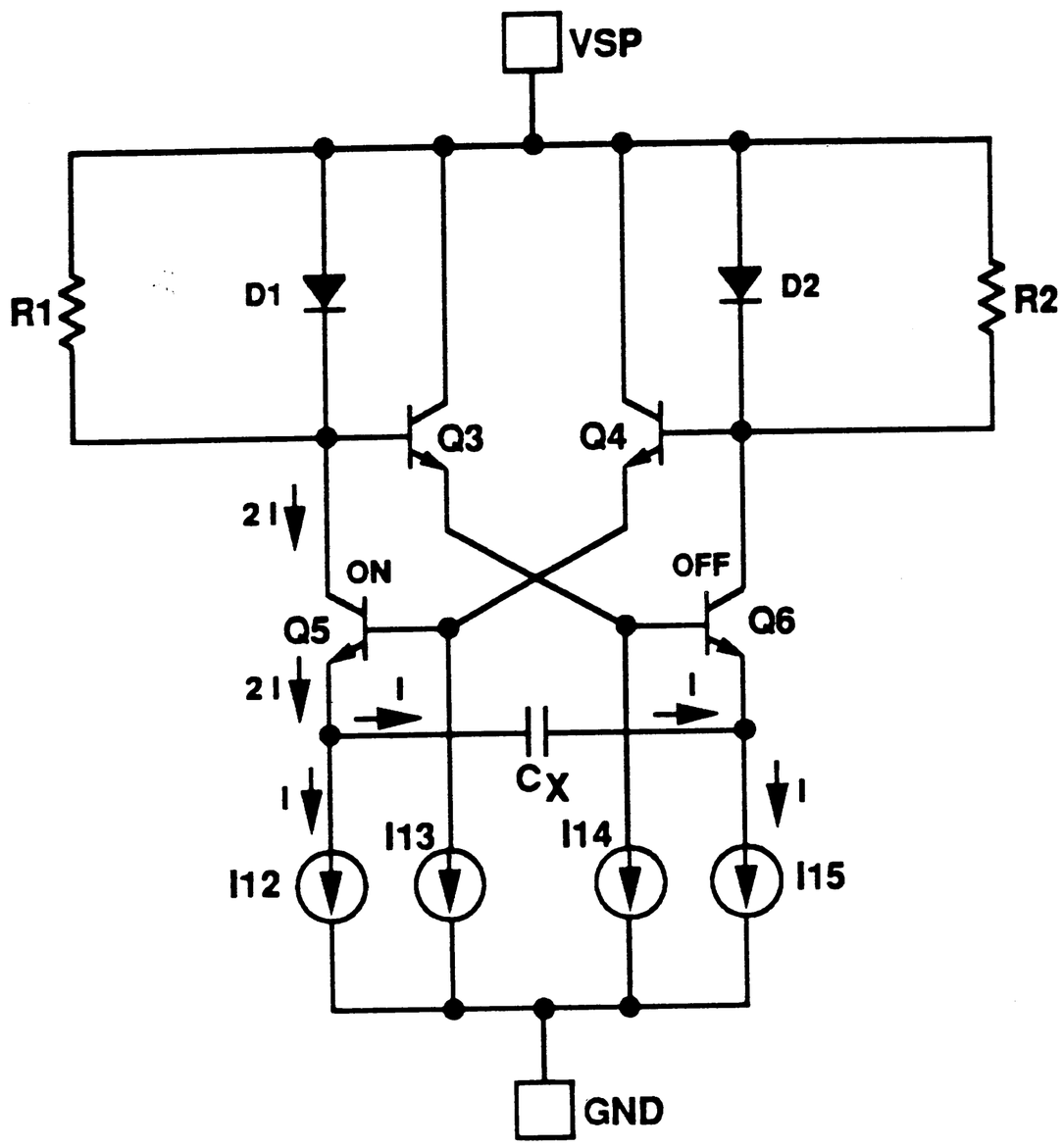


Figure 3.4 Second Half-Cycle of Oscillation

The circuit is symmetrical and the action during this second half-cycle is identical to the first half-cycle, only involving the components that are counterparts to those described above. Note at the beginning of the second half-cycle that the emitter voltage of Q6 is one V_{BE} above its base voltage. This means that its emitter must slew $2V_{BE}$ volts before it again conducts.

The action of the oscillator core subcircuit is depicted in the waveforms

shown in Figure 3.5.

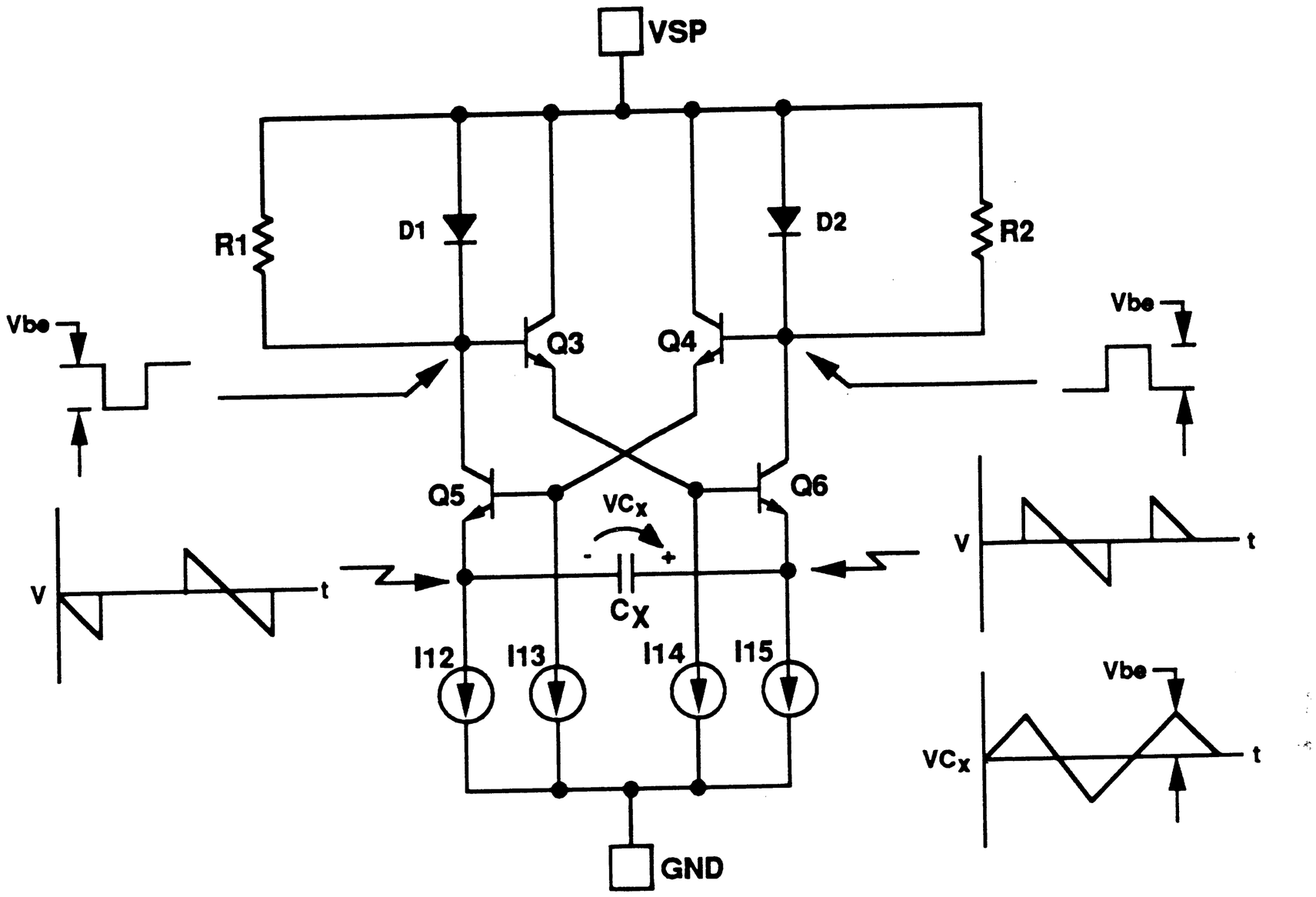


Figure 3.5 Ideal Oscillator Waveforms

The voltage across timing capacitor Cx is a triangular waveform since the charging/discharging action is accomplished with constant-current sources I12 and I15. The magnitude of V_{Cx} is $2V_{BE}$ volts peak-to-peak, and one period T requires a total excursion of $4V_{BE}$ volts across Cx. Since the slewing of the voltage is produced by the timing current I, the period of one cycle is

$$T = (4V_{BE}Cx) / I \qquad (3.1)$$

This circuit contains only NPN transistors (which have a slightly higher frequency capability than the PNP devices), is non-saturating and has small voltage swings. To further optimize this circuit for high speed operation, Equation

3.1 shows that this can be accomplished by utilizing a high timing current I in conjunction with a small value timing capacitor Cx. From the electrical characteristics for the CBIC-U components in Appendix A, it can be seen that the peak f_T for the NPN transistors occurs in the 4 to 5 mA range. The corresponding base-emitter voltage at this operating point is about 0.82 V, and the ALA201 linear array's smallest metal-to-metal capacitor is 1 pF. Therefore the operating frequency for these nominal values is 1.2 GHz. It should be noted here that extensive simulations invoiving the complete circuit attempting to attain a higher frequency indicated that 1.2 GHz is the maximum center frequency for reliable operation. These simulations involved increasing the timing current, reducing the value of the timing capacitor, etc. It was concluded from worst-case analyses that operation above 1.2 GHz would be unreliable given the manufacturing tolerances for CBIC-U.

A high-quality output signal should be stable and provide a duty cycle of 50%. To accommodate the former requirement, the constant-current source which provides the timing current must be stable. This is addressed in the next section of this chapter where the design of the current supply subcircuit is presented. To accomplish the latter requirement for a high-quality output signal, symmetrical operation of the circuit is necessary. This is highly dependent on the matching of the base-emitter voltages between the left-hand branch (Q1,Q3 and Q5) and right-hand branch (Q2, Q4 and Q6) of the oscillator core. In order to optimize the matching, the design of the chip layout (Chapter 4) must be such that these transistors are placed symmetrically about a common point.

The optimization of the circuit design based on simulations using ADVICE will be presented in later sections of this thesis. These simulations address the effect on circuit performance that processing variations and layout parasitics may have.

3.2 CURRENT SUPPLY SUBCIRCUIT

The design of the bias circuitry of any integrated circuit is critical because it determines the internal voltage and current levels during operation. The constraints and limitations imposed by the fabrication technology must be overcome, resulting in the successful operation of the IC.

Although the base-emitter voltage-referenced bias circuit family (e.g., the Wilson and Widlar current sources) provides an elegantly simple method to obtain multiple currents, they have poor performance with respect to temperature variation. Since V_{BE} has a temperature coefficient of about -2 mV/°C, implementations of V_{BE}-referenced bias circuits[23] have typical output current temperature coefficients (TC_O) in the range of several thousand parts per million (PPM).

Since the oscillator core subcircuit requires a constant timing current to provide a quality output signal, a TC_O as large as that mentioned above would be unacceptable. A popular approach to overcome this difficulty is to employ a "band-gap" voltage reference. However, this reference circuit has the disadvantage of utilizing a relatively high component count. This impacts the cost by requiring a larger die size (and its corresponding lower yield), and impacts power dissipation by virtue of its greater number of active components. Also, band-gap references by themselves only provide a reference voltage which then must somehow be converted to a current for application in the UHF VCO.

Another approach to temperature-independent biasing is the use of the zener-referenced bias circuit. It has the technical advantages of a smaller chip area requirement and lower power consumption by virtue of its smaller component utilization. The use of this reference scheme in our UHF VCO implementation could prove the viability of using this technique in the CBIC-U technology. One possible disadvantage to using a zener reference in monolithic technology is that since the

reference is generated by a breakdown phenomenon[24], noise injection into other portions of the die may occur. However, the noise is likely to be no more than 50 uV and less than 10 kHz[25]. Therefore it would have no effect on the UHF VCO operation which has voltage swings over 500 mV at 1.2 GHz.

3.2.1 BASIC ZENER DIODE BIAS CIRCUIT

The basic zener diode bias circuit is shown in Figure 3.6.

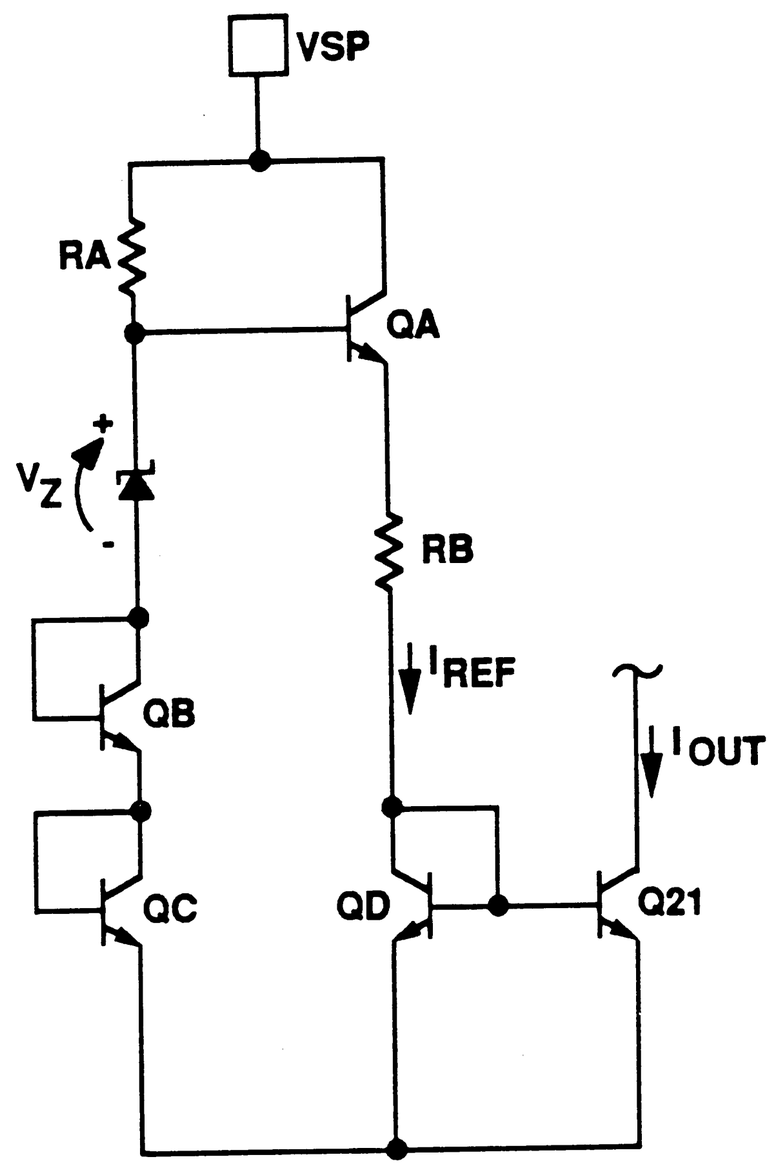


Figure 3.6 Basic Zener Diode Bias Circuit

For the transistor structure that will be employed in the CBIC-U technology, a breakdown voltage of about 5.6 volts will be realized. With resistor RA providing the current to bias diode DA and transistors QB and QC, the equation around the loop formed by DA, QB, QC, QD, RB and QA is

$$V_{BE(QA)} + I_{REF}R_{BIAS} + V_{BE(QD)} = V_Z + V_{BE(QB)} + V_{BE(QC)} \quad (3.2)$$

Since the transistors will all have approximately the same V_{BE}, the reference current is

$$I_{REF} = V_Z / R_{BIAS} \quad (3.3)$$

The current mirror formed by QD and Q21 provides an output current

$$I_{OUT} = V_Z / R_{BIAS} \quad (3.4)$$

This circuit produces an output current that has eliminated the effects of temperature variation of V_{BE}. However, the circuit may have a temperature variation due to the temperature coefficients of the resistor value and zener voltage. Indeed, TC_O values in the range of 375-760 PPM were observed during ADVICE simulation of the circuit, depending on the component values. In order to optimize the circuit to obtain a near-zero TC_O, the temperature compensation for the circuit will involve scaling the drift sources. By proper design the different magnitude and polarity drifts can be made to cancel to realize this goal.

3.2.2 COMPONENT CHARACTERIZATION

In order to execute the design of a temperature-compensated current biasing circuit, it is necessary to model each drift source. The three component parameters that will be modeled as a function of temperature are: the base-emitter voltage in the on state; the resistance of the 1 kΩ per square diffused resistors; and, the zener voltage.

The temperature coefficient of V_{BE} was obtained for an NU320PA 1X NPN transistor, the type used throughout the UHF VCO, using the test set-up illustrated in Figure 3.7.

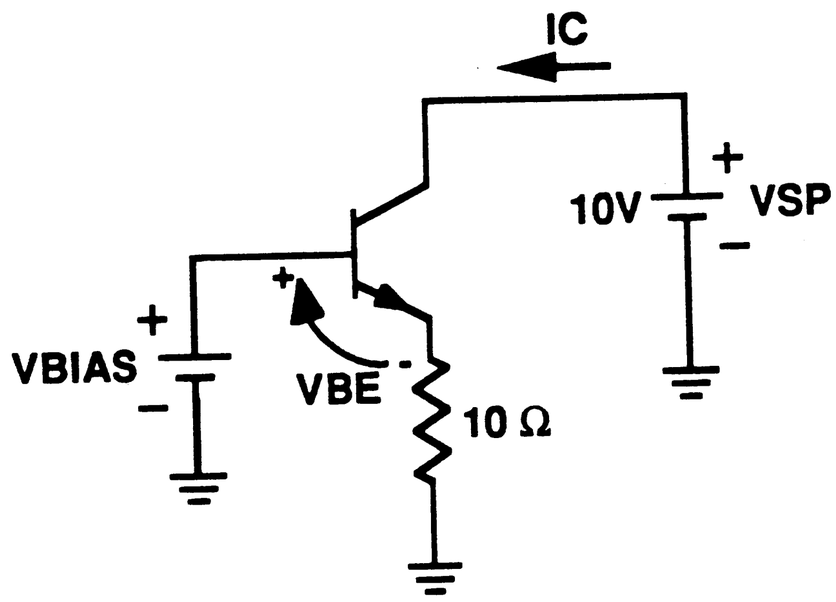


Figure 3.7 VBE Test Circuit

With a constant collector voltage, V_{BIAS} was adjusted to keep the collector current constant at I_C = 1.00 mA as the temperature was varied from 0 to 100 °C. The values of V_{BE} as a function of temperature are shown in Figure 3.8. The equation for this plot is

$$V_{BE} = (-1.660E\text{-}3\ V/°C)T = 0.818\ V \qquad (3.5)$$

with a coefficient of fit R^2 = 1.00. Therefore, the temperature coefficient for V_{BE} is TC_V = -1.660 mV / °C.

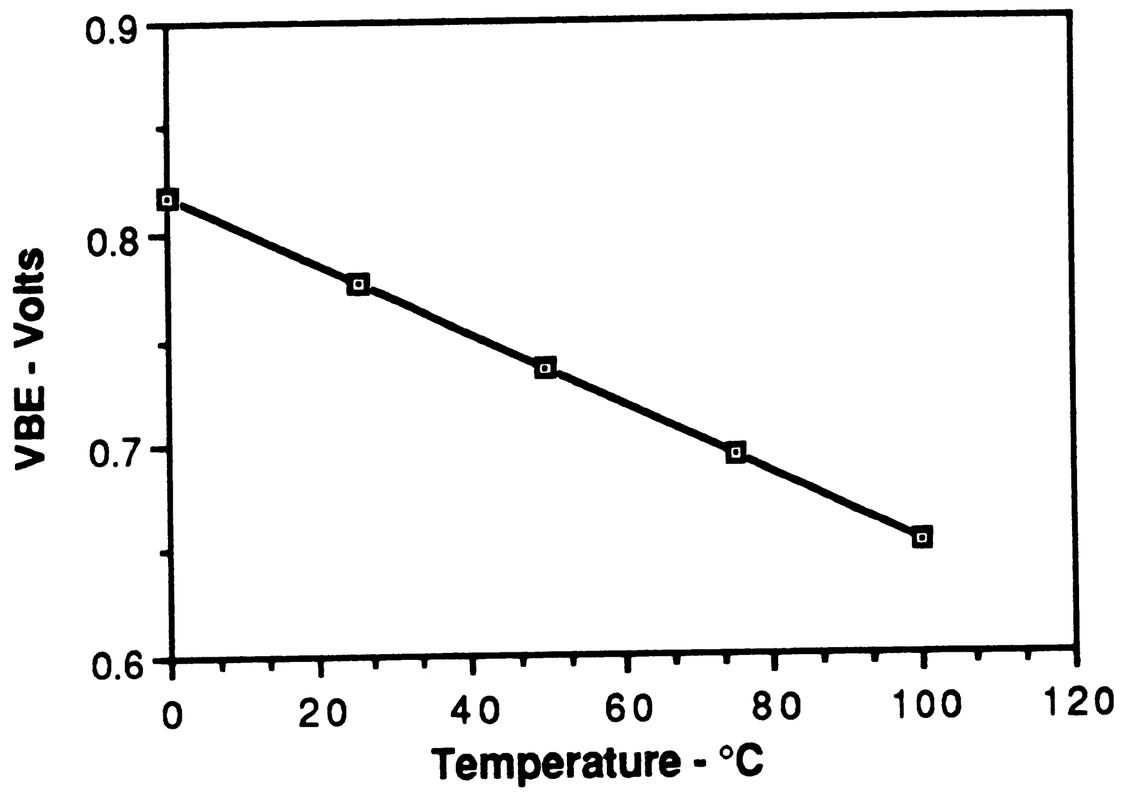


Figure 3.8 VBE(T) for 1X NPN

The temperature coefficient for the resistance of the diffused resistors was obtained using the test set-up shown in Figure 3.9.

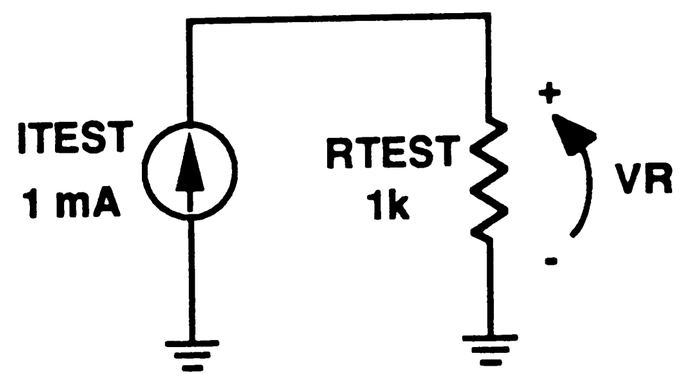


Figure 3.9 R(T) Test Circuit

With a constant test current of 1 mA, V_R was measured as the temperature was

varied from 0 to 100 °C. The values of resistance obtained as a function of temperature[26] are shown on Figure 3.10.

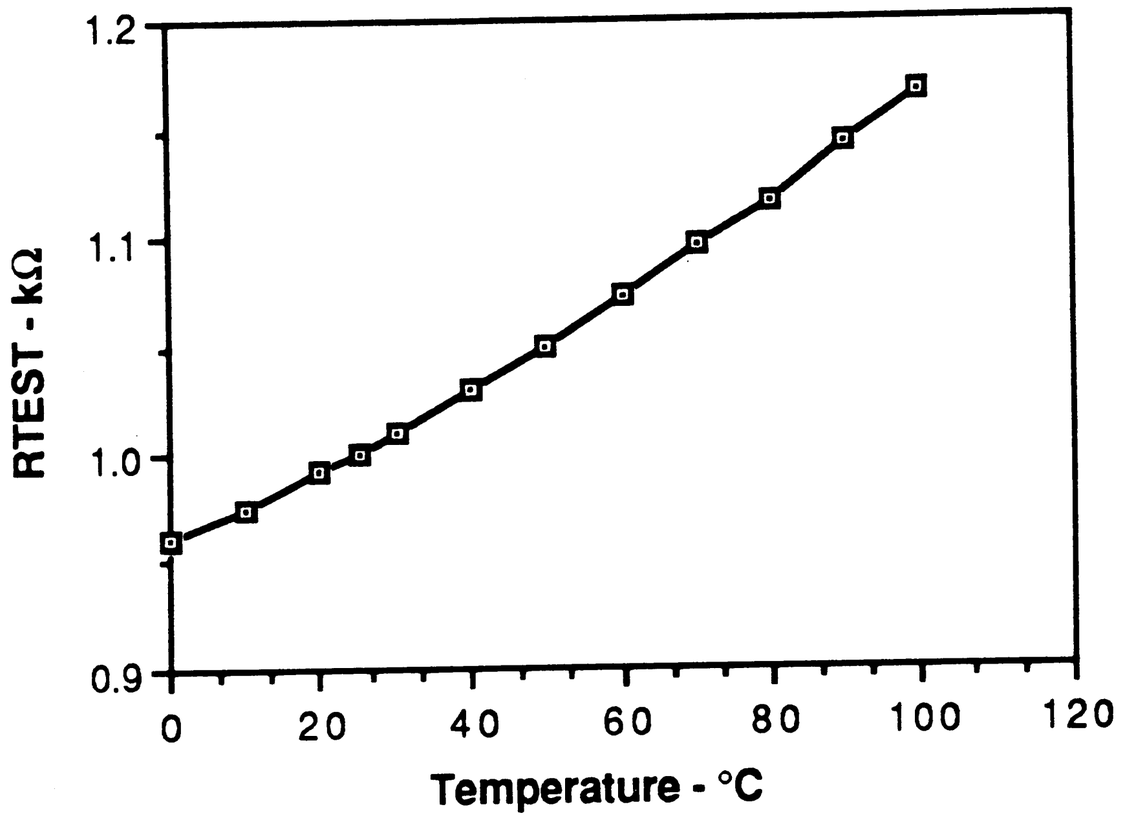


Figure 3.10 R(T) for Diffused Resistor

This plot is non-linear, and when fitted with a second-order polynomial the equation is

$$R_{1k} = 959\ \Omega + (1.564\text{E-}3\ \Omega / °C)T + (5.276\text{E-}6\ \Omega / °C^2)T^2 \qquad (3.6)$$

with a coefficient of fit $R^2 = 0.995$. Therefore, the resistor temperature coefficient (for hand analysis purposes) is $TC_R = +1564$ PPM.

The zener diode will need both an electrical model and a temperature coefficient developed. For the electrical model, it was previously determined that the "sharpest" emitter-base junction breakdown mode was obtained with the

collector shorted to the emitter[27]. By using the BV_{EBC} mode, a soft knee is avoided in the characteristic and the behavior will more accurately resemble a constant-voltage source over a wider range of operating currents.

There was no model available for the zener diode because ADVICE is incapable of modeling a breakdown phenomenon. In order to develop an equivalent model for the emitter-base breakdown phenomenon, a PU320PA 1X PNP transistor will be characterized to extract the appropriate parameters. Using the test set-up shown in Figure 3.11 at room temperature

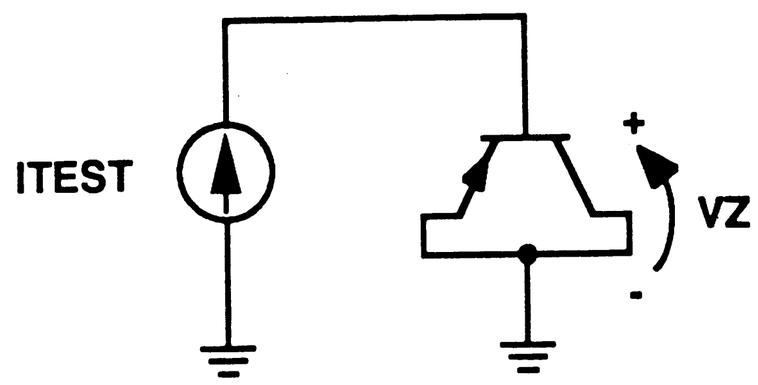


Figure 3.11 Zener Voltage Test Circuit

the breakdown voltage as a function of test current was obtained as shown in Figure 3.12. The function is very linear in the mid-range current region (the UHF VCO will operate in this range), and can be described by the equation

$$V_Z(T = 25\ °C) = (25.5\ V / A)I_{TEST} + 5.60\ V \qquad (3.7)$$

with a coefficient of fit $R^2 = 0.986$.

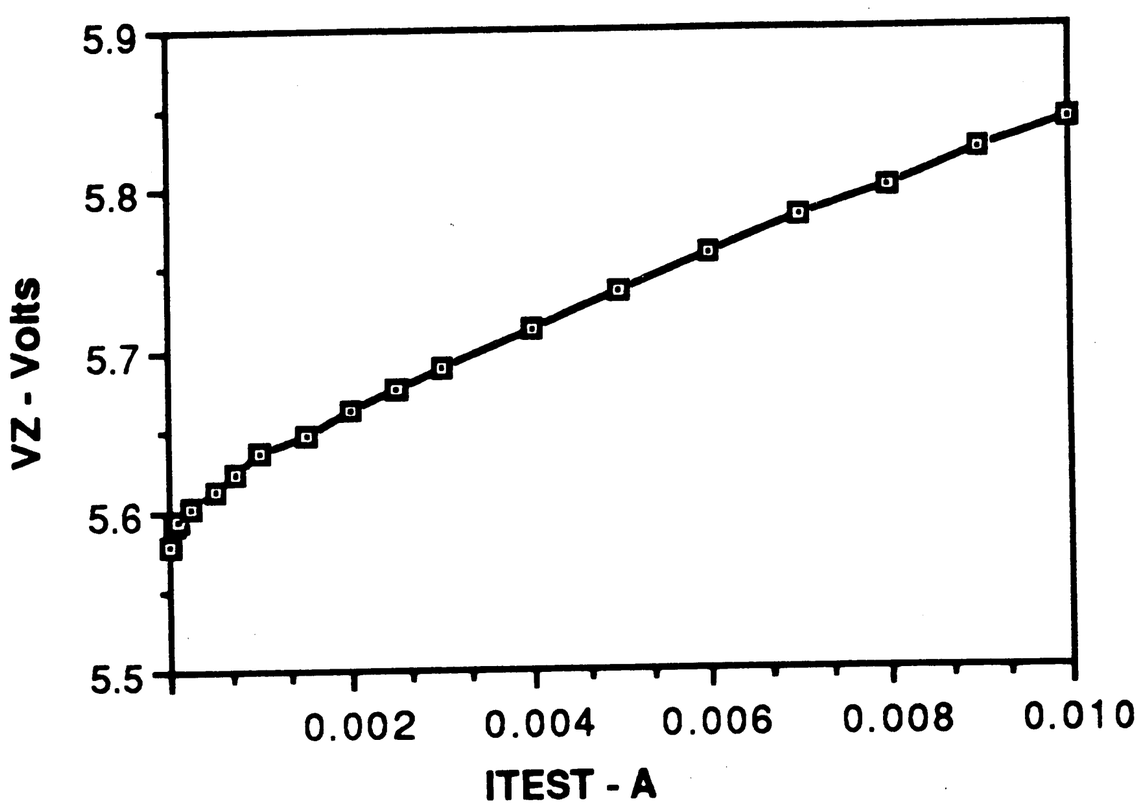
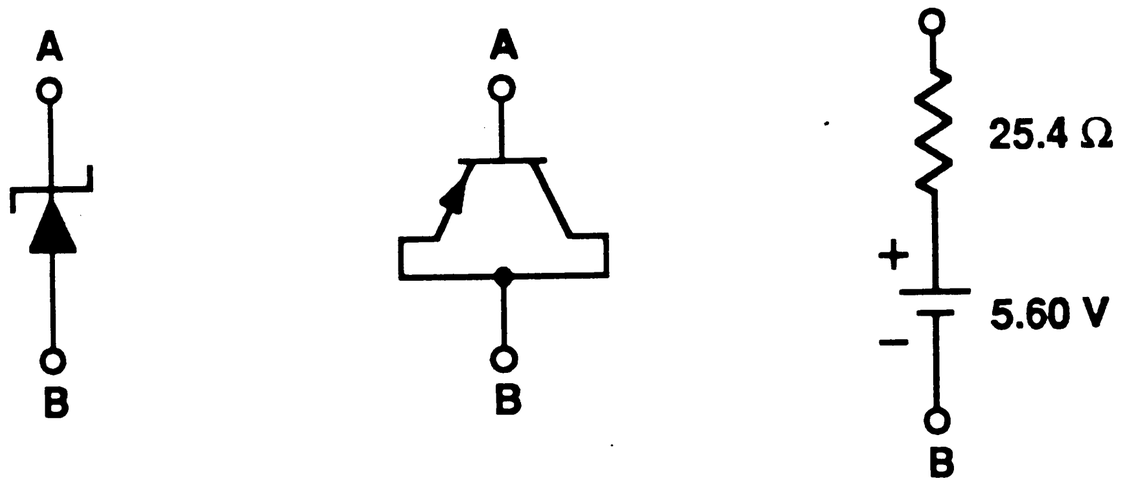


Figure 3.12 VZ(T=25) for 1X PNP

The slope of this line is the zener series resistance and the y-intercept will be the temperature-dependent voltage source value for the equivalent model shown in Figure 3.13.



Zener Diode **CBIC-U Implementation** **ADVICE Model**

Figure 3.13 CBIC-U Zener Diode Model

This equivalent model will be used for the CBIC-U emitter-base zener breakdown

in all ADVICE simulations.

The temperature coefficient of the voltage source was obtained with the same test set-up, only now a constant 1 mA test current was applied to the device as the temperature was varied from 0 - 100 °C. The resulting data shown in Figure 3.14 is very linear.

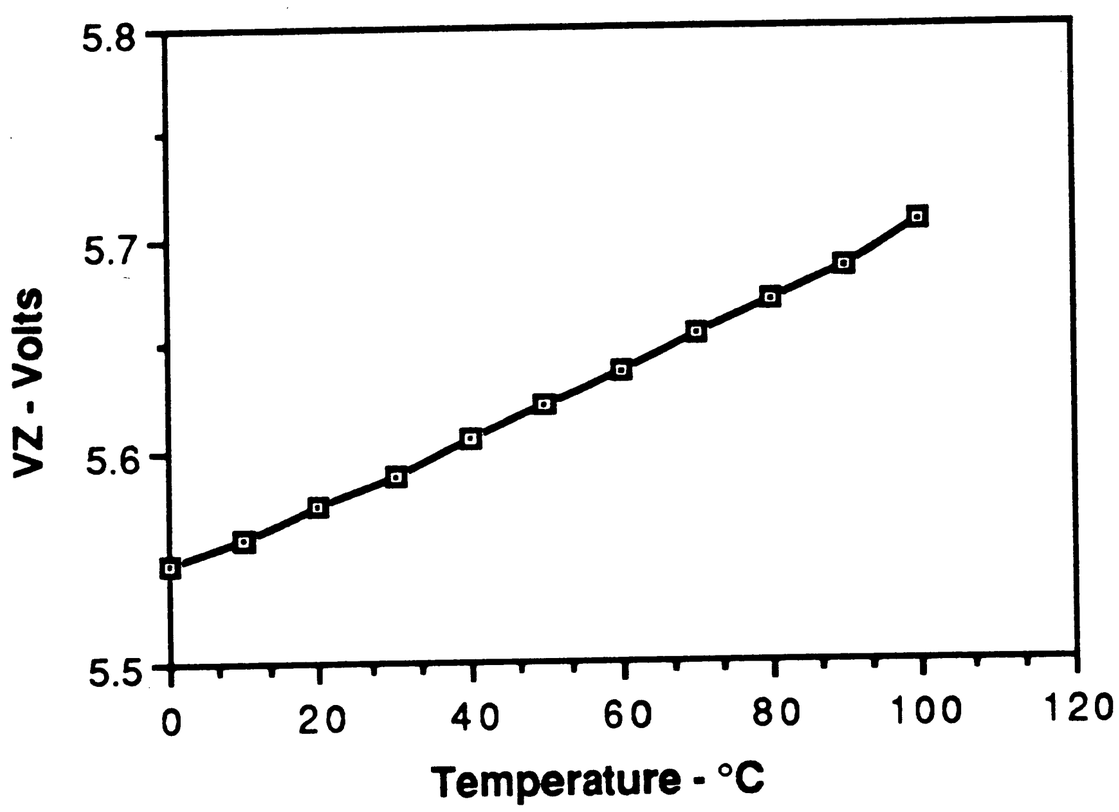


Figure 3.14 VZ(T) for 1X PNP

The equation for this plot is

$$V_Z(T) = (1.60E\text{-}3\ V / °C)T + 5.543\ V \qquad (3.8)$$

with a coefficient of fit $R^2 = 0.998$. Thus the temperature coefficient for the zener voltage is $TC_Z = +1.60$ mV / °C. The temperature coefficient for the zener series resistance was not modeled because the value of Rz is much less than the other

resistors in the circuit and its effect would be negligible.

3.2.3 COMPLETE ZENER DIODE BIAS CIRCUIT

The design of the temperature-independent bias circuit will now be completed. In Section 3.2.1 it was found that in the basic zener diode bias circuit that V_{BE} cancellation resulted in an output current given by

$$I_{OUT} = V_Z / R_{BIAS} \tag{3.9}$$

However, I_{OUT} still would have a temperature coefficient because the temperature coefficients of Vz and R_{BIAS} are not equal. With the circuit in the form shown in Figure 3.6 simulations showed that TC_O was approximately 100 PPM. In order to yield a nominally zero temperature coefficient for I_{OUT} a negative-going drift component would need to be added to the circuit. By adding this to the branch of the circuit containing the zener diode, the total drift component for that branch can be scaled to null out the drift component for the remainder of the circuit. By employing the known negative temperature coefficient of V_{BE}, this goal was achieved.

The complete zener diode bias circuit necessary to drive the UHF VCO is shown in Figure 3.15. Several improvements and changes have been made to the basic circuit. By removing resistor RA from the basic circuit of Figure 3.6 and adding Q16 and Q17, the voltage at the base of Q18 is held more constant. This "self-bias" arrangement reduces the supply dependence of the output currents. Since the UHF VCO circuit requires five identical output currents produced by Q11 - Q15, the total base drive current for these five transistors would become a non-negligible part of I_{REF}. To provide the base drive necessary, "helper transistor" Q22 was added.

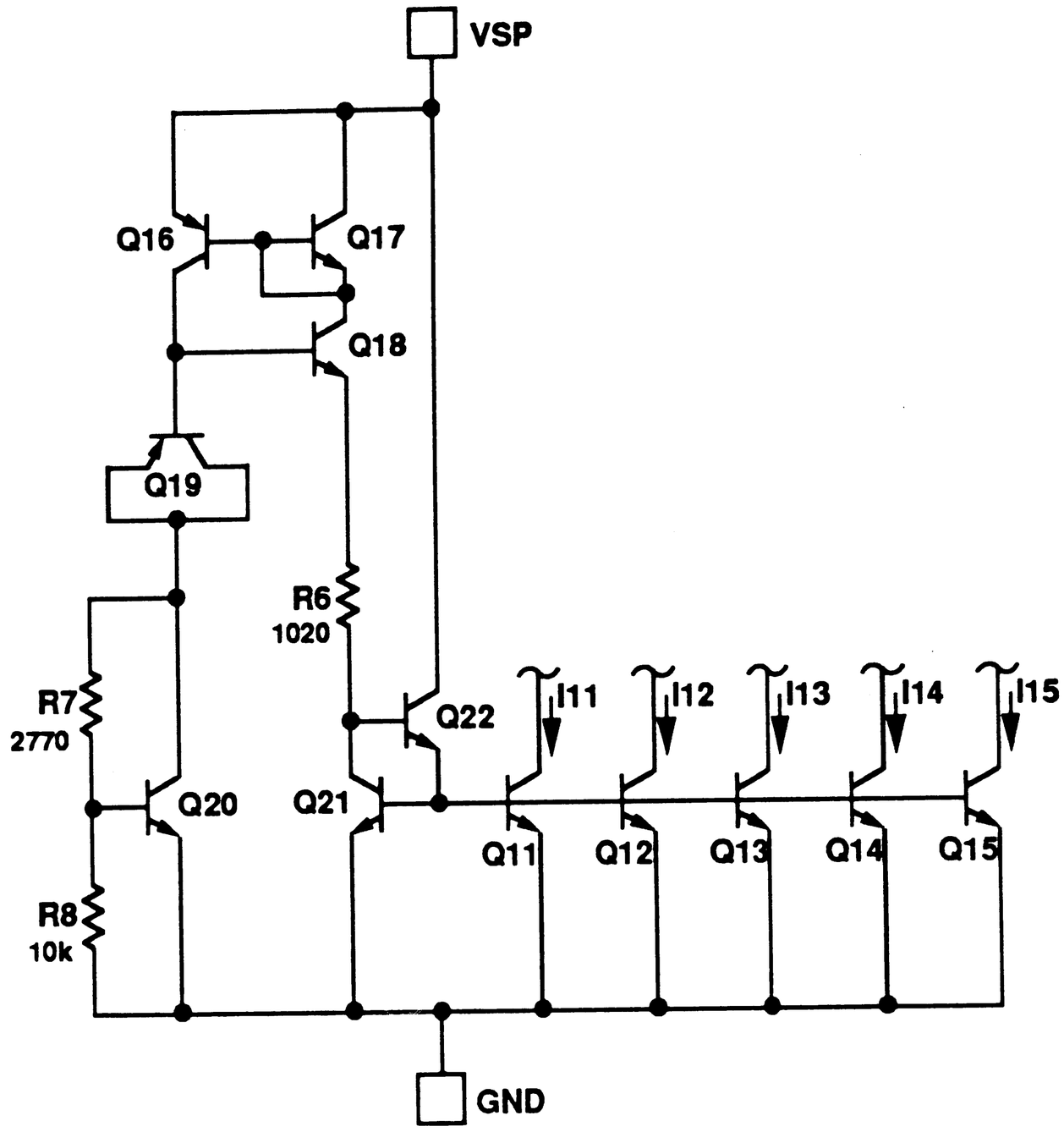


Figure 3.15 Complete Zener Diode Bias Circuit

The third modification to the basic circuit was the addition of the "V_{BE} multiplier" consisting of R7, R8 and Q20. As shown in Figure 3.16 the effective V_{BE} from this arrangement can be made any non-integer value of V_{BE} greater than one.

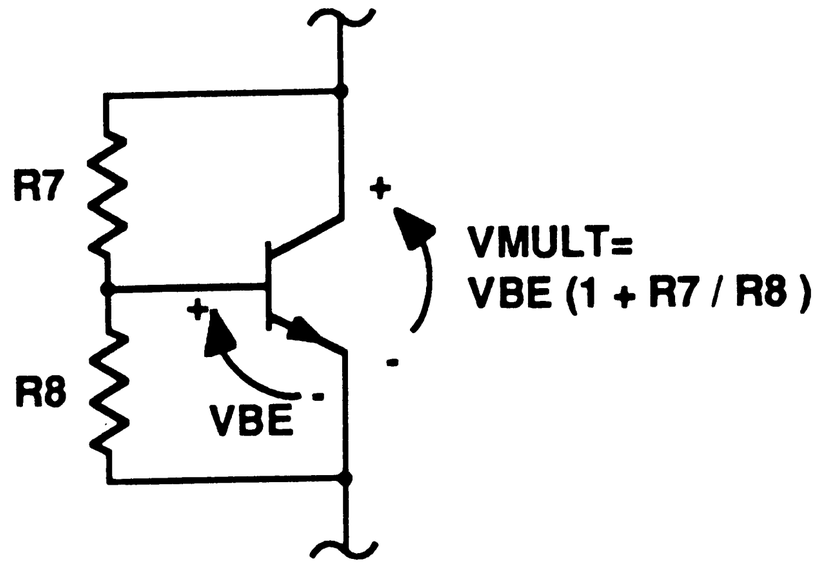


Figure 3.16 VBE Multiplier

By changing the ratio of R7 and R8, the V_{BE} multiplier will provide the properly scaled negative drift component necessary to obtain temperature-independent biasing.

The complete oscillator requires that bias currents I12 - I15 all be 5.00 mA for a center frequency of 1.2 GHz, and to achieve this the bias reference resistor R6 must be 1020 Ω. Satisfactory operation of the multiplier requires that the current through transistor Q20 be nearly equal to the reference current through R6. In order to accomplish this, the current through the R7-R8 path must be kept to a minimum. By choosing R8 as 10k Ω, this current is only 1.5% of the transistor collector current of about 5 mA. Optimization with ADVICE showed that in order to obtain the minimum output current temperature coefficient, the V_{BE} multiplication factor must be n = 1.277. Hence R7 must be 2770 Ω.

3.3 FREQUENCY TUNING SUBCIRCUIT

The frequency of operation of the oscillator is proportional to the timing current. In order to vary the frequency of oscillation it is necessary to vary the timing current. By providing circuitry that will sink current from each end of the timing

capacitor this can be accomplished. The circuit that will do this is shown in Figure 3.17.

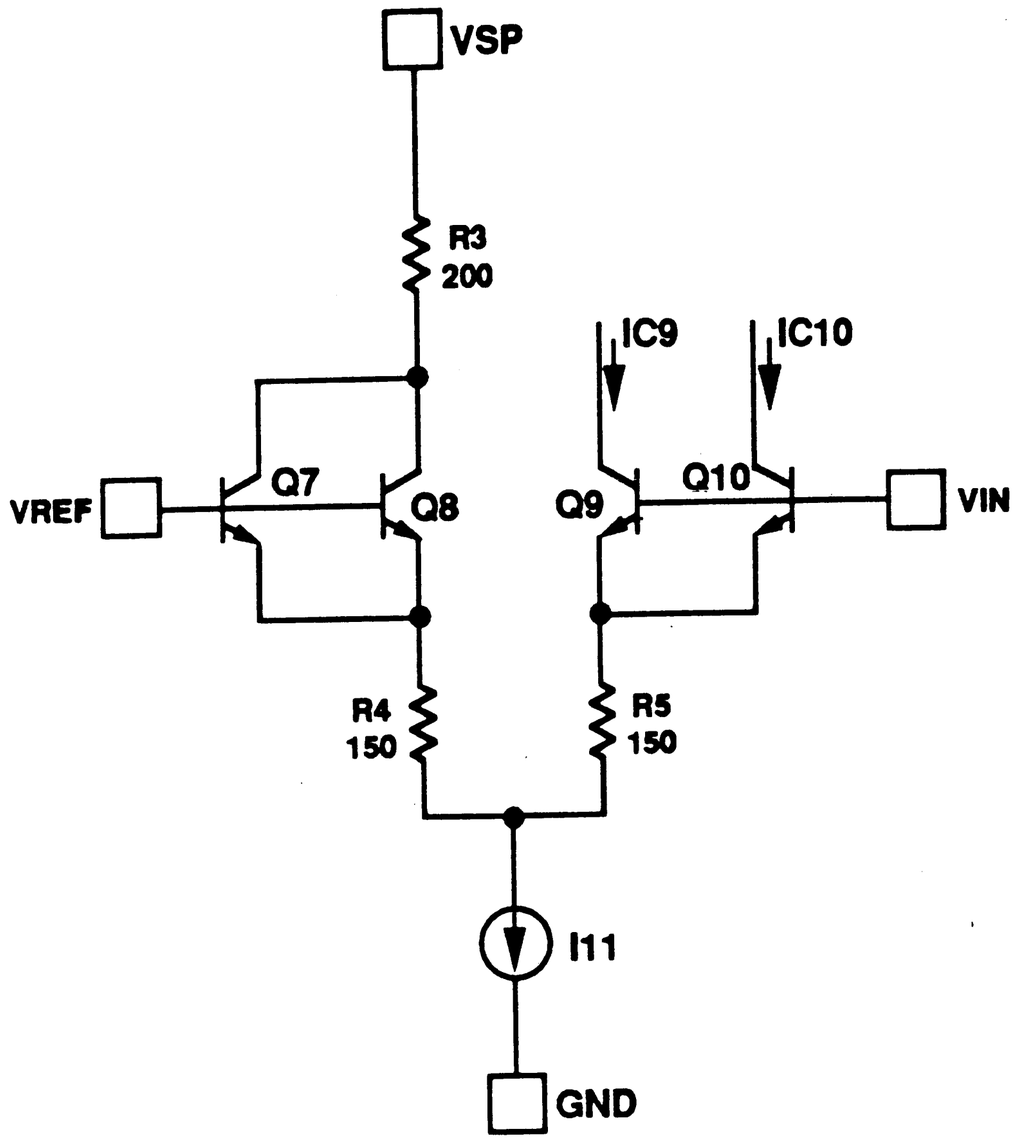


Figure 3.17 Frequency Tuning Subcircuit

It is a modified emitter-coupled pair with the collectors of Q9 and Q10 to be connected to the timing capacitor C_X. When $V_{IN} > V_{REF}$, Q9 and Q10 are on and Q7 and Q8 are off. In this state the collector currents of Q9 and Q10 sink a fraction of the timing current from C_X and reduce the oscillation frequency. When $V_{REF} > V_{IN}$, Q9 and Q10 are off and the oscillator operates at its highest frequency. The center frequency of the oscillator is defined to be when $V_{IN} = V_{REF}$.

The emitter degeneration resistors R4 and R5 modify the DC transfer characteristic of the emitter-coupled pair. With R4 = R5 = 150 Ω, the linear behavior

of the emitter-coupled pair is extended so that the range of input control voltage V_{IN} is from V_{REF} - 1 V to V_{REF} + 1 V. Without the emitter degeneration resistors, an unsatisfactorily narrow control range of about +/- 75 mV would be exhibited. These resistors introduce local feedback at the pair and extend the linear range of operation by an amount approximately equal to $I_{EE}R_E$. By extending the linear range of the frequency tuning control over a wider voltage range, the tuning function is more easily accomplished and more reliable (i.e., more noise immunity). Resistor R3 acts as a load for Q7 and Q8. This provides a voltage drop so that their collector voltage equals that of Q9 and Q10 (about 7.5 V) when $V_{IN} = V_{REF}$. This minimizes the effects of Early voltage (see Appendix A) to ensure symmetrical tuning about the center frequency.

3.4 FUNCTIONALITY SIMULATION OF COMPLETE VCO

The complete UHF VCO circuit is shown in Figure 3.18. Using ADVICE the functionality of the circuit was verified and found to meet all design criteria. Appendix C contains the netlist describing this circuit, and the DC operating point analysis is contained in Appendix D. Several key waveforms are shown in Figure 3.19 to illustrate the operation of the UHF VCO at 1.2 GHz. As can be seen the waveforms appear "rounded," or smoothed, rather than sharp as in Figure 3.5. This is typical for very high frequency circuit operation due to the filtering effects of the parasitic capacitances.

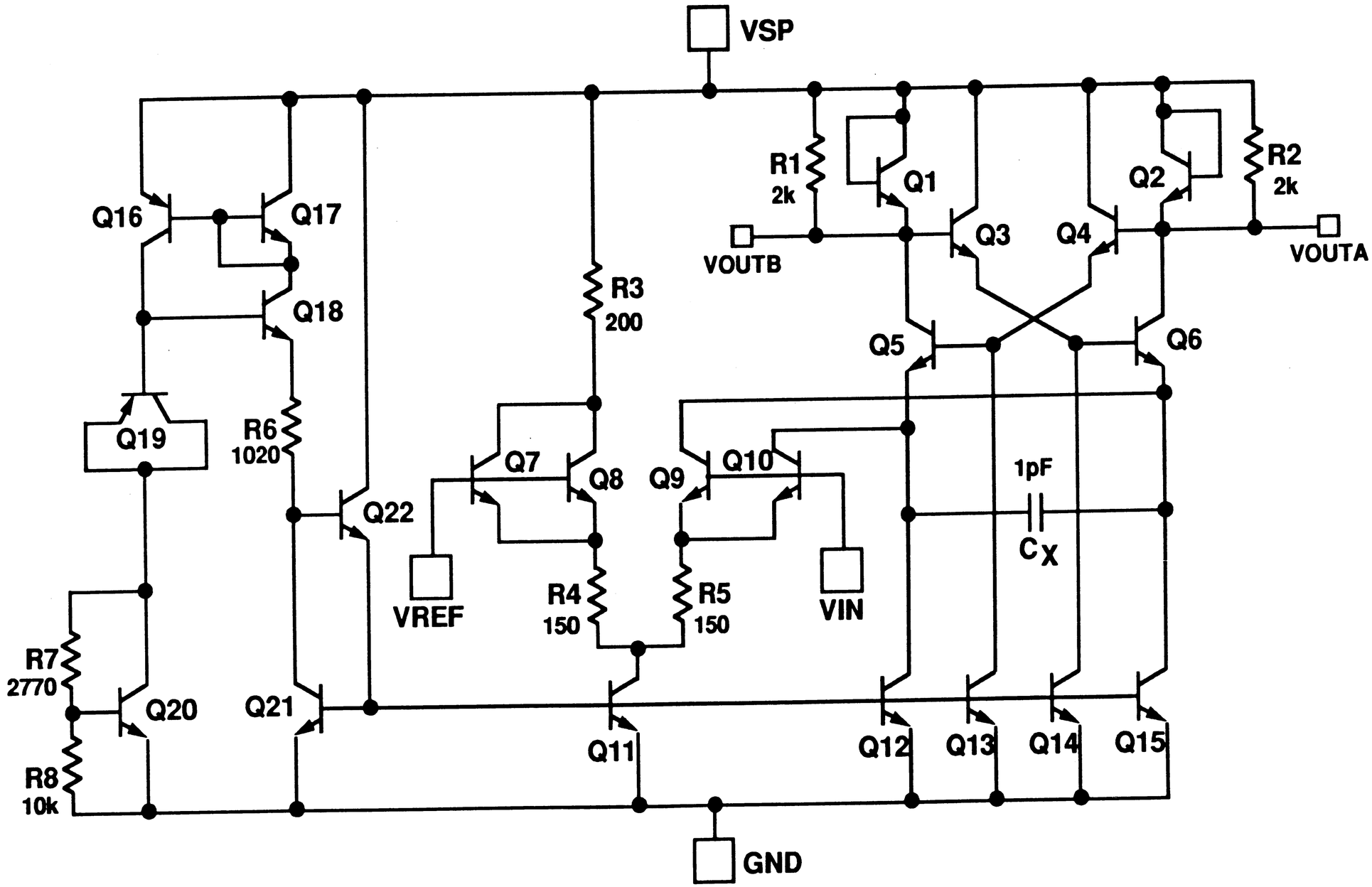


Figure 3.18 Complete Voltage-Controlled Oscillator Circuit

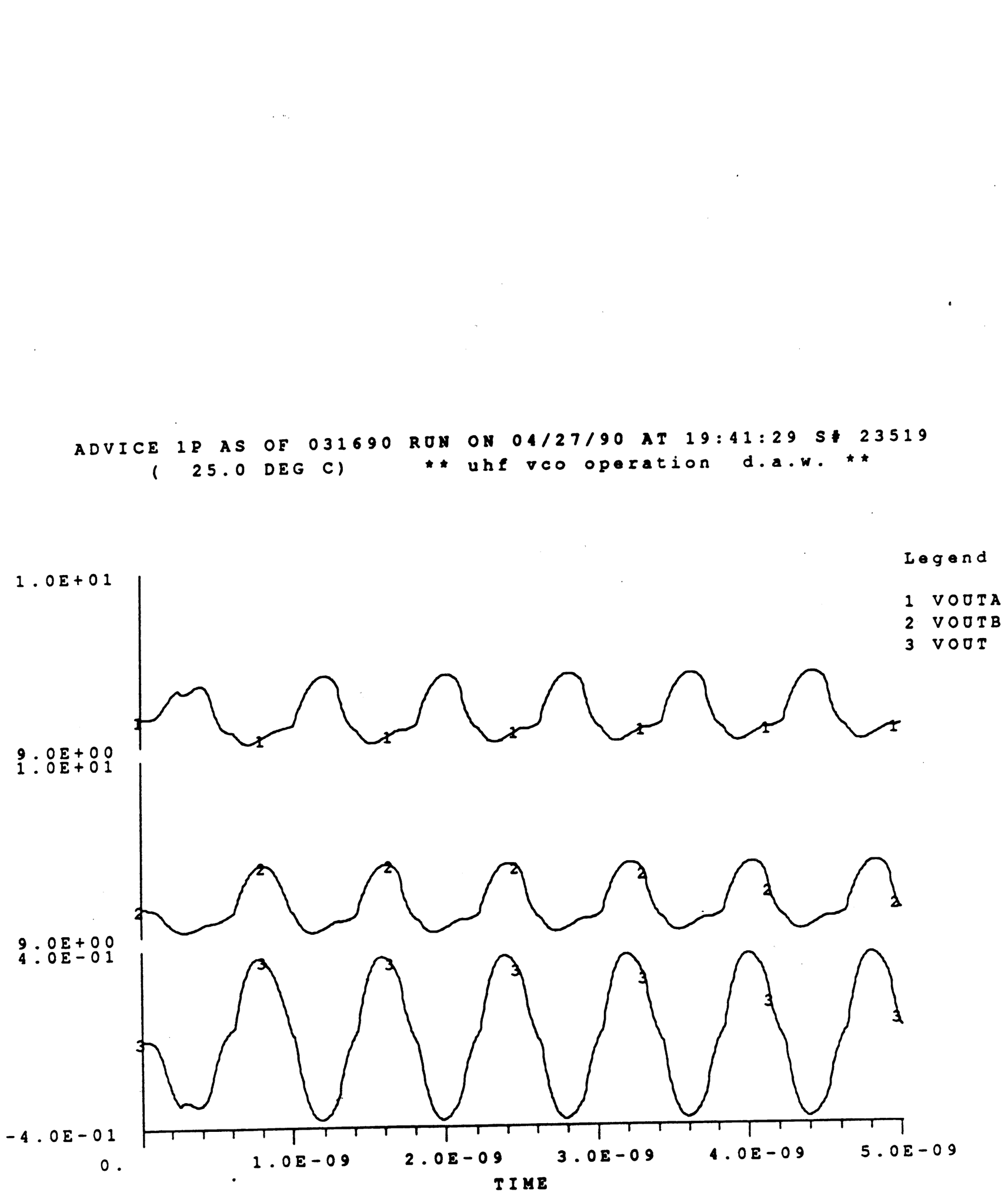


Figure 3.19 Waveforms During VCO Operation

The simulation netlist contained a temperature-dependent voltage source (which ADVICE can model) rather than a breakdown phenomenon (which ADVICE can't model) for the zener voltage. In order to initiate oscillation in the simulation environment, a "jump-start" current source was employed to induce a small perturbation on the timing capacitor. In the actual operation of a fabricated IC, slight mismatches in components and noise would cause the circuit to leave its stable state and begin oscillating. It should be noted that the circuit reaches steady-state operation after only one oscillation cycle as seen in Figure 3.19. Simulations comparing the oscillation period after 100 cycles to the oscillation period after 2 cycles detected no difference.

A more in-depth discussion of the performance of the UHF VCO will be given in Chapter 4 where the effects of processing variations are discussed, and in Chapter 5 where the fabricated prototype chip is characterized and the measurements are compared to the simulation and design goals.

4. DESIGN AND SIMULATIONS OF THE VCO CHIP

4.1 SEMICUSTOM LINEAR ARRAY OVERVIEW

The development of the semicustom linear array family was intended to provide a cost-effective, short lead-time option for providing analog circuit functions on a bipolar monolithic integrated circuit. It is a less expensive approach than a full-custom chip because each new circuit requires the design of only four photolithographic masks to provide the metalization pattern. The turn-around time is much quicker because wafers only need to receive the metalization processing steps. These advantages made the ALA201 CBIC-U Linear Array an ideal candidate for realizing the VCO design.

4.2 SUBCIRCUIT AND CHIP LAYOUT

The ALA201 chip consists of several "tiles" symmetrically located on the chip. These tiles allow the chip design to be implemented on a subcircuit-by-subcircuit basis, thus permitting the critical needs of each subcircuit (e.g., component matching, thermal gradient considerations, current densities, etc.) to be addressed within its own block. The components within the tiles, and the tiles themselves, are interconnected with two levels of metalization.

The general strategies and concerns of integrated circuit chip layout[28, 29] are beyond the scope of this thesis, as are the specific guidelines[30] concerning the CBIC-U technology. However, several considerations need to be mentioned here. First, it was crucial to lay out the oscillator core subcircuit as close as possible to symmetrical to assure symmetry between each side. That is, Q1, Q3, Q5 and R1 are as symmetrical as possible with Q2, Q4, Q6 and R2 within the constraints imposed by the array design itself. Also, each subcircuit tile (even those without active circuitry) has its substrate connections tied to GND. Finally, the subcircuit

tiles are connected to the VSP and GND pads with oversized metalization. These latter two layout considerations address the need to minimize undesirable noise being introduced into the circuit from small resistive voltage drops during switching transients

The computer-aided design tools used to perform this chip layout were: GRED, a graphics editor; SCHEMA, a schematic capture tool; GOALIE, a netlist extraction tool; and ICED, an IC layout editor.

A block diagram of the chip is shown in Figure 4.1 and the complete chip layout is shown in Figure 4.2.

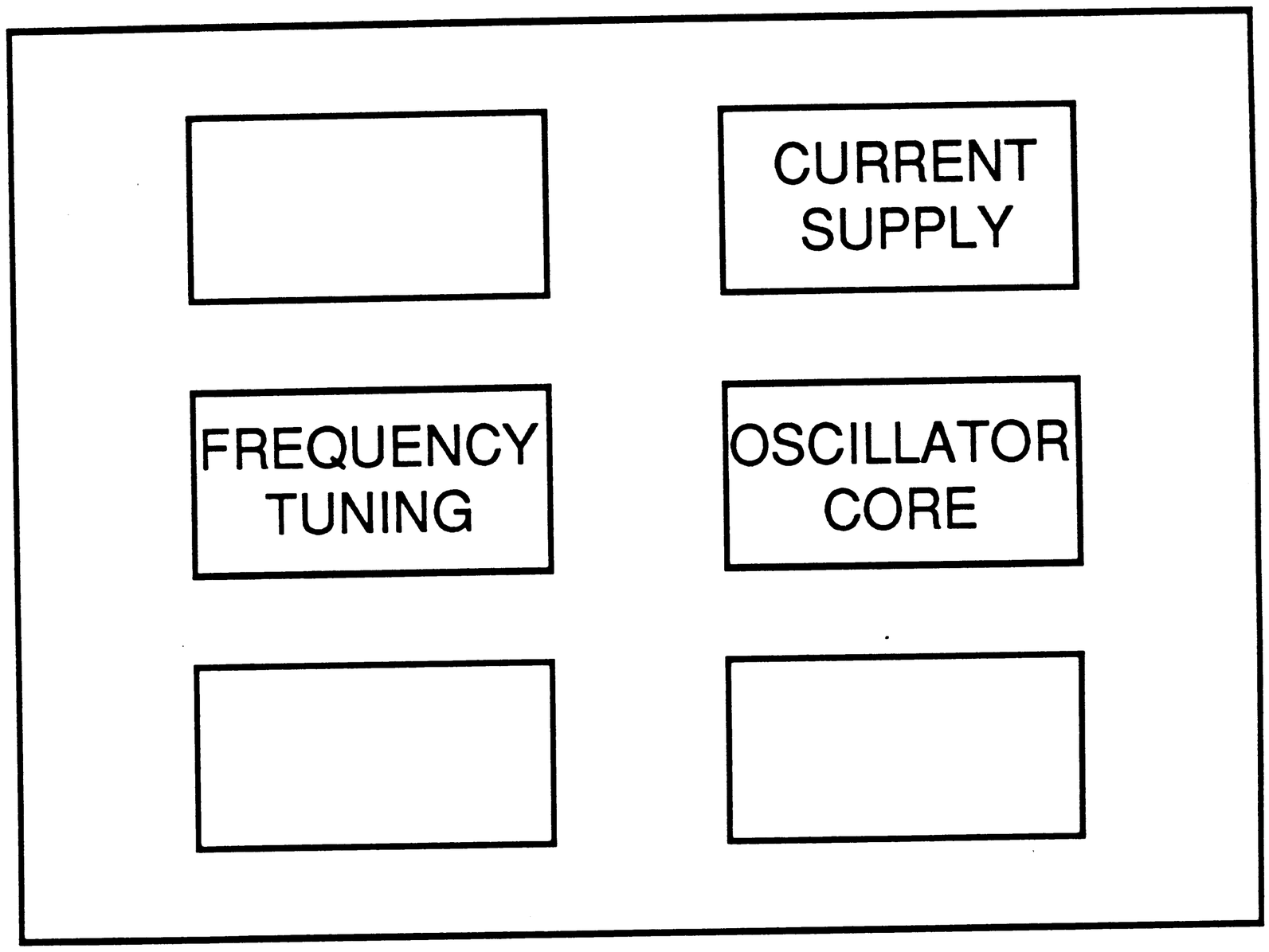


Figure 4.1 Block Diagram of Chip Layout

MASK LEVELS:

N71,N171,RETCH

N239,BILEMITP

N17,N117,THIKMET

BOTMET
N121,N114,N12,N42,N112

TOPMET
N115,N62,N120,N249,N349
N119,N123,N149,N49,N113

BASEP,EMITTERP
N102,N2,N302,N16,BURIEDP
N134,N202,N39,N139,N34

EMITTERN
N205,N238,COLLECTN,BASEN
N38,N5,N108,N138,N105

GATEN
N3,N103,N203,N9,BURIEDN

VIAX
NT,BORDER,TEXT,WINR,RESCAP
N709,N125,N167,N41,N211,N710
N111,N25,N800,N1,N67

CLUMP PRIM3.X

WINDOW :
(X1,Y1): -1608 , -1213
(X2,Y2): 1778 , 1213

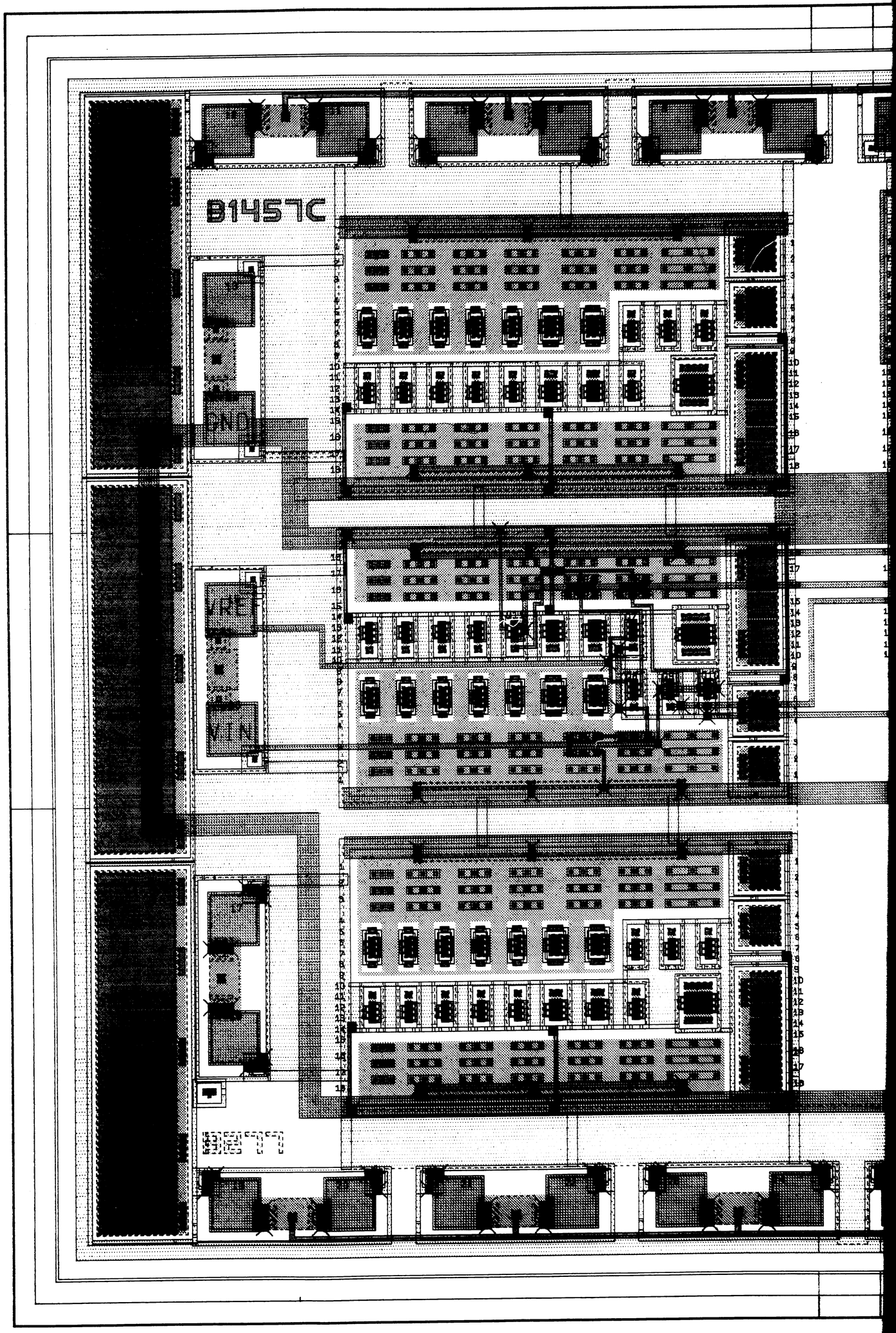
SCALE:
245 UNITS/INCH

SCALE FACTOR:
4.082 MILS/UNIT

RRJ 3394 45237

DATE PLOT GENERATED:
11-APR-90 10:55:04

SOURCE MACHINE: RDESCS1
GRED VERSION: 7.2.7



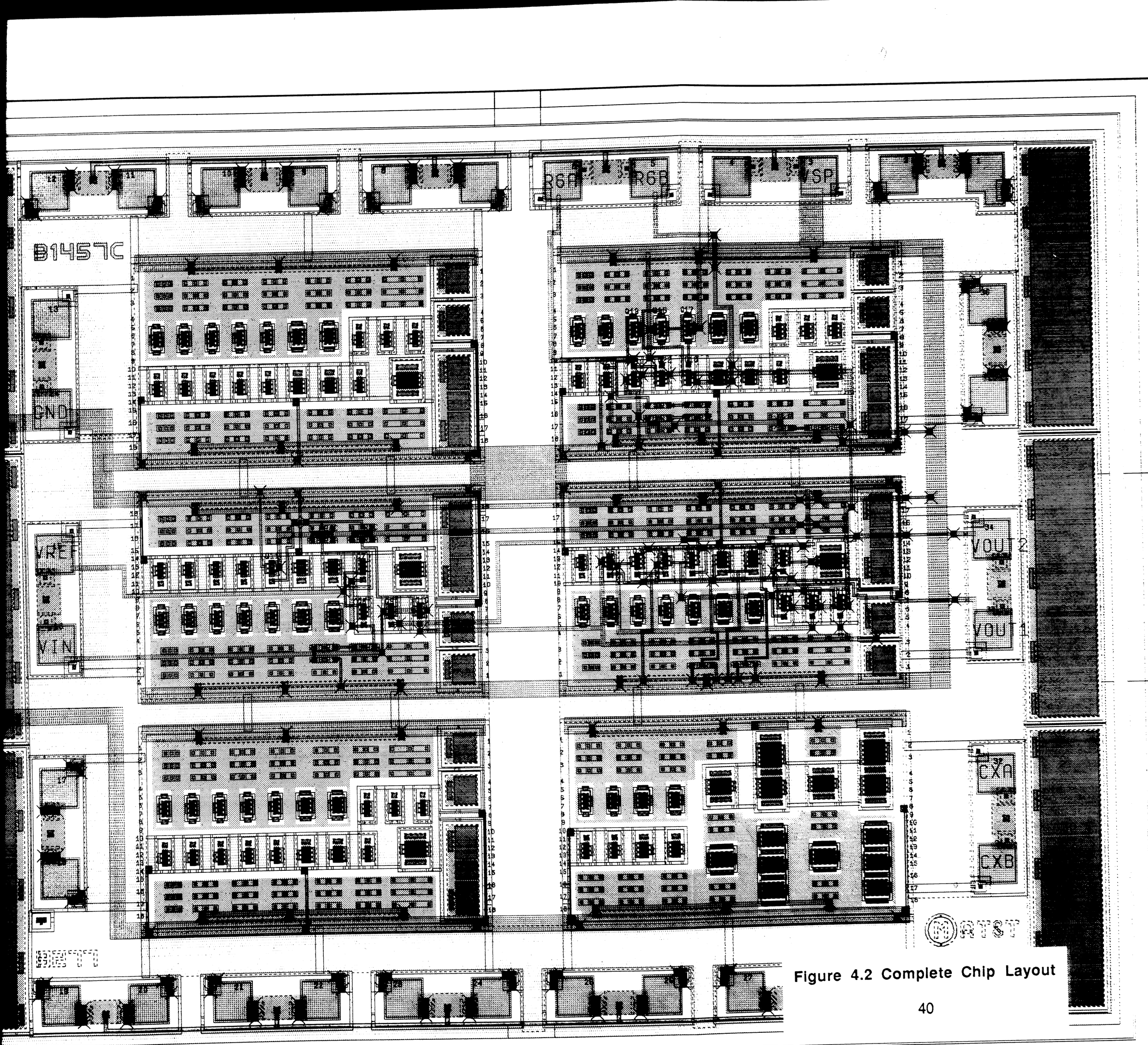


Figure 4.2 Complete Chip Layout

4.3 PARASITIC EXTRACTION

The design of an integrated circuit is an iterative process in which the circuit design and chip design evolve somewhat simultaneously. The availability of components for wiring at the subcircuit tile level on the chip further compound the design process when a linear array is used. For example, it may not be possible to obtain an exact resistor value desired with a reasonable series-parallel combination of available resistors. Therefore, the designer must take this into account and make small adjustments to optimize the design "on-the-fly."

Once the circuit/chip design is "frozen," but before masks are ordered, extraction of all parasitic components is done. The CAD tool that performs this function provides a comprehensive netlist containing the circuit description based on the chip layout database. Included are the lumped wiring interconnect capacitances, resistor segmentation and other layout-specific information. The extracted netlist used for final verification of this design is contained in Appendix E. The results of simulations of the final design will be discussed in Section 5 of this chapter.

4.4 PROCESSING VARIATIONS

In addition to the component considerations pertaining to the final chip design discussed above, the manufacturability of the product is another very important consideration. The product must be robust so as to minimize the effects of the many normal variations in the wafer processing facility. The final UHF VCO circuit and chip design is composed of five types of components: NPN and PNP transistors, 1080 and 50 Ω/square resistors, and a metal-to-metal capacitor. The characteristics of each of these can vary over the normal range of processing independently of the other components. Considering the high-end, low-end and nominal cases for the five types of components yields a total of 243 possible

combinations of processing variations. However, in order to guarantee the performance of the circuit, only six worst-case processing combinations need to be considered in addition to the nominal case. Since this circuit is optimized for speed, its performance is somewhat dependent on the gain of the transistors in the oscillator core subcircuit. The "slow" and "fast" combinations examine the effect of all transistors simultaneously having low and high betas, respectively. The "ß mismatch" cases examine the effects of mismatch between the PNP and NPN transistors, and the "R mismatch" cases examine the effects of mismatch between the 1080 and 50 Ω/square resistors. The performance of the current source subcircuit has a very minor dependence on the matching of its components, and these four cases were used to guarantee its robustness. Table 4.1 summarizes the worst-case analyses performed on the circuit to guarantee its operation over the processing variations expected.

	Description	$ß_{NPN}$	$ß_{PNP}$	R_{1k}	R_{50}	Cap
Combo 1	Nominal	Nominal	Nominal	Nominal	Nominal	Nominal
Combo 2	Slow	Low	Low	High	High	High
Combo 3	Fast	High	High	Low	Low	Low
Combo 4	ß mismatch	Low	High	High	High	High
Combo 5	ß mismatch	High	Low	High	High	High
Combo 6	R mismatch	Low	Low	High	Low	Nominal
Combo 7	R mismatch	Low	Low	Low	High	Nominal

Table 4.1 - Processing Variation Combinations for Simulations

4.5 CIRCUIT SPECIFICATIONS

Since great care was used in the design of this chip to minimize parasitic capacitances and optimize component matching within the oscillator core, the final dynamic simulation results showed immeasurable differences compared to the simulations of the nominal circuit. The characteristics illustrated in Chapter 3 can therefore be considered an accurate representation of the performance of the device and will not be reproduced here. The DC operating point analysis is included as Appendix F for completeness. The DC and AC performance specification based on the full-chip simulations are tabulated in Section 2 of Chapter 5. This provides for greater clarity and will allow easier comparison to the measured values obtained from the prototype chips.

It should be noted here that the specifications for this emitter-coupled implementation of a voltage-controlled oscillator compare favorably to those of lower-speed, commercially available components[31-33]. The architecture and performance of this circuit could easily form the basis for the implementation of higher-performance, large-scale functions such as phase-locked loops, clock regenerators, timing recovery, frequency synthesizers, etc.

5. EXPERIMENTAL RESULTS

5.1 MANUFACTURE OF THE IC

The experimental VCO based on the design presented in Chapters 4 and 5 was fabricated in the CBIC-U technology at the AT&T Microelectronics plant in Reading, Pennsylvania. Three wafers were available for testing and characterization, and of these two were sawn and a sample prepared for further assembly. A photomicrograph of the prototype chip is shown in Figure 5.1

To facilitate reliable DC and AC electrical testing of the completed chips, the chips were mounted in a 16-lead dual-in-line ceramic package. In order to eliminate any detrimental effects on the high frequency operation of the VCO, only the pads that carry DC potentials were wirebonded to make connection to the package leads. These connections are for the power supply (VSP and GND), bias resistor nodes (R6A and R6B), and frequency tuning control (VIN and VREF). In addition, the package lids that are normally hermetically sealed were not installed on the packages to allow internal probing operations. A photomicrograph of the completed device is shown in Figure 5.2, and the corresponding package pin-out is illustrated in Figure 5.3.

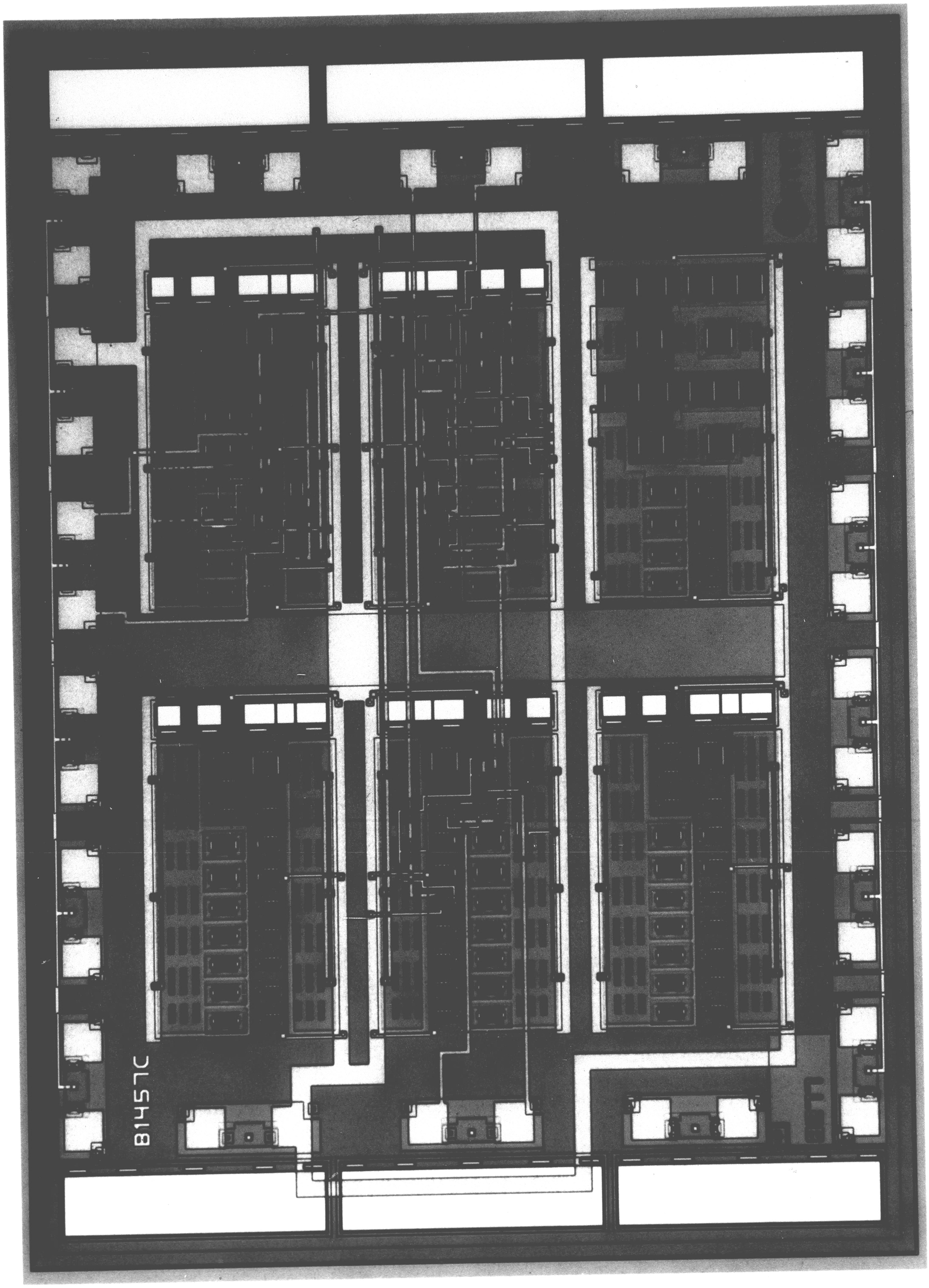


Figure 5.1 Photomicrograph of UHF VCO Chip

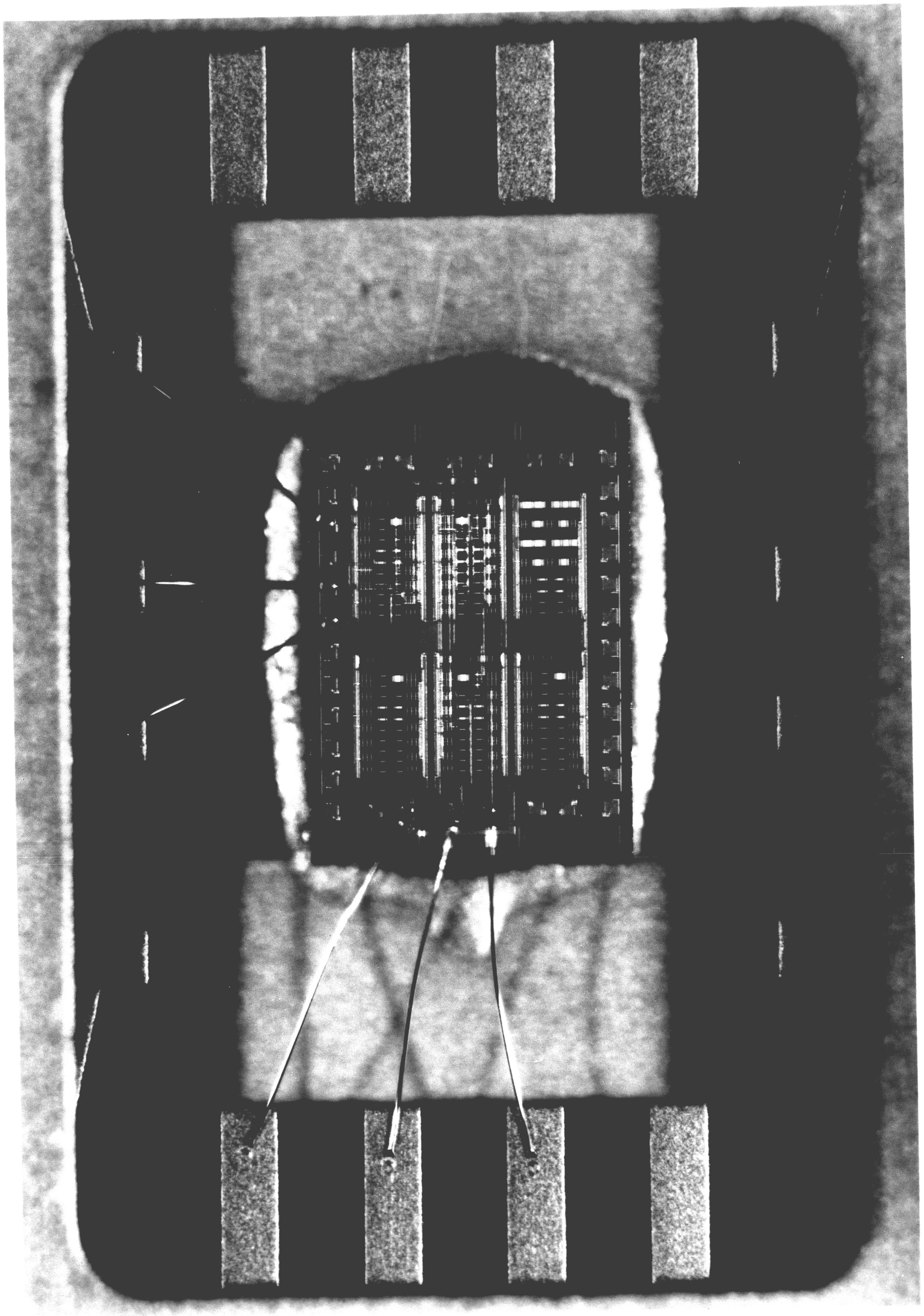


Figure 5.2 Photomicrograph of Packaged Chip

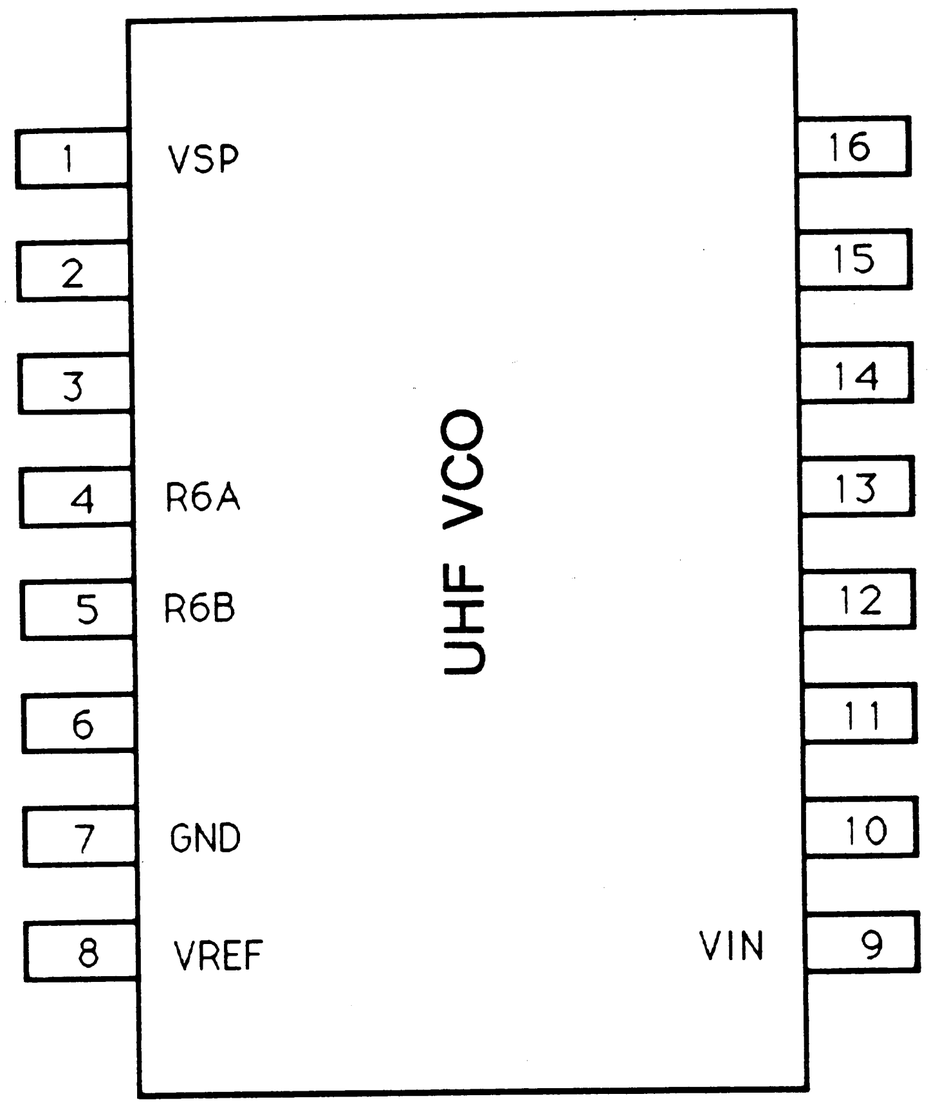


Figure 5.3 UHF VCO Package Pin-Out

5.2 ELECTRICAL MEASUREMENTS

Immediately following the packaging operation, the units were subjected to a visual screen for any mechanical and packaging defects[34]. A simple electrical test that measured the power supply current (with V_{IN}=V_{REF}=open) served as an electrical screen to remove D_0-induced circuit failures[35, 36]. From the units that remained, a random sample of eight were chosen for complete testing. The IC packages were mounted on a two-sided printed circuit board for testing of the DC and AC performance characteristics.

The DC parameters measured were the power supply current I_{VSP}, frequency tuning reference current I_{VREF} and input current I_{VIN}. These were all

found to be well centered between the minimum and maximum values obtained during the worst-case full-chip simulations. The measured DC parameters correspond with wafer processing in which the sheet resistance of the R_{1k} and R_{50} resistors are slightly above nominal. The DC characteristics are summarized in Table 5.1.

The VCO output stage is unbuffered, and its lack of 50 Ω drive capability presented some difficulty during dynamic testing. The state-of-the-art[37-40] in test probe performance is: (1) high impedance probes have a maximum bandwidth of about 600 MHz; and (2) GHz-capable probes impose a 50 Ω load on the measurement node. It should be noted, however, that typical applications for which the VCO circuit would be used are not affected by this shortcoming. Either the output of the VCO would be used to drive the high-impedance input stage of another chip-level circuit (e.g., the phase detector of a phase-locked loop) or the output of the VCO be buffered to increase its drive capability (e.g., a stand-alone oscillator). Due to this lack of drive capability, an oscilloscope record of the output waveform is not available.

The dynamic performance of the prototype chip was verified using a modified version[41] of a non-contact measurement technique[42]. This technique was originally developed for measurement of noise in high-speed digital telecommunications systems where loading by the test equipment adversely affected the measurement results. The measurement system for the testing described here consisted of a Hewlett-Packard Model 70001A Mainframe Spectrum Analyzer (BW=22 GHz), Model 70206A System Graphics Display and RF pick-up coil. The RF pick-up was fabricated from bare wire approximately four inches long that was turned into a five-loop coil about one-quarter inch in diameter. The loop is held in close proximity to the chip (5 mm or less produced the best results), which allows the frequency to be coupled into the spectrum analyzer. Thus

the induced voltage on the pick-up coil allows the frequency of operation to be determined without disturbing the device under test.

The AC characterization consisted of measuring the tuning range above and below the center frequency. The observed values for the tuning range are well above the minimum values observed during worst-case full-chip simulations. Figure 5.4 shows the 1.2 GHz center frequency operation of the prototype VCO. The measured AC parameters correspond with wafer processing in which β_{NPN} is slightly above nominal. The AC electrical characteristics are summarized in Table 5.1.

Parameter	Test Conditions VSP	VREF	VIN	Min.	Typical	Max.	Unit
I_{VSP}	10V	5V	3V	33.3	36.4	37.2	mA
I_{VSP}	10V	5V	5V	33.3	36.6	37.2	mA
I_{VSP}	10V	5V	7V	33.3	36.8	37.2	mA
I_{VREF}	10V	5V	3V	17	53	106	uA
I_{VIN}	10V	5V	7V	20	67	119	uA
Tuning Range Above f_{center}	10V	5V	3V	42	124	N/A	MHz
Tuning Range Below f_{center}	10V	5V	7V	85	100	N/A	MHz

Notes:

(1) The values shown as Min. or Max. are the worst-case values over the expected range of processing variations.

(2) Positive current is defined as current into the device.

(3) The values shown as Typical are representative for the devices used in this research, which were obtained from one processing lot.

Table 5.1 Summary of Electrical Characteristics

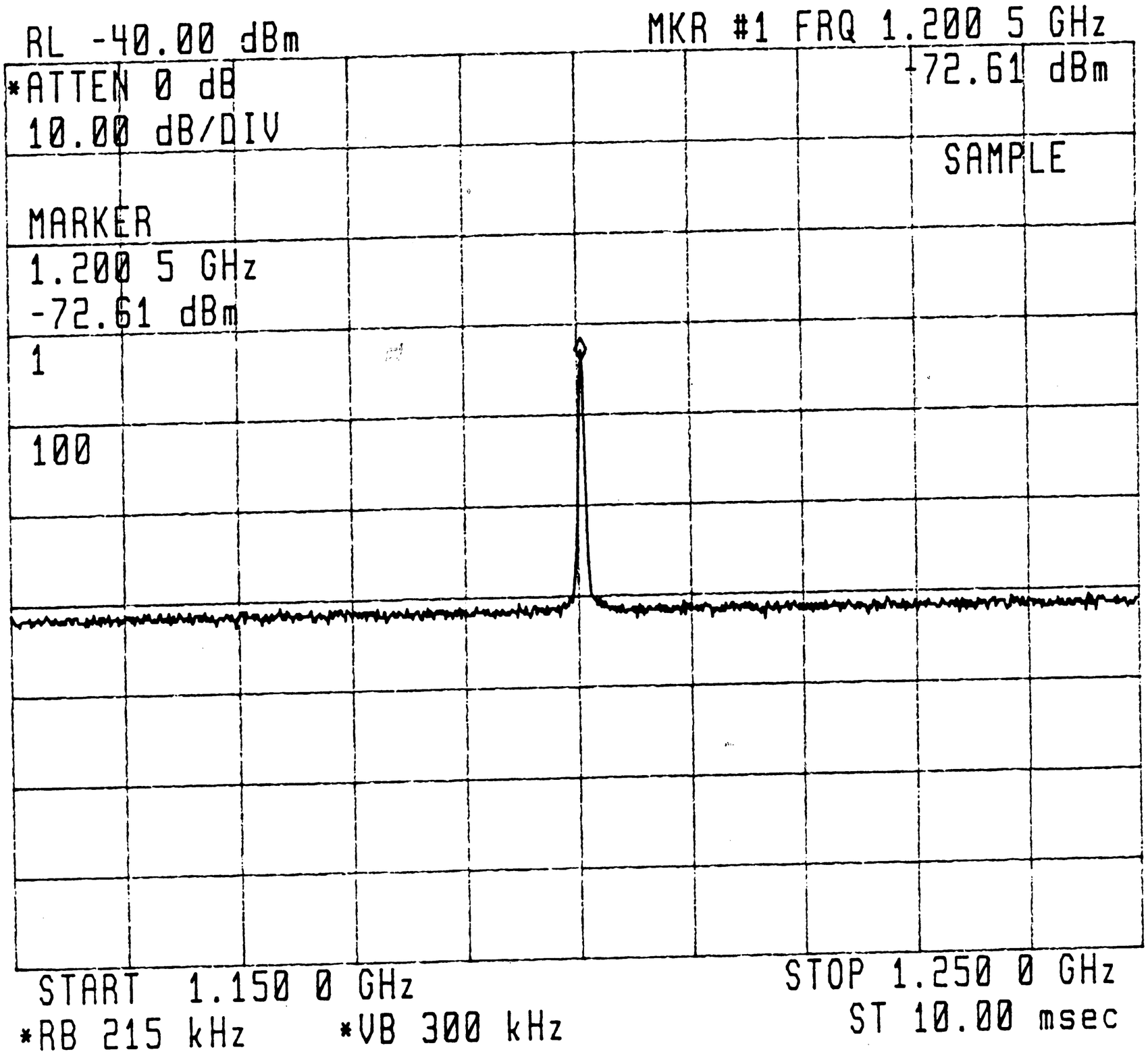


Figure 5.4 1.2 GHz Output Frequency Measurement

6. CHIP-LEVEL INTERCONNECTION STUDY

6.1 INTERCONNECTION CONCERNS

Historically, on-chip interconnect modeling has been given very little attention in analog integrated circuit design. However, recent advances in bipolar device technology that allow operating frequencies in the UHF range suggest that the effects of on-chip interconnects be investigated. Section 2 of this chapter investigates a typical CBIC-U on-chip interconnect structure, but the technique can be applied to any integrated circuit fabrication technology. Knowing the limitations imposed by the interconnect, guidelines for their application are then developed in Section 3.

The availability of the linear array allows a quick-turnaround option for the fabrication of analog functions. By designing a mask set that contains a matrix of chips with several different analog functions, it would be possible to interconnect only the known good die sites after testing via wirebonding to construct a higher-level analog function. This chip-level interconnection scheme would allow a novel form of analog wafer-level integration. An approach such as this could be taken for the evaluation of experimental circuits or for the manufacture of low production volume functions, both of which may not support the development costs associated with the development of a full-custom, medium- to large-scale integrated circuit. To achieve good circuit function, however, it is necessary to know the limitations imposed by the chip-to-chip interconnections. Section 4 of this chapter investigates a typical chip-to-chip interconnect structure, and guidelines for their application are developed in Section 5.

6.2 ON-CHIP INTERCONNECTS

The fabrication of interconnects in any integrated circuit technology imposes

a set of unique constraints on circuit performance. And as design rules shrink, chip sizes grow and operating frequency increases, the on-chip interconnects become an increasingly important concern. To contend with these problems low resistivity materials are being used for the metalization scheme in integrated circuit fabrication technologies.

Unique to the CBIC-U technology is the use of a titanium-platinum-gold metalization system that provides a sheet resistance of only 0.04 Ω per square. This interconnection system provides two levels of interconnection ("top metal" and "bottom metal"), and the two levels can be connected with "vias." The metal lines are surrounded by an SiO_2 insulator as shown schematically in Figure 6.1.

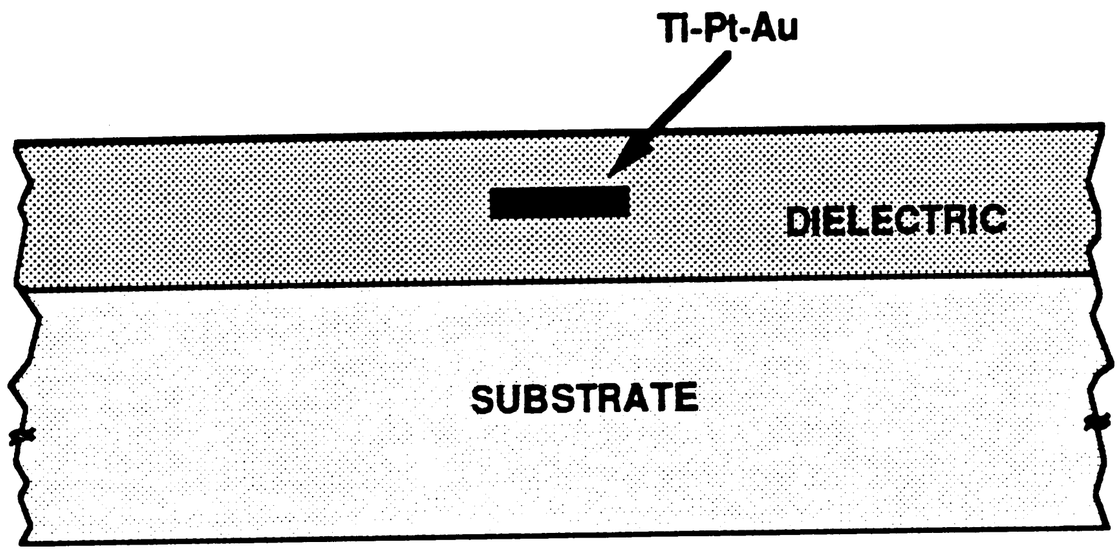


Figure 6.1 Typical CBIC-U Conductor

In earlier chapters of this thesis it was found that the maximum reliable operating frequency for this technology was 1.2 GHz. The prototype UHF VCO chip design emphasized localized interconnects, and the parasitic capacitance associated with these were modeled as simple lumped elements. The validity of this was demonstrated by no discernible differences being detected between the simulations using the nominal netlist and the extracted netlist..

However, for "long-distance" interconnects this lumped element approximation may no longer be valid. Since long-distance interconnects may be necessary in the design of large chips, the details of how they are modeled can be critical for a circuit.

When the physical dimensions of an element affect the propagation of a signal on it, the element is termed "distributed" and transmission-line effects can occur[43]. In analyzing the propagation of a signal in the frequency domain, when the length of the interconnect is greater than one-fifteenth of the wavelength of the signal it carries, the interconnect must be treated as a transmission line[44]. This "breakpoint" at which the interconnect must be modeled as a transmission-line is important because: (1) the circuit and chip designs must take this into account to realize optimum performance if a transmission-line model is required, or to be avoided; and (2) a substantial increase in computing power and/or time is needed when including all the elements associated with a transmission-line model, so it must be considered only when necessary.

Proceeding with the analysis of the interconnect element in the frequency domain, the velocity of propagation is first found. When the medium surrounding the conductor is not air or vacuum, the velocity of the signal is reduced accordingly. For the structure shown in Figure 6.1, the velocity of propagation[45] is then given by

$$v = \frac{c_0}{\sqrt{\varepsilon_r}} = 1.518 \text{ meters / second} \qquad (6.1)$$

where the speed of light is c_0 = 2.9979E8 meters/second and the relative permittivity of the dielectric medium is e_r = 3.9. The wavelength of the 1.2 GHz signal is therefore

$$\lambda = \frac{v}{f_{max}} = 0.127 \text{ meters} \tag{6.2}$$

To remain below the transmission-line "breakpoint," the following ratio must be satisfied

$$\frac{\lambda}{l} \geq 15 \tag{6.3}$$

where l is the length of the interconnect. This is satisfied for an interconnect that is

$$l \leq 8.43 \text{ mm} \tag{6.4}$$

For the ALA201 linear array used to fabricate the prototype UHF VCO, the worst-case interconnect is shown in Figure 6.2. The active area available for interconnect wiring on the chip is 2.25 mm by 1.90 mm. Thus the worst-case long-distance interconnect would be 4.15 mm, which is well under the breakpoint for this technology.

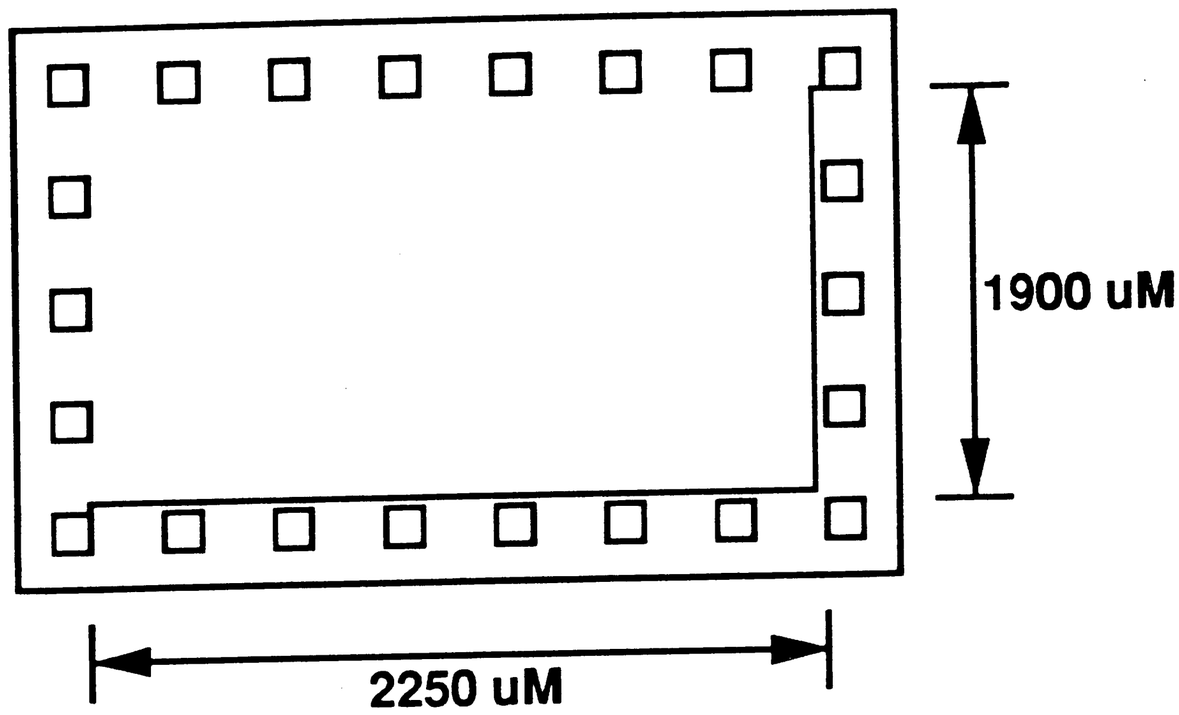


Figure 6.2 Worst-Case ALA201 Interconnect

6.3 GUIDELINES AND MODEL FOR ON-CHIP INTERCONNECTS

The worst-case long-distance interconnect shown above would rarely, if ever, be used in the layout design of an integrated circuit. Indeed, it is typical for long-distance interconnects to be[46] of a length given by the expression

$$l_{max} = \frac{\sqrt{\text{chip area}}}{2} \tag{6.5}$$

For an interconnect at the breakpoint frequency of CBIC-U, Equation 6.5 yields a chip with an active area of 12.7 mm by 12.7 mm. This implies that the maximum chip size for 1.2 GHz operation have an active area about 38 times as large as the ALA201. As the scale of integration increases for high frequency circuits, power dissipation may become the limiting factor[47] long before the breakpoint is

reached.

However, even for integration at a scale where the typical long-distance interconnect length remains below the breakpoint, propagation delay may still be a concern. In applications where the interconnect delay must be modeled accurately, the distributed RC network can be employed. Shown symbolically in Figure 6.3,

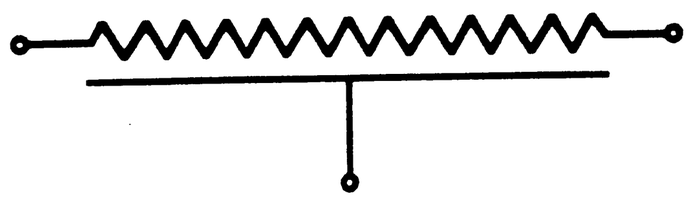


Figure 6.3 Symbolic Distributed RC Network

geometrically distributed effects of the parasitic resistance and capacitance can be modeled by the equivalent network shown in Figure 6.4.

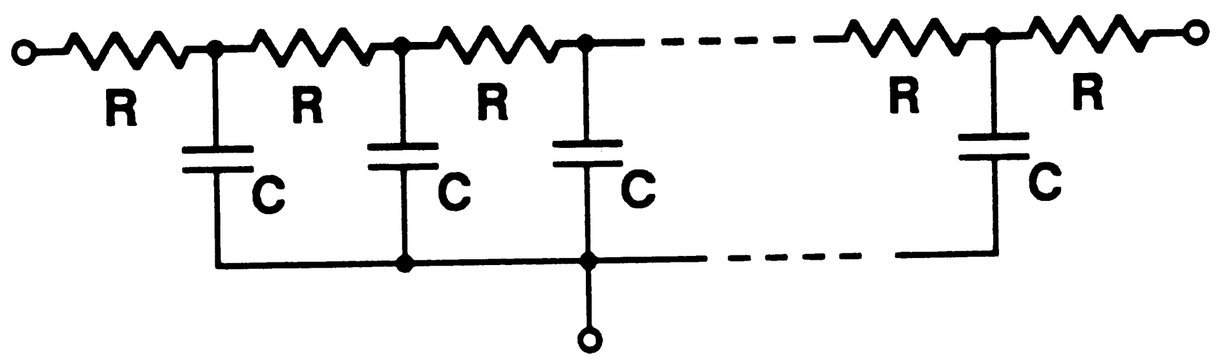


Figure 6.4 Equivalent RC Network

When the interconnect is segmented as shown above, the response in the time domain can be found. Referring to the representation in Figure 6.5

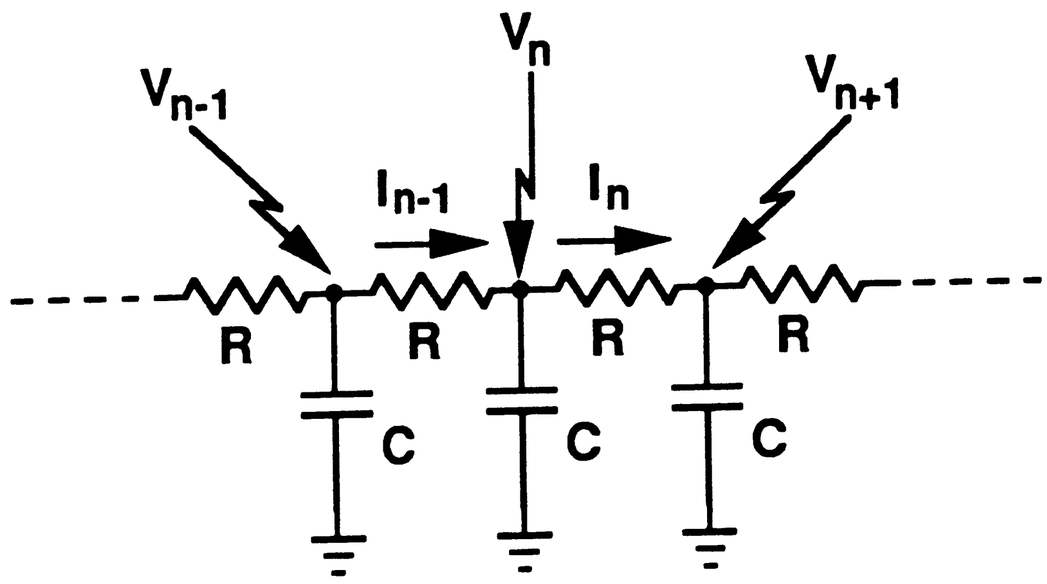


Figure 6.5 Response of RC Network

the response at node n is given by

$$C\frac{dV_n}{dt} = I_{n-1} - I_n \tag{6.6}$$

$$= \frac{V_{n-1} - V_n}{R} - \frac{V_n - V_{n+1}}{R} \tag{6.7}$$

By increasing the segmentation of the interconnect, the differential form of the above expression can be used as given in Equation 6.8.

$$rc\frac{dV}{dt} = \frac{d^2V}{dx^2} \tag{6.8}$$

where c is the capacitance per unit length, r is the resistance per unit length and x is the distance along the interconnect from the input.

The solution to this equation gives the propagation delay of a signal along the interconnection at a distance x as

$$t_x = Ax^2 \qquad (6.9)$$

where A is a constant.

A discrete solution of the segmented circuit[48] yields an approximate delay of

$$t_n = \frac{RCn(n+1)}{2} \qquad (6.10)$$

By increasing the segmentation of the interconnect, the delay for the total interconnect length l becomes

$$t_l = \frac{(rl)(cl)}{2} = \frac{rcl^2}{2} \qquad (6.11)$$

where c is the capacitance per unit length, r is the resistance per unit length and l is the total length of the interconnect.

The series resistance of a metal chip-level interconnect is determined by counting the number of squares and multiplying by the sheet resistance. In the CBIC-U technology bottom interconnection metalization has a sheet resistance of

0.04Ω per square and a minimum width (which can carry 2 mA per uM of width) of 5uM[30]. Thus the worst-case ALA201 interconnect shown earlier in Figure 6.2 would have a total resistance of 33.2 Ω.

The parasitic capacitance of a metal chip-level interconnect is determined by multiplying the total area by the capacitance per unit area. In the CBIC-U technology, the bottom metal interconnects will have the highest capacitance as they are closer to the substrate. Using a formula that accounts for fringing effects[30],the capacitance is given by

$$C = (5.162E\text{-}5)(L)(W + 1.947) \qquad (6.12)$$

where L and W are the interconnect length and width in uM. For the worst-case runner the parasitic capacitance would be 1.5 pF.

Using these parasitic values, the propagation delay as given by Equation 6.11 through a segmented form of the worst-case interconnect would be

$$t_{Eqn.\ 6.11} = 0.025\ nS \qquad (6.13)$$

This shows excellent agreement with the delay predicted by the propagation velocity given by Equation 6.1 of

$$t_{Eqn.\ 6.1} = 0.027\ nS \qquad (6.14)$$

It should be noted that the difference between these results is only 0.2% of the period of a 1.2 GHz signal.

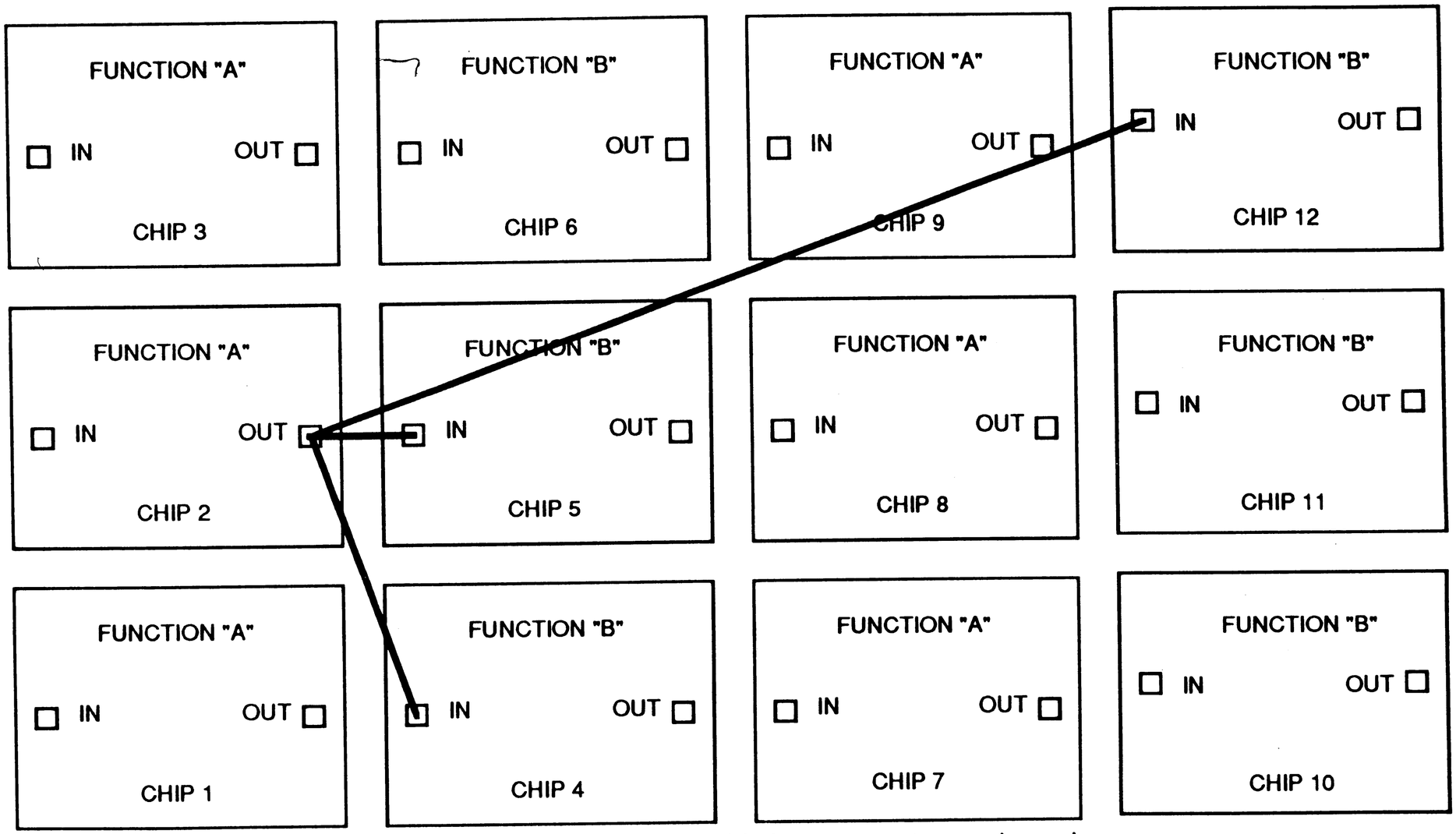
Based on extensive simulations using ADVICE for a number of test cases

using variety of network values, the representation of an interconnect by 8 or more segments provides adequate accuracy (i.e., within 1% of the calculated delay). Therefore, for those applications that demand accurate modeling of the interconnect propagation delay, an 8-segment distributed RC network will generally yield successful, accurate simulation results.

6.4 CHIP-TO-CHIP INTERCONNECTS

As described in Section 6.1, the linear array offers the possibility of wafer-level integration of analog circuits. For example, wafers could be fabricated with several different low-level "building-block" analog functions arranged in an alternating pattern across the wafer. These functions would be tested individually after wafer fabrication. Then, knowing which chips pass final test, the individual sites could be connected in various combinations to form higher-level analog functions. The interconnection would be accomplished with an automated wirebonding system that would select the proper chips to realize the desired function.

To illustrate this concept, consider a scenario involving two building blocks as shown in Figure 6.6. Here the output of function "A" must be connected to the input of function "B" to form the higher-level analog function "AB." Assume that chip #2 passed final test for "A" and either chip #4, #5 or #12 passed final test for "B." There then exists three possibilities to form "AB": chip #2 to chip #4; chip #2 to chip #5; or chip #2 to chip #12. The three different wirebonds necessary to realize "AB" are mapped simultaneously onto the diagram for illustration purposes; only one wirebond would actually be required. As can be seen in Figure 6.6, vastly different length wire interconnects are required to accomplish the desired integration depending upon the chips selected.



Note: Three possible chip-to-chip interconnects are shown here simultaneously for illustration purposes only.

Figure 6.6 Linear Array Wafer-Level Integration Scenario

To realize these chip-to-chip interconnects, wirebonds that terminate in a wedge bond at both ends are used. In a wedge bond a short piece of wire is bonded parallel to the surface, becoming flattened in the process. The connections span from one bond pad to another in a somewhat arched shape. The shape of the wire loop is dictated by the mechanics of the bonding process: The peak of the wire is closer to the first wedge bond because the bonding capillary first lifts vertically and pulls slightly on the wire as it moves to the second wedge bond and lowers into position. Actual typical chip-to-chip wire interconnections are illustrated in the photomicrograph of Figure 6.7. Note that it is a reflection of the wire that is visible on the surface of the chip, appearing just to the left of the actual wire.

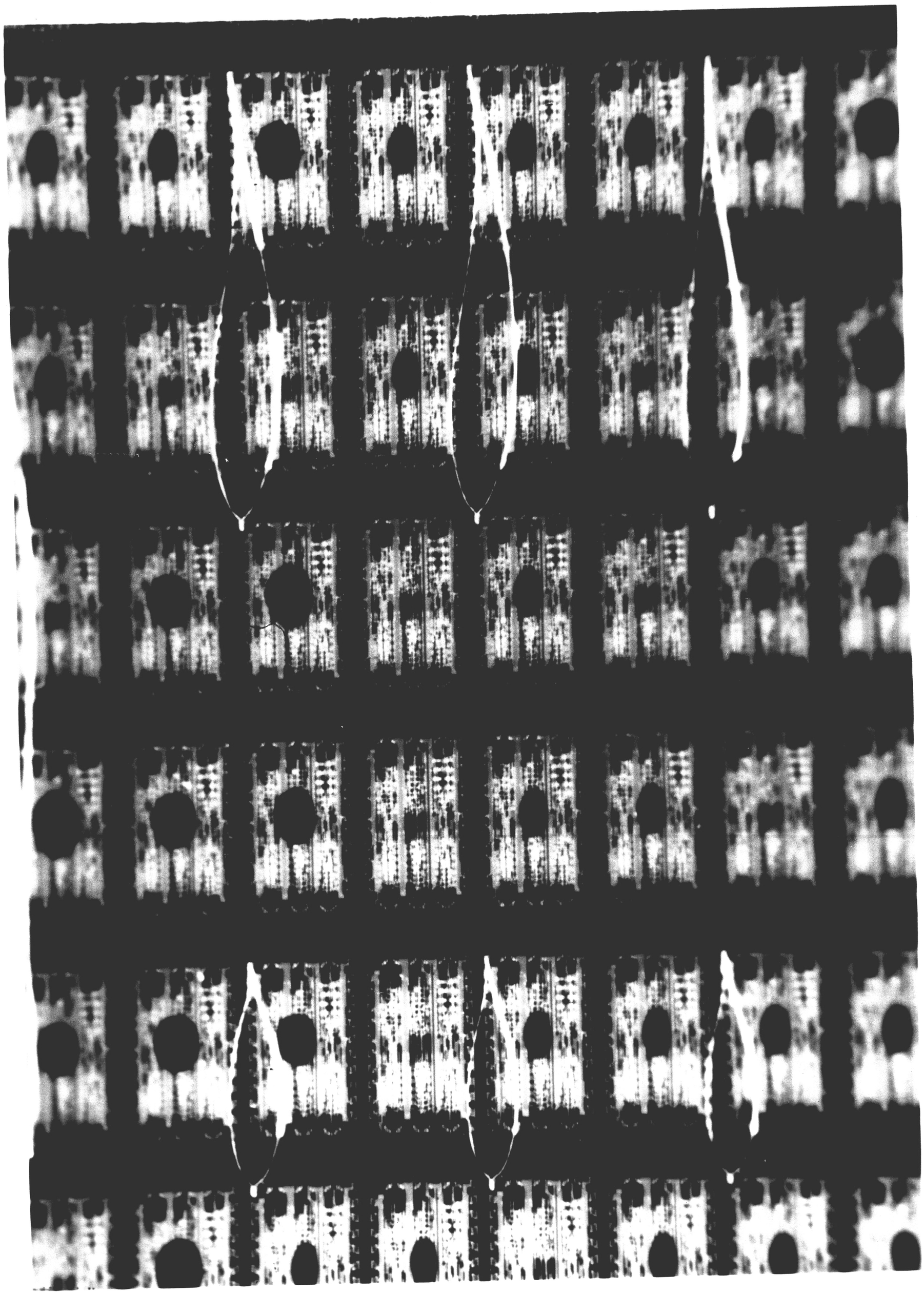


Figure 6.7 Photomicrograph of Chip-to-Chip Interconnect

The feasibility and limitations of wirebonding in the context of wafer-level integration will be carried out in the frequency domain. For the previous analysis of on-chip interconnects, the structure was uniform and flat with rectangular gold conductors surrounded by a planar dielectric. For the chip-to-chip wirebond the geometry is now different (a 1 mil diameter round wire that forms an arch), as are the material properties (aluminum wire surrounded by air). For the wire surrounded by air, the propagation velocity is simply

$$v = c_o = 2.9979E8 \text{ meters / second} \tag{6.15}$$

since $e_r = 1.00$ for air. The 1.2 GHz signal therefore has a wavelength

$$\lambda = \frac{v}{f_{max}} = 0.250 \text{ meters} \tag{6.16}$$

To adhere to the one-fifteenth rule (see Section 6.2) so as to remain below the transmission-line breakpoint, the chip-to-chip interconnect must have a length

$$l \leq 16.7 \text{ mm} \tag{6.17}$$

The geometry of the on-chip interconnects across the monolithic integrated circuit required only a two-dimensional analysis. Now, however, the geometry of the wirebond demands that the analysis account for the added dimension of the wire loop. In order to accomplish this a selection of chip-to-chip interconnects were fabricated at the AT&T Microelectronics plant in Allentown, Pennsylvania. A sample of three wirebonds were made for each of five different lengths. The five different

lengths were chosen in "one-chip increments" to simulate interconnecting an adjacent chip, a chip two sites away, etc. Since the horizontal step distance for the ALA201 linear array matrix is 3.13 mm, the pad-to-pad bonding distances were: 3.13 mm; 6.26 mm; 9.39 mm; 12.52 mm; and 15.65 mm.

To characterize the propagation delay through the wirebond for the various step distances, a method known as time-domain reflectometry was employed. A step generator and an oscilloscope form the basis of the measurement system which can best be described as "closed-loop radar." In TDR a voltage step is propagated down the interconnect under investigation, and the incident and reflected waves are monitored by the oscilloscope at a particular point on the line. In the case of the wirebonds, the signal was injected and monitored at the same end. And, since the opposite end is an open circuit, the response from the reflected wave was captured by the oscilloscope. This then allowed the propagation delay to be determined. The test set-up used to in this evaluation consisted of a Hewlett-Packard Model 54120A Digitizing Oscilloscope Mainframe and Model 54121A Four-Channel Test Set (with TDR capability).

The measurements for the fifteen sample wirebonds as a function of step distance are illustrated in Figure 6.8.

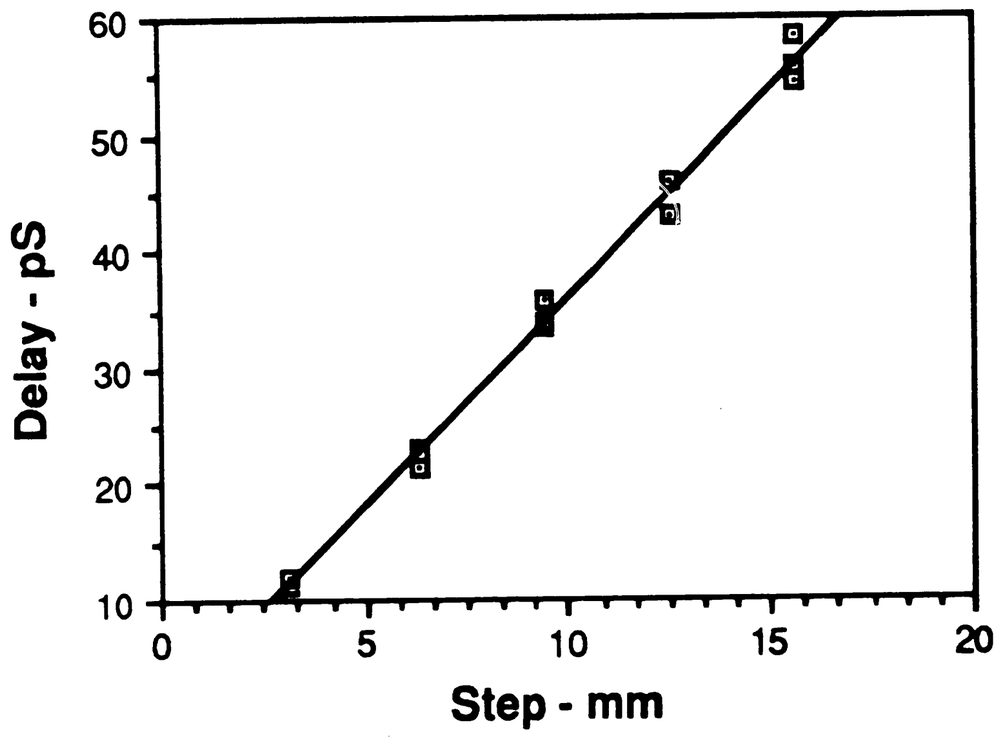


Figure 6.8 Measured Delay vs Step Distance

As can be seen the propagation delay ranged from about 10 to 60 pS. However, it should be noted that as step distance increased the individual delay times became less consistent for a given step distance. For example, at 15.65 mm step distance there was a 7% difference between the minimum and maximum propagation delay times.

Further investigation of the wirebonds revealed that there were variations in the geometry of the wire loop that caused a variation in the length of the wire for a given step distance. In order to quantify this variation, the wirebonds were removed and the length of each wire measured using a Hiedenhain Model MT25 Measurement System. The measured propagation delay now correlates very well when using the actual wire length instead of the pad-to-pad step distance. This is illustrated in Figure 6.9.

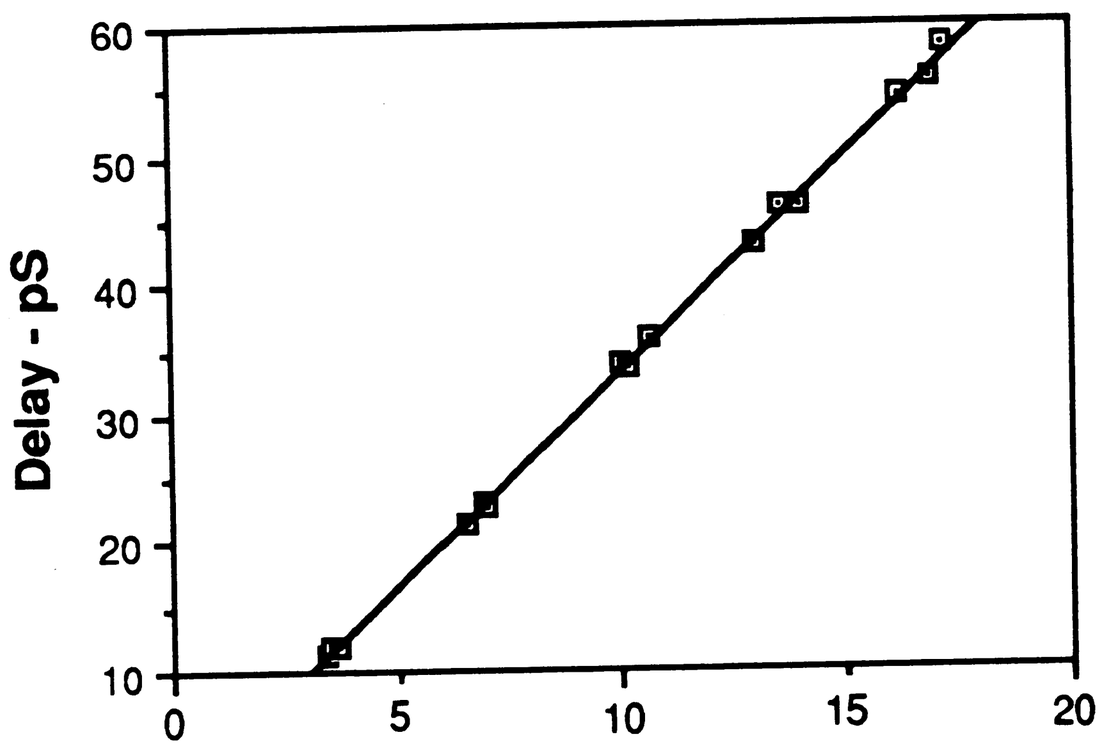


Figure 6.9 Measured Delay vs Wire Length

The calculated propagation delay using Equations 6.15 and 6.18 and based on the

$$t_{wire} = \frac{l_{wire}}{v_{Eqn.\ 6.15}} \qquad (6.18)$$

measured wire lengths also correlates very well with the measured propagation delay as illustrated in Figure 6.10.

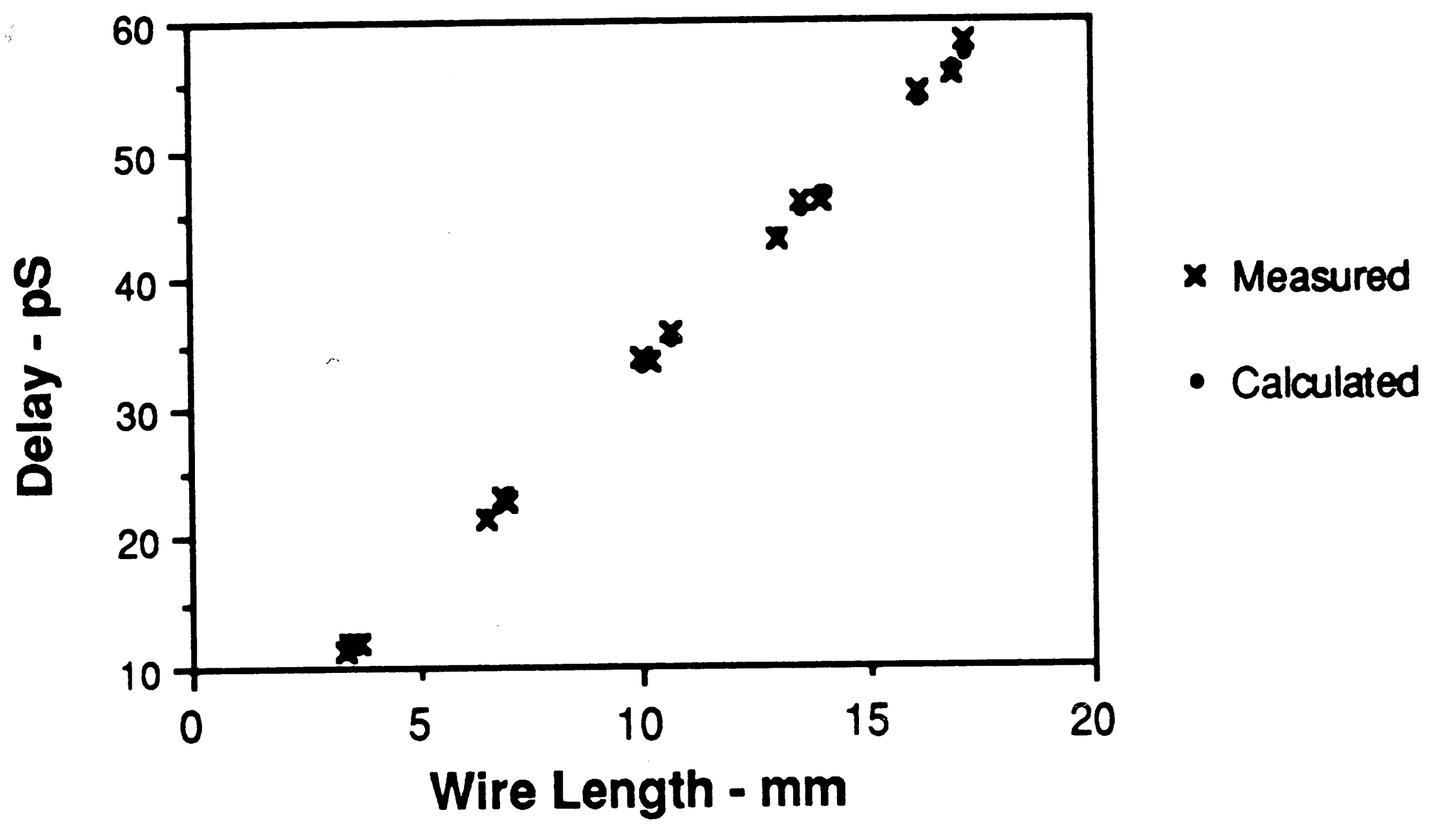


Figure 6.10 Measured and Calculated Delay vs Wire Length

6.5 GUIDELINES AND MODEL FOR CHIP-TO-CHIP INTERCONNECTS

The breakpoint length for wirebonds in the CBIC-U technology was given by Equation 6.17 as 16.7 mm, and was based on a 1.2 GHz operating frequency. Based on the experimental results obtained here, the maximum step distance

across an ALA201 wafer for the interconnection of two building-blocks would include matrix of chips that would range between 5 chips by 5 chips to 1 chip by 6 chips (based on a chip site step and repeat of 3.13 mm by 2.34 mm). The implies that the manufacturing yield would have to be so low as to range between 8% to 30% at final test to require such interconnect spans. If the manufacturing yields are greater than that, the maximum span would be much less that the breakpoint length of 16.7 mm. For general application of wafer-scale integration, the feasibility depends on chip size, manufacturing yield and the layout and number of building-blocks on a wafer matrix. All of these factors combined would require an in-depth study to determine whether wafer-scale integration is economically justified for a particular application case.

7. CONCLUSION

7.1 SUMMARY OF WORK

The research undertaken in this thesis was two-fold in purpose: The upper limit of reliable high frequency operation of the CBIC-U bipolar integrated circuit fabrication technology was to be determined. Then at that frequency, the effects of chip-level interconnects were to be examined.

For the former purpose, a high-frequency voltage-controlled oscillator was designed and fabricated. It was determined that the emitter-coupled oscillator architecture was best suited for implementation in a bipolar technology. An overview of the CBIC-U technology and a comparison to the SBC technology was then given for background. The electrical characteristics and simulation models for the standard components that were used in the design of this circuit were also presented.

The UHF VCO operates from a single 10 volt power supply and requires about 37 mA supply current. The design of the circuit consists of three subcircuits: the oscillator core subcircuit, the current supply subcircuit and the frequency tuning subcircuit. The oscillator core was optimized for speed and thus operates with small voltage swings and large bias currents. It provides a differential output voltage. The current supply uses a zener-based reference scheme and was designed for a nominally zero temperature coefficient over the range 0 to 100 °C. The frequency tuning subcircuit controls the oscillator operation by means of a differential input voltage with a two volt range about a reference voltage. Based on ADVICE simulations, the maximum center frequency for reliable operation across all processing variations was found to be 1.2 GHz. The prototype UHF VCO chip was designed and fabricated on an ALA201 linear array. The chip successfully demonstrated operation at a center frequency of 1.2 GHz, with a tuning range of

+124 MHz / -100 MHz.

The effects of both "long-distance" on-chip interconnects and "chip-to-chip" wire interconnects were studied. The breakpoint at which transmission line effects would become a concern was established for both types of interconnects for the CBIC-U technology. For a minimum-width, bottom-metal on-chip interconnect, that length was found to be 8.43 mm. For typical designs that equates to a chip with an active area of 12.7 mm by 12.7 mm. It is believed that as the scale of integration increases, power dissipation may be the limiting factor, rather than interconnect effects, for high-frequency circuits in CBIC-U. Below the breakpoint, a distributed RC network model for critical interconnects was shown to be valid.

To evaluate wirebonding as a possible method to implement wafer-scale integration, prototype chip-to-chip interconnects were fabricated. Based on delay time measurements, the breakpoint was found to be 16.7 mm. The technical feasibility of this integration method was demonstrated, but it was determined that an in-depth study of each potential application would need to be made. Factors to be considered in justifying this technique are chip size, processing yield, etc.

7.2 FUTURE TOPICS

The prototype VCO demonstrated the capability of the emitter-coupled integrated circuit oscillator architecture to operate at frequencies in the UHF range. This capability may be of interest for the implementation other VCO circuit architectures in this and other technologies. For example, the still-experimental next-generation CBIC-V technology has an NPN f_T of 13 GHz. This could yield a VCO that operates at 4 GHz or higher. Given these potentials, several topics for future research would be: (1) design and fabrication of an emitter-coupled VCO that operates in the SHF range and employs parasitic capacitance as the frequency determining element; (2) implementing a higher-level analog function (e.g., a

phase-locked loop) that employs the UHF VCO described in this thesis; (3) adding to the UHF VCO output emitter-coupled logic that performs a "programmable modulus" counter function, yielding a frequency tuning range of several orders of magnitude down to the LF range; and (4) design and fabrication of test chips of assorted linear circuits for further study of the feasibility of wafer-level integration of analog functions, in terms of both the electrical and mechanical limitations.

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APPENDIX A

Typical Electrical Characteristics of Selected CBIC-U Components

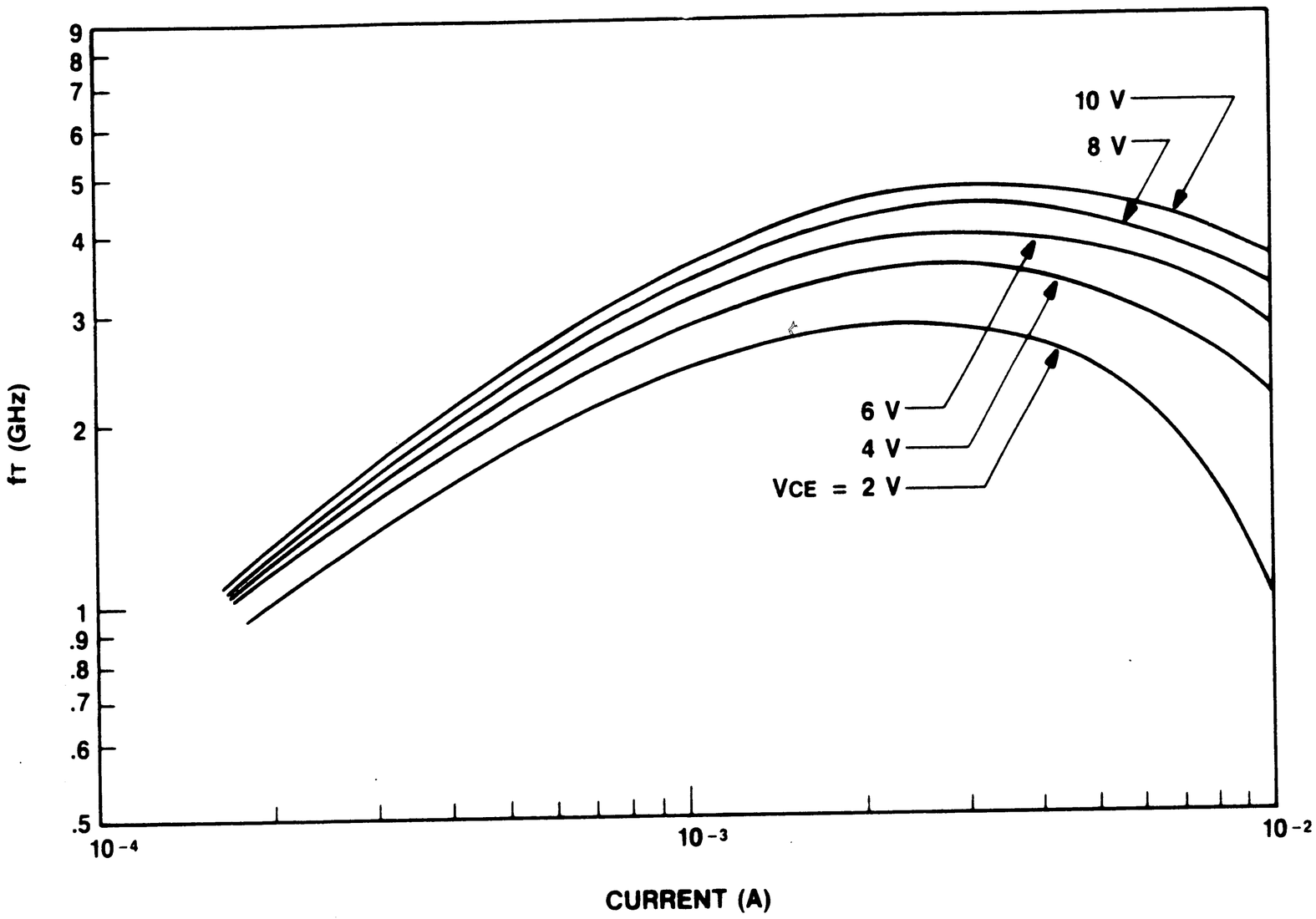
NPN TRANSISTOR ELECTRICAL CHARACTERISTICS

(All data is at T_{AMB}=25 °C)

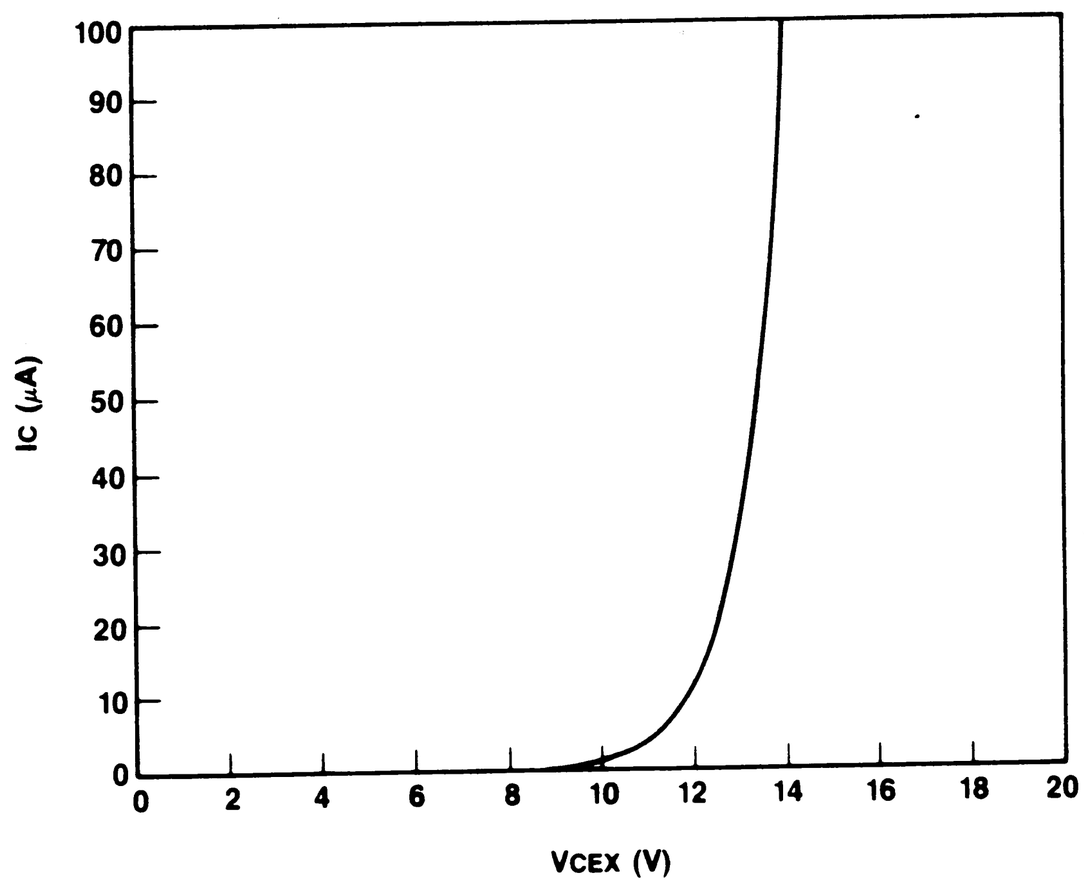
DC Parameters for the NU320PA 1X NPN

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}	I_C = 1 mA, V_{CE} = 2 V	25	40	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	2.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	8	11	—	V
$V_{CE\ (sat)}$	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}†	I_E = 1 mA, V_{CE} = 2 V	.730	.780	.830	V
BV_{CEX}	I_C = 100 μA, I_B = 0.1 μA	11	14	—	V
I_{EBO}	V_{EB} = 2 V, I_C = 0	—	.01	1	μA
BV_{CBO}	I_C = 1 μA	16	19	—	V
BV_{CSO} (collector substrate breakdown)	I_C = 1 μA	20	40	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	5.0	5.4	6.7	V

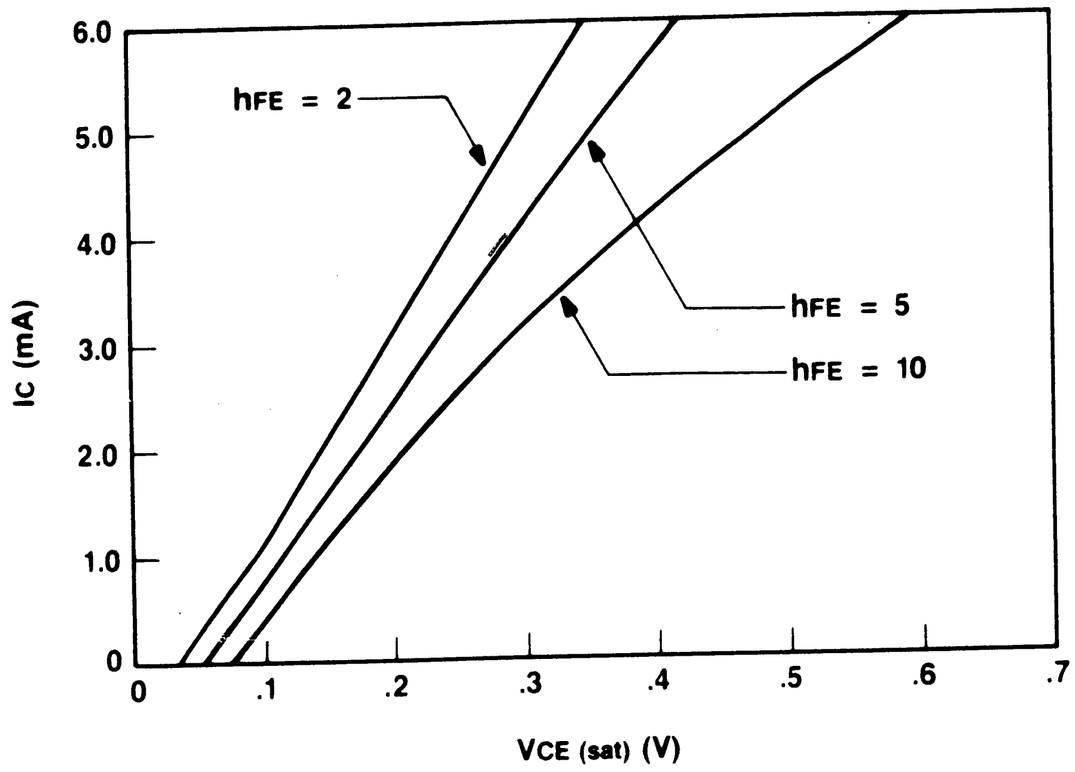
Frequency vs. Current for a Typical NU320PA 1X NPN



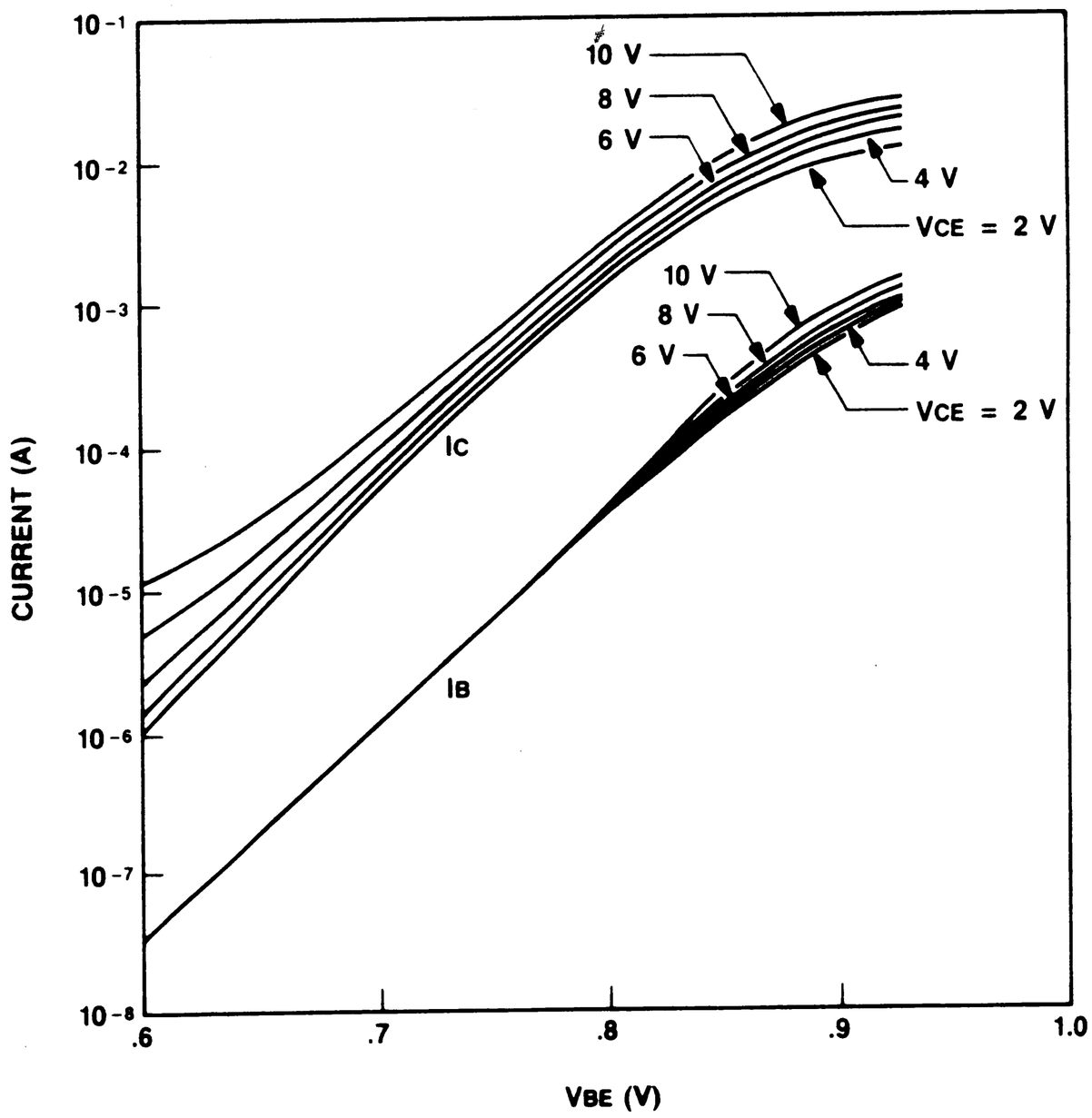
Current vs. Breakdown Voltage for a Typical NU320PA 1X NPN



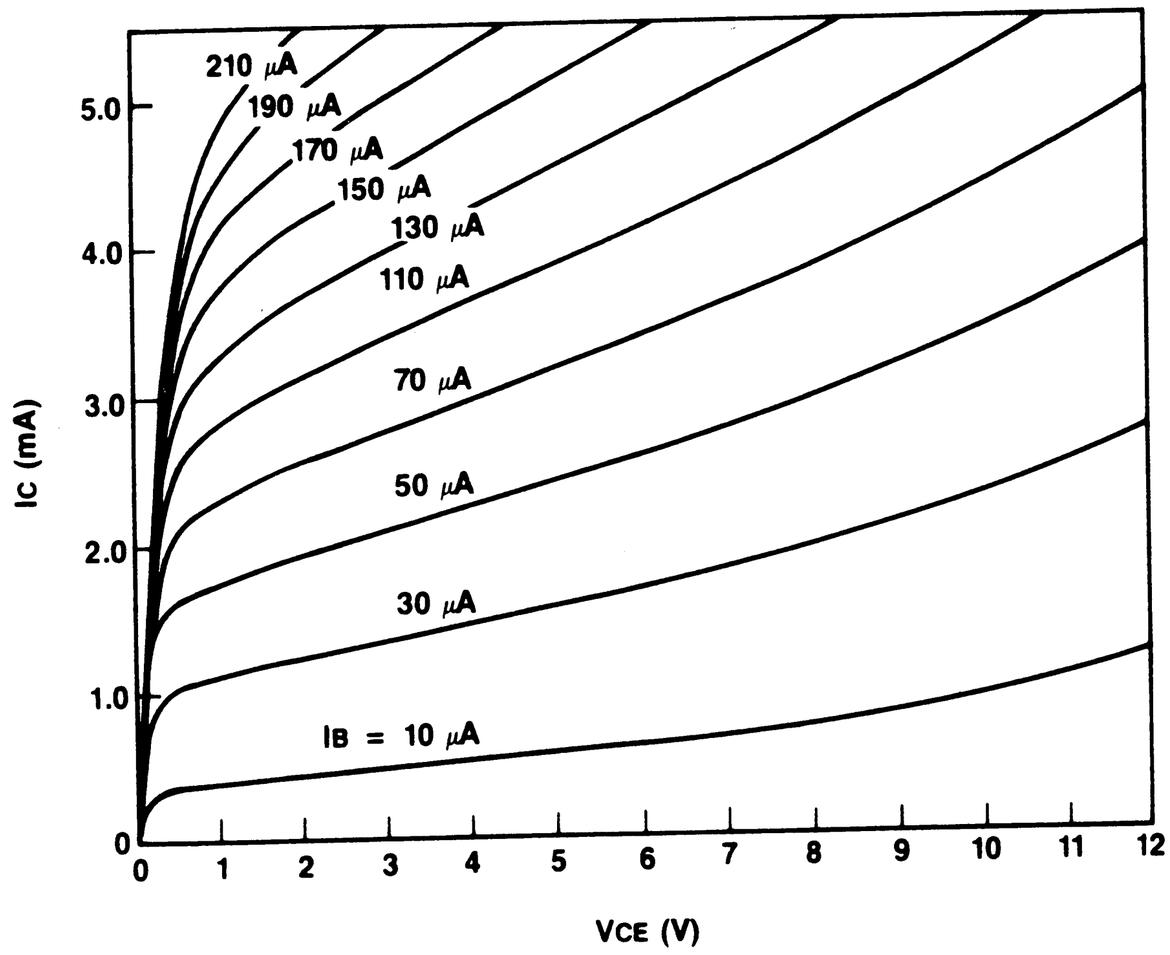
Current vs. Saturation Voltage for a Typical NU320PA 1X NPN



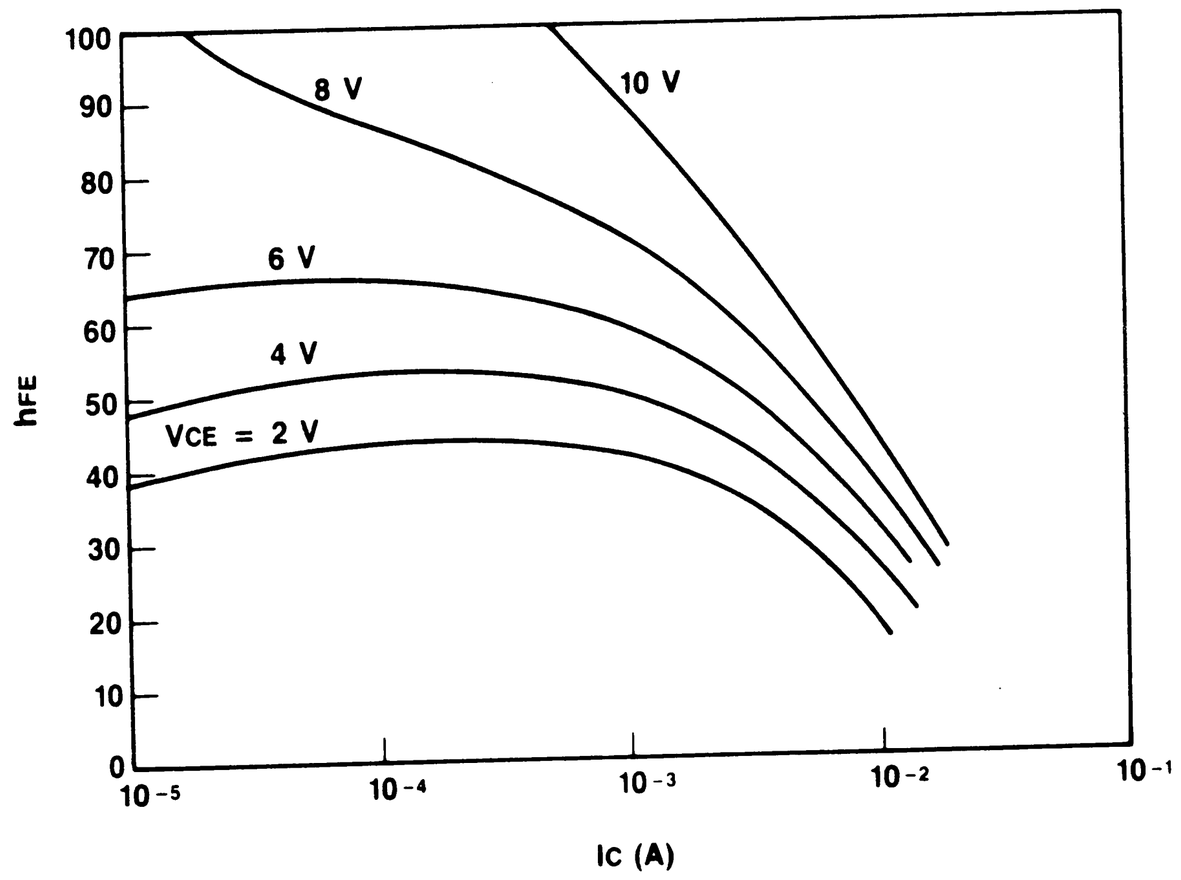
Current vs. Base-Emitter Voltage for a Typical NU320PA 1X NPN



Output Voltage Characteristics for a Typical NU320PA 1X NPN



Current Gain Characteristics for a Typical NU320PA 1X NPN



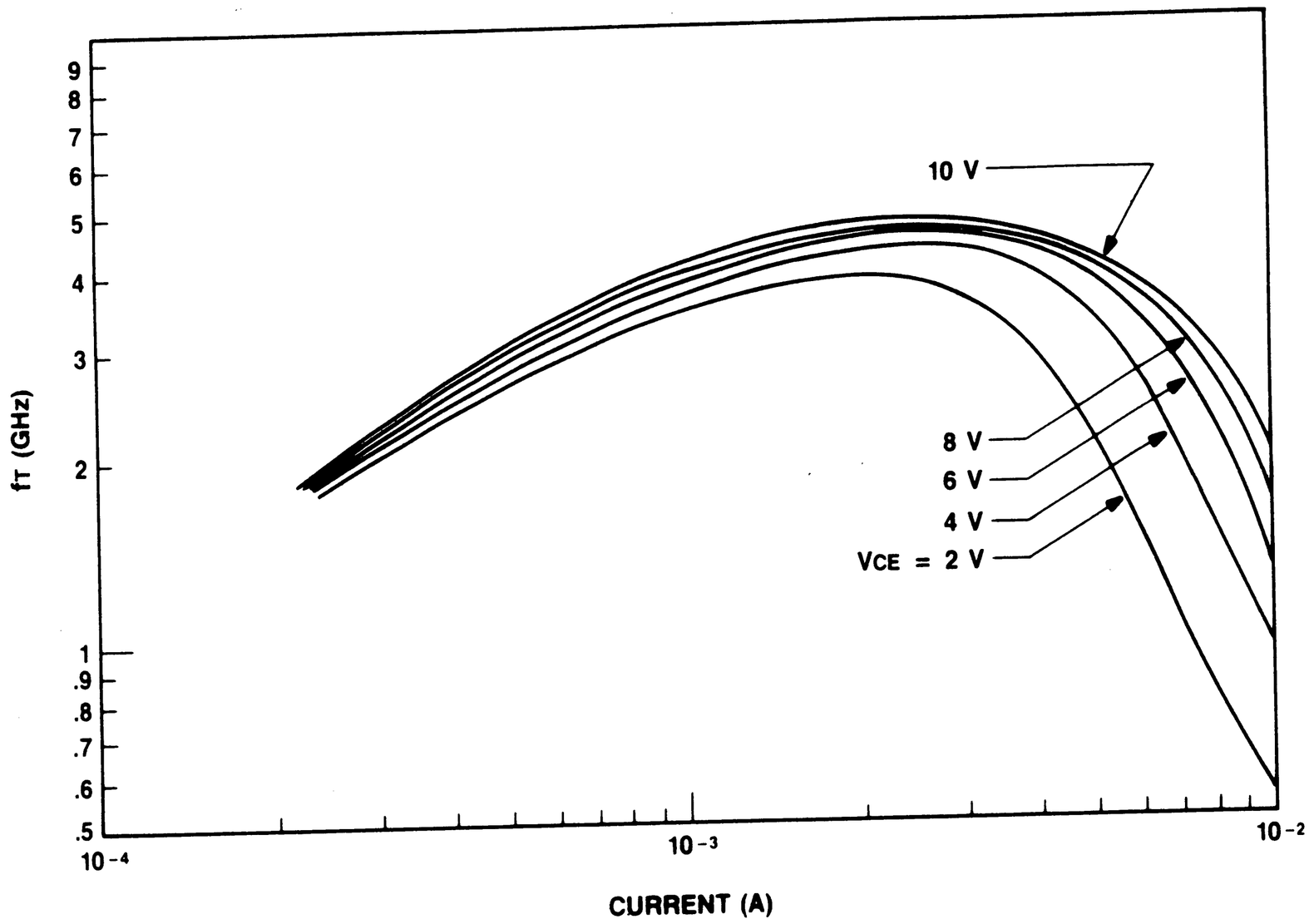
PNP TRANSISTOR ELECTRICAL CHARACTERISTICS

(All data is at T_{AMB}=25 °C)

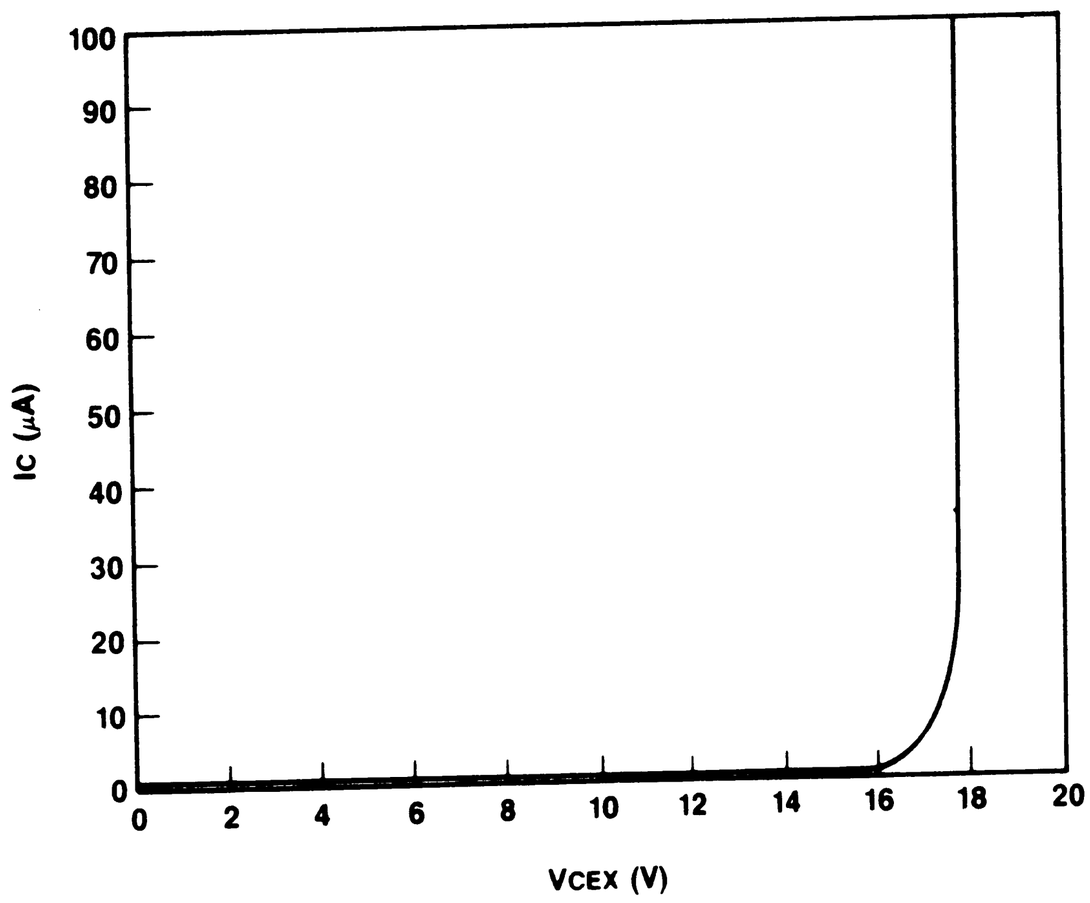
DC Parameters for the PU322PA 1X PNP

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}	I_C = 1 mA, V_{CE} = 2 V	80	110	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	3.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	20	40	—	V
$V_{CE\ (sat)}$	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}†	I_E = 1 mA, V_{CE} = 2 V	.720	.775	.820	V
BV_{CEX}	I_C = 100 μA, I_B = 0.1 μA	12	18	—	V
I_{EBO}	V_{EB} = 2 V, I_C = 0	—	.02	1	μA
BV_{CBO}	I_C = 1 μA	20	30	—	V
BV_{CSO} (collector substrate breakdown)	I_C = 1 μA	20	60	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	4.7	5.3	5.9	V

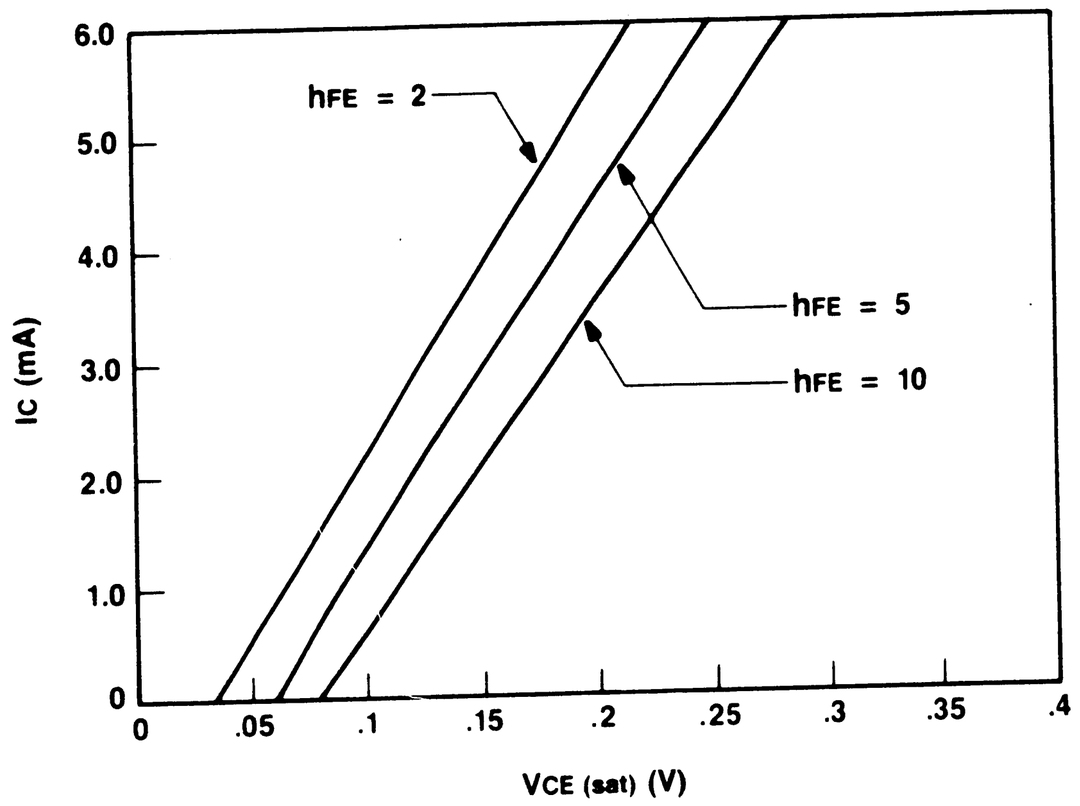
Frequency vs. Current for a Typical PU322PA 1X PNP



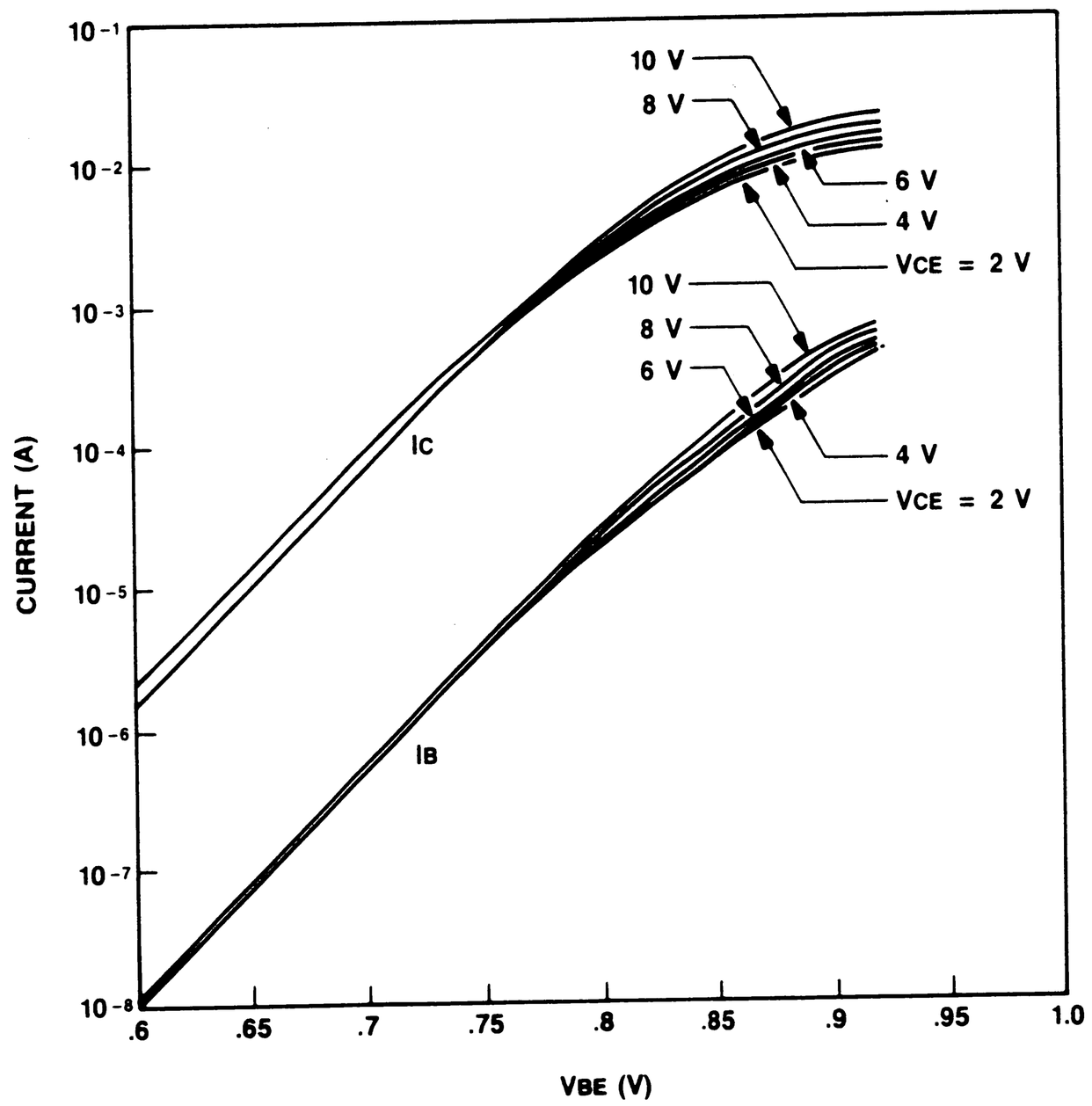
Current vs. Breakdown Voltage for a Typical PU322PA 1X PNP



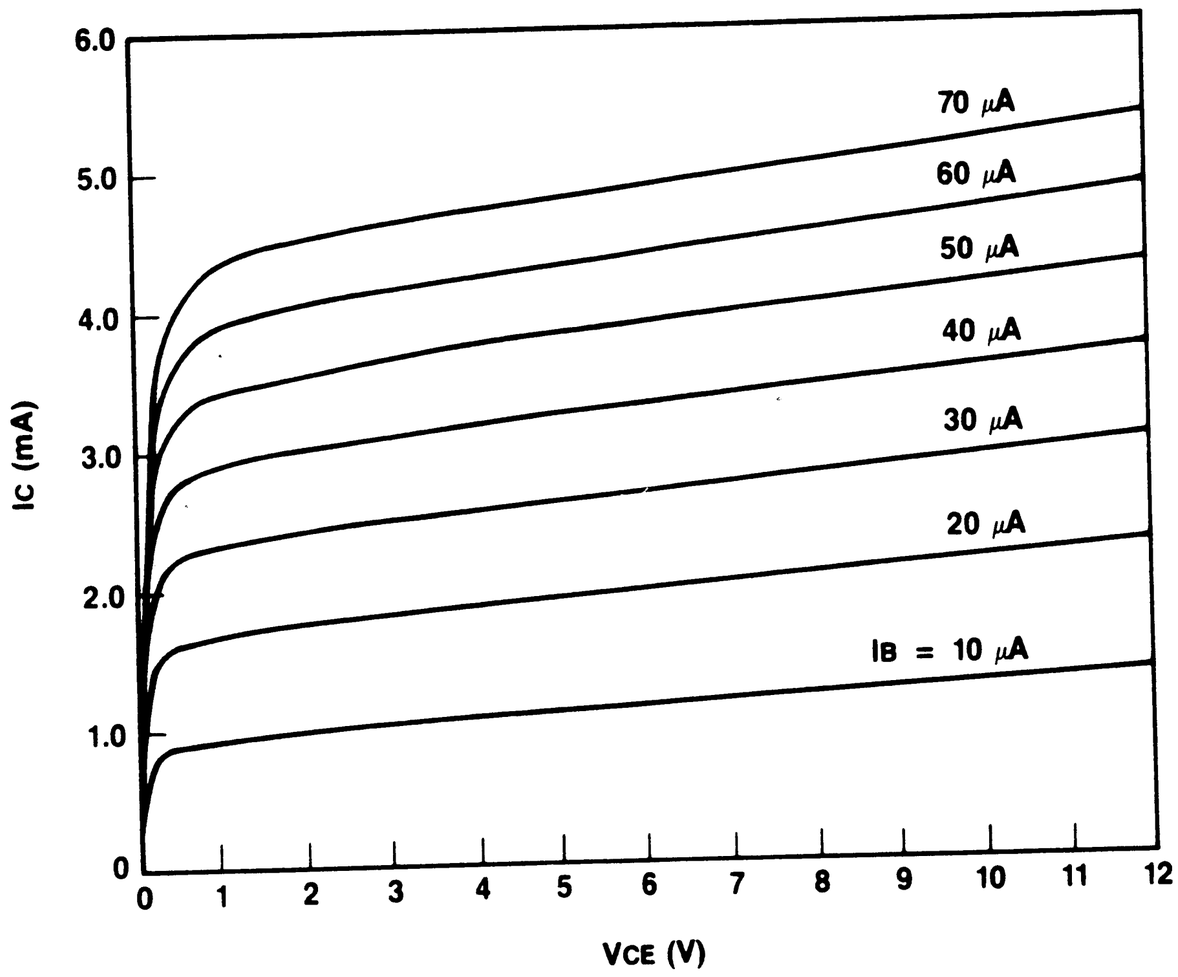
Current vs. Saturation Voltage for a Typical PU322PA 1X PNP



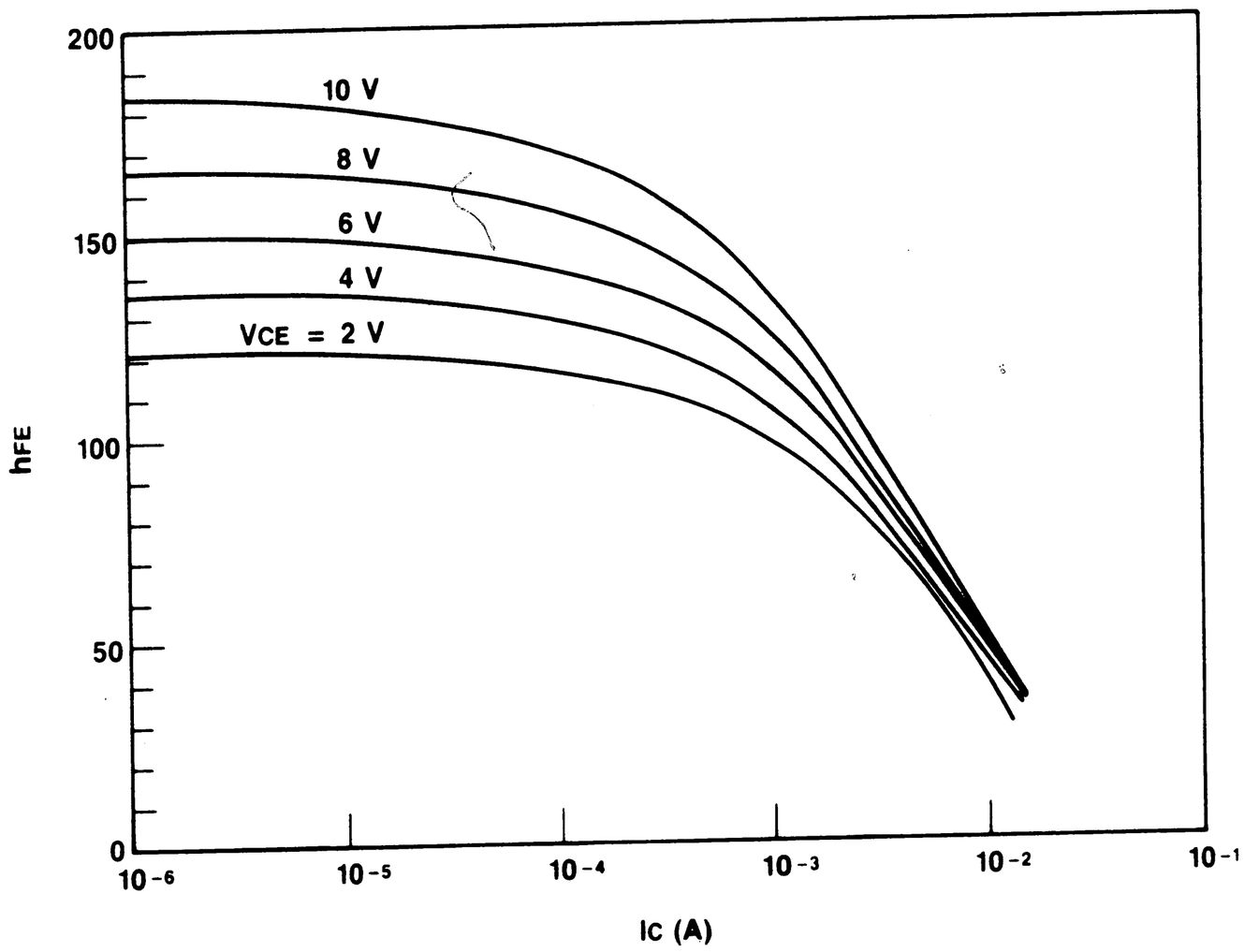
Current vs. Base-Emitter Voltage for a Typical PU322PA 1X PNP



Output Voltage Characteristics for a Typical PU322PA 1X PNP



Current Gain Characteristics for a Typical PU322PA 1X PNP



APPENDIX B

Model Parameters of Selected CBIC-U Components for ADVICE Simulation

The Bipolar Junction Transistor Model

The ADVICE models for the CBIC-U bipolar transistors follow the well-known formulation of Gummel-Poon, which models second-order effects such as nonideal base currents, gain fall-off at high current and basewidth modulation. The parameters that were included for these models are defined below. However, the actual values are the proprietary information of AT&T and cannot be released. For reference the equivalent SPICE model parameters have been provided.

Parameter	Definition	Unit
RBX	Extrinsic base resistance	ohm
RBI	Zero-bias intrinsic base resistance	ohm
RC	Extrinsic collector resistance	ohm
RE	Extrinsic emitter resistance	ohm
CCS	Collector-substrate capacitance	farad
CBS	Base-substrate capacitance	farad
IS	Transport saturation current	amp
I1	Ideal B-E saturation current	amp
I2	Nonideal B-E saturation current	amp
NE	B-E emission coefficient	-
IK	Forward knee current	amp
VBO	Zero-bias reverse Early voltage	volt
TFO	Zero-bias forward transit time	sec
CJE	Zero-bias B-E junction capacitance	farad
PE	B-E junction potential	volt
ME	B-E grading coefficient	-
BE	B-E maximum cap. coefficient	-
I3	Ideal B-C saturation current	amp
I4	Nonideal B-C saturation current	amp
NC	B-C emission coefficient	-
IKR	Reverse knee current	amp
VAO	Zero-bias forward bias Early voltage	volt

The Bipolar Junction Transistor Model - cont'd.

Parameter	Definition	Unit
TRO	Zero-bias reverse transit time	sec
CJC	Zero-bias B-C capacitance	farad
MC	B-C grading coefficient	-
PC	B-C junction potential	volt
BC	B-C maximum cap. coefficient	-
TD	Small-signal excess-phase delay	sec
EA	Activation energy for IS	eV
DEA	Delta EA for current gain	eV
TO	Referance temperature	°C
DTMP	Device offset temperature	°C
BVBC	B-C breakdown voltage	volt
ALC1	First B-C breakdown coefficient	$volt^{-1}$
ALC2	Second B-C breakdown coefficient	$volt^{-1}$
ALTC	B-C breakdown temp. exponent	-
BVBE	B-E breakdown voltage	volt
ALE1	First B-E breakdown coefficient	$volt^{-1}$
ALE2	Second B-E breakdown coefficient	$volt^{-1}$
ALTE	B-E breakdown temp. exponent	-
CJS	Zero-bias C-substrate capacitance	farad
PS	Substrate junction built-in potential	volt
MS	Substrate junction grading coeff.	-
BS	Substrate junction max. cap. coeff.	-
ISS	Saturation current of substrate trans.	amp
ISC	C-substrate saturation current	amp
IKS	Substrate knee current	amp
KFN	Flicker noise coefficient	-
AFN	Flicker noise current exponent	-
BFN	Flicker noise frequency exponent	-

SPICE Parameters for the low-gain npn transistor models:

```
* NPN1X - NU320PA TRANSISTOR
.MODEL NU320PA NPN RB=53.6 IRB=0 RBM=25.3 RC=54.3 RE=1.4
+IS=52.5E-18 EG=1.206 XTI=2 XTB=2.363 BF=100
+IKF=12E-3 NF=1 VAF=84 ISE=11.93E-16 NE=1.7
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=1.922E-20 NC=1.7
+TF=28P TR=5.25N CJE=1.81E-13 VJE=1.105 MJE=0.495
+CJC=2.04E-13 VJC=0.615 MJC=0.335 XCJC=0.138
+CJS=4.27E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=45E-3 VTF=10 XTF=30

* NPN2X - NU340PA TRANSISTOR
.MODEL NU340PA NPN RB=26.8 IRB=0 RBM=12.65 RC=27.15 RE=0.7
+IS=1.05E-16 EG=1.206 XTI=2 XTB=2.363 BF=100
+IKF=24E-3 NF=1 VAF=84 ISE=2.386E-15 NE=1.7
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=3.844E-20 NC=1.7
+TF=22P TR=6.25N CJE=3.62E-13 VJE=1.105 MJE=0.495
+CJC=3.323E-13 VJC=0.615 MJC=0.335 XCJC=0.17
+CJS=5.233E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=40E-3 VTF=10 XTF=30
```

SPICE Parameters for the nominal-gain npn transistor models:

```
* NU320PA - NPN1X TRANSISTOR
.MODEL NU320PA NPN RB=89.8 IRB=0 RBM=19.9 RC=46.05 RE=1.4
+IS=158E-18 EG=1.206 XTI=2 XTB=2.363 BF=220
+IKF=6.03E-3 NF=1 VAF=66 ISE=11.93E-16 NE=1.7
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=1.922E-20 NC=1.7
+TF=25P TR=3.75N CJE=1.2E-13 VJE=1.105 MJE=0.55
+CJC=1.73E-13 VJC=0.615 MJC=0.335 XCJC=0.138
+CJS=3.817E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=55E-3 VTF=10 XTF=15

* NU340PA - NPN2X TRANSISTOR
.MODEL NU340PA NPN RB=44.9 IRB=0 RBM=9.95 RC=23.02 RE=0.7
+IS=3.16E-16 EG=1.206 XTI=2 XTB=2.363 BF=220
+IKF=12E-3 NF=1 VAF=66 ISE=2.386E-15 NE=1.7
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=3.844E-20 NC=1.7
+TF=22P TR=4.25N CJE=2.4E-13 VJE=1.105 MJE=0.495
+CJC=2.815E-13 VJC=0.615 MJC=0.335 XCJC=0.17
+CJS=4.678E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=50E-3 VTF=10 XTF=15
```

SPICE Parameters for the high-gain npn transistor models:

```
* NPN1X - NU320PA TRANSISTOR
.MODEL NU320PA NPN RB=143.2 IRB=0 RBM=12.2 RC=37.8 RE=1.4
+IS=293E-18 EG=1.206 XTI=2 XTB=2.363 BF=380
+IKF=8E-3 NF=1 VAF=30 ISE=1.193E-15 NE=1.8
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=1.922E-20 NC=1.7
+TF=20P TR=1.75N CJE=0.89E-13 VJE=1.105 MJE=0.55
+CJC=1.42E-13 VJC=0.615 MJC=0.335 XCJC=0.138
+CJS=3.45E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=55E-3 VTF=10 XTF=10

* NPN2X - NU340PA TRANSISTOR
.MODEL NU340PA NPN RB=71.6 IRB=0 RBM=6.1 RC=18.9 RE=0.7
+IS=5.86E-16 EG=1.206 XTI=2 XTB=2.363 BF=380
+IKF=16E-3 NF=1 VAF=30 ISE=2.386E-15 NE=1.8
+BR=4 IKR=1E6 NR=1 VAR=3 ISC=3.844E-20 NC=1.7
+TF=19P TR=2N CJE=1.78E-13 VJE=1.105 MJE=0.495
+CJC=2.316E-13 VJC=0.615 MJC=0.335 XCJC=0.17
+CJS=4.227E-13 VJS=0.500 MJS=0.318 FC=0.5 ITF=55E-3 VTF=10 XTF=10
```

SPICE Parameters for the low-gain pnp transistor models:

```
* PNP1X - PU322PA TRANSISTOR - 2 COLLECTORS
.MODEL PU322PA PNP RB=52.61 IRB=0 RBM=33.81 RC=34.48 RE=0.6
+IS=5.32E-17 EG=1.206 XTI=1.5 XTB=2.053 BF=64
+IKF=15E-3 NF=1 VAF=50 ISE=13E-15 NE=1.557
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=2.49E-18 NC=1.634
+TF=65P TR=10.75N CJE=1.63E-13 VJE=0.8939 MJE=0.493
+CJC=3.81E-13 VJC=0.530 MJC=0.190 XCJC=0.138
+CJS=9.54E-13 VJS=0.600 MJS=0.348 FC=0.8 ITF=150E-3 VTF=10 XTF=5

* PNP2X - PU342PA TRANSISTOR - 2 COLLECTORS
.MODEL PU342PA PNP RB=26.31 IRB=0 RBM=16.91 RC=17.24 RE=0.3
+IS=1.064E-16 EG=1.206 XTI=1.5 XTB=2.053 BF=64
+IKF=30E-3 NF=1 VAF=50 ISE=26E-15 NE=1.557
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=4.98E-18 NC=1.634
+TF=68P TR=12.25N CJE=3.26E-13 VJE=0.8939 MJE=0.493
+CJC=6.199E-13 VJC=0.530 MJC=0.190 XCJC=0.1689
+CJS=1.168E-12 VJS=0.600 MJS=0.348 FC=0.8 ITF=150E-3 VTF=10 XTF=5
```

SPICE Parameters for the nominal-gain pnp transistor models:

```
* PU322PA - PNP1X TRANSISTOR - 2 COLLECTORS
.MODEL PU322PA PNP RB=71.4 IRB=0 RBM=25.66 RC=28.35 RE=0.6
+IS=12.1E-17 EG=1.206 XTI=1.5 XTB=2.053 BF=115
+IKF=15E-3 NF=1 VAF=30.0 ISE=6.1E-15 NE=1.557
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=2.49E-18 NC=1.634
+TF=36P TR=4.25N CJE=1.2E-13 VJE=0.8939 MJE=0.493
+CJC=3.3E-13 VJC=0.530 MJC=0.190 XCJC=0.138
+CJS=9.09E-13 VJS=0.600 MJS=0.348 FC=0.8 ITF=150E-3 VTF=10 XTF=4

* PU342PA - PNP2X TRANSISTOR - 2 COLLECTORS
.MODEL PU342PA PNP RB=35.68 IRB=0 RBM=12.83 RC=14.18 RE=0.3
+IS=2.42E-16 EG=1.206 XTI=1.5 XTB=2.053 BF=115
+IKF=30E-3 NF=1 VAF=30 ISE=12.1E-15 NE=1.557
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=4.98E-18 NC=1.634
+TF=36P TR=5.25N CJE=2.40E-13 VJE=0.8939 MJE=0.493
+CJC=5.374E-13 VJC=0.530 MJC=0.190 XCJC=0.1689
+CJS=1.113E-12 VJS=0.600 MJS=0.348 FC=0.8 ITF=150E-3 VTF=10 XTF=5
```

SPICE Parameters for the high-gain pnp transistor models:

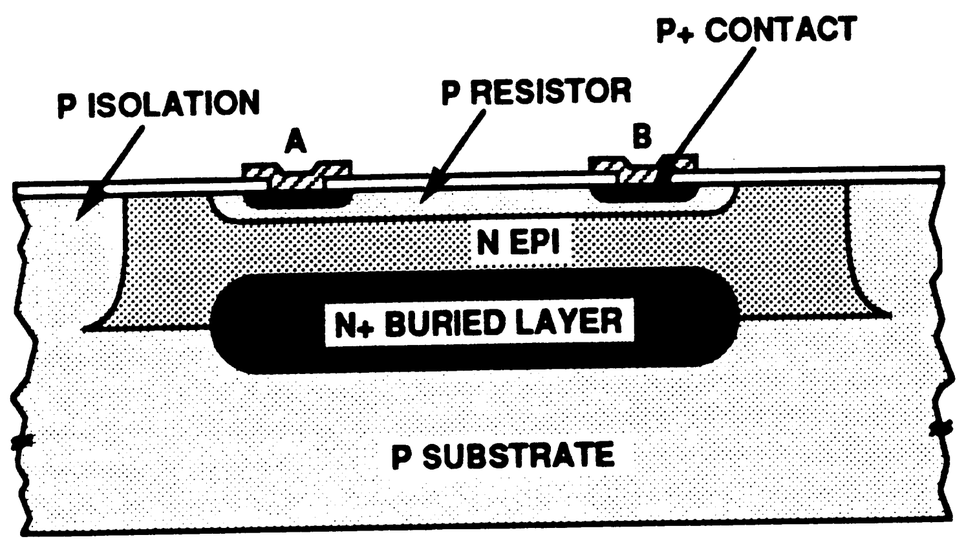
```
* PNP1X - PU322PA TRANSISTOR - 2 COLLECTORS
.MODEL PU322PA PNP RB=98.8 IRB=0 RBM=16.8 RC=22.17 RE=0.6
+IS=21.8E-17 EG=1.206 XTI=1.5 XTB=2.053 BF=190
+IKF=20E-3 NF=1 VAF=21 ISE=5.7E-15 NE=1.6
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=2.49E-18 NC=1.634
+TF=33P TR=1.25N CJE=89E-15 VJE=0.8939 MJE=0.493
+CJC=2.79E-13 VJC=0.530 MJC=0.190 XCJC=0.138
+CJS=8.63E-13 VJS=0.600 MJS=0.348 FC=0.8 ITF=130E-3 VTF=10 XTF=3

* PNP2X - PU342PA TRANSISTOR - 2 COLLECTORS
.MODEL PU342PA PNP RB=49.4 IRB=0 RBM=8.4 RC=11.09 RE=0.3
+IS=4.36E-16 EG=1.206 XTI=1.5 XTB=2.053 BF=190
+IKF=40E-3 NF=1 VAF=21 ISE=11.4E-15 NE=1.6
+BR=4 IKR=1E6 NR=1 VAR=1.4 ISC=4.98E-18 NC=1.634
+TF=32P TR=1.25N CJE=1.78E-13 VJE=0.8939 MJE=0.493
+CJC=4.539E-13 VJC=0.530 MJC=0.190 XCJC=0.1689
+CJS=1.057E-12 VJS=0.600 MJS=0.348 FC=0.8 ITF=150E-3 VTF=10 XTF=4
```

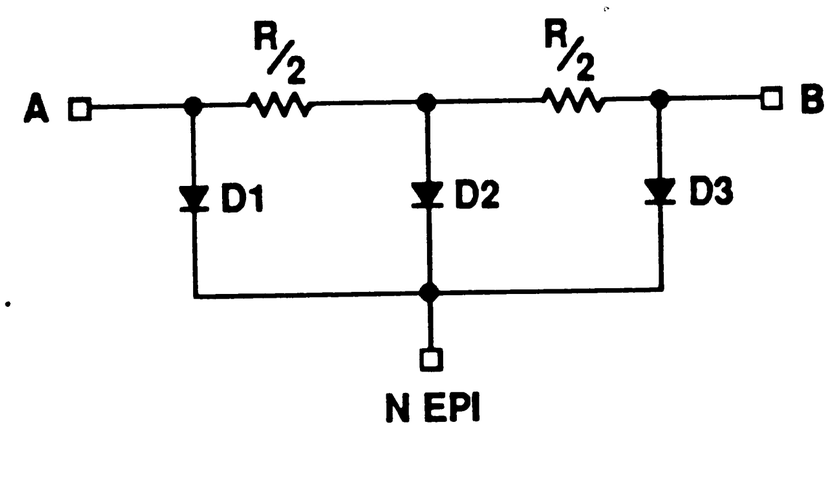
The Diffused Resistor Model

The CBIC-U resistors are modeled as shown below to account for parasitic junctions.

1. Schematic Representation



2. Diffused Resistor Structure



3. Model to Approximate Distributed Junction

The formulation for resistor elements includes a quadratic dependence of resistance value upon temperature. The pn junction diode model contains series resistance and junction capacitance. The parameters that were included for the resistors and pn junction diodes that comprise the ADVICE model are defined and

tabulated below. However, the actual values are the proprietary information of AT&T and cannot be released. For reference the equivalent SPICE model parameters have been provided.

The Resistor Model

Parameter	Definition	Unit
TC1	First-order temperature coeff.	ppm/°C
TC2	Second-order temperature coeff.	ppm/°C

The PN Junction Diode Model

Parameter	Definition	Unit
RS	Series resistance	ohm
I1	Ideal saturation current	amp
CJO1	First zero-bias junction cap.	farad

SPICE Parameters for the low-sheet resistor models:

```
* RU50 - 50 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=50, W=10}
.MODEL RLO RES (R=0.80 TC1=1.382E-3 TC2=1.138E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.1597E-12 VJ=0.675 M=0.326)
.SUBCKT RU50 (1, 2, 3)
  DR1 (1,3) DR (0.15824)
  DR2 (4,3) DR (0.073138)
  DR3 (2,3) DR (0.15824)
  R1 (1,4) RLO 25
  R2 (4,2) RLO 25
.ENDS

* RU1K - 1080 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=1K, W=10}
.MODEL RHI RES (R=0.80 TC1=1.769E-3 TC2=5.638E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.1597E-12 VJ=0.675 M=0.326)
.SUBCKT RU1K (1, 2, 3)
  DR1 (1,3) DR (0.15824)
  DR2 (4,3) DR (0.073138)
  DR3 (2,3) DR (0.15825)
  R1 (1,4) RHI 500
  R2 (4,2) RHI 500
.ENDS
```

SPICE Parameters for the nominal-sheet resistor models:

```
* RU50 - 50 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=50, W=10}
.MODEL RLO RES (R=1.00 TC1=1.382E-3 TC2=1.138E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.1785E-12 VJ=0.675 M=0.326)
.SUBCKT RU50 (1, 2, 3)
  DR1 (1,3) DR (0.17287)
  DR2 (4,3) DR (0.079787)
  DR3 (2,3) DR (0.17287)
  R1 (1,4) RLO 25
  R2 (4,2) RLO 25
.ENDS

* RU1K - 1080 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=1K, W=10}
.MODEL RHI RES (R=1.00 TC1=1.769E-3 TC2=5.638E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.1785E-12 VJ=0.675 M=0.326)
.SUBCKT RU1K (1, 2, 3)
  DR1 (1,3) DR (0.17287)
  DR2 (4,3) DR (0.079787)
  DR3 (2,3) DR (0.17287)
  R1 (1,4) RHI 500
  R2 (4,2) RHI 500
.ENDS
```

SPICE Parameters for the high-sheet resistor models:

```
* RU50 - 50 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=50, W=10}
.MODEL RLO RES (R=1.20 TC1=1.382E-3 TC2=1.138E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.2060E-12 VJ=0.675 M=0.326)
.SUBCKT RU50 (1, 2, 3)
  DR1 (1,3) DR (0.18750)
  DR2 (4,3) DR (0.086436)
  DR3 (2,3) DR (0.18750)
  R1 (1,4) RLO 25
  R2 (4,2) RLO 25
.ENDS

* RU1K - 1080 OHM PER SQUARE RESISTOR SUBCIRCUIT {R=1K, W=10}

.MODEL RHI RES (R=1.20 TC1=1.769E-3 TC2=5.638E-6)
.MODEL DR D (RS=5 IS=3.0E-16 CJO=0.2060E-12 VJ=0.675 M=0.326)
.SUBCKT RU1K (1, 2, 3)
  DR1 (1,3) DR (0.18750)
  DR2 (4,3) DR (0.086436)
  DR3 (2,3) DR (0.18750)
  R1 (1,4) RHI 500
  R2 (4,2) RHI 500
.ENDS
```

APPENDIX C

Input Netlist for ADVICE Simulation

of Nominal VCO Circuit

```
* uhf vco nominal circuit
* advice input netlist
* douglas a. williams
*
*
* transistors:
*
q1 vsp vsp c5 nu320pa
q2 vsp vsp c6 nu320pa
q3 vsp c5 b6 nu320pa
q4 vsp c6 b5 nu320pa
q5 c5 b5 e5 nu320pa
q6 c6 b6 e6 nu320pa
q7 c7 vref e7 nu320pa
q8 c7 vref e7 nu320pa
q9 e5 vin e9 nu320pa
q10 e6 vin e9 nu320pa
q11 c11 bias 0 nu320pa
q12 e5 bias 0 nu320pa
q13 b5 bias 0 nu320pa
q14 b6 bias 0 nu320pa
q15 e6 bias 0 nu320pa
q16 b18 b16 vsp pu320pa
q17 b16 b16 vsp pu320pa
q18 b16 b18 e18 nu320pa
q20 c20 b20 0 nu320pa
q21 c21 bias 0 nu320pa
q22 vsp c21 bias nu320pa
*
* resistors:
*
r1 vsp c5 rmod1 2k
r2 vsp c6 rmod1 2k
r3 vsp c7 rmod1 200
r4 e7 c11 rmod1 150
r5 e9 c11 rmod1 150
r6 e18 c21 rmod1 1020
r7 c20 b20 rmod1 2770
r8 b20 0 rmod1 10k
*
* capacitor:
*
cx e5 e6 1e-12
*
* power supply:
*
vsp vsp 0 10
*
* jumpstart current source:
*
istart e5 e6 table(0 0 0.1ns 5e-3 0.2ns 5e-3 0.3ns 0)
*
* frequency tuning voltage sources:
*
```

```
vref vref 0 5
vin vin 0 4
*
* zener diode model:
*
vz z c20 vzen 5.60
rz b18 z 25.5
.model vzen v (TC1=288.7)
*
.end
```

APPENDIX D

DC Operating Points of

Nominal VCO Circuit

DC operating point analysis completed in 21 iterations

***** node voltages

Node	Voltage	Node	Voltage	Node	Voltage
(0)	0.00000e+00	(B16)	9.15332e+00	(B18)	7.07633e+00
(B20)	8.46900e-01	(B5)	8.31655e+00	(B6)	8.31655e+00
(BIAS)	8.38576e-01	(C11)	3.48418e+00	(C20)	1.33660e+00
(C21)	1.58175e+00	(C5)	9.16036e+00	(C6)	9.16036e+00
(C7)	9.06304e+00	(E18)	6.23990e+00	(E5)	7.47412e+00
(E6)	7.47412e+00	(E7)	4.19471e+00	(E9)	3.48419e+00
(VIN)	4.00000e+00	(VREF)	5.00000e+00	(VSP)	1.00000e+01
(Z)	6.93660e+00				

***** resistor operating points

name	current	voltage	power	value
R1	4.198e-04	.840	3.525e-04	2.000e+03
R2	4.198e-04	.840	3.525e-04	2.000e+03
R3	4.685e-03	.937	4.389e-03	2.000e+02
R4	4.737e-03	.711	3.366e-03	1.500e+02
R5	1.291e-07	.000	2.500e-12	1.500e+02
R6	4.567e-03	4.658	2.127e-02	1.020e+03
R7	1.768e-04	.490	8.657e-05	2.770e+03
R8	8.469e-05	.847	7.172e-05	1.000e+04
RZ	5.479e-03	.140	7.656e-04	2.550e+01

***** capacitor operating points

name	current	voltage	power	value
CX	0.000e+00	.000	0.000e+00	1.000e-12

***** independent current source operating points

name	current	voltage	power
ISTART	0.000e+00	.000	0.000e+00

***** independent voltage source operating points

name	current	voltage	power
VSP	-3.529e-02	10.000	-3.529e-01
VREF	-5.209e-05	5.000	-2.604e-04
VIN	-1.032e-09	4.000	-4.129e-09
VZ	5.479e-03	5.600	3.068e-02

***** BJT operating points

name	ib	ic	vbe	vbc	vce	beta	power	rci-mod
Q1	7.613e-05	4.516e-03	.840	.000	.840	59.3	3.855e-03	1.157
Q2	7.613e-05	4.516e-03	.840	.000	.840	59.3	3.855e-03	1.157
Q3	8.439e-05	5.057e-03	.844	-.840	1.683	59.9	8.584e-03	1.275
Q4	8.439e-05	5.057e-03	.844	-.840	1.683	59.9	8.584e-03	1.275
Q5	8.124e-05	4.927e-03	.842	-.844	1.686	60.6	8.377e-03	1.266
Q6	8.124e-05	4.927e-03	.842	-.844	1.686	60.6	8.377e-03	1.266
Q7	2.604e-05	2.342e-03	.805	-4.063	4.868	89.9	1.142e-02	1.111
Q8	2.604e-05	2.342e-03	.805	-4.063	4.868	89.9	1.142e-02	1.111
Q9	5.161e-10	6.404e-08	.516	-3.474	3.990	124.1	2.558e-07	1.000
Q10	5.161e-10	6.404e-08	.516	-3.474	3.990	124.1	2.558e-07	1.000
Q11	7.206e-05	4.737e-03	.839	-2.646	3.484	65.7	1.657e-02	1.253

Q12	7.051e-05	5.008e-03	.839	-6.636	7.474	71.0	3.749e-02	1.27
2								
Q13	7.022e-05	5.060e-03	.839	-7.478	8.317	72.1	4.214e-02	1.27
5								
Q14	7.022e-05	5.060e-03	.839	-7.478	8.317	72.1	4.214e-02	1.27
5								
Q15	7.051e-05	5.008e-03	.839	-6.636	7.474	71.0	3.749e-02	1.27
2								
Q16	-1.711e-04	-5.547e-03	-.847	2.077	-2.924	32.4	1.636e-02	1.52
8								
Q17	-1.907e-04	-4.137e-03	-.847	.000	-.847	21.7	3.664e-03	1.10
1								
Q18	6.808e-05	4.499e-03	.836	-2.077	2.913	66.1	1.316e-02	1.23
8								
Q20	9.210e-05	5.302e-03	.847	-.490	1.337	57.6	7.165e-03	1.29
2								
Q21	7.307e-05	4.564e-03	.839	-.743	1.582	62.5	7.280e-03	1.24
2								
Q22	2.847e-06	4.238e-04	.743	-8.418	9.161	148.8	3.884e-03	1.01
8								

APPENDIX E

Input Netlist for ADVICE Simulation of Component-Extracted VCO Circuit

```
* uhf vco w/ extracted parasitics
* advice input netlist
* douglas a. williams
*
*
* transistors:
*
   B3        (#104,#104,#21,#21)  PU322PA;* standb#1/q17
   B4        (#118,#104,#21,#21)  PU322PA;* standb#1/q16
   B15       (#104,#118,#83,gnd)  NU320PA;* standb#1/q18
   B16       (#21,#130,#32,gnd)  NU320PA;* standb#1/q22
   B17       (#130,#32,gnd,gnd)  NU320PA;* standb#1/q21
   B18       (#143,#66,gnd,gnd)  NU320PA;* standb#1/q20
   B116      (#21,#21,vout2,gnd)  NU340PA;* standd#1/q1
   B117      (#21,#21,vout1,gnd)  NU340PA;* standd#1/q2
   B119      (#2,#32,gnd,gnd)  NU320PA;* standd#1/q15
   B120      (#38,#32,gnd,gnd)  NU320PA;* standd#1/q14
   B121      (#61,#32,gnd,gnd)  NU320PA;* standd#1/q13
   B122      (#1,#32,gnd,gnd)  NU320PA;* standd#1/q12
   B123      (vout2,#61,#1,gnd)  NU340PA;* standd#1/q5
   B124      (#21,vout1,#61,gnd)  NU320PA;* standd#1/q4
   B125      (#21,vout2,#38,gnd)  NU320PA;* standd#1/q3
   B126      (vout1,#38,#2,gnd)  NU340PA;* standd#1/q6
   B335      (#2,vin,#210,gnd)  NU320PA;* standc#1/q10
   B336      (#1,vin,#210,gnd)  NU320PA;* standc#1/q9
   B337      (#235,vref,#242,gnd)  NU320PA;* standc#1/q8
   B338      (#235,vref,#242,gnd)  NU320PA;* standc#1/q7
   B339      (#248,#32,gnd,gnd)  NU320PA;* standc#1/q11
*
* resistors:
*
   XR50      (#140,#66,#21)  RU1K {R=2K,W=10};* standb#1/r7a
   XR56      (#66,#60,#21)  RU1K {R=2K,W=10};* standb#1/r8c
   XR81      (#119,#108,#21)  RU50 {R=100,W=10};* standb#1/r7g
   XR82      (#108,#105,#21)  RU50 {R=100,W=10};* standb#1/r7f
   XR83      (#143,#133,#21)  RU50 {R=100,W=10};* standb#1/r7i
   XR84      (#133,#119,#21)  RU50 {R=100,W=10};* standb#1/r7h
   XR89      (#140,#134,#21)  RU50 {R=100,W=10};* standb#1/r7b
   XR90      (#134,#120,#21)  RU50 {R=100,W=10};* standb#1/r7c
   XR91      (#120,#109,#21)  RU50 {R=100,W=10};* standb#1/r7d
   XR92      (#109,#105,#21)  RU50 {R=100,W=10};* standb#1/r7e
   XR97      (#60,#45,#21)  RU1K {R=4K,W=10};* standb#1/r8b
   XR98      (#45,gnd,#21)  RU1K {R=4K,W=10};* standb#1/r8a
   XR147     (#21,vout2,#21)  RU1K {R=2K,W=10};* standd#1/r1b
   XR148     (vout2,#21,#21)  RU1K {R=2K,W=10};* standd#1/r1a
   XR149     (#21,vout1,#21)  RU1K {R=2K,W=10};* standd#1/r2b
   XR150     (vout1,#21,#21)  RU1K {R=2K,W=10};* standd#1/r2a
   XR383     (#284,#273,#21)  RU50 {R=100,W=10};* standc#1/r3e
   XR384     (#273,#21,#21)  RU50 {R=100,W=10};* standc#1/r3f
   XR397     (#284,#272,#21)  RU50 {R=100,W=10};* standc#1/r3d
   XR398     (#272,#261,#21)  RU50 {R=100,W=10};* standc#1/r3c
   XR399     (#261,#249,#21)  RU50 {R=100,W=10};* standc#1/r3b
   XR400     (#249,#235,#21)  RU50 {R=100,W=10};* standc#1/r3a
   XR401     (#234,#210,#21)  RU50 {R=100,W=10};* standc#1/r5b
   XR402     (#210,#234,#21)  RU50 {R=100,W=10};* standc#1/r5a
```

```
* uhf vco w/ extracted parasitics
* advice input netlist
* douglas a. williams
*
*
* transistors:
*
   B3        (#104,#104,#21,#21)  PU322PA;* standb#1/q17
   B4        (#118,#104,#21,#21)  PU322PA;* standb#1/q16
   B15       (#104,#118,#83,gnd)  NU320PA;* standb#1/q18
   B16       (#21,#130,#32,gnd)   NU320PA;* standb#1/q22
   B17       (#130,#32,gnd,gnd)   NU320PA;* standb#1/q21
   B18       (#143,#66,gnd,gnd)   NU320PA;* standb#1/q20
   B116      (#21,#21,vout2,gnd)  NU340PA;* standd#1/q1
   B117      (#21,#21,vout1,gnd)  NU340PA;* standd#1/q2
   B119      (#2,#32,gnd,gnd)   NU320PA;* standd#1/q15
   B120      (#38,#32,gnd,gnd)   NU320PA;* standd#1/q14
   B121      (#61,#32,gnd,gnd)   NU320PA;* standd#1/q13
   B122      (#1,#32,gnd,gnd)   NU320PA;* standd#1/q12
   B123      (vout2,#61,#1,gnd)  NU340PA;* standd#1/q5
   B124      (#21,vout1,#61,gnd)  NU320PA;* standd#1/q4
   B125      (#21,vout2,#38,gnd)  NU320PA;* standd#1/q3
   B126      (vout1,#38,#2,gnd)  NU340PA;* standd#1/q6
   B335      (#2,vin,#210,gnd)  NU320PA;* standc#1/q10
   B336      (#1,vin,#210,gnd)  NU320PA;* standc#1/q9
   B337      (#235,vref,#242,gnd)  NU320PA;* standc#1/q8
   B338      (#235,vref,#242,gnd)  NU320PA;* standc#1/q7
   B339      (#248,#32,gnd,gnd)  NU320PA;* standc#1/q11
*
* resistors:
*
   XR50      (#140,#66,#21)  RU1K {R=2K,W=10};* standb#1/r7a
   XR56      (#66,#60,#21)  RU1K {R=2K,W=10};* standb#1/r8c
   XR81      (#119,#108,#21)  RU50 {R=100,W=10};* standb#1/r7g
   XR82      (#108,#105,#21)  RU50 {R=100,W=10};* standb#1/r7f
   XR83      (#143,#133,#21)  RU50 {R=100,W=10};* standb#1/r7i
   XR84      (#133,#119,#21)  RU50 {R=100,W=10};* standb#1/r7h
   XR89      (#140,#134,#21)  RU50 {R=100,W=10};* standb#1/r7b
   XR90      (#134,#120,#21)  RU50 {R=100,W=10};* standb#1/r7c
   XR91      (#120,#109,#21)  RU50 {R=100,W=10};* standb#1/r7d
   XR92      (#109,#105,#21)  RU50 {R=100,W=10};* standb#1/r7e
   XR97      (#60,#45,#21)  RU1K {R=4K,W=10};* standb#1/r8b
   XR98      (#45,gnd,#21)  RU1K {R=4K,W=10};* standb#1/r8a
   XR147     (#21,vout2,#21)  RU1K {R=2K,W=10};* standd#1/r1b
   XR148     (vout2,#21,#21)  RU1K {R=2K,W=10};* standd#1/r1a
   XR149     (#21,vout1,#21)  RU1K {R=2K,W=10};* standd#1/r2b
   XR150     (vout1,#21,#21)  RU1K {R=2K,W=10};* standd#1/r2a
   XR383     (#284,#273,#21)  RU50 {R=100,W=10};* standc#1/r3e
   XR384     (#273,#21,#21)  RU50 {R=100,W=10};* standc#1/r3f
   XR397     (#284,#272,#21)  RU50 {R=100,W=10};* standc#1/r3d
   XR398     (#272,#261,#21)  RU50 {R=100,W=10};* standc#1/r3c
   XR399     (#261,#249,#21)  RU50 {R=100,W=10};* standc#1/r3b
   XR400     (#249,#235,#21)  RU50 {R=100,W=10};* standc#1/r3a
   XR401     (#234,#210,#21)  RU50 {R=100,W=10};* standc#1/r5b
   XR402     (#210,#234,#21)  RU50 {R=100,W=10};* standc#1/r5a
```

```
   XR403     (#265,#242,#21)   RU50 {R=100,W=10};* standc#1/r4b
   XR404     (#242,#265,#21)   RU50 {R=100,W=10};* standc#1/r4a
   XR418     (#248,#265,#21)   RU50 {R=100,W=10};* standc#1/r4c
   XR420     (#248,#234,#21)   RU50 {R=100,W=10};* standc#1/r5c
*
* capacitor:
*
   XC130     (#2,#1,gnd)   C3T {C=1PF};* standd#1/cap1p50#2
*
* power supplies:
*
vsp #21 0 10
vgnd gnd 0 0
*
* jumpstart current source:
*
istart #1 #2 table(0 0 0.1ns 5e-3 0.2ns 5e-3 0.3ns 0)
*
* frequency tuning voltage sources:
*
vref vref 0 5
vin vin 0 4
*
* external resistor:
*
r6ext #83 #130 1020
*
* zener diode model
*
vz #z #143 vzen 5.60
rz #118 #z 25.5
.model vzen v (TC1=288.7)
*
* extracted parasitics:
*
   CD1        #1        gnd       botsub    (1.673E-13, 3.046E+03, 2.000E+02)
   CD2        #2        gnd       botsub    (7.903E-14, 1.350E+03, 1.855E+02)
   CD3        gnd       gnd       botsub    (1.621E-12, 3.060E+04, 8.275E+02)
   CD8        vout2     gnd       botsub    (3.223E-13, 5.959E+03, 2.920E+02)
   CD9        vout1     gnd       botsub    (3.278E-13, 6.006E+03, 3.535E+02)
   CD13       #21       gnd       botsub    (1.016E-12, 1.831E+04, 1.408E+03)
   CD17       #32       gnd       botsub    (3.375E-13, 5.974E+03, 5.790E+02)
   CD19       #38       gnd       botsub    (7.624E-14, 1.359E+03, 1.215E+02)
   CD25       #45       gnd       botsub    (3.304E-15, 6.400E+01, 0.000E+00)
   CD38       #60       gnd       botsub    (1.564E-14, 3.030E+02, 0.000E+00)
   CD39       #61       gnd       botsub    (1.123E-13, 2.097E+03, 8.000E+01)
   CD40       #66       gnd       botsub    (7.070E-14, 1.317E+03, 5.400E+01)
   CD53       #83       gnd       botsub    (1.105E-13, 1.988E+03, 1.575E+02)
   CD71       #104      gnd       botsub    (1.085E-13, 1.869E+03, 2.400E+02)
   CD72       #105      gnd       botsub    (1.229E-14, 2.380E+02, 0.000E+00)
   CD75       #108      gnd       botsub    (3.304E-15, 6.400E+01, 0.000E+00)
   CD76       #109      gnd       botsub    (3.304E-15, 6.400E+01, 0.000E+00)
   CD84       #118      gnd       botsub    (1.604E-13, 2.865E+03, 2.490E+02)
   CD85       #119      gnd       botsub    (1.745E-14, 3.380E+02, 0.000E+00)
   CD86       #120      gnd       botsub    (1.745E-14, 3.380E+02, 0.000E+00)
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CD94	#130	gnd	botsub	(6.334E-14, 1.088E+03, 1.430E+02)
CD97	#133	gnd	botsub	(3.304E-15, 6.400E+01, 0.000E+00)
CD98	#134	gnd	botsub	(3.304E-15, 6.400E+01, 0.000E+00)
CD104	#140	gnd	botsub	(1.974E-14, 3.630E+02, 2.000E+01)
CD107	#143	gnd	botsub	(1.338E-13, 2.341E+03, 2.580E+02)
CD151	vin	gnd	botsub	(1.036E-13, 1.773E+03, 2.400E+02)
CD152	#210	gnd	botsub	(1.106E-13, 2.103E+03, 4.000E+01)
CD173	#234	gnd	botsub	(3.220E-14, 5.945E+02, 3.000E+01)
CD174	#235	gnd	botsub	(6.682E-14, 1.197E+03, 1.000E+02)
CD175	#242	gnd	botsub	(9.442E-14, 1.829E+03, 0.000E+00)
CD176	vref	gnd	botsub	(9.025E-14, 1.684E+03, 6.600E+01)
CD181	#248	gnd	botsub	(1.234E-13, 2.313E+03, 8.000E+01)
CD182	#249	gnd	botsub	(3.304E-15, 6.400E+01, 0.000E+00)
CD194	#261	gnd	botsub	(1.745E-14, 3.380E+02, 0.000E+00)
CD195	#265	gnd	botsub	(3.220E-14, 5.945E+02, 3.000E+01)
CD202	#272	gnd	botsub	(3.304E-15, 6.400E+01, 0.000E+00)
CD203	#273	gnd	botsub	(3.304E-15, 6.400E+01, 0.000E+00)
CD214	#284	gnd	botsub	(1.329E-14, 2.380E+02, 2.000E+01)
CF303	#1	gnd	topsub	(3.424E-13, 1.246E+04, 4.850E+02)
CF304	#2	gnd	topsub	(3.857E-13, 1.420E+04, 4.425E+02)
CF305	gnd	gnd	topsub	(9.152E-12, 3.451E+05, 5.655E+03)
CF310	vout2	gnd	topsub	(4.046E-13, 1.524E+04, 2.630E+02)
CF311	vout1	gnd	topsub	(4.134E-13, 1.541E+04, 3.635E+02)
CF315	#21	gnd	topsub	(5.770E-12, 2.179E+05, 3.384E+03)
CF319	#32	gnd	topsub	(7.884E-13, 2.716E+04, 2.031E+03)
CF321	#38	gnd	topsub	(1.955E-13, 6.752E+03, 4.925E+02)
CF322	#61	gnd	topsub	(7.276E-14, 2.552E+03, 1.600E+02)
CF323	#66	gnd	topsub	(1.517E-13, 5.350E+03, 3.160E+02)
CF326	#83	gnd	topsub	(4.348E-13, 1.668E+04, 1.000E+02)
CF328	#130	gnd	topsub	(4.266E-13, 1.633E+04, 1.200E+02)
CF336	vin	gnd	topsub	(5.153E-13, 1.918E+04, 4.720E+02)
CF340	vref	gnd	topsub	(4.545E-13, 1.758E+04, 2.000E+01)
CF341	#248	gnd	topsub	(1.769E-14, 5.520E+02, 8.000E+01)
CH353	#1	#2	topbot	(6.965E-15, 9.600E+01, 4.000E+01)
CH354	#1	gnd	topbot	(7.989E-15, 1.548E+02, 0.000E+00)
CH355	vout2	#1	topbot	(7.744E-15, 1.500E+02, 0.000E+00)
CH356	vout1	#1	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH357	#2	vout2	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH358	vout2	gnd	topbot	(7.757E-15, 1.502E+02, 0.000E+00)
CH359	#2	vout1	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH360	gnd	vout1	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH362	#2	#21	topbot	(5.162E-15, 1.000E+02, 0.000E+00)
CH363	gnd	#21	topbot	(6.742E-14, 1.306E+03, 0.000E+00)
CH364	vout1	vout2	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH365	#32	#1	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH366	#21	vout2	topbot	(1.291E-14, 2.500E+02, 0.000E+00)
CH367	#32	gnd	topbot	(4.459E-14, 8.638E+02, 0.000E+00)
CH368	vout1	#21	topbot	(2.065E-14, 4.000E+02, 0.000E+00)
CH369	#32	vout2	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH370	#32	vout1	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH372	#38	vout2	topbot	(2.581E-15, 5.000E+01, 0.000E+00)
CH373	#21	#32	topbot	(5.162E-15, 1.000E+02, 0.000E+00)
CH374	#38	vout1	topbot	(7.098E-15, 1.375E+02, 0.000E+00)
CH375	#38	#21	topbot	(1.936E-14, 3.750E+02, 0.000E+00)
CH376	#66	gnd	topbot	(5.162E-15, 1.000E+02, 0.000E+00)

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CH378       #61       vout2     topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH379       vout1     #61       topbot    (5.162E-15, 1.000E+02, 0.000E+00)
CH380       #61       #21       topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH382       #21       #83       topbot    (2.065E-14, 4.000E+02, 0.000E+00)
CH384       #32       #83       topbot    (6.808E-15, 1.319E+02, 0.000E+00)
CH386       #21       #118      topbot    (5.162E-15, 1.000E+02, 0.000E+00)
CH387       gnd       #143      topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH388       #32       #118      topbot    (4.937E-15, 9.562E+01, 0.000E+00)
CH390       #32       #130      topbot    (4.937E-15, 9.562E+01, 0.000E+00)
CH393       #66       #140      topbot    (9.034E-15, 1.750E+02, 0.000E+00)
CH394       #248      gnd       topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH395       #32       #234      topbot    (1.613E-14, 3.125E+02, 0.000E+00)
CH396       #130      #143      topbot    (6.453E-15, 1.250E+02, 0.000E+00)
CH397       #32       #248      topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH398       #32       #265      topbot    (1.613E-14, 3.125E+02, 0.000E+00)
CH400       vin       #210      topbot    (9.873E-15, 1.912E+02, 0.000E+00)
CH401       #235      vref      topbot    (2.581E-15, 5.000E+01, 0.000E+00)
CH402       vin       #284      topbot    (2.581E-15, 5.000E+01, 0.000E+00)
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.end
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APPENDIX F

DC Operating Points of Component-

Extracted VCO Circuit

***** node voltages

Node	Voltage	Node	Voltage	Node	Voltage
(0)	0.00000e+00	(#104)	9.16196e+00	(#105)	1.21330e+00
(#108)	1.22893e+00	(#109)	1.19767e+00	(#118)	6.99431e+00
(#119)	1.24456e+00	(#120)	1.18204e+00	(#130)	1.58014e+00
(#133)	1.26019e+00	(#134)	1.16641e+00	(#140)	1.15078e+00
(#143)	1.27582e+00	(#2)	7.54278e+00	(#21)	1.00000e+01
(#210)	3.49485e+00	(#234)	3.49484e+00	(#235)	7.23744e+00
(#242)	4.19364e+00	(#248)	3.49484e+00	(#249)	7.69786e+00
(#261)	8.15829e+00	(#265)	3.96070e+00	(#272)	8.61872e+00
(#273)	9.53957e+00	(#284)	9.07915e+00	(#32)	8.37702e-01
(#38)	8.35271e+00	(#45)	3.35272e-01	(#60)	6.70544e-01
(#61)	8.35271e+00	(#66)	8.38180e-01	(#83)	6.15882e+00
(#Z)	6.87582e+00	(#1)	7.54278e+00	(GND)	0.00000e+00
(VIN)	4.00000e+00	(VOUT1)	9.19554e+00	(VOUT2)	9.19554e+00
(VREF)	5.00000e+00	(XR147 .D)	9.59777e+00	(XR148 .D)	9.59777e+00
(XR149 .D)	9.59777e+00	(XR150 .D)	9.59777e+00	(XR383 .D)	9.30936e+00

(XR384 .D	)	9.76979e+00	(XR397 .D	)	8.84893e+00	(XR398 .D	) 8.38850e+00
(XR399 .D	)	7.92808e+00	(XR400 .D	)	7.46765e+00	(XR401 .D	) 3.49485e+00
(XR402 .D	)	3.49485e+00	(XR403 .D	)	4.07717e+00	(XR404 .D	) 4.07717e+00
(XR418 .D	)	3.72777e+00	(XR420 .D	)	3.49484e+00	(XR50 .D	) 9.94481e-01
(XR56 .D	)	7.54362e-01	(XR81 .D	)	1.23675e+00	(XR82 .D	) 1.22112e+00
(XR83 .D	)	1.26801e+00	(XR84 .D	)	1.25238e+00	(XR89 .D	) 1.15860e+00
(XR90 .D	)	1.17423e+00	(XR91 .D	)	1.18986e+00	(XR92 .D	) 1.20549e+00
(XR97 .D	)	5.02908e-01	(XR98 .D	)	1.67636e-01		

***** resistor operating points

name	current	voltage	power	value
R6EXT	4.489e-03	4.579	2.055e-02	1.020e+03
RZ	4.646e-03	.118	5.505e-04	2.550e+01
XR50 .R1	1.563e-04	.156	2.443e-05	1.000e+03
XR50 .R2	1.563e-04	.156	2.443e-05	1.000e+03
XR56 .R1	8.382e-05	.084	7.025e-06	1.000e+03
XR56 .R2	8.382e-05	.084	7.025e-06	1.000e+03
XR81 .R1	1.563e-04	.008	1.221e-06	5.000e+01
XR81 .R2	1.563e-04	.008	1.221e-06	5.000e+01
XR82 .R1	1.563e-04	.008	1.221e-06	5.000e+01
XR82	1.563e-04	.008	1.221e-06	5.000e+01

.R2				
XR83	1.563e-04	.008	1.221e-06	5.000e+01
.R1				
XR83	1.563e-04	.008	1.221e-06	5.000e+01
.R2				
XR84	1.563e-04	.008	1.221e-06	5.000e+01
.R1				
XR84	1.563e-04	.008	1.221e-06	5.000e+01
.R2				
XR89	-1.563e-04	-.008	1.221e-06	5.000e+01
.R1				
XR89	-1.563e-04	-.008	1.221e-06	5.000e+01
.R2				
XR90	-1.563e-04	-.008	1.221e-06	5.000e+01
.R1				
XR90	-1.563e-04	-.008	1.221e-06	5.000e+01
.R2				
XR91	-1.563e-04	-.008	1.221e-06	5.000e+01
.R1				
XR91	-1.563e-04	-.008	1.221e-06	5.000e+01
.R2				
XR92	-1.563e-04	-.008	1.221e-06	5.000e+01
.R1				
XR92	-1.563e-04	-.008	1.221e-06	5.000e+01
.R2				
XR97	8.382e-05	.168	1.405e-05	2.000e+03
.R1				
XR97	8.382e-05	.168	1.405e-05	2.000e+03
.R2				
XR98	8.382e-05	.168	1.405e-05	2.000e+03
.R1				
XR98	8.382e-05	.168	1.405e-05	2.000e+03
.R2				
XR147	4.022e-04	.402	1.618e-04	1.000e+03
.R1				
XR147	4.022e-04	.402	1.618e-04	1.000e+03
.R2				
XR148	-4.022e-04	-.402	1.618e-04	1.000e+03
.R1				
XR148	-4.022e-04	-.402	1.618e-04	1.000e+03
.R2				
XR149	4.022e-04	.402	1.618e-04	1.000e+03
.R1				
XR149	4.022e-04	.402	1.618e-04	1.000e+03
.R2				
XR150	-4.022e-04	-.402	1.618e-04	1.000e+03
.R1				
XR150	-4.022e-04	-.402	1.618e-04	1.000e+03
.R2				
XR383	-4.604e-03	-.230	1.060e-03	5.000e+01
.R1				
XR383	-4.604e-03	-.230	1.060e-03	5.000e+01
.R2				
XR384	-4.604e-03	-.230	1.060e-03	5.000e+01
.R1				

XR384	-4.604e-03	-.230	1.060e-03	5.000e+01
.R2				
XR397	4.604e-03	.230	1.060e-03	5.000e+01
.R1				
XR397	4.604e-03	.230	1.060e-03	5.000e+01
.R2				
XR398	4.604e-03	.230	1.060e-03	5.000e+01
.R1				
XR398	4.604e-03	.230	1.060e-03	5.000e+01
.R2				
XR399	4.604e-03	.230	1.060e-03	5.000e+01
.R1				
XR399	4.604e-03	.230	1.060e-03	5.000e+01
.R2				
XR400	4.604e-03	.230	1.060e-03	5.000e+01
.R1				
XR400	4.604e-03	.230	1.060e-03	5.000e+01
.R2				
XR401	-4.314e-08	.000	9.305e-14	5.000e+01
.R1				
XR401	-4.313e-08	.000	9.302e-14	5.000e+01
.R2				
XR402	4.313e-08	.000	9.302e-14	5.000e+01
.R1				
XR402	4.314e-08	.000	9.305e-14	5.000e+01
.R2				
XR403	-2.329e-03	-.116	2.713e-04	5.000e+01
.R1				
XR403	-2.329e-03	-.116	2.713e-04	5.000e+01
.R2				
XR404	2.329e-03	.116	2.713e-04	5.000e+01
.R1				
XR404	2.329e-03	.116	2.713e-04	5.000e+01
.R2				
XR418	-4.659e-03	-.233	1.085e-03	5.000e+01
.R1				
XR418	-4.659e-03	-.233	1.085e-03	5.000e+01
.R2				
XR420	-8.630e-08	.000	3.724e-13	5.000e+01
.R1				
XR420	-8.630e-08	.000	3.724e-13	5.000e+01
.R2				

***** capacitor operating points

name	current	voltage	power	value
CD1	0.000e+00	7.543	0.000e+00	1.673e-13
CD2	0.000e+00	7.543	0.000e+00	7.903e-14
CD3	0.000e+00	.000	0.000e+00	1.621e-12
CD8	0.000e+00	9.196	0.000e+00	3.223e-13
CD9	0.000e+00	9.196	0.000e+00	3.278e-13

CD13	0.000e+00	10.000	0.000e+00	1.016e-12
CD17	0.000e+00	.838	0.000e+00	3.375e-13
CD19	0.000e+00	8.353	0.000e+00	7.624e-14
CD25	0.000e+00	.335	0.000e+00	3.304e-15
CD38	0.000e+00	.671	0.000e+00	1.564e-14
CD39	0.000e+00	8.353	0.000e+00	1.123e-13
CD40	0.000e+00	.838	0.000e+00	7.070e-14
CD53	0.000e+00	6.159	0.000e+00	1.105e-13
CD71	0.000e+00	9.162	0.000e+00	1.085e-13
CD72	0.000e+00	1.213	0.000e+00	1.229e-14
CD75	0.000e+00	1.229	0.000e+00	3.304e-15
CD76	0.000e+00	1.198	0.000e+00	3.304e-15
CD84	0.000e+00	6.994	0.000e+00	1.604e-13
CD85	0.000e+00	1.245	0.000e+00	1.745e-14
CD86	0.000e+00	1.182	0.000e+00	1.745e-14
CD94	0.000e+00	1.580	0.000e+00	6.334e-14
CD97	0.000e+00	1.260	0.000e+00	3.304e-15
CD98	0.000e+00	1.166	0.000e+00	3.304e-15
CD104	0.000e+00	1.151	0.000e+00	1.974e-14
CD107	0.000e+00	1.276	0.000e+00	1.338e-13
CD151	0.000e+00	4.000	0.000e+00	1.036e-13
CD152	0.000e+00	3.495	0.000e+00	1.106e-13
CD173	0.000e+00	3.495	0.000e+00	3.220e-14
CD174	0.000e+00	7.237	0.000e+00	6.682e-14
CD175	0.000e+00	4.194	0.000e+00	9.442e-14
CD176	0.000e+00	5.000	0.000e+00	9.025e-14
CD181	0.000e+00	3.495	0.000e+00	1.234e-13
CD182	0.000e+00	7.698	0.000e+00	3.304e-15
CD194	0.000e+00	8.158	0.000e+00	1.745e-14
CD195	0.000e+00	3.961	0.000e+00	3.220e-14
CD202	0.000e+00	8.619	0.000e+00	3.304e-15
CD203	0.000e+00	9.540	0.000e+00	3.304e-15
CD214	0.000e+00	9.079	0.000e+00	1.329e-14
CF303	0.000e+00	7.543	0.000e+00	3.424e-13
CF304	0.000e+00	7.543	0.000e+00	3.857e-13
CF305	0.000e+00	.000	0.000e+00	9.152e-12
CF310	0.000e+00	9.196	0.000e+00	4.046e-13
CF311	0.000e+00	9.196	0.000e+00	4.134e-13
CF315	0.000e+00	10.000	0.000e+00	5.770e-12
CF319	0.000e+00	.838	0.000e+00	7.884e-13
CF321	0.000e+00	8.353	0.000e+00	1.955e-13
CF322	0.000e+00	8.353	0.000e+00	7.276e-14
CF323	0.000e+00	.838	0.000e+00	1.517e-13
CF326	0.000e+00	6.159	0.000e+00	4.348e-13
CF328	0.000e+00	1.580	0.000e+00	4.266e-13
CF336	0.000e+00	4.000	0.000e+00	5.153e-13
CF340	0.000e+00	5.000	0.000e+00	4.545e-13
CF341	0.000e+00	3.495	0.000e+00	1.769e-14
CH353	0.000e+00	.000	0.000e+00	6.965e-15
CH354	0.000e+00	7.543	0.000e+00	7.989e-15
CH355	0.000e+00	1.653	0.000e+00	7.744e-15
CH356	0.000e+00	1.653	0.000e+00	2.581e-15
CH357	0.000e+00	-1.653	0.000e+00	2.581e-15
CH358	0.000e+00	9.196	0.000e+00	7.757e-15
CH359	0.000e+00	-1.653	0.000e+00	2.581e-15

CH360	0.000e+00	-9.196	0.000e+00	2.581e-15
CH362	0.000e+00	-2.457	0.000e+00	5.162e-15
CH363	0.000e+00	-10.000	0.000e+00	6.742e-14
CH364	0.000e+00	.000	0.000e+00	2.581e-15
CH365	0.000e+00	-6.705	0.000e+00	2.581e-15
CH366	0.000e+00	.804	0.000e+00	1.291e-14
CH367	0.000e+00	.838	0.000e+00	4.459e-14
CH368	0.000e+00	-.804	0.000e+00	2.065e-14
CH369	0.000e+00	-8.358	0.000e+00	2.581e-15
CH370	0.000e+00	-8.358	0.000e+00	2.581e-15
CH372	0.000e+00	-.843	0.000e+00	2.581e-15
CH373	0.000e+00	9.162	0.000e+00	5.162e-15
CH374	0.000e+00	-.843	0.000e+00	7.098e-15
CH375	0.000e+00	-1.647	0.000e+00	1.936e-14
CH376	0.000e+00	.838	0.000e+00	5.162e-15
CH378	0.000e+00	-.843	0.000e+00	2.581e-15
CH379	0.000e+00	.843	0.000e+00	5.162e-15
CH380	0.000e+00	-1.647	0.000e+00	2.581e-15
CH382	0.000e+00	3.841	0.000e+00	2.065e-14
CH384	0.000e+00	-5.321	0.000e+00	6.808e-15
CH386	0.000e+00	3.006	0.000e+00	5.162e-15
CH387	0.000e+00	-1.276	0.000e+00	2.581e-15
CH388	0.000e+00	-6.157	0.000e+00	4.937e-15
CH390	0.000e+00	-.742	0.000e+00	4.937e-15
CH393	0.000e+00	-.313	0.000e+00	9.034e-15
CH394	0.000e+00	3.495	0.000e+00	2.581e-15
CH395	0.000e+00	-2.657	0.000e+00	1.613e-14
CH396	0.000e+00	.304	0.000e+00	6.453e-15
CH397	0.000e+00	-2.657	0.000e+00	2.581e-15
CH398	0.000e+00	-3.123	0.000e+00	1.613e-14
CH400	0.000e+00	.505	0.000e+00	9.873e-15
CH401	0.000e+00	2.237	0.000e+00	2.581e-15
CH402	0.000e+00	-5.079	0.000e+00	2.581e-15
XC130	0.000e+00	.000	0.000e+00	1.000e-12

.C1

***** independent current source operating points

name	current	voltage	power
ISTART	0.000e+00	.000	0.000e+00

***** independent voltage source operating points

name	current	voltage	power
VSP	-3.398e-02	10.000	-3.398e-01
VGND	3.404e-02	.000	0.000e+00
VREF	-5.441e-05	5.000	-2.720e-04

VIN	-7.069e-10	4.000	-2.828e-09
VZ	4.646e-03	5.600	2.602e-02

***** diode operating points

name	id	vd	power
XR50	-8.849e-12	-8.849	7.831e-11
.DR#1			
XR50	-9.006e-12	-9.006	8.110e-11
.DR#2			
XR50	-9.162e-12	-9.162	8.394e-11
.DR#3			
XR56	-9.162e-12	-9.162	8.394e-11
.DR#1			
XR56	-9.246e-12	-9.246	8.548e-11
.DR#2			
XR56	-9.330e-12	-9.329	8.704e-11
.DR#3			
XR81	-8.755e-12	-8.755	7.666e-11
.DR#1			
XR81	-8.763e-12	-8.763	7.679e-11
.DR#2			
XR81	-8.771e-12	-8.771	7.693e-11
.DR#3			
XR82	-8.771e-12	-8.771	7.693e-11
.DR#1			
XR82	-8.779e-12	-8.779	7.707e-11
.DR#2			
XR82	-8.787e-12	-8.787	7.721e-11
.DR#3			
XR83	-8.724e-12	-8.724	7.611e-11
.DR#1			
XR83	-8.732e-12	-8.732	7.625e-11
.DR#2			
XR83	-8.740e-12	-8.740	7.638e-11
.DR#3			
XR84	-8.740e-12	-8.740	7.638e-11
.DR#1			
XR84	-8.748e-12	-8.748	7.652e-11
.DR#2			
XR84	-8.755e-12	-8.755	7.666e-11
.DR#3			
XR89	-8.849e-12	-8.849	7.831e-11
.DR#1			
XR89	-8.841e-12	-8.841	7.817e-11
.DR#2			
XR89	-8.834e-12	-8.834	7.803e-11
.DR#3			
XR90	-8.834e-12	-8.834	7.803e-11
.DR#1			
XR90	-8.826e-12	-8.826	7.789e-11

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.DR#2
 XR90      -8.818e-12   -8.818  7.776e-11
.DR#3
 XR91      -8.818e-12   -8.818  7.776e-11
.DR#1
 XR91      -8.810e-12   -8.810  7.762e-11
.DR#2
 XR91      -8.802e-12   -8.802  7.748e-11
.DR#3
 XR92      -8.802e-12   -8.802  7.748e-11
.DR#1
 XR92      -8.795e-12   -8.795  7.734e-11
.DR#2
 XR92      -8.787e-12   -8.787  7.721e-11
.DR#3
 XR97      -9.330e-12   -9.329  8.704e-11
.DR#1
 XR97      -9.497e-12   -9.497  9.020e-11
.DR#2
 XR97      -9.665e-12   -9.665  9.341e-11
.DR#3
 XR98      -9.665e-12   -9.665  9.341e-11
.DR#1
 XR98      -9.832e-12   -9.832  9.668e-11
.DR#2
 XR98      -1.000e-11  -10.000  1.000e-10
.DR#3
 XR147     -8.904e-28     .000  7.908e-43
.DR#1
 XR147     -4.023e-13    -.402  1.618e-13
.DR#2
 XR147     -8.045e-13    -.804  6.472e-13
.DR#3
 XR148     -8.045e-13    -.804  6.472e-13
.DR#1
 XR148     -4.023e-13    -.402  1.618e-13
.DR#2
 XR148     -8.904e-28     .000  7.908e-43
.DR#3
 XR149     -8.904e-28     .000  7.908e-43
.DR#1
 XR149     -4.023e-13    -.402  1.618e-13
.DR#2
 XR149     -8.045e-13    -.804  6.472e-13
.DR#3
 XR150     -8.045e-13    -.804  6.472e-13
.DR#1
 XR150     -4.023e-13    -.402  1.618e-13
.DR#2
 XR150     -8.904e-28     .000  7.908e-43
.DR#3
 XR383     -9.209e-13    -.921  8.480e-13
.DR#1
 XR383     -6.907e-13    -.691  4.770e-13
.DR#2
```

```
 XR383     -4.605e-13     -.460  2.120e-13
.DR#3
 XR384     -4.605e-13     -.460  2.120e-13
.DR#1
 XR384     -2.303e-13     -.230  5.301e-14
.DR#2
 XR384     -8.904e-28      .000  7.908e-43
.DR#3
 XR397     -9.209e-13     -.921  8.480e-13
.DR#1
 XR397     -1.151e-12    -1.151  1.325e-12
.DR#2
 XR397     -1.381e-12    -1.381  1.908e-12
.DR#3
 XR398     -1.381e-12    -1.381  1.908e-12
.DR#1
 XR398     -1.612e-12    -1.611  2.597e-12
.DR#2
 XR398     -1.842e-12    -1.842  3.392e-12
.DR#3
 XR399     -1.842e-12    -1.842  3.392e-12
.DR#1
 XR399     -2.072e-12    -2.072  4.293e-12
.DR#2
 XR399     -2.302e-12    -2.302  5.300e-12
.DR#3
 XR400     -2.302e-12    -2.302  5.300e-12
.DR#1
 XR400     -2.532e-12    -2.532  6.413e-12
.DR#2
 XR400     -2.763e-12    -2.763  7.632e-12
.DR#3
 XR401     -6.505e-12    -6.505  4.232e-11
.DR#1
 XR401     -6.505e-12    -6.505  4.232e-11
.DR#2
 XR401     -6.505e-12    -6.505  4.232e-11
.DR#3
 XR402     -6.505e-12    -6.505  4.232e-11
.DR#1
 XR402     -6.505e-12    -6.505  4.232e-11
.DR#2
 XR402     -6.505e-12    -6.505  4.232e-11
.DR#3
 XR403     -6.039e-12    -6.039  3.647e-11
.DR#1
 XR403     -5.923e-12    -5.923  3.508e-11
.DR#2
 XR403     -5.806e-12    -5.806  3.371e-11
.DR#3
 XR404     -5.806e-12    -5.806  3.371e-11
.DR#1
 XR404     -5.923e-12    -5.923  3.508e-11
.DR#2
 XR404     -6.039e-12    -6.039  3.647e-11
```

```
.DR#3
 XR418     -6.505e-12    -6.505   4.232e-11
.DR#1
 XR418     -6.272e-12    -6.272   3.934e-11
.DR#2
 XR418     -6.039e-12    -6.039   3.647e-11
.DR#3
 XR420     -6.505e-12    -6.505   4.232e-11
.DR#1
 XR420     -6.505e-12    -6.505   4.232e-11
.DR#2
 XR420     -6.505e-12    -6.505   4.232e-11
.DR#3
 XC130     -7.543e-12    -7.543   5.690e-11
.DR#1
 XC130     -7.543e-12    -7.543   5.690e-11
.DR#2
```

```
*****  Four-terminal BJT operating points

name             ib            ic            vbe           vbc           vce          beta        power
                 isub          vsc           rci-mod

B3         -1.409e-04    -4.147e-03      -.838          .000         -.838          29.4     3.593e-03
            6.923e-13          .838     1.29545
B4         -1.349e-04    -4.713e-03      -.838         2.168        -3.006          34.9     1.428e-02
            2.840e-12         3.006     1.41553
B15         6.624e-05     4.423e-03       .835        -2.168         3.003          66.8     1.334e-02
           -9.074e-12        -9.162     1.23257
B16         2.771e-06     4.134e-04       .742        -8.420         9.162         149.2     3.790e-03
           -9.992e-12       -10.000     1.01796
B17         7.129e-05     4.486e-03       .838         -.742         1.580          62.9     7.148e-03
           -1.491e-12        -1.580     1.23669
B18         7.248e-05     4.490e-03       .838         -.438         1.276          61.9     5.789e-03
           -1.186e-12        -1.276     1.23695
B116        5.175e-05     4.097e-03       .804          .000          .804          79.2     3.337e-03
           -9.959e-12       -10.000     1.09576
B117        5.175e-05     4.097e-03       .804          .000          .804          79.2     3.337e-03
           -9.959e-12       -10.000     1.09576
B119        6.879e-05     4.932e-03       .838        -6.705         7.543          71.7     3.726e-02
           -7.444e-12        -7.543     1.26651
B120        6.851e-05     4.982e-03       .838        -7.515         8.353          72.7     4.167e-02
           -8.253e-12        -8.353     1.26989
B121        6.851e-05     4.982e-03       .838        -7.515         8.353          72.7     4.167e-02
           -8.253e-12        -8.353     1.26989
B122        6.879e-05     4.932e-03       .838        -6.705         7.543          71.7     3.726e-02
           -7.444e-12        -7.543     1.26651
B123        6.145e-05     4.871e-03       .810         -.843         1.653          79.3     8.100e-03
           -9.147e-12        -9.196     1.11595
B124        8.220e-05     4.961e-03       .843         -.804         1.647          60.4     8.241e-03
           -9.901e-12       -10.000     1.26847
B125        8.220e-05     4.961e-03       .843         -.804         1.647          60.4     8.241e-03
```

	-9.901e-12	-10.000	1.26847				
B126	6.145e-05	4.871e-03	.810	-.843	1.653	79.3	8.100e-03
	-9.147e-12	-9.196	1.11599				
B335	3.535e-10	4.278e-08	.505	-3.543	4.048	121.0	1.734e-07
	-7.543e-12	-7.543	1.00000				
B336	3.535e-10	4.278e-08	.505	-3.543	4.048	121.0	1.734e-07
	-7.543e-12	-7.543	1.00000				
B337	2.720e-05	2.302e-03	.806	-2.237	3.044	84.6	7.029e-03
	-7.191e-12	-7.237	1.10891				
B338	2.720e-05	2.302e-03	.806	-2.237	3.044	84.6	7.029e-03
	-7.191e-12	-7.237	1.10891				
B339	7.031e-05	4.659e-03	.838	-2.657	3.495	66.3	1.634e-02
	-3.402e-12	-3.495	1.24806				

VITA

Douglas A. Williams was born on September 9, 1958, to E. Joan and (the late) Alan S. Williams in Wilkes-Barre, Pennsylvania. Douglas, a graduate of the E. L. Meyers High School and the Wilkes-Barre Area Vocational Technical School, earned the degree of Associate in Electrical Engineering Technology with High Honors in May 1978 from the Pennsylvania State University. He also earned the degree of Bachelor of Science in Physics from Albright College in May 1985. Douglas expects to graduate from Lehigh University in June 1990 with the degree of Master of Science in Electrical Engineering.

Douglas is a Member of Technical Staff at AT&T Bell Laboratories in Reading, Pennsylvania, where he has been employed since June 1978. He resides in Reading, Pennsylvania, with his wife Donna, and their daughters Deanna and Danielle.