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Development of a high speed fully differential emitter-coupled logic family

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DEVELOPMENT OF A HIGH SPEED FULLY DIFFERENTIAL EMITTER-COUPLED LOGIC FAMILY

by

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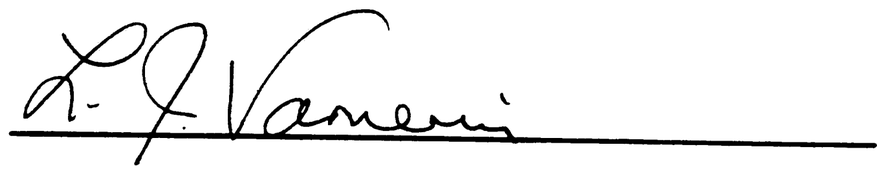

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Abstract

Analytic methods have been used to studied the DC characteristics of fully differential Emitter-Coupled Logic (ECL) gates. Differential operation was chosen because of its inherent immunity to noise. The analysis resulted in equations that predict the DC noise margin of differential gates based on the magnitude of the logic voltage swing and maximum logic swing to avoid saturation. The results of the analysis were confirmed by computer simulation for a logic swing of 340 mV, which yielded a DC noise margin of approximately 115 mV.

A family of ECL gates was then developed. The gates are fully differential and have 3 levels of logic. The family provides 19 different functions with a set of 53 gates. All 19 functions are realized in gates that have a maximum operating frequency of 50 MHz over an ambient temperature range of 0 to 80 degrees Celsius and over all process corners. A subset of the functions were designed in gates that operate at 100 MHz under the same conditions. Computer simulations showed the best case power delay product of a 2-input AND gate to be 1.6 pJ.

All of the gates have been laid out on a high performance, junction isolated, complementary Bipolar process known as CBIC-U. The simulations were performed on files that included the parasitic layout capacitances. The logic gates were developed in conjunction with analog cells for use in a high-performance data separator for hard disk drives. A computer analysis of a Coincidence Phase Detector shows that the logic gates can be used in the most critical circuits when architectural modifications are made.

1.0 INTRODUCTION

Circuits used in Hard Disk Drive electronics and other leading edge applications need to be fast, have analog and digital functions on the same die and need to work in a noisy environment. A further constraint is power. The industry trend is to pack more functions into the same package; therefore, each function needs to consume as little power as possible.

The speed requirements for the hard disk application, 96 MHz, eliminated CMOS as a potential process. A bipolar process provides the speed and also allows the integration of analog and digital cells. High speed gates can be achieved with a bipolar process because Emitter-Coupled logic (ECL) is one of the fastest forms of logic.

The challenge of a noisy environment is best met by using the logic in a fully differential manner [1]. Single-ended emitter-coupled logic has one side of the emitter-coupled pair tied to a reference voltage. Differential logic does not compare the input signal to a reference voltage; instead, both sides of the emitter-coupled pair are differentially driven by the output of the preceding gate. Differential signals are inherently more robust than a single-ended approach because noise

is perceived by the circuit as a common-mode signal and is rejected.

The area required for the differential gates and routing is approximately 20% greater than a single-ended system [1], but immunity to noise and high speed are the primary objective and the price must be paid.

The power-delay product of a differential ECL gate is smaller than that of an equivalent single-ended gate because the voltage swing is smaller. The differential gate requires less power and time to charge and discharge the parasitic capacitances. The power needed by a gate could be further reduced by using Current Mode Logic (CML) [12]. A CML gate is just an ECL gate without the emitter-followers. However, CML saturates the transistors during part of the logic swing. Since the operation of the Bipolar transistor in the saturation region on the target process is not well characterized and since ECL does not saturate any transistors, ECL was chosen for the application in spite of the power saving offered by CML.

In this thesis, the fundamental equations governing the DC characteristics of differential ECL gates will be discussed. The noise margin will be calculated with the

equations and verified through simulations. The logic family will be described and its switching characteristics discussed. Some applications circuits in the hard disk area will then be illustrated. Even though the logic family has not been fabricated, the target process is a High-Performance, Complementary Bipolar process known as CBIC-U, which is manufactured by AT&T.

2.0 BASIC DESIGN ANALYSIS

The equations that describe the BJT will be used to investigate the DC characteristics of the gates. The transient characteristics are studied through computer-aided simulations. The DC properties of interest are noise margin, maximum voltage swing, generating logic levels, series gating and voltage drops in the supply lines due to line resistance.

2.1 NOISE MARGIN

Noise margin is the first property to be investigated. The object of the design is to keep the voltage swing across the load resistors as small as possible. The smaller the swing, the faster the parasitic capacitors are charged and discharged. Therefore, the swing should be small while maintaining a healthy noise margin.

Some commercial single-ended ECL families guarantee worse case noise margins of 115 mV from -30 to 85 degrees Celsius [2]. This application requires a high degree of noise immunity. The differential nature should inherently provide more noise immunity than a single-ended design. All signals will consist of 2 wires; the signal and its complement. It is assumed that all signal pairs run side by side and are therefore in the same environment. When noise is present, it will be coupled equally into both signals and will be rejected by the emitter-coupled pair as a common-mode signal. Therefore, because of the differential design, noise is seen by a gate as a common-mode signal and is suppressed.

The effects of noise are layout dependent. Simulating noise is difficult. For this logic family, it is assumed that the DC noise margin should match what has been done previously in single-ended logic and that the differential nature will make it superior to single-ended logic. Empirical data would be required to prove or disprove the above premise. Based on the above, a noise margin of 115 mV was made the design objective.

A general description of noise margin will be given, then the equations of a simple emitter-coupled pair will be developed for analysis.

2.1.1 GENERAL DEFINITION

The definition of noise margin, for restorative logic, can be found in most books on digital design [3] [4]. The equations describing noise margin are:

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Where:

NM_H noise margin of the high logic state.

NM_L noise margin of the low logic state.

V_{OH} highest voltage level out of the gate.

V_{OL} lowest voltage level out of the gate.

V_{IH} high level input where the absolute value of the gain is 1.

V_{IL} low level input where the absolute value of the gain is 1.

The definitions of V_{OH}, V_{OL}, V_{IH} and V_{IL} are best understood by referring to Figures 1, 2 and 3.

Figure 1 displays the transfer characteristic of an inverting gate. V_{OH} is the maximum high and V_{OL} is the minimum low voltage output levels. V_{IL} and V_{IH} are the input voltages at which the absolute value of the gain

of the gate is unity. The gain of a gate is the derivative of its transfer function and is written as:

$$G = \frac{d(V_{OUT})}{d(V_{IN})}$$

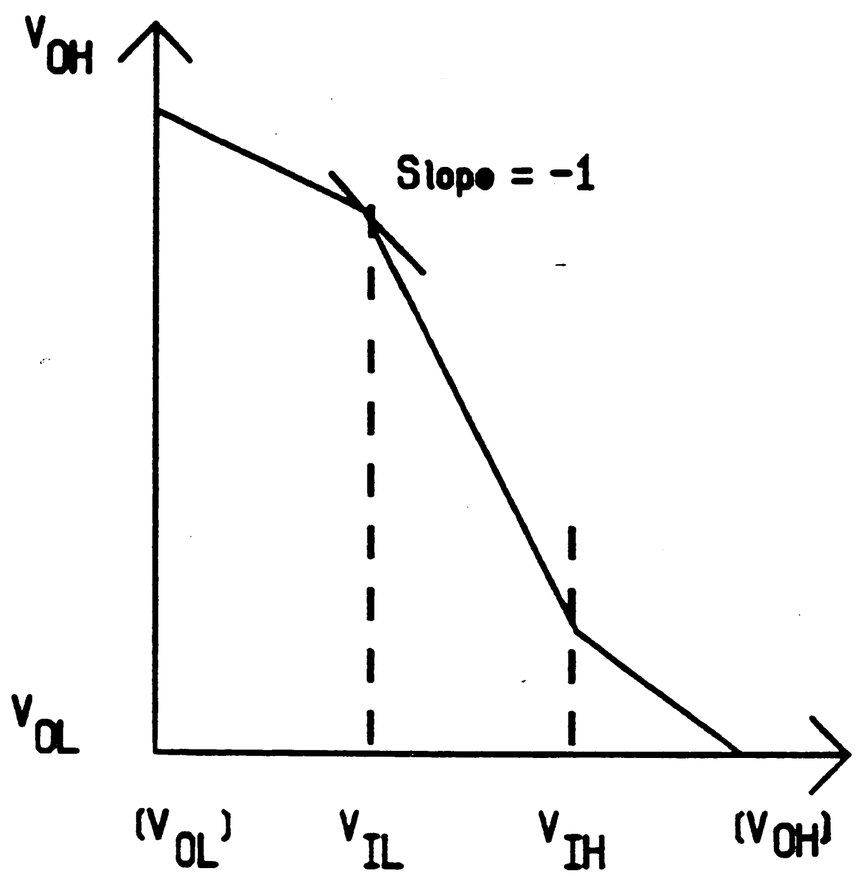
The unity gain points can be seen directly on the transfer function or a plot of the derivative can be made to determine V_{IL} and V_{IH}.

Any input voltage less than V_{IL} is considered a low logic level. An input voltage greater than V_{IH} is interpreted as a high logic level. If the input voltage is greater than V_{IL} and less than V_{IH} the output of the gate is in an indeterminate state; it is neither high nor low. A summary of the input ranges follows:

Input Voltage Level	Logic Level	Output Voltage Level
V_{OL} <= V_{IN} <= V_{IL} V_{IH} <= V_{IN} <= V_{OH}	Low high	>= V_{IH} <= V_{IL}

Voltage Level Summary

Table 1

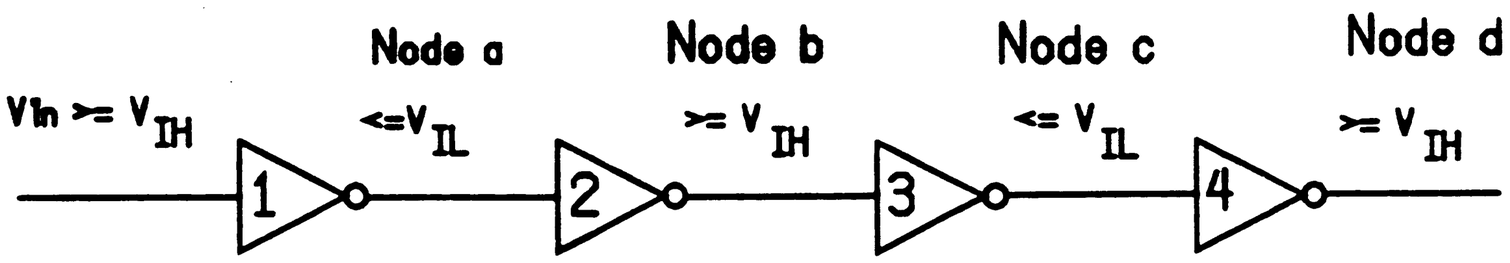


Inverting Transfer Characteristic

Figure 1

The noise margin is defined as the difference between low voltage levels and high voltage levels. The V_{IN} axis of Figure 1 shows that the input voltage can vary between V_{OL} and V_{IL} and the output of the gate will be high enough to be interpreted as a logic high by the subsequent gate.

A string of inverting gates is shown in Figure 2. If the input voltage, V_{IN}, is greater than or equal to V_{IH}, the output voltage of gate 1 is guaranteed to be equal to or less than V_{IL}. Therefore, the input to gate 2 is guaranteed to see a low voltage which will cause node b to be at a guaranteed high voltage etc.



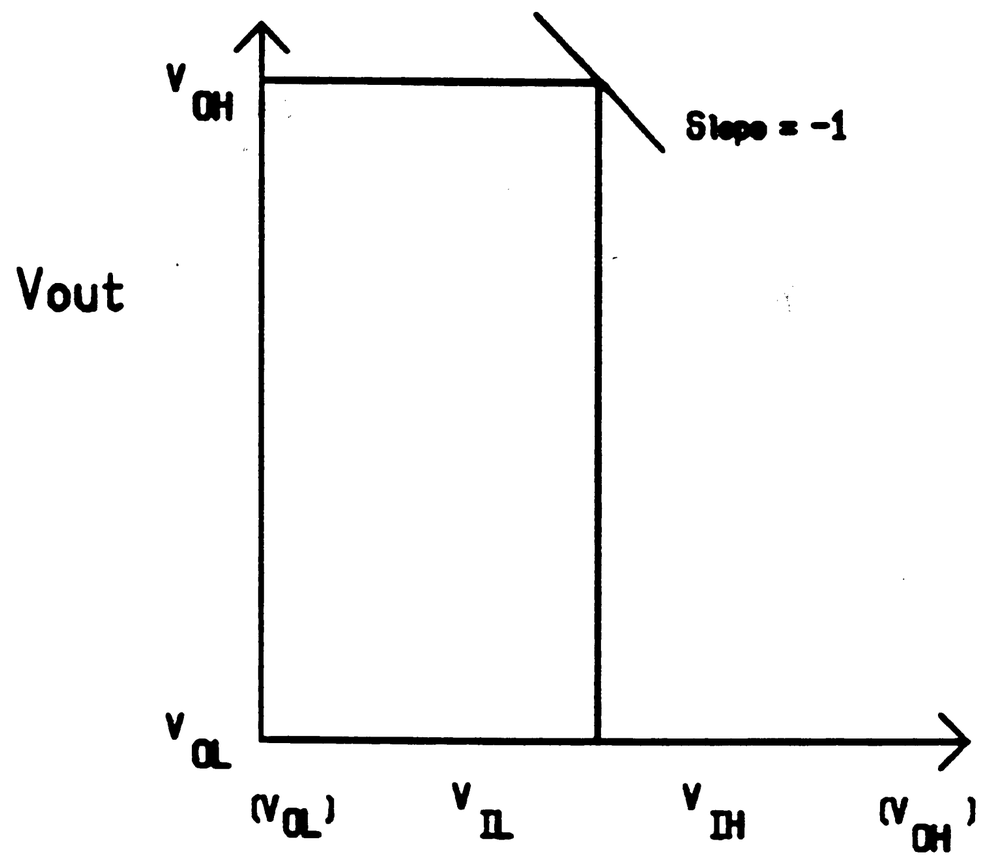
Inverting Gates

Figure 2

If an AC or DC noise source were attached to node a, its voltage level could be forced anywhere between V_{OL} and V_{IL} without affecting the gate 2 output level. Furthermore, none of the gates following gate 2 would be affected. The noise margin quantifies the boundary in which a voltage can vary without causing a logic error.

The transfer characteristic of Figure 3 represents an ideal gate. Note that the slope of the line in the

transition region is infinite, which means the gain of the gate is infinite. The noise margins are as large as possible because the transition region approaches zero. The slope of the line between V_{OL}, V_{IL} and V_{IH}, V_{OH} is zero.



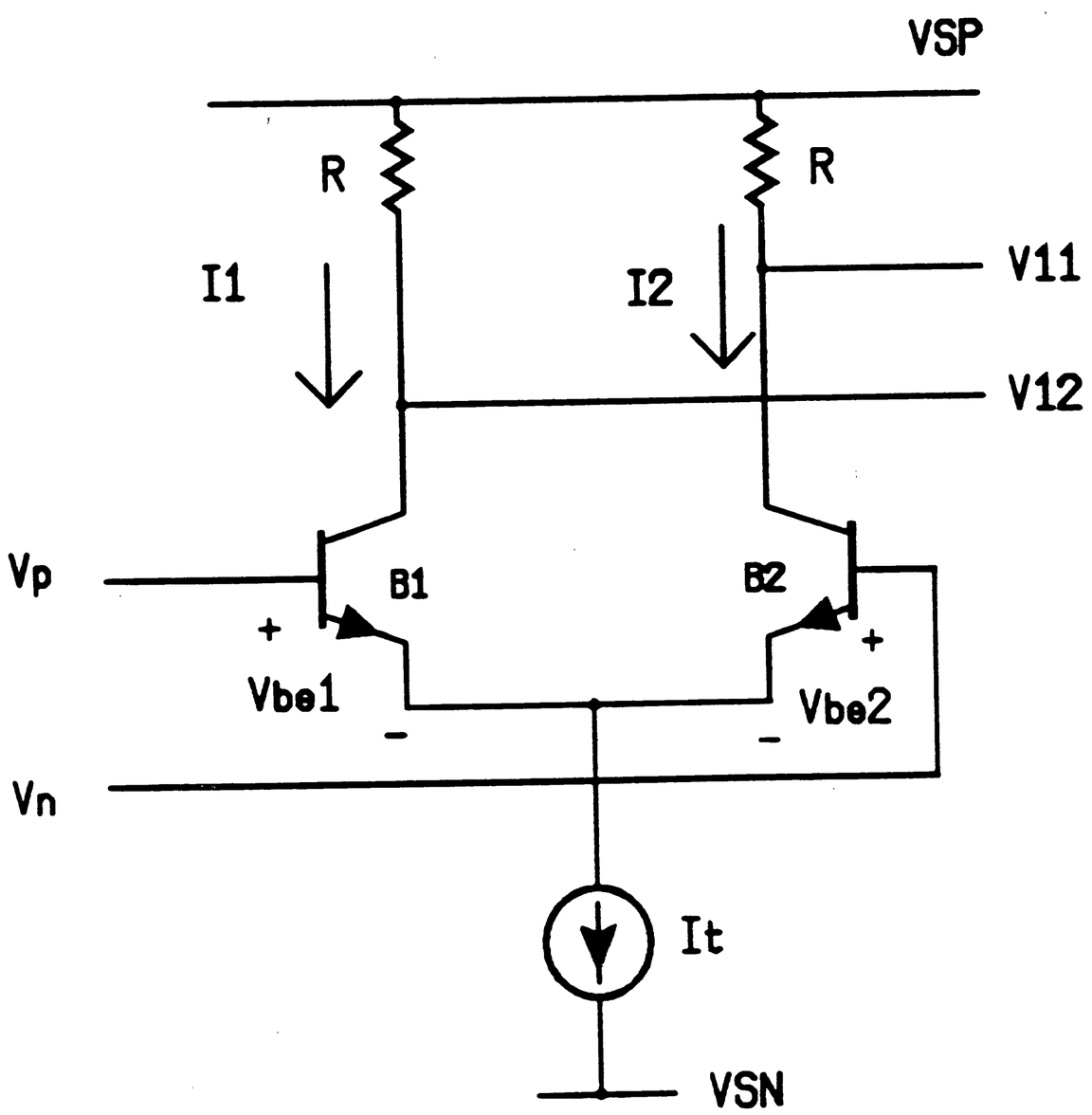
Ideal Inverting
Transfer Characteristic

Figure 3

2.1.2 APPLICATION TO FULLY DIFFERENTIAL ECL

It is important to study the equations of the differential pair to comprehend its first order behavior. The equations are used to predict the noise

margin. A complete DC analysis of single-ended CML has been done [5]. The analysis of differential ECL is similar with minor adjustments to account for the emitter-followers and the differential operation. The equations used are those that describe the emitter-coupled pair shown in Figure 4.



Emitter-Coupled Pair
Figure 4

The following equations will be used for the analysis:

$$I_t = I_1 + I_2 \tag{1}$$

$$V_{in} = V_p - V_n = V_{be1} - V_{be2} \tag{2}$$

$$V_{sm} = I_t R \tag{3}$$

$$V_{out} = V_{11} - V_{12} = (I_1 - I_2)R \tag{4}$$

The value V_{sm} is a constant. It represents the maximum voltage drop that can occur across the resistor R. It will be shown in the following equations that the output voltage is some fractional quantity of V_{sm} Ranging from 0 to 1.

The equation for the current through a transistor is:

$$I_1 := I_s \cdot \left[e^{\left[\frac{V_{be1}}{V_t} \right]} - 1 \right]$$

Where I_S is the saturation current and V_t is kT/q. The voltage V_{BE1} is the base-emitter voltage of an active device and is in the range of 0.7 V. Therefore, the following is true:

$$e^{\left[\frac{V_{be1}}{V_t}\right]} > 1$$

The equation for I_1 can be simplified to:

$$I_1 := I_s \cdot e^{\left[\frac{V_{be1}}{V_t}\right]} \qquad (5a)$$

Likewise, the equation for I_2 is:

$$I_2 := I_s \cdot e^{\left[\frac{V_{be2}}{V_t}\right]} \qquad (5b)$$

Using equations 5a and 5b and substituting in equation 2 yields the ratio of I_1 and I_2 and the reciprocal:

$$\frac{I_1}{I_2} := e^{\left[\frac{V_{in}}{V_t}\right]} \tag{6a}$$

$$\frac{I_2}{I_1} := e^{-\left[\left[\frac{V_{in}}{V_t}\right]\right]} \tag{6b}$$

Performing algebra on equations 6a, 6b and 1 yields the following relationship between I_t and I_1 and I_2:

$$\frac{I_t}{I_1} := e^{-\left[\frac{V_{in}}{V_t}\right]} + 1 \tag{7a}$$

$$\frac{I_t}{I_2} := e^{\left[\frac{V_{in}}{V_t}\right]} + 1 \qquad (7b)$$

The equations describing the voltages V_{11} and V_{12} are:

$$V_{11} = V_{SP} - I_2 R \qquad (8a)$$

$$V_{12} = V_{SP} - I_1 R \qquad (8b)$$

Equations 3 and 8 yield equations that relate the output voltage to the voltage swing across the load resistor and the current. They are as follows:

$$V_{11} := V_{sp} - \left[\frac{I_2}{I_t}\right] \cdot V_{sm} \qquad (9a)$$

$$V_{12} := V_{sp} - \left[\frac{I_1}{I_t}\right] \cdot V_{sm} \qquad (9b)$$

The equations 9a and 9b can be combined with 7a and 7b to get the final form of the voltages across the load

resistors. It is expressed in terms of V_{SM}, V_{IN} and V_t.

$$V_{11} := V_{sp} - V_{sm} \cdot \left[\frac{1}{e^{-\left[\frac{V_{in}}{V_t}\right]} + 1} \right] \qquad (10a)$$

$$V_{12} := V_{sp} - V_{sm} \cdot \left[\frac{1}{e^{\left[\frac{V_{in}}{V_t}\right]} + 1} \right] \qquad (10b)$$

An alternate form of V_{12} is given below. It simply states that V_{12} is the inverse of V_{11}.

$$V_{12} := V_{sp} - V_{sm} + V_{sm} \cdot \left[\frac{1}{e^{\left[\frac{V_{in}}{V_t}\right]} + 1} \right] \qquad (11)$$

A useful form of V_{OUT} can be derived by substituting equations 10a and 11 in equation 4. The resulting equation, shown below, represents the differential output voltage. It should not be used in the single-ended case as in [5].

$$V_{out} := V_{sm} - 2 \cdot V_{sm} \cdot \left[\frac{1}{\left[e^{\left[\frac{V_{in}}{V_t} \right]} + 1 \right]} \right] \qquad (12)$$

The range for V_{IN} in equation 12 is:

$$-V_{sm} <= V_{in} <= V_{sm} \qquad (13)$$

which represent the full differential input voltage. The input voltage for single-ended logic ranges from 0 to V_{sm}. Transfer characteristics for both cases are shown in Section 2.1.3.

The differential gain can be found in two ways. The most obvious way would be to differentiate equation 12 with respect to V_{IN} and set it equal to 1. It will be noted that the differential of equation 12 is simply double the differentiated result of equation 10a. It is easy to see that the gain of the differential gate is twice that of the single-ended one.

The second method for finding V_{IH} and V_{IL} is to double the voltage swing, V_{SM}, of the single-ended equations. The results of differentiating equations 10a and 10b are as follows:

$$G_{11} := \frac{V_{sm}}{V_t} \cdot \left[\frac{e^{\left[\frac{V_{in}}{V_t}\right]}}{\left[\left[e^{\left[\frac{V_{in}}{V_t}\right]} + 1\right]\right]^2} \right] \qquad (14a)$$

$$G_{12} := \frac{-V_{sm}}{V_t} \cdot \left[\frac{e^{\left[\frac{V_{in}}{V_t}\right]}}{\left[\left[e^{\left[\frac{V_{in}}{V_t}\right]} + 1\right]\right]^2} \right] \qquad (14b)$$

The definitions of V_{IL} and V_{IH} are the input voltages that cause the gain to go to unity. The equations 14a and 14b have been previously derived for a single-ended system [5]. As stated, they can be modified to find V_{OH} and V_{OL} for a differential gate by multiplying V_{SM} by 2 and equating 14a to 1 and 14b to -1 and solving for V_{IN}. When compared to a single-ended family, the differential gates have twice as much gain and noise margin for a given V_{SM}.

For $G_{11} = 1$:

$$V_{in} := V_t \cdot \ln\left[\frac{2 \cdot V_{sm}}{V_t} - 2\right] \qquad (15a)$$

For $G_{12} = -1$:

$$V_{in} := -V_t \cdot \ln\left[\frac{2 \cdot V_{sm}}{V_t} - 2\right] \qquad (15b)$$

The operation of the emitter-coupled pair is symmetrical. The value of V_{IN} from equation 15a represents V_{IH} and the negative is V_{IL}. The same applies to equation 15b.

The equations 12, 15a and 15b are the modifications to the single-ended case required to calculate the noise margin. Equation 12 gives the value of V_{OL} and V_{OH} when V_{IN} is equal to $-V_{SM}$ and $+V_{SM}$ respectively. Equation 15a provides V_{IH} and V_{IL}. Tables of noise margins for a given V_{SM} follow.

The values in Tables 2a, 2b and 2c are for V_t = 20.1 mV, 25 mV and 33.9 mV respectively, which corresponds to -40, 16.9 and 120 degrees Celsius. All numbers are expressed in millivolts.

V_{SM}	V_{OH}	V_{OL}	V_{IH}	V_{IL}	NM_H	NM_L
150	149.3	-149.3	51.4	-51.4	98.4	98.4
170	169.6	-169.6	54.3	-54.3	115.6	115.6
200	199.9	-199.9	58.0	-58.0	142.0	142.0
250	250.0	-250.0	62.9	-62.9	187.1	187.1
300	300.0	-300.0	66.9	-66.9	233.1	233.1
400	400.0	-400.0	73.0	-73.0	327.0	327.0

Noise Margin (T = -40C)

Table 2a

V_{SM}	V_{OH}	V_{OL}	V_{IH}	V_{IL}	NM_H	NM_L
150	149.3	-149.3	57.6	-57.6	91.7	91.7
170	169.6	-169.6	61.3	-61.3	108.4	108.4
200	199.9	-199.9	66.0	-66.0	133.9	133.9
250	250.0	-250.0	72.3	-72.3	177.7	177.7
300	300.0	-300.0	77.3	-77.3	222.7	222.7
400	400.0	-400.0	85.0	-85.0	315.0	315.0

Noise Margin (T = 16.9C)

Table 2b

V_{SM}	V_{OH}	V_{OL}	V_{IH}	V_{IL}	NM_H	NM_L
150	149.3	-149.3	65.2	-65.2	81.2	81.2
170	169.6	-169.6	70.6	-70.6	97.1	97.1
200	199.9	-199.9	77.4	-77.4	121.5	121.5
250	250.0	-250.0	86.3	-86.3	163.4	163.4
300	300.0	-300.0	93.4	-93.4	206.6	206.6
400	400.0	-400.0	104.2	-104.2	295.8	295.8

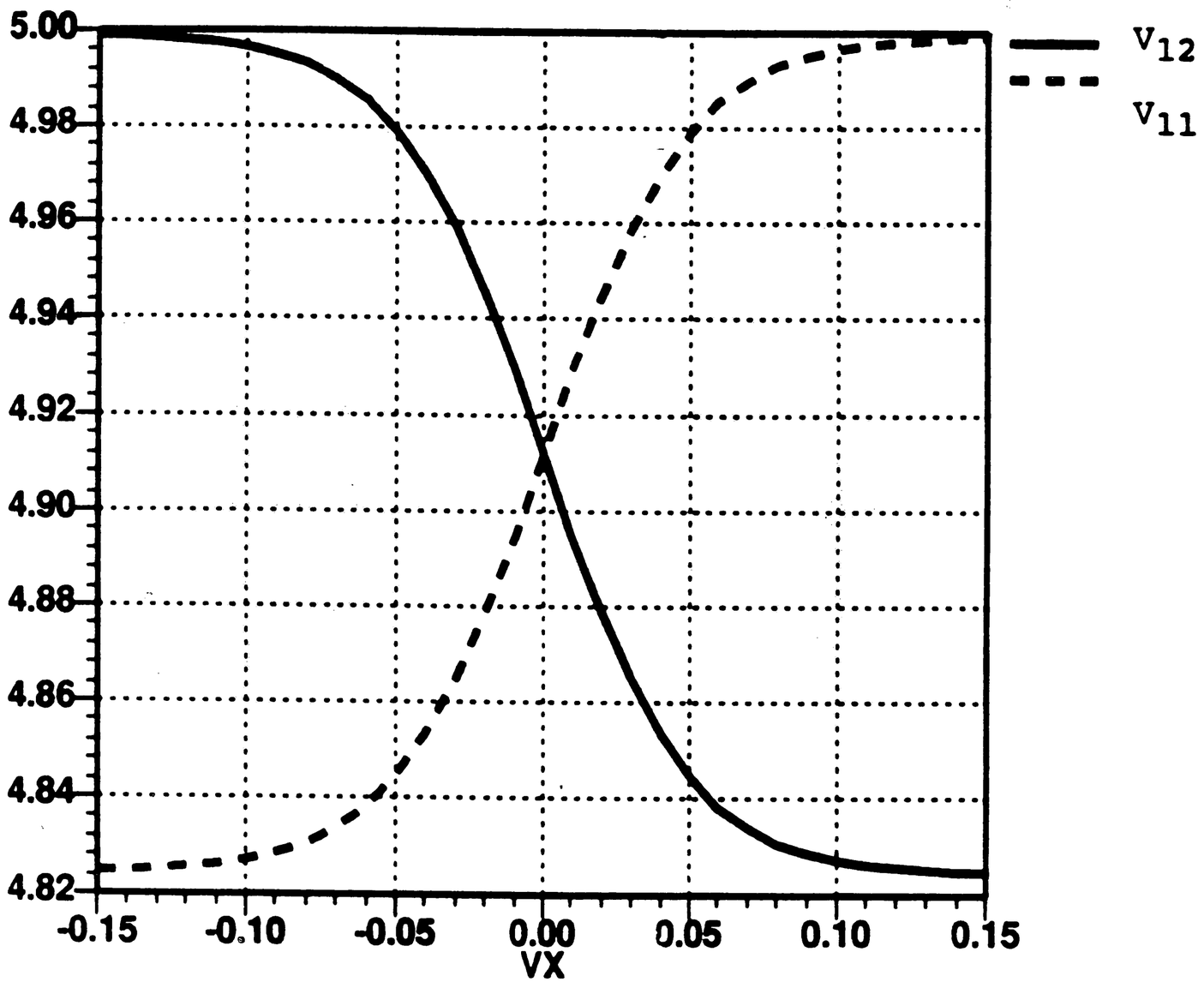
Noise Margin (T = 120C)

Table 2c

The noise margin degrades as the temperature increases because V_t, and therefore, V_{OH} and V_{OL} increase with temperature. To obtain a DC noise margin of 115 mV, at 120 degrees, the voltage swing, V_{SM}, will need to be approximately 190 mV. The accuracy of the above calculations will be checked for V_{SM} = 170 mV.

2.1.3 SIMULATED DC NOISE MARGIN RESULTS

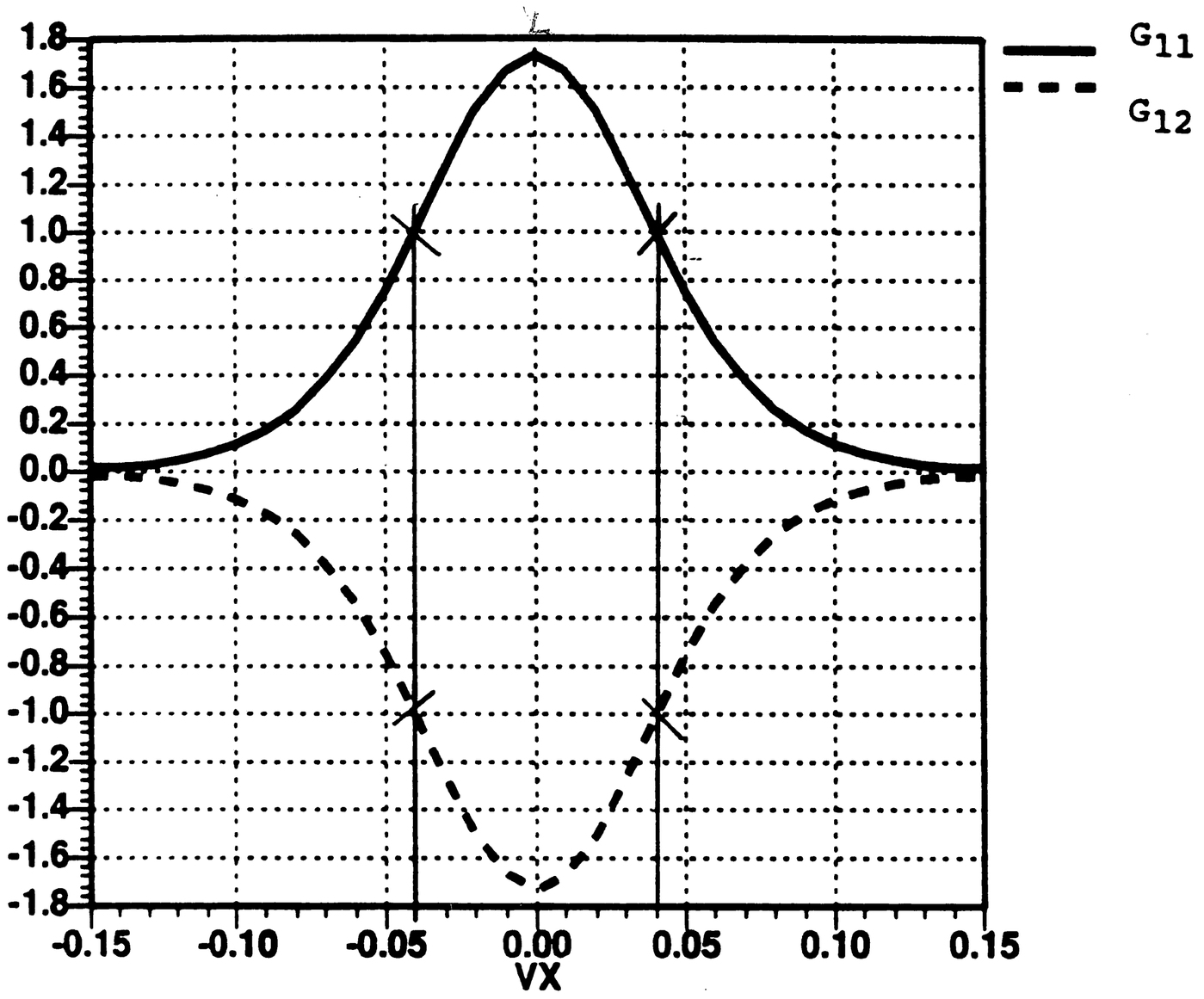
The DC simulations were performed at 120 degrees on an emitter-coupled pair with V_{SM} = 170 mV. The transfer characteristics of V_{11} and V_{12} are shown in Figure 5.



DC Transfer Characteristic

Figure 5

The unity gain points are distinguishable and it can be seen that V_{OH} and V_{OL} will be V_{SP} and V_{SP} - V_{SM} respectively. The single ended gains G_{11} and G_{12} are shown in Figure 6. The intersection of the curves with 1 and -1 show that V_{IH} = +38mV and V_{IL} = -38mV.



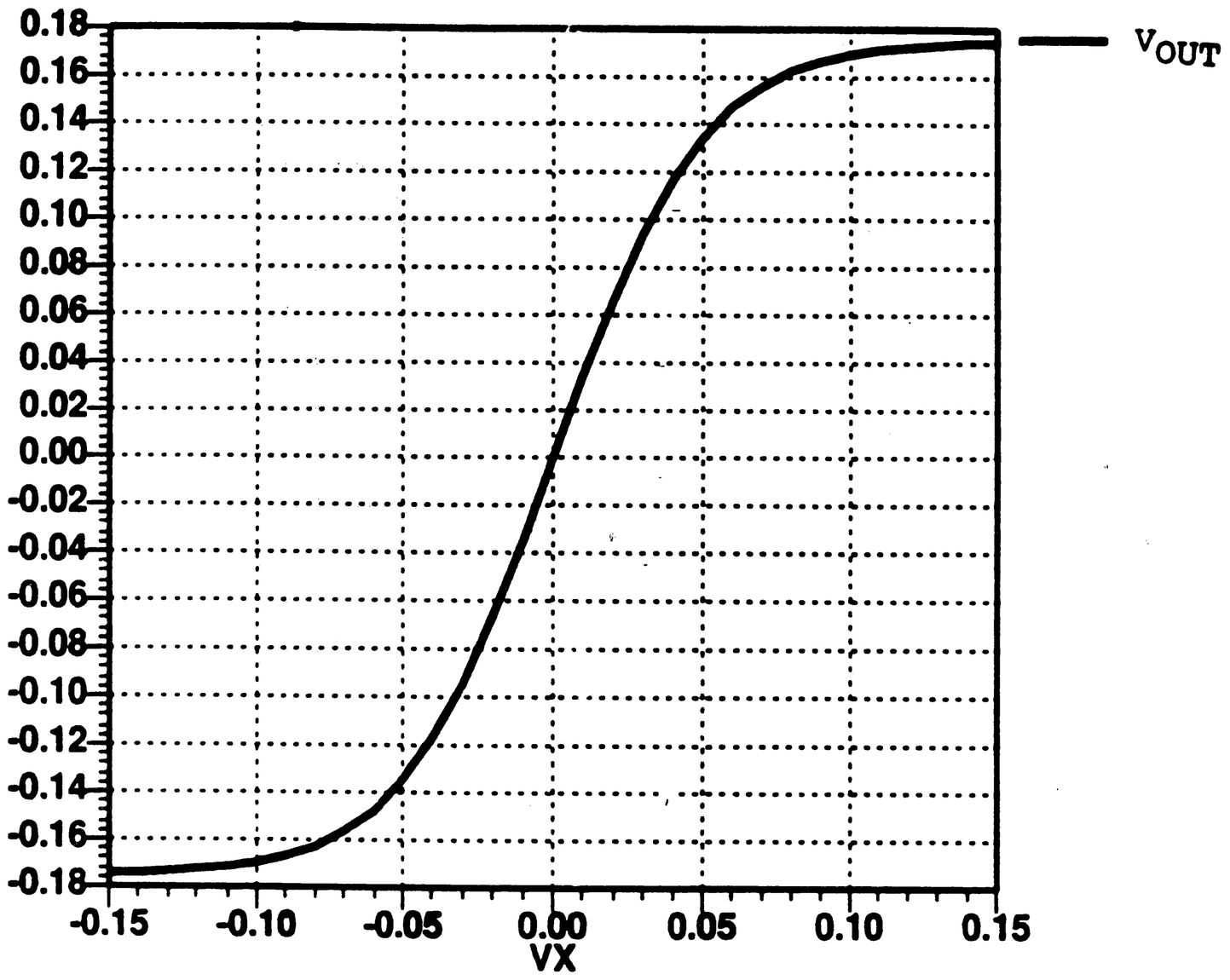
DC Gain

Figure 6

The differential output voltage, V_{OUT}, is the difference between V_{11} and V_{12}; therefore, if V_{11} varies by V_{SM}, the differential voltage will vary by 2 times V_{SM}. The DC transfer characteristic of V_{OUT} is shown in Figure 7. The values for V_{OH} and V_{OL} are:

$$V_{OH} = + V_{SM}$$

$$V_{OL} = - V_{SM}$$



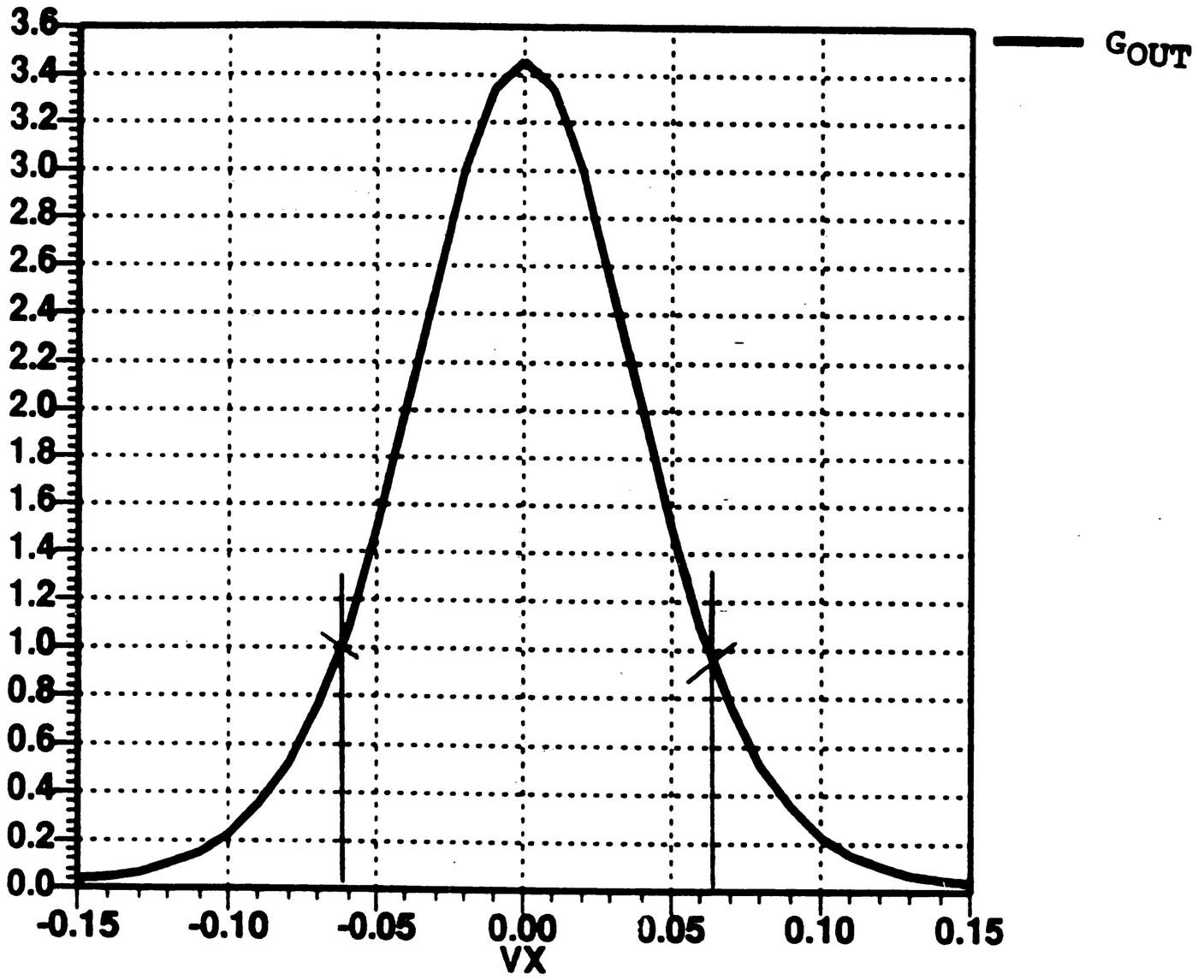
DC Differential Output Voltage

Figure 7

The differential gain of the emitter-coupled pair is shown in Figure 8. The plot of G_{OUT} was obtained by differentiating the waveform of Figure 7. The same result could have been reached by subtracting G_{12} from G_{11}. From Figure 8, V_{IH} and V_{IL} respectively are:

$$V_{IH} = + 63 \text{ mV}$$

$$V_{IL} = - 63 \text{ mV}$$



DC Differential Gain

Figure 8

The simulated noise margins are:

$$NM_H = 107 \text{ mV}$$

$$NM_L = 107 \text{ mV}$$

The simulations were done using a circuit simulator called ADVICE which offers greater accuracy than most circuit simulators. The transistor models are given in Appendix 2.

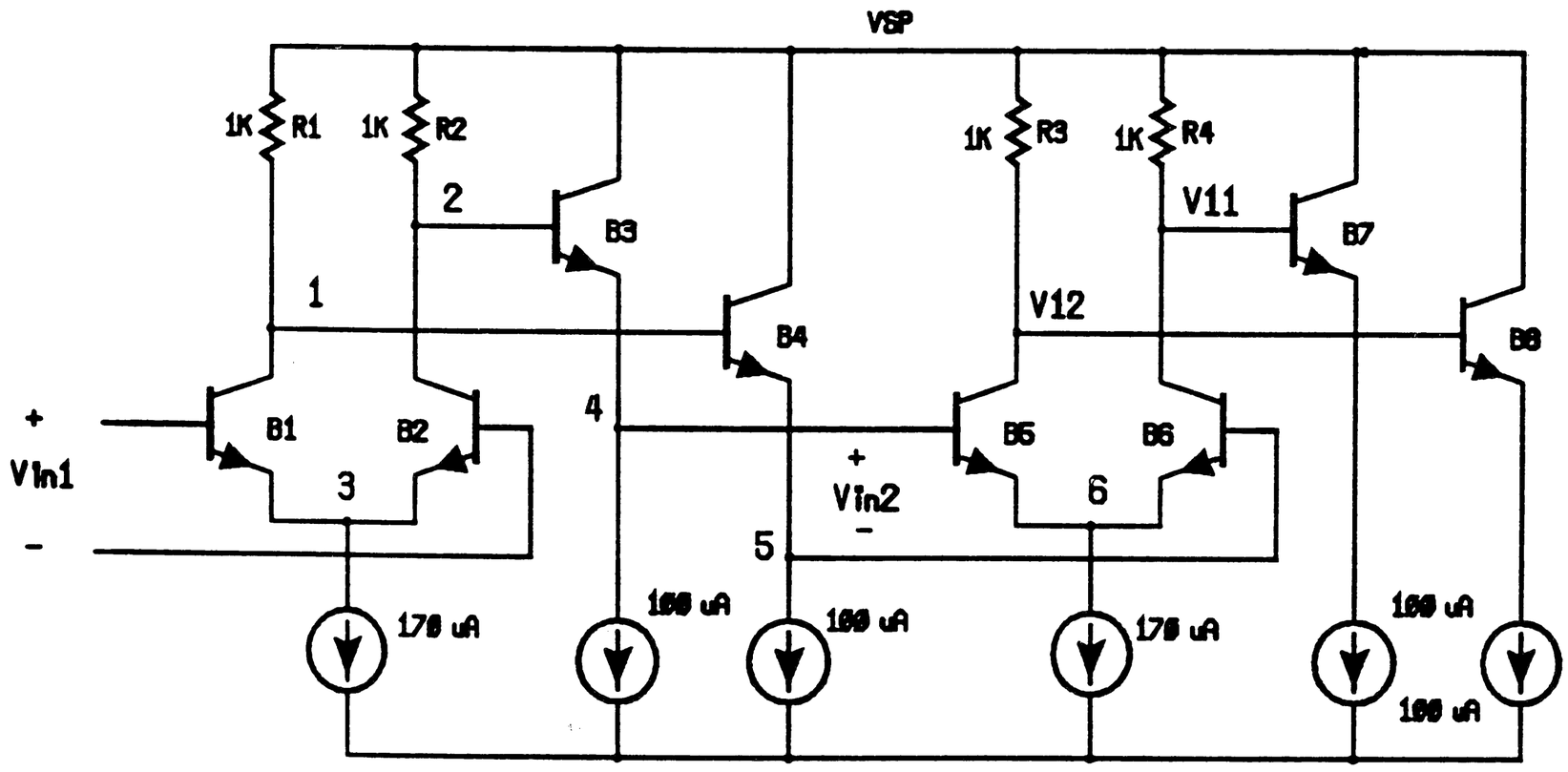
The simulations were performed at a temperature of 120 degrees Celsius. The logic family is being designed for the ambient temperature range of 0 to 80 degrees Celsius. If the ambient is 80 degrees, the junction temperature is higher because of the thermal coefficient of the package. The junction temperature will depend on the package and on the power consumed by the circuit.

It was assumed that the thermal coefficient would be 40 degrees/watt, which is average for a 44-pin PLCC package. It was also assumed that the largest circuit would consume 1 watt. Therefore, at an ambient temperature of 80, the junction temperature would be 120 degrees Celsius.

For V_{SM} = 170 mV at 120 degrees, Table 2c shows the expected noise margin as 97 mV, while the simulated noise margin is 107 mV. The calculated noise margins are first order while the simulated noise margins account for higher order effects. The single data point taken shows the true noise margin to be slightly higher than that of the calculations. The simulations show that V_{SM} = 170 mV is almost sufficient to meet the DC noise goal of 115 mV.

2.2 MAXIMUM VOLTAGE SWING

Logic functions implemented in a MOS process provide noise margins on the order of volts; depending on the supply voltage. In contrast, the noise margins in Tables 2a, 2b and 2c are only hundreds of millivolts. The noise margin does increases as the voltage swing increases; however, there is an upper limit on V_{SM}. If V_{SM} is too large, transistors will be driven into saturation and performance will deteriorate. The maximum V_{SM} can be calculated by analyzing two emitter-coupled pairs with emitter followers as shown in Figure 9.



Maximum Vsm

Figure 9

Assume that V_{IN1} is a logic high; therefore, the current through R_2 is zero. The node voltages are as follows:

$$\text{node 2:} \quad V_2 = V_{SP}$$

$$\text{node 4:} \quad V_4 = V_{SP} - V_{BE}$$

$$\text{node 6:} \quad V_6 = V_{SP} - 2V_{BE} \qquad (16)$$

Assume that V_{SM} is so large that transistor B5 is saturated. In saturation, the collector-emitter voltage, $V_{CE(SAT)}$, of B5 is known and the voltage at node 6 can also be expressed as:

$$\text{node 6:} \quad V_6 = V_{SP} - V_{SM} - V_{CE(SAT)} \qquad (17)$$

Equations 16 and 17 can be equated to find the maximum voltage swing that will saturate devices:

$$V_{SM(MAX)} = 2V_{BE} - V_{CE(SAT)} \qquad (18)$$

Since V_{BE} decreases with temperature and emitter current, V_{BE} should be measured at the highest temperature with the minimum amount of emitter current during normal operation. The maximum junction temperature is 120 degrees Celsius. Measurements on a

larger, but similar transistor showed V_{BE}, under high temperature, low current conditions, to be:

$$V_{BE} = 0.55 \text{ V}$$

If the transistor is driven into deep saturation, V_{CE} is about 150 mV. However, as the transistor passes from the active mode to the saturated mode, it must pass through the quasisaturation region [6]. The effects of the quasisaturation region are noticeable when the current through the transistor is many times higher than the peak F_T current. A conservative design would try to minimize the effects of the quasisaturation region. This is accomplished by using a small V_{SM} or by not using excessive current in the transistors. On the target technology, the quasisaturation region started at approximately V_{CE} = 820 mV. Using the above voltages, $V_{SM(MAX)}$ is tabulated in Table 3:

Temp Celsius	$V_{SM(MAX)}$ Deep Sat (mV)	$V_{SM(MAX)}$ Quasi-Sat (mV)
120	950	280

Maximum V_{SM}

Table 3

The choice of V_{SM}, from a DC viewpoint, depends only on the maximum allowed swing and the desired noise margin. The current levels, for the target technology, are not above the peak F_T current; hence, the quasisaturation region is not a consideration and V_{SM} does not need to be limited to 280 mV.

2.3 LOGIC LEVELS

The simple emitter-coupled pair has been useful for analysis, but it is not very useful as a logic element. More complex logic functions require the stacking of emitter-coupled pairs; which is known as series gating [7] [1]. A 3-input AND gate is shown in Figure 10. There are 3 levels of emitter-coupled pairs. The first level emitter-coupled pair has the tags IX and IXN attached to the base inputs, the second level is labeled IY and IYN, while the third level is IZ and IZN. The letter 'N' at the end of a signal name signifies that it is a complementary signal; thus the signal IXN is the complement of IX.

The corresponding X, Y and Z level outputs are shown as OX, OY and OZ and their complements. The logic levels

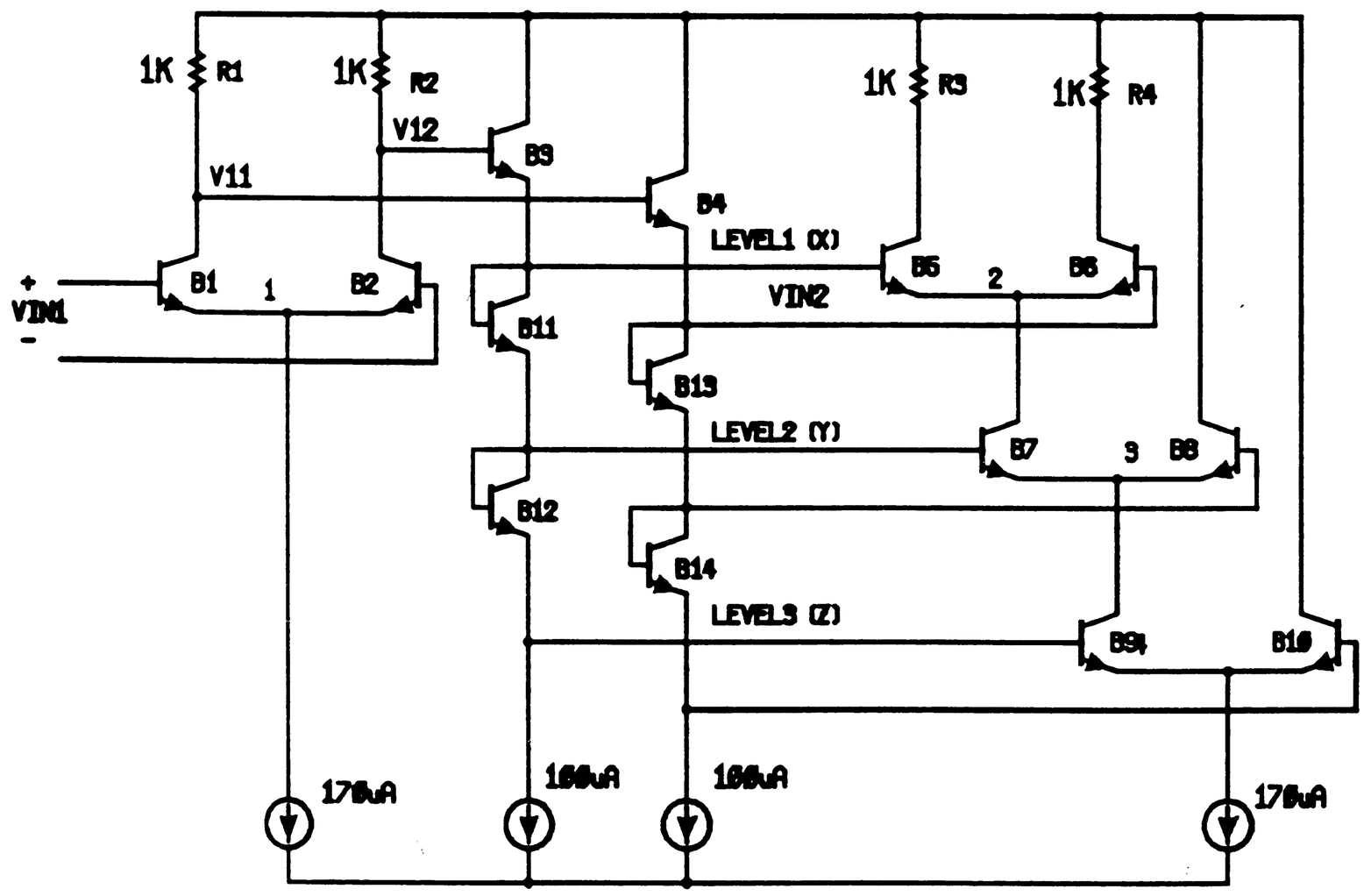
must be separated by a wide enough margin to prevent devices from saturating. It will be shown that the logic levels need be separated by only a single V_{BE} drop.

The devices labeled B9, B10, B12 and B13 are diode connected and are biased with the same current; therefore, the logic levels are separated by approximately equal diode drops.

3-Input AND Gate

Figure 10

The magnitude of the diode drop changes with temperature. At room temperature V_{BE} = 0.7 V while at 120 degrees Celsius, V_{BE} = 0.55 V. It will be shown that the change does not affect the differential voltage applied across the emitter-coupled pair which means that the magnitude of the output voltage is independent of logic level separation variations. However, if the voltage between the logic levels gets too small, transistors could be forced into saturation. The circuit of Figure 11 is used to analyze V_{BE} variations and the effect on logic levels.



Logic Level Analysis

Figure 11

If V_{IN1} is set to a logic high, the drop across R_2 is zero. The loop equation for V_{IN2} is:

$$V_{11} - V_{BE3} - V_{BE5} + V_{BE6} + V_{BE4} - V_{12} = 0 \qquad (19)$$

Since the diode drops are equal and their variation with temperature is matched, the equation becomes:

$$V_{IN2} = - V_{OUT} \qquad (20)$$

Therefore, temperature variations do not affect the magnitude of the differential voltage. Additional loop equations show that the low value of V_{BE} at high temperature does not cause one level to saturate another level. If V_{IN1}, in Figure 11, is a logic '1', the equation for the voltage at node 2 is:

$$V_2 = V_{SP} - V_{BE3} - V_{BE5}$$

$$V_2 = V_{SP} - 2V_{BE}$$

The voltage at node 3 is:

$$V_3 = V_{SP} - V_{BE3} - V_{BE11} - V_{BE9}$$

$$V_3 = V_{SP} - 3V_{BE}$$

The relationships between V_2 and V_3 are:

$$V_2 - V_3 = V_{CE7}$$

$$V_2 - V_3 = V_{BE}$$

Therefore, if

$$V_{BE} <= V_{CE(SAT)}$$

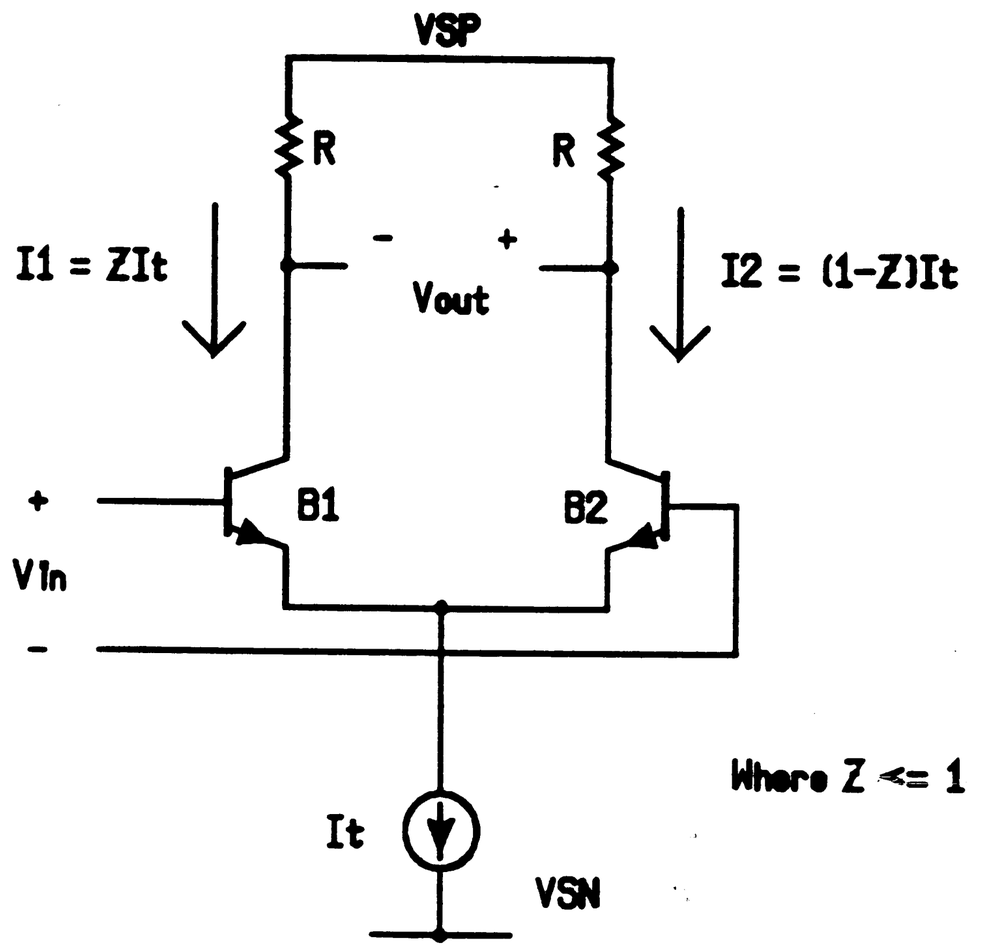
then the voltage between the logic levels is too small and transistors are being saturated. For the target process the minimum V_{BE} at high temperature is 550 mV; therefore, if the logic levels are separated by a single voltage drop there is no jeopardy of saturation. However, since the quasisaturation region begins at a higher voltage, the devices may operate in the quasisaturation region if the current levels were to be increased.

2.4 SERIES GATING

Series gating must be used to implement logic functions; however, a known problem caused by series gating is the degradation of V_{OH} and V_{OL} resulting in a decrease in the noise margins. It was mentioned that driving gates differentially compensates for the loss [5]. This paper develops the equations for an n level series-gated structure for differential and single-ended logic. This particular development has not been seen elsewhere. The analysis shows that the deleterious effects of series gating on single-ended logic are mitigated, by using differential logic.

The ratio between the currents in the transistors of an emitter-coupled pair are shown in Figure 12. The equation for the output voltage is:

$$V_{OUT} = (2Z - 1)RI_t$$



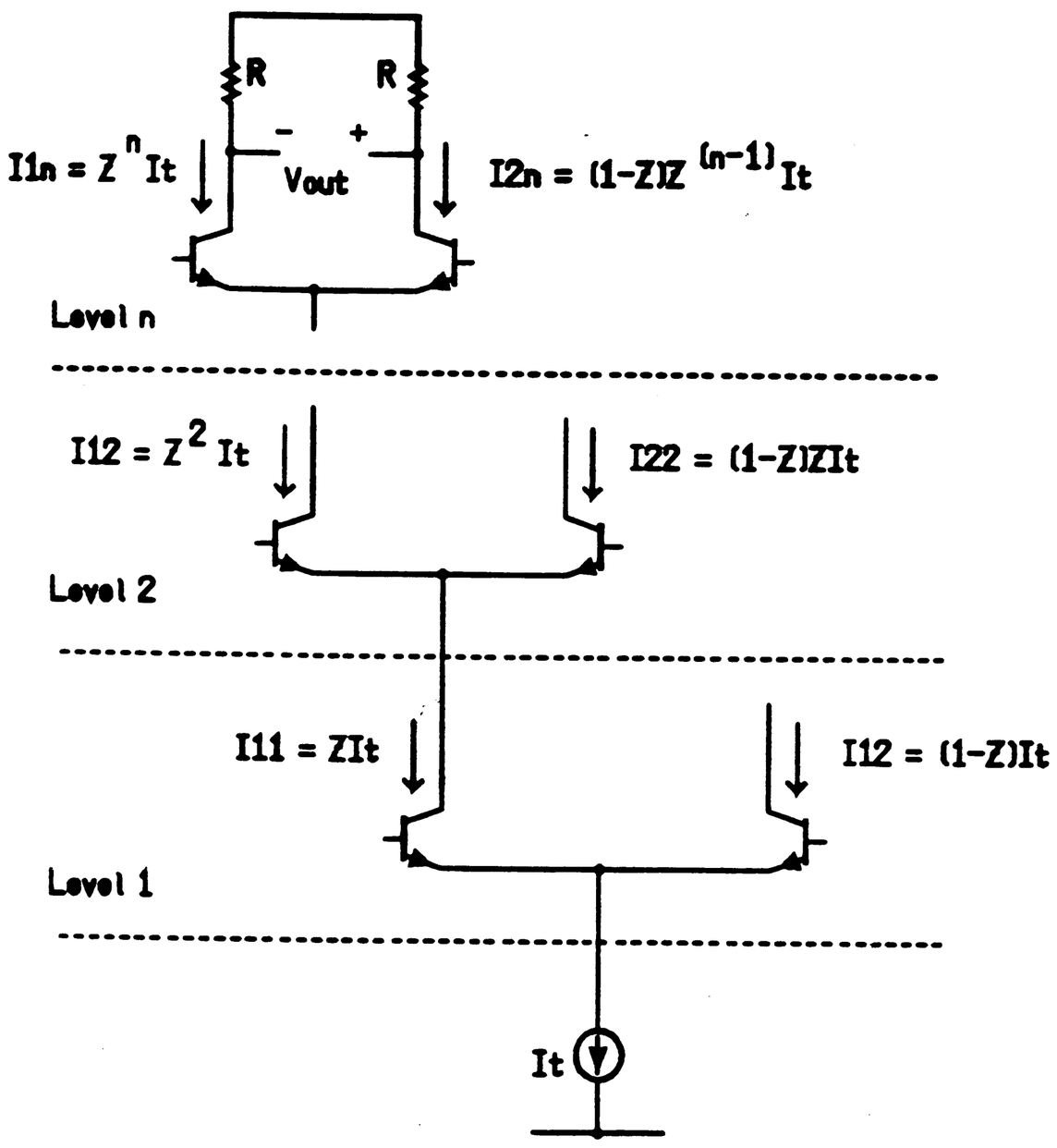
Current Ratios

Figure 12

The formula for Z is derived from equations 1 and 6b.

$$Z := \frac{1}{1 + e^{-\left[\frac{V_{in}}{V_t}\right]}} \qquad (21)$$

The value of Z ranges from 0 to 1 inclusive for both the single-ended and differential logic. Equation 21 describes a differential gate when V_{IN} ranges from $-V_{SM}$ to $+V_{SM}$. The limits of V_{IN} for a single-ended gate is $-V_{SM}/2$ to $+V_{SM}/2$. A series gating structure of n levels is shown in Figure 13.



Series Gating Current Ratios

Figure 13

The differential output voltage is:

$$V_{OUT} = (2Z - 1)Z^{(n-1)}RI_t$$

and the non-inverting single-ended output voltage is:

$$V_{OUT} = Z^n RI_t$$

As n increases, the output voltage and therefore noise margins decrease. The deterioration of the noise margin is severe in the single-ended logic. The quantity

$$(2Z - 1)Z^{(n - 1)}$$

for the differential case is shown in Table 4 and

$$Z^n$$

from the single-ended output voltage is shown in Table 5 for different values of n.

	$(2Z - 1)Z^{(n-1)}$				
V_{SM}	n=1	n=2	n=3	n=4	n=5
150	0.9951	0.9779	0.9610	0.9398	0.9145
170	0.9978	0.9900	0.9823	0.9725	0.9607
200	0.9993	0.9970	0.9946	0.9916	0.9880
250	0.9999	0.9996	0.9993	0.9989	0.9984
300	1.0	0.9999	0.9999	0.9998	0.9998
400	1.0	1.0	1.0	1.0	1.0

Differential V_{OUT} for Series Gating

Table 4

	Z^n				
V_{SM}	n=1	n=2	n=3	n=4	n=5
150	0.9526	0.7434	0.5541	0.3747	0.2299
170	0.9677	0.8194	0.6721	0.5163	0.3714
200	0.9820	0.8962	0.8035	0.6947	0.5792
250	0.9933	0.9604	0.9225	0.8742	0.8174
300	0.9975	0.9852	0.9707	0.9517	0.9284
400	0.9997	0.9980	0.9960	0.9933	0.9900

Single-ended V_{OUT} for Series Gating

Table 5

Based on the information of Table 4, if V_{SM} = 170 mV and n = 3, the V_{OH} and V_{OL} of the gate would be 3 mV lower and higher, respectively, than the values given in Table 2b. Therefore, NM_H and NM_L would decrease by 3 mV which is a 2.7% change. With 5 levels of logic, the noise margins are decreased by only 6.6 mV; a 6.2% change. The effects of series gating are minimal in a differential logic family.

The effect on single-ended logic is more drastic. With V_{SM} = 170 mV and n = 3, the noise margins are decreased

by 55.7 mV. The data of Table 5 shows that V_{SM} would have to be doubled to operate as well as the differential logic, which makes sense because differential operation is equivalent to doubling V_{SM} without changing anything.

The consequences of series gating have been mitigated by differential operation. Most single-ended logic families do not suffer from series gating problems because a large voltage swing is used. The other factor that limits the number of possible logic levels is the supply voltage. The maximum number of logic levels is determined by the magnitude of V_{BE}, the voltage across the current source and the drop across the load resistors. Conservatively, if 1 volt is allocated for each logic level, the current supply transistor and the load resistor, the formula for the required power supply voltage would be:

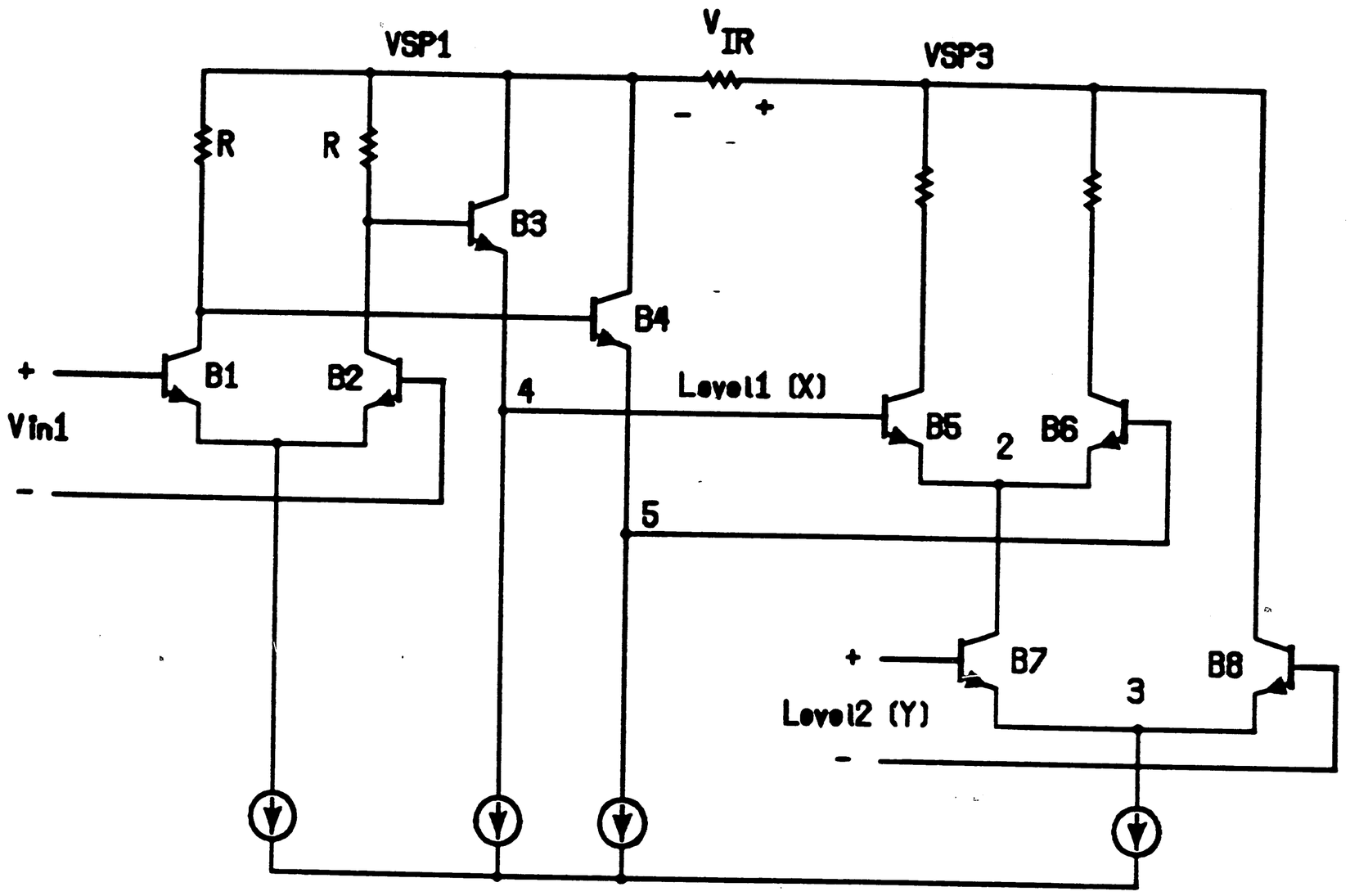
$$V_{SP} = n + 2$$

Therefore, a logic gate powered by a 10 V supply, could conservatively have a maximum of 8 logic levels. The family under consideration works with a 5 V supply and has a maximum of 3 levels.

2.5 IR DC NOISE

The operation of the logic is also affected by the placement of the gates when developing larger circuit blocks. Voltage (IR) drops in signal lines between gates due to the metal resistance is a source of DC noise. The circuit of Figure 14 can be used to determine the maximum allowable IR drop. The resistor V_{IR} represents the resistance of the supply line. The maximum voltage drop across V_{IR} will be calculated. Once the maximum voltage drop and metal sheet resistance are known, the maximum allowable current through the supply line can be calculated. The analysis is similar to the logic level analysis.

Assume that V_{SP3} is directly connected to the supply; therefore, V_{SP1} is at a lower potential due to the voltage drop represented by V_{IR}. The nodes 4 and 5 vary directly with V_{SP1} and represent the X logic level as shown in Figure 11. The input voltage V_{IN2} enters at the Y logic level. As V_{SP1} decreases, the difference between the X and Y levels decreases and transistor B7 saturates.



IR DC Noise

Figure 14

As previously shown when analyzing the logic levels in Section 2.3, the voltage difference between nodes 2 and 3 must not be less than $V_{CE(SAT)}$; which is about 150 mV. In Figure 14 it can be seen that:

$$V_{IR} = V_{SP3} - V_{SP1}$$

and it was shown in Section 2.3 that

$$V_{level1} - V_{level2} = V_{BE}$$

To avoid saturating transistors, the following must be true:

$$V_{level1} - V_{level2} - V_{IR} >= V_{CE(SAT)}$$

Combining equations yields the maximum IR drop in a signal line:

$$V_{IR} <= V_{BE} - V_{CE(SAT)}$$

Since the lowest value of V_{BE} is 550 mV, the maximum value of V_{IR} is 400 mV. This constraint applies to all signal lines. The IR drop in any line cannot exceed $V_{BE} - V_{CE(SAT)}$ or there will be danger of saturating a device. So, as cells are connected together, the signal lines must be made wide enough to ensure less than a 400 mV drop from point to point.

3.0 LOGIC FAMILY

A 3-input AND gate from the logic family was introduced in Figure 10. The logic levels were explained where the X level is the highest logic level, Y the next and Z the lowest logic level. The family consists of a subset of

unique cells while the remainder are derivatives of the unique cells. For example, The 3-input AND gate required original layout. The 3-input NAND gate is a derivative of the 3-input AND gate. It is made by inverting the output signals of the 3-input AND gate. Since the logic is fully differential, inverting a signal is a simple as making OX become OXN, OY become OYN and OZ become OZN and visa-versa. In other words, a simple label change on the schematic and layout is enough to produce the 3-input NAND.

3.1 NOMENCLATURE

The cell nomenclature is straight forward. The name AND3 means a 3-input AND gate. A MUX2 stands for a 2:1 mux. The names for the Flip-Flops (FFs) are more cryptic. Each FF is given a 3 letter name, "Fab", where the letters stand for:

F = Flip Flop

a =	1	positive edge triggered
	2	negative edge triggered
	3	positive level triggered
	4	negative level triggered
	5	positive edge triggered, fixed D input
	6	negative edge triggered, fixed D input

	7	positive level triggered, fixed D input
	8	negative level triggered, fixed D input
b =	A	no preset or clear
	B	preset
	C	preset and clear
	D	clear

The logic family has been developed with two different current levels. The low power gates use I_t = 170 microAmps. The higher power gates use I_t = 340 microAmps. The different power levels enable the gates to work at 50 MHz and 100 MHz respectively over process variations and temperature. A gate that has higher current is denoted by appending an 'H' in the name. For example, the AND2H is a higher current 2-input AND gate. There is one case in which I_t was lowered to be approximately 100 microAmps. The gates are the DEL1L and DEL1LXY. The current was decreased so the gates would provide more of a delay.

Generally, each gate provides all three output levels, X, Y and Z. However, in some cases, area was saved by providing only the X and Y or only the X level outputs. An example is the DEL1 and DEL1XY gates. The DEL1 is

delay gate that provides the 3 output levels, whereas, the DEL1XY provides only the X and Y outputs. The DEL1X would be a delay gate that had only the X output level.

3.2 GATES DEVELOPED

The unique cells were those that required original layout. All other gates are a derivative of a unique cell. They were obtained by complementing input or output signals or by simple resistor value changes to allow higher currents. The unique cells are the following:

AND2: 2-input AND gate	XOR2: XOR gate
AND3: 3-input AND gate	MUX2: 2:1 multiplexer
DEL1: Delay gate	
REF0: Logic 0 reference	REF1: Logic 1 reference

F1A	F1B	F1C	F1D
F3A	F3B	F3C	F3D
F5B	F5D	F7A	F7D

The derivative cells are the 'H' version of most of the above gates in addition to:

OR2	NOR2	NAND2	
F2A	F2B	F2C	F2D

F4A	F4B	F4C	F4D
F6B	F6D	F8B	F8D

Counting all of the unique cells and their derivatives, the library of logic gates consists of 53 cells. Schematics and data sheets for most of the above gates are located in Appendix 1.

3.3 DESCRIPTION OF OPERATION

The logic family was designed to have a nominal voltage swing, V_{SM}, of 170 mV. The differential voltage swing is 340 mV. Therefore, the noise margin, as determined by simulations is 107 mV at 120 degrees Celsius. Other differential designs have a logic swing that ranges from 230 to 500 mV [1] [8] [9] [10] [11], but it is not always clear if VSM or the differential voltage swing was cited. The logic swing of this design seems comparable.

The logic is designed to have a constant voltage swing over temperature and process variations. The bias circuitry will be described followed by an explanation of the operation of two basic gates; the AND2 and F1C gates.

3.3.1 CURRENT BIAS CIRCUIT

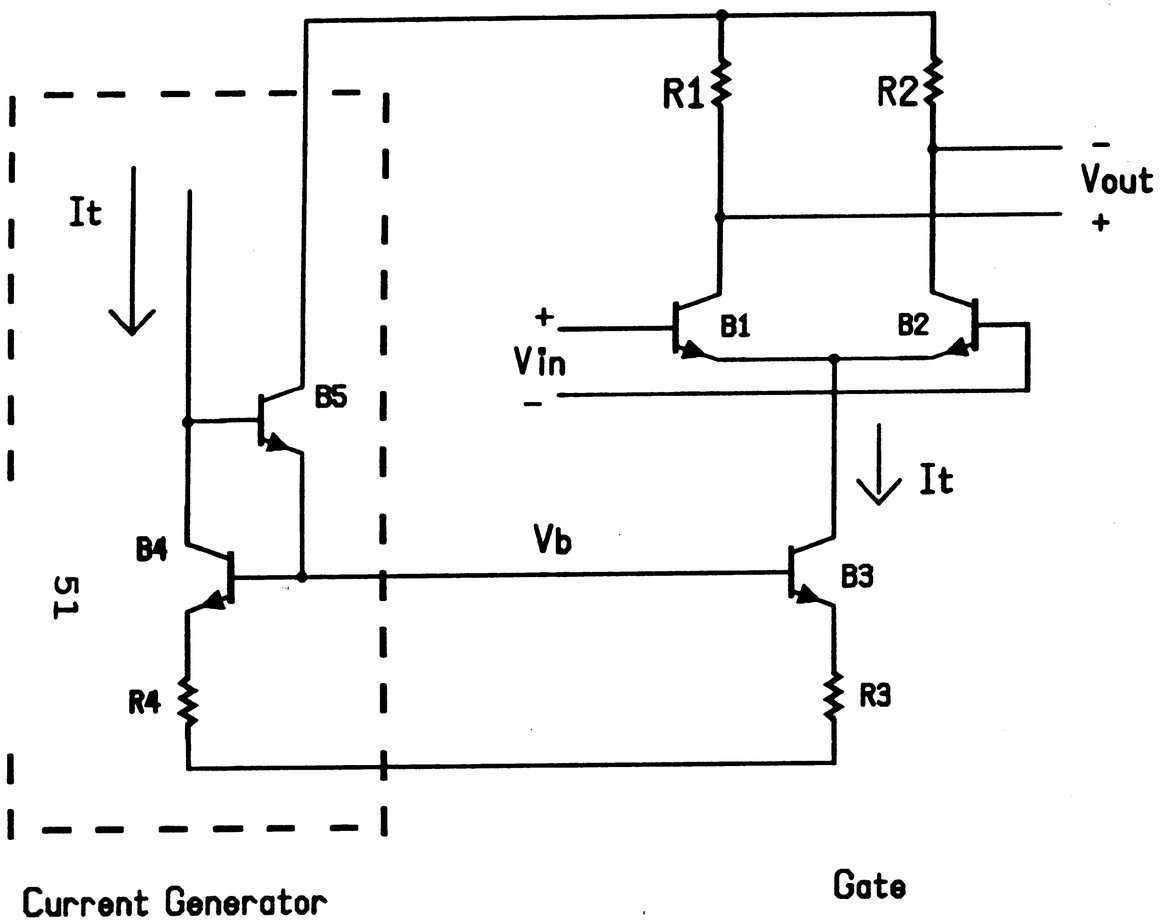
An emitter-coupled pair with its associated transistor current source is shown in Figure 15. The transistor B3 operates as a current source. The bias voltage Vb sets the magnitude of I_t. The node Vb is part of a current mirror also shown in Figure 15. The current I_t can be mirrored in to more than one logic gate. The current mirror will not be shown in subsequent discussion of the gates. The manner in which I_t is generated affects the noise margin.

The voltage swing of a gate is developed across R_1 and R_2 as shown in Figure 15. The resistor variation with process can be as much as +/- 20%; furthermore, the resistors also have a positive temperature coefficient. If the current, I_t, in the gate were held constant regardless of temperature or process variations, the voltage swing would vary at least +/- 20% as the value of the resistors changed. A variable voltage swing would result in a variable noise margin which is an undesirable situation. Furthermore, the transient characteristics of the gate would be negatively affected; therefore, the voltage swing is held constant by varying the current, I_t, appropriately.

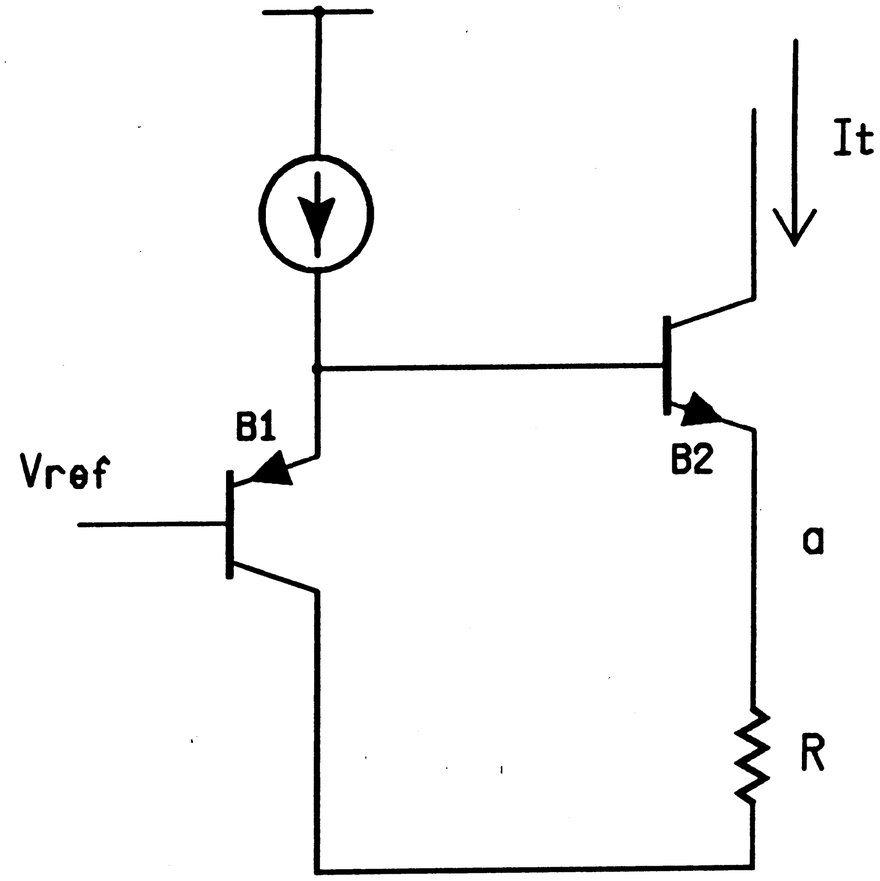
The circuit concept for varying the current is shown in Figure 16. The basic concept is to hold the voltage across a resistor constant over temperature and process. The current flowing through the resistor will be proportional to the variations in the value of the resistor and can be used to maintain a constant voltage swing in the gates. In Figure 16, V_{REF} is the independent voltage. It is fixed across the resistor by the transistors B1 and B2. The resulting proportional current is mirrored, as shown in Figure 15, into the logic gates so that they have a constant voltage swing. The actual design uses a BandGap Reference Generator [15] to produce the independent voltage V_{REF}.

3.3.2 AND2 GATE

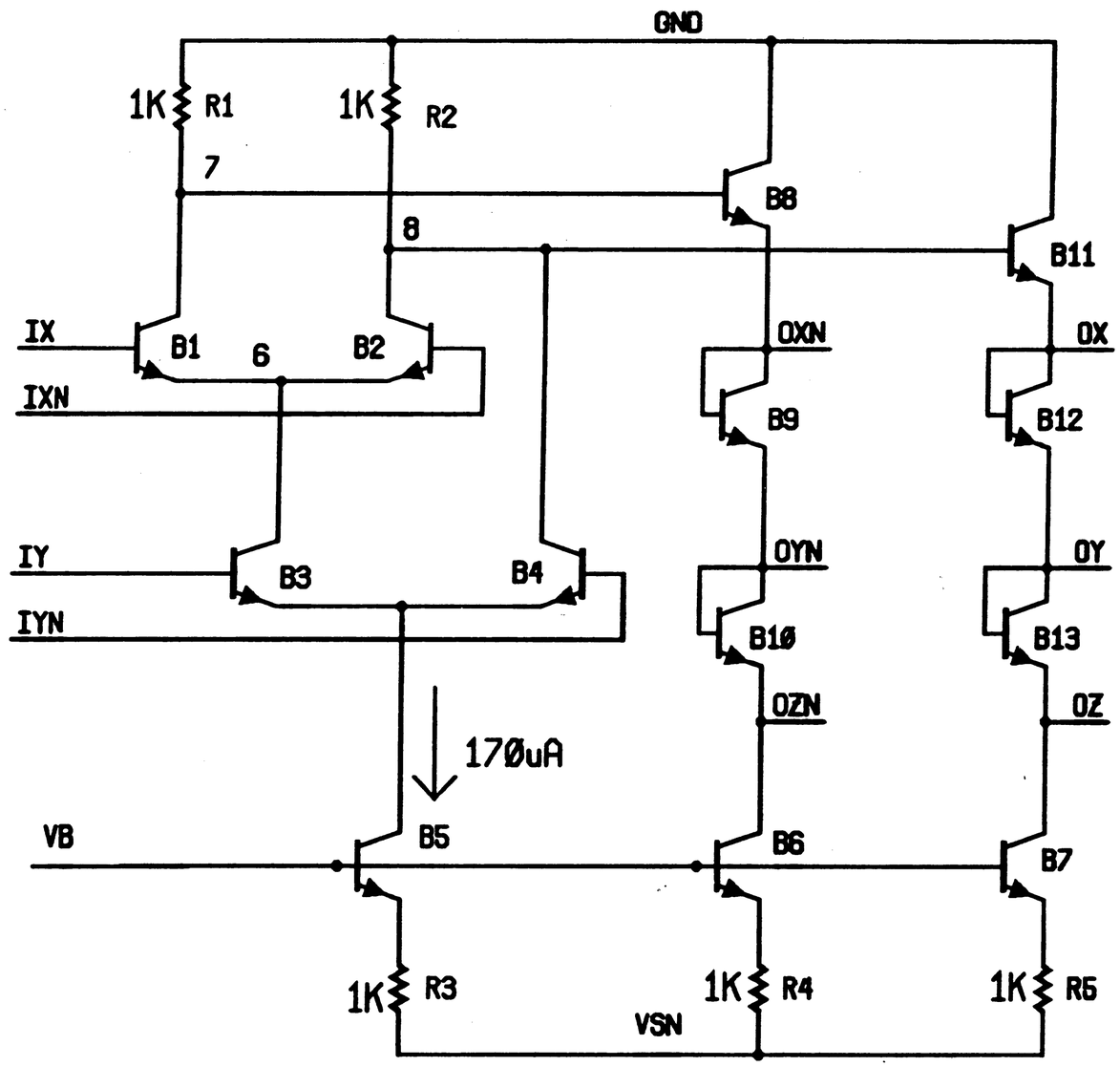
The AND2 gate is shown in Figure 17. If the IX and IXN inputs are a logic '1', meaning IX - IXN = +170 mV, and the IY and IYN inputs are also a logic '1', the current will be steered through R_1, B1 and B3. The voltage of node 7 will be lower than the voltage of node 8; therefore, the output will be a logic '1'. If either of the inputs is a zero, the current is sent through R_2, thereby making the output a logic '0'.



Current Generator
Figure 15

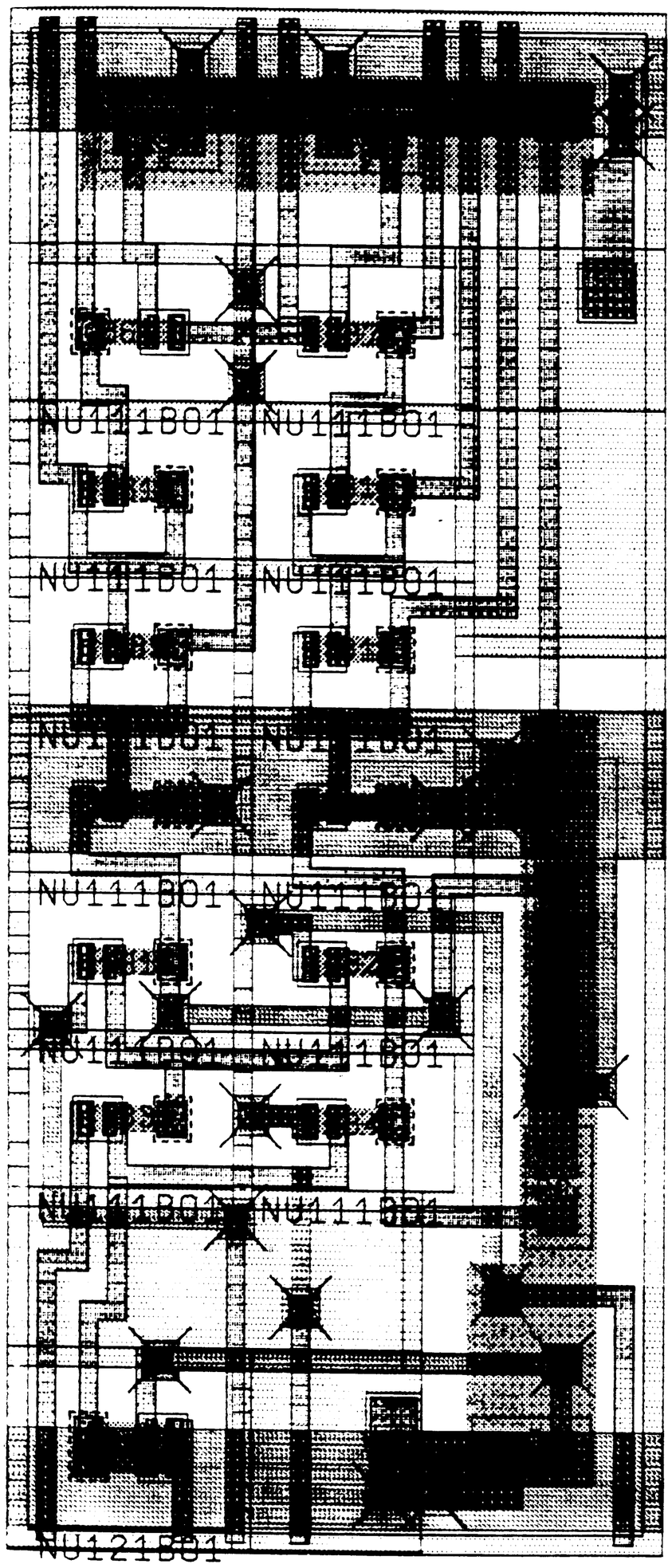


Biasing Current Concept
Figure 16



AND2 Gate

Figure 17



AND2 Layout

Figure 18

The layout of the AND2 gate is shown in Figure 18. The dimensions are 135 X 310 microns. The inputs enter at the bottom and the outputs leave at the top of the cell. The power supplies run horizontally through the cell and provide a continuous path for the supplies when cells are abutted. Routing channels form between rows of cells. The transistor has a single base stripe and its dimensions from the perimeter of the isolation is 51.5 X 36 microns. Parasitic capacitance values were extracted from the layout for simulation.

Circuit simulations were performed to quantify the transient characteristics such as propagation delay, rise and fall times. The simulations were done with process information that represented actual manufacturing variations. There were 7 distinct cases that tracked the changes in transistors and resistors. A bandgap voltage reference was used to produce a varying current that would provide a constant voltage swing, V_{SM}, over process and temperature variations. The results of simulation with a fan-out of 1 at 120 degrees Celsius are shown in Table 6. Complete data sheets for the gates can be found in Appendix 1.

Case	Rise time (ns)	Fall time (ns)	Propagation delay (ns)	Power (mW)	Power Delay Product (pJ)
0	3.36	3.35	1.61	1.82	2.9
1	2.23	2.24	1.08	1.47	1.6
2	1.19	1.19	0.67	2.36	1.6
3	2.16	2.16	1.05	1.55	1.6
4	1.75	1.75	0.91	1.46	1.3
5	2.23	2.24	1.08	1.47	1.6
6	1.52	1.54	0.79	2.24	1.8

AND2 Simulation Summary

Table 6

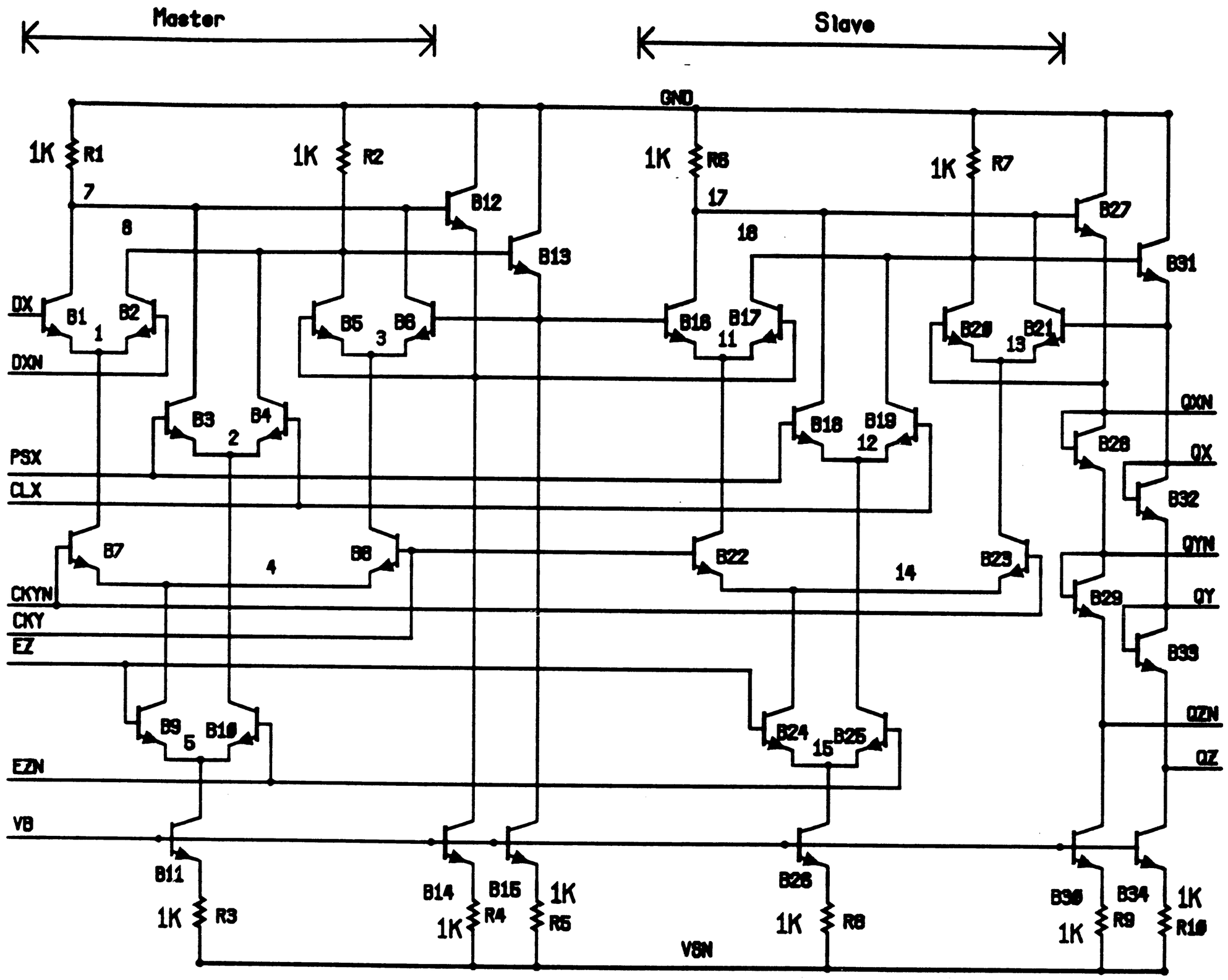
3.3.3 F1C FLIP-FLOP

The FF is more complex. As shown in Figure 19, the F1C consists of a master and a slave latch with emitter followers and in the case of the slave, diodes for output levels. The latches are the same except for the polarity of the clock connection. Ideally, when the clock is low, the master accepts data from the data line and the slave is latched. When the clock is high, the master is latched and the slave accepts data from the master. Therefore, the master latch accepts data from the outside world and passes it to the slave on the

rising edge of the clock. The data output value, held by the slave, is updated only on the rising edge of the clock.

The latches have a data input path and a feedback path. In the case of the master, the emitter-coupled pair formed by B1 and B2 is the data path. The transistors B5 and B6 form the feedback path. The clock transistors, B7 and B8 determine if the current flows in the data or the feedback transistors. When the clock is low, the data controls nodes 7 and 8 through the data transistors; the FF is in the flow through mode. When the clock goes high, the value of the data can change without affecting nodes 7 and 8 because the feedback latch transistors hold them fixed; the latch is in the latch mode.

The slave operates in a similar manner except it is in the flow through mode when the clock is high and latched when it is low. Further, the slave receives its data from the master. The transistors B3, B4, B9 and B10 asynchronously preset and clear the FF. The PSX and CLX lines are complements. If PSX is a logic '1', the FF is preset when the enable line, EZ, goes low. If CLX is high, the FF is cleared.



F1C Flip-Flop

Figure 19

The transient characteristics of the FF were determined through simulations over the 7 process cases. The results at 120 degrees Celsius are shown in Table 7. Data sheets of most of the gates are in Appendix 1.

Case	Propagation delay (ns)	Power (mW)	Power Delay Product (pJ)
0	2.28	6.27	14.3
1	1.58	5.05	8.0
2	0.97	8.13	8.0
3	1.54	5.36	8.3
4	1.28	5.03	6.4
5	1.53	5.05	7.7
6	1.39	7.65	10.6

F1C Simulation Summary

Table 7

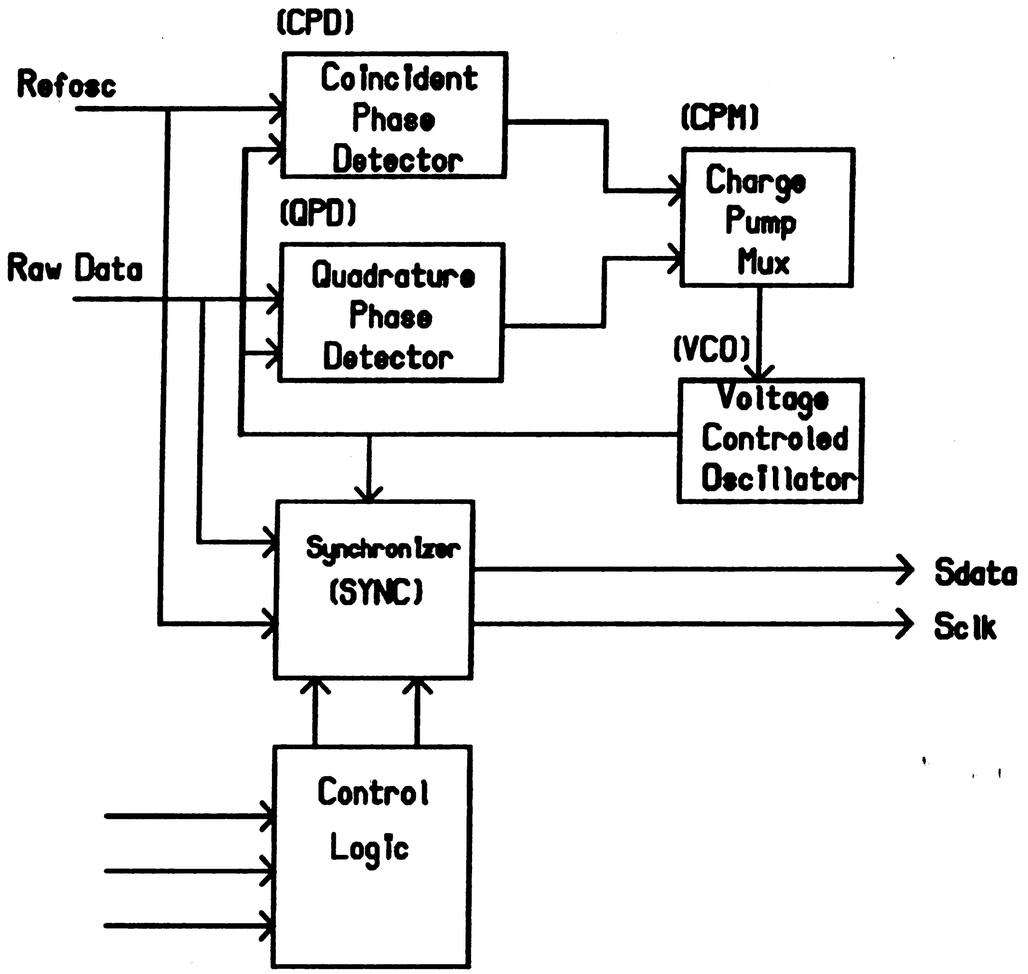
4.0 HARD DISK DATA SEPARATOR APPLICATION

The fully differential ECL logic was developed to be used in noisy, high speed environments such as hard disk drive electronics. An example circuit would be the digital portion of a Dual Phase Detector, 48 MBit/s data separator. A block diagram of the data separator is illustrated in Figure 20. The Phase Lock Loop (PLL)

contains analog circuits such as the Voltage Controlled Oscillator (VCO) and the Charge Pump. The remainder of the PLL and the other circuit blocks are digital by nature. The differential gates were developed to implement the digital blocks. The most critical sections are the phase detectors and the standardizer. The results from circuit simulations of the Coincident Phase Detector (CPD) are discussed here, to illustrate the application of the logic. The simulations were performed using the ADVICE circuit simulator.

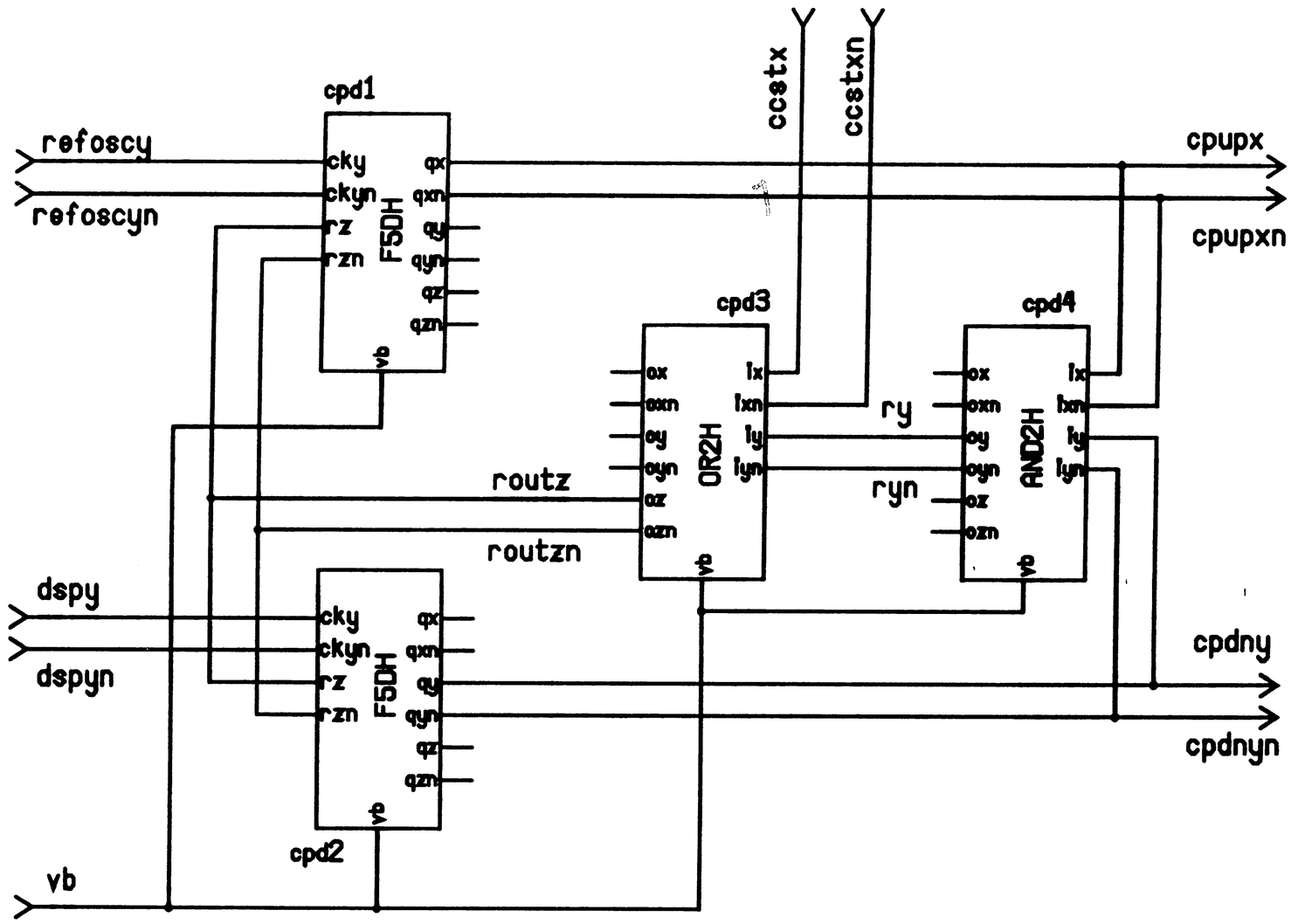
4.1 COINCIDENCE PHASE DETECTOR (CPD)

The Coincident Phase Detector is used to measure phase and frequency differences between the Reference Oscillator (REFOSC) and the VCO output signal which is called DSP [13] [14]. The CPD schematic is shown in Figure 21. The input signals, REFOSC and DSP go to the clock inputs on two F5DH FFs. The F5DH is a positive-edge triggered FF that has its input tied to a logic 1; therefore, each rising edge of the input signals will cause the output signals, CPUP and CPDN, to go high. The FFs are reset by the OR2H and AND2H gates. The reset signal, ROUT, goes high when CCST or CPUP and CPDN are logic 1 levels. Once the FFs have been reset, they can detect another rising edge of the input signals.



Data Separator Block Diagram

Figure 20



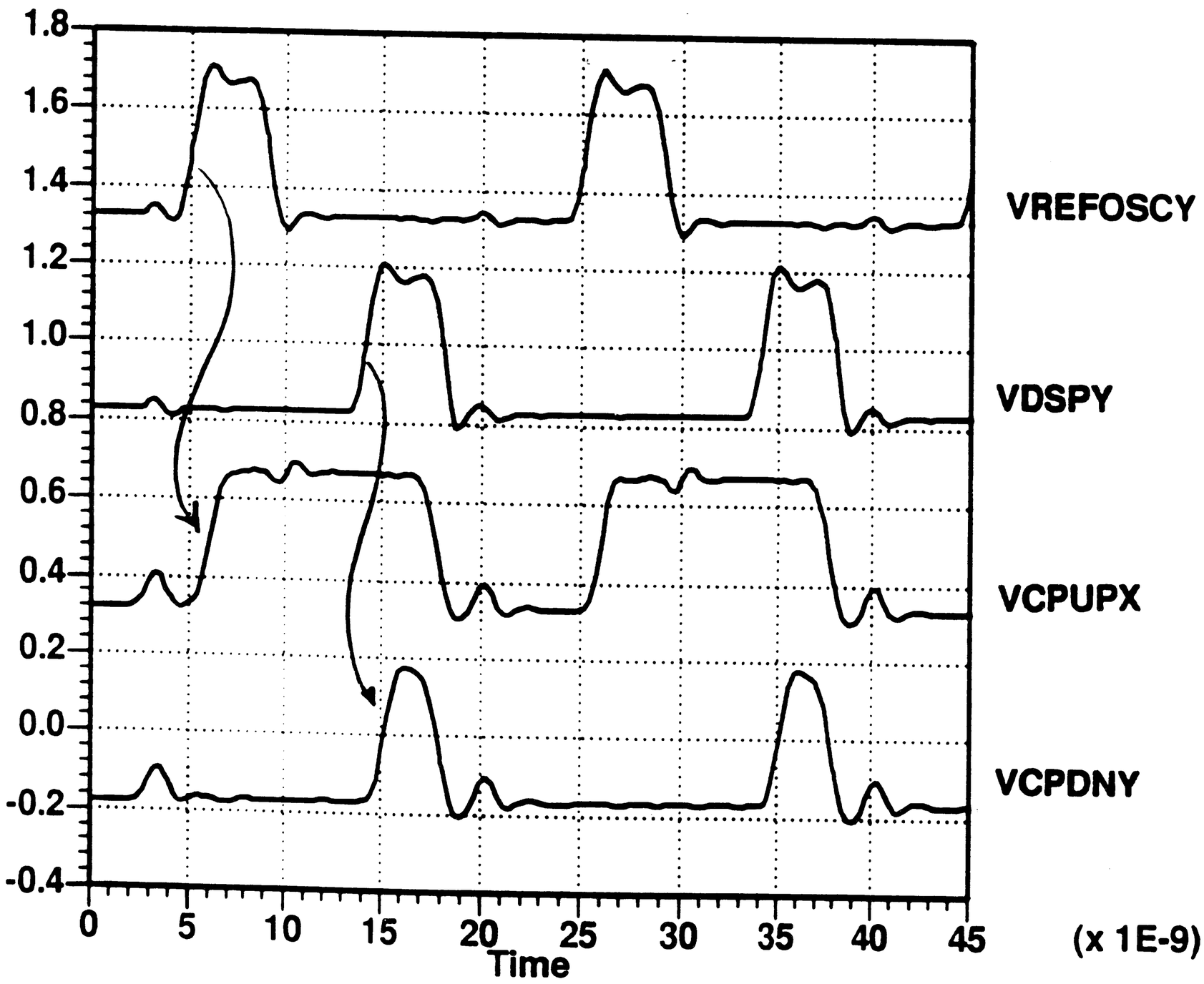
Coincident Phase Detector Schematic

Figure 21

The output signals CPUP and CPDN are called the pump-up and pump-down signals respectively. As mentioned above, when both output signals are high, the F5DH FFs are reset which in turn means that the output signals return to a logic 0. Since both signals must be high to reset the FFs, it is guaranteed that the CPUP and CPDN signals will go low simultaneously and hence the coincident nature of the phase detector; meaning the termination of the output signals is coincident.

The relative widths of the pump-up and pump-down signals determine if the VCO frequency will be increased (pumped up) or decreased (pumped down). As long as the input signals, REFOSC and DSP, are not in phase or frequency, the CPUP and CPDN outputs will have different widths.

Correct operation of the CPD can be seen in Figure 22. As shown, there is a phase difference between the REFOSC and DSP signals. The REFOSC signal leads the DSP signal; therefore, the VCO must speed up to eliminate the phase difference. Note that the CPUP signal goes high when the REFOSC signal goes high while the CPDN pulse is triggered by the DSP signal. Because of the phase difference, the CPUP signal goes high before the CPDN signal. The resulting CPUP pulse is wider than the CPDN pulse, so the VCO increases its speed. The VCO corrects



Correct Operation
of
Coincident Phase Detector

Figure 22

its speed until the CPUP and CPDN signals are equal in width. The coincident termination of the CPUP and CPDN signals can be seen in Figure 22.

When necessary, the operation of the CPD can also be frozen so it will not respond to any input stimuli. The PLL utilizes two phase detectors. When switching between the Quadrature Phase Detector (QPD) and the Coincident Phase Detector (CPD), the operation of both phase detectors is suspended to eliminate the possibility of passing erroneous signals to the Charge Pump. The operation of the CPD is suspended by asserting the CCST input. When CCST is a logic 1, shown in Figure 21, the F5DH FFs are held in a reset condition and the output signals are held low.

The CPD is used to lock the PLL to the REFOSC signal which has a maximum frequency of 96 MHz. Simulations were performed for a REFOSC frequency of 50 MHz at 120 degrees Celsius on the slow and the fast process files. The two signals have the same frequency, but have phase differences of 162 and 18 degrees. A summary of the simulation results are listed in Table 8. The maximum speed of operation of the CPD for each case is shown in Table 9.

Process File	Phase Dif (dg)	Pass or Fail	Simulation Figures
Slow	162	Fail	23,24
Slow	18	Pass	25,26,27
Fast	162	Pass	28,29
Fast	18	Pass	30,31,32

CPD Pass/Fail Results

Table 8

Process File	Phase Dif (dg)	Maximum Operation (MHz)
Slow	162	45.5
Slow	18	66.7
Fast	162	66.7
Fast	18	125.0

CPD Maximum Speed Results

Table 9

The simulations results on the slow file with 162 degree phase difference is shown in Figure 23. The CPD does not

operate properly. The CPUP and CPDN signals respond properly to the first REFOSC and DSP signals; the pump-up is wider than the pump-down pulse. The error occurs one the rising edge of the second REFOSC pulse. The CPUP signal should go high with the second REFOSC pulse, but it does not. CPDN goes high with the second DSP pulse and stays high until the third REFOSC pulse. The CPUP signal finally goes high with the third REFOSC pulse and then both CPUP AND CPDN go low. As a result of the error, the second CPDN pulse is wider than the second CPUP pulse and therefore, the VCO is told to slow down instead of speeding up like it should.

The source of the error can be seen in Figure 24. The ROUT signal drives the reset input of the F5DH FFs. The problem occurs because the reset is still active when the rising edge of the second REFOSC pulse occurs. Since the reset is still a logic high, the FF does not detect the second REFOSC pulse. For proper operation, the propagation delays associated with ROUT must be reduced or the phase difference between REFOSC and DSP must kept small.

Specifying that the CPD will work for a limited range of phase differences only limits its usefulness, but it does work correctly. When the phase difference is

lowered to 18 degrees, the CPD will work on the slow process file. Correct operation of the CPD with an 18 degree phase difference is shown in Figure 25. The close-up view in Figure 26 displays that correct operation is possible because the ROUT signal is able to reset CPUP and CPDN long before the next REFOSC pulse occurs. The ROUT signal is explicitly shown in Figure 27. There are approximately 7 ns between the fall of ROUT and the rising edge of the subsequent REFOSC signal.

The circuit does not fail when the fast process file is used to simulate because the propagation delays are smaller than those of the slow file. Correct operation of the CPD with 162 phase difference is shown in Figure 28. Note that there is a CPUP pulse corresponding to every rising edge of REFOSC. The ROUT signal is explicitly shown in Figure 29a; it is low before REFOSC even begins to rise. The magnified view in Figure 29b shows that the ROUT signal is low 5 ns before the rising edge of REFOSC. Therefore, the period of REFOSC and DSP could be made 5 ns shorter giving the circuit a maximum operating frequency of 66.7 MHz.

Since the CPD worked properly on the fast process file with a phase difference of 162 degrees, it seems

reasonable that it should work with a phase difference of 18 degrees as shown in Figure 30. The close-up view found in Figure 31 shows that the time, t_{d1}, between the resetting of CPUP and CPDN and the next REFOSC pulse is approximately 14ns which is a large percentage of the 20ns cycle time. The ROUT signal is shown in Figure 32. The time, t_{d2} between the fall of ROUT and the next REFOSC pulse is about 12ns. If the cycle time were decreased until ROUT fell just before the REFOSC signal rose, the estimated maximum operating frequency with a phase difference of 18 degrees would be 125 MHz.

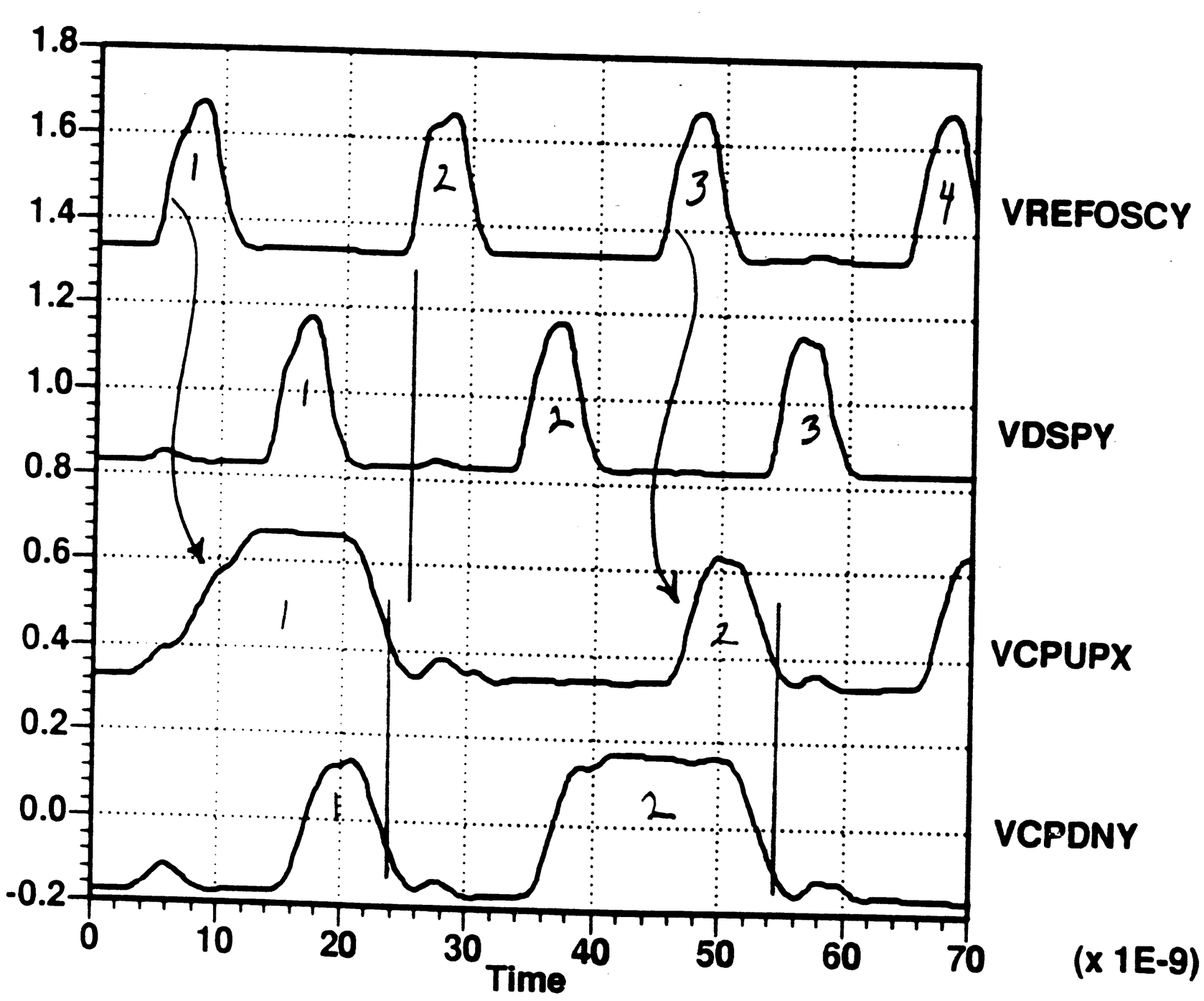
The Figures 23 through 32 show that the CPD will work at 96 MHz only on the fast file and with a maximum phase error of about 118 degrees (extrapolated from Figure 32). In order to meet the data separator specification, The CPD circuit will have to operate at 96 MHz and be able to cope with a maximum phase error of approximately 310 degrees.

For correct operation the ROUT signal must not be asserted when subsequent REFOSC pulses occur. At 96 MHz, the REFOSC signal would have a rising edge every 10.4 ns. If the maximum phase error is set at 311 degrees, the DSP pulse would occur 9 ns after the REFOSC pulse. Therefore, there is only 1.4 ns between the rising edge

of DSP and the rising edge of the subsequent REFOSC pulse. Correct operation requires that the ROUT signal be activated by the DSP rising edge and deactivated by resetting the F5DH FFs all in 1.4ns.

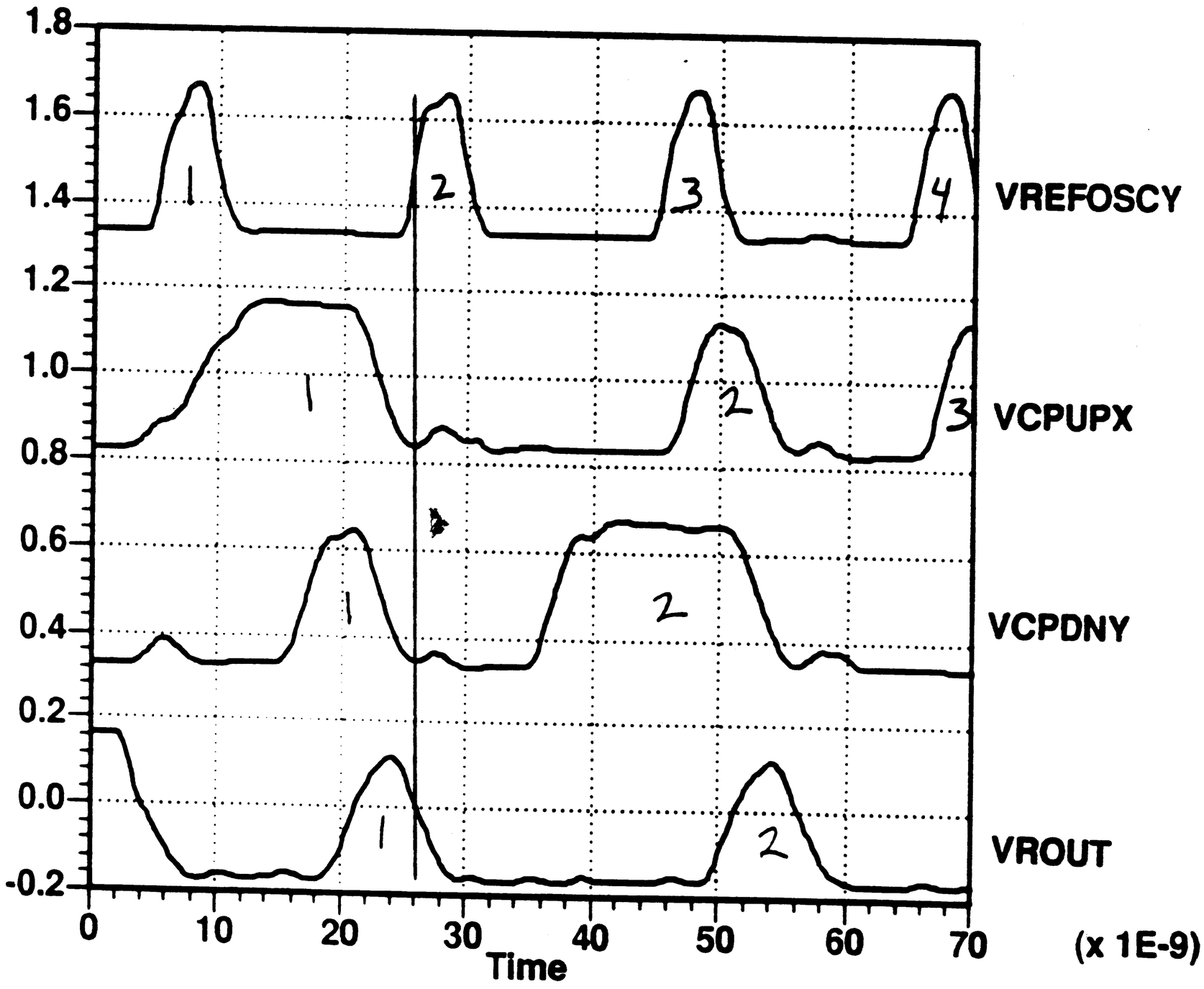
Figures 29 and 32 show that even when the fast file is used, it takes 7ns from the rising edge of DSP to the point where ROUT is a logic low. Making it all happen in 1.4 ns is clearly impossible with the present gates.

The fact that the logic gates are not fast enough for the CPD does not mean that its performance is not high enough for the rest of the data separator. The CPD is a special case where the logic is configured in such a way that a 100 MHz gate is not fast enough; however, 100 MHz is fast enough for the counters, decoders and other logic circuits. There are two approaches to making the CPD work properly. Either faster gates may be developed or a new architecture may be used.



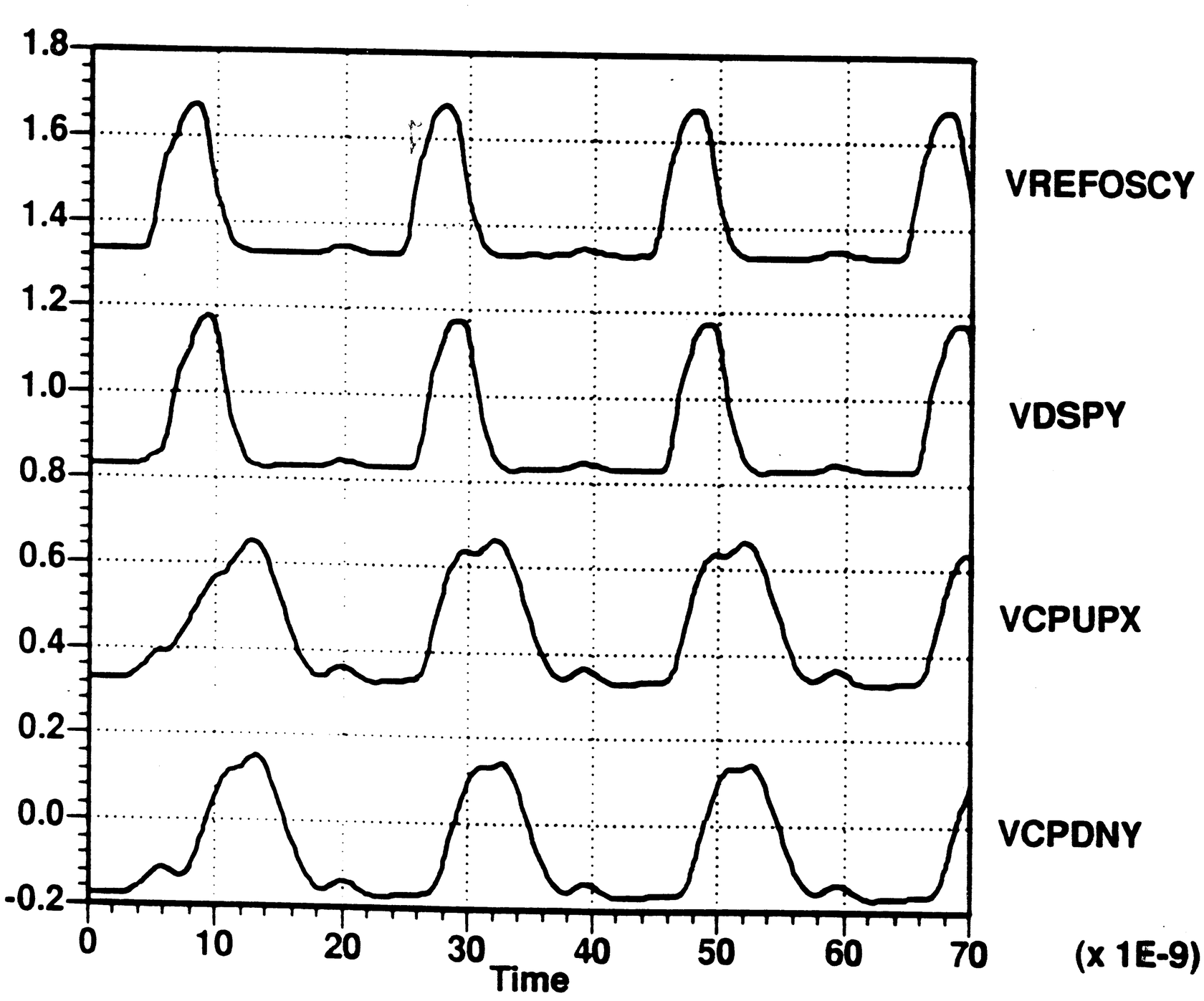
Slow File, 162 Degree Difference

Figure 23



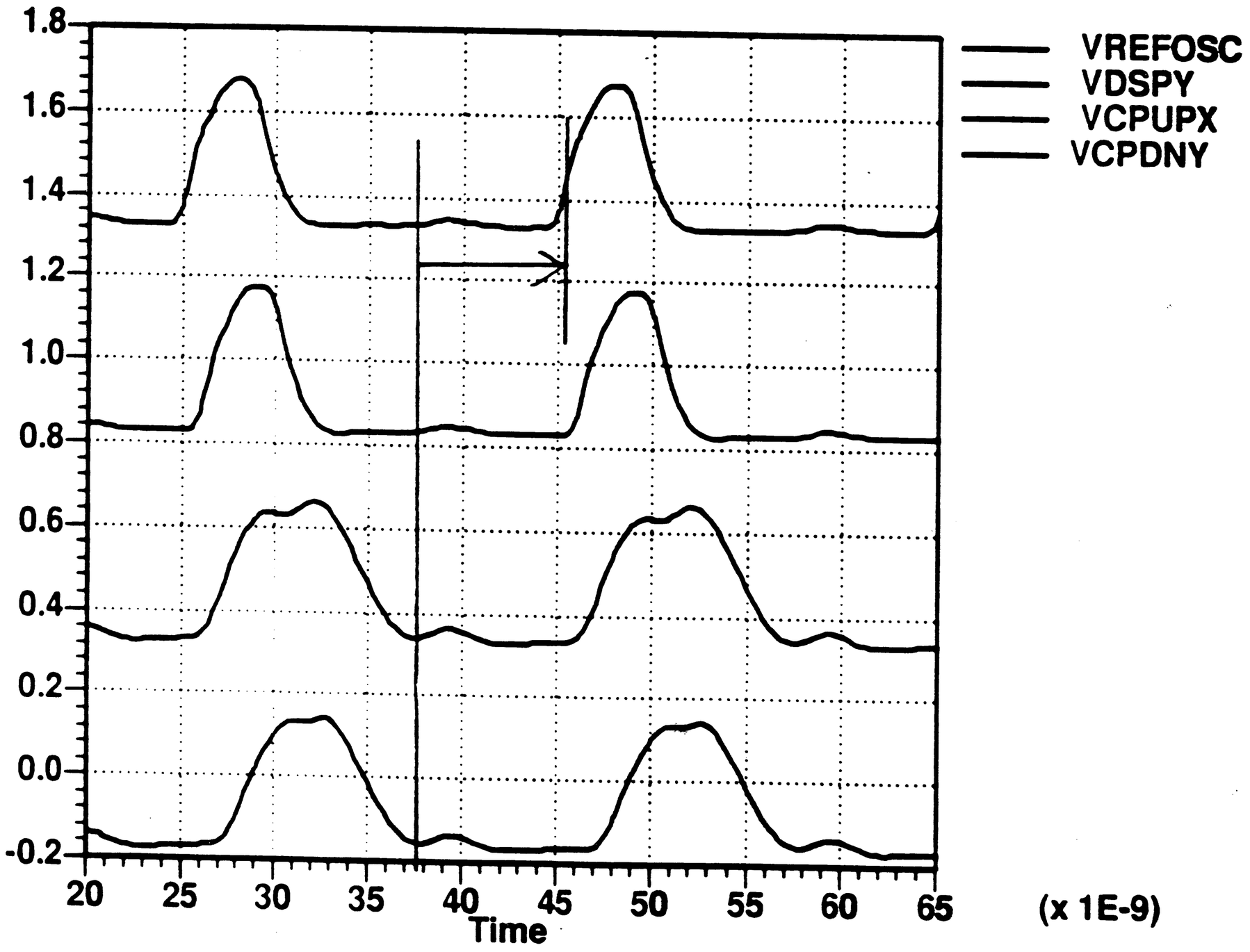
Slow File, 162 Degree Difference
with ROUT

Figure 24



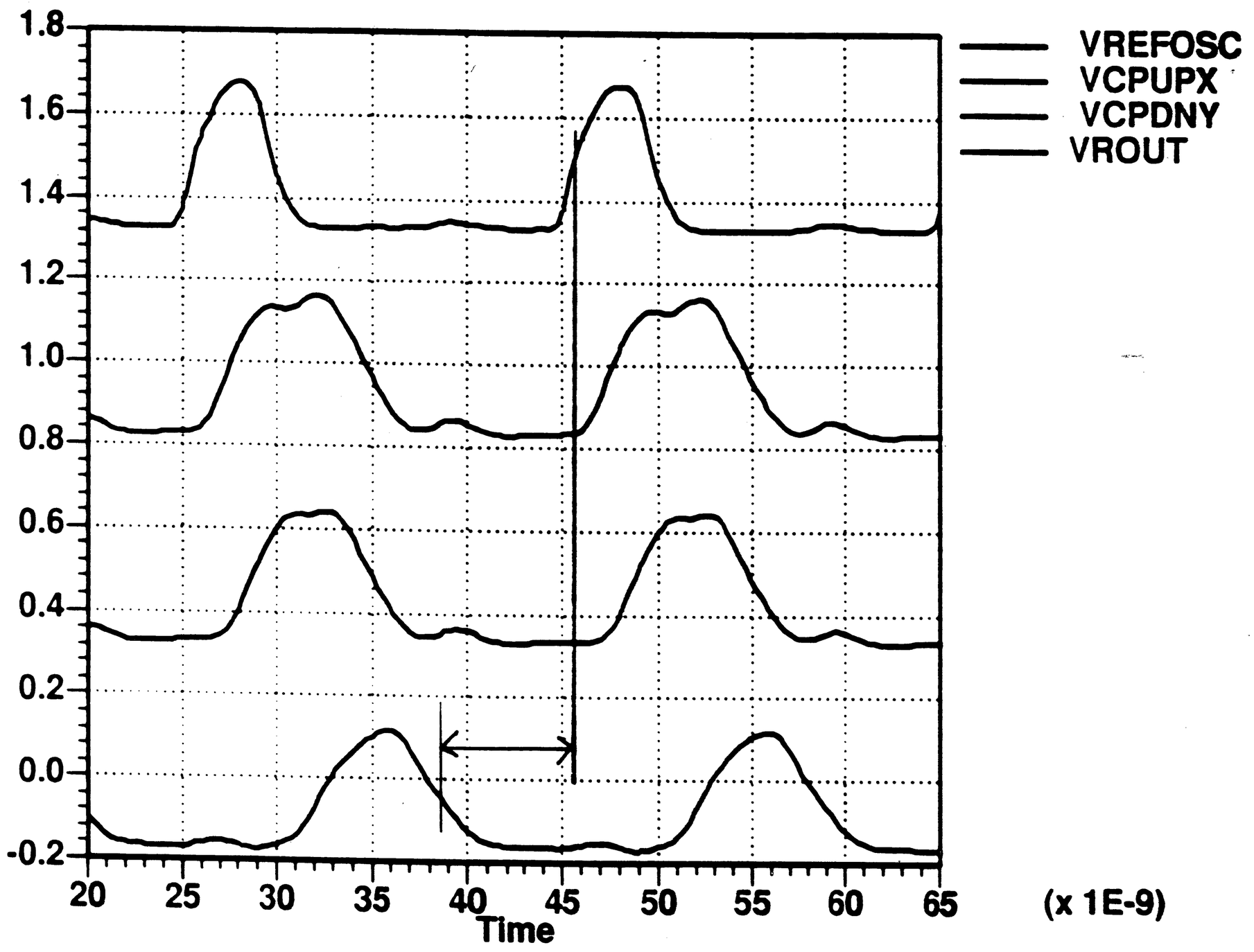
Slow File, 18 Degree Difference

Figure 25



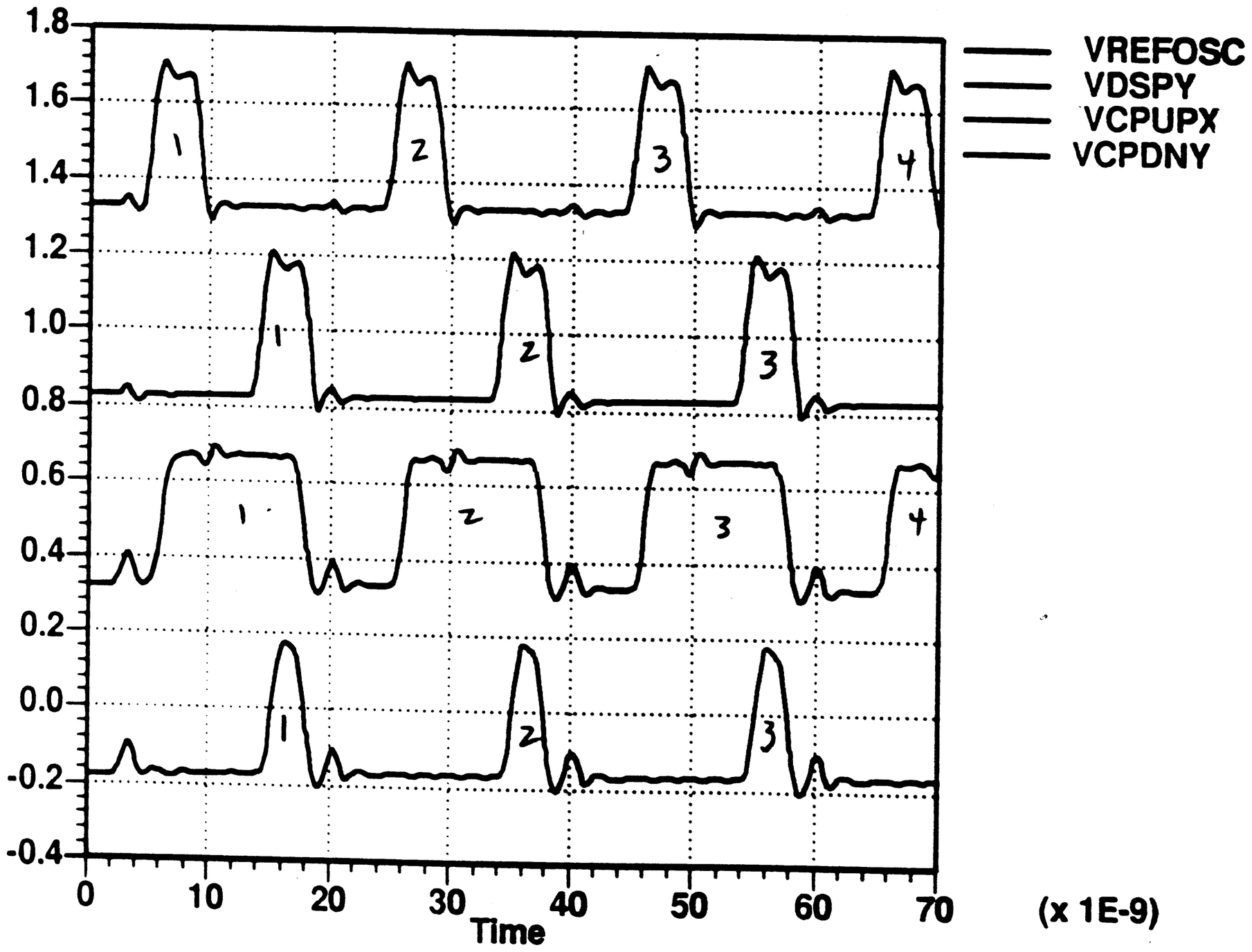
Slow File, 18 Degree Difference
(magnified)

Figure 26



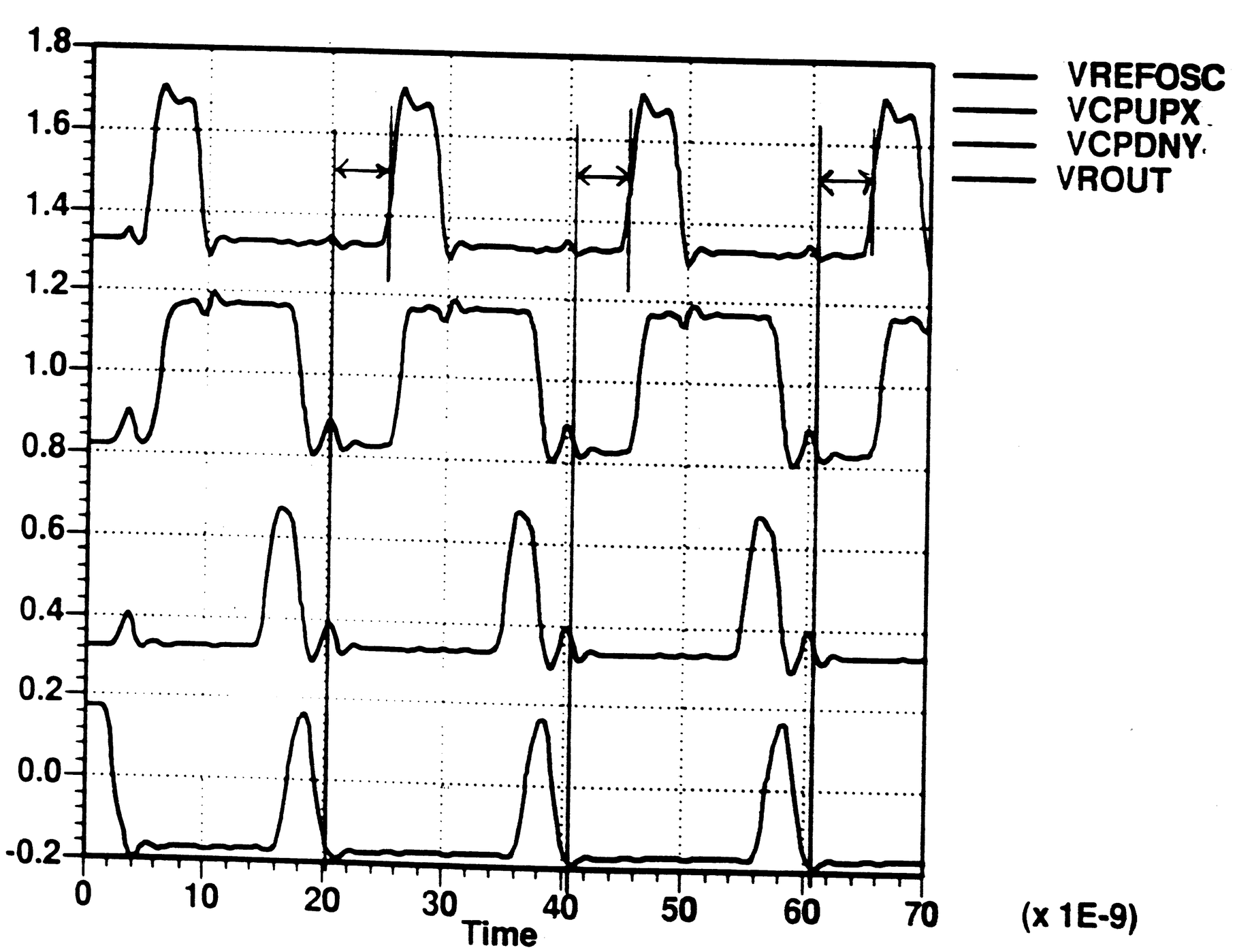
Slow File, 18 Degree Difference
with ROUT

Figure 27



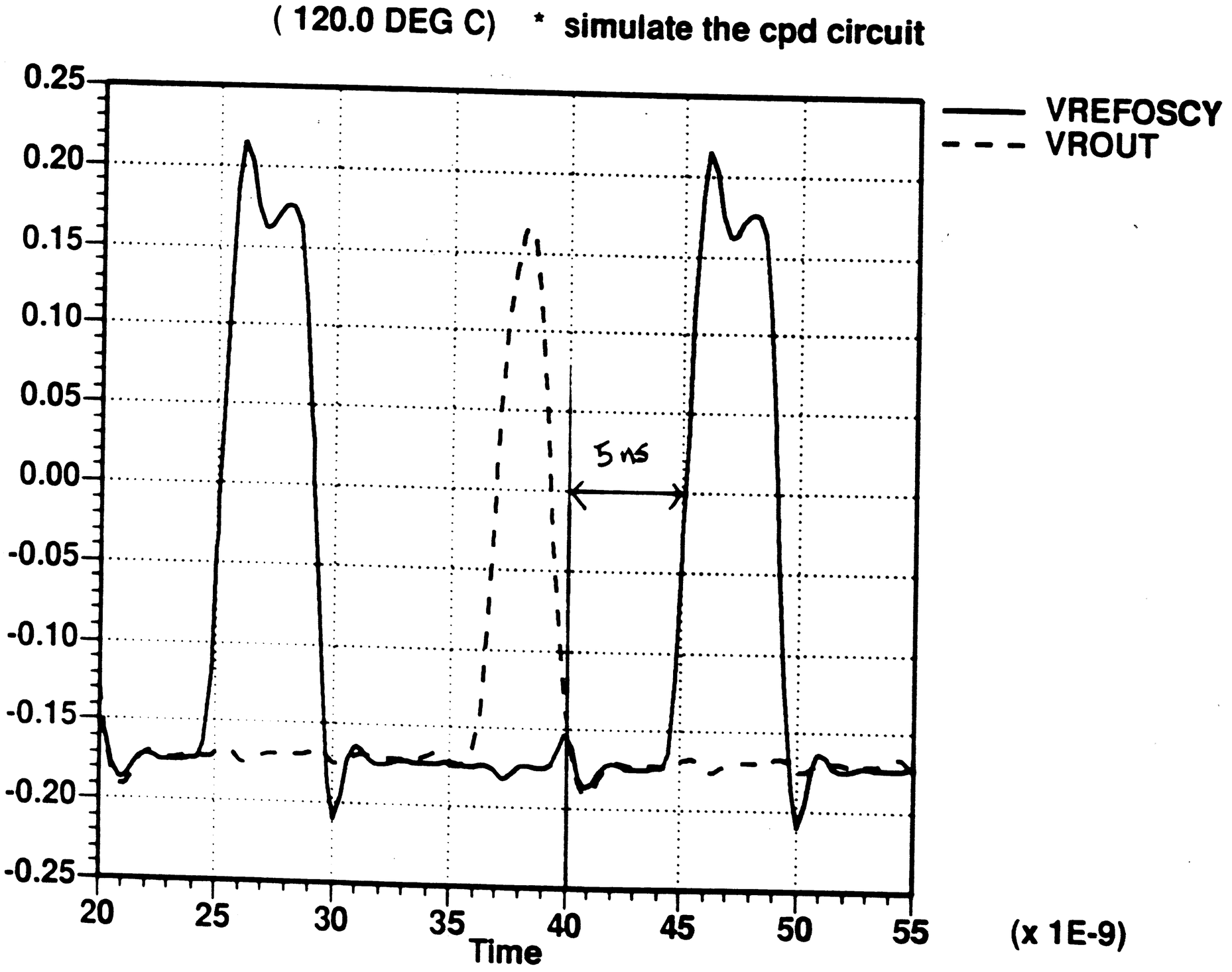
Fast File, 162 Degree Difference

Figure 28



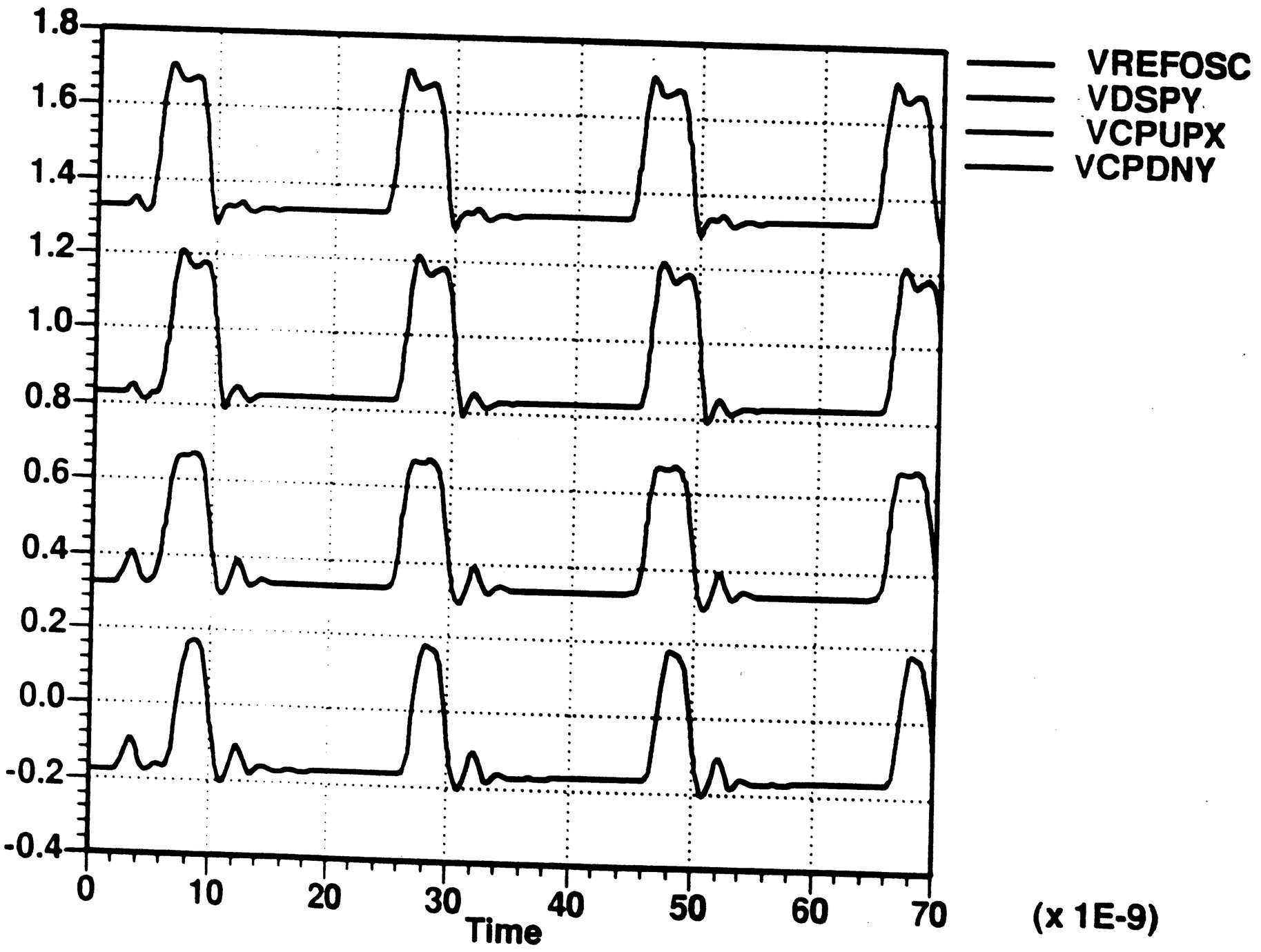
Fast File, 162 Degree Difference
with ROUT

Figure 29a



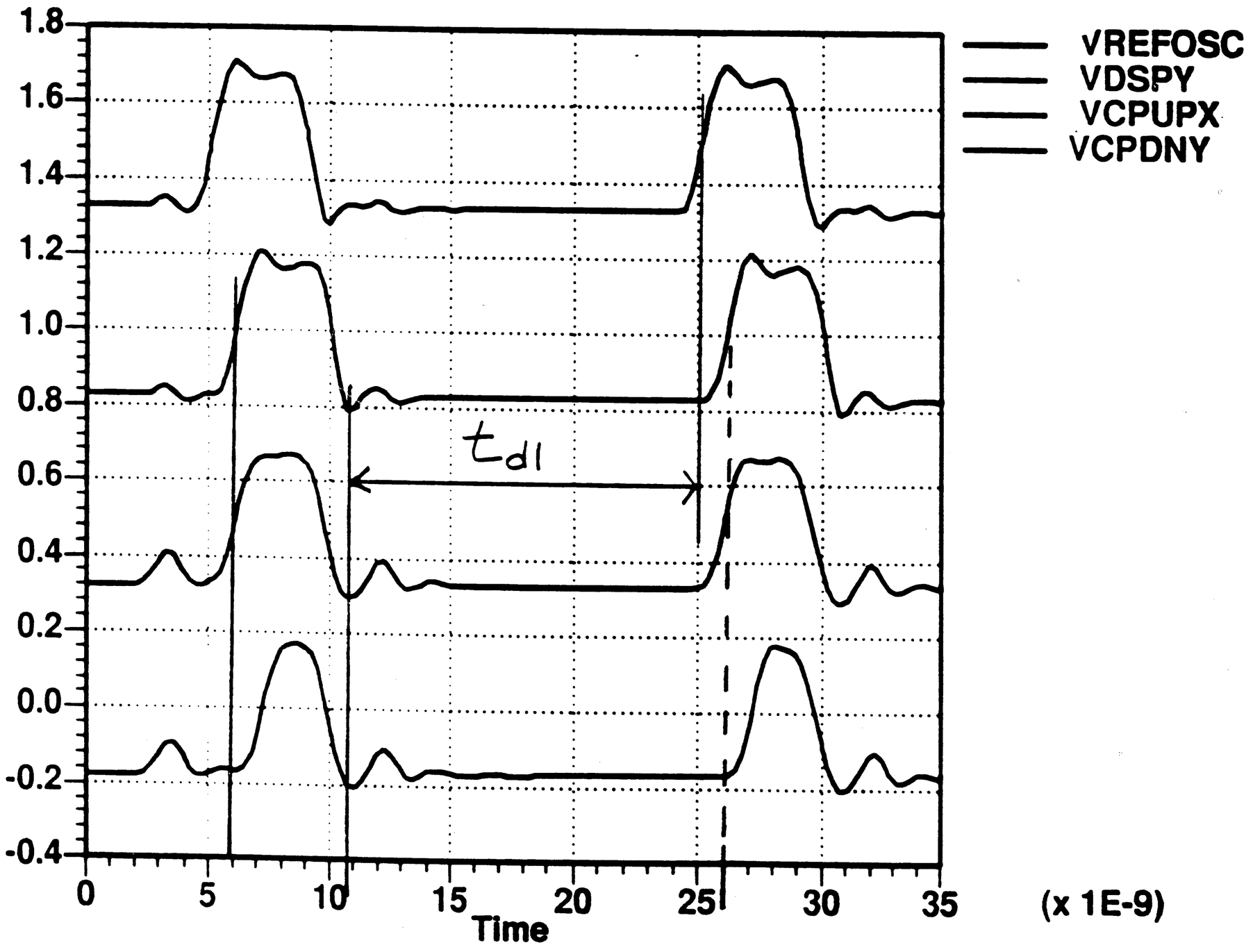
Fast File, 162 Degree Difference
with ROUT

Figure 29b



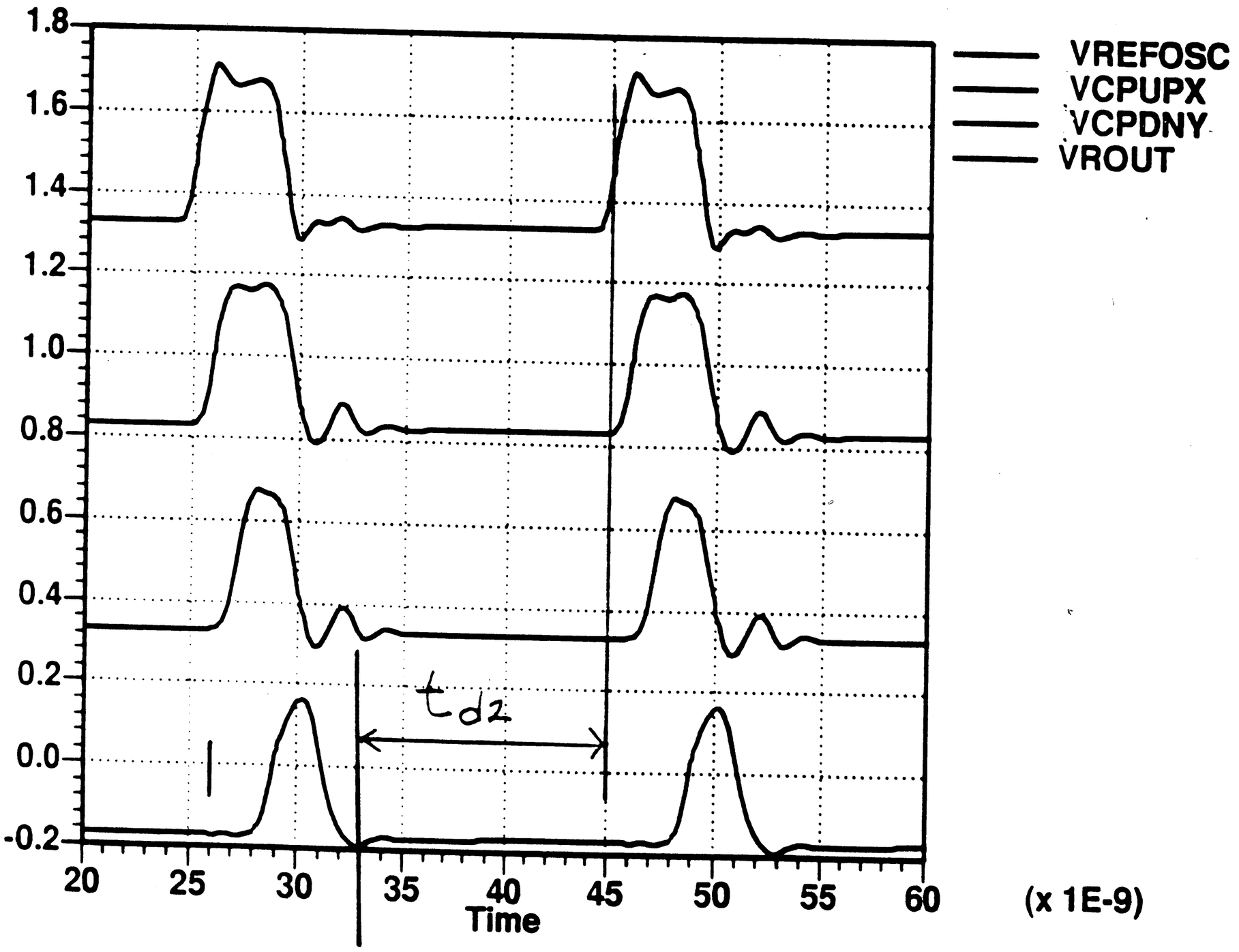
Fast File, 18 Degree Difference

Figure 30



Fast File, 18 Degree Difference
(magnified)

Figure 31



Fast File, 18 Degree Difference
with ROUT

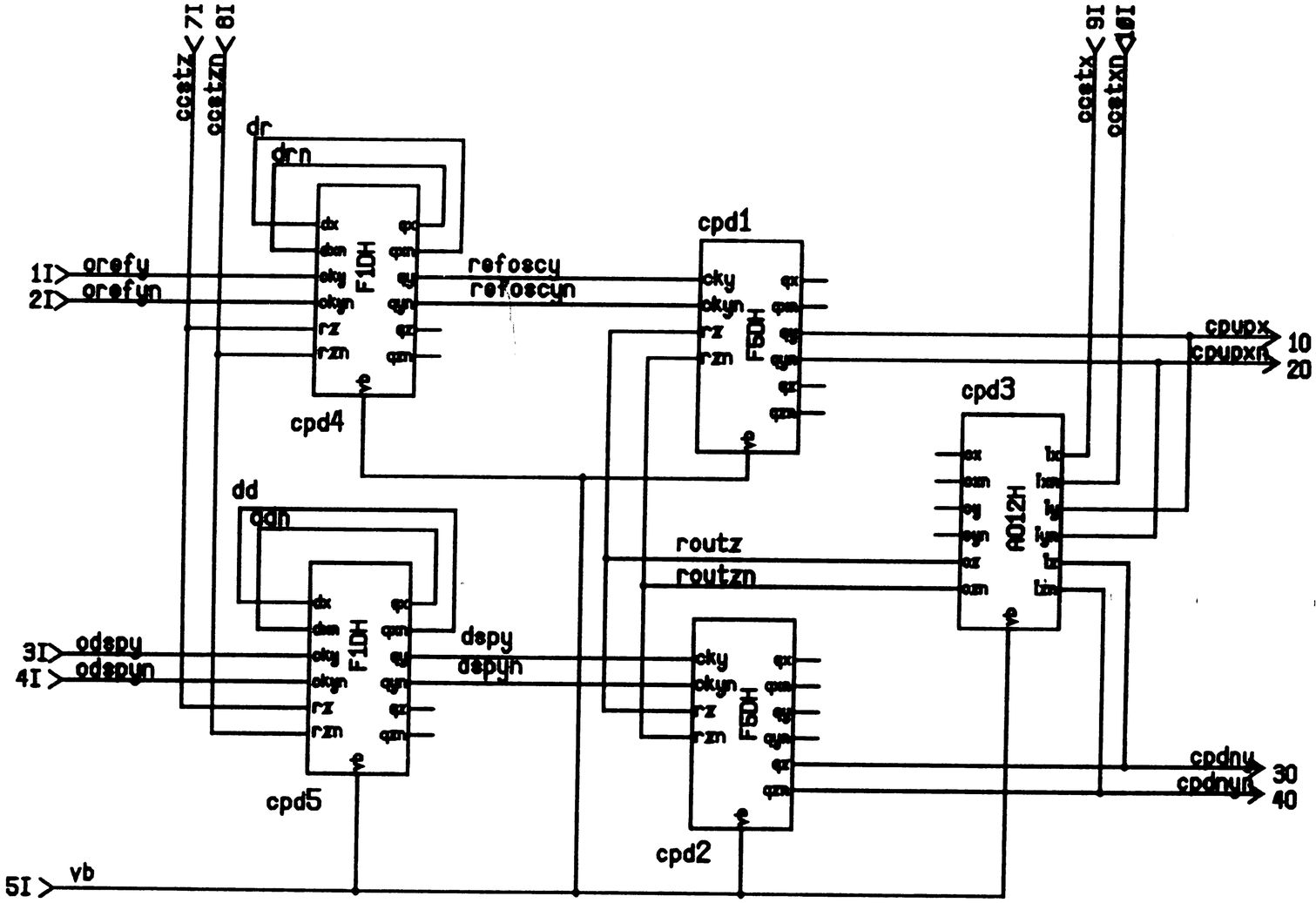
Figure 32

4.1.1 IMPROVEMENT VIA NEW ARCHITECTURE

The data of Table 9 shows that the original CPD architecture operates correctly up to 45.5 MHz on the slow file with a phase error of 162 degrees. If the AND2 and OR2 gates shown in Figure 21 are combined, the original architecture operates at 48 MHz. The REFOSC and DSP signals operate at a maximum frequency of 96 MHz. If they are divided by 2, the CPD would have to work at a rate of 48 MHz instead of 96 MHz.

Indeed, the new architecture is an implementation of the above suggestions. Both the REFOSC and DSP inputs are divided by 2 before they enter the phase detector circuit that has the combined gate. The combination of the AND2 and OR2 gates is called the AO12H; the boolean equation for the gate would be (CPUP*CPDN)+CCST. Refer to Figure 33. The simulated results of the new architecture can be seen in Figures 34 through 39.

The signals shown in Figure 34 are the divided inputs, REFOSC and DSP, and the pump-up and pump-down signals, CPUP and CPDN. It demonstrates that the new architecture does operate correctly at 96 MHz on the slow file at 120 degrees Celsius.



New CPD Architecture
Figure 33

A close-up, in Figure 35, shows the phase error to be 164 degrees. The undivided input signals at 96 MHz, Figure 36, have a phase difference of 311 degrees. The divided and undivided signals are shown in Figure 37 with a magnified view of the same in Figure 38. Dividing the signals decreases the maximum required operating frequency of the phase detector and also delivers a signal with a lower phase error than the original signals. The divided signals in relation to ROUT are shown in Figure 39. The ROUT signal goes low soon enough to not interfere with the rising edge of the REFOSC signal.

The same simulations were performed on the fast process file. The circuit performed successfully as expected. The divided signals and the pump-up and pump-down signals are shown in Figure 40. The ROUT signal is shown in Figure 41. It can be seen that ROUT falls to a logic 0 many nanoseconds before the next rising edge of REFOSC.

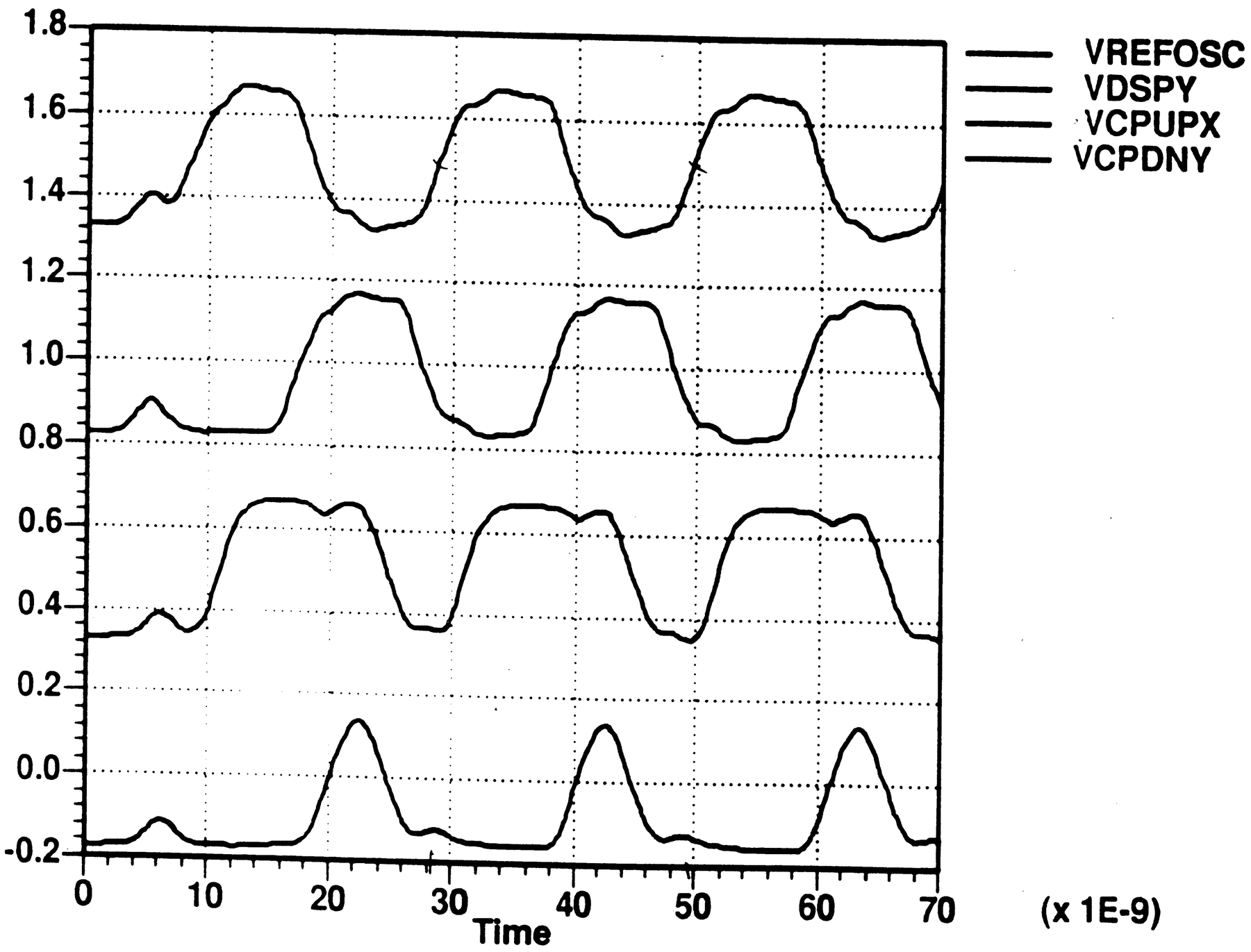
The power consumption and the area of the new architecture circuit are greater than that of the original architecture. The power consumption rose from 18.2 mW to 27.4 mW; a 50% increase. The area expanded from 272,800 to 420,000 square microns which is a 53%

increase. However, it will be seen, when compared to using faster gates, that the increases are minimal and necessary to get a working circuit.

One disadvantage of the new architecture is that only 1 out of 2 REFOSC and DSP edges are compared; therefore, the closed-loop gain of the PLL decreases. Any gain lost by dividing REFOSC and DSP must be regained by adjusting the gain of the Charge Pump. Increasing the gain of the Charge Pump by a factor of 2 to compensate is possible. As a result, dividing the input signals to the CPD will not pose a problem and the new architecture approach represents a viable solution.

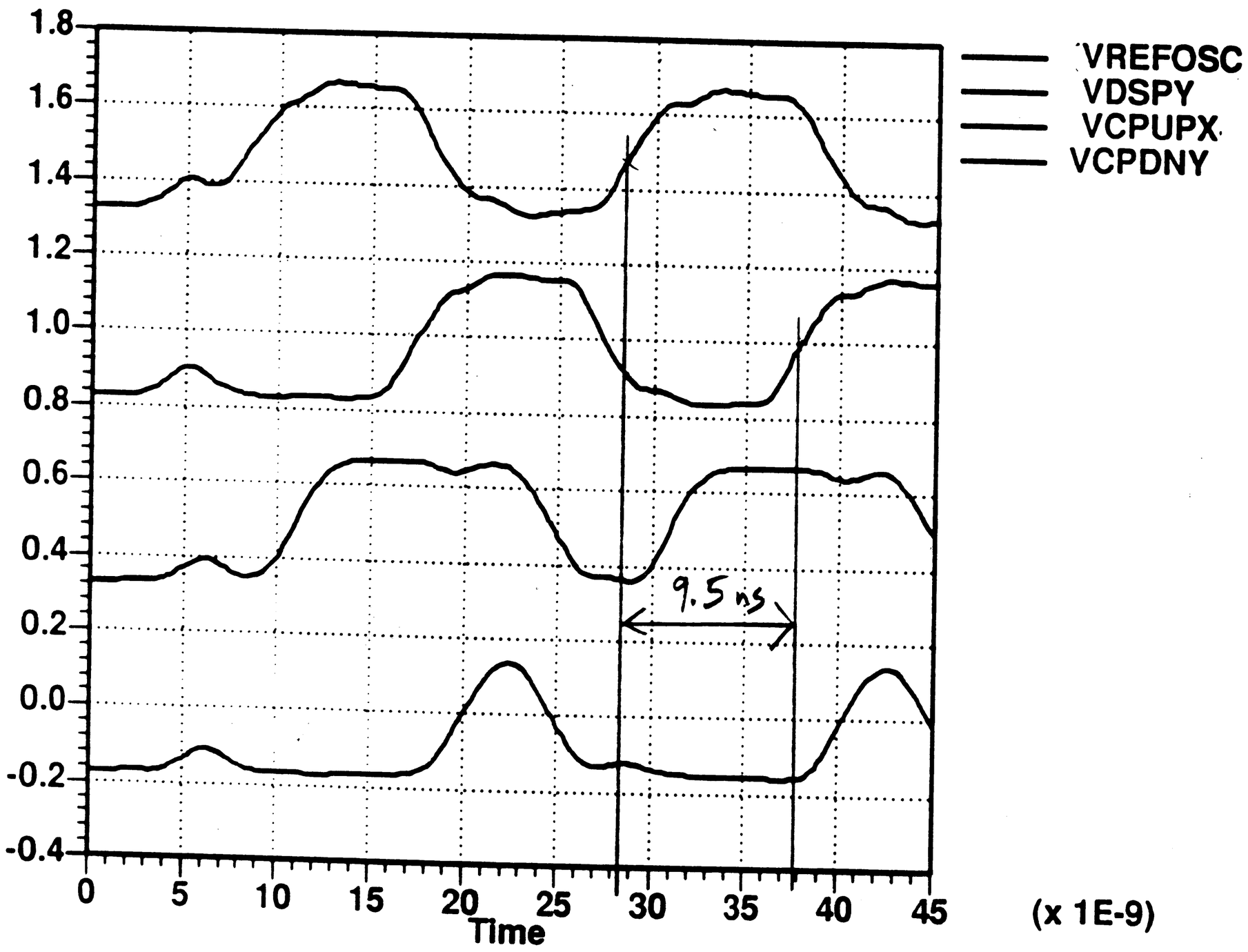
4.1.2 IMPROVEMENT VIA FASTER GATES

The second approach to meeting the speed requirements of the system is to just make the original architecture work faster. Increasing the speed of a gate can be accomplished by increasing the current in the current sources, which means the power used by the gate is increased. The first simulations of the original architecture used the 'H' gates; the nominal value of the current source, I_t, was 340 uA. The gate current was increase to 500 uA and tested in the original architecture.



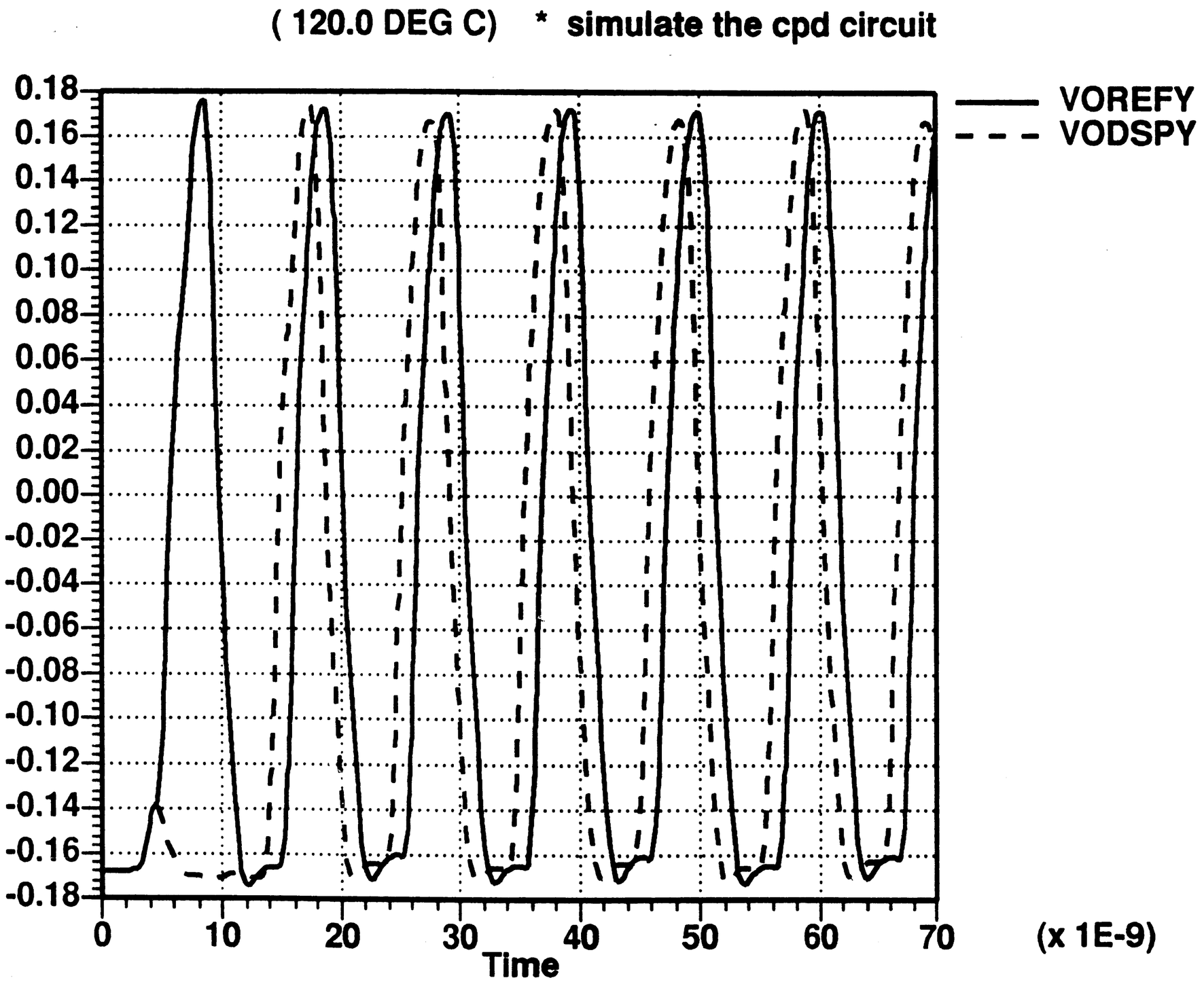
Slow File, New CPD Architecture
96 MHz, 311 Degree Difference

Figure 34



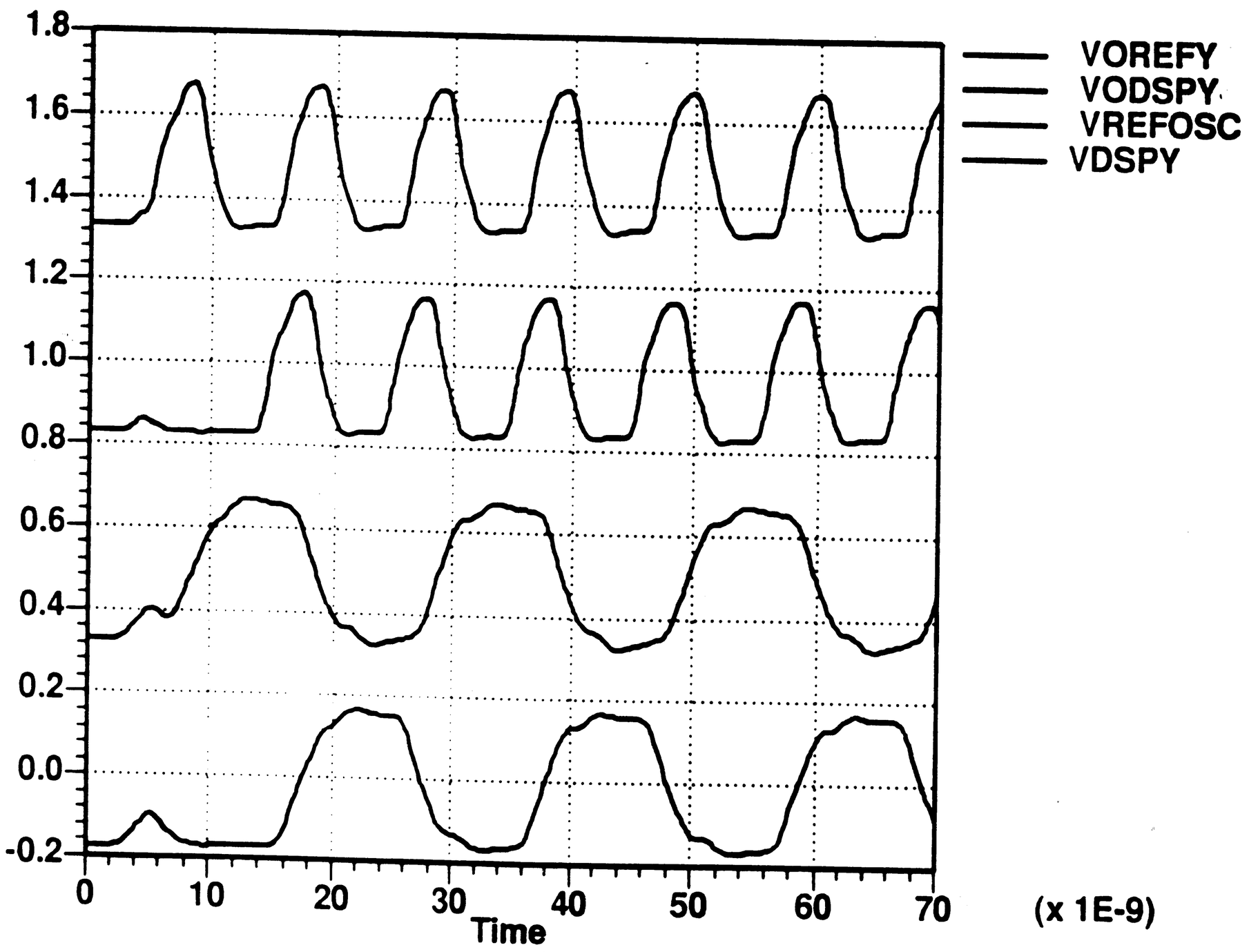
Slow File, New CPD Architecture
96 MHz, 311 Degree Difference
(magnified)

Figure 35



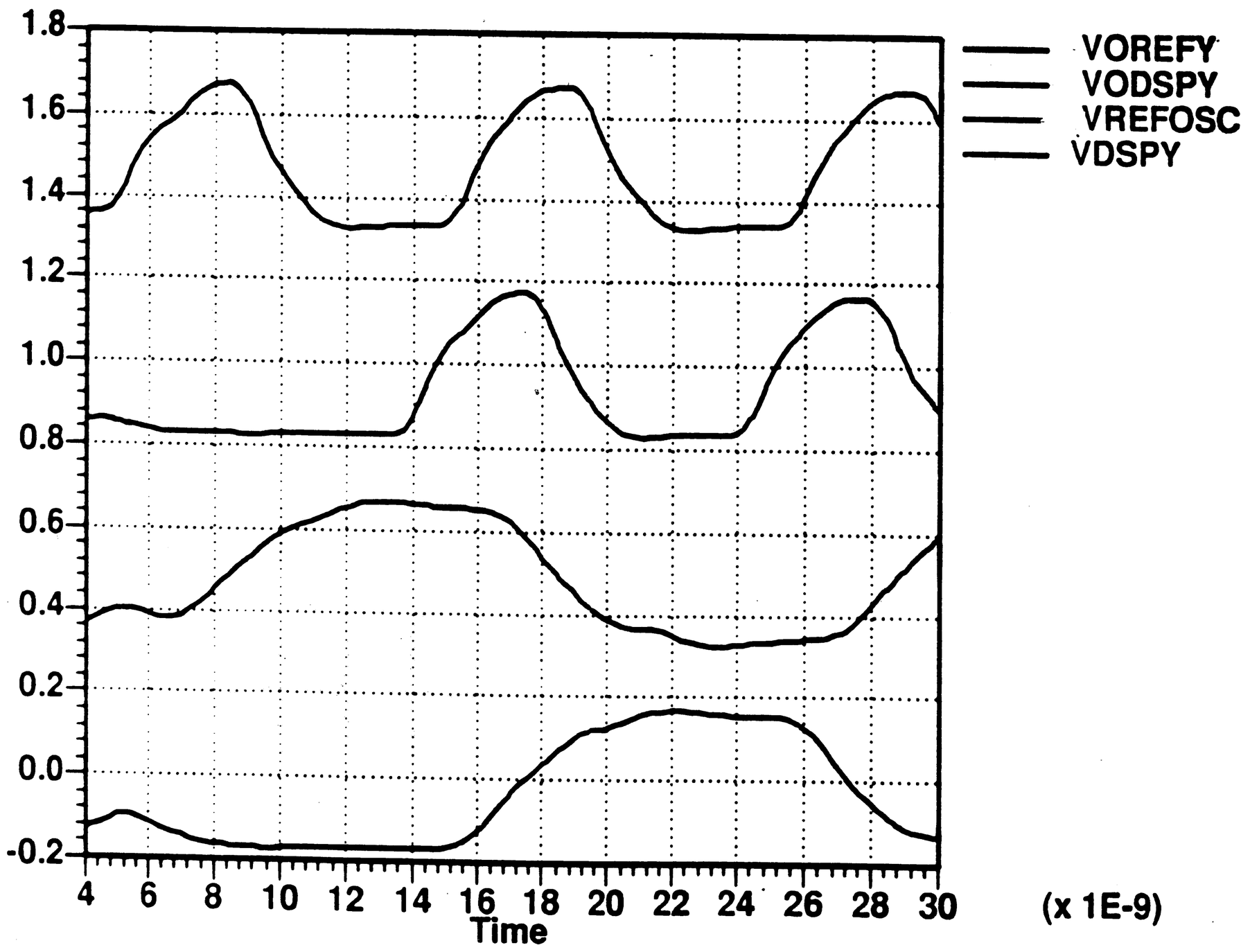
Slow File, New CPD Architecture, Input Signals
96 MHz, 311 Degree Difference

Figure 36



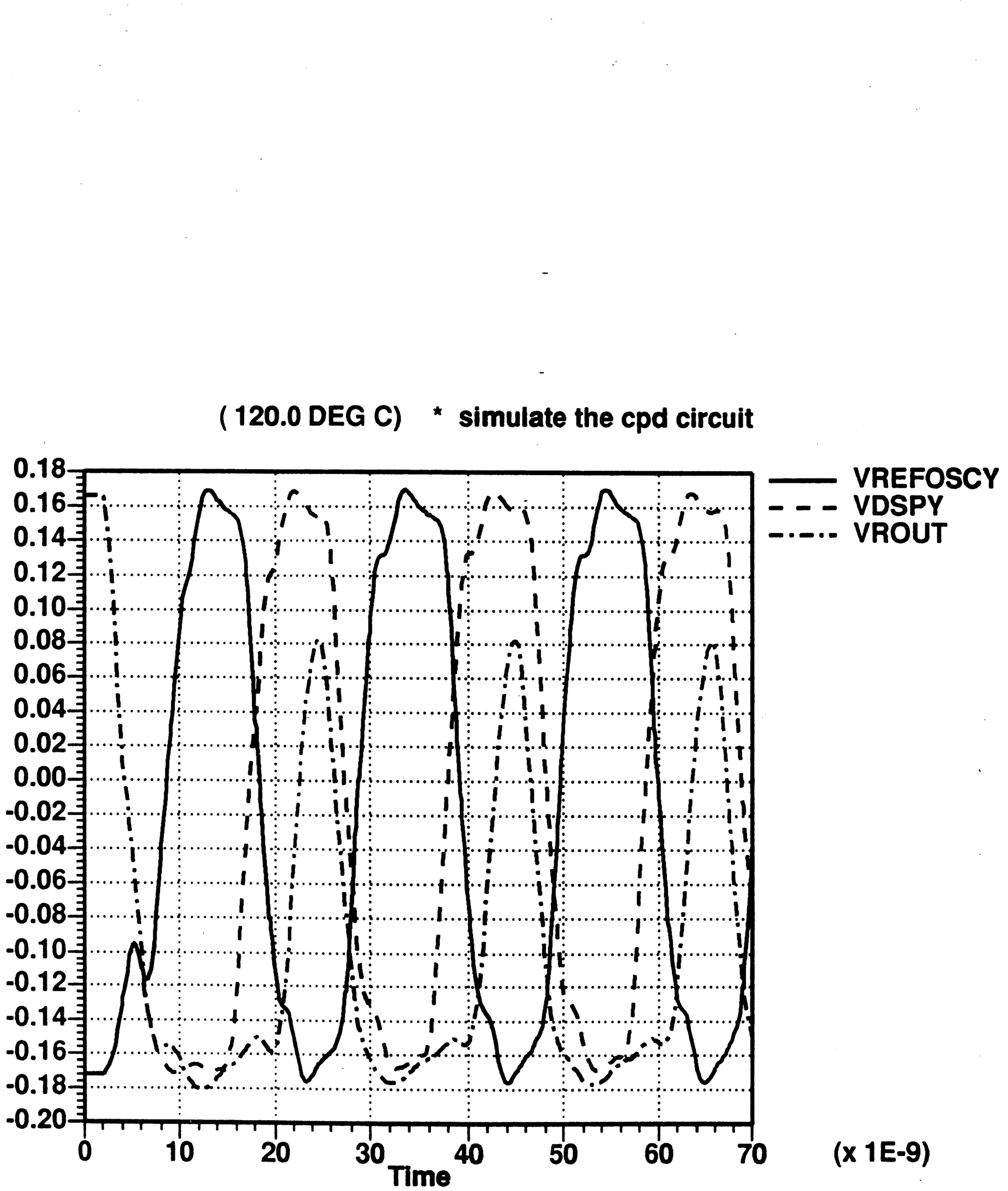
Slow File, New CPD Architecture
Divided and Undivided Signals
96 MHz, 311 Degree Difference

Figure 37



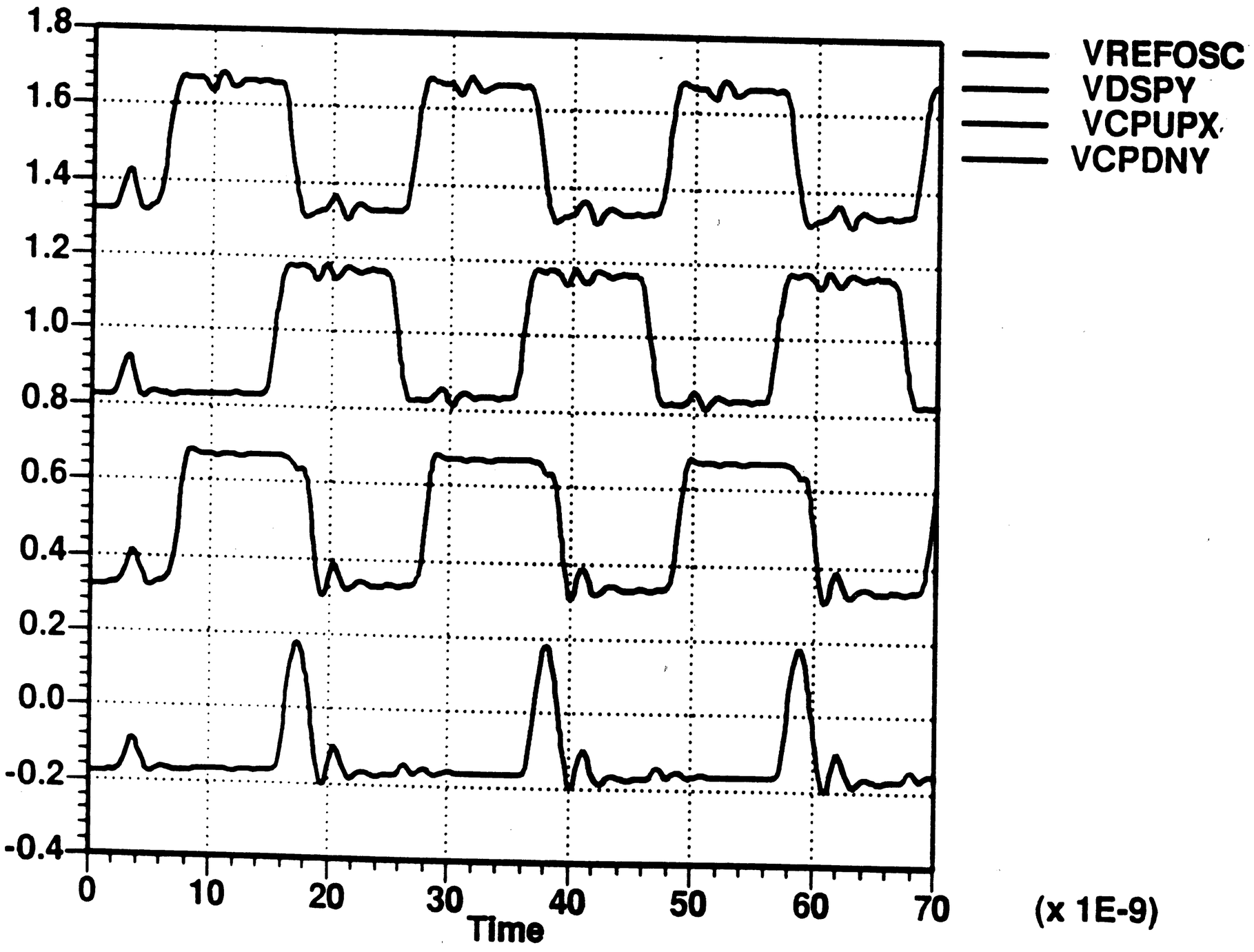
Slow File, New CPD Architecture
Divided and Undivided Signals
96 MHz, 311 Degree Difference
(magnified)

Figure 38



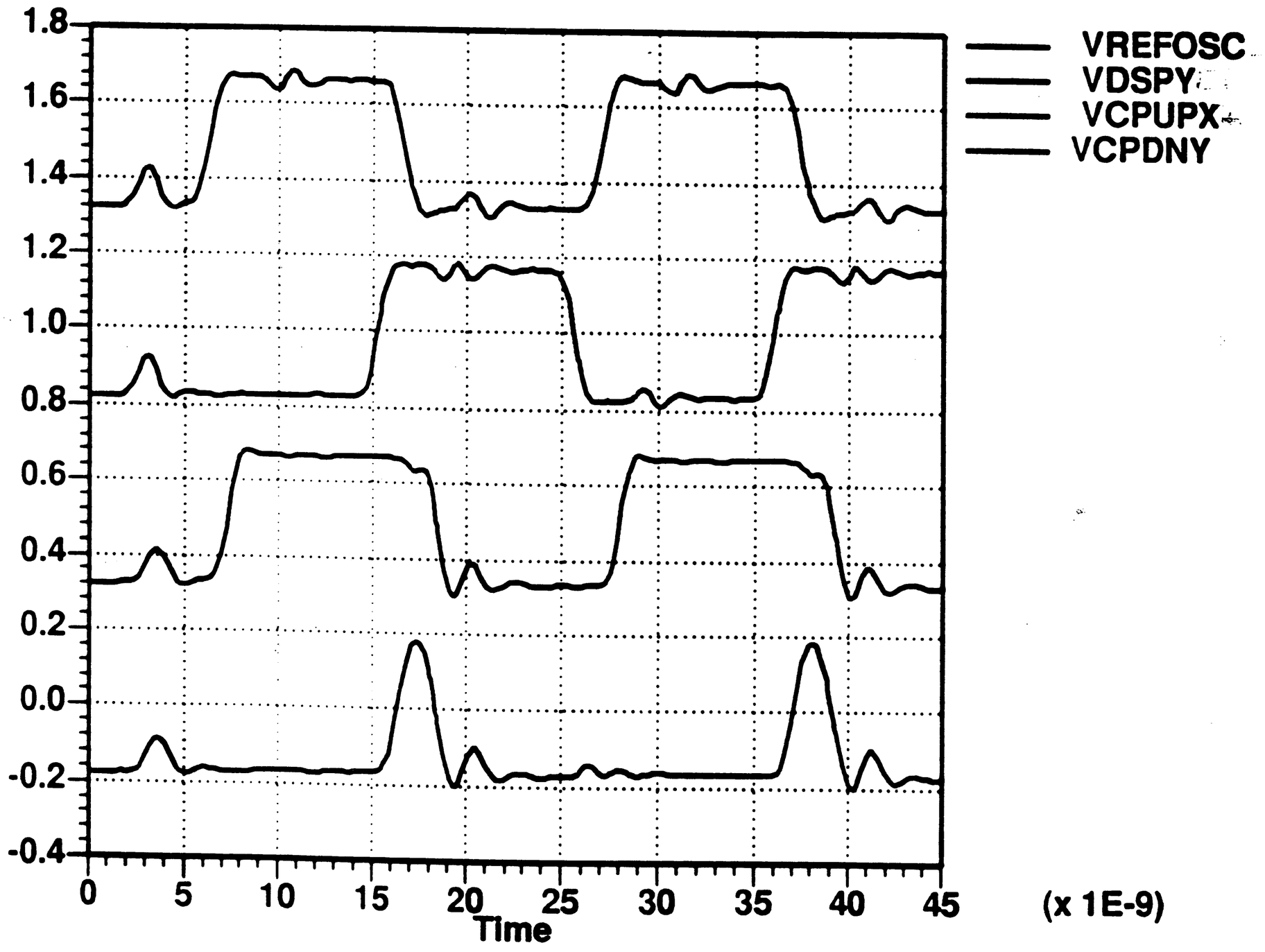
Slow File, New CPD Architecture
Divided Signals with ROUT
96 MHz, 311 Degree Difference

Figure 39



Fast File, New CPD Architecture
96 MHz, 311 Degree Difference

Figure 40



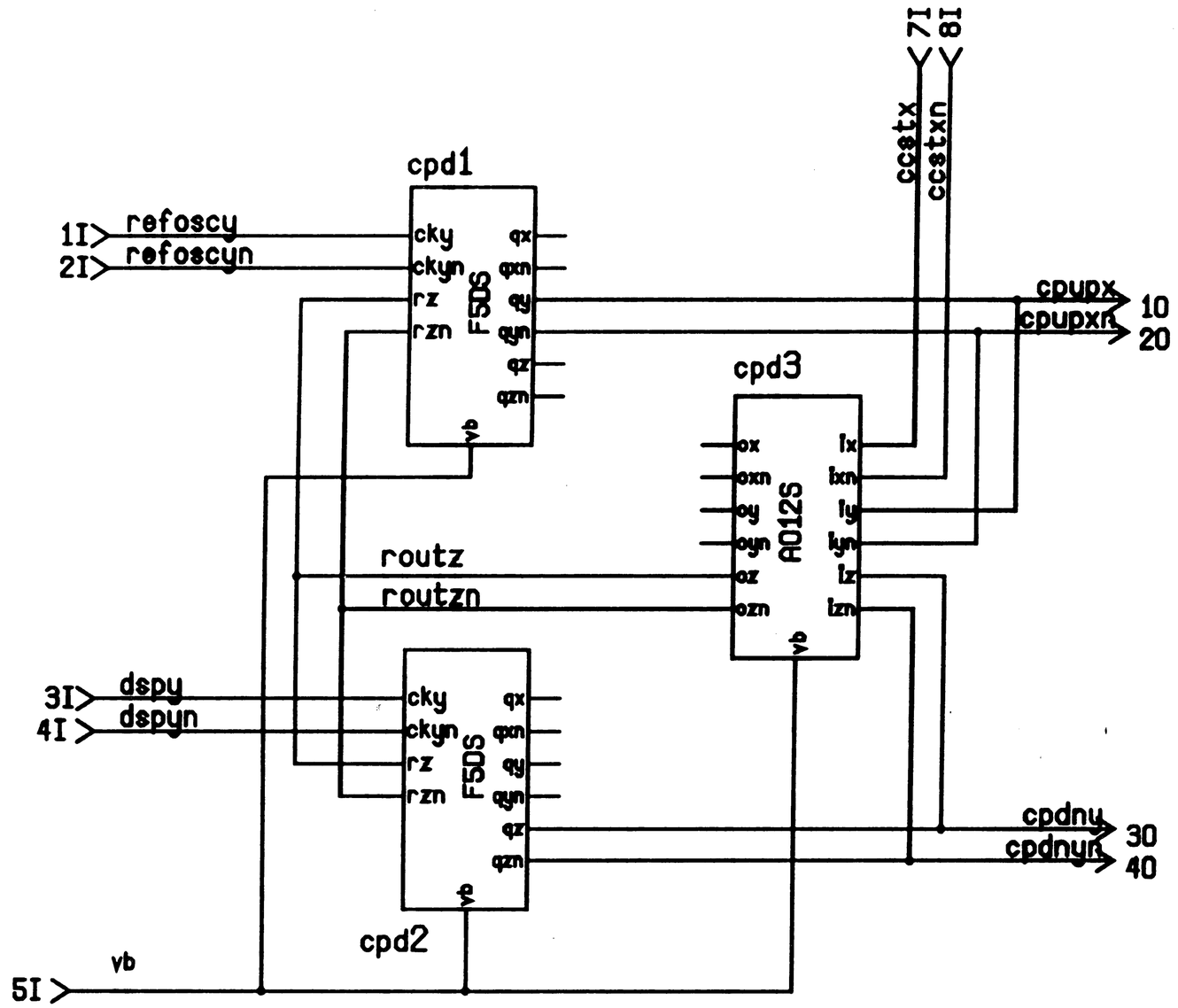
Fast File, New CPD Architecture
96 MHz, 311 Degree Difference
with ROUT

Figure 41

The high powered gates were not layed out and the simulations were performed without extracted parasitic capacitances; therefore, the actual results will not be a good as the simulated results.

The high speed CPD,in Figure 42, is the same as the original CPD except it uses higher power gates, labeled F5DS and AO12S. In addition, the original AND and OR gates have been combined into a single AO12S gate. The gates are the same as the original gates except the value of the load resistors have been decreased and the current has been increased from 340 uA to 500 uA.

Simulations using the slow process file showed that the circuit does not function at 96 MHz; however, it did operate correctly at 80 MHz. A plot of the signals at 80 MHz are shown in Figures 43 and 44. It must be remembered that the parasitic capacitances of the gate were not modeled; therefore, 80 MHz operation represents a theoretical maximum that will not be achievable in real life. Once more it can be seen, in Figure 44, that the ROUT signal goes low just in time to not interfere with the rising edge of REFOSC. The area of the CPD with the 500 uA gates is estimated to be 322,000 square microns, 18% larger than the original circuit and consumes 31.9 mW.

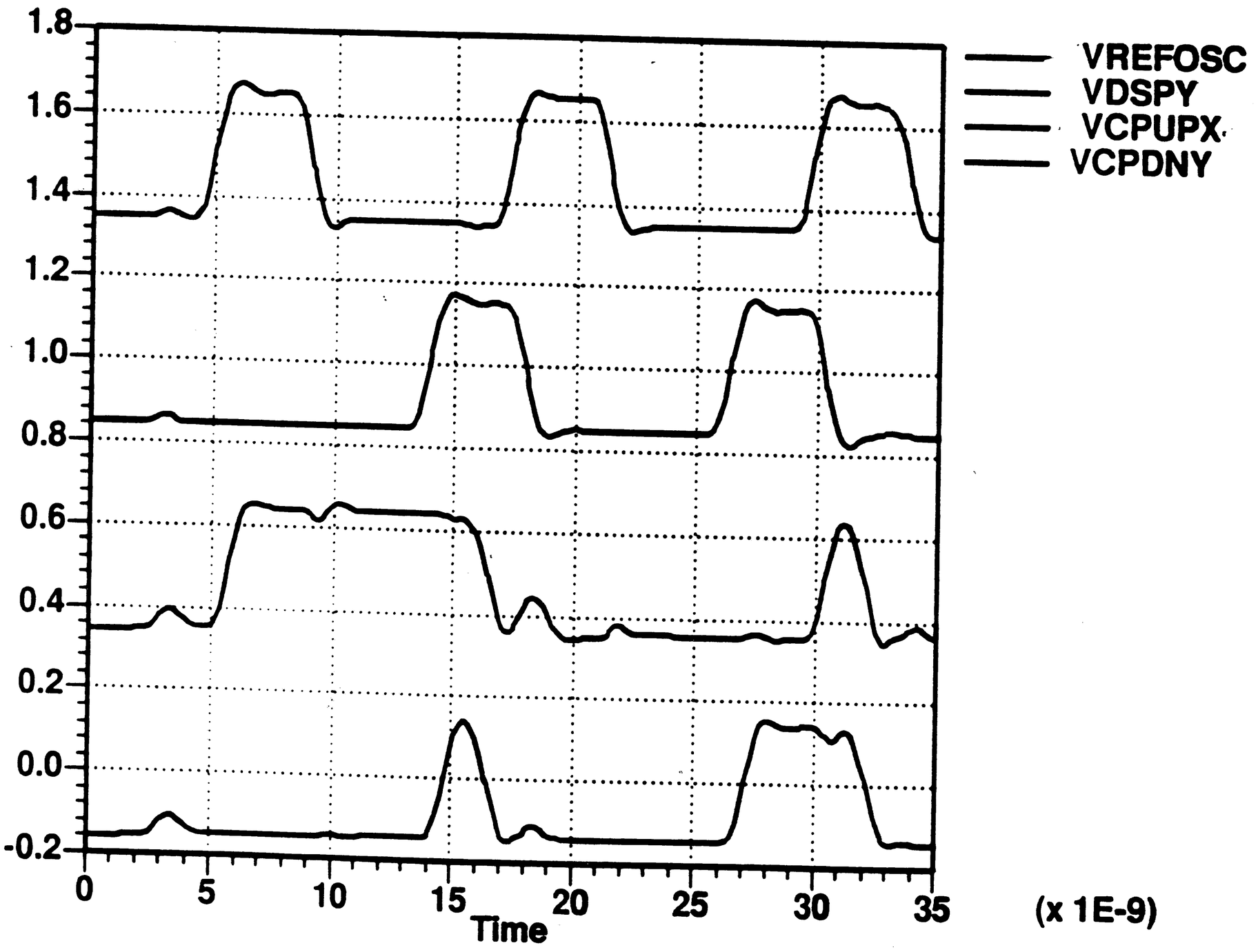


High Speed CPD

Figure 42

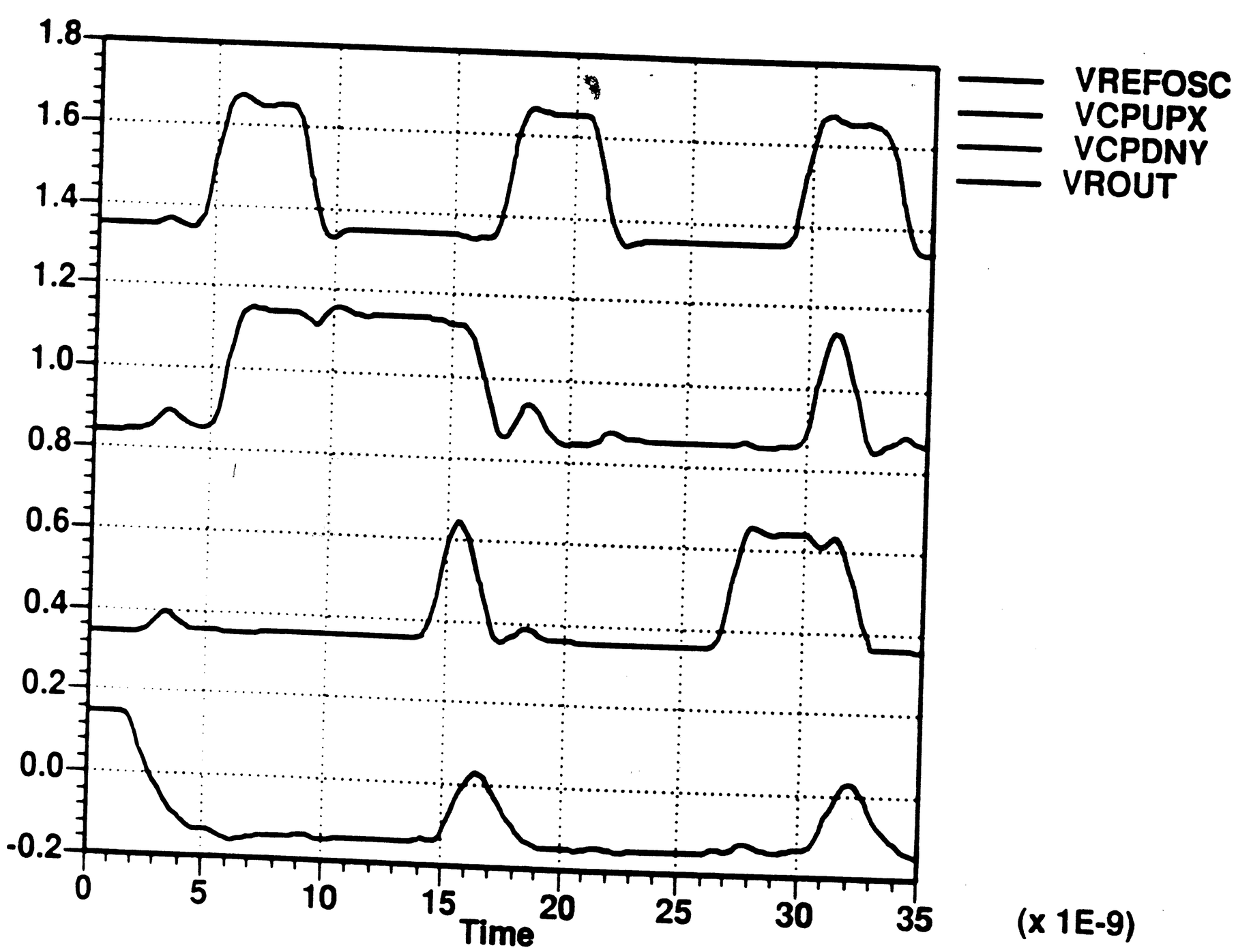
In an attempt to boost the speed to 96 MHz, the current, I_t, in the gates was increased to 1 mA. Larger transistors were used to handle the additional current. Simulations on the slow process file showed that the increase in current did not increase the speed. The circuit would not perform properly over 80 MHz even though the power consumption increased to 69 mW. The circuit probably did not get faster due to the increased load due to larger transistors and the fact that the current was not the maximum f_T current for the larger device. However, a trend was established.

There is a limit to the speed that can be gained by increasing the power of a gate. The original CPD circuit operated at a maximum frequency of 45.5 MHz; refer to Table 9. Increasing the power of the gate did raise the maximum speed to 80 MHz which is a 77% increase; however, the circuit could not meet the 96 MHz requirement. It may be possible that faster gates could be used in a different configuration to meet the speed requirement, but it is highly likely that it will use more power than the new architecture already presented that uses only standard gates. Therefore, the new architecture is chosen over the faster gates because it meets the requirements without excessive increases in area and power.



Slow File, 500 uA Gates
80 MHz

Figure 43



Slow File, 500 uA Gates
80 MHz

Figure 44

5.0 CONCLUSION

Analytic methods have been used to studied the DC characteristics of fully differential Emitter-Coupled Logic (ECL) gates. Differential operation was chosen because of its inherent immunity to noise. The analysis resulted in equations that predict the DC noise margin of differential gates based on the magnitude of the logic voltage swing and maximum logic swing to avoid saturation. The results of the analysis were confirmed by computer simulation for a logic swing of 340 mV, which yielded a DC noise margin of approximately 115 mV.

A family of ECL gates was then developed. The gates are fully differential and have 3 levels of logic. The family provides 19 different functions with a set of 53 gates. All 19 functions are realized in gates that have a maximum operating frequency of 50 MHz over an ambient temperature range of 0 to 80 degrees Celsius and over all process corners. A subset of the functions were designed in gates that operate at 100 MHz under the same conditions. Computer simulations showed the best case power delay product of a 2-input AND gate to be 1.6 pJ.

All of the gates have been laid out on a high performance, junction isolated, complementary Bipolar process known as CBIC-U. The simulations were performed

on files that included the parasitic layout capacitances. The logic gates were developed in conjunction with analog cells for use in a high-performance data separator for hard disk drives. A computer analysis of a Coincidence Phase Detector shows that the logic gates can be used in the most critical circuits when architectural modifications are made.

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Vita

Lawrence Letham is the son of Daryl L. Letham and Joan Walker Letham and was born on September 1, 1960 in Salt Lake City, Utah. He attended the University of Utah where he received the Bachelor of Science Degree in Electrical Engineering in June of 1986. Upon graduation he accepted employment with the Intel Corporation in Folsom, California where he designed integrated circuits in the Programmable Memory Operation. In April of 1988 he joined AT&T Bell Laboratories in Reading, Pennsylvania where he has designed the ECL logic family using a complementary Bipolar process. While employed at Bell Labs, he started his work on the Master of Science Degree at Lehigh University in September of 1988.

Appendix 1 Data Sheets

The data sheets for the various gates are grouped by function. A description of each gate is given and the propagation delay for various fanouts. The fanout is the number of inputs that the output is driving. Parasitic capacitance of inter-gate connection is not considered; however, the inner-gate parasitic capacitances are included.

The power for each gate is given in the data sheet. The measured power is that consumed only by the gate. The power used by the load is not measured and will vary with the load.

DATA SHEET FOR: **F1A, F1AH, F2A, F2AH**

F1A:	Positive-edge triggered D-FF	50 MHz
F1AH:	Positive-edge triggered D-FF	100 MHz
F2A:	Negative-edge triggered D-FF	50 MHz
F2AH:	Negative-edge triggered D-FF	100 MHz

All of the gates have an area of 305 um X 310 um.

F1A, F2A:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	3.5	2.2	1.3
3	3.8	2.4	1.4
5	4.1	2.8	1.6
7	4.5	2.8	1.6

Power (mW)

Max	Nom	Min
4.7	3.5	2.9

F1AH, F2AH:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	2.3	1.5	1.0
3	2.5	1.7	1.0
5	2.7	1.8	1.1
7	2.9	1.9	1.2

Power (mW)

Max	Nom	Min
8.1	6.1	5.0

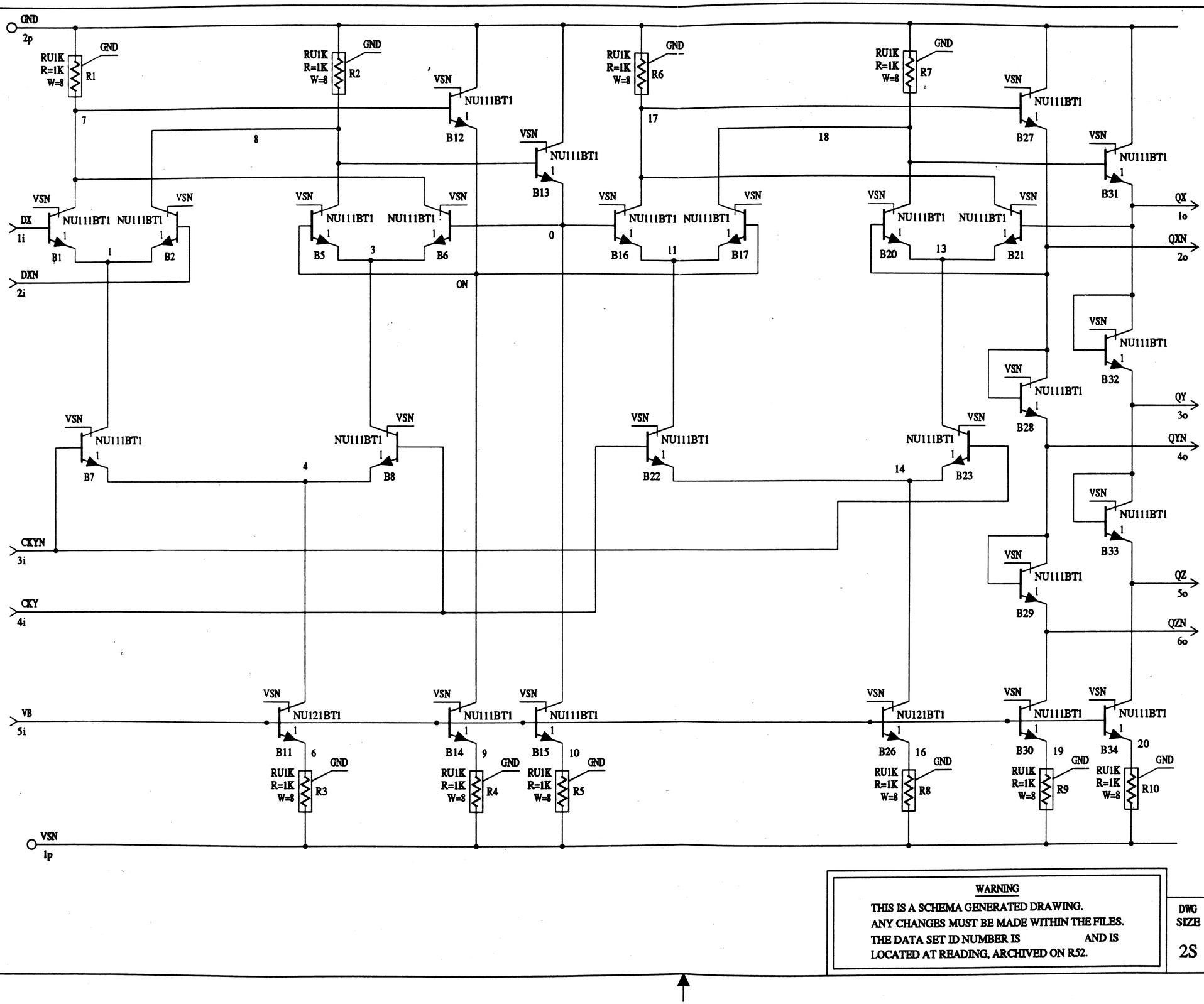
Setup and Hold times:

Setup (ns)

Max	Nom	Min
2.1	1.6	1.2

Hold (ns)

Max	Nom	Min
1.3	0.8	0.38



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F1A.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE
TRIGGERED
(F1A.1)

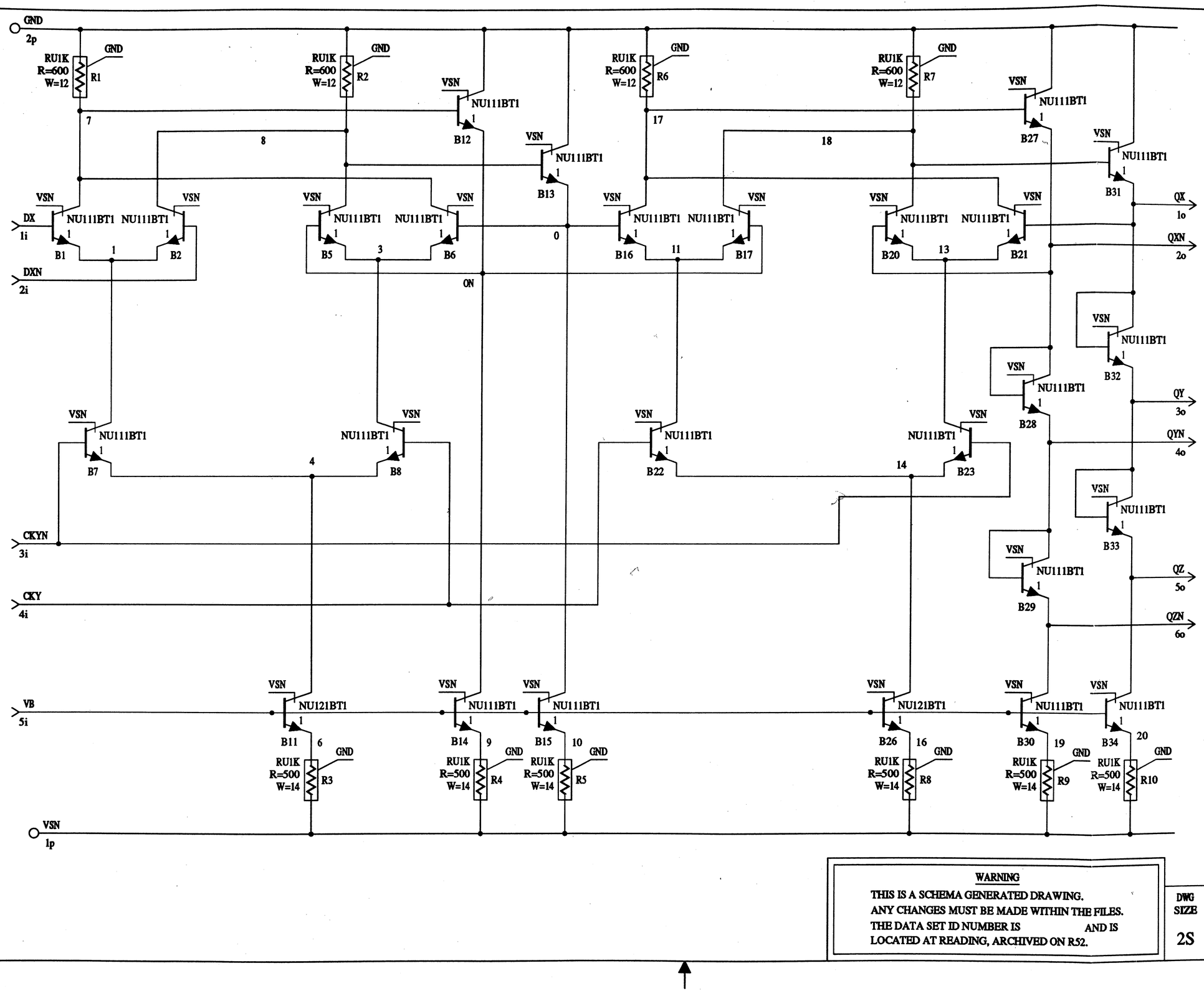
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 106

17X11



ENGR	DLL
DRWN	MDA
Nov. 21, 1989	ISSUE

F1AH.1

USED ON	DRAWING
AT&T -	

DFF
POS. EDGE TRIG.
HIGH CURRENT
(F1AH.1)

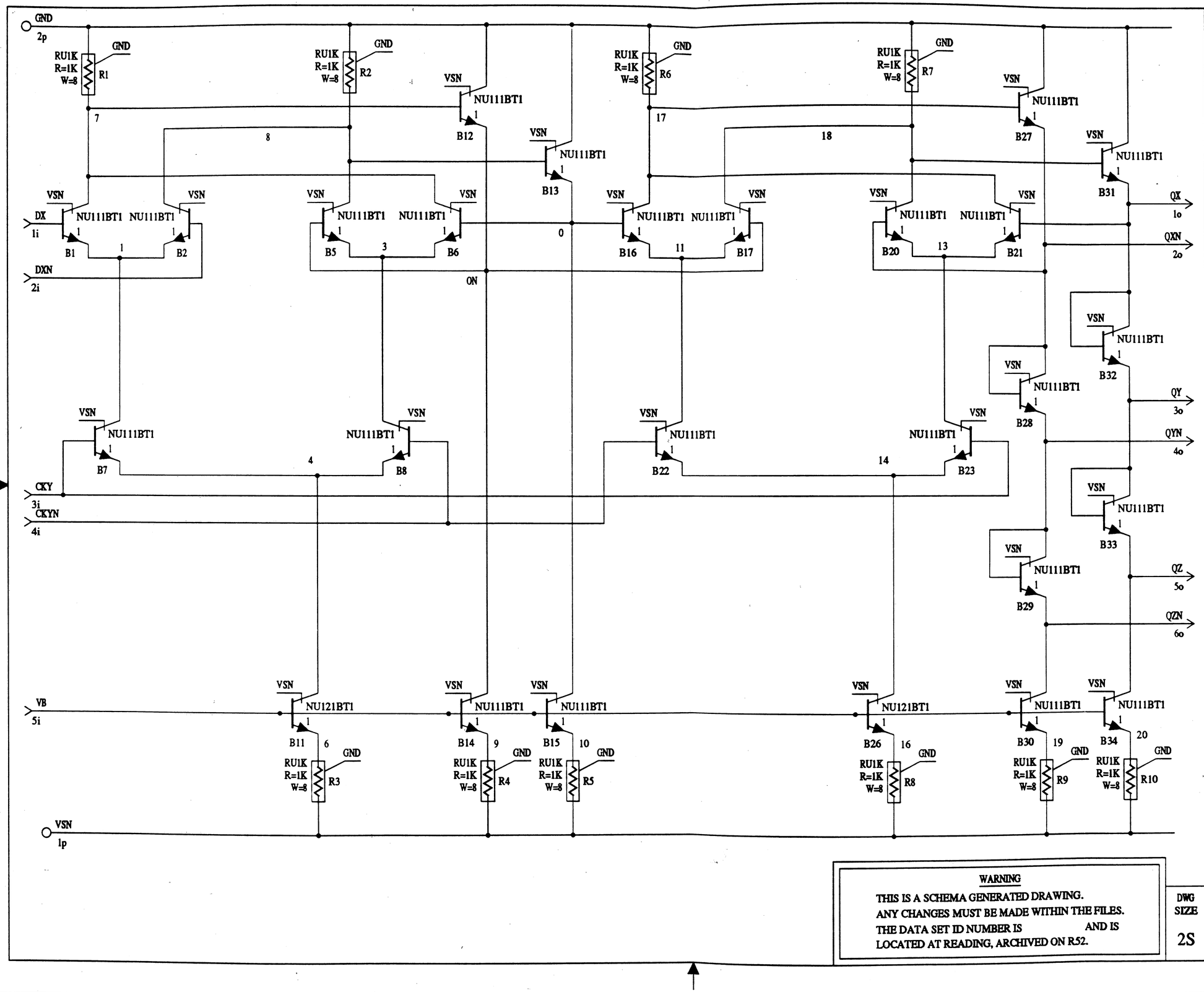
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 107

17X11



ENGR	DLL
DRWN	MDA

Nov. 21, 1989 ISSUE

F2A.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE
TRIGGERED
(F2A.1)

WARNING

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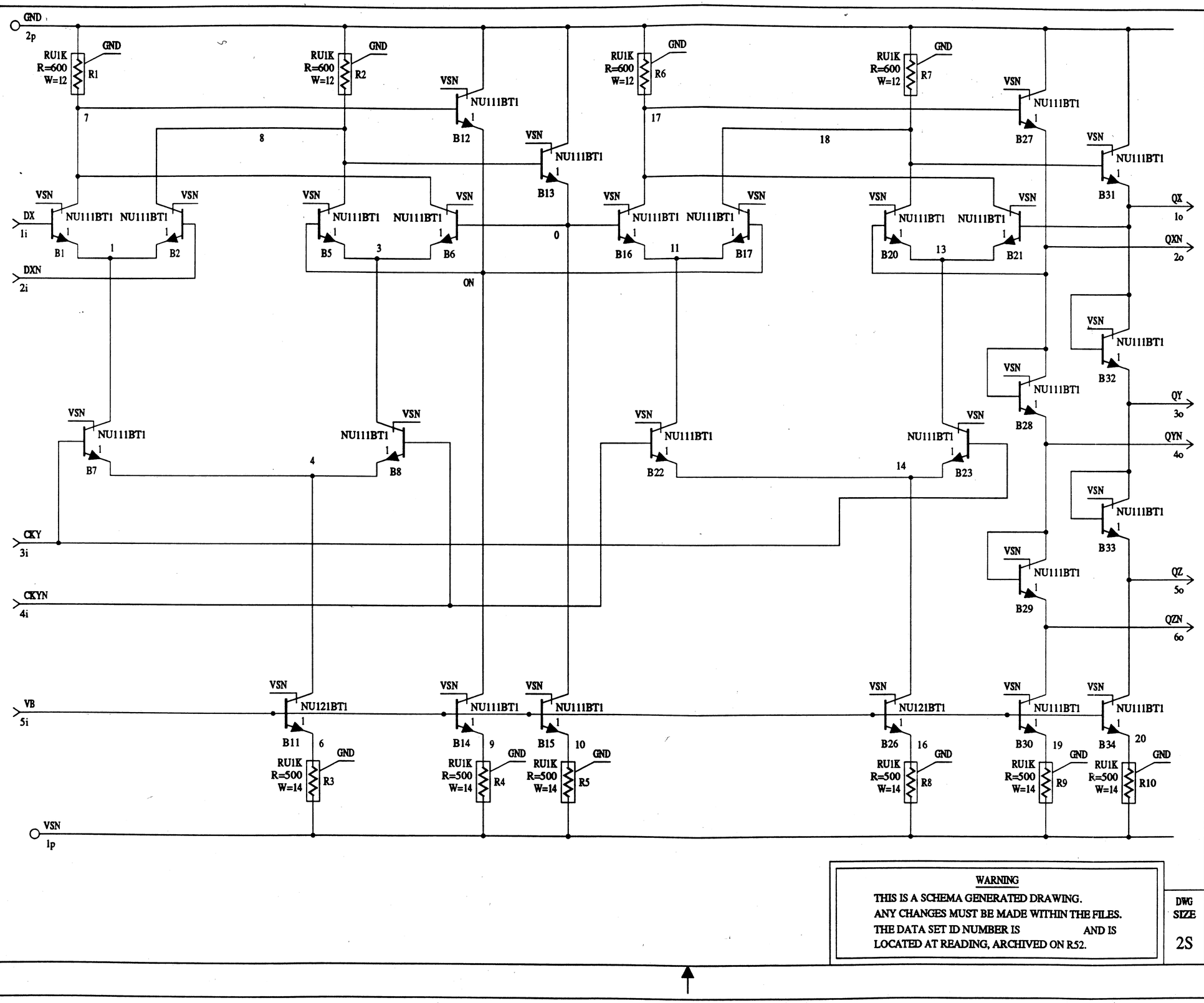
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 108

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

F2AH.1

USED ON	DRAWING

AT&T -

DFF
NEG. EDGE TRIG.
HIGH CURRENT
(F2AH.1)

WARNING

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THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 109

17X11

DATA SHEET FOR: F1B, F1BH, F2B, F2BH, F5B, F6B

F1B:	Positive-edge D-FF with preset	50 MHz
F1BH:	Positive-edge D-FF with preset	100 MHz
F2B:	Negative-edge D-FF with preset	50 MHz
F2BH:	Negative-edge D-FF with preset	100 MHz
F5B:	Positive-edge D-FF with preset, D=0	50 MHz
F6B:	Negative-edge D-FF with preset, D=0	50 MHz

All of the gates have an area of 305 um X 310 um.

F1B, F2B, F5B, F6B:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	3.5	2.2	1.3
3	3.8	2.4	1.4
5	4.1	2.8	1.6
7	4.5	2.8	1.6

Power (mW)

Max	Nom	Min
4.7	3.5	2.9

F1BH, F2BH:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	2.3	1.5	1.0
3	2.5	1.7	1.0
5	2.7	1.8	1.1
7	2.9	1.9	1.2

Power (mW)

Max	Nom	Min
8.1	6.1	5.0

Setup and Hold times:

Setup (ns)

Max	Nom	Min
2.1	1.6	1.2

Hold (ns)

Max	Nom	Min
1.3	0.8	0.38

The characteristics of the pulse required to preset or clear the FF has not been specified by a pulse width, but by the magnitude of the pulse peak. If the preset, clear or enable signal is driven by a gate from this family, a pulse of the stated magnitude will have the width needed to preset or clear the FF. The magnitude of the pulse needed to preset or clear the FF is:

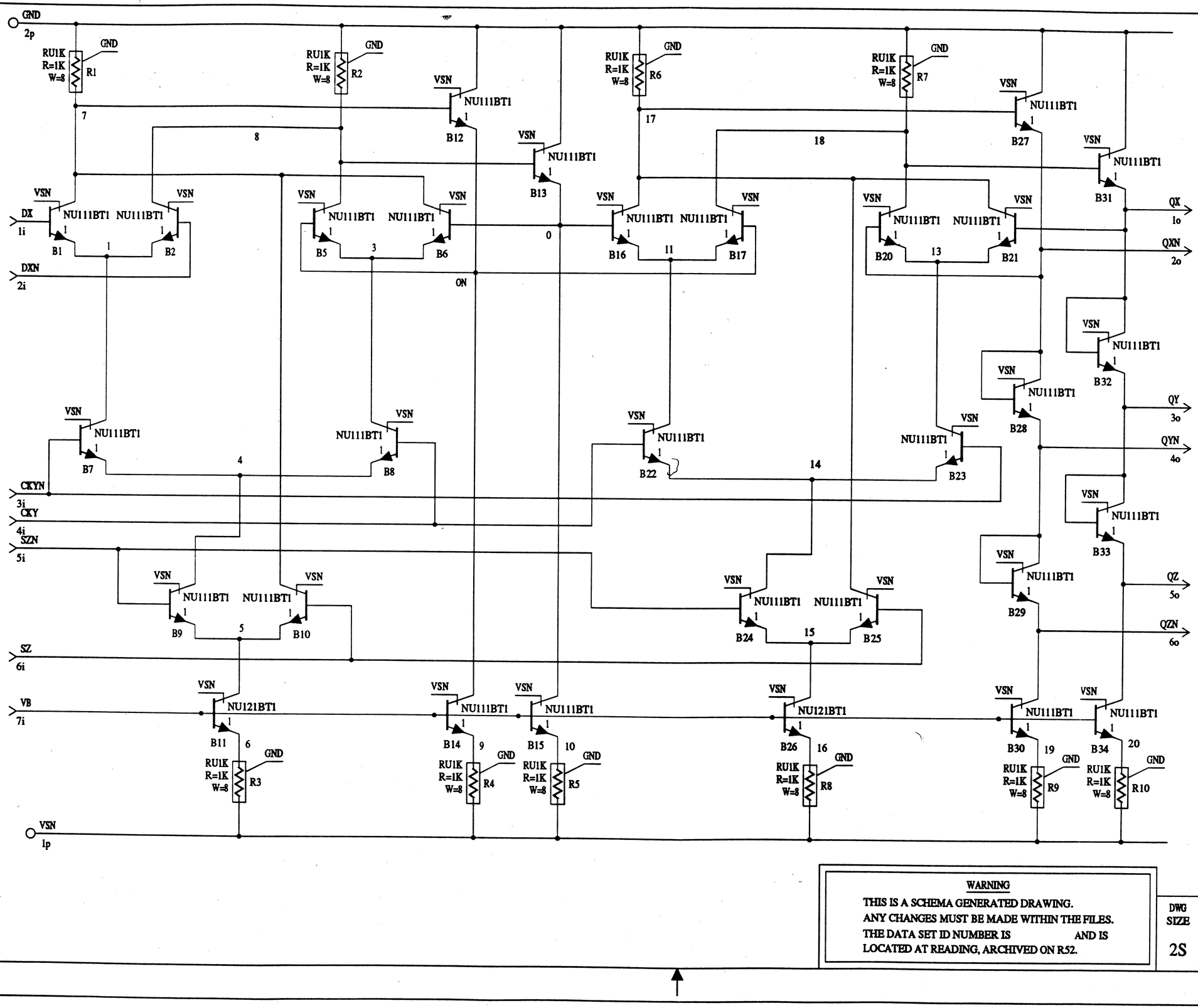
Preset or Clear Pulse Magnitude (mV)

Max	Nom	Min
237	197	185

The time from asserting the preset, clear or enable signal to valid output is (Fanout = 3):

Preset or Clear to valid output (ns)

Max	Nom	Min
3.7	2.3	1.4



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F1B.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE
TRIGGERED
(F1B.1)

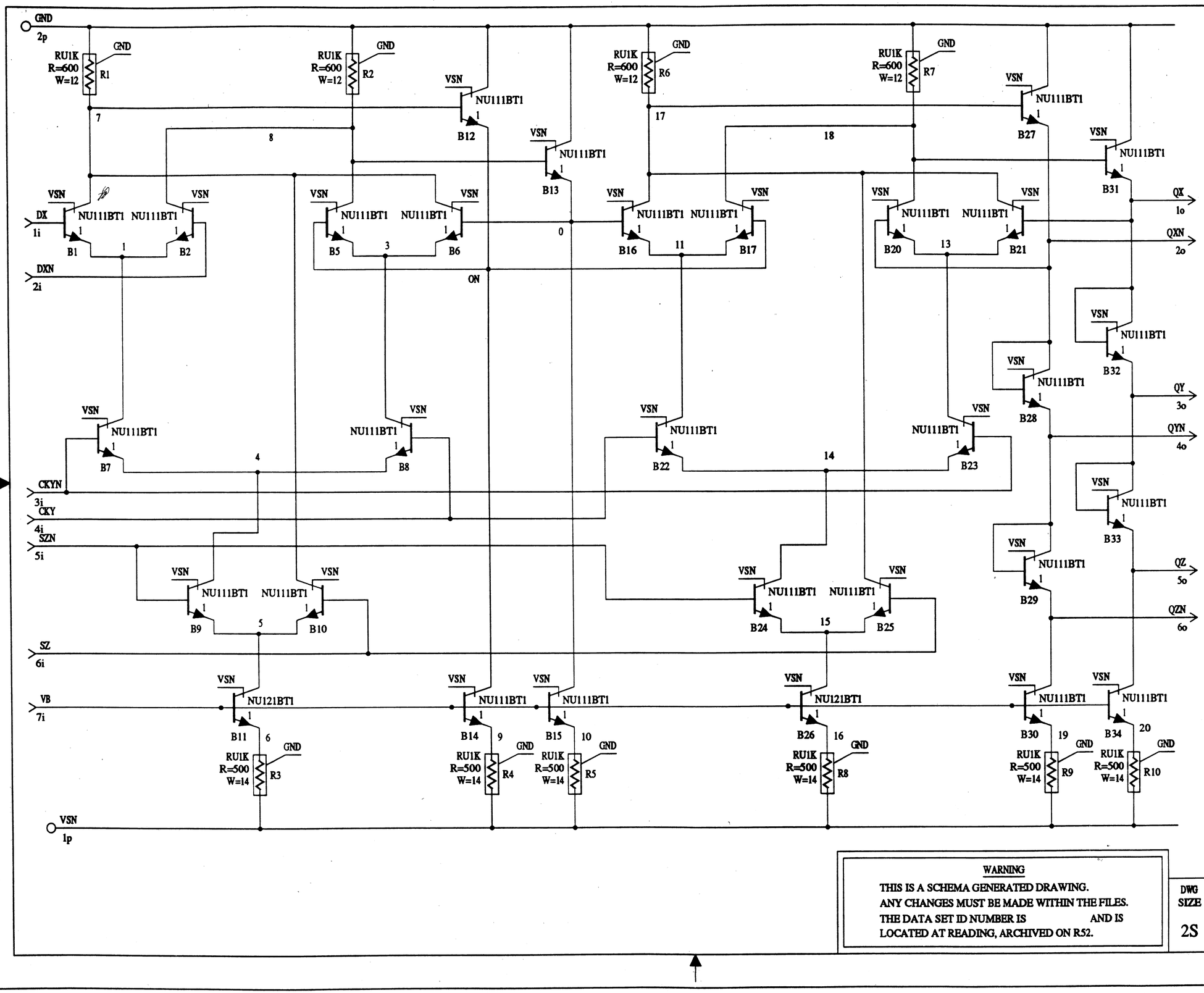
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 112

17X11



ENGR	DLL
DRWN	MDA
Nov. 21, 1989	ISSUE

F1BH.1

USED ON	DRAWING
AT&T -	

DFF
POS. EDGE TRIG.
HIGH CURRENT
(F1BH.1)

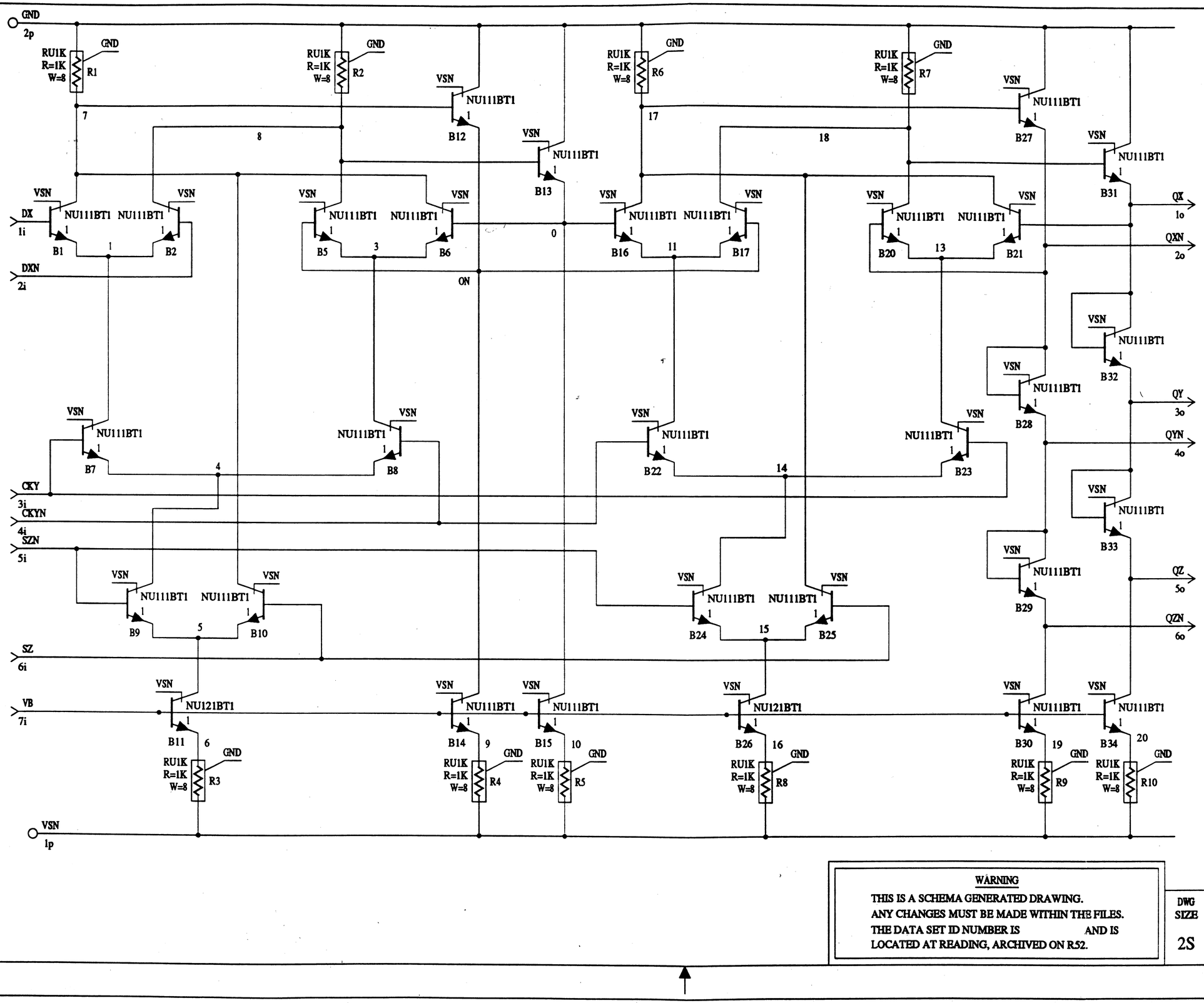
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 113

17X11



ENGR	DLL
DRWN	MDA

Nov. 20, 1989 ISSUE

F2B.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE
TRIGGERED
(F2B.1)

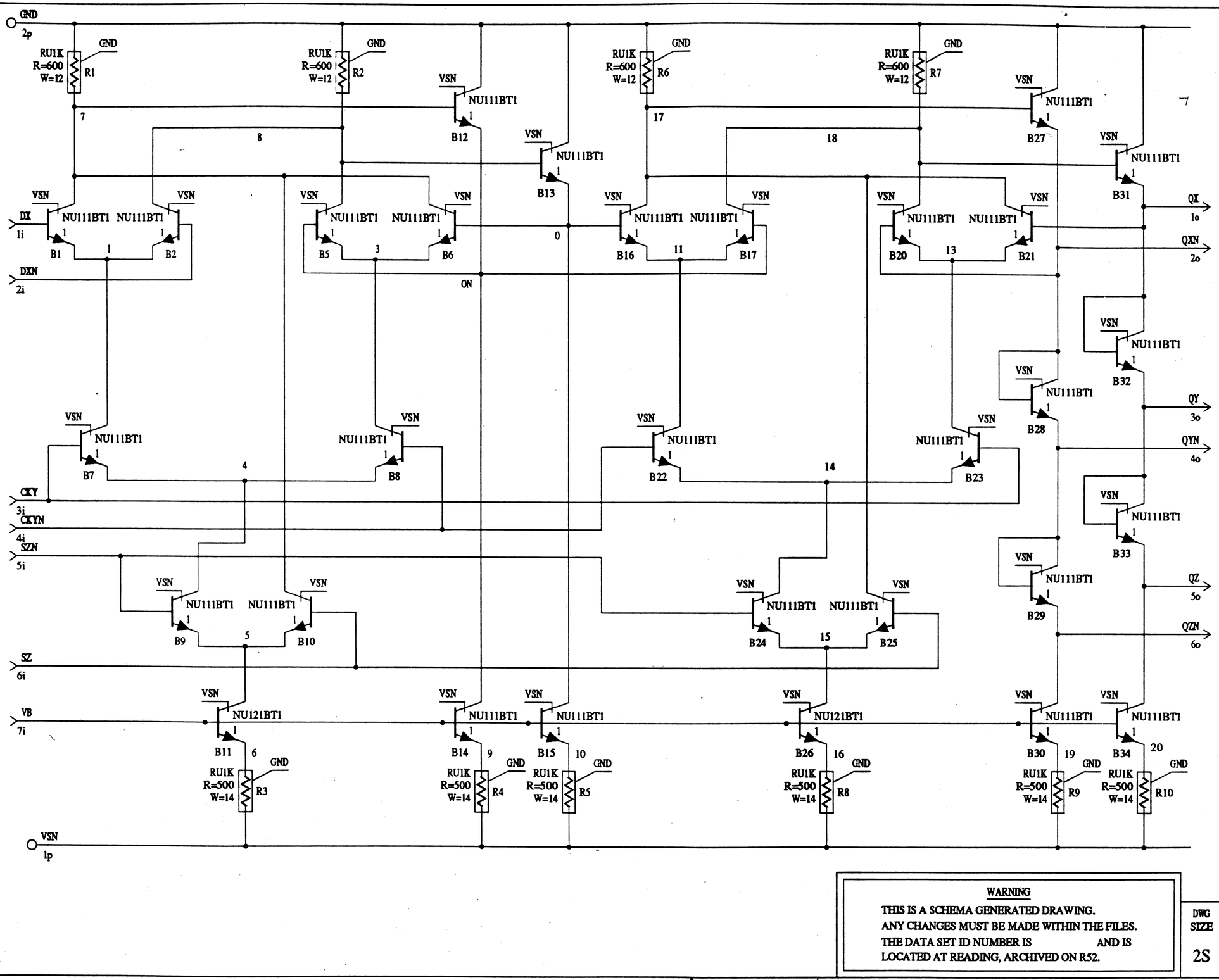
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 114

17X11



ENGR	DLL
DRWN	MDA

Dec. 13, 1989 ISSUE

F2BH.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE TRIG.
HIGH CURRENT
(F2BH.1)

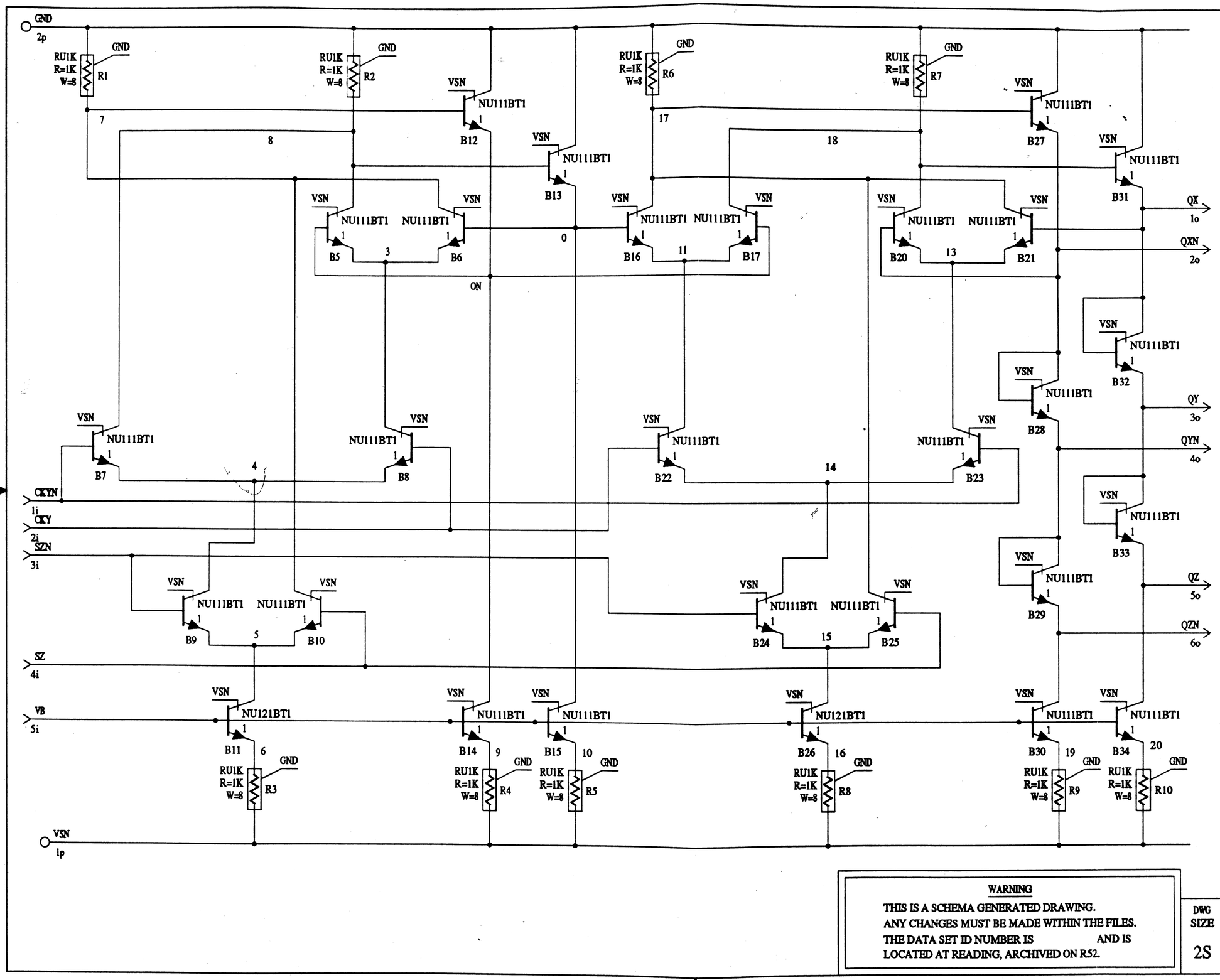
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 115

17X11



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F5B.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE
TRIGGERED
(F5B.1)

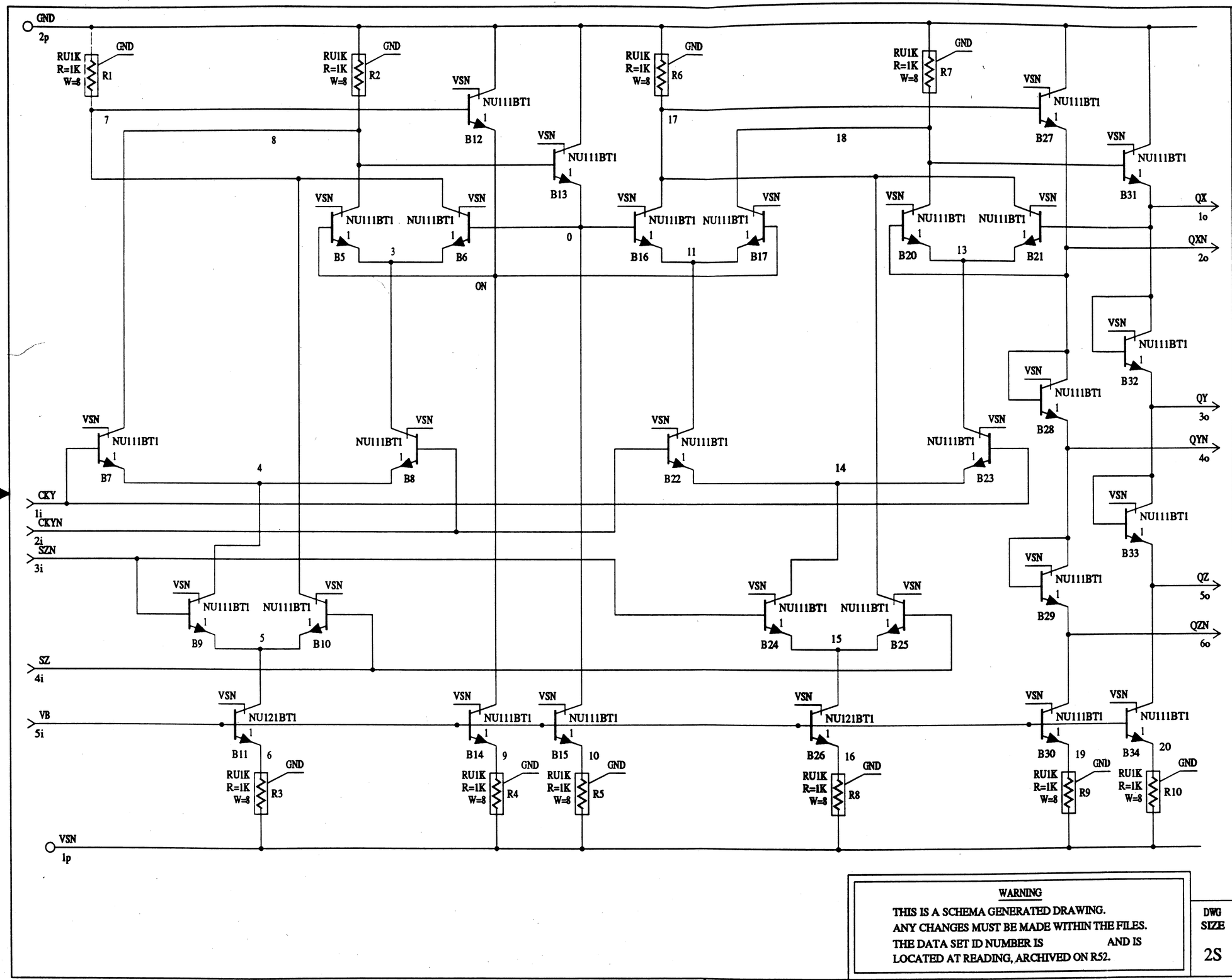
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 116

17X11



ENGR	DLL
DRWN	MDA
Nov. 21, 1989	ISSUE

F6B.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE
TRIGGERED
(F6B.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 117

17X11

DATA SHEET FOR: F1C, F2C

F1C: Positive-edge D-FF with preset and clear 50 MHz

F2C: Negative-edge D-FF with preset and clear 50 MHz

All of the gates have an area of 335 um X 310 um.

F1C, F2C:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	3.5	2.2	1.3
3	3.8	2.4	1.4
5	4.1	2.8	1.6
7	4.5	2.8	1.6

Power (mW)

Max	Nom	Min
4.7	3.5	2.9

Setup and Hold times:

Setup (ns)

Max	Nom	Min
2.1	1.6	1.2

Hold (ns)

Max	Nom	Min
1.3	0.8	0.38

The characteristics of the pulse required to preset or clear the FF has not been specified by a pulse width, but by the magnitude of the pulse peak. If the preset, clear or enable signal is driven by a gate from this family, a pulse of the stated magnitude will have the width needed to preset or clear the FF. The magnitude of the pulse needed to preset or clear the FF is:

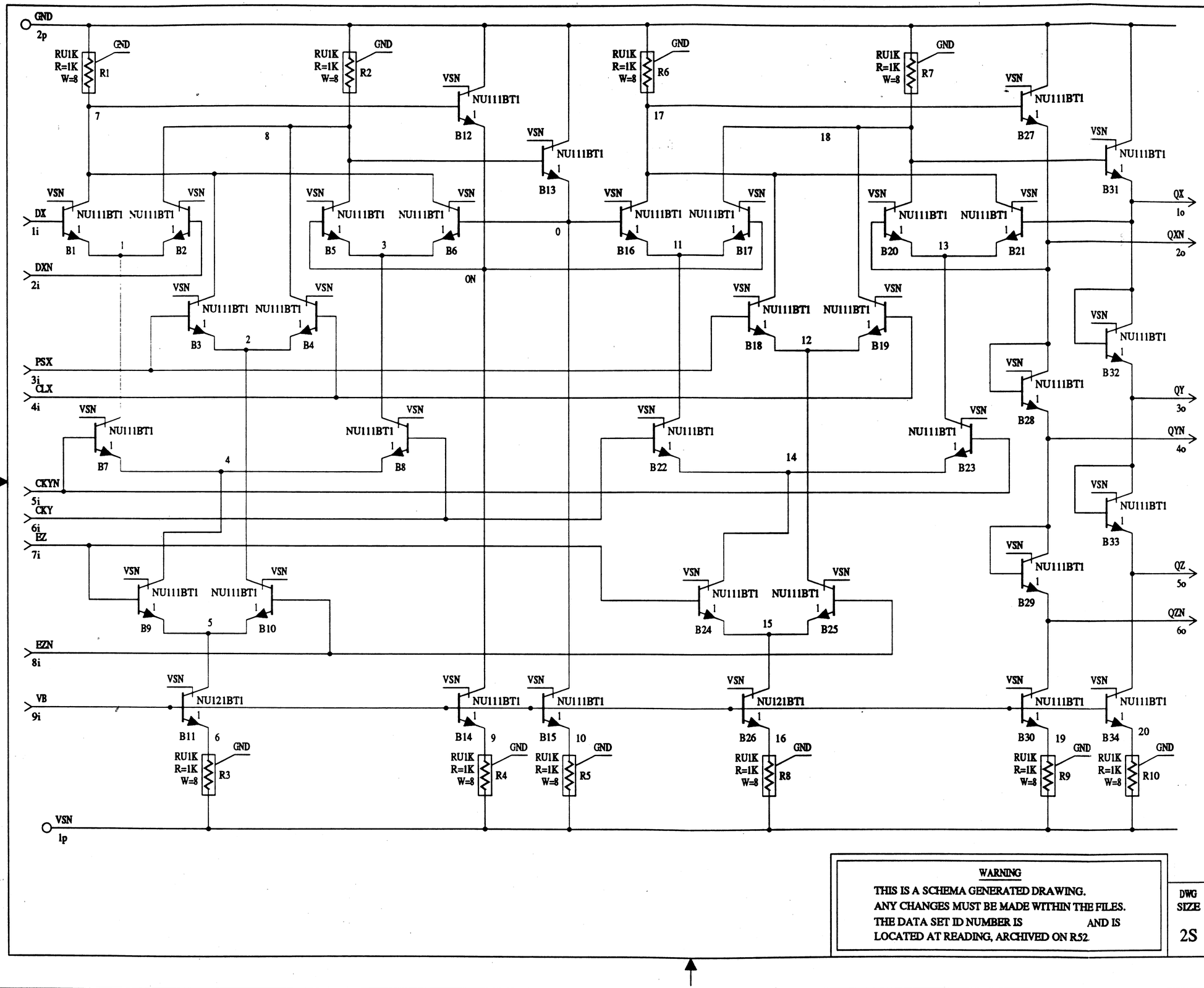
Preset or Clear
Pulse Magnitude
(mV)

Max	Nom	Min
237	197	185

The time from asserting the preset, clear or enable signal to valid output is (Fanout = 3):

Preset or Clear
to valid output
(ns)

Max	Nom	Min
3.7	2.3	1.4



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F1C.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE
TRIGGERED
(F1C.1)

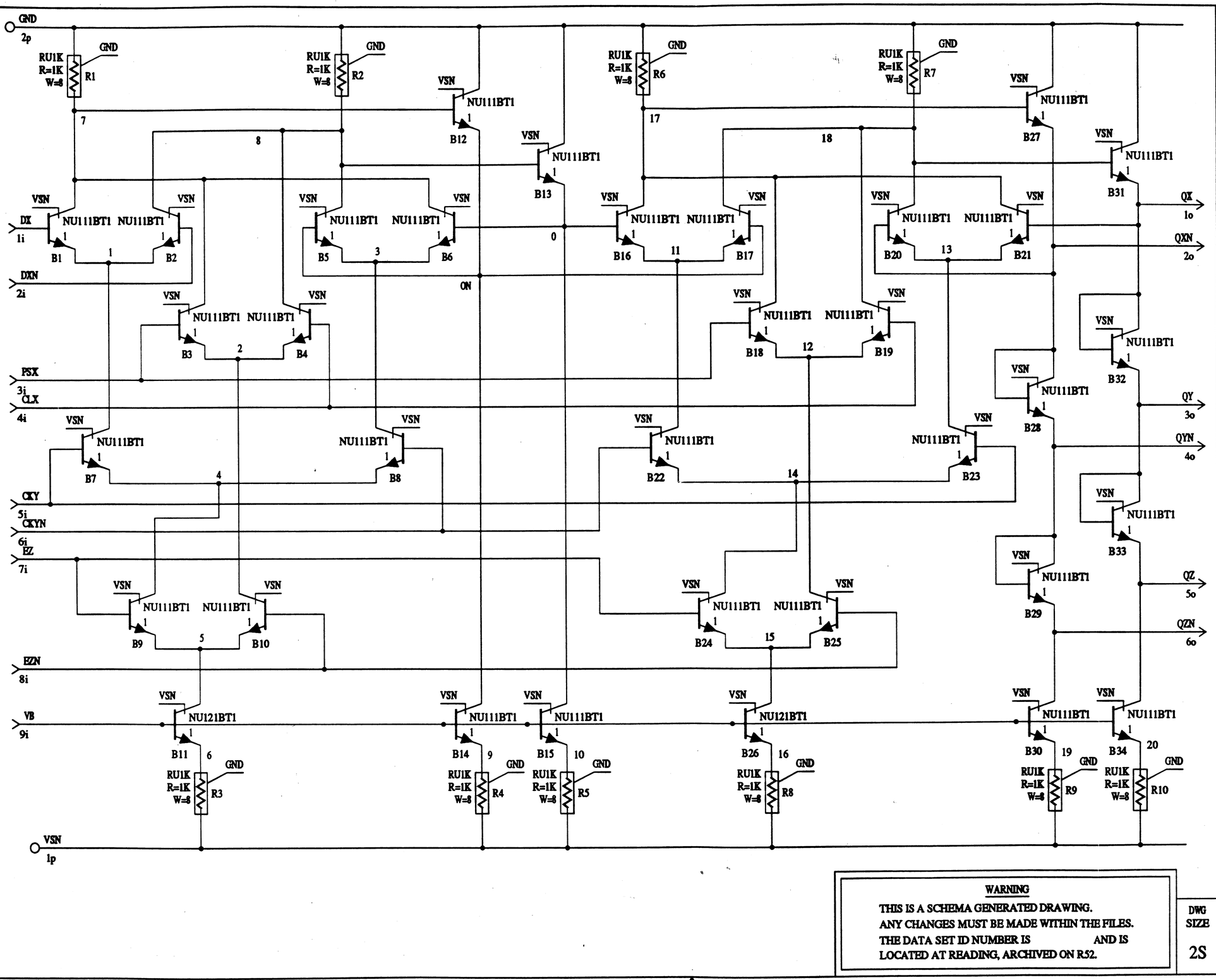
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 120

17X11



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F2C.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE
TRIGGERED
(F2C.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 121

17X11

DATA SHEET FOR: F1D, F1DH, F2D, F2DH, F5D, F5DH, F6D

F1D:	Positive-edge D-FF with clear	50 MHz
F1DH:	Positive-edge D-FF with clear	100 MHz
F2D:	Negative-edge D-FF with clear	50 MHz
F2DH:	Negative-edge D-FF with clear	100 MHz
F5D:	Positive-edge D-FF with clear, D=1	50 MHz
F5DH:	Positive-edge D-FF with clear, D=1	100 MHz
F6D:	Negative-edge D-FF with clear, D=1	50 MHz

All of the gates have an area of 305 um X 310 um.

F1D, F2D, F5D, F6D:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	3.5	2.2	1.3
3	3.8	2.4	1.4
5	4.1	2.8	1.6
7	4.5	2.8	1.6

Power (mW)

Max	Nom	Min
4.7	3.5	2.9

F1DH, F2DH, F5DH:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	2.3	1.5	1.0
3	2.5	1.7	1.0
5	2.7	1.8	1.1
7	2.9	1.9	1.2

Power (mW)

Max	Nom	Min
8.1	6.1	5.0

Setup and Hold times:

Setup (ns)

Max	Nom	Min
2.1	1.6	1.2

Hold (ns)

Max	Nom	Min
1.3	0.8	0.38

The characteristics of the pulse required to preset or clear the FF has not been specified by a pulse width, but by the magnitude of the pulse peak. If the preset, clear or enable signal is driven by a gate from this family, a pulse of the stated magnitude will have the width needed to preset or clear the FF. The magnitude of the pulse needed to preset or clear the FF is:

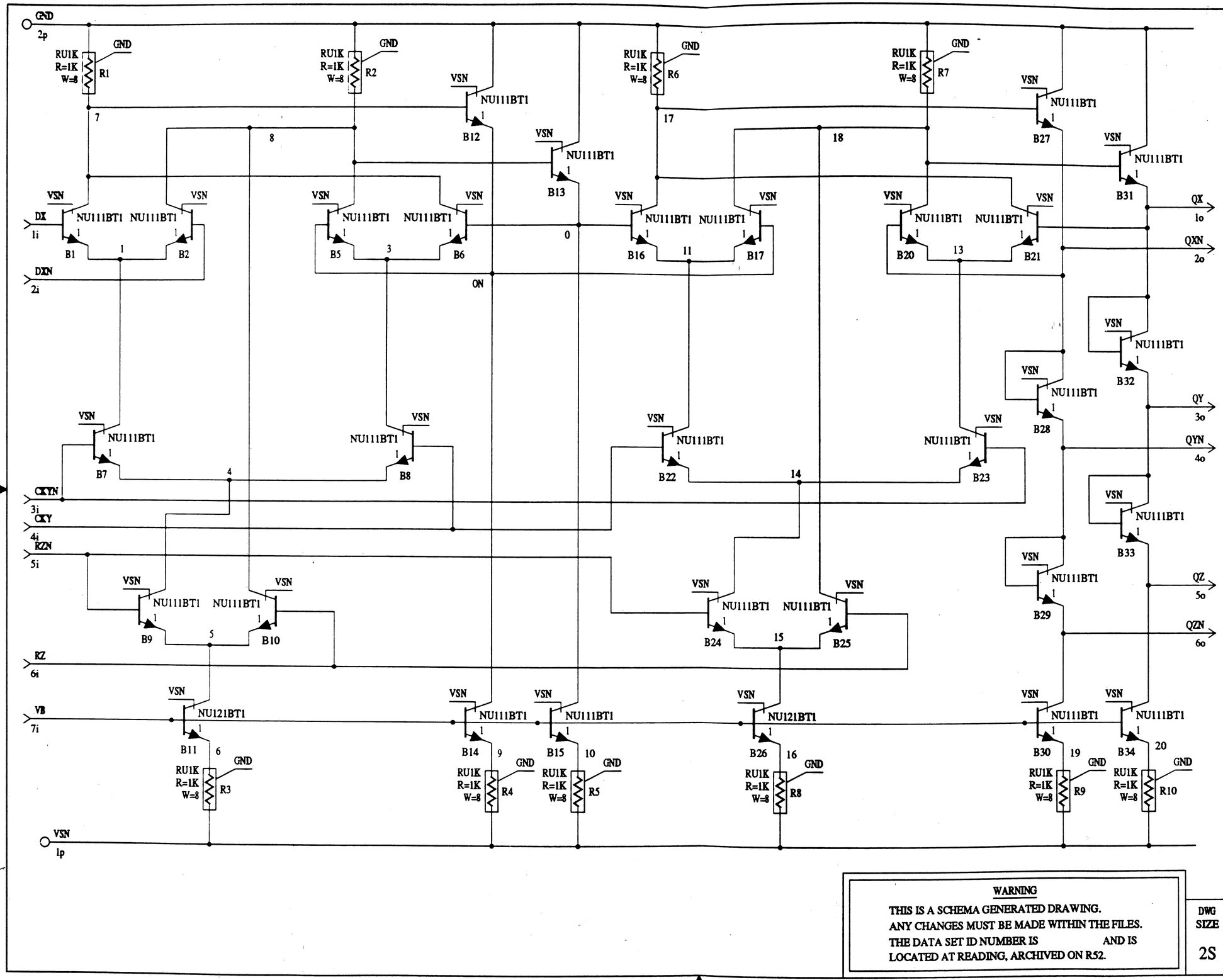
Preset or Clear Pulse Magnitude (mV)

Max	Nom	Min
237	197	185

The time from asserting the preset, clear or enable signal to valid output is (Fanout = 3):

Preset or Clear to valid output (ns)

Max	Nom	Min
3.7	2.3	1.4



ENGR	DLL
DRWN	MDA
Nov. 20, 1989	ISSUE

F1D.1

USED ON	DRAWING
AT&T -	

DFF
POS. EDGE
TRIGGERED
(F1D.1)

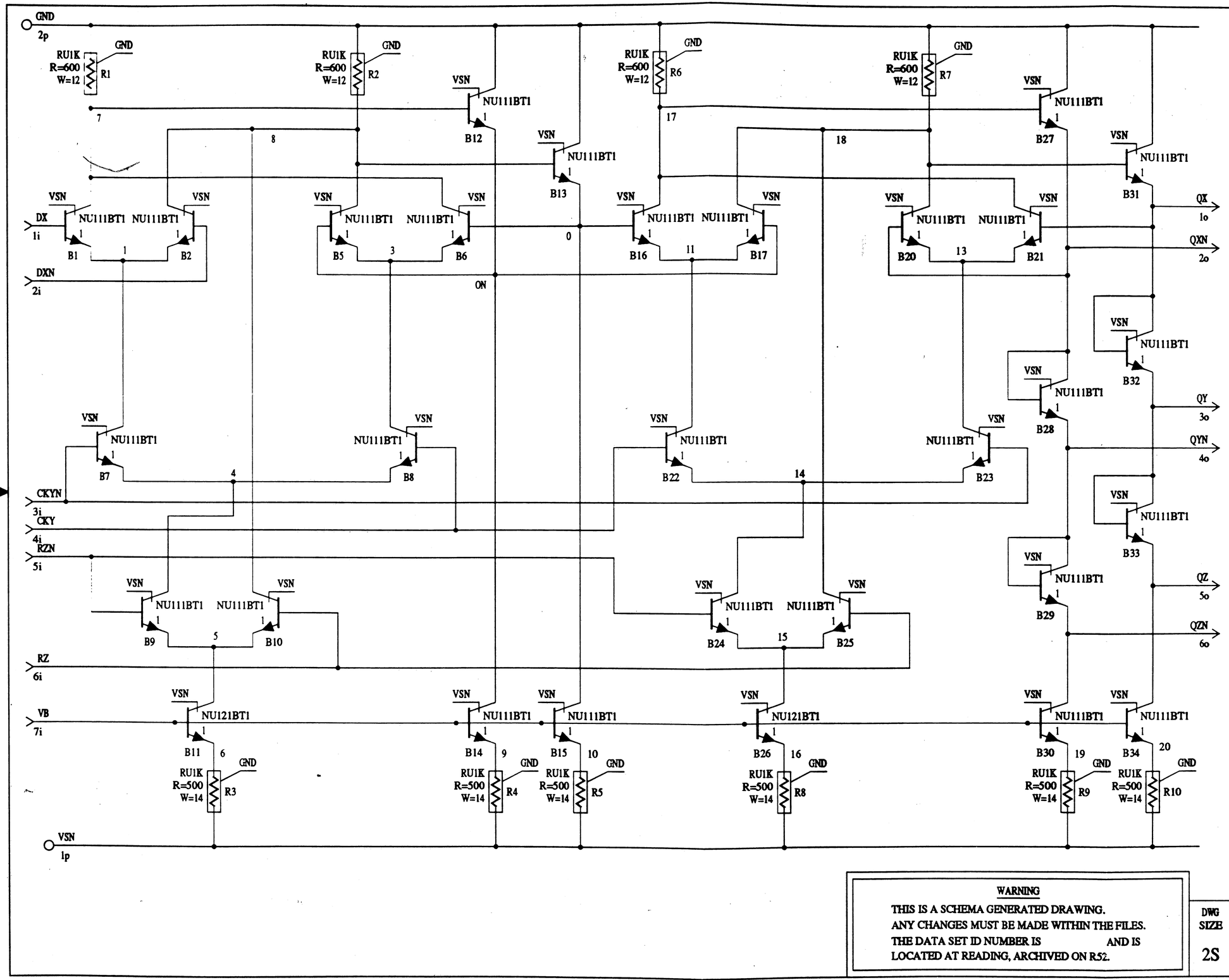
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 124

17X11



ENGR	DLL		
DRWN	MDA		
Nov. 21, 1989	ISSUE		

F1DH.1

USED ON	DRAWING
AT&T -	

DFF
POS. EDGE TRIG.
HIGH CURRENT
(F1DH.1)

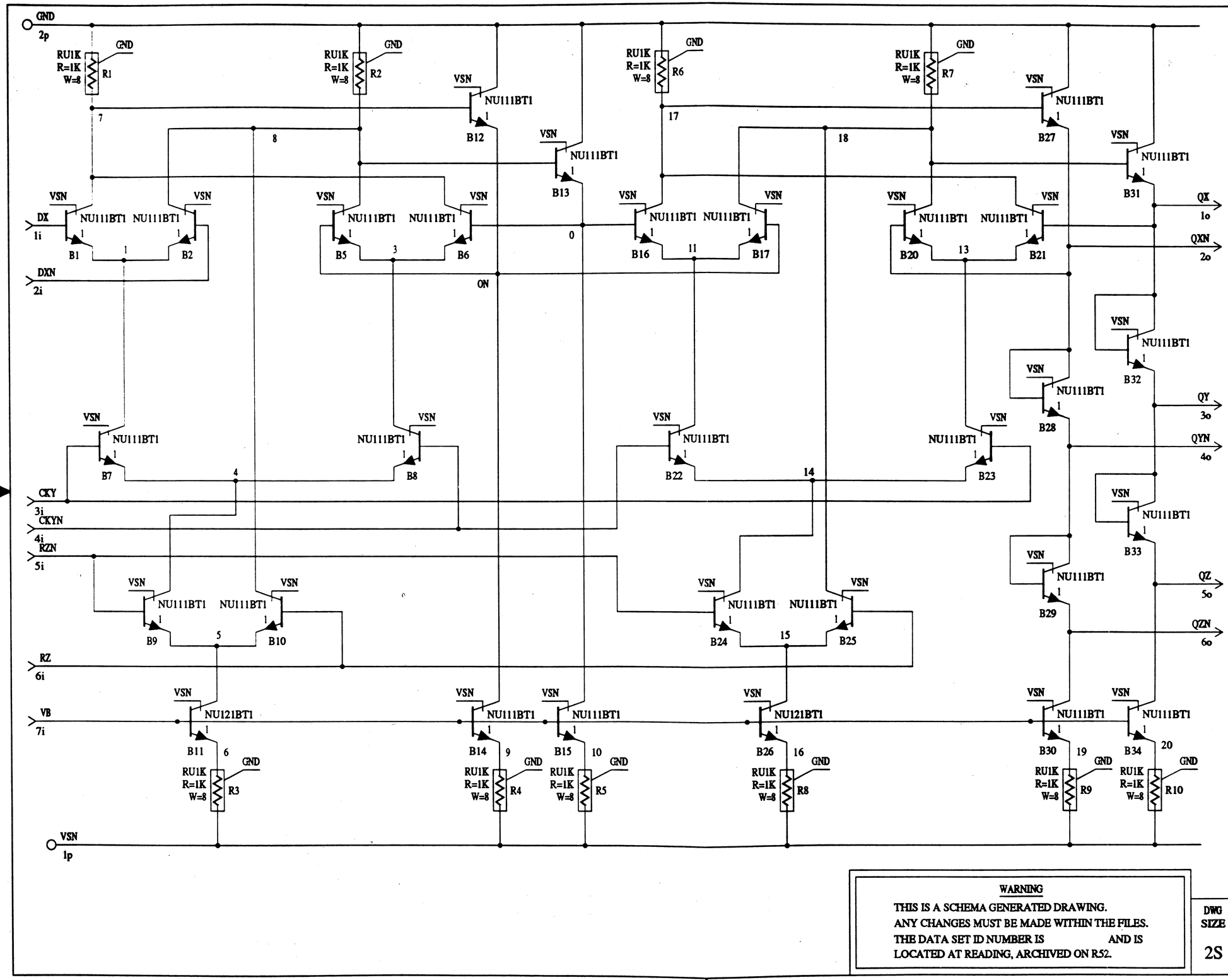
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 125

17X11



ENGR	DLL		
DRWN	MDA		
Nov. 20, 1989	ISSUE		

F2D.1

USED ON	DRAWING

AT&T -

DFF
NEG. EDGE
TRIGGERED
(F2D.1)

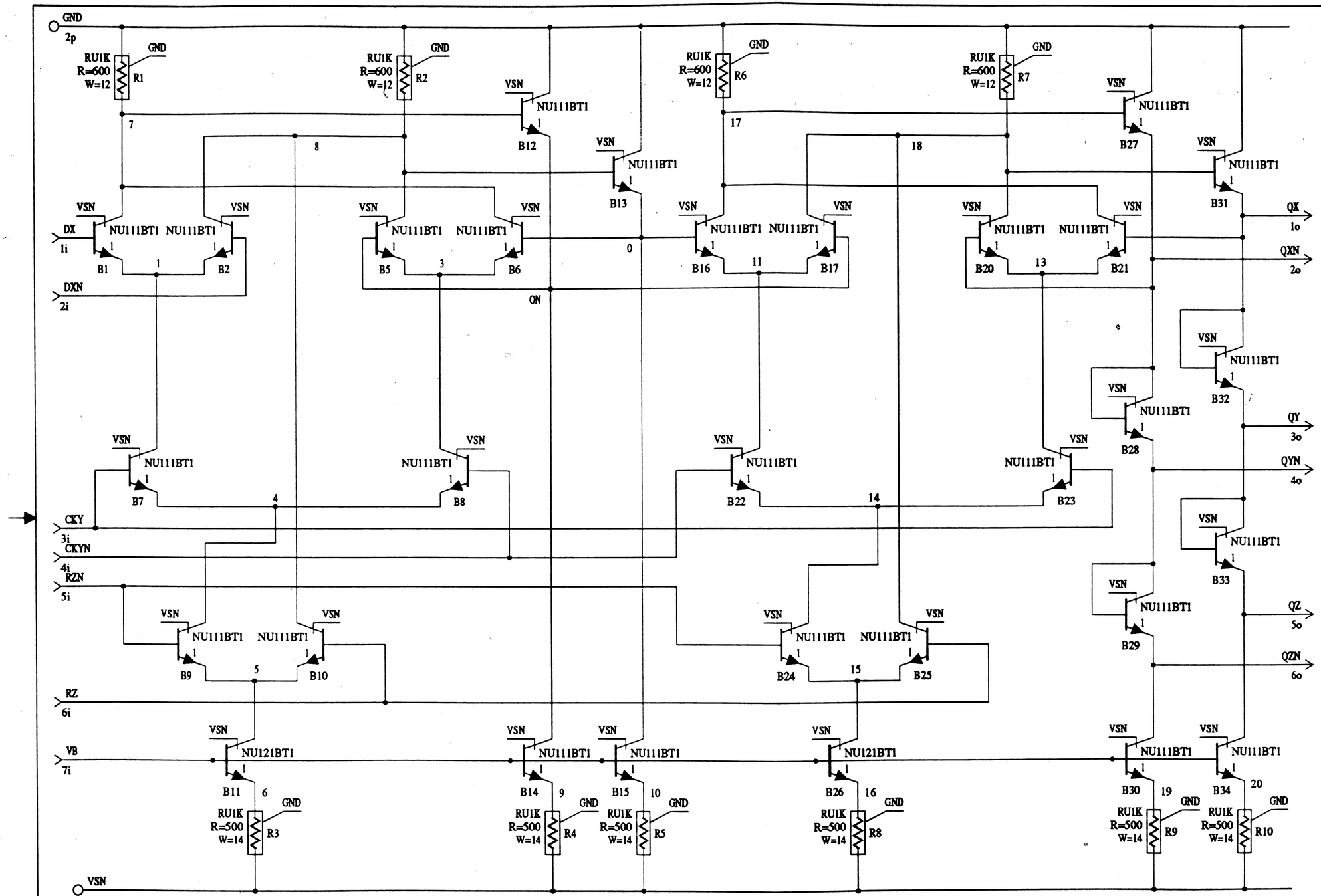
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 126

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

F2DH.1

USED ON	DRAWING

AT&T -

DFF
NEG. EDGE TRIG.
HIGH CURRENT
(F2DH.1)

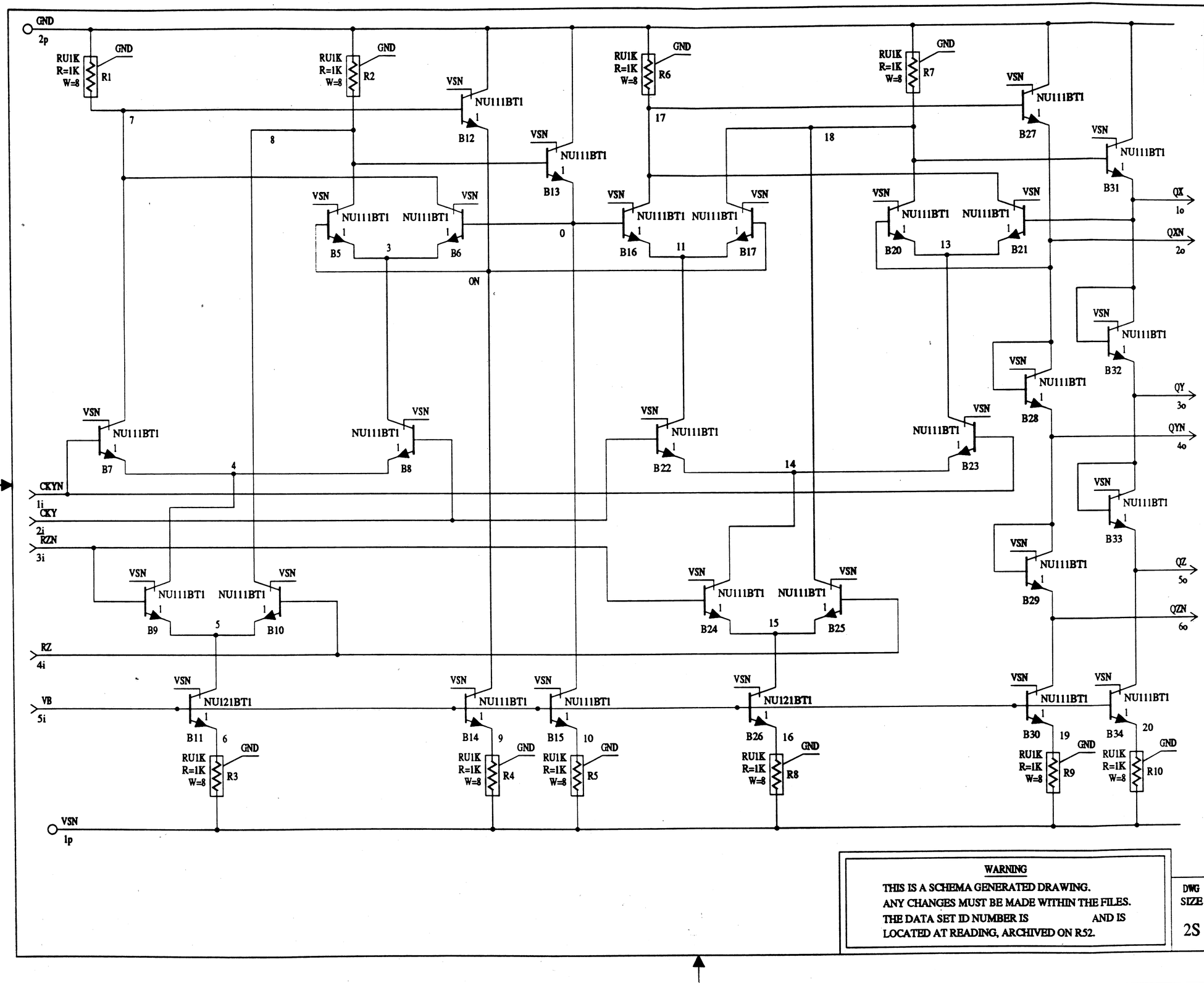
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 127

17X11



ENGR	DLL
DRWN	MDA

Nov. 21, 1989 ISSUE

F5D.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE
TRIGGERED
(F5D.1)

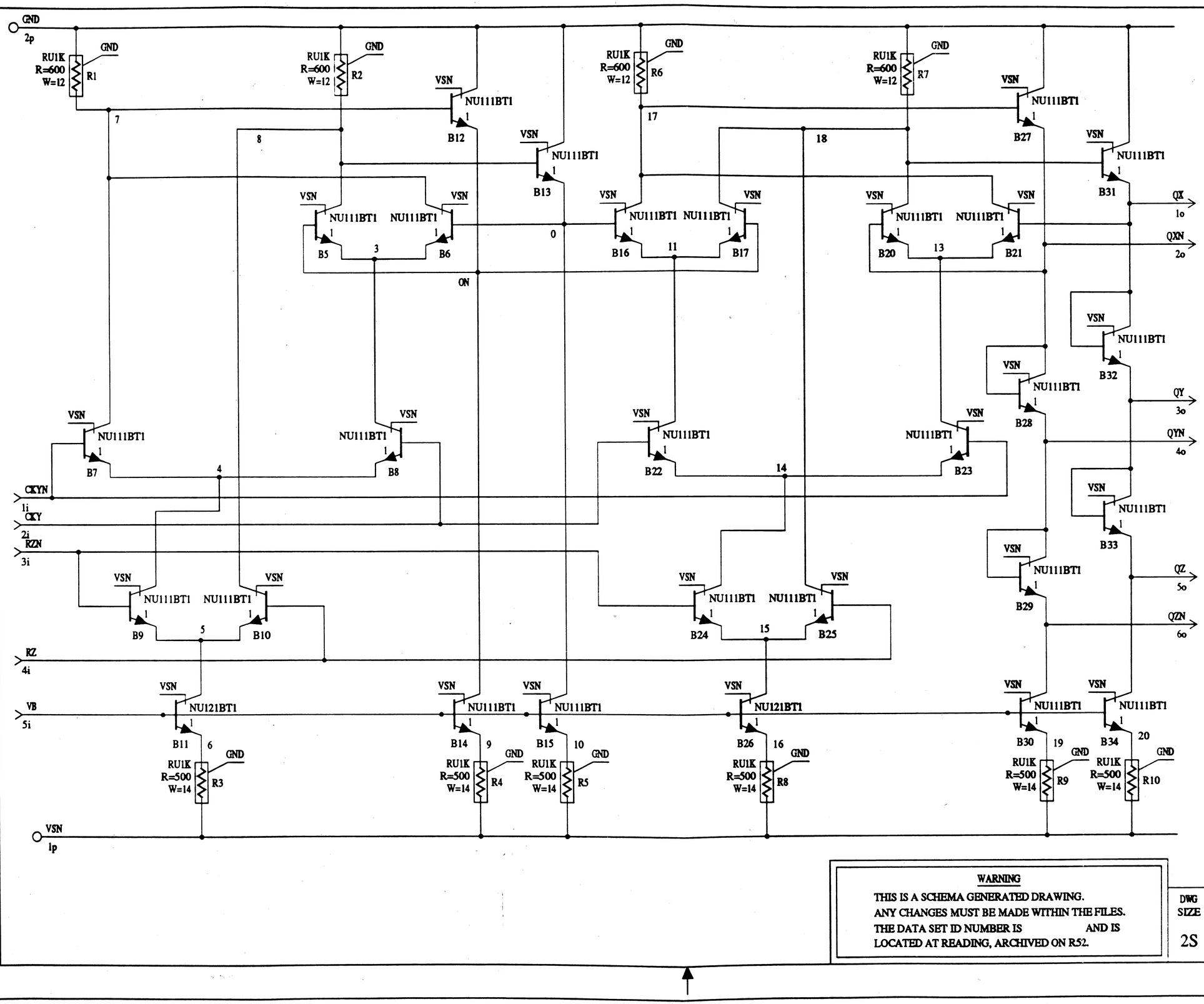
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 128

17X11



ENGR	DLL
DRWN	MDA
Nov. 21, 1989	ISSUE

F5DH.1

USED ON	DRAWING

AT&T -

DFF
POS. EDGE TRIG.
HIGH MODE
(F5DH.1)

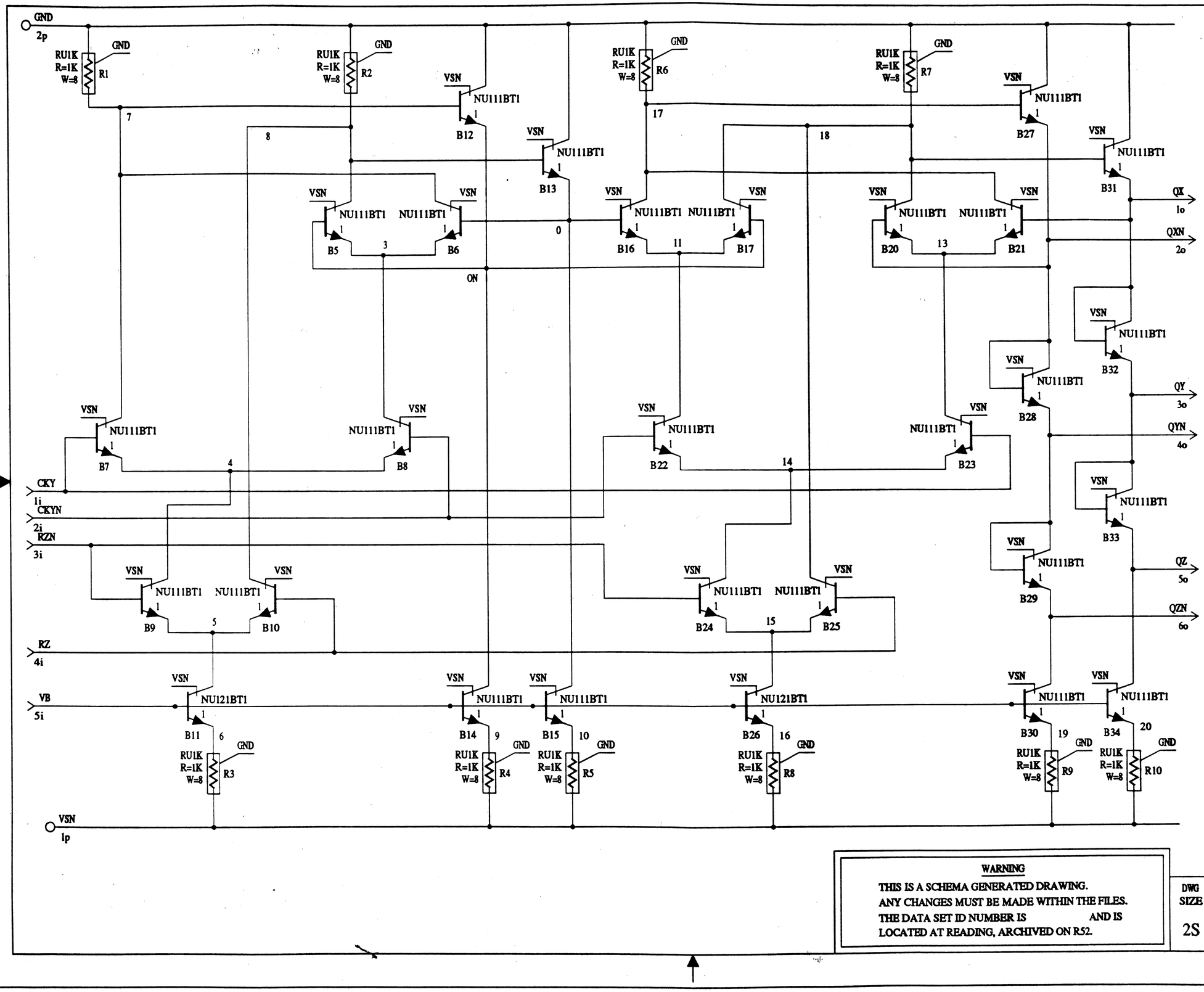
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 129

17X11



ENGR	DLL
DRWN	MDA
Nov. 21, 1989	ISSUE

F6D.1

USED ON	DRAWING
AT&T -	

DFF
NEG. EDGE
TRIGGERED
(F6D.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 130

17X11

DATA SHEET FOR:

AND2, AND2H, NAND2, NAND2H, OR2, OR2H, NOR2, NOR2H

AND2:	2-input AND gate	50 MHz
AND2H:	2-input AND gate	100 MHz
NAND2:	2-input NAND gate	50 MHz
NAND2H:	2-input NAND gate	100 MHz
OR2:	2-input OR gate	50 MHz
OR2H:	2-input OR gate	100 MHz
NOR2:	2-input NOR gate	50 MHz
NOR2H:	2-input NOR gate	100 MHz

All of the gates have an area of 135 um X 310 um.

AND2, NAND2, OR2, NOR2:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.6	1.0	0.7
3	1.9	1.2	0.8
5	2.2	1.4	0.9
7	2.5	1.5	1.0

Power (mW)

Max	Nom	Min
2.4	1.8	1.5

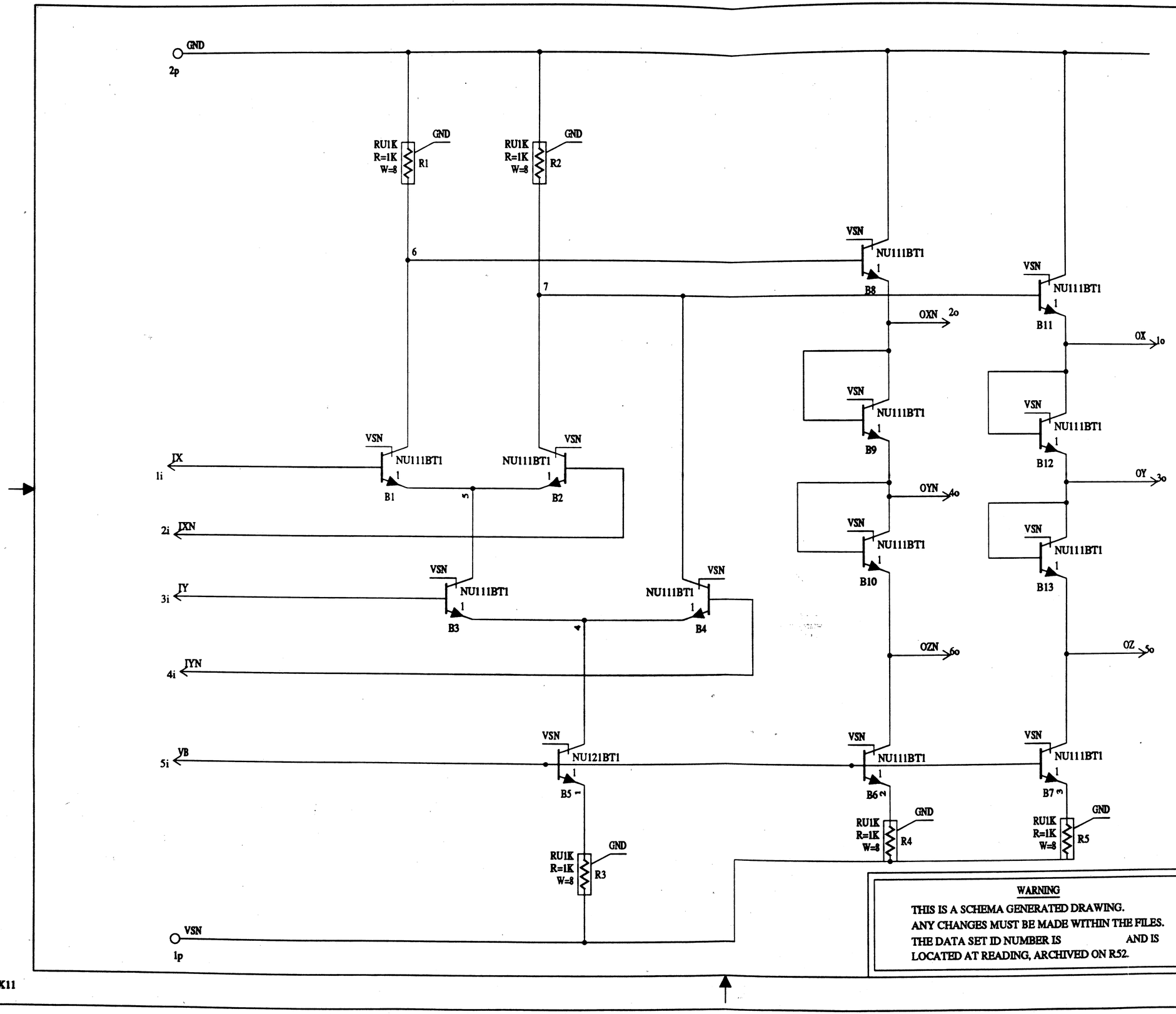
AND2H, NAND2H, OR2H, NOR2H:

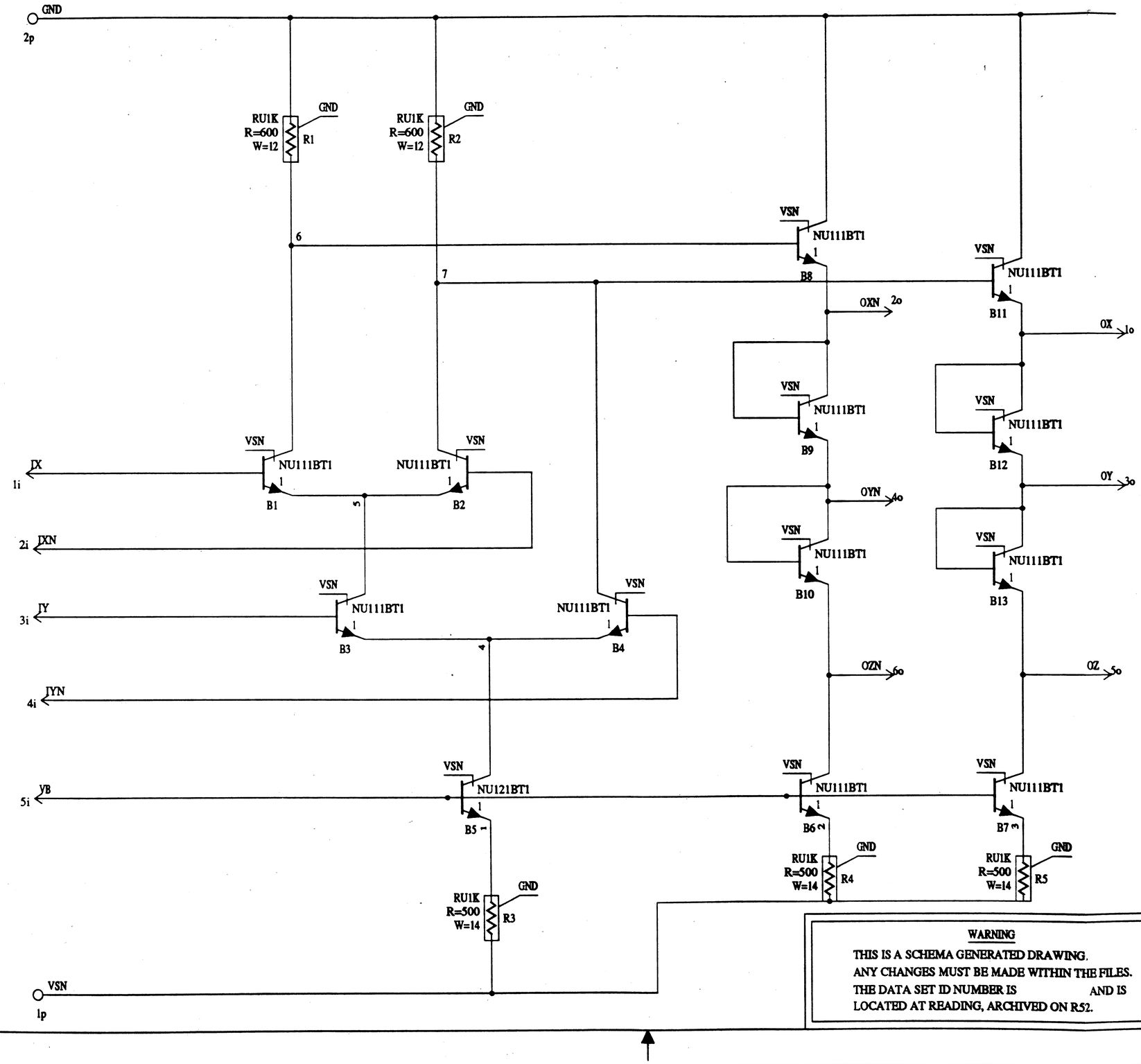
Propagation delay (ns)

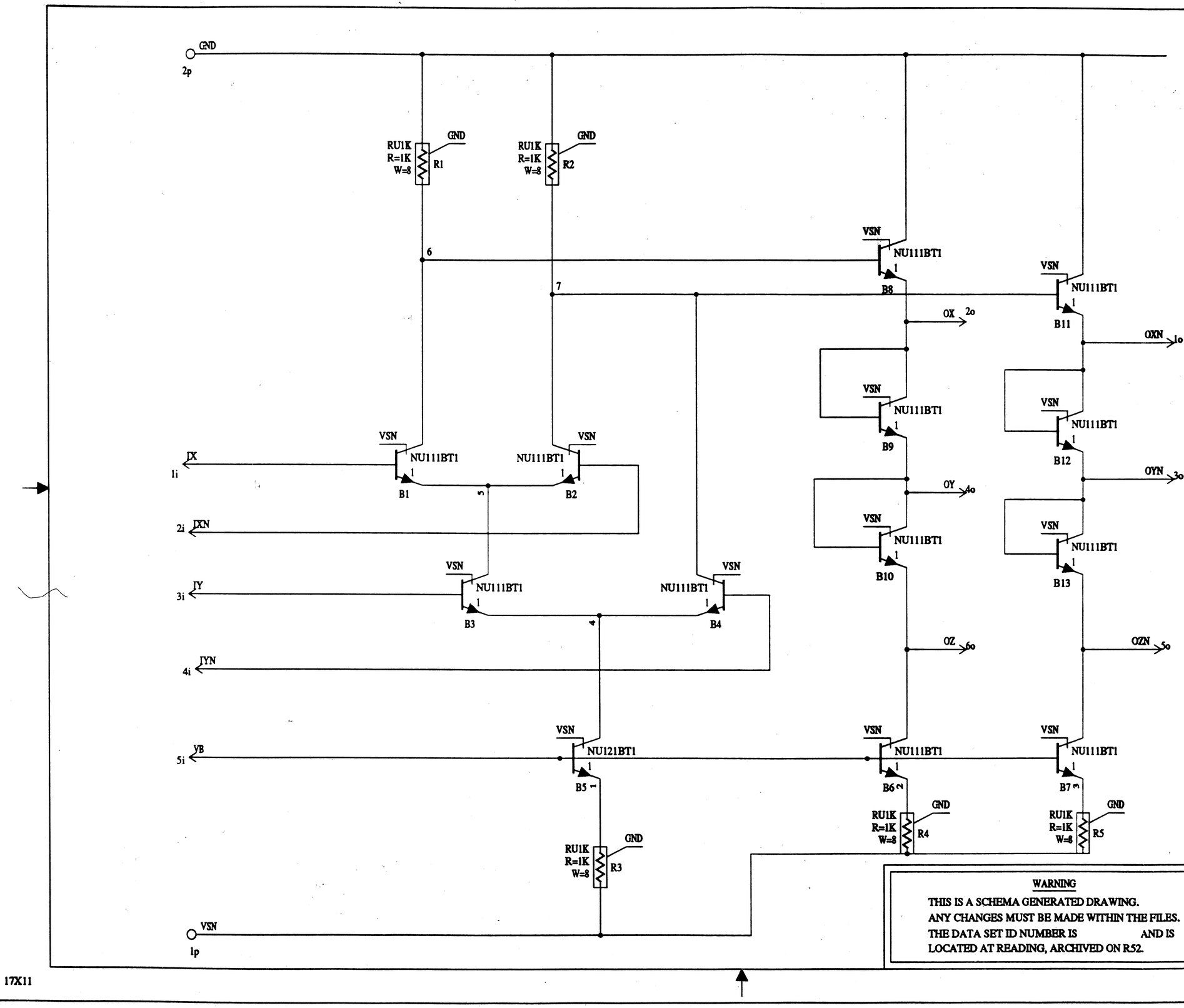
Fanout	Max	Nom	Min
1	1.1	0.7	0.5
3	1.3	0.9	0.6
5	1.6	1.0	0.7
7	1.7	1.1	0.7

Power (mW)

Max	Nom	Min
4.0	3.0	2.5


GND
2p
RU1K
R=1K
W=8
R1
R2
6
7
VSN
NU111BT1
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
NU121BT1
IX
1i
IXN
2i
IY
3i
IYN
4i
YB
5i
OXN
2o
OX
1o
OYN
4o
OY
3o
OZN
6o
OZ
5o
R3
R4
R5
1p
WARNING
THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.
ENGR DLL
DRWN MDA
July 31, 1989 ISSUE
USED ON
DRAWING
AT&T -
2 INPUT
AND GATE
(AND2.1)
DWG
SIZE
2S
SHEET
132
17X11


GND
2p
RU1K
R=600
W=12
R1
GND
RU1K
R=600
W=12
R2
GND
VSN
NU111BT1
1
B8
6
7
VSN
NU111BT1
1
B11
OXN
2o
OX
1o
VSN
NU111BT1
1
B9
VSN
NU111BT1
1
B12
OYN
4o
OY
3o
VSN
NU111BT1
1
B10
VSN
NU111BT1
1
B13
OZN
6o
OZ
5o
VSN
NU111BT1
1
B1
VSN
NU111BT1
1
B2
IX
1i
5
IXN
2i
VSN
NU111BT1
1
B3
VSN
NU111BT1
1
B4
IY
3i
4
IYN
4i
VSN
NU121BT1
1
B5
YB
5i
VSN
NU111BT1
1
B6
VSN
NU111BT1
1
B7
RU1K
R=500
W=14
R3
GND
RU1K
R=500
W=14
R4
GND
RU1K
R=500
W=14
R5
GND
VSN
1p
WARNING
THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.
ENGR DLL
DRWN MDA
Sept. 1, 1989 ISSUE
USED ON
DRAWING
AT&T -
2 INPUT
AND GATE
HIGH CURRENT
(AND2H.1)
DWG
SIZE
2S
SHEET 133
17X11



ENGR	DLL
DRWN	MDA
Nov. 16, 1989	ISSUE

NAND2.1

USED ON	DRAWING
AT&T -	

2 INPUT
NAND GATE

(NAND2.1)

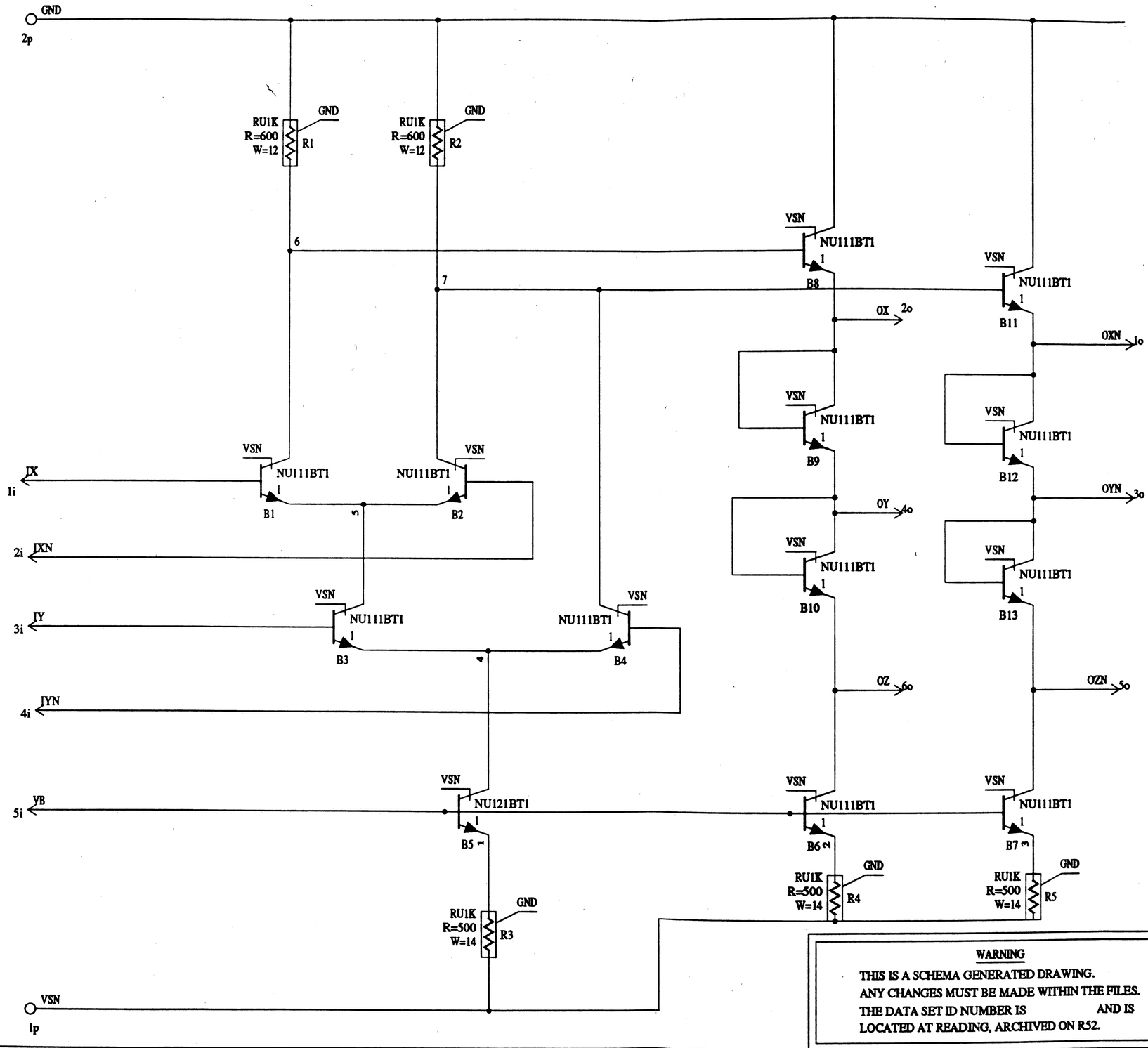
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 134

17X11



ENGR	DLL
DRWN	MDA

Dec. 13, 1989 ISSUE

NAND2H.1

USED ON	DRAWING

AT&T -

2 INPUT
NAND GATE
HIGH CURRENT
(NAND2H.1)

WARNING

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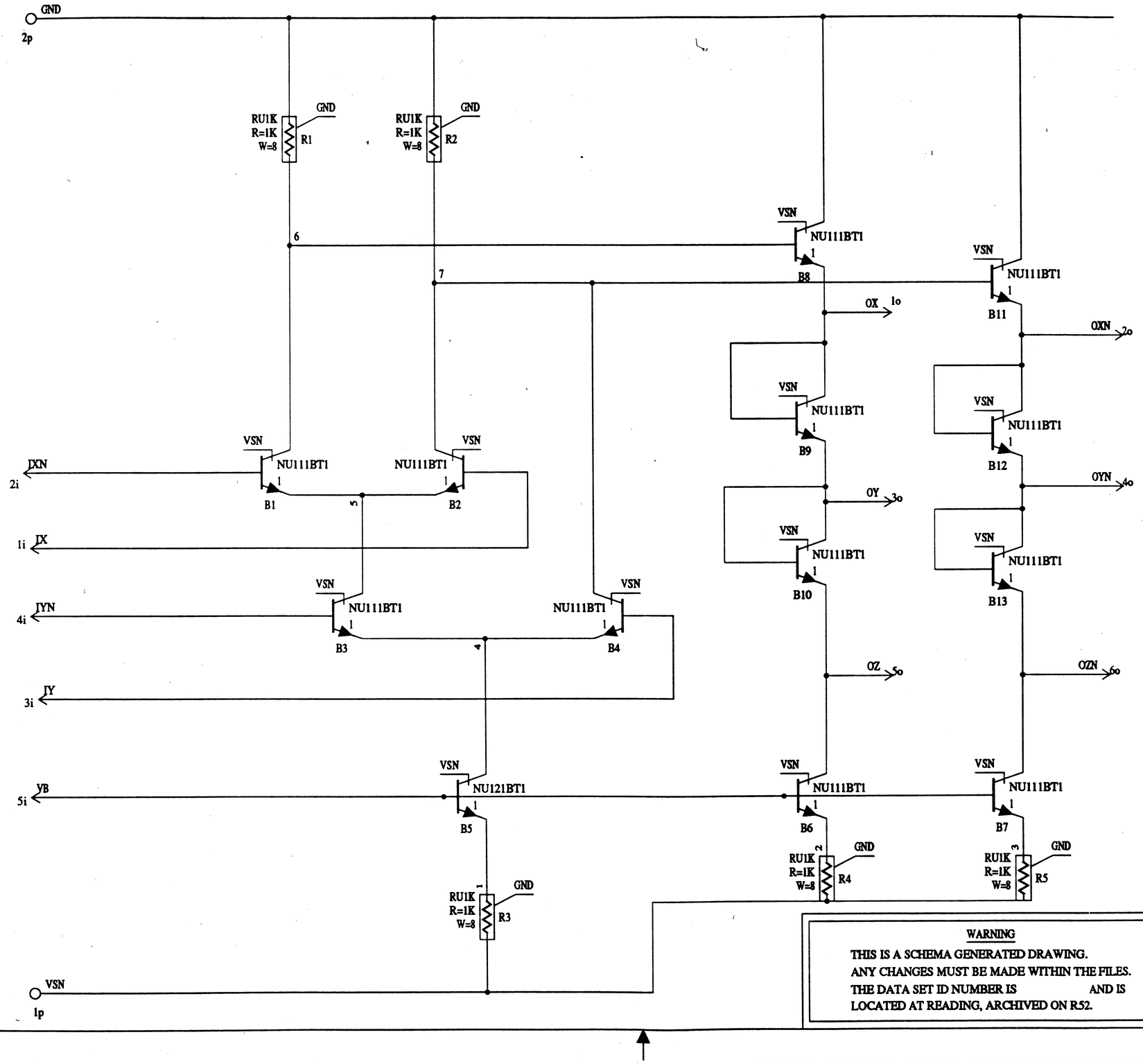
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 135

17X11



ENGR	DLL		
DRWN	MDA		
Sept. 28, 1989	ISSUE		

USED ON	DRAWING

AT&T -

2 INPUT
OR GATE

(OR2.1)

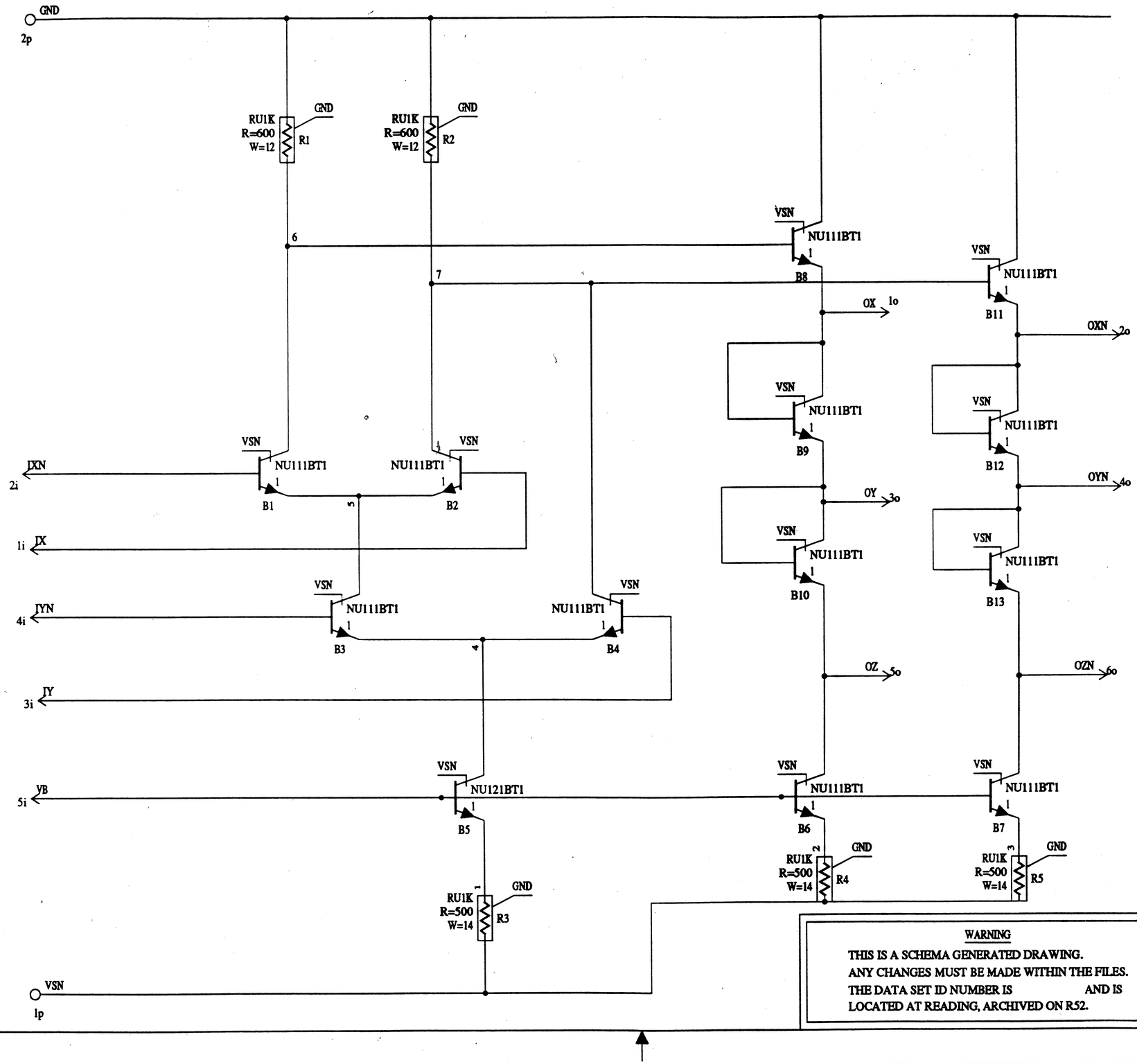
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 136

17X11



WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

ENGR	DLL		
DRWN	MDA		

Sept. 28, 1989 ISSUE

USED ON	DRAWING

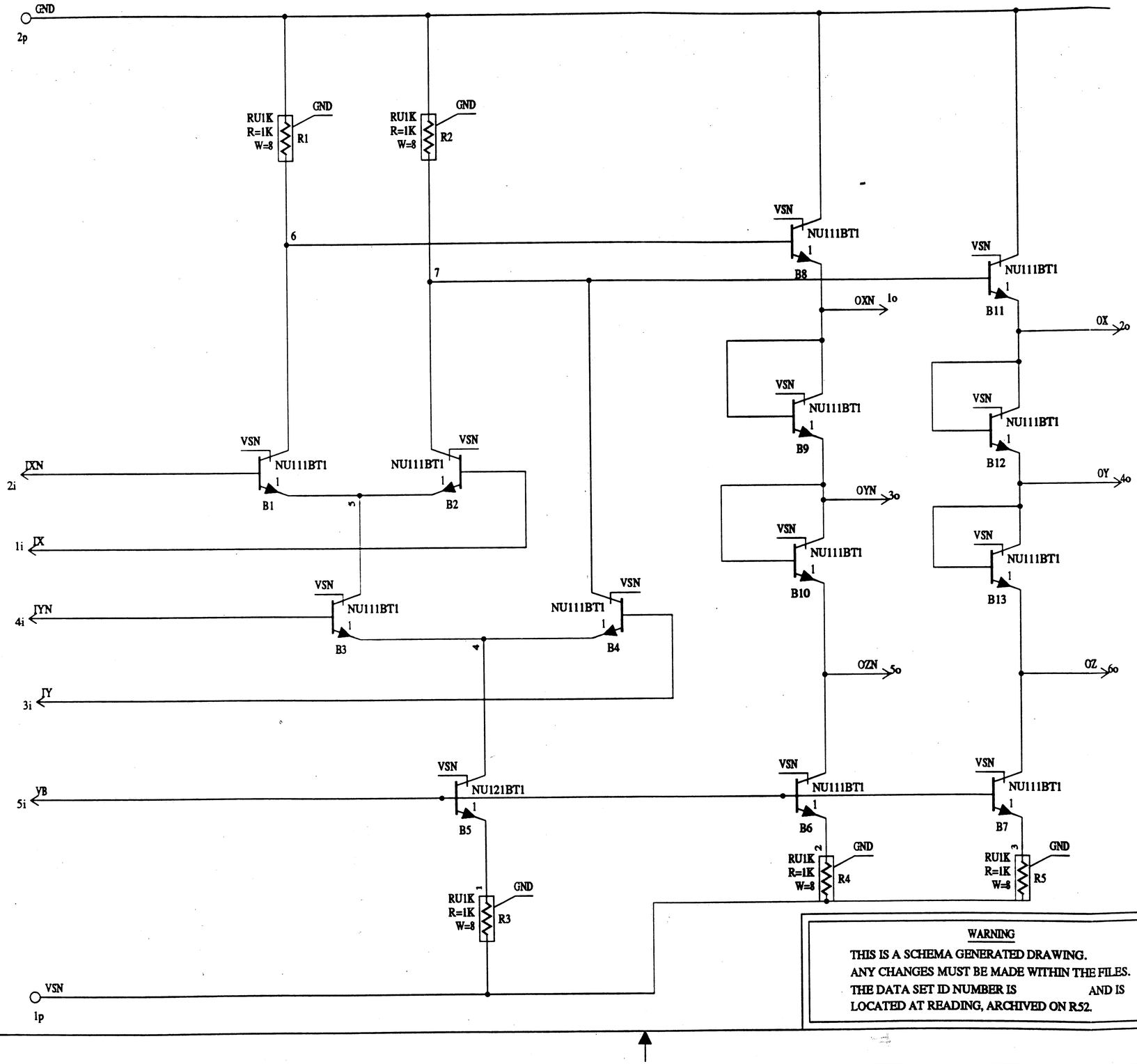
AT&T -

2 INPUT
OR GATE
HIGH MODE
(OR2H.1)

DWG SIZE
2S

SHEET 137

17X11



ENGR	DLL
DRWN	MDA
Sept. 28, 1989	ISSUE

USED ON	DRAWING
AT&T -	

2 INPUT
NOR GATE

(NOR2.1)

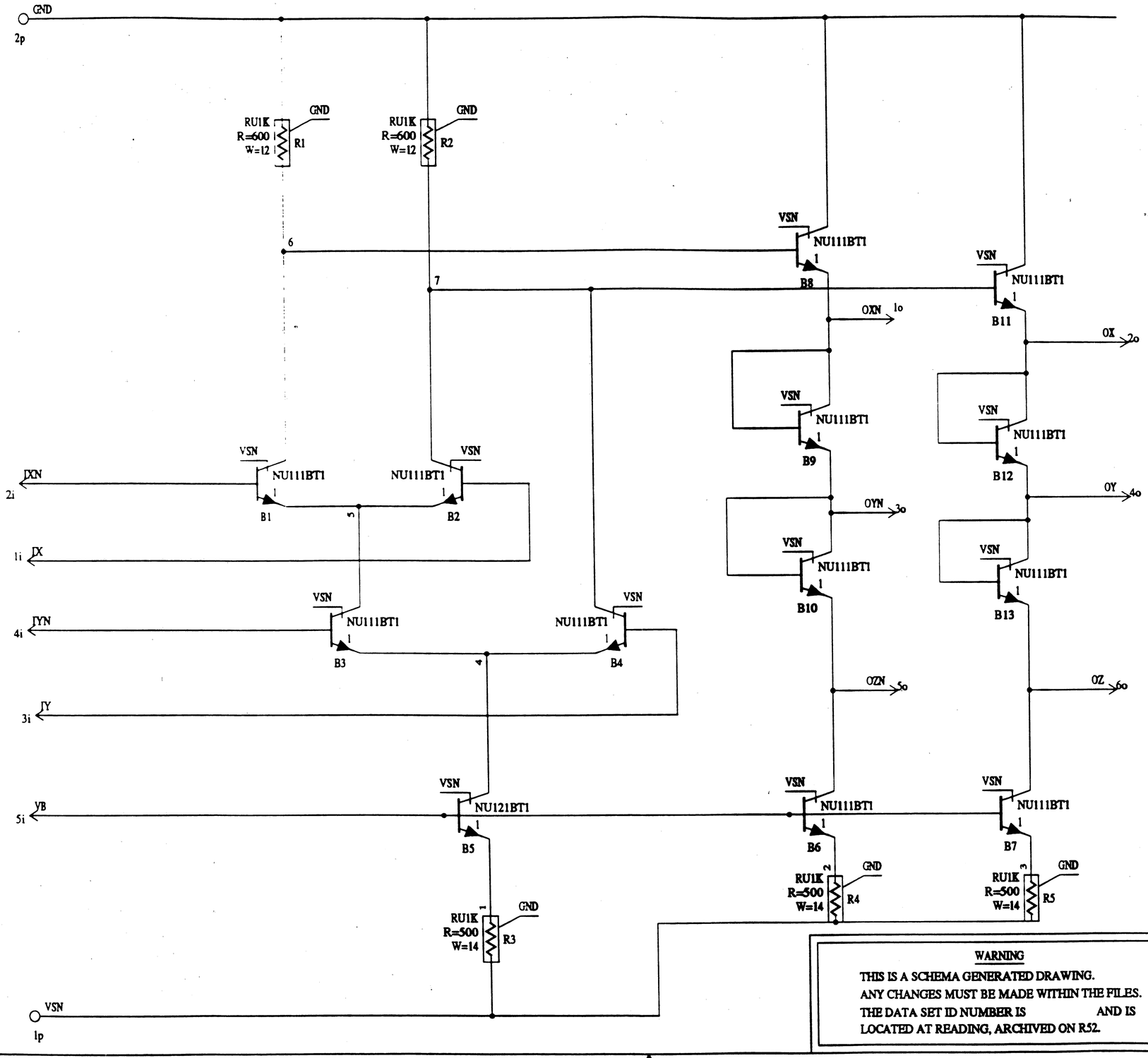
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 138

17X11



ENGR	DLL		
DRWN	MDA		
Sept. 28, 1989	ISSUE		

USED ON	DRAWING

AT&T -

2 INPUT
NOR GATE
HIGH MODE
(NOR2H.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 139

17X11

DATA SHEET FOR:
AND3, AND3H, NAND3, NAND3H, OR3, OR3H, NOR3, NOR3H

AND3:	3-input AND gate	50 MHz
AND3H:	3-input AND gate	100 MHz
NAND3:	3-input NAND gate	50 MHz
NAND3H:	3-input NAND gate	100 MHz
OR3:	3-input OR gate	50 MHz
OR3H:	3-input OR gate	100 MHz
NOR3:	3-input NOR gate	50 MHz
NOR3H:	3-input NOR gate	100 MHz

All of the gates have an area of 135 um X 310 um.

AND3, NAND3, OR3, NOR3:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.7	1.1	0.7
3	2.0	1.3	0.8
5	2.3	1.5	0.9
7	2.6	1.7	1.0

Power (mW)

Max	Nom	Min
2.4	1.8	1.5

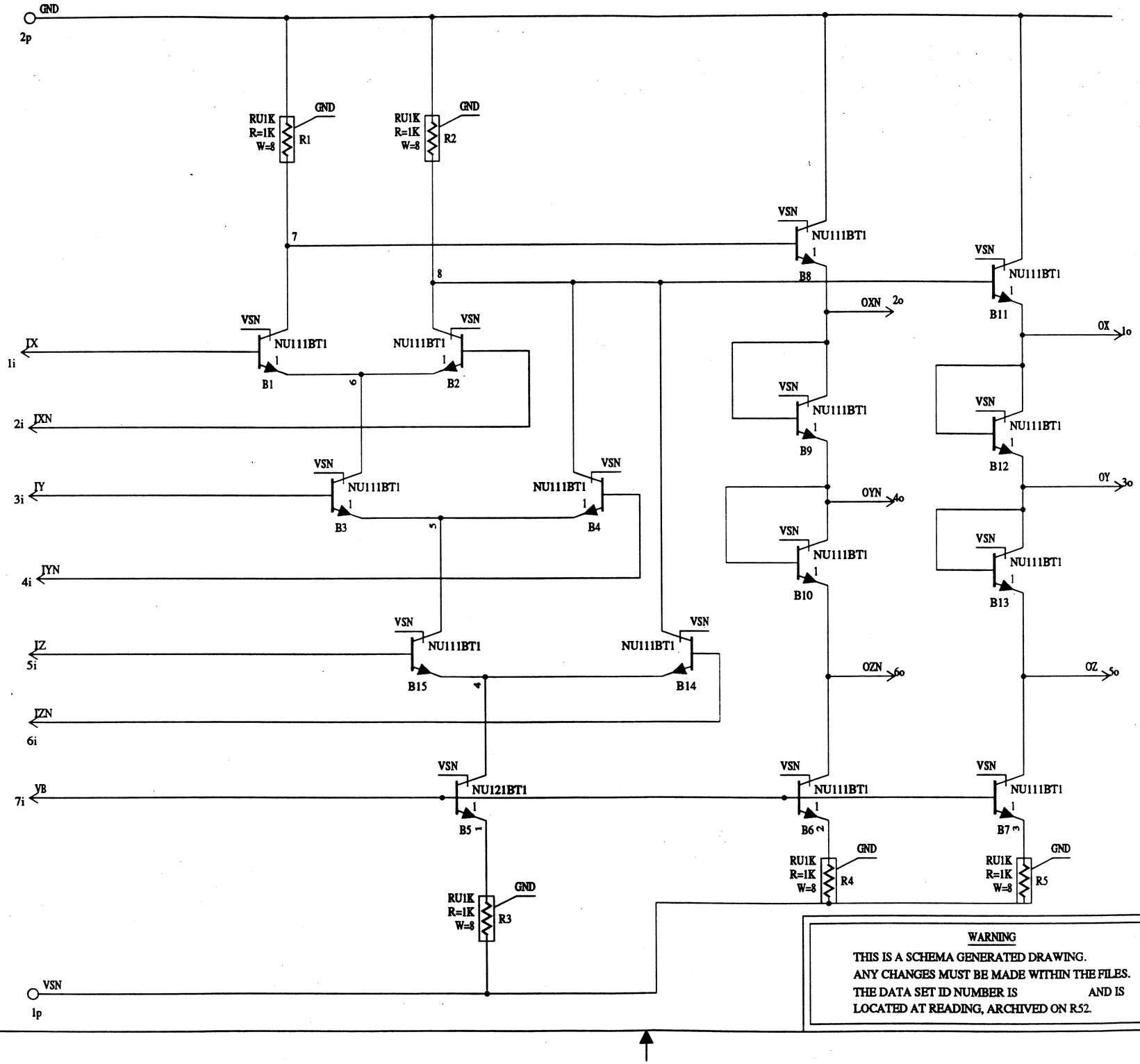
AND3H, NAND3H, OR3H, NOR3H:

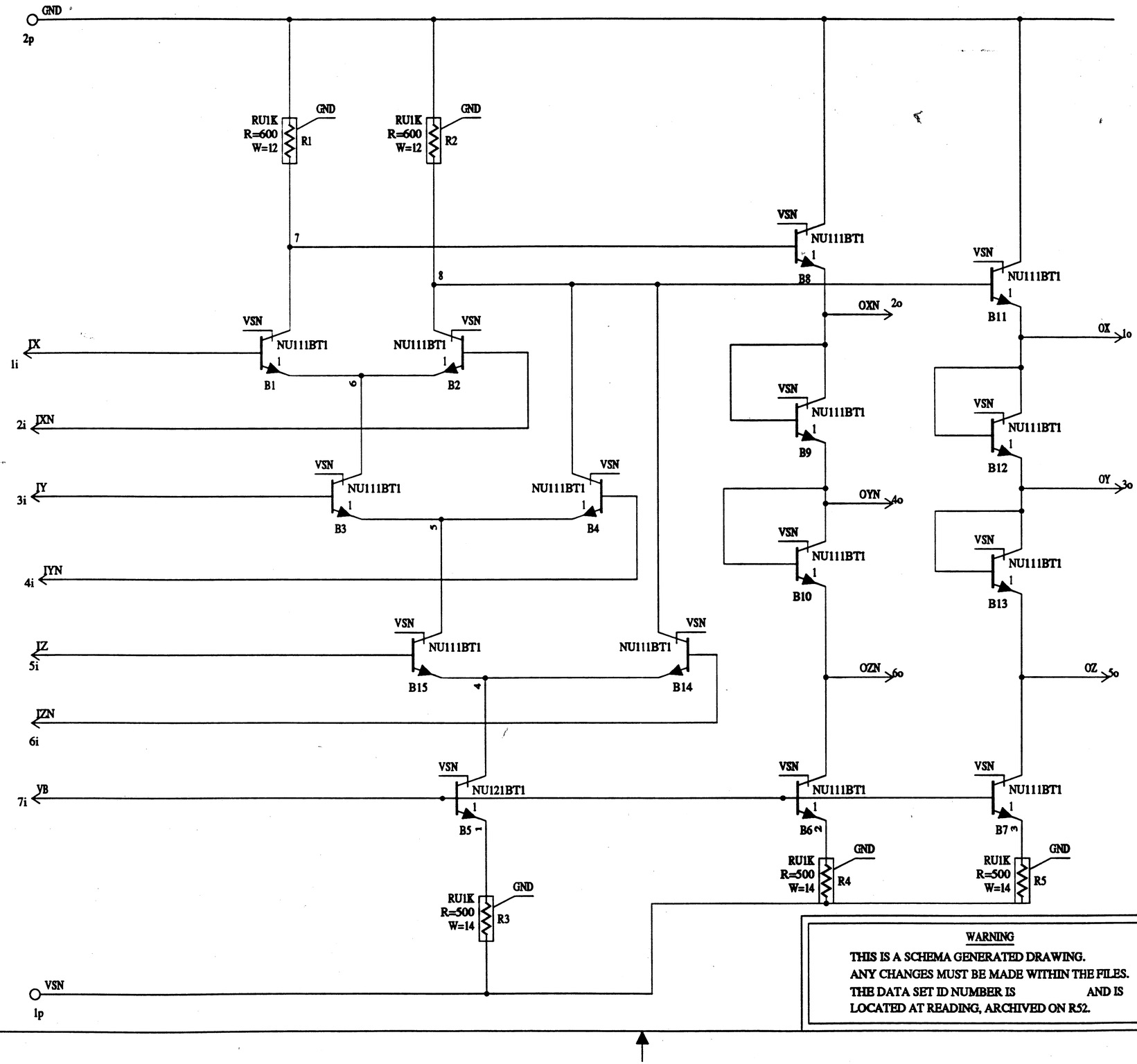
Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.2	0.8	0.5
3	1.4	0.9	0.6
5	1.6	1.1	0.7
7	(overloaded)		

Power (mW)

Max	Nom	Min
4.0	3.0	2.5


GND
2p
RU1K
R=1K
W=8
R1
R2
7
8
VSN
NU111BT1
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
NU121BT1
IX
1i
IXN
2i
IY
3i
IYN
4i
IZ
5i
IZN
6i
YB
7i
OXN
2o
OX
1o
OYN
4o
OY
3o
OZN
6o
OZ
5o
R3
R4
R5
1p
WARNING
THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.
ENGR DLL
DRWN MDA
July 31,1989 ISSUE
USED ON DRAWING
AT&T -
3 INPUT
AND GATE
(AND3.1)
DWG
SIZE
2S
SHEET 141
17X11



ENGR	DLL
DRWN	MDA
Sept. 5, 1989	ISSUE

USED ON	DRAWING

AT&T -

3 INPUT
AND GATE
HIGH CURRENT
(AND3H.1)

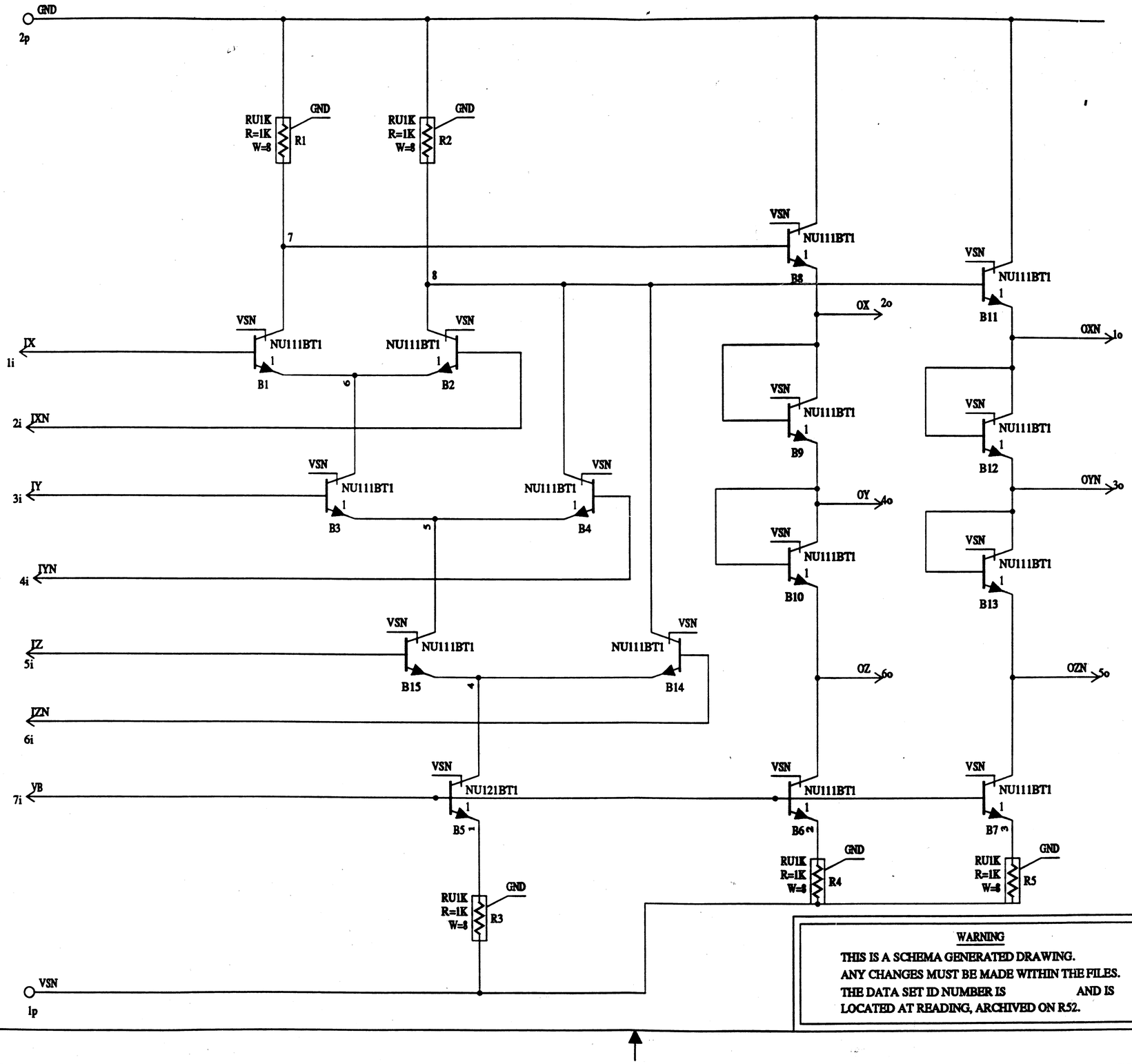
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 142

17X11



ENGR	DLL
DRWN	MDA
Sept. 28, 1989	ISSUE

USED ON	DRAWING
AT&T -	

3 INPUT
NAND GATE

(NAND3.1)

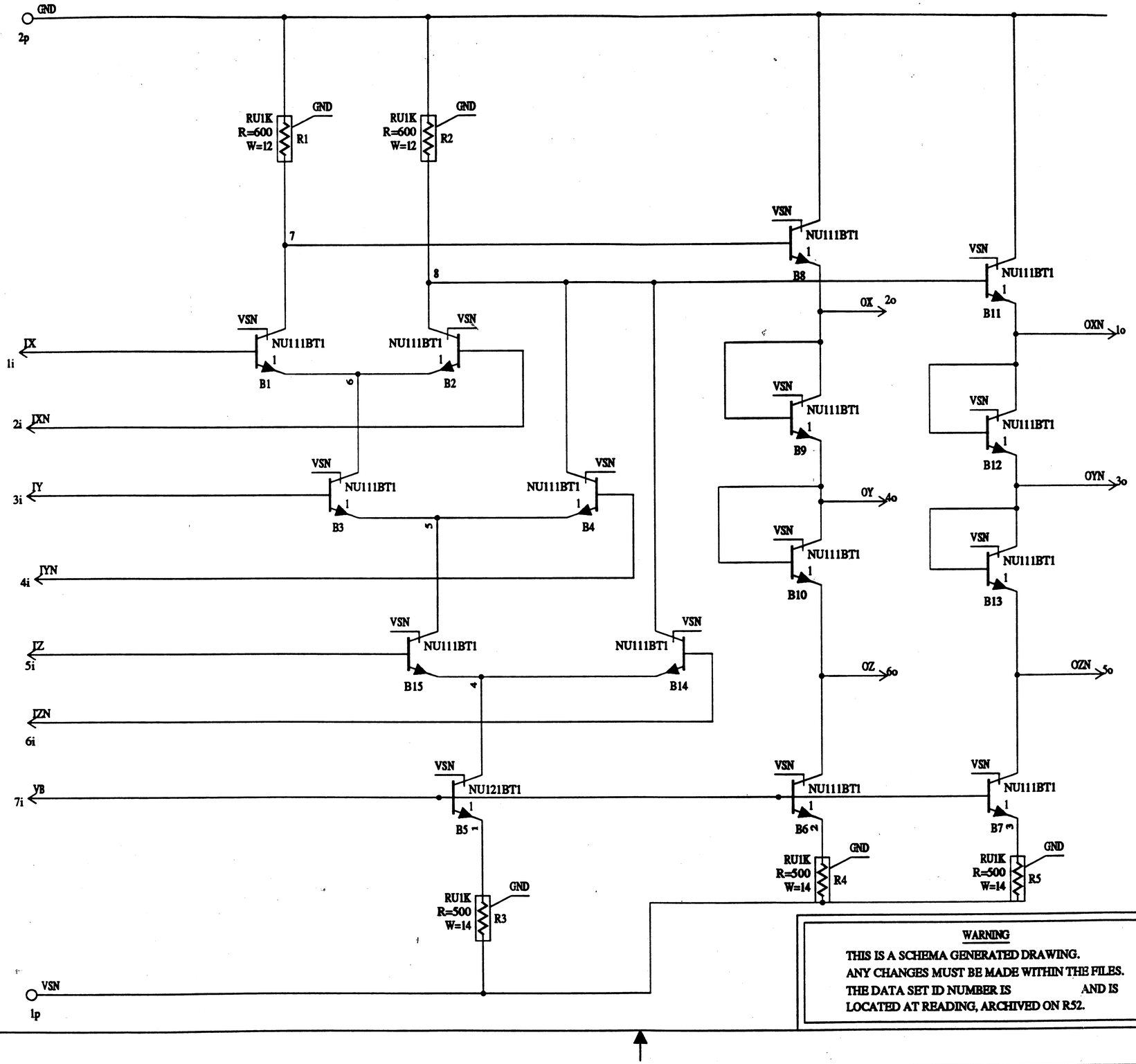
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 143

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

	NAND3H.1
USED ON	DRAWING

AT&T -

3 INPUT
NAND GATE
HIGH CURRENT
(NAND3H.1)

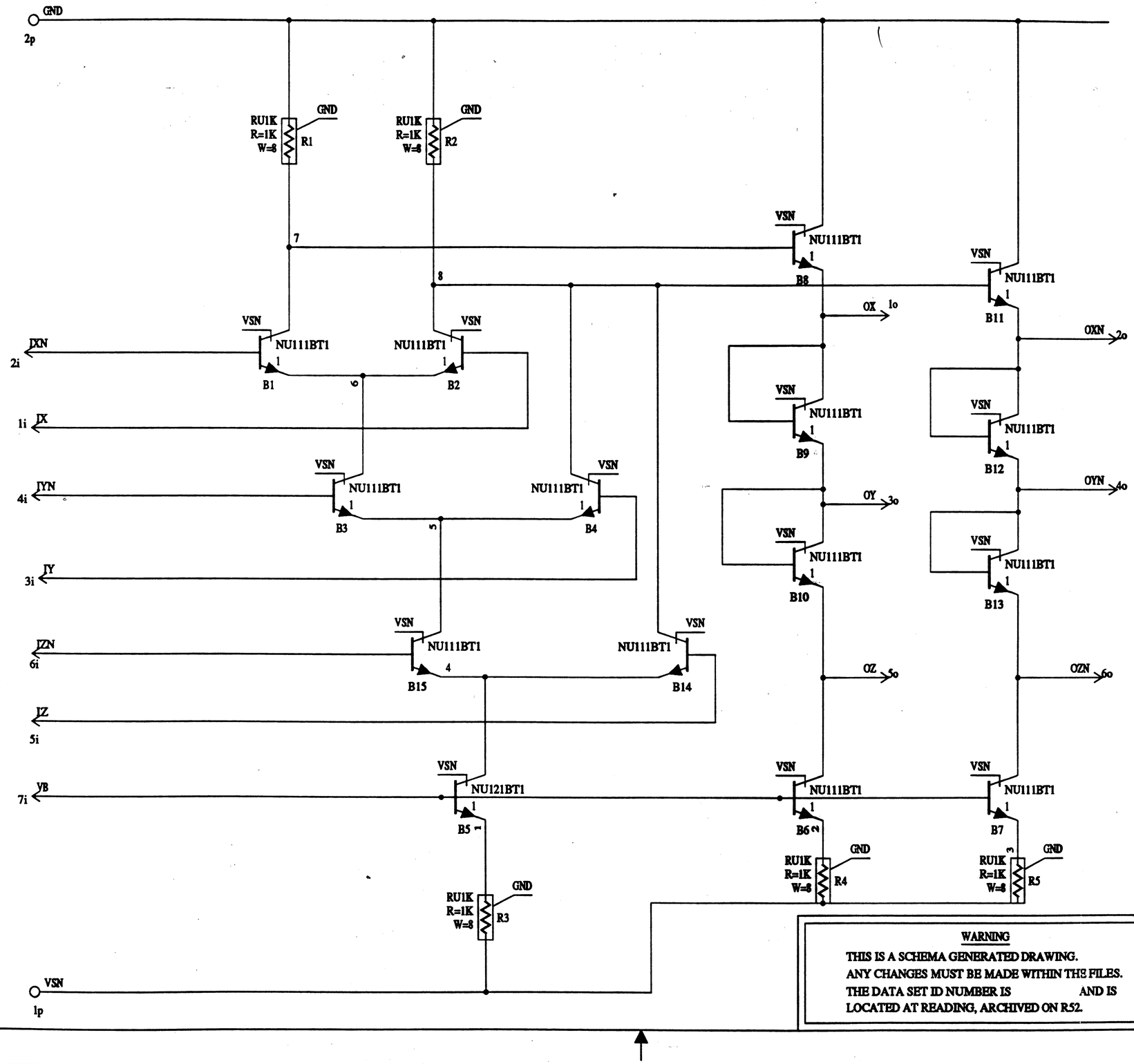
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 144

17X11



WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

ENGR	DLL		
DRWN	MDA		

Nov. 16, 1989 ISSUE

	OR3.1
USED ON	DRAWING

AT&T -

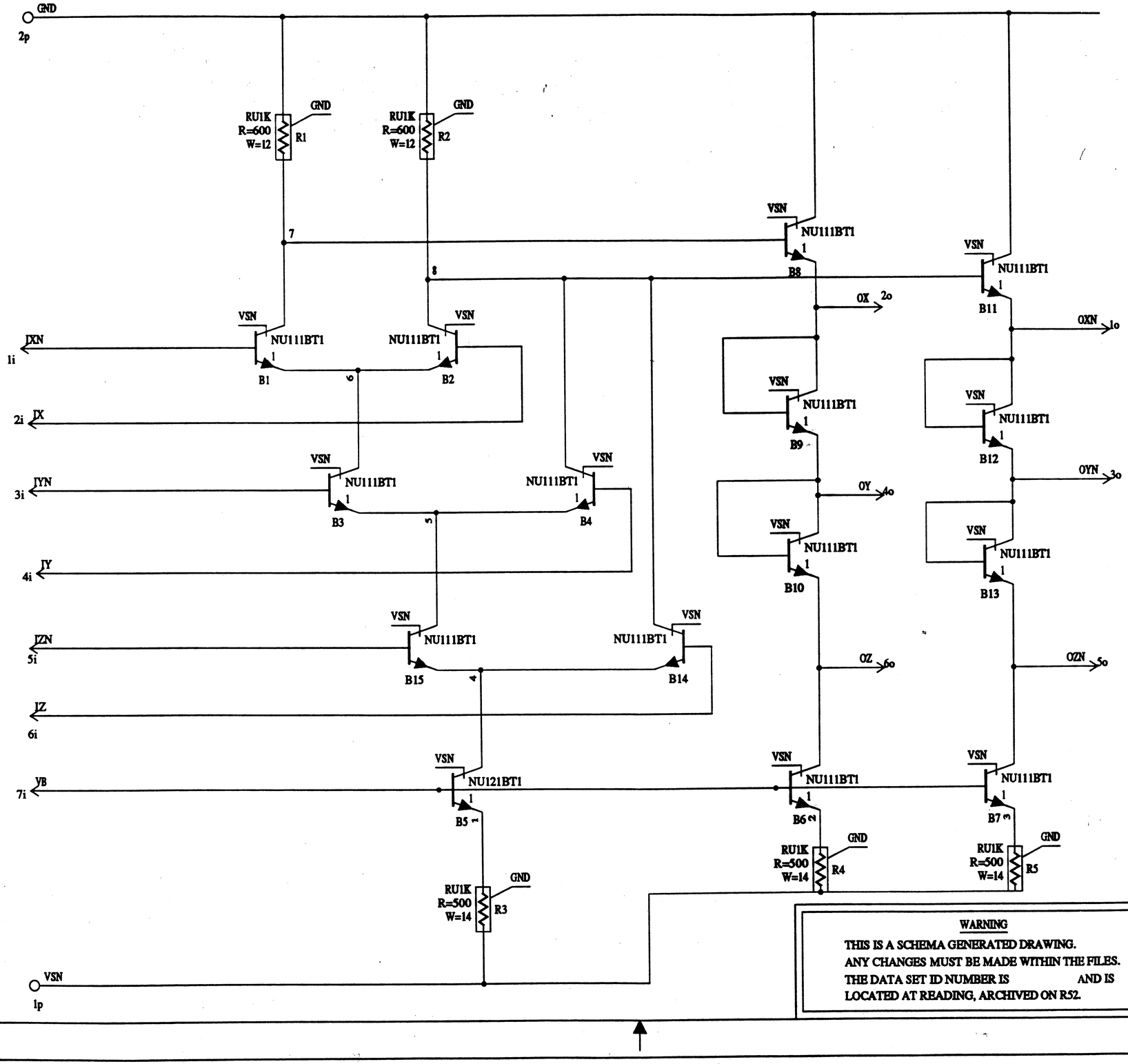
3 INPUT
OR GATE

(OR3.1)

DWG SIZE 2S

SHEET 145

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

OR3H.1

USED ON	DRAWING
AT&T -	

3 INPUT
OR GATE
HIGH CURRENT
(OR3H.1)

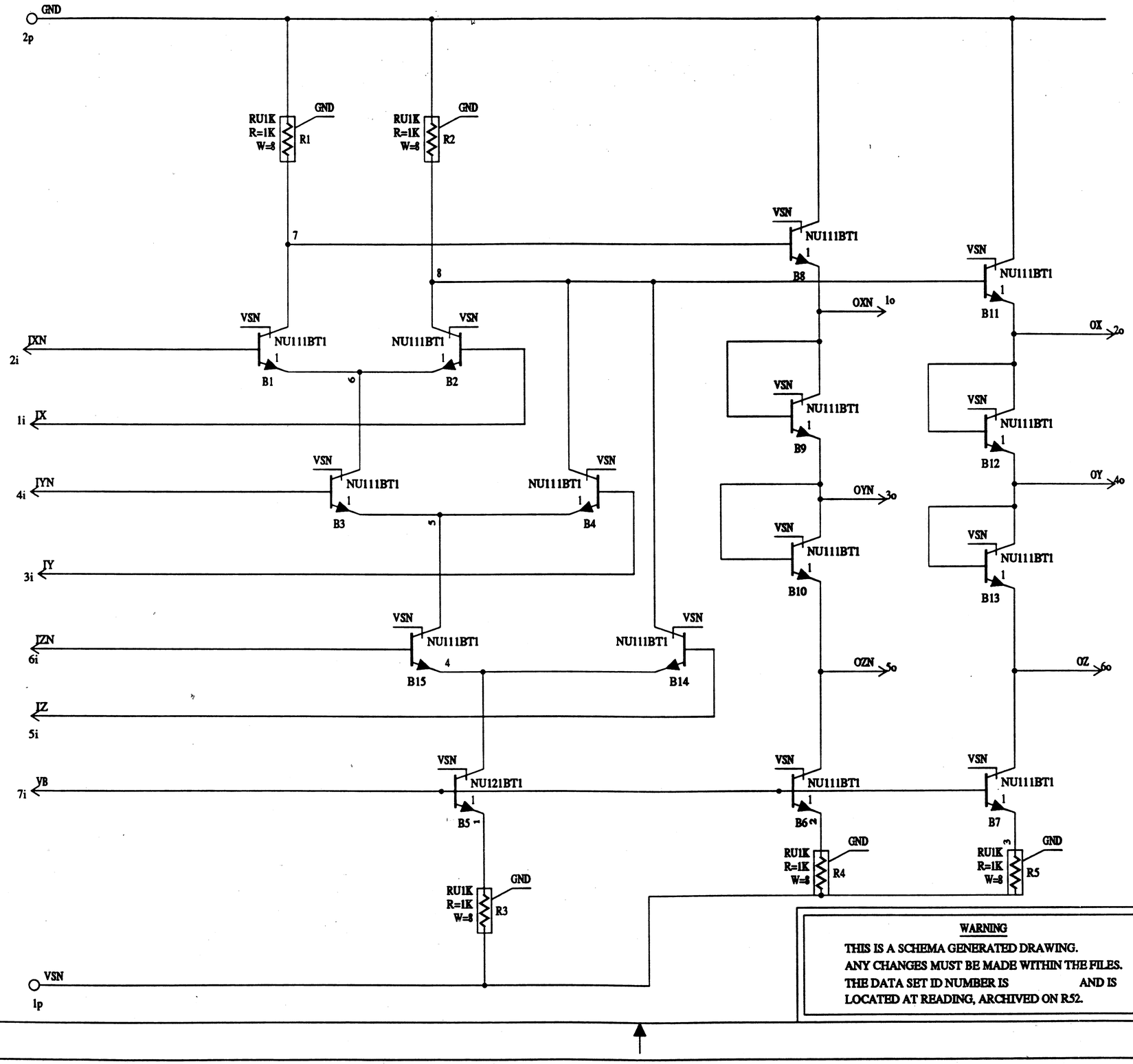
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 146

17X11



ENGR	DLL
DRWN	MDA
Nov. 16, 1989	ISSUE

	NOR3.1
USED ON	DRAWING

AT&T -

3 INPUT
NOR GATE

(NOR3.1)

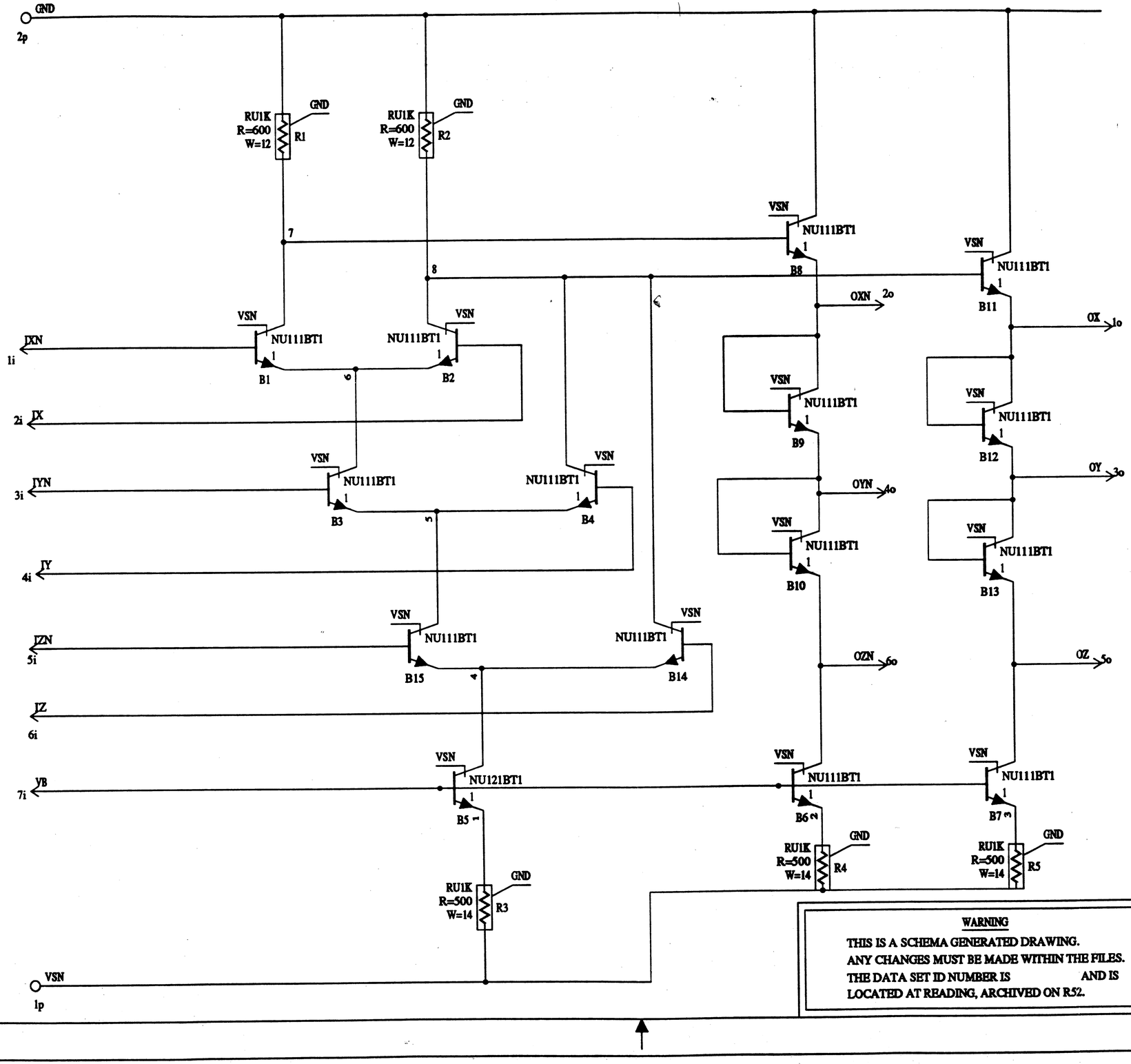
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 147

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

NOR3H.1

USED ON	DRAWING
AT&T -	

3 INPUT
NOR GATE
HIGH CURRENT
(NOR3H.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 148

17X11

DATA SHEET FOR: MUX2, MUX2H

MUX2:	2:1 Multiplexer	50 MHz
MUX2H:	2:1 Multiplexer	100 MHz

Both of the gates have an area of 135 um X 310 um.

MUX2:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.9	1.2	0.9
3	2.2	1.4	0.9
5	2.4	1.6	1.0
7	2.8	1.7	1.1

Power (mW)

Max	Nom	Min
2.4	1.8	1.5

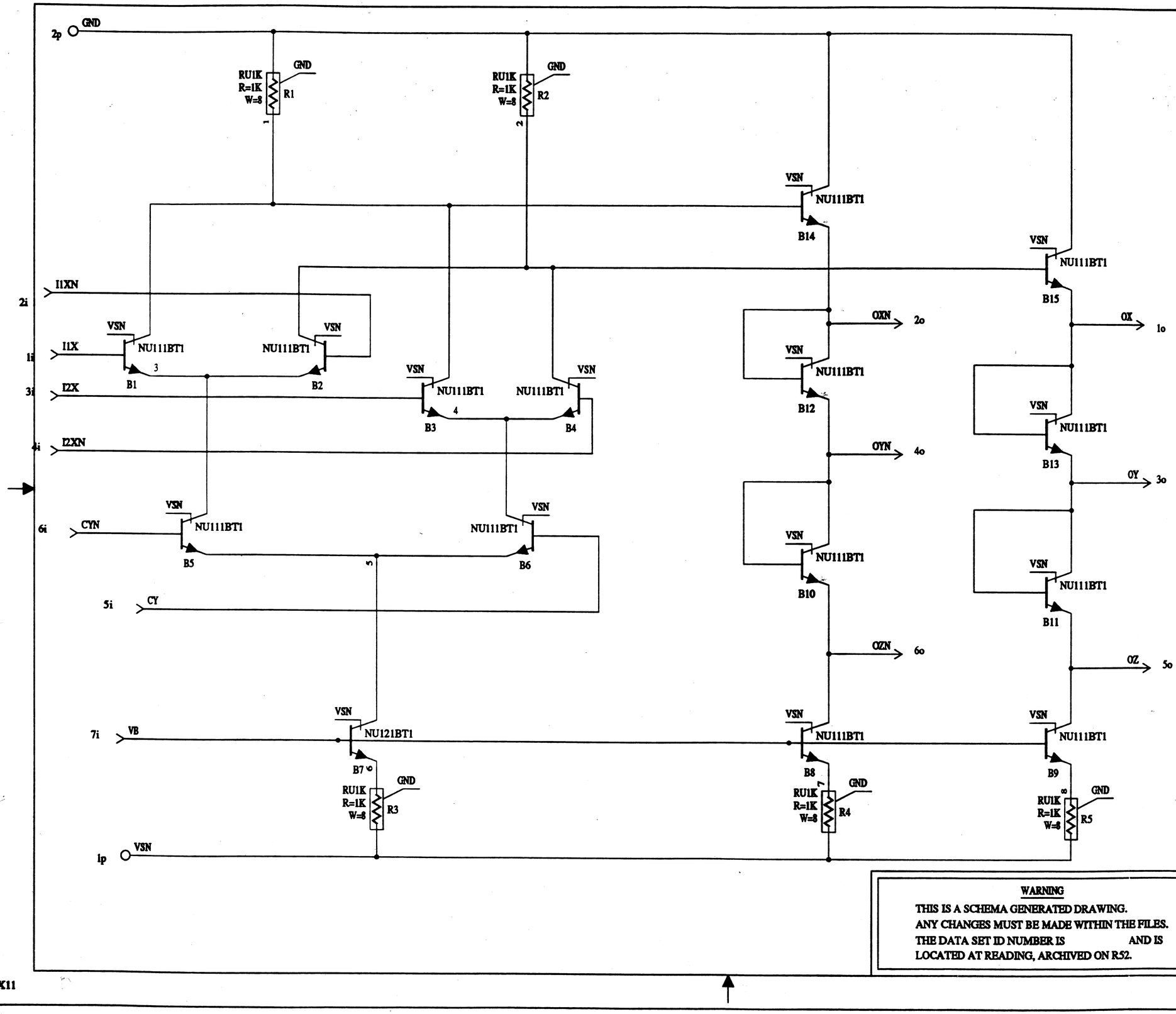
MUX2H:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.4	1.0	0.7
3	1.6	1.0	0.8
5	1.8	1.2	0.9
7	2.0	1.3	0.9

Power (mW)

Max	Nom	Min
4.0	3.0	2.4



ENGR	DLL
DRWN	MDA

Sept. 22, 1989 ISSUE

USED ON	DRAWING
AT&T -	

MULTIPLEXER CIRCUIT

(MUX2.1)

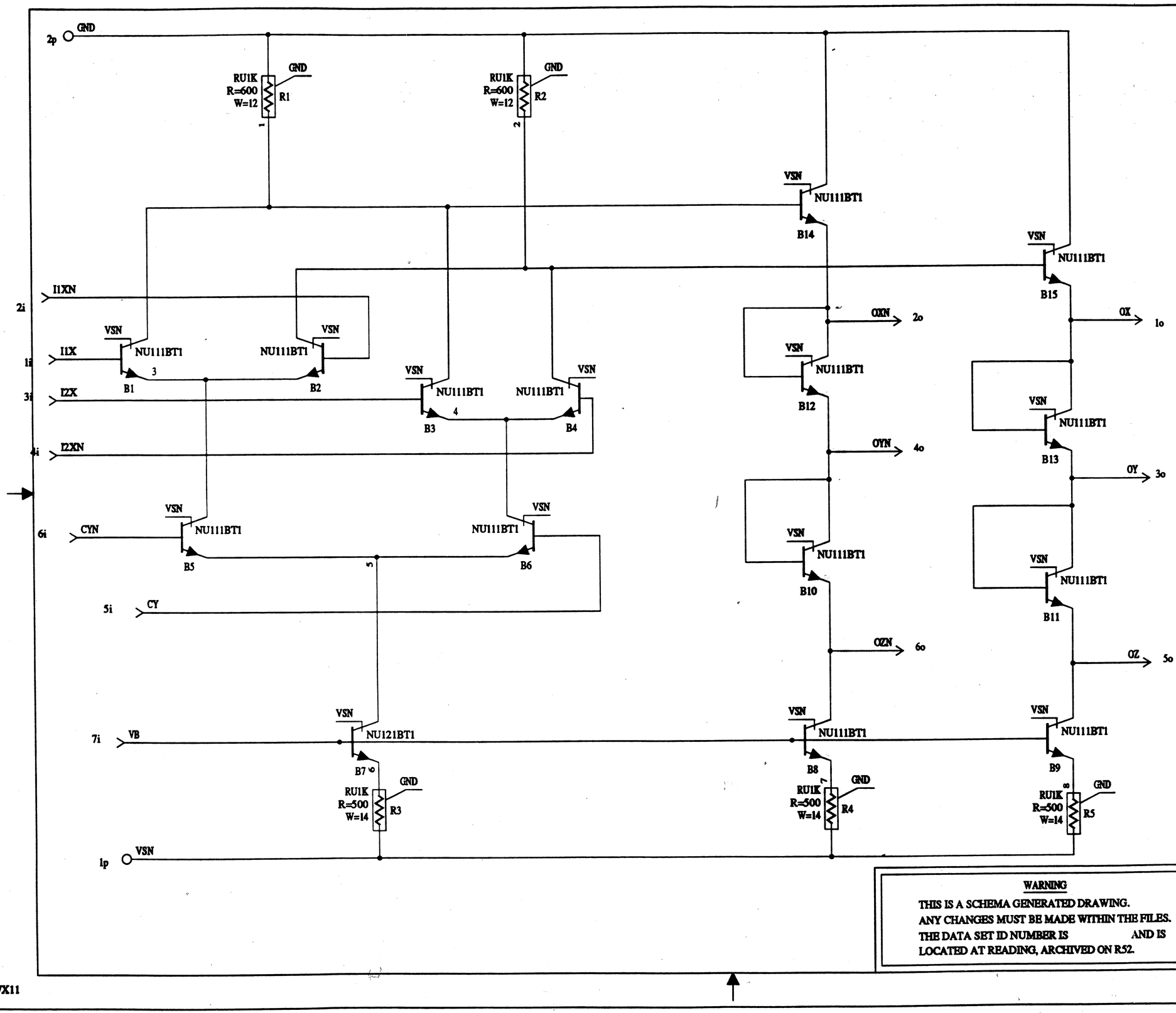
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 150

17X11



ENGR	DLL
DRWN	MDA

Sept. 22, 1989 ISSUE

USED ON	DRAWING

AT&T -

MULTIPLEXER
CIRCUIT
HIGH CURRENT
(MUX2H.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 151

17X11

DATA SHEET FOR: DEL1, DEL1XY, DEL1L, DEL1LXY, INV1, INV1XY

DEL1:	Non-inverting buffer	50 MHz
DEL1XY:	Non-inverting buffer, X&Y levels only	50 MHz
DEL1L:	Non-inverting buffer, low current	25 MHz
DEL1LXY:	Non-inverting buffer, X&Y levels only	25 MHz
INV1:	Inverter	50 MHz
INV1XY:	Inverter, X&Y levels only	50 MHz

Area for DEL1, DEL1L, INV1: 120 um X 310 um
Area for DEL1XY, DEL1LXY, INV1XY: 105 um X 310 um

DEL1, DEL1XY, INV1, INV1XY (fanout = 1):

Propagation delay for 1 gate (ns)

Max	Nom	Min
1.4	0.9	0.6

Propagation delay for 3 gates in series (ns)

Max	Nom	Min
5.4	3.5	2.3

Maximum Power: 2.6 mW

DEL1L, DEL1LXY (fanout = 1):

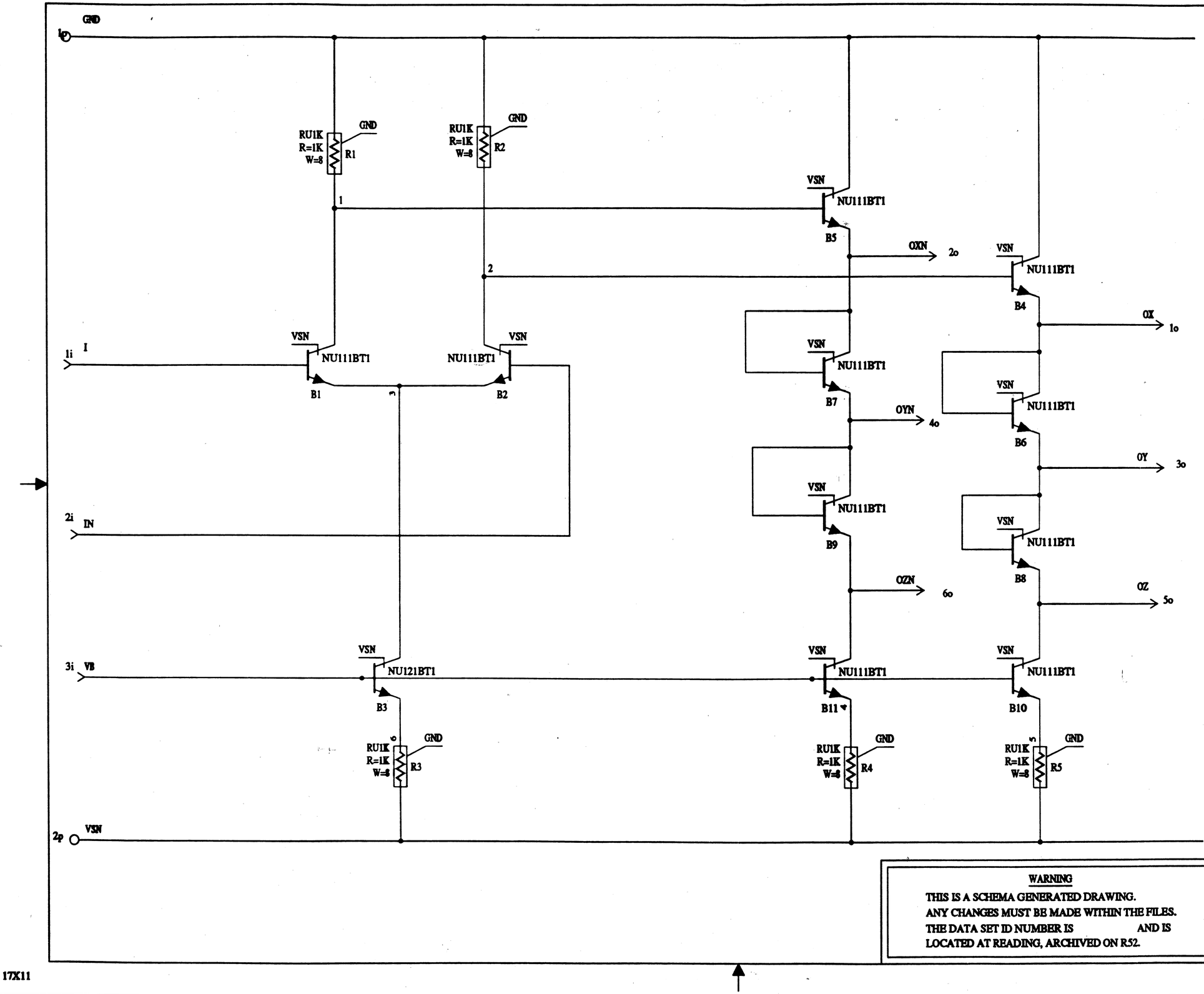
Propagation delay for 1 gate (ns)

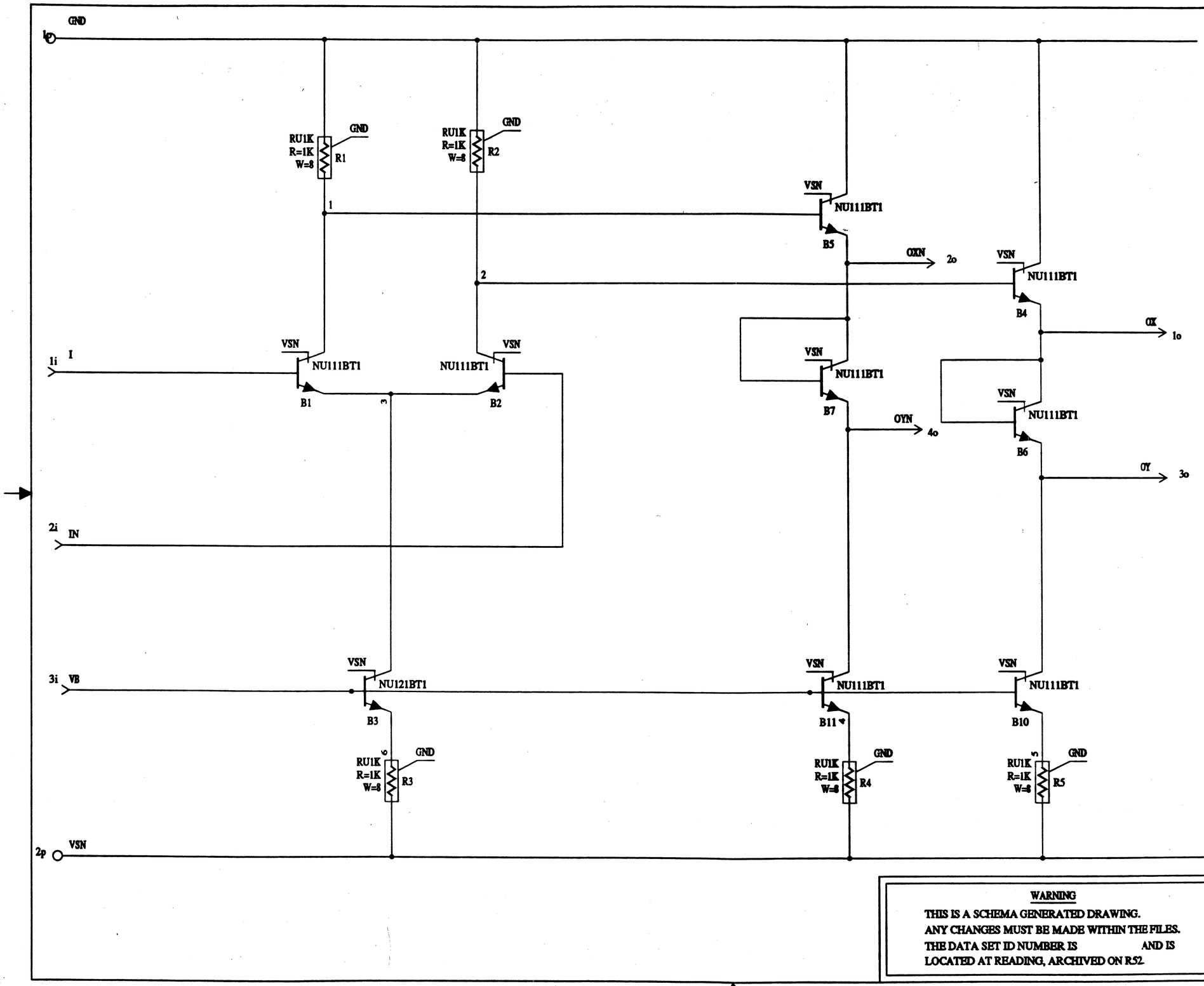
Max	Nom	Min
1.6	1.0	0.6

Propagation delay for 3 gates in series (ns)

Max	Nom	Min
5.8	3.7	2.3

Maximum Power: 1.6 mW


GND
1p
RU1K
R=1K
W=8
R1
GND
RU1K
R=1K
W=8
R2
GND
1
2
VSN
NU111BT1
B5
OXN
2o
VSN
NU111BT1
B4
OX
1o
1i I
VSN
NU111BT1
B1
VSN
NU111BT1
B2
VSN
NU111BT1
B7
OYN
4o
VSN
NU111BT1
B6
OY
3o
VSN
NU111BT1
B9
VSN
NU111BT1
B8
OZN
6o
OZ
5o
2i IN
3i VB
VSN
NU121BT1
B3
VSN
NU111BT1
B11
VSN
NU111BT1
B10
6
RU1K
R=1K
W=8
R3
GND
RU1K
R=1K
W=8
R4
5
RU1K
R=1K
W=8
R5
GND
2p VSN
WARNING
THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.
DWG SIZE
2S
SHEET 153
17X11
ENGR DLL
DRWN MDA
August 18, 1989 ISSUE
USED ON
DRAWING
AT&T -
DELAY
GATE
(DEL1.1)



ENGR	DLL		
DRWN	MDA		

August 18, 1989 ISSUE

USED ON	DRAWING
AT&T -	

DELAY
GATE

(DEL1XY.1)

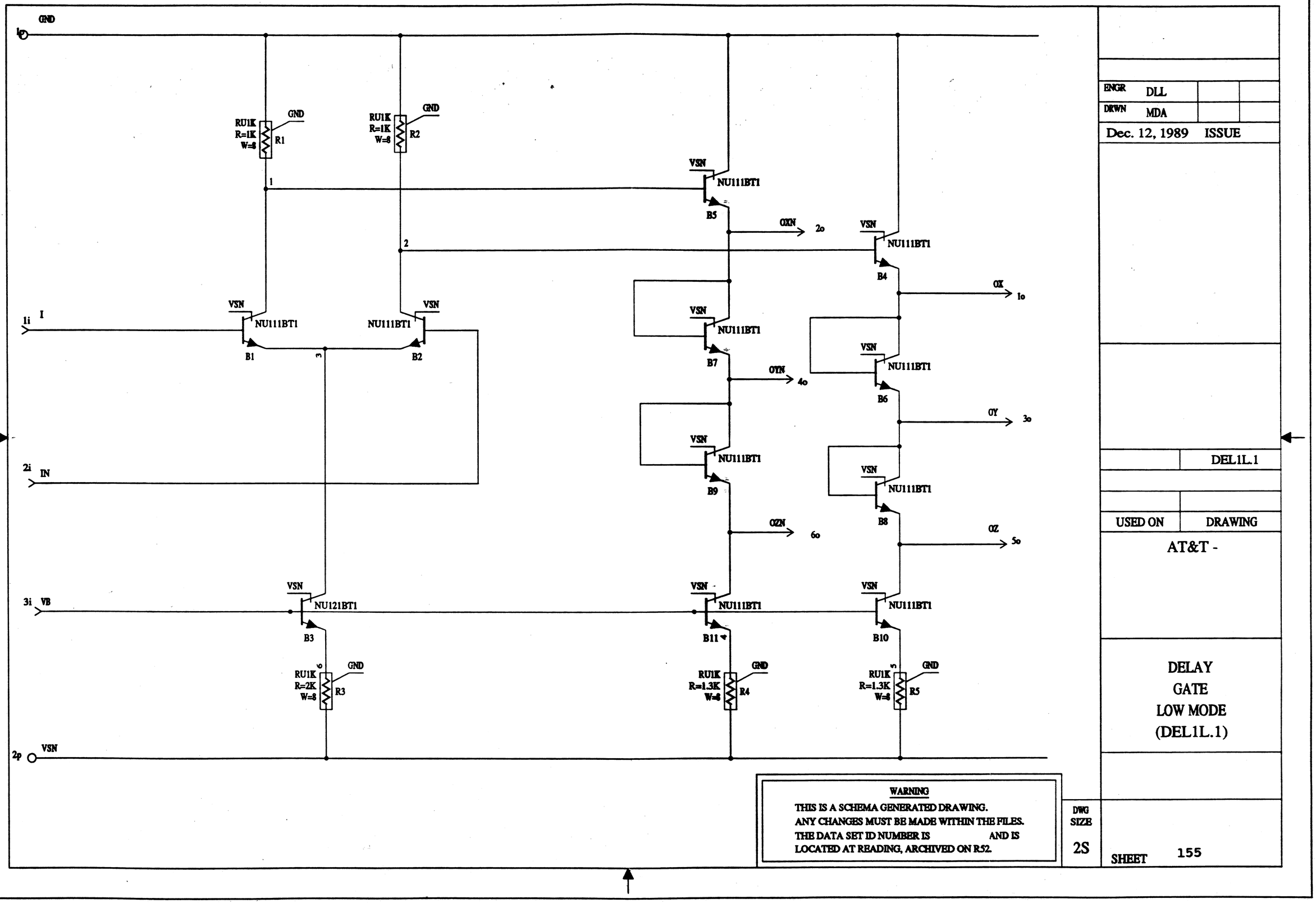
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 154

17X11



ENGR	DLL		
DRWN	MDA		
Dec. 12, 1989	ISSUE		

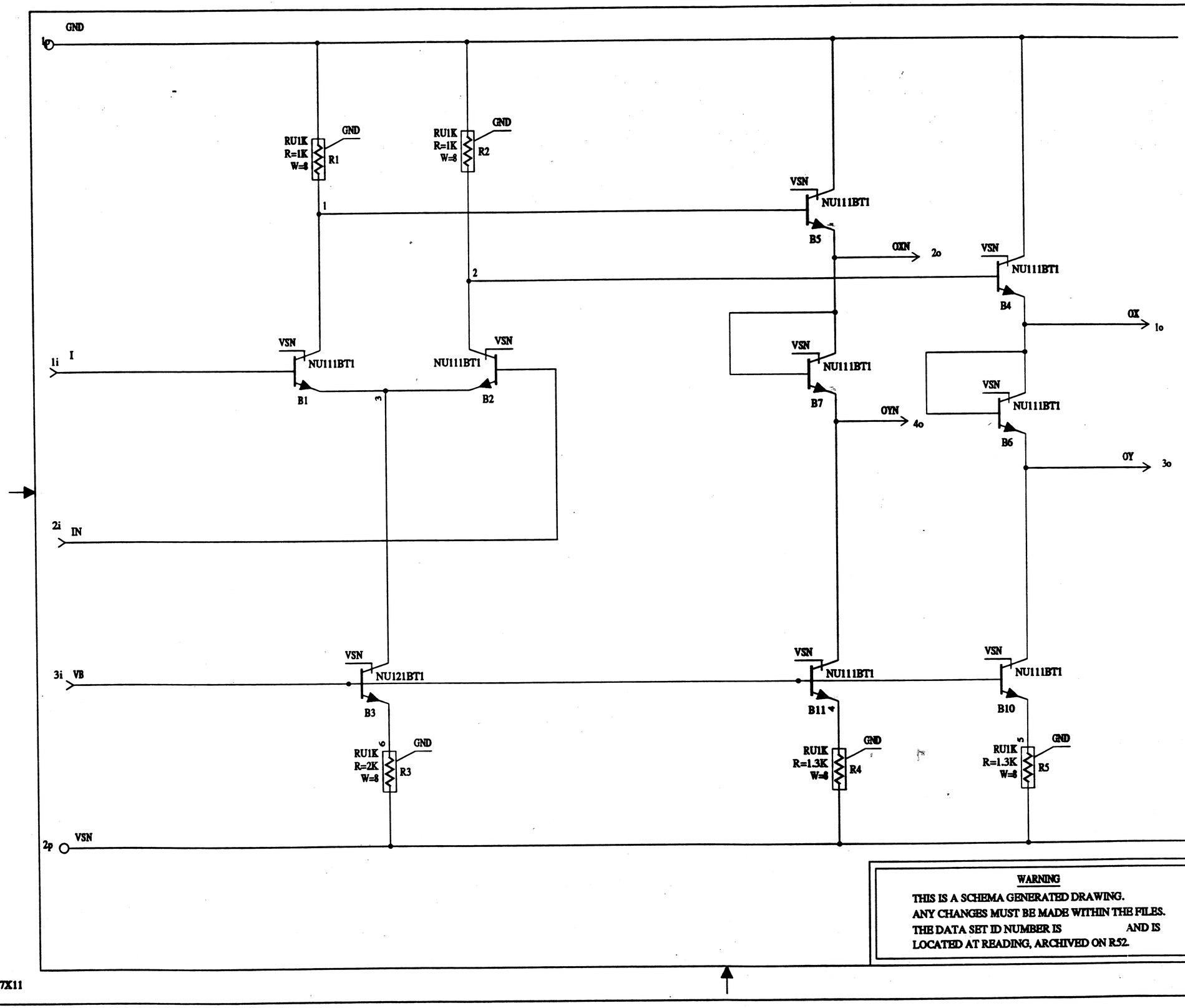
DEL1L.1

USED ON	DRAWING
AT&T -	

DELAY
GATE
LOW MODE
(DEL1L.1)

DWG SIZE
2S

SHEET 155



ENGR	DLL
DRWN	MDA
Dec. 12, 1989	ISSUE

	DEL1LXY.1
USED ON	DRAWING

AT&T -

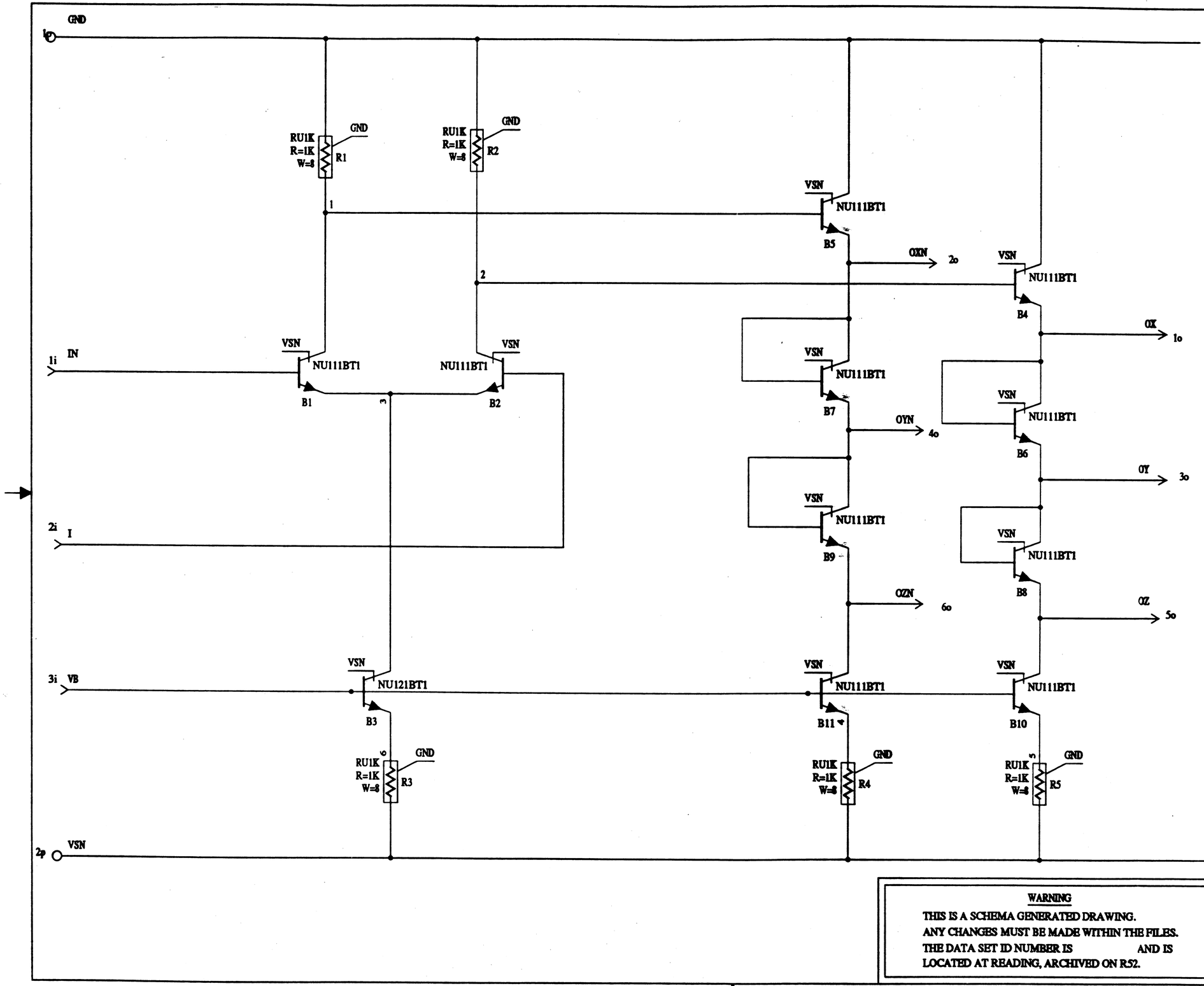
DELAY
GATE
LOW MODE
(DEL1LXY.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 156



ENGR	DLL
DRWN	MDA
June 30, 1989	ISSUE

USED ON	DRAWING
AT&T -	

INVERTER

(INV1.1)

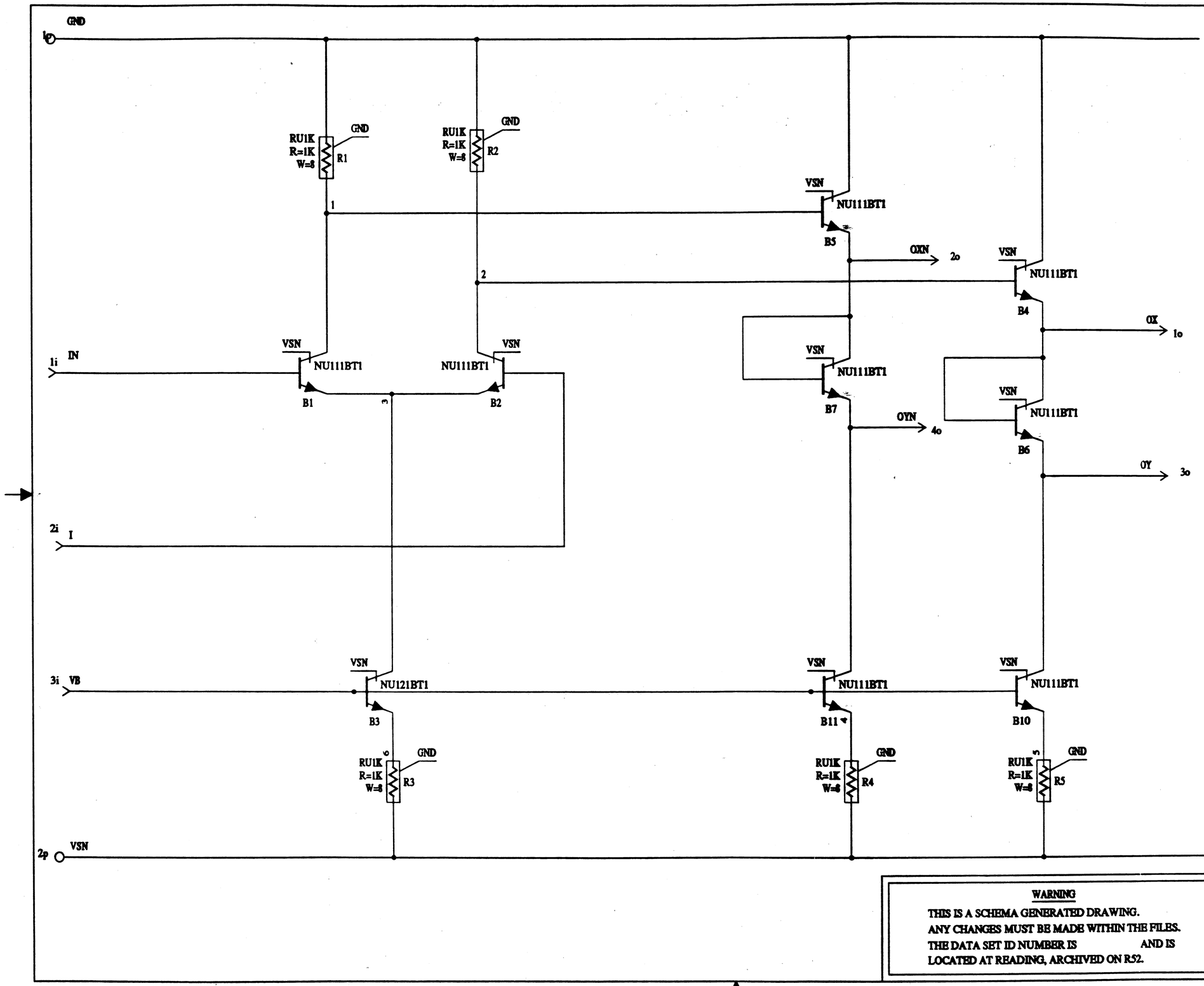
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 157

17X11



ENGR	DLL
DRWN	MDA
Nov. 16, 1989	ISSUE

	INV1XY.1
USED ON	DRAWING

AT&T -

INVERTER

(INV1XY.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 158

17X11

DATA SHEET FOR: XOR2, XOR2H, XNOR2, XNOR2H

XOR2:	2-input Exclusive-OR	50 MHz
XOR2H:	2-input Exclusive-OR	100 MHz
XNOR2:	2-input Exclusive-NOR	50 MHz
XNOR2H:	2-input Exclusive-NOR	100 MHz

All of the gates have an area of 135 um X 310 um.

XOR2, XNOR2:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	2.4	1.6	1.0
3	2.7	1.7	1.1
5	3.0	1.9	1.2
7	3.3	2.1	1.3

Power (mW)

Max	Nom	Min
2.4	1.8	1.5

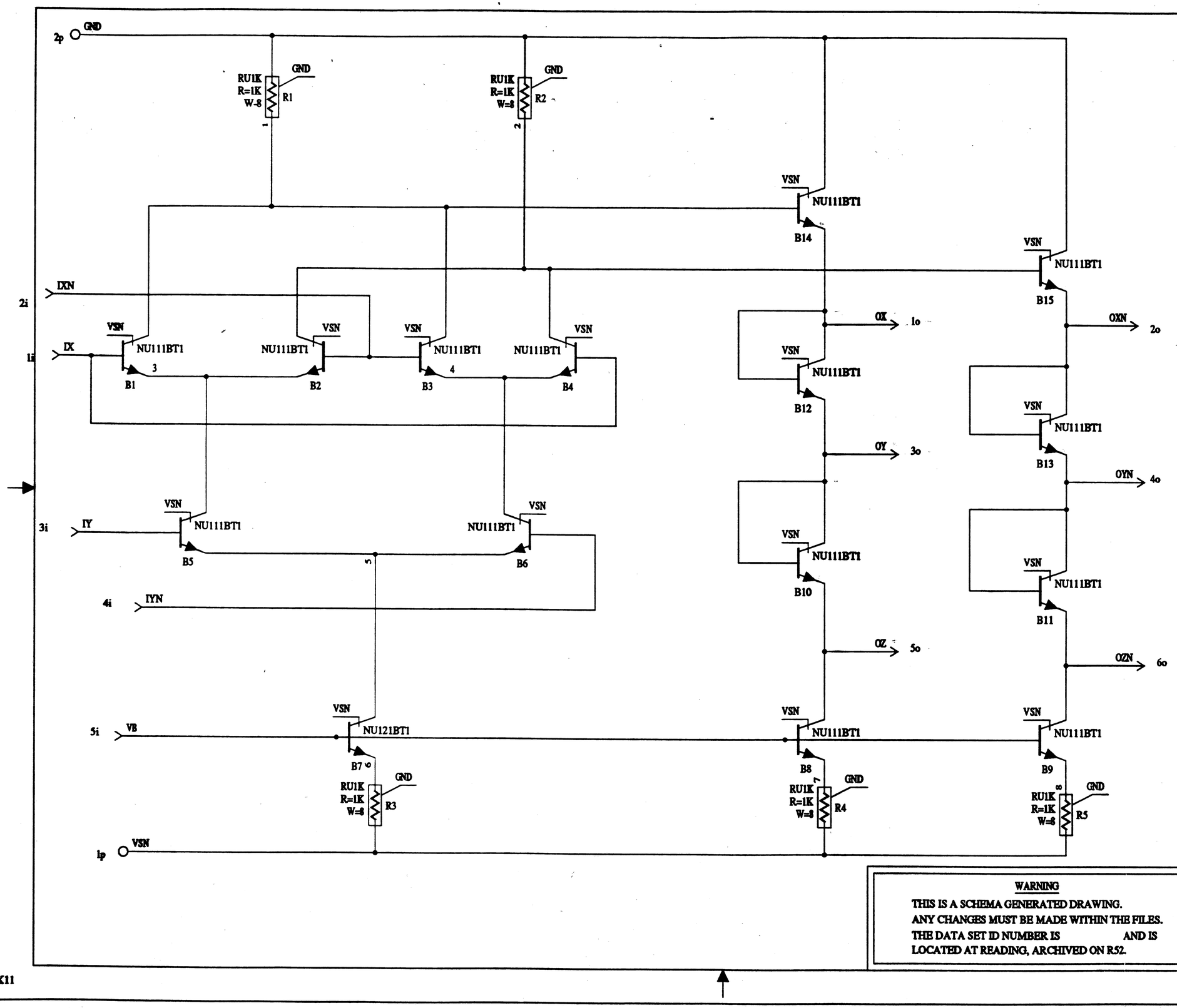
XOR2H, XNOR2H:

Propagation delay (ns)

Fanout	Max	Nom	Min
1	1.7	1.1	0.8
3	1.9	1.3	0.9
5	2.1	1.4	0.9
7	2.3	1.5	1.0

Power (mW)

Max	Nom	Min
3.9	2.9	2.4



ENGR	DLL		
DRWN	MDA		

August 10, 1989 ISSUE

USED ON	DRAWING
AT&T -	

2 INPUT
EXCLUSIVE-
OR GATE
(XOR2.1)

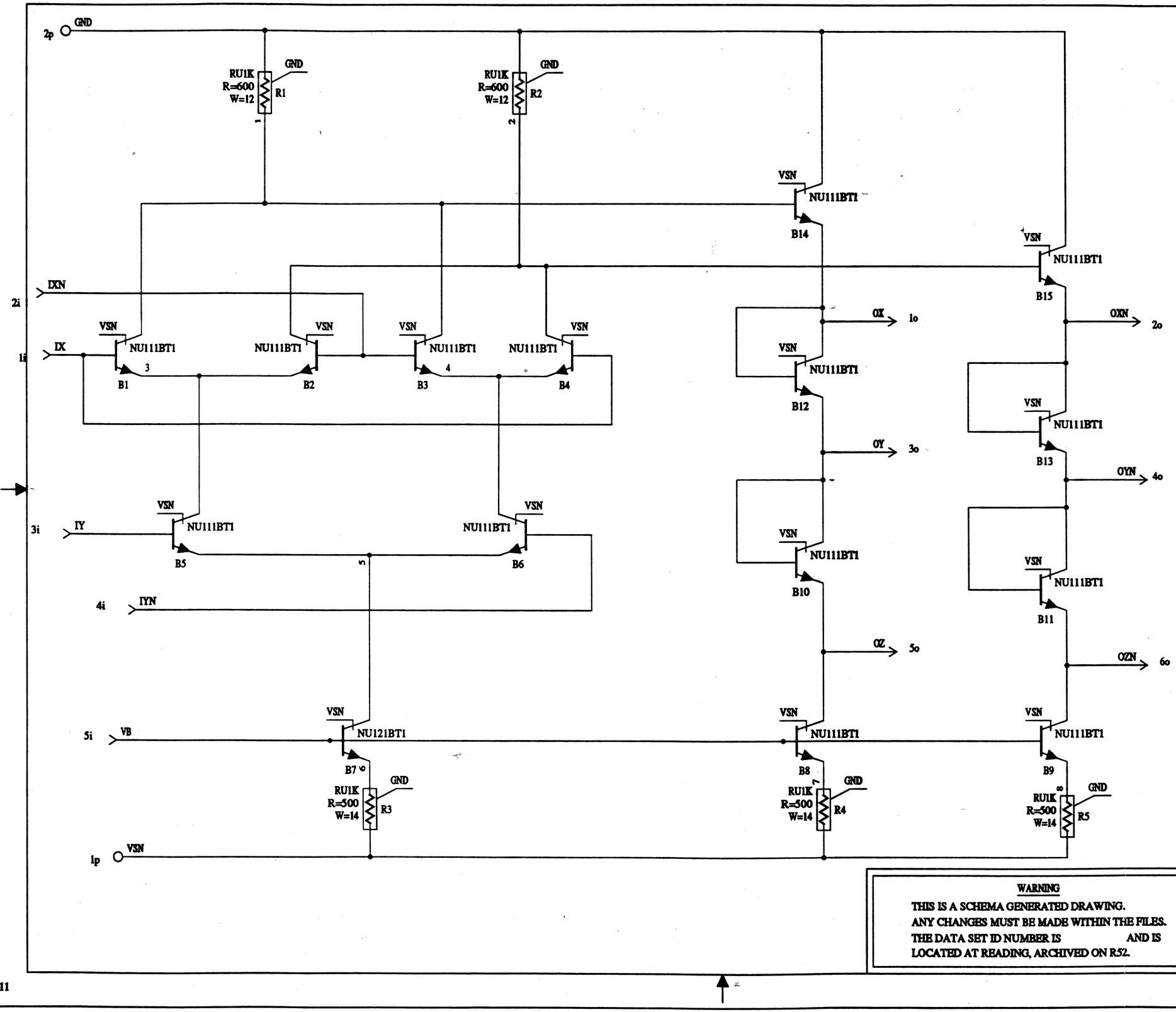
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 160

17X11



ENGR	DLL		
DRWN	MDA		
Sept. 5, 1989	ISSUE		

USED ON	DRAWING

AT&T -

2 INPUT
EXCLUSIVE-OR GATE
HIGH CURRENT
(XOR2H.1)

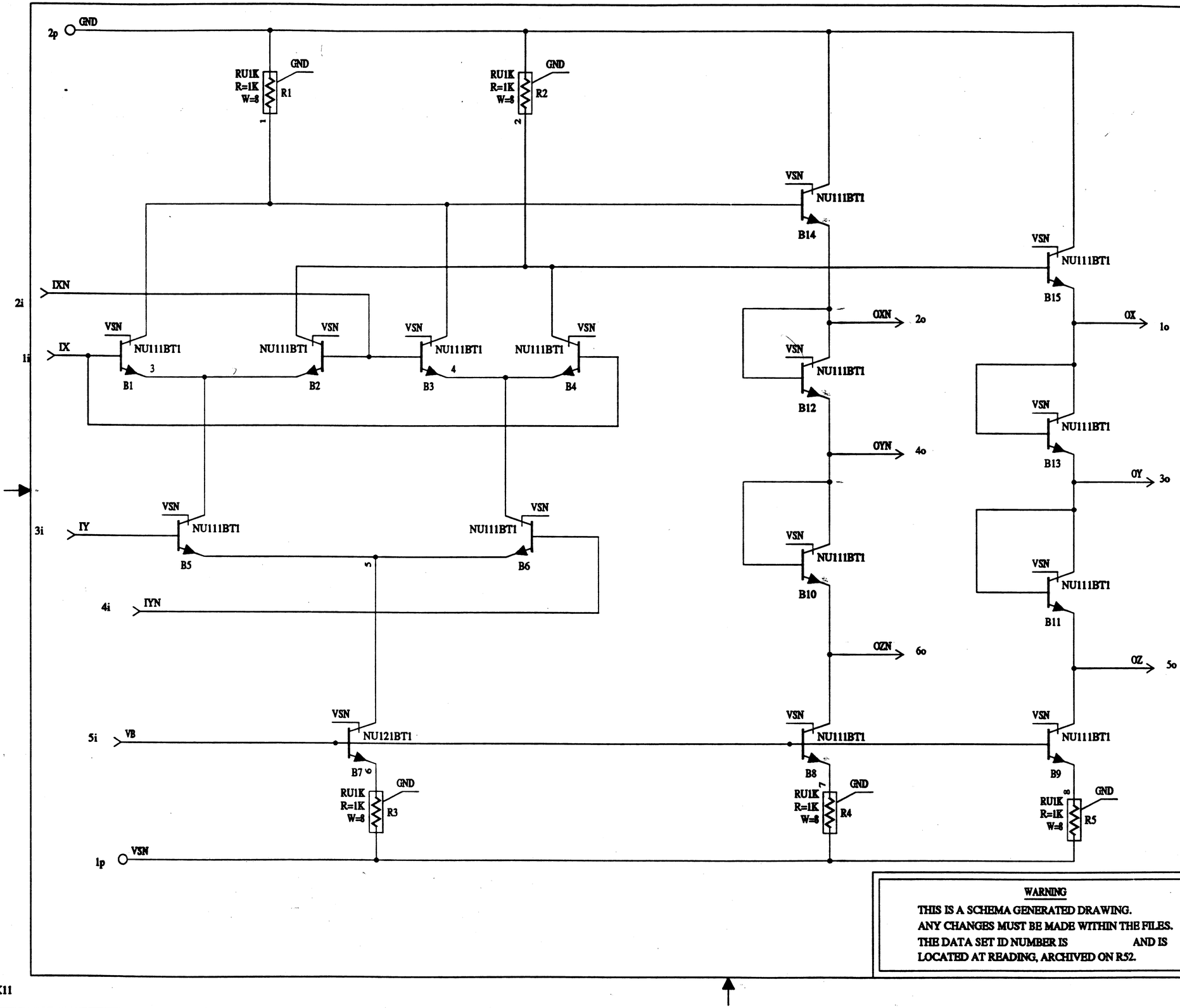
WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 161

17X11



ENGR	DLL
DRWN	MDA
Nov. 16, 1989	ISSUE

	XNOR2.1
USED ON	DRAWING

AT&T -

2 INPUT EXCLUSIVE-NOR GATE (XNOR2.1)

WARNING

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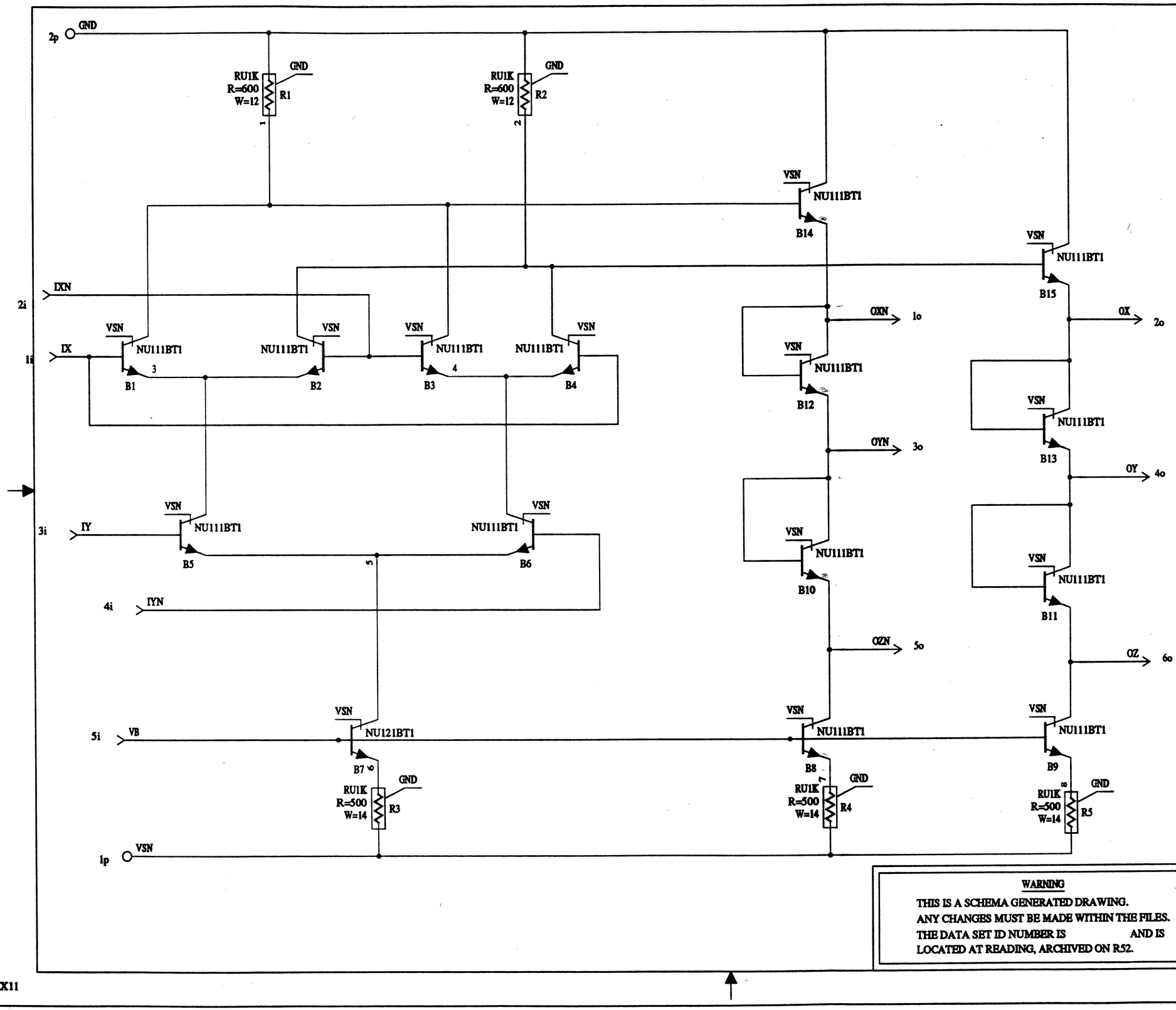
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 162

17X11



ENGR	DLL
DRWN	MDA
Dec. 13, 1989	ISSUE

	XNOR2H.1
USED ON	DRAWING

AT&T -

2 INPUT
EXCLUSIVE-NOR GATE
HIGH CURRENT
(XNOR2H.1)

WARNING

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THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE
2S

SHEET 163

17X11

DATA SHEET FOR: REF0, REF1

The REF0 and REF1 circuits provide logic 0 and logic 1 DC voltage levels. They are used in the following manner: if the signals IX and IXN represent a differential input signal, a logic 1 is applied by attaching the X level output of REF1 to IX and the X level output of REF0 to IXN. The REF0 circuit supplies the low level and REF1 the high level of a differential voltage.

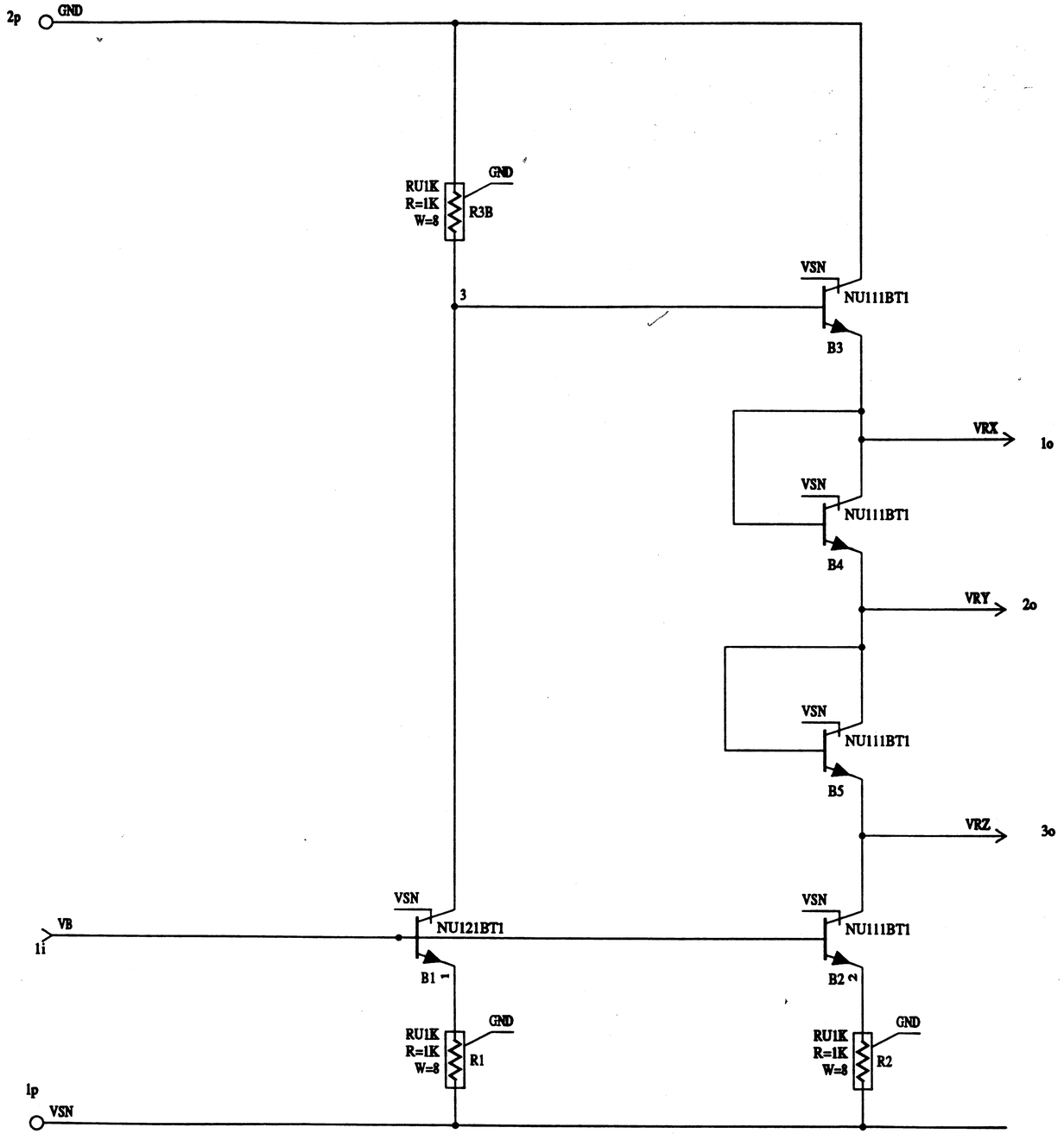
REF0: Low level of differential voltage
REF1: High level of differential voltage

All of the gates have an area of 60 um X 310 um.

REF0, REF1:

Power (mW)

Max	Nom	Min
1.2	0.9	0.8



ENGR	DLL		
DRWN	MDA		

August 18, 1989 ISSUE

USED ON	DRAWING
AT&T -	

REFERENCE
LEVEL '0'
CIRCUIT
(REF0.1)

WARNING

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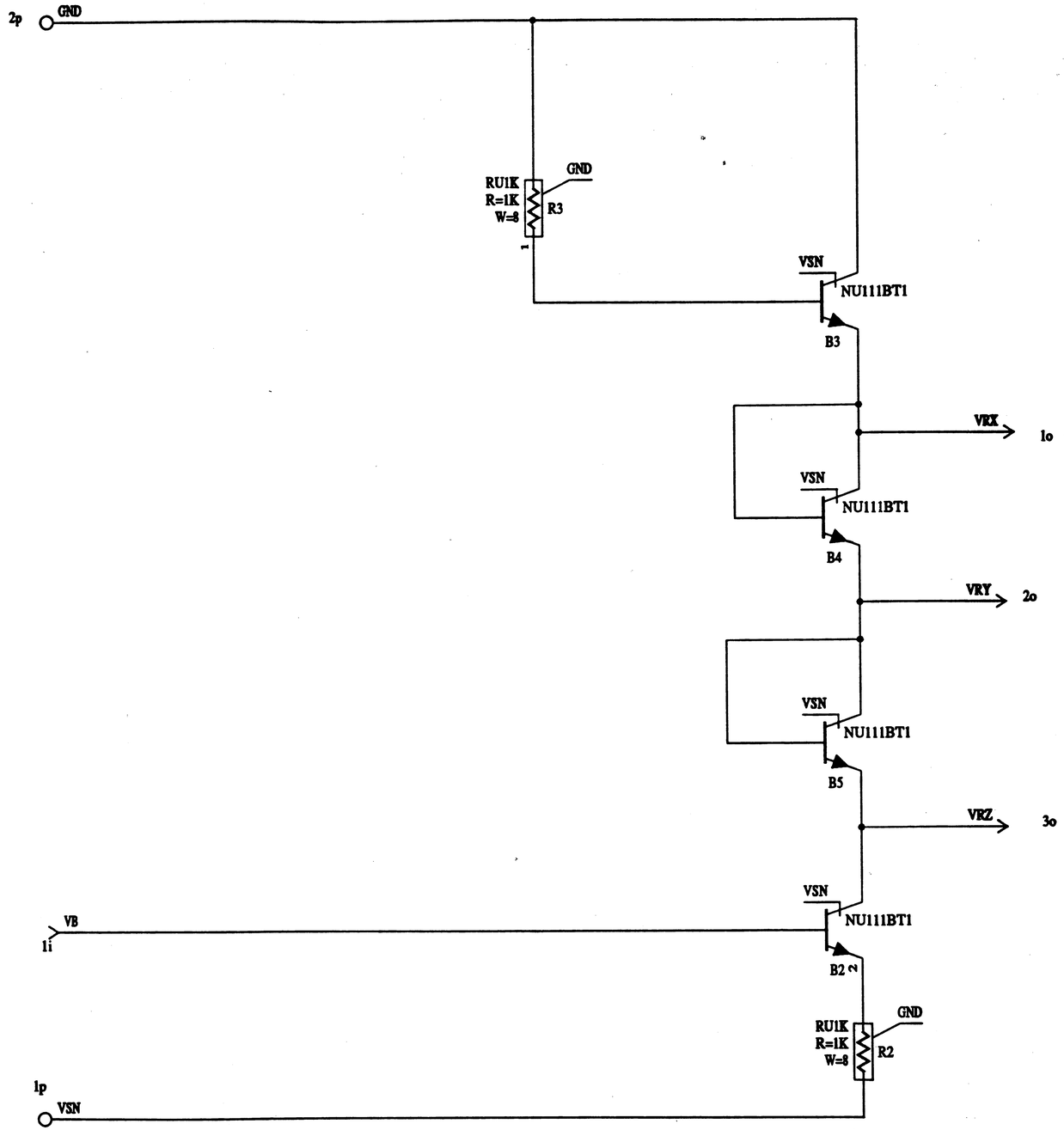
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 165

17X11



ENGR	DLL		
DRWN	MDA		

August 18, 1989 ISSUE

USED ON	DRAWING

AT&T -

REFERENCE
LEVEL '1'
CIRCUIT
(REF1.1)

WARNING

THIS IS A SCHEMA GENERATED DRAWING.
ANY CHANGES MUST BE MADE WITHIN THE FILES.
THE DATA SET ID NUMBER IS AND IS
LOCATED AT READING, ARCHIVED ON R52.

DWG SIZE 2S

SHEET 166

17X11

Appendix 2 Bipolar Transistor Models

The models of the NPN bipolar transistors used in the logic gates are included in this appendix for completeness. The variable names are not explained.

```
**
**  LOW MODEL
**
* ONE 1.5 BY 5 MICRON STRIPES (ONE BASE STRIPE)
* emitter between the collector and the base
.MODEL NU111BT1 NEB (RBX =  2.602E+02 RBI =  6.792E+02 RCX =  3.925E+01
+  RE  =  8.400E+00 RCI =  6.658E+02 RBIP=  2.446E+02 IS  =  6.313E-18
+  I1  =  5.883E-20 I2  =  1.667E-16 NE  =  1.700E+00 IK  =  1.005E-03
+  VBO =  2.780E+00 TFO =  2.900E-11 CJE =  3.017E-14 PE  =  11.05E-01
+  ME  =  4.950E-01 BE  =  1.000E-01 I3  =  6.250E-19 I4  =  2.685E-21
+  NC  =  1.700E+00 IKR =  1.667E+05 VAO =  2.050E+01 TRO =  3.240E-10
+  CJC =  4.692E-15 PC  =  6.150E-01 MC  =  3.350E-01 BC  =  1.000E-01
+  EA  =  1.206E+00 DEA =  8.000E-02 TO  =  2.500E+01 VBDC=  0.
+  ALC1=  2.000E+00 ALC2=  0.        ALTC=  7.500E-01 VBDE=  0.
+  ALE1=  2.000E+00 ALE2=  0.        ALTE=  7.500E-01 KFN =  0.
+  AFN =  1.000E+00 BFN =  1.000E+00 NID =  1.040E-11 QCO =  1.860E-13
+  VJCO=  4.600E+00 I1P =  4.093E-19 I2P =  3.275E-20 NEP =  1.283E+00
+  IKP =  4.614E-05 CJEP=  5.484E-14 ISP =  2.358E-17 I3P =  3.275E-17
+  CJCP=  2.893E-13 PS  =  5.000E-01 MS  =  3.180E-01 BS  =  1.000E-01
+  TRCI=  2.000E+00 TVCO=  1.680E+00)
*


**
**  HIGH MODEL
**
* ONE 1.5 BY 5 MICRON STRIPES (ONE BASE STRIPE) :    HIGH MODEL*
* emitter between the collector and the base
.MODEL NU111BT1 NEB (RBX =  1.255E+02 RBI =  3.144E+03 RCX =  2.732E+01
+  RE  =  8.400E+00 RCI =  3.047E+02 RBIP=  2.446E+02 IS  =  5.650E-17
+  I1  =  1.078E-19 I2  =  1.667E-16 NE  =  1.700E+00 IK  =  1.000E-03
+  VBO =  1.000E+00 TFO =  2.300E-11 CJE =  1.483E-14 PE  =  11.05E-01
+  ME  =  4.950E-01 BE  =  1.000E-01 I3  =  6.250E-19 I4  =  2.685E-21
+  NC  =  1.653E+00 IKR =  1.667E+05 VAO =  6.500E+00 TRO =  3.240E-10
+  CJC =  3.308E-15 PC  =  6.150E-01 MC  =  3.350E-01 BC  =  1.000E-01
+  EA  =  1.206E+00 DEA =  8.000E-02 TO  =  2.500E+01 VBDC=  0.
+  ALC1=  2.000E+00 ALC2=  0.        ALTC=  7.500E-01 VBDE=  0.
+  ALE1=  2.000E+00 ALE2=  0.        ALTE=  7.500E-01 KFN =  0.
+  AFN =  1.000E+00 BFN =  1.000E+00 NID =  2.500E-11 QCO =  4.149E-14
+  VJCO=  2.340E+00 I1P =  4.093E-19 I2P =  3.275E-20 NEP =  1.653E+00
+  IKP =  4.585E-05 CJEP=  3.813E-14 ISP =  2.358E-17 I3P =  3.275E-17
+  CJCP=  2.336E-13 PS  =  5.000E-01 MS  =  3.180E-01 BS  =  1.000E-01
+  TRCI=  2.000E+00 TVCO=  1.680E+00)
*
```

```
**
** NOMINAL MODEL
**
* ONE 1.5 BY 5 MICRON STRIPES (ONE BASE STRIPE)
* emitter between the collector and the base
.MODEL NU111BT1 NEB (RBX =  2.046E+02 RBI =  1.678E+03 RCX =  3.328E+01
+  RE  =  8.400E+00 RCI =  4.796E+02 RBIP=  2.446E+02 IS  =  1.900E-17
+  I1  =  7.167E-20 I2  =  1.667E-16 NE  =  1.700E+00 IK  =  1.005E-03
+  VBO =  1.600E+00 TFO =  2.500E-11 CJE =  2.000E-14 PE  =  11.05E-01
+  ME  =  4.950E-01 BE  =  1.000E-01 I3  =  6.250E-19 I4  =  2.685E-21
+  NC  =  1.700E+00 IKR =  1.667E+05 VAO =  1.430E+01 TRO =  3.240E-10
+  CJC =  3.978E-15 PC  =  6.150E-01 MC  =  3.350E-01 BC  =  1.000E-01
+  EA  =  1.206E+00 DEA =  8.000E-02 TO  =  2.500E+01 VBDC=  0.
+  ALC1=  2.000E+00 ALC2=  0.        ALTC=  7.500E-01 VBDE=  0.
+  ALE1=  2.000E+00 ALE2=  0.        ALTE=  7.500E-01 KFN =  0.
+  AFN =  1.000E+00 BFN =  1.000E+00 NID =  1.513E-11 QCO =  1.073E-13
+  VJCO=  3.320E+00 I1P =  4.093E-19 I2P =  3.275E-20 NEP =  1.283E+00
+  IKP =  4.614E-05 CJEP=  4.647E-14 ISP =  2.358E-17 I3P =  3.275E-17
+  CJCP=  2.586E-13 PS  =  5.000E-01 MS  =  3.180E-01 BS  =  1.000E-01
+  TRCI=  2.000E+00 TVCO=  1.680E+00)
+  ALC1=  2.000E+00 ALC2=  0.        ALTC=  7.500E-01 VBDE=  0.
+  ALE1=  2.000E+00 ALE2=  0.        ALTE=  7.500E-01 KFN =  0.
+  AFN =  1.000E+00 BFN =  1.000E+00 NID =  1.513E-11 QCO =  3.000E-13
+  VJCO=  3.320E+00 I1P =  1.627E-18 I2P =  1.302E-19 NEP =  1.283E+00
+  IKP =  1.834E-04 CJEP=  1.803E-13 ISP =  9.374E-17 I3P =  1.302E-16
+  CJCP=  4.120E-13 PS  =  5.000E-01 MS  =  3.180E-01 BS  =  1.000E-01
+  TRCI=  2.000E+00 TVCO=  1.680E+00)
*
```

The different process files are made by using combinations of the low, nom and high models for the transistors and the resistors. The resistor model is called RU1K which stands for a resistor made of 1 Kohms/square material. Since the bandgap reference circuit provides current to the gates at it uses the RU50 resistor, it's variations are also shown. The various combinations are listed below:

C0:	NPN - nom	C1:	NPN - low	C2:	NPN - high
	RU1K - nom		RU1K - high		RU1K - low
	RU50 - nom		RU50 - high		RU50 - low

C3: NPN - low
RU1K - high
RU50 - high

C4: NPN - high
RU1K - high
RU50 - high

C5: NPN - low
RU1K - high
RU50 - low

C6: NPN - low
RU1K - low
RU50 - high

Appendix 3 Extracted Circuit Example

The parasitic capacitance due to metal lines play an important part in the performance of high speed circuits. All of the gates were layed out in the target process. A computer program was used to extract the value of all of the parasitic capacitors caused by metal lines. The simulations were performed using the extracted circuit file.

An example is shown here of the information that is included in the extracted file. The capacitors models have the following meanings:

BOTSUB - Bottom metal to substrate capacitance

TOPSUB - Top metal to substrate capacitance

TOPBOT - Top to bottom metal capacitance

```
*
.subckt and2 (ix  ixn  iy  iyn  vb  ox  oxn  oy  oyn  oz  ozn)
*
.global  gnd      vsp      vsn
*
*
b1        6        ix       5        vsn      null1bt1
b2        7        ixn      5        vsn      null1bt1
b3        5        iy       4        vsn      null1bt1
b4        7        iyn      4        vsn      null1bt1
b5        4        vb       1        vsn      null1bt1 2
b6        ozn      vb       2        vsn      null1bt1
b7        oz       vb       3        vsn      null1bt1
b8        gnd      6        oxn      vsn      null1bt1
b9        oxn      oxn      oyn      vsn      null1bt1
b10       oyn      oyn      ozn      vsn      null1bt1
b11       gnd      7        ox       vsn      null1bt1
b12       ox       ox       oy       vsn      null1bt1
b13       oy       oy       oz       vsn      null1bt1
```

```
*
xr1     6       gnd     gnd     rulk    {r=1.003k,w=8}
xr2     gnd     7       gnd     rulk    {r=1.003k,w=8}
xr3     vsn     1       gnd     rulk    {r=1.003k,w=8}
xr4     2       vsn     gnd     rulk    {r=1.003k,w=8}
xr5     vsn     3       gnd     rulk    {r=1.003k,w=8}
*
*
cc1     oz      vsn     botsub  (2.823e-14 0.000e+00 0.000e+00)
cc2     oy      vsn     botsub  (4.256e-14 0.000e+00 0.000e+00)
cc3     ox      vsn     botsub  (5.111e-14 0.000e+00 0.000e+00)
cc4     7       vsn     botsub  (3.804e-14 0.000e+00 0.000e+00)
cc5     1       vsn     botsub  (1.649e-14 0.000e+00 0.000e+00)
cc6     ixn     vsn     botsub  (2.459e-14 0.000e+00 0.000e+00)
cc7     6       vsn     botsub  (3.234e-14 0.000e+00 0.000e+00)
cc8     3       vsn     botsub  (1.474e-14 0.000e+00 0.000e+00)
cc9     ozn     vsn     botsub  (2.582e-14 0.000e+00 0.000e+00)
cc10    4       vsn     botsub  (3.619e-14 0.000e+00 0.000e+00)
cc11    oyn     vsn     botsub  (4.050e-14 0.000e+00 0.000e+00)
cc12    oxn     vsn     botsub  (4.798e-14 0.000e+00 0.000e+00)
cc13    5       vsn     botsub  (2.627e-14 0.000e+00 0.000e+00)
cc14    vb      vsn     botsub  (2.217e-14 0.000e+00 0.000e+00)
cc15    iyn     vsn     botsub  (1.837e-14 0.000e+00 0.000e+00)
cc16    ix      vsn     botsub  (2.334e-14 0.000e+00 0.000e+00)
cc17    vb      vsn     botsub  (7.228e-15 0.000e+00 0.000e+00)
cc18    2       vsn     botsub  (1.335e-14 0.000e+00 0.000e+00)
cc19    iy      vsn     botsub  (2.227e-14 0.000e+00 0.000e+00)
cd20    1       vsn     topsub  (1.579e-14 0.000e+00 0.000e+00)
cd21    ixn     vsn     topsub  (2.169e-14 0.000e+00 0.000e+00)
cd22    6       vsn     topsub  (1.322e-14 0.000e+00 0.000e+00)
cd23    oxn     vsn     topsub  (8.400e-15 0.000e+00 0.000e+00)
cd24    iyn     vsn     topsub  (1.195e-14 0.000e+00 0.000e+00)
cd25    ix      vsn     topsub  (1.527e-14 0.000e+00 0.000e+00)
ce26    gnd     ox      topbot  (1.011e-14 0.000e+00 0.000e+00)
ce27    vsn     oz      topbot  (4.130e-15 0.000e+00 0.000e+00)
ce28    vsn     oy      topbot  (4.130e-15 0.000e+00 0.000e+00)
ce29    gnd     7       topbot  (3.072e-15 0.000e+00 0.000e+00)
ce30    vsn     ox      topbot  (4.130e-15 0.000e+00 0.000e+00)
ce31    ixn     7       topbot  (1.652e-15 0.000e+00 0.000e+00)
ce32    vsn     1       topbot  (6.110e-15 0.000e+00 0.000e+00)
ce33    gnd     6       topbot  (6.208e-15 0.000e+00 0.000e+00)
ce34    6       7       topbot  (8.260e-16 0.000e+00 0.000e+00)
ce35    vsn     ixn     topbot  (4.130e-15 0.000e+00 0.000e+00)
ce36    ixn     6       topbot  (8.260e-16 0.000e+00 0.000e+00)
ce37    vsn     3       topbot  (1.084e-15 0.000e+00 0.000e+00)
ce38    gnd     oxn     topbot  (1.028e-14 0.000e+00 0.000e+00)
ce39    vsn     ozn     topbot  (4.130e-15 0.000e+00 0.000e+00)
ce40    vsn     4       topbot  (4.303e-15 0.000e+00 0.000e+00)
ce41    vsn     oyn     topbot  (4.130e-15 0.000e+00 0.000e+00)
ce42    vsn     oxn     topbot  (4.130e-15 0.000e+00 0.000e+00)
ce43    6       5       topbot  (8.260e-16 0.000e+00 0.000e+00)
ce44    1       iyn     topbot  (8.260e-16 0.000e+00 0.000e+00)
```

```
ce45      vsn       vb        topbot    (4.130e-15 0.000e+00 0.000e+00)
ce46      vsn       iyn       topbot    (4.130e-15 0.000e+00 0.000e+00)
ce47      1         ix        topbot    (8.260e-16 0.000e+00 0.000e+00)
ce48      vsn       ix        topbot    (4.130e-15 0.000e+00 0.000e+00)
ce49      vsn       vb        topbot    (4.633e-15 0.000e+00 0.000e+00)
ce50      vsn       2         topbot    (1.162e-15 0.000e+00 0.000e+00)
ce51      vsn       iy        topbot    (4.130e-15 0.000e+00 0.000e+00)
ce52      iyn       4         topbot    (8.260e-16 0.000e+00 0.000e+00)
ce53      oxn       vb        topbot    (8.260e-16 0.000e+00 0.000e+00)
ce54      ix        4         topbot    (8.260e-16 0.000e+00 0.000e+00)
ce55      ix        iy        topbot    (8.260e-16 0.000e+00 0.000e+00)
*
.finis
*
```