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MEMORY WINDOW STUDIES OF NONVOLATILE SILICON-OXIDE-NITRIDE-OXIDE-SILICON (SONOS) MEMORY DEVICES

by

Margaret Larson French

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

December 15, 1989

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

December 14, 1989
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Most importantly, I must acknowledge my husband who kept on pushing me forward toward reaching my educational goals and cheering me up after a long day of research with no results. Finally, I cannot forgot my parents who were the first to encourage me to continue my education.

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Abstract

The placement of the memory window with regards to voltage of nonvolatile SONOS memory devices was studied. The scaled SONOS transistors and capacitors were fabricated at Lehigh University. These devices, which program at low programming voltages (5-10 volts), have a tunnel oxide thickness of 20Å, a nitride thickness of 94Å, and a blocking oxide thickness of 25-34Å. The memory window, retention and erase/write characteristics of these scaled devices were examined.

Ground was used as the read voltage of these devices to eliminate the necessity to generate a separate read voltage. This stipulation, when combined with the charge decay rates for the erase and write states of the device, sets the design of the memory window. The alteration of the memory window was studied by (1) using n^+ and p^+ polysilicon gate devices and (2) implanting the bulk of the device. From the study of the n^+ and p^+ polysilicon gate devices, a 0.6 volt shift in the memory window was observed.

Adding an implant into the bulk of the device results in a positive shift in the memory window. The retention characteristics of the implanted devices were better than those of the nonimplanted devices. However, the programming speed of the implanted devices increased by as much as 200 ms (for the maximum implant dosage used).

Also, the effect of the read measurement set-up on the memory window was studied. It has been shown that the memory window position will change depending on whether the flatband voltage, threshold voltage, or turn-on voltage is read. This study showed a different memory window position on capacitors depending on whether the voltage is read in accumulation, depletion or flatband.

Chapter 1
Introduction

1.1 What is the Memory Window?

My research deals with the placement of the memory window of a SONOS device with regards to read voltage which will be assumed to be selected as ground. The memory window is determined by the measured voltage in the written state and the measured voltage in the erased state. One method to determine the memory window is to examine the retention plot of a SONOS device. This plot is obtained when a device is programmed with a fixed voltage and pulse width and then measured after a desired retention time. The charge stored in the device upon programming will gradually decay with time. Thus, the memory window will begin by being centered around one voltage level with a given width and as time progress, it will have a smaller width and may be be centered around a different voltage. Figure 1-1 shows a retention plot for a p-channel SONOS device with the erase and write states indicated. Figure 1-2 shows the same plot for a n-channel SONOS device.

One can also look at the memory window in an erase/write plot. The device is read with various different pulse widths of a fixed programming voltage. This measurement allows one to examine the speed of the device. Figure 1-3 shows an erase/write plot for a p-channel SONOS device.

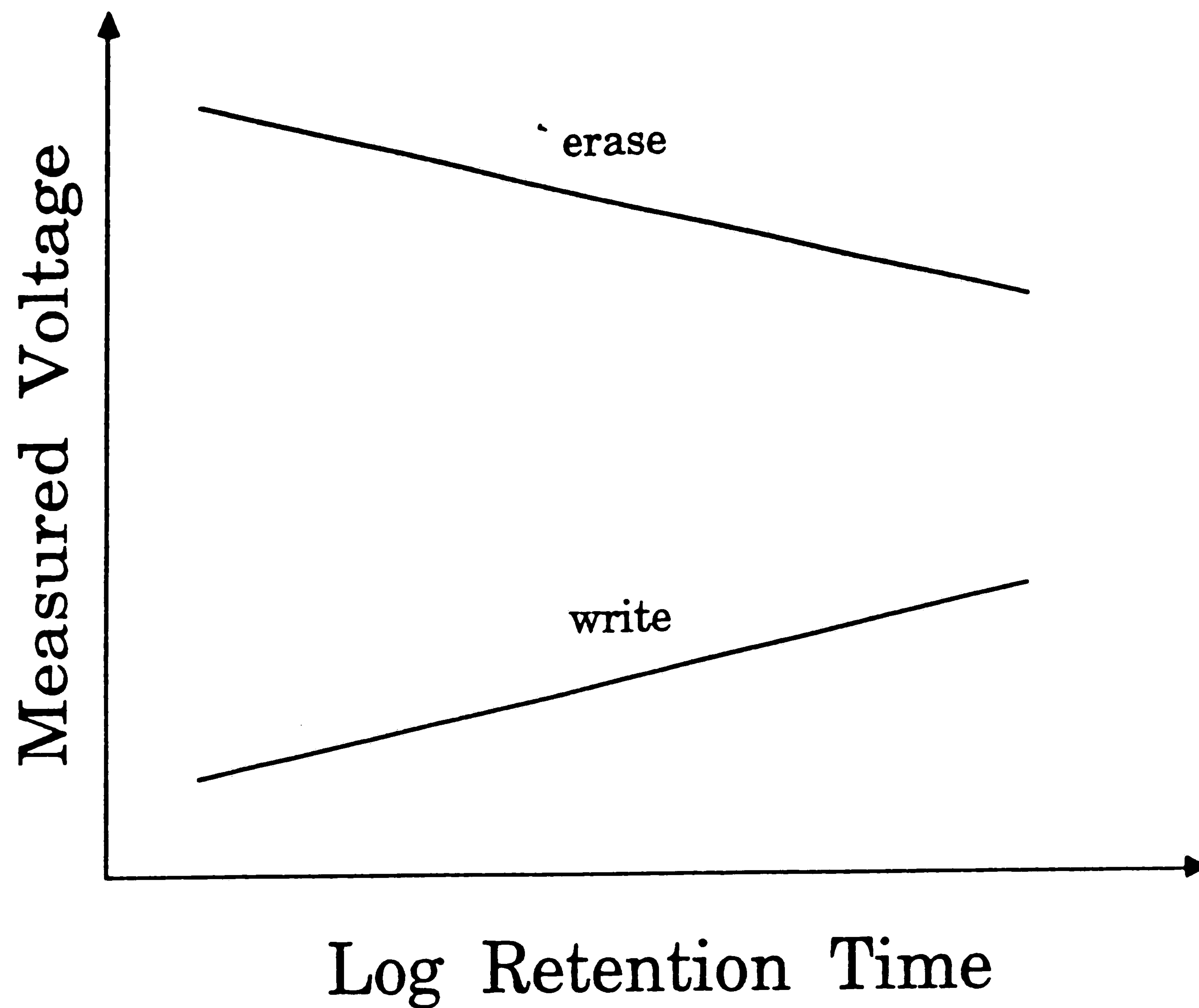


Figure 1-1: Sample retention plot for a p-channel SONOS device

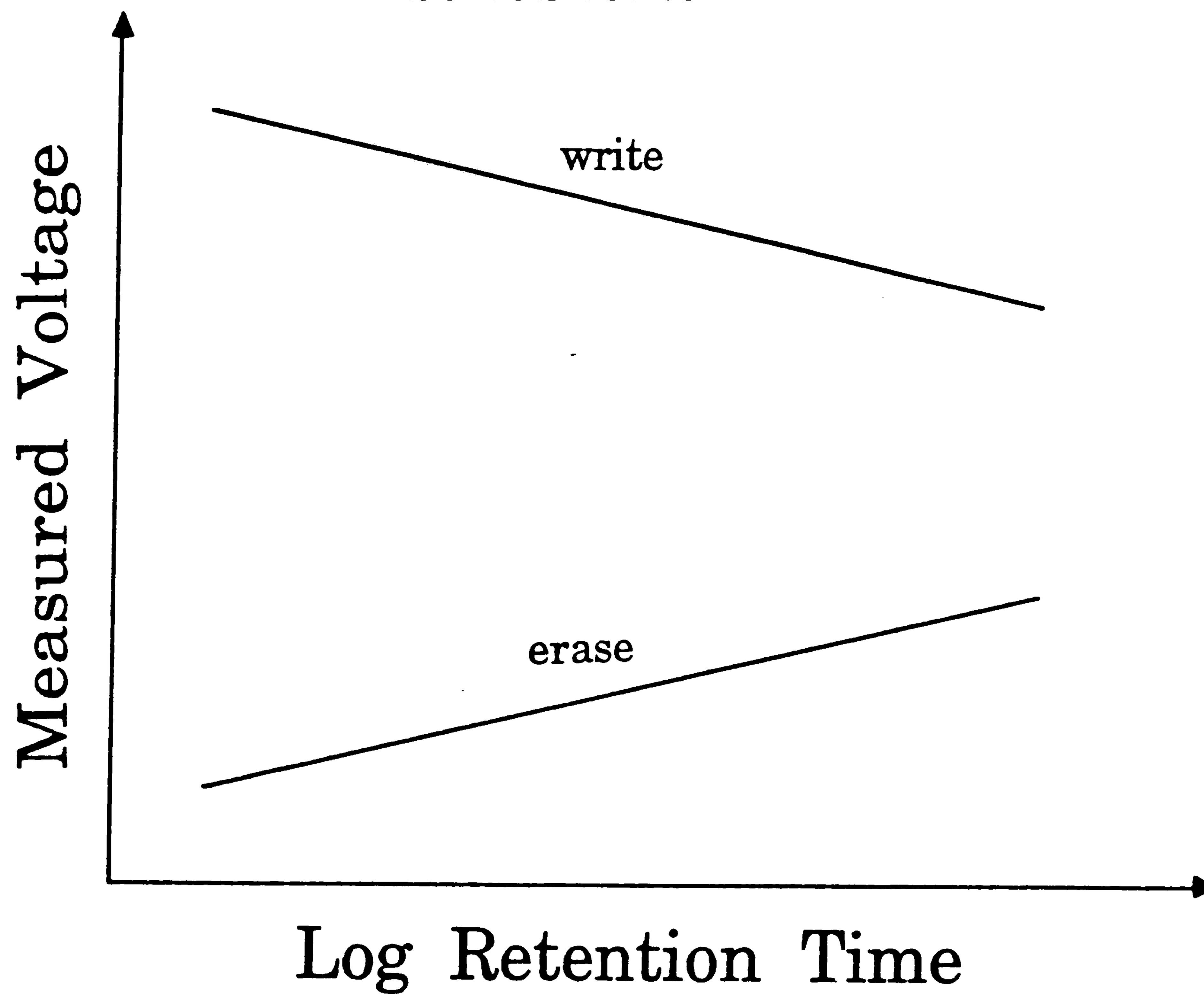


Figure 1-2: Sample retention plot for a n-channel SONOS device

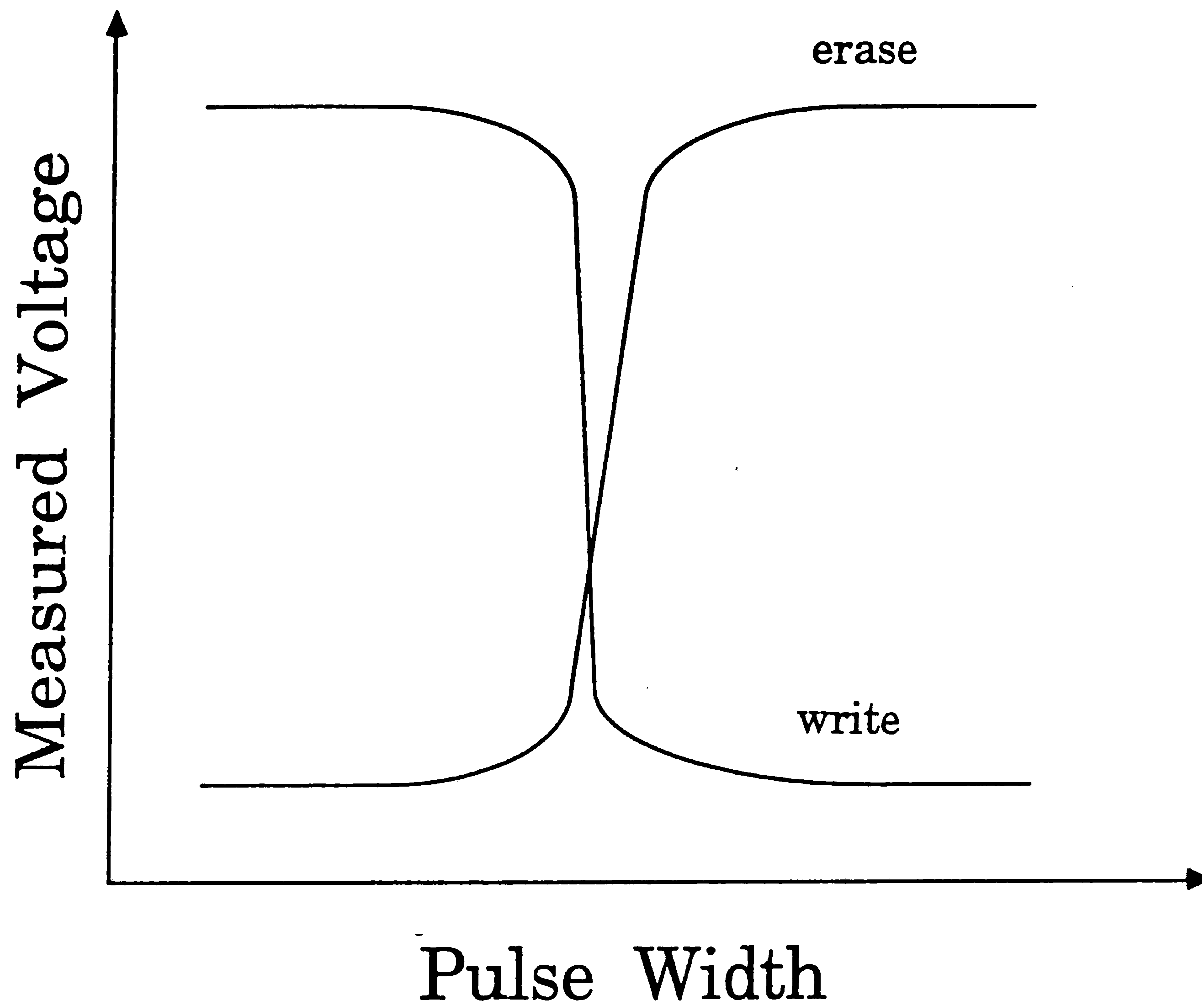


Figure 1-3: Sample erase/write plot for a p-channel SONOS device

1.2 Historical Review of the Memory Window

Historically, the memory window has been measured at various different voltage levels with several different decay rates for the erase and write state.

1. Lundkvist et al,1973.[1]
   - Device Structure: p-channel MNOS transistor with tunnel oxide thickness (x_{ot}) of 22.5Å and nitride thickness (x_n) of 900Å .
   - Measurement Conditions: Retention measurement taken from 1 second to $1x10^7$ seconds with a varied programming voltage (V_P) and a pulse width (t_p) of 1 msec.
   - Memory Window: The written state begins at -5 volts with a decay rate of 0.18 volts/decade and the erased state begins at -10 volts with a decay rate of -0.12 volts/decade.
   - Other Comments: A plot of the discharge rate versus the initial V_{TH} has a slope which is proportional to the initial stored charge.
2. White & Cricchi, 1972.[2]
   - Device Structure: MNOS transistor with x_{ot} = 25Å and x_n = 335Å .
   - Measurement Conditions: Pulsed retention measurements were taken with $V_P = \pm 25$ volts.
   - Memory Window: The n-channel transistor exhibited a written state starting at 8 volts with a decay rate of 0.27 volts/decade and an erased state starting at -7 volts with a decay rate of -0.48 volts/decade. The p-channel transistor showed a window beginning at 4 volts and -10 volts with respective decay rates of 0.27 volts/decade and -0.46 volts/decade.
   - Other Comments: The measurements show a similar decay rate for both n-channel and p-channel transistors.
3. Topich, 1984.[3]
   - Device Structure: n-channel double poly SNOS transistor with x_{ot} = 20Å and x_n = 390Å .
   - Measurement Conditions: Retention measurements are taken at a temperature of 100°C with a programming voltage of ±25 volts for a time period from 1 second to 1 year.
   - Memory Window: The window begins at 5 volts and -9 volts.

- Other Comments: The decay rate is logarithmic and increases for longer retention times.

4. Jacobs & Ulrich, 1981.[4]
    - Device Structure: n-channel SNOS transistor with $x_{ot} = 27 \pm 3Å$ and $x_n = 305Å$.
    - Measurement Conditions: The programming voltage is ±25 volts with a pulse width of 10 ms for the write state and 100 ms for the erase state for this measurement taken from 10 minutes to $1x10^5$ minutes.
    - Memory Window: The decay rate for the written state is 0.6 volts per decade in the short term and 1.0 volts per decade in the long term.
    - Other Comments: The logarithmic decay rate increases with time.
5. Suzuki et al, 1983.[5]
    - Device Structure: MONOS transistor with $x_{ot} = 21.9Å$, $x_n = 30Å$, and a blocking oxide (x_{ob}) of 33Å .
    - Measurement Conditions: The devices are measured for a decay time from 100 seconds to 10,000 seconds with $V_P = \pm 7$ volts and $t_p = 10$ ms.
    - Memory Window: The initial memory window is 2.5 volts wide with a decay rate of 0.11 volts/decade for the written state and -0.094 volts/decade for the erased state.
6. Libsch & Roy, 1989.[6]
    - Device Structure: p-type MONOS capacitor with $x_{ot} = 20Å$, $x_n = 50Å$, and $x_{ob} = 35Å$.
    - Measurements Conditions: The measurement is taken after 10^6 cycles for 0.1 seconds to 10^5 seconds with $V_P = \pm 5$ volts and $t_p = 10$ seconds.
    - Memory Window: A window from 0.1 volts to -3.4 volts is obtained with a decay rate of 0.075 volts/decade for the written state and -0.15 volts/decade for the erased state.
7. Chen, 1977.[7]
    - Device Structure: p-type SONOS capacitor with $x_{ot} = 30Å$, $x_n = 400Å$, and $x_{ob} = 150Å$.
    - Measurement Conditions: The retention measurement is taken by observing the change in the high frequency C-V plot over a time range of 10 seconds to 10^7 seconds for a programming voltage of ±25 volts.

- Memory Window: The write state begins at 3.8 volts with a decay rate of 0.40 volts per decade, and the erase state starts at -2.5 volts with a decay rate of -0.15 volts per decade.

8. Sharma, 1989.[8]
   - Device Structure: p-channel SONOS transistor with $x_{ot} = 20Å$, $x_n = 72Å$, and $x_{ob} = 42Å$.
   - Measurement Conditions: The measurement is taken from .03 seconds to $3x10^3$ seconds with $V_P = \pm 5$volts and $t_p = 10$ seconds.
   - Memory Window: The memory window begins at 1.9 volts and -1.4 volts and decays at a rate of 0.08 volts/decade and -0.12 volts/decade respectively.

1.3 Research Goals

My research was motivated by the need to be able to reposition the memory window such that after a long decay time, the window is centered around the read voltage in this case chosen to be 0 volts. By centering the window, one can improve the retention time since one state will not enter the undetectable voltage range much earlier than the other state. The window should not be centered at the initial point because the decay rates are unequal and the window will then not be centered as time progresses when the device will be read. Historically many different researchers have measured the window at different positions. In section 2.2, I will also show that the memory window position changes depending on the measurement technique used. Yet, for a given process sequence, one can reproduce the same memory window for different fabrication runs. My research was toward finding methods to predictable change the memory window by slightly altering the fabrication process. They are (1) employing different gate materials which corresponds to changing the gate to semiconductor workfunction and (2) implanting the bulk which corresponds to changing the bulk doping or the bulk potential.

When the memory window is changed using either of these methods, the

internal electric fields in the insulator will also be altered. Thus, one will see a difference in (1) the decay rates of the erase and write states during retention measurement, (2) the initial voltage to which the device is programmed for a given programming voltage, and (3) the programming speed for a given programming voltage. Thus, in exploring the methods used to change the memory window, I want to see how the other characteristics of the device as discussed above are effected. Does the retention and erase/write characteristics of the device improve or get worse? If so, how much of a change is there?

In this thesis, these questions will be answered. First, the theory of the memory window will be discussed along with the fabrication sequence used to make these device. Then, the measurements and analysis of these devices will show the change in the memory window position and any corresponding change in the retention and erase/write characteristics.

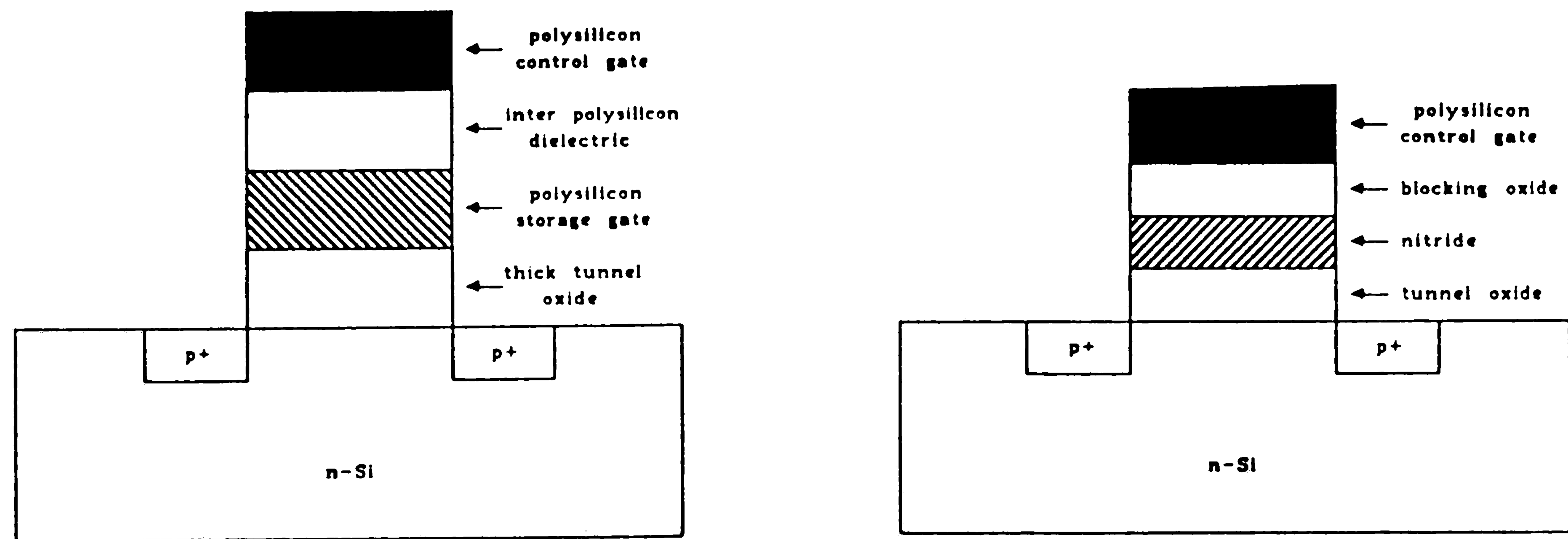
Chapter 2
Theory of the SONOS Device

2.1 Background

Nonvolatile semiconductor memory devices retain information when power is removed. Two basic types of devices exist, namely, the floating gate device (fig. 2-1a) and the floating trap device (fig. 2-1b). The floating gate device stores charge in the polysilicon as free charge in the conduction band, while the floating trap device, i.e., the Silicon Oxide Nitride Oxide Silicon (SONOS) device, stores charge in deep level traps located in the silicon nitride dielectric. Thus, the SONOS device stores charge as isolated trapped charges within the dielectric.

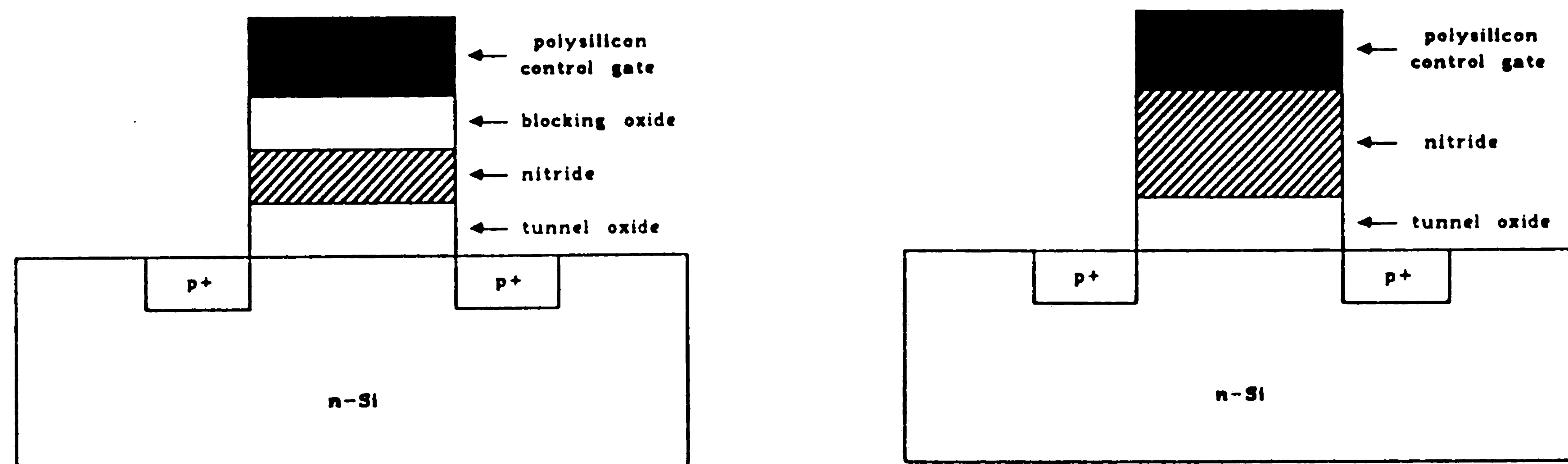
The Metal Nitride Oxide Silicon (MNOS) device, Silicon Nitride Oxide Silicon (SNOS) device, and the Metal Oxide Nitride Oxide Silicon (MONOS) device are also floating trap devices. The MNOS and MONOS devices have metal gates, while the SNOS and SONOS devices have n^+ or p^+ polysilicon gates. The MONOS and SONOS devices (fig. 2-2a) are different from the MNOS and SNOS devices (fig. 2-2b) in that they have an additional oxide, the blocking oxide, between the gate and the nitride. This blocking oxide, usually with a thickness greater than 30Å, is added to prevent hole injection from the gate. In the future I will refer to all of these devices as just the SONOS device, except when referring to one of them specifically.

The SONOS device operates similarly to a MOSFET except for one major difference which is a MOSFET has only one dielectric, an oxide, between the gate and the substrate (fig. 2-3a), while the SONOS device has three dielectrics, a blocking oxide, a nitride, and a tunnel oxide (fig. 2-3b). The extra dielectric layers in the SONOS device allow for the trapping of charge in the nitride



a) Floating Gate Device b) Floating Trap or SONOS Device

Figure 2-1: Comparison of floating gate device and floating trap device



a) SONOS/MONOS p-channel transistor b) SNOS/MNOS p-channel transistor

Figure 2-2: Contrast of SONOS/MONOS devices and SNOS/MNOS devices

forcing a shift in the threshold voltage which serves as a memory element. The MOS device has only a constant threshold voltage.

For a p-channel SONOS memory transistor, the four operational modes are erase, write, read, and inhibit. Given a p-channel SONOS transistor in an n-well (fig. 2-4) with a single programming supply and a read voltage of 0 volts, one can obtain these modes by applying the voltages given in the following table to the gate, source, drain, and bulk.

Operational Modes of a p-channel SONOS Transistor				
mode	gate	source	drain	bulk
erase	V_P	0	0	0
write	0	V_P	V_P	V_P
inhibit	0	float	0	V_P
read	0	V_P	0	V_P

In the erase mode, a positive voltage is applied relative to the gate allowing electrons to tunnel through the tunnel oxide and be trapped in the nitride. This trapped charge shifts the threshold voltage positive. The write mode is just the opposite of the erase mode. A negative voltage is applied from gate to bulk and the threshold voltage shifts negative. In the read mode the threshold voltage is not shifted. The gate is grounded, and a current is driven in at the source of the SONOS device to read the threshold voltage. Finally for the inhibit mode the voltages at the gate, drain, source, and bulk are chosen such that the device will not be written or erased.

For my research, I have used p-type MONOS capacitors (fig. 2-5a) and n-channel SONOS transistor (fig. 2-5b) which are made directly on p-type Si substrates. When integrating the CMOS and SONOS technology, the p-channel SONOS transistor in an n-well is preferred such that the SONOS device has a separate bulk contact than the CMOS devices. This bulk contact is employed to apply a positive programming voltage to the bulk to write the SONOS device

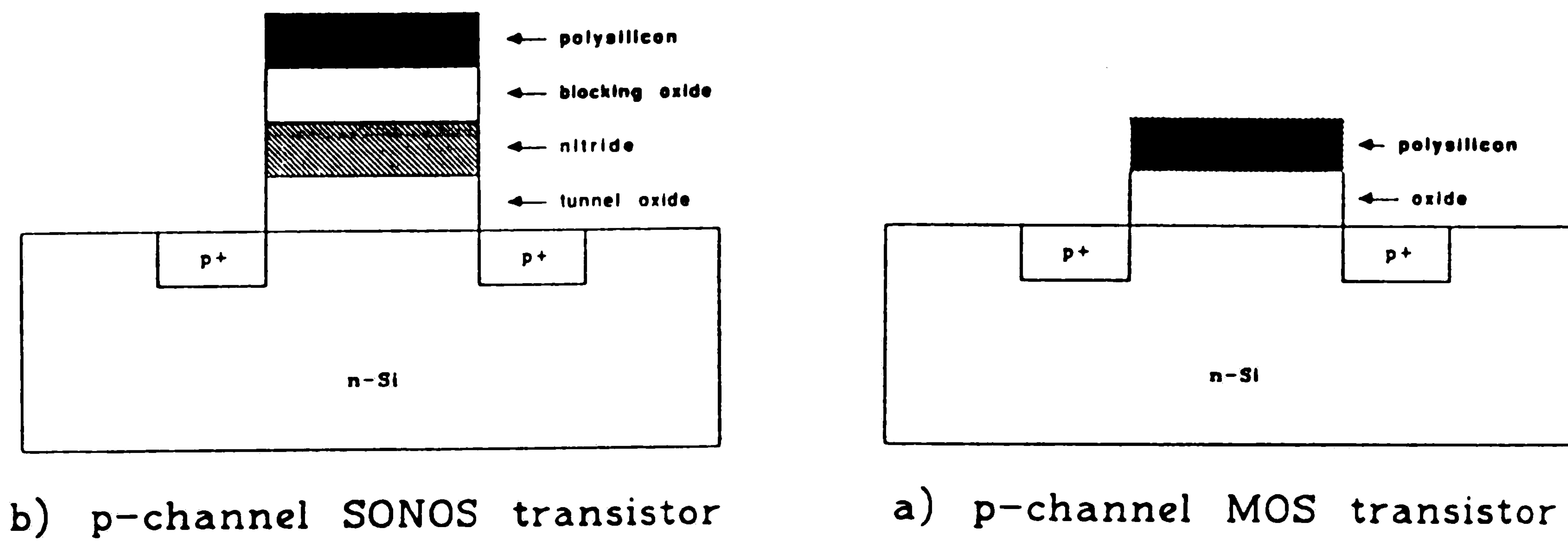


Figure 2-3: Comparison of SONOS transistor and MOS transistor

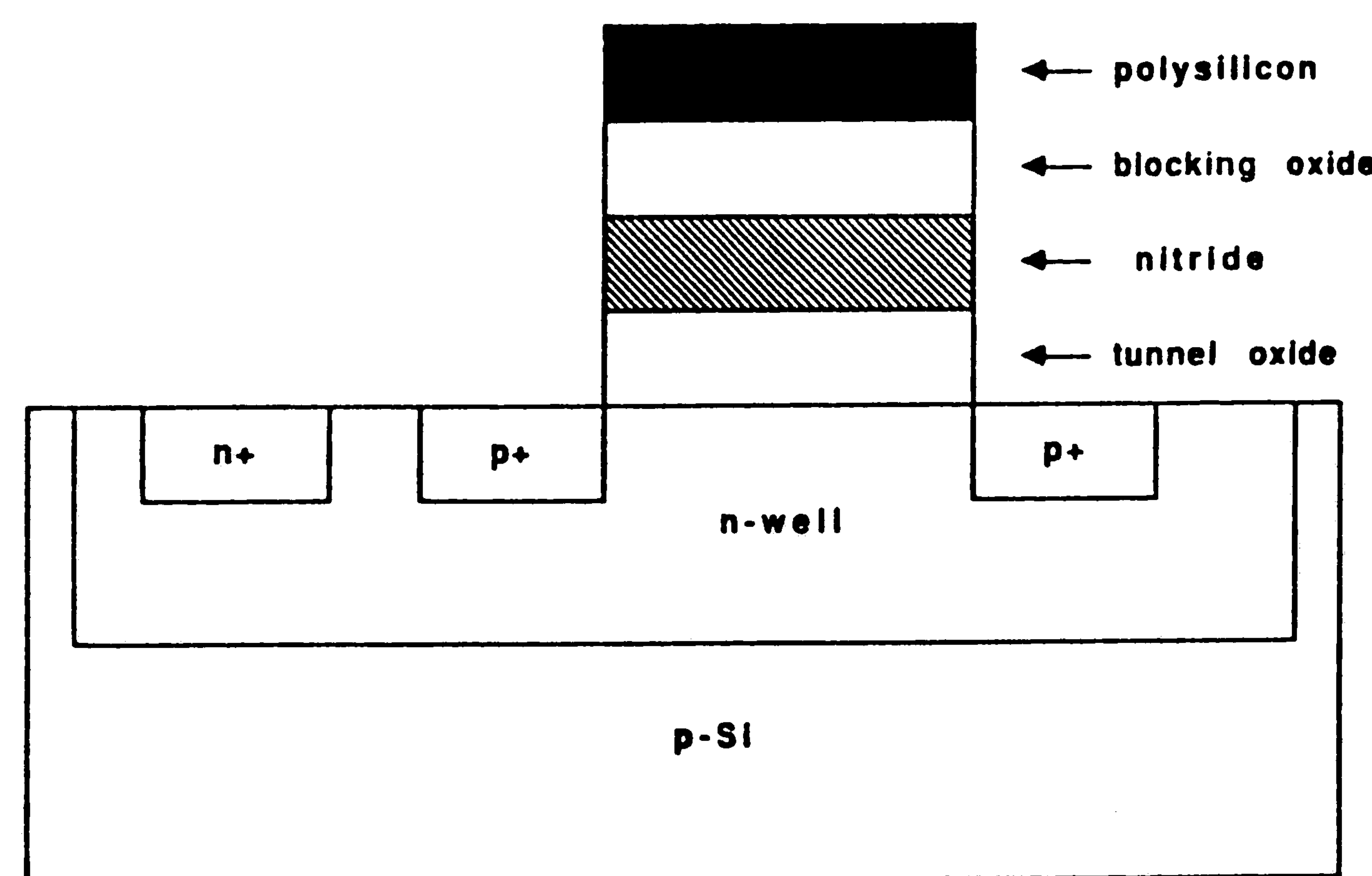
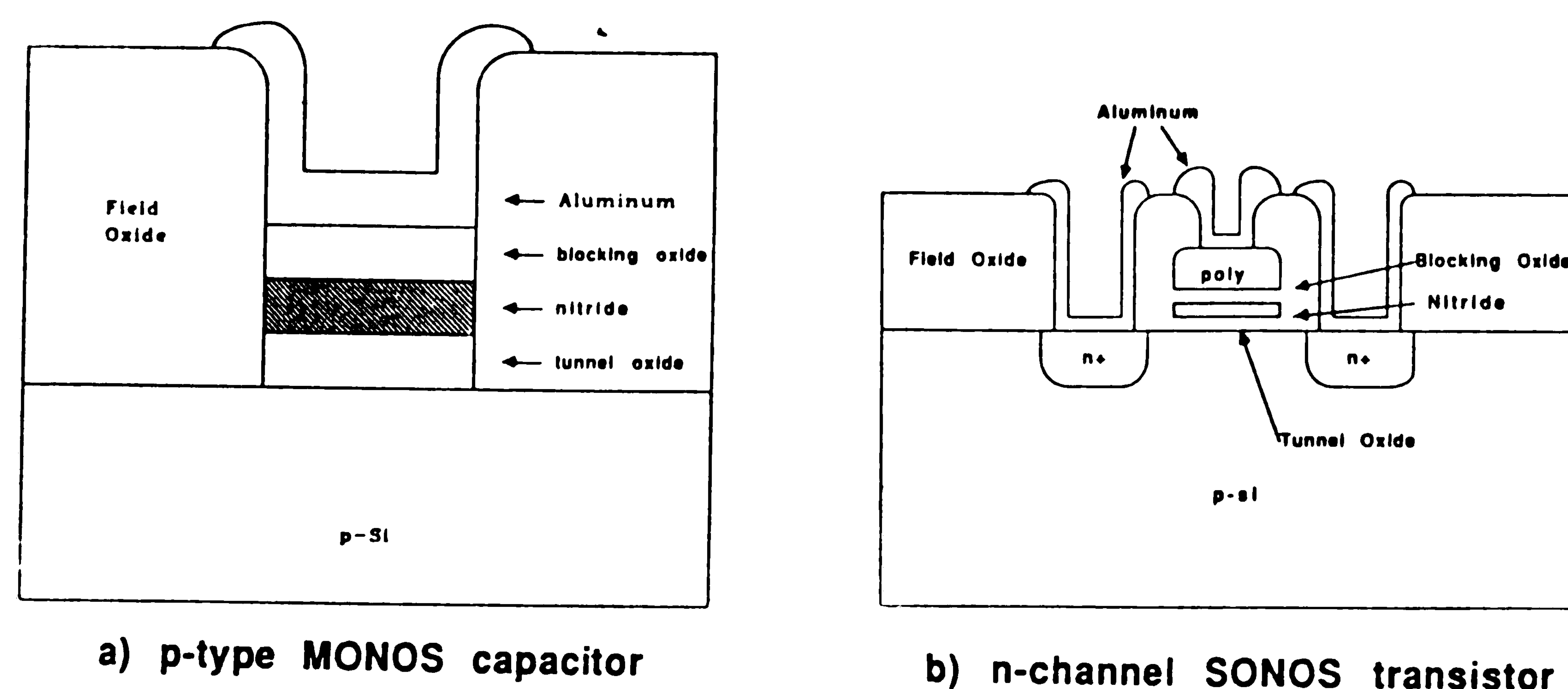


Figure 2-4: p-channel SONOS transistor in an n-well



a) p-type MONOS capacitor

b) n-channel SONOS transistor

Figure 2-5: Actual transistor and capacitor used for research

while maintaining the substrate at ground. Thus, a single power supply (V_P) can be used to accomplish both the erase and write operations. I chose to study the p-type MONOS capacitors and n-channel SONOS transistors since p-type Si wafers were readily available in our fabrication lab and I wanted to shorten the process sequence by avoiding the n-well process step.

These n-channel devices have the same operational modes as the p-channel devices but they are not obtained in the same manner. For my devices, I use two programming voltages, a write voltage which is positive and an erase voltage which is negative. For the p-type MONOS capacitor, the write mode is obtained by applying a positive voltage to the gate, and the erase mode can be achieved by applying a negative voltage to the gate. The gate is kept at ground during the inhibit mode to keep the device from being erased or written. Depending on the measurement equipment being used, different voltages and currents may be applied to read the device. The substrate is at ground at all times. The n-channel SONOS transistor operates in the same manner as the p-type MONOS capacitor with the source grounded through a 30K resistor and the drain tied directly to ground for the erase, write, and inhibit modes.

2.2 Measurement Dependence on the Memory Window

The memory window placement will depend on the measurement equipment and whether a transistor or capacitor is being used. For a capacitor, one has only a gate and substrate contact. When the voltage is measured, one usually obtains the flatband voltage from a C-V plot where the flatband voltage is expressed as

$$V_{FB} = \phi_{GS} - \frac{Q_f}{C_{eff}} - \left(\frac{x_{ob}}{\varepsilon_{ox}} + \frac{x_n - \bar{x}}{\varepsilon_N}\right) Q_N \quad (1)$$

where ϕ_{GS} is the gate to semiconductor workfunction, Q_f is the fixed charge in the insulator, x_{ob} and x_n are the blocking oxide and nitride thicknesses, ε_{ox} and ε_N are the dielectric permittivities of an oxide and a nitride, $\bar{x}$ is the charge centroid where $\bar{x} \approx \frac{x_n}{2}$, Q_N is the trapped charge in the nitride, and C_{eff} is the effective capacitance given as

$$C_{eff} = \frac{\varepsilon_{ox}}{x_{eff}}$$

$$x_{eff} = x_{ot} + \frac{\varepsilon_N}{\varepsilon_{ox}} x_n + x_{ob} \quad (2)$$

with x_{ot} as the tunnel oxide thickness, x_n as the nitride thickness, and x_{ob} as the blocking oxide thickness. We assume the tunnel oxide and the blocking oxide have the same relative dielectric constant, although this may not be the case since the tunnel oxide is known to be silicon rich and the blocking oxide is really an oxynitride. Depending on the measurement equipment used the measured voltage may not be the flatband voltage as discussed later in the thesis.

With a transistor, one has a source and drain contact in addition to the gate and substrate. Now, one can read the threshold voltage which is given as

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_{si} q N_B \phi_B}}{C_{eff}} \quad (3)$$

$$\phi_B = \frac{kt}{q} \ln\left(\frac{N_B}{n_i}\right) \quad (4)$$

where ϕ_B is the bulk potential, $\frac{kt}{q}$ is the thermal voltage, N_B is the bulk doping, ε_{si} is the dielectric permittivity of silicon, and n_i is the intrinsic carrier density. A transistor located in a memory cell may be characterized more accurately by measuring the voltage at a specified current which corresponds to the turn-on voltage, where

$$V_T = V_{TH} + \sqrt{\frac{2I_{DS}}{\beta}} \quad (5)$$

with I_{DS} is the drain to source current and

$$\beta = \bar{\mu}_{eff} \left(\frac{W}{L}\right) C_{eff} \quad (6)$$

where W is the width of the transistor, L is the length of the transistor, and $\bar{\mu}_{eff}$ is the effective mobility. The effective mobility is the bulk mobility reduced by Coulombic and surface scattering of carriers in the inversion layer. This mobility is influenced by the gate and substrate voltages.[9]

Thus, depending on which voltage is read, the memory window can change in both its center position and width. Figure 2-6 shows a retention plot in which the flatband voltage is measured. The threshold voltage and the turn-on voltage have also been calculated and plotted to show how the memory window will change depending on the voltage measured. For the turn-on voltage calculation, a transistor with a W/L of 5/1 is assumed with the measurement taken at a drain to source current of 10μa.

2.3 Methods to Change the Memory Window

I have studied different methods for changing the memory window which corresponds to changing the threshold voltage. As discussed previously, the equation for the threshold voltage of a SONOS device is:

$$V_{TH} = \phi_{GS} - \frac{Q_f}{C_{eff}} - \left(\frac{x_{ob}}{\varepsilon_{ox}} + \frac{x_n - \bar{x}}{\varepsilon_N}\right)Q_N + 2\phi_B + \frac{\sqrt{4\varepsilon_{si} q N_B \phi_B}}{C_{eff}} \quad (7)$$

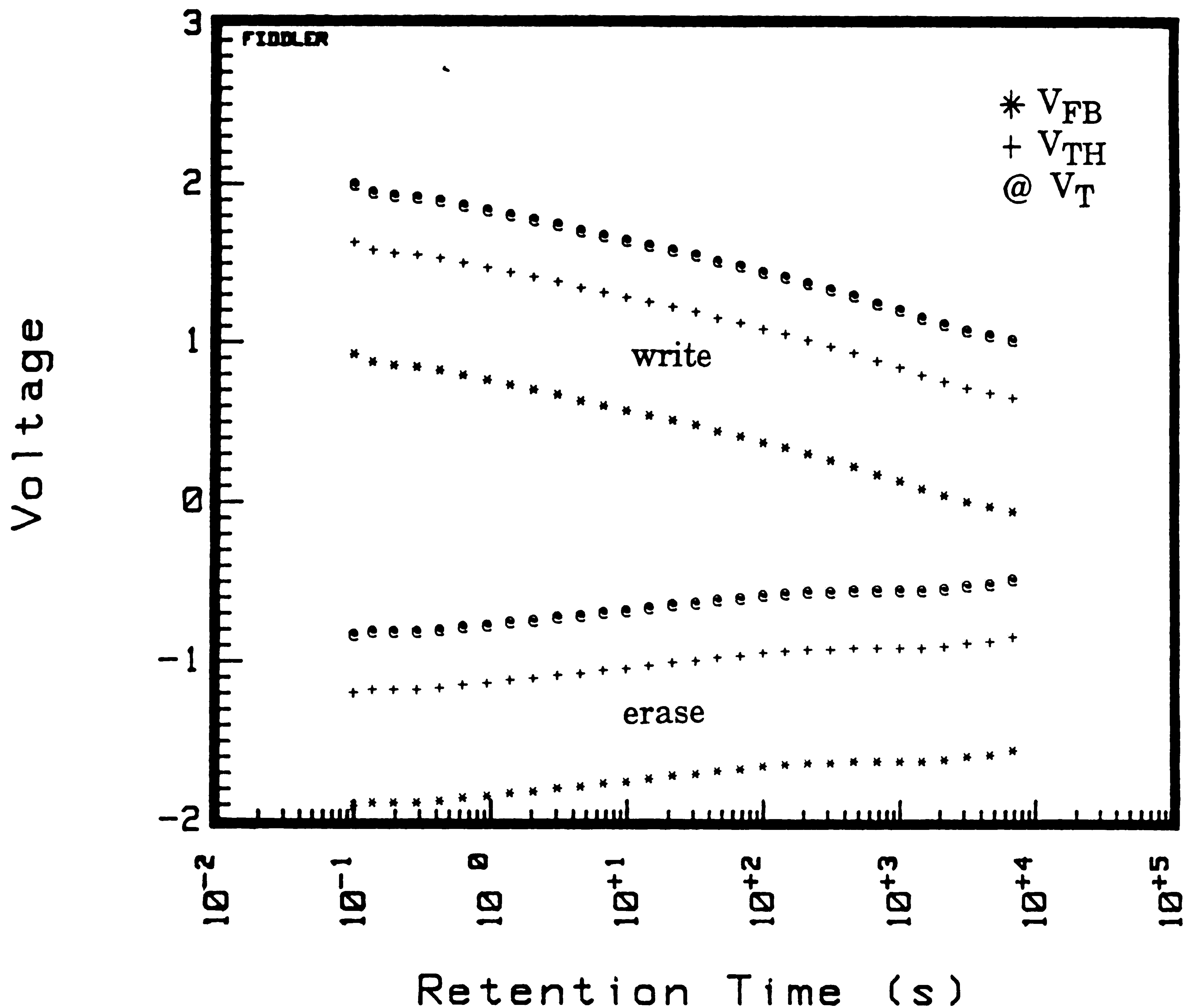


Figure 2-6: Retention Measurement of MONOS capacitor taken with a programming voltage of 5 volts and a pulse width of 10ms measuring V_{FB}(*) and calculating V_{TH}(+) and V_T(@)

Looking at this equation, we can change the threshold voltage by altering the gate to semiconductor workfunction (ϕ_{GS}), the fixed charge in the insulator (Q_f), the bulk potential (ϕ_B), the bulk doping (N_B), the effective insulator capacitance (C_{eff}), or the charge stored in the nitride (Q_N). In my research, I have explored two possible methods to change the memory window. They are (1) employing different gate materials which corresponds to changing ϕ_{GS} and (2) implanting the bulk which corresponds to changing ϕ_B or N_B.

Several different gate materials exist which will provide different gate to semiconductor workfunctions. Presently, the standard process at Lehigh and industry uses a heavily doped n^+ polysilicon gate. If we employ, however, a heavily doped p^+ polysilicon gate then the gate to semiconductor workfunction will be raised by almost the Si bandgap voltage (i.e. 1 volt) which will result in a one volt positive shift in the threshold voltage. Frank Libsch has also shown a higher gate to semiconductor workfunction more effectively blocks electron injection from the gate electrode.[6]

With MOS transistors, an ion implant is frequently used to adjust the threshold voltage. This same procedure can be used with the SONOS device. If the implant is very shallow, then we may approximate the impurity profile with a delta function and the threshold voltage becomes

$$V_{TH} = \phi_{GS} - \frac{Q_f}{C_{eff}} - \left(\frac{x_{ob}}{\varepsilon_{ox}} + \frac{x_n - \bar{x}}{\varepsilon_N}\right)Q_N + 2\phi_B + \frac{\sqrt{4\varepsilon_{si} q N_B \phi_B}}{C_{eff}} + \frac{qD_i}{C_{eff}} \quad (8)$$

where D_i is the implant dose. This equation differs from the original threshold voltage equation (7) by the addition of the term $\frac{qD_i}{C_{eff}}$. In the other limiting case in which a heavy implant is used such that the maximum depletion layer width under heavy inversion is smaller than the implant depth, the threshold voltage can then be expressed by equation (7) in which the bulk doping density N_B and the bulk potential ϕ_B are replaced by the implant doping density.[10]

Chapter 3
Fabrication

The test structures used in my research consist of one set of wafers in which I have both n^+ and p^+ polysilicon gate SONOS transistors with all the other processing steps unchanged, and another set of wafers with MONOS capacitors containing different doses of Boron implanted into the bulk. In this chapter, I will give a detailed description of the fabrication procedures used in making my test structures since the memory window placement varies with different processing conditions.

3.1 Transistors vs. Capacitors

A major decision in studying SONOS devices is whether to use capacitors or transistors. The advantage of using capacitors is the relatively short fabrication time. Only two mask steps are required for capacitors, while n-channel only transistors require 4 mask steps and both n-channel and p-channel (CMOS) transistors require 9 mask steps. Capacitors can be fabricated in less than a week while transistors can take weeks or months to fabricate.

Yet, there are many problems to studying only capacitors. First, only large capacitors of the order of $4x10^3 \mu m^2$ can be used due to noise; while, device sizes more realistic to VLSI applications can be studied with transistors. Because of the large capacitor size, an adequate hydrogen anneal cannot be performed due to the lateral diffusion rate of hydrogen. Most importantly, more realistic device operation can be studied with transistors. Using a transistor, we can measure the threshold voltage instead of just the flatband voltage. Also, subthreshold characteristics can be studied.[11] In taking measurements with capacitors, we have a lack of minority carriers. Strong light is used to attempt

to generate electrons when taking measurements on p-substrate MONOS capacitors, but *there is still insufficient electrons to realistically* study the write characteristics of the memory device and obtain linear voltage ramp measurements at ramp rates much more than 50 mV/sec. This problem is avoided in transistors since the n^+ source/drain in the n-channel device provides a source of electrons.

For my study, I have chosen capacitors to do the implant studies since they can be fabricated quickly. If the chosen implants shift the memory window appropriately in the capacitor structure, then further studies can be done with transistors. For the gate to semiconductor workfunction study, I have used transistor since I was able to do a joint run with another student.

3.2 Capacitor Fabrication

3.2.1 Background

The MONOS capacitors were fabricated using a 2 mask process with 3 inch p-type wafers. The capacitor mask sequence provides three different rectangular capacitors of varying width and length as shown in the photomicrograph of the fabricated devices (fig. 3-1). Figure 3-2 shows the final cross section of these devices, and the detailed process steps to fabricate them are described in section 2.2.2.

This process uses a Boron implant to adjust the memory window with an energy of 15 keV and a dose varying from $3x10^{12}cm^2$ to $15x10^{12}cm^2$. This energy and dose level provide a deep implant. Due to the thin gate dielectric used in this device, a large doping is needed to noticeably shift the threshold voltage, and it is nearly impossible to keep such a large implant near the surface.

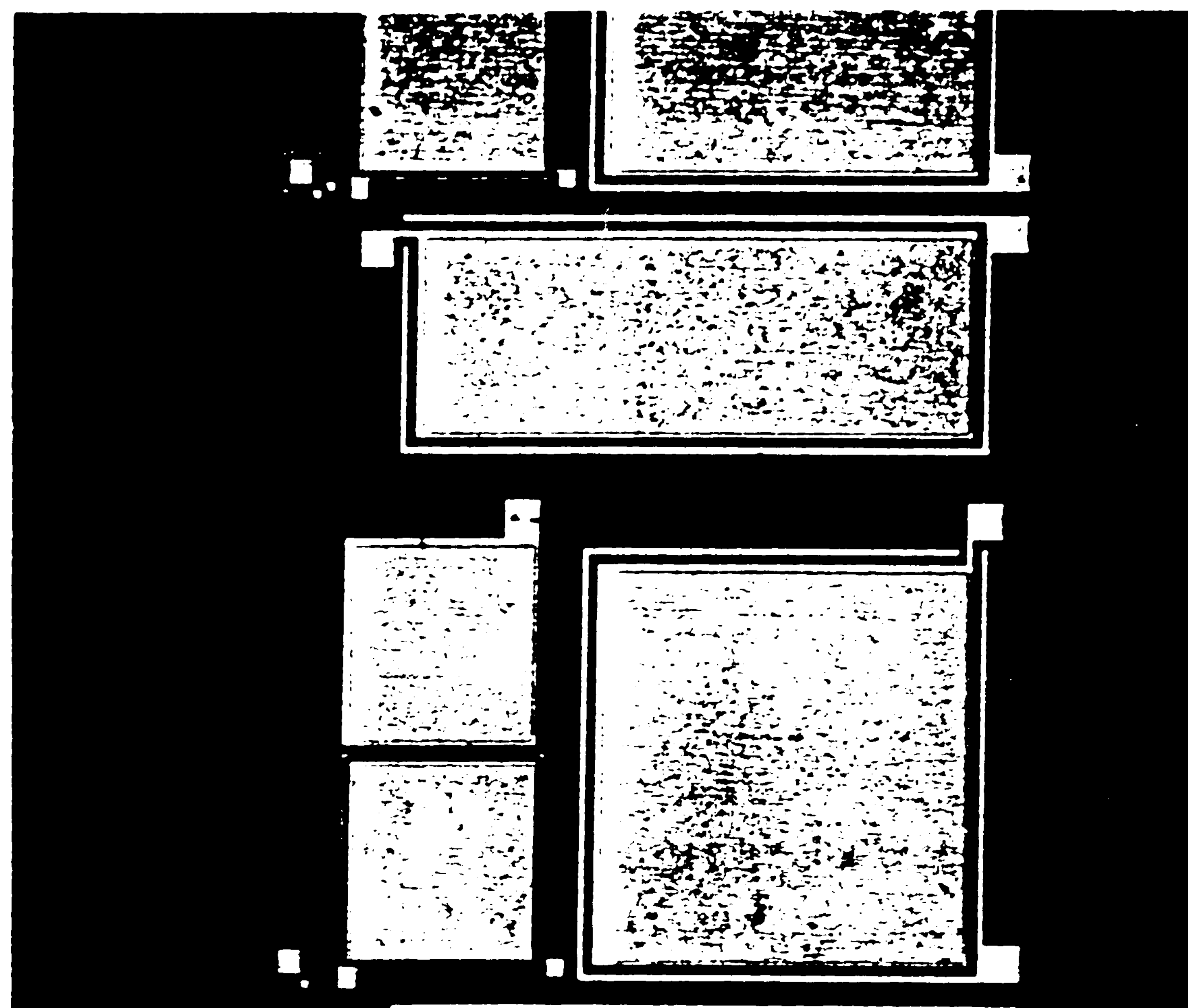


Figure 3-1: Photomicrograph of fabricated capacitor structures

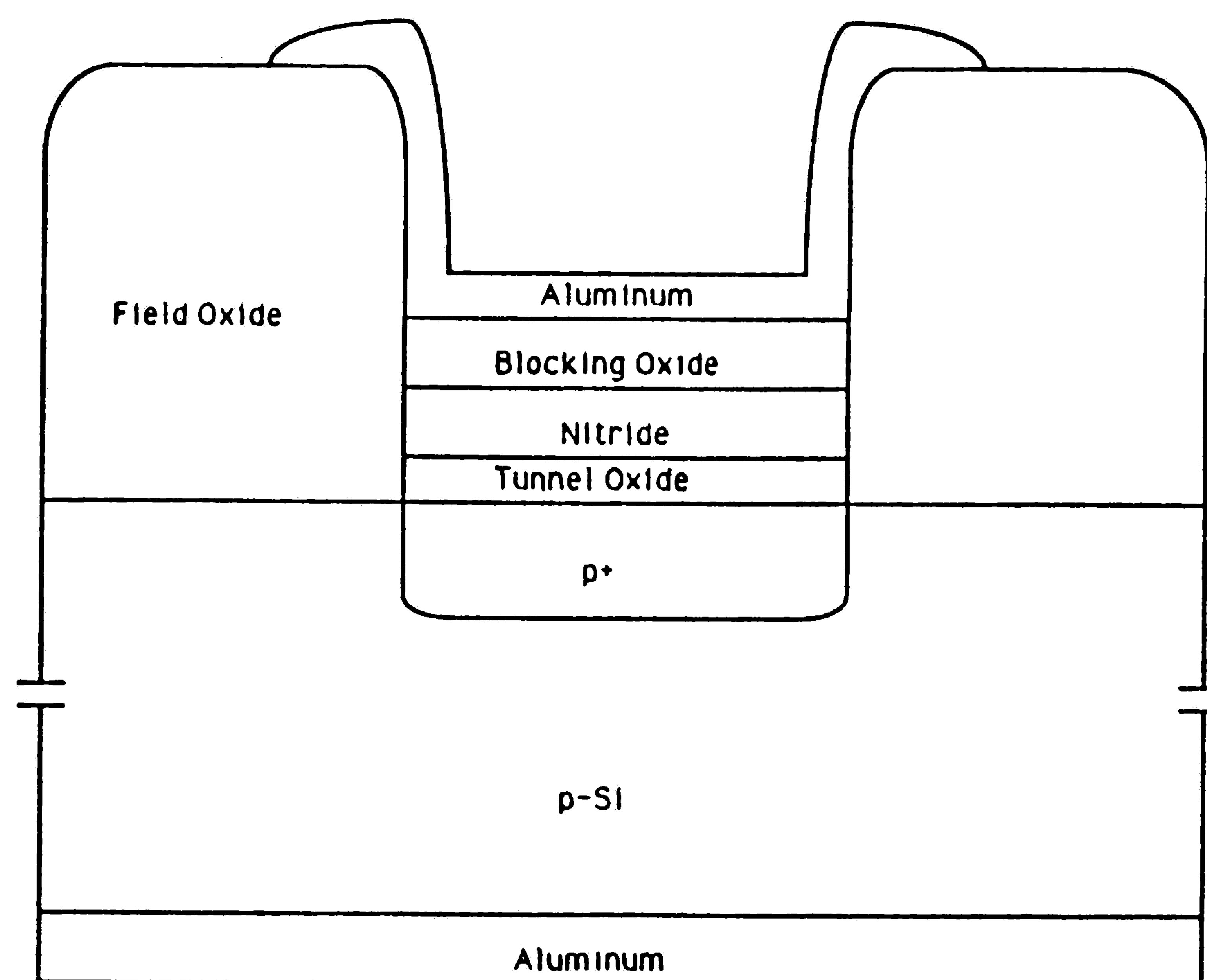


Figure 3-2: Cross Section of Capacitors

3.2.2 MONOS Capacitor Fabrication Sequence

1. Starting material:p-substrate 100, $6.5x10^{15}cm^{-3}$, 3 inch diameter
2. Active Area
    a. Furnace Clean
    b. 2800Å oxide (Wet oxide, 1100°C , 60 min.)
    c. Photo 1 (field oxide)
    d. Etch (2800Å oxide, BHF, 12 min.)
    e. Strip (PR, PRS-2000)
3. Memory Window Adjust Implant
    a. Furnace Clean
    b. 190Å oxide (Dry oxide, 950°C , 25 min.)
    c. Implant (Boron, 15 keV, none to $15x10^{12}cm^{2}$)
    d. Anneal (Dry N_2, 950 °C , 15 min.)
    e. Etch (190Å oxide, BHF, 35 sec.)
4. Triple Dielectric
    a. Furnace Clean
    b. Etch (dilute HF)
    c. 20Å oxide (Dry oxide, 720°C , 11 min.)
    d. 115Å nitride (LPCVD: 0.3 torr, 100 sccm NH_3, 10 sccm $SiCl_2H_2$, 725°C , 6 min. 30 sec.)
    e. 25Å oxide (Wet oxide, 900°C , 120 min.)
5. Metal
    a. 7KÅ Metal (Al, sputtered)
    b. Photo 2 (Metal)
    c. Etch (7KÅ metal, PAN etch, 45 °C , 2 min.)
    d. Strip (PR, PRS-2000)
    e. Etch backside (BHF, 12 min.)
    f. 7KÅ Metal backside (Al, sputtered)
    g. Anneal (H_2/N_2, 400°C , 60 min.)

3.3 Transistor Fabrication

3.3.1 Background

The SONOS transistors are fabricated using the TP-300 mask sequence developed at Lehigh University. The complete process sequence for the n^+ polysilicon transistors is contained in section 2.3.2, and a photomicrograph of the fabricated transistors are shown in fig. 3-3 along with a cross section of the device in fig. 3-4.

The fabrication of the p^+ polysilicon transistor follows the process sequence used by R.Pfiester and L.Parillo[12]. After the gate dielectric is grown, the polysilicon layer is deposited and implanted. Then, a nitride layer is used to prevent subsequent doping of the polysilicon when the source and drain are diffused. Thus, the p^+ polysilicon gate structure follows the same fabrication procedure as the n^+ polysilicon gate except for steps 3 and 4 described in section 2.3.2 which are replaced by steps 1 and 2 discussed in section 2.3.3.

3.3.2 Transistor Fabrication Sequence for n^+ polysilicon gate

1. Starting material: p substrate 100, $6.5x10^{15}cm^{-3}$, 3 inch diameter
2. Active Area
    a. Furnace Clean
    b. 160Å oxide (Dry oxide, 950°C , 20 min.)
    c. Implant back side (Boron, 32 keV, $2x10^{15}cm^2$)
    d. Implant front side (Boron, 32 keV, $1.2x10^{13}cm^2$)
    e. Furnace Clean
    f. Anneal (Dry N_2, 950°C , 30 min.)
    g. Etch (160Å oxide, dilute HF, 30 sec.)
    h. 7000Å oxide (Wet Oxide, 1100°C , 60 min.)
    i. Photo 1 (n^+ S/D, p^+ S/D)
    j. Etch (7000Å oxide, BHF, 8 min.)
    k. Strip (PR, PRS-2000)

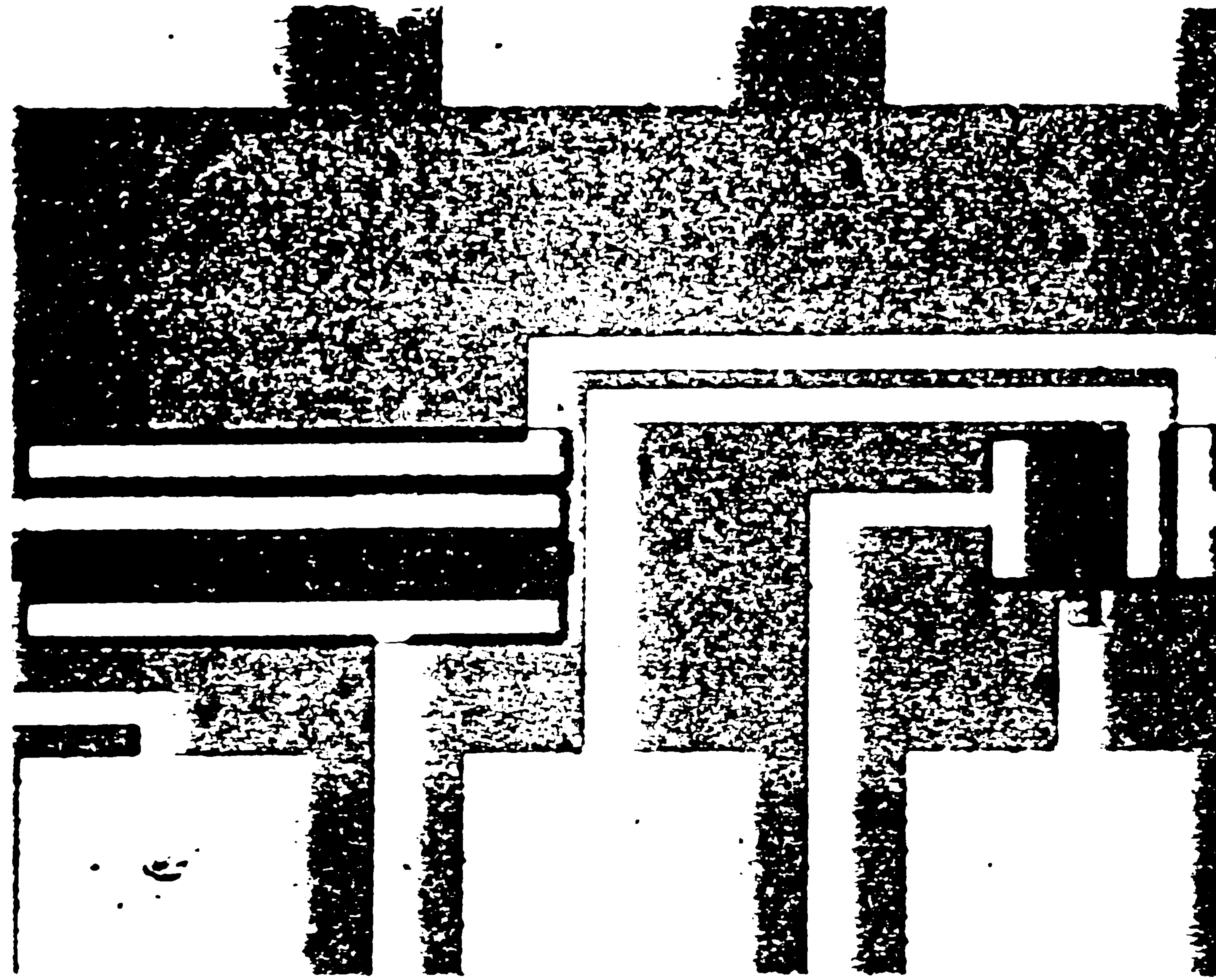


Figure 3-3: Photomicrograph of fabricated transistors

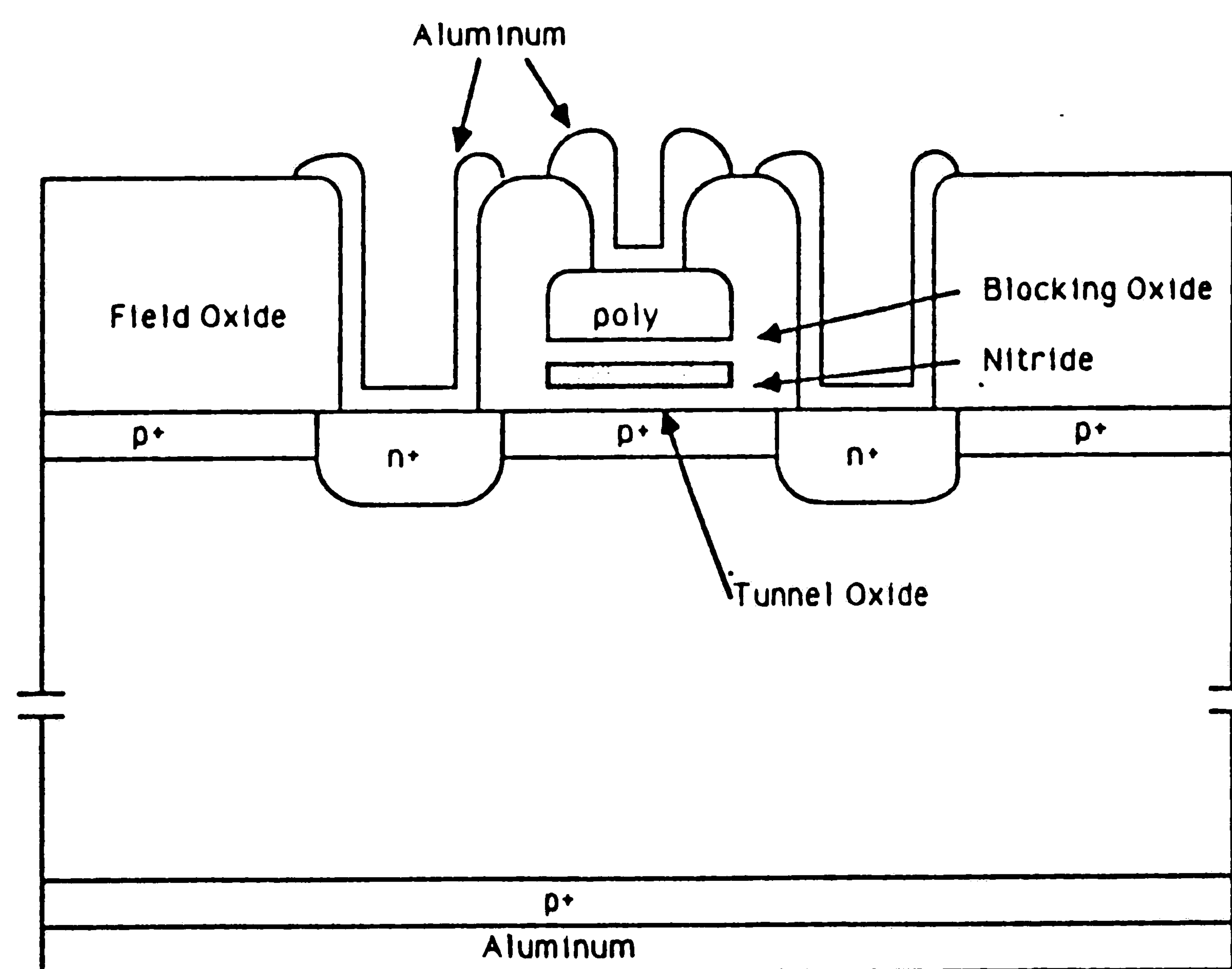


Figure 3-4: Cross Section of Transistors

3. Triple Dielectric
   a. Furnace Clean
   b. Etch (dilute HF)
   c. Anneal (LPCVD: 0.5 torr, 200 sccm NH_3, 725°C , 30 min.)
   d. 20Å oxide (Dry oxide, 720°C , 9 min.)
   e. 117Å nitride (LPCVD: 0.3 torr, 100 sccm NH_3, 11.5 sccm $SiCl_2H_2$, 725°C , 8 min.)
   f. 25Å oxide (Wet oxide, 900°C , 120 min.)
4. Polysilicon
   a. 12KÅ polysilicon (LPCVD: 0.8 torr, 100 sccm N_2, 200 sccm N_2/SiH_4, 625°C , 2 min.)
   b. Etch (4.8KÅ polysilicon, $1HF:26HNO_3:33CH_3COOH$, 2min. 40 sec.)
5. n^+ S/D (self aligned)/Polysilicon doping
   a. Photo 2 (polysilicon)
   b. Etch (7.2KÅ polysilicon, plasma: 0.3 torr, 200W, SF_6, 6 min.)
   c. Strip (PR, PRS-2000)
   d. Furnace Clean
   e. Diffusion ($POCL_3$, 900°C , 20 min.)
   f. Drive-in (Dry N_2, 900 °C , 30 min.)
   g. Etch (p glass, BHF, 15 sec.)
   h. 1200Å oxide (Wet oxide, 900°C , 30 min.)
6. Contact Window
   a. Photo 3 (CW)
   b. Etch (1200Å oxide, BHF, 4 min. 30 sec.)
   c. Strip (PR, PRS-2000)
   d. Furnace Clean
   e. Anneal (H_2/N_2, 900°C , 1 hour)
7. Metal
   a. 7KÅ Metal (Al, sputtered)
   b. Photo 4 (Metal)

c. Etch (7KÅ metal, PAN etch, 45°C , 2 min.)

d. Strip (PR, PRS-2000)

e. Etch backside (Plasma: 0.3 torr, 200 W, SF_6, 5 min.)

f. 7KÅ Metal backside (Al, sputtered)

g. Organic Clean

h. Anneal (H_2/N_2)

3.3.3 Transistor Fabrication Sequence for p+ polysilicon gate

1. Polysilicon/Polysilicon doping

a. 12KÅ polysilicon (LPCVD: 0.8 torr, 100 sccm N_2, 200 sccm N_2/SiH_4, 625°C , 120 min.)

b. Etch (4.8KÅ polysilicon, $1HF{:}26HNO_3{:}33CH_3COOH$, 2 min. 40 sec.)

c. Furnace Clean

d. 180Å oxide (Dry oxide, 900°C , 20 min.)

e. Implant (BF_2, 50 KeV, $2x10^{15}cm^2$)

f. Furnace Clean

g. Anneal (Dry N_2, 900°C , 15 min.)

h. 320Å Nitride (LPCVD: 0.3 torr, 50 sccm NH_3, 50 sccm $SiCl_2H_2$, 725 °C , 10 min.)

2. n^+ S/D (self aligned)

a. Photo 2 (polysilicon)

b. Etch (7.2KÅ polysilicon and 320Å nitride, plasma: 0.3 torr, 200W, SF_6, 6 min.)

c. Strip(PR, PRS-2000)

d. Furnace Clean

e. Diffusion ($POCl_3$, 900°C , 20 min.)

f. Drive-in (Dry N_2, 900°C , 20 min.)

g. Etch (p glass, BHF, 15 sec.)

h. Etch (320Å Nitride, H_3PO_4, 150 °C , 8 min)

i. 1200Å oxide (Wet oxide, 900°C , 30 min.)

3.4 Film Thickness Measurements

3.4.1 Ellipsometry

To measure the thickness of the separate triple dielectric films, a Rudolph EL-II Ellipsometer is used to determine Δ and Ψ. The values of Δ and Ψ are then input into a computer program to determine the film thickness. For accurate measurements of thin films, the refractive index must also be specified as an input to the program. In measuring the tunnel oxide, the refractive index is given as 1.465 and the thickness across the control wafer is 20Å ± 1Å which is fairly uniform.

Three different methods can be used to determine the nitride thickness. In the first, the control wafer is subjected to a NH_3 anneal. A bare wafer which corresponds to a silicon wafer which has been etched in hydroflouric acid, rinsed in DI water, and blown dry in nitrogen, measured after a half hour NH_3 anneal has 11-12Å of oxide and subsequent further anneal does not increase the oxide thickness. After the anneal, the nitride is deposited on top of the 12Å oxide. The thickness of the nitride film can then be found by using a double film thickness program given the known bottom oxide thickness of about 12Å and the refractive indexes of the top and bottom films. This measurement is made on the p^+/n^+ polysilicon gate transistors, and an initial nitride film thickness of 117Å is found.

In the second method, control wafers with a thick oxide are grown, and the oxide thickness is measured. The wafers are then cleaned using the standard RCA clean in which 3-4Å of oxide is lost. Then, the nitride is deposited. Again the thickness of the nitride can be determined using a double film program specifying the bottom oxide thickness as the original oxide thickness minus 4Å and the refractive index of the top and bottom films. This

method will be more accurate than the first method if the bottom oxide thickness is in the middle of the film thickness order. Measuring the MONOS implant adjust capacitors, the initial nitride thickness is found to be 115Å .

Finally, the nitride thickness can also be found by first growing a very thick nitride layer on a bare wafer and measuring this with the ellipsometer. Then, the control wafer is cleaned with a slight loss in nitride thickness. This control is placed in the LPCVD furnace along with the device wafers and the memory nitride is deposited. The thickness of the memory nitride is found by measuring the control again with the ellipsometer and subtracting the known previous thick nitride thickness from this measurement. This method is the most accurate since only a single dielectric is measured with the ellipsometer requiring only the single film program. Yet, thick nitride controls are needed to use this method and they require more effort to make than oxide controls.

To determine the blocking oxide thickness, one starts by placing two control wafers through the first procedure used to find the nitride thickness. One of the controls is then used to determine the nitride thickness. The other is taken immediately from the LPCVD system to the furnace to steam the blocking oxide along with the device wafers. The oxide thickness is then determined by using an iterative procedure. One uses the double film thickness program inputting a guess for the final nitride thickness since some of the nitride is consumed in the steam process and improves this guess until the ratio of the oxide formed to nitride consumed is 1.64. This ratio has been determined by Enomoto et al and is calculated using the densities of nitride and oxide and the fact that 3 moles of SiO_2 are formed per mole of Si_3N_4 consumed[13]. The thickness of the bottom oxide is converted into a nitride thickness and this value is subtracted from the final nitride thickness found by iteration to give the actual nitride thickness. Using this method to measure the blocking oxide

thickness of the p^+/n^+ polysilicon transistors, the final nitride thickness is 94Å with a blocking oxide thickness of 25Å .

3.4.2 Etch Back Experiments

Another method to determine the blocking oxide thickness is also used. Two control wafers are made in which a thick oxide is grown with a nitride layer deposited on top. Both the bottom oxide and top nitride layers are measured on one of the wafers using the methods discussed previously. The other wafer is steamed to form a blocking oxide. The final diagram of this wafer is shown in figure 3-5. The blocking oxide thickness is determined by etching the wafer in a solution of 100:1 water to buffered hydroflouric acid in five second intervals. After each interval, the wafer is measured with the ellipsometer and the thickness of the entire film as an oxide (t_{ox}) is determined. Also, the thickness of the top film as a nitride (t_N) is determined with the known thick bottom control oxide thickness as an input into the program.

Figure 3-5: Control wafer used in etch back experiment

Table of Etch Rate and Thicknesses			
time (sec)	t_{ox} (Å)	Δt_{ox} (Å)	t_N
0	292	11	121
5	281	11	113
10	270	6	105
15	264	4	100
20	260	4	97
25	258	2	95
30	257	1	94
35	256	1	94

Looking at the data in the above table from the MONOS capacitor run with implant adjust, the top oxide is etched at a rate of 11Å per 5 second interval followed by a decrease in the etch rate as the nitride layer is reached. Thus, the final nitride thickness is 94Å, the point at which the etch rate has finished decreasing, corresponding to an oxide thickness of 34Å. These values give a ratio of 1.89 for the ratio of the oxide formed to the nitride consumed. This ratio is different from the theoretical value of 1.64 discussed earlier due to experimental error. First, a double film thickness program must be used with the ellipsometer to measure the film thickness, and this program is not very accurate. Also, two different control wafers are used in this measurement. One is used to obtain the initial nitride thickness and the other is used in the actual etch back experiment. There is a variation between the nitride thickness of adjacent wafers in the LPCVD furnace and the initial nitride thickness obtained from the first control may not be exactly the initial nitride thickness on the etch back control.

3.4.3 Capacitance Measurements

We can confirm the thickness measurements taken with the ellipsometer by capacitance measurements. In the linear voltage ramp measurements, the effective capacitance $C_{eff} = \frac{I_{INV}}{\alpha}$ where I_{INV} is the inversion current and α is the ramp rate. Note that the effective capacitance determines an effective thickness

$$x_{eff} = x_{ot} + x_n \frac{\varepsilon_{ox}}{\varepsilon_N} + x_{ob}$$

where x_{ot} is the tunnel oxide thickness, x_n is the nitride thickness, x_{ob} is the blocking oxide thickness, ε_{ox} is the dielectric permittivity of the oxide, assuming the same permittivity for the blocking oxide and the tunnel oxide, and ε_N is the dielectric permittivity of the nitride.

We can also confirm the thickness measurements using high frequency C-V measurements. In my experiments, this is done with a HP4280A 1MHz C-V meter. The capacitance in accumulation will be equal to the effective capacitance of the device under test.

3.5 Polysilicon Doping Measurements

To verify the polysilicon doping, control wafers with an uniform polysilicon layer deposited on them are used. For the n^+ polysilicon wafers, the controls are subjected to the same doping as the transistors which consists of a $POCl_3$ diffusion of 900°C with a 20 minute predeposition and a 30 minute drive in. Sheet resistance measurements with a 4 point probe set up indicate a resistance of 90.3 ohms per square. Thus, the n^+ polysilicon transistors are heavily doped.

For the p^+ polysilicon control, a thin pad oxide is grown and then the wafer is implanted with BF_2 at an energy of 50 keV and a dose of $2x10^{15}cm^2$. The oxide is then etched and a protective nitride layer of 320Å is deposited. The

wafer is diffused using the same conditions as for the n^+ polysilicon gate to simulate the source/drain formation and the nitride layer is etched. Sheet resistance measurements indicate a value of 3449 ohms per square for this process. This wafer is not heavily doped because the nitride did not protect the p^+ doped polysilicon during the $POCl_3$ diffusion. This conclusion can be supported by literature. Chu et al found that phosphorous pentoxide is reactive toward silicon nitride and can break down the protective nitride layer.[14] Further experiments into protecting the p^+ polysilicon doping from subsequent n^+ diffusion need to be done to optimize this process.

Chapter 4
Results and Analysis

4.1 Quasistatic C-V Measurements of Implant Devices

4.1.1 Linear Voltage Ramp Measurement Set-Up

To observe the memory behavior of the devices quasistatic C-V measurements are used. Figure 4-1 illustrates the block diagram of the linear voltage ramp measurement set-up. The measurements are driven by an HP 9836 computer which allows the user to change the ramp rate and voltage range. Also, the voltage ramp can be stopped by the user at any time. A linear voltage ramp supplied by the function generator is applied to the gate creating a current from the device under test. This current is measured at the bulk using an electrometer and can be expressed as

$$I_G = \frac{dV_{GB}}{dt} I_G = \frac{dQ_G}{dV_{GB}} \frac{dV_{GB}}{dt}$$

$$I_G = \alpha C_{eff} \qquad (1)$$

where α is the ramp rate. Thus, the current is proportional to the capacitance giving the user a quasistatic C-V measurement.

4.1.2 Linear Voltage Ramp Results

Initially static measurements are taken from the MONOS capacitors to see if they work. In these measurements, the voltage ramp is applied to the substrate and the current is read from the gate which is opposite to the set-up discussed previously.

Looking at the results in figure 4-2, one can first verify the dielectric thicknesses measured by the ellipsometer. The current level in inversion and accumulation is $4x10^{-11}$ amps. Using equation (1), this current corresponds to a capacitance of $8x10^{-10}$F or $3.2x10^{-7}$F/cm^2 where the area is $2.5x10^{-3}$cm^2. From

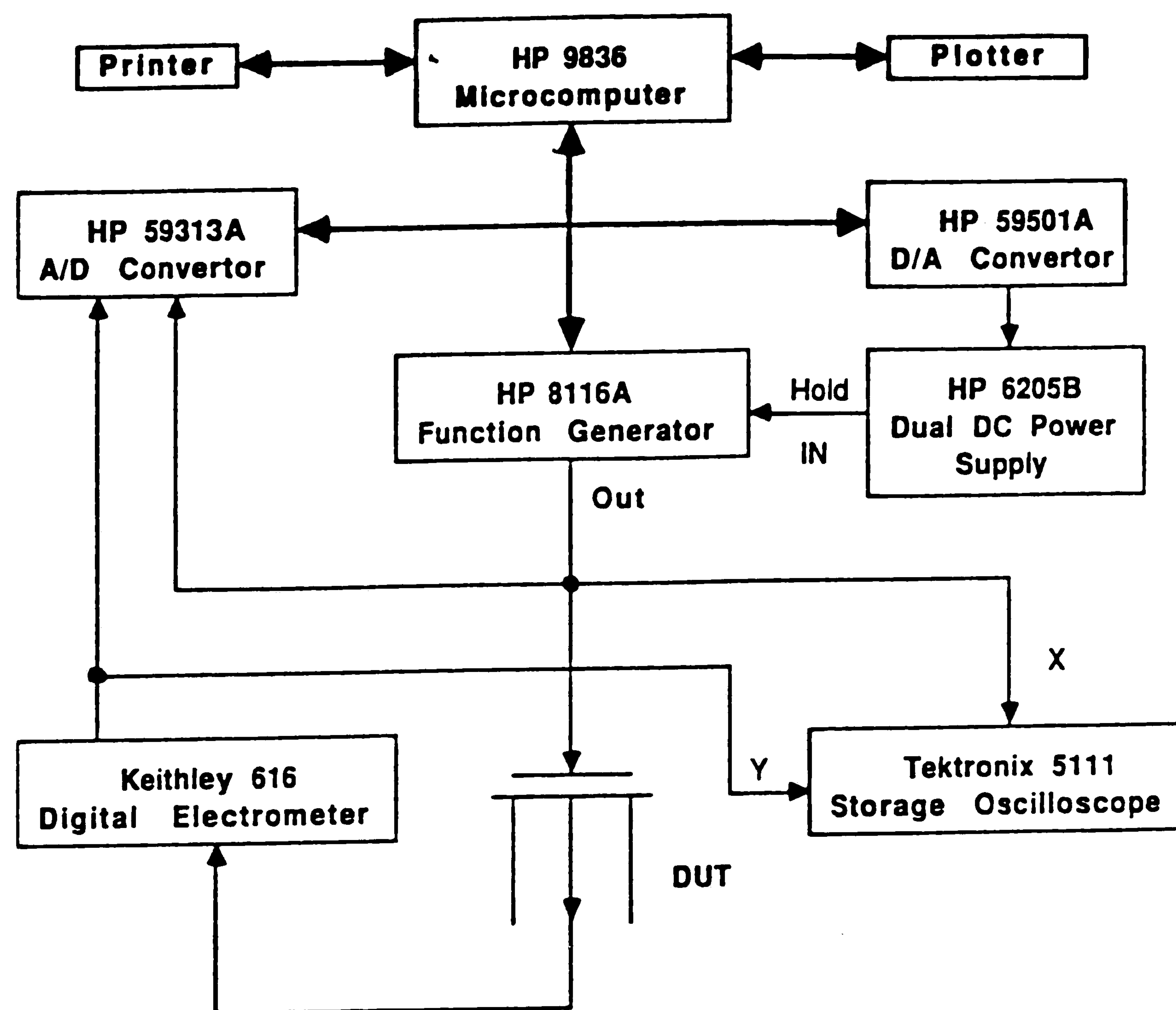


Figure 4-1: Block diagram of the linear voltage ramp set-up

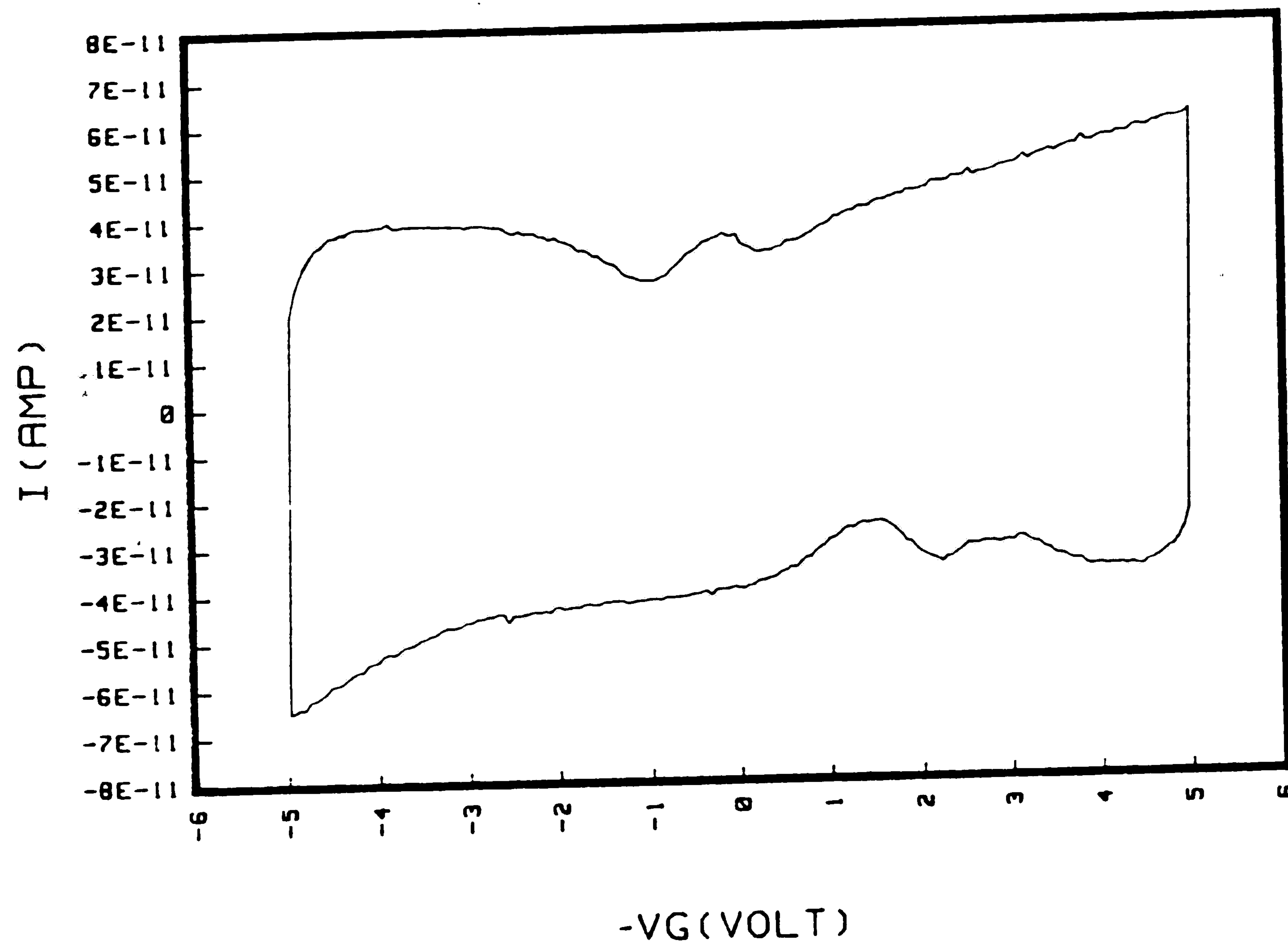


Figure 4-2: Linear voltage ramp measurement on a MONOS capacitor with a ramp rate of 50mV/s for an implant dose of $6x10^{12}$ cm^2

this capacitance, one finds an effective dielectric thickness of 107Å. The dielectric thicknesses measured by the ellipsometer were x_{ot} = 20Å, x_n = 94Å, and x_{ob} = 34Å for an effective thickness of 110Å. Thus, these two different measurement techniques agree on the dielectric thickness within 3Å.

Looking at the I-V plot, the device begins in accumulation at $-V_G = 5$ volts with a capacitance value equal to that of the triple dielectric. As the voltage is decreased from 5 volts to -5 volts corresponding to the negative current portion of the I-V curve since the ramp rate is negative, the device departs from accumulation into depletion, and the capacitance level will decrease as the depletion layer increases. Eventually, the capacitance will increase again back to the effective triple dielectric capacitance as the device enters inversion. The same action will occur in the forward sweep of the voltage as the MONOS capacitor begins in inversion at -5 volts and moves into accumulation at 5 volts.

The decreasing capacitance portions of the plot do not occur at the same point since the device is being programmed as the voltage is swept from -5 to 5 volts and back. This device shows a memory window of about 2.5 volts the difference between the flatband point on the device during the forward and reverse voltage sweeps. The flatband point is found on the decreasing portion of the capacitance plot.

These measurements show the device works except for one strange effect. Instead of a single hump in the capacitance as the device moves from inversion to accumulation, there is a double hump. This second hump cannot be fully explained. The measurements are taken at a low ramp rate of 50 mV/s and a slower ramp rate does not eliminate the second hump. Thus, there does not appear to be any problem due to a nonequilibrium effect.[15] The device is also

illuminated by a strong light source during the measurements to generate minority carriers and keep the device in equilibrium.

The other possible explanation would be the presence of interface traps. A forming gas anneal at 400°C for 30 minutes was performed at the end of the fabrication sequence on the devices to reduce the interface traps. After measuring the devices, a second forming gas anneal was done for another 30 minutes. This subsequent anneal reduced the second hump on some of the devices, especially those with no Boron implant or a very low implant. Thus, I conclude that there must be some interface traps in the wafer which I have not eliminated.

4.2 High Frequency C-V Measurements of Implant Devices

4.2.1 Background

High frequency capacitance versus voltage measurements are taken with a HP 4280A 1MHz CV meter interfaced to a HP 9836 computer. From these measurements, we can determine the initial flatband voltage shift between the nonimplanted wafer and each of the implanted wafers before any programming occurs.

From the high frequency C-V plot for a nonimplanted device (fig. 4-3), we find that the capacitance in accumulation is $8.54x10^{-10}$F or $3.42x10^{-10}$ F/cm^2 where the area of the capacitor is $2.5x10^{-3}$ cm^2. This capacitance corresponds to an effective thickness of 101Å which is in agreement with the triple dielectric thickness measured with the ellipsometer of 110Å where x_{ot} = 20Å , x_n = 94Å , and x_{ob} = 34Å .

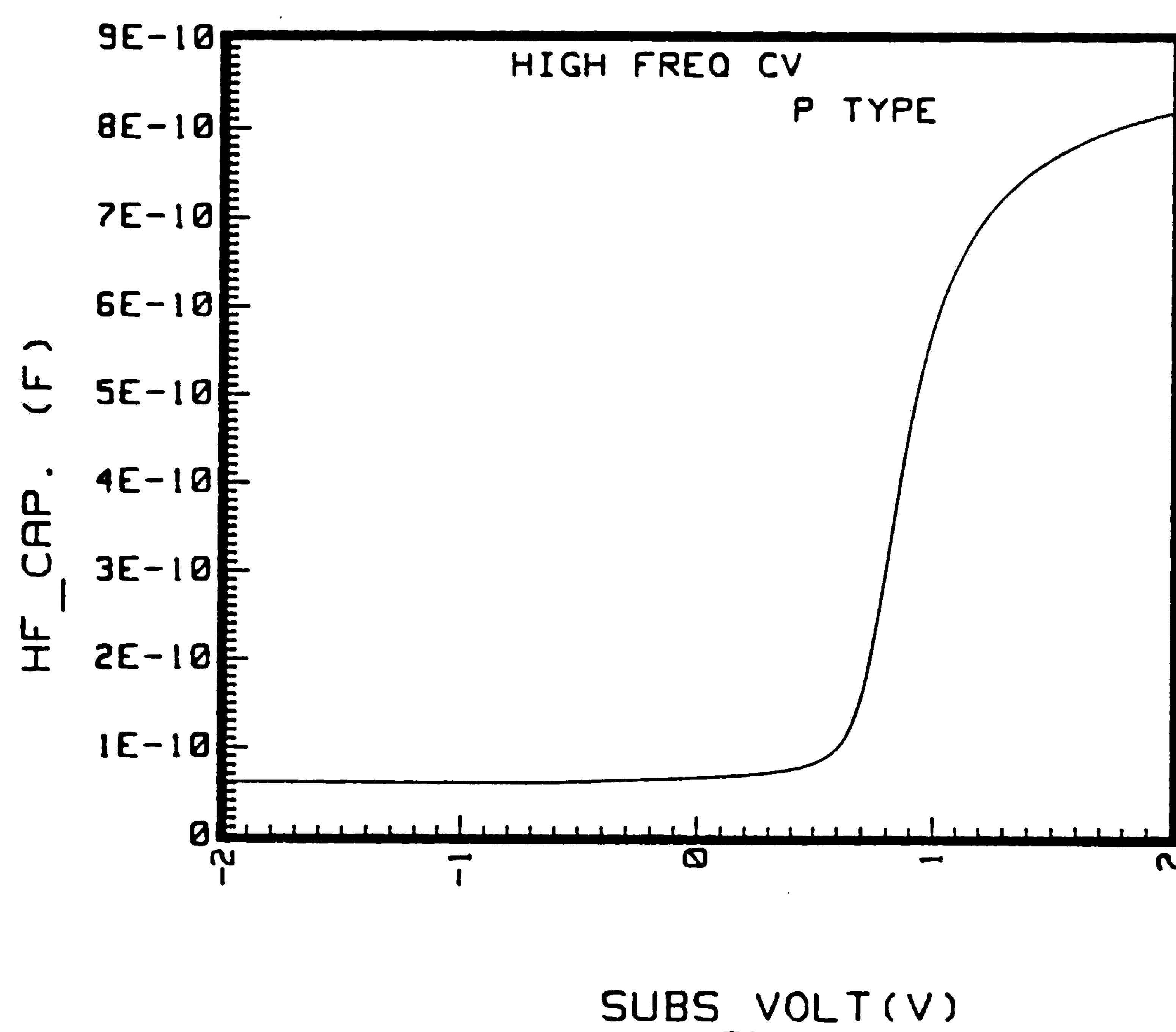


Figure 4-3: High Frequency C-V graph of a nonimplanted MONOS capacitor

4.2.2 Doping Density

Before analytically determining the flatband voltage shift of the wafers, we must find the doping density. One method of finding the doping density is to use the depletion capacitance of the device evaluated at strong inversion $\left(\phi_s(inv) = 2\phi_B\right)$where

$$C_d = \frac{\varepsilon_{si}}{x_d} \tag{2}$$

$$x_d = \sqrt{\frac{2\varepsilon_{si}\phi_s(inv)}{qN_B}} \tag{3}$$

$$\phi_s(inv) = 2\phi_B \tag{4}$$

$$\phi_B = \frac{kT}{q}ln\left(\frac{N_B}{n_i}\right) \tag{5}$$

Using an iterative procedure, one can solve for the doping density N_B assuming a uniform doping. The inversion capacitance for each of the different implant dose conditions is obtained from figure 4-4. In these plots, the inversion capacitance increases as the implant dose is increased.

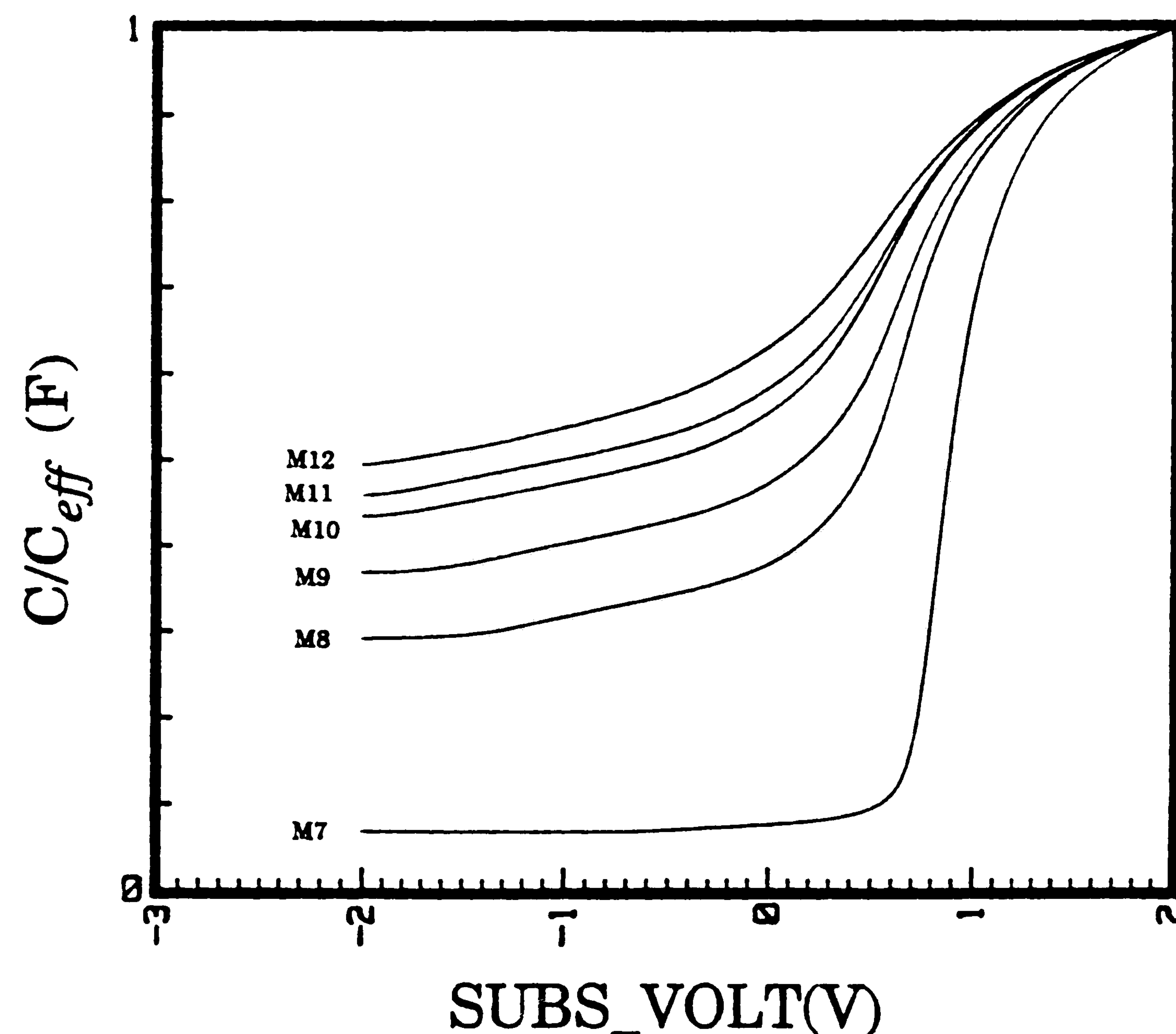


Figure 4-4: High Frequency C-V graphs of implant capacitors with no implant (M7) and an implant dose of $3x10^{12}$ cm^2 (M8), $9x10^{12}$ cm^2 (M10), and $15x10^{12}$ cm^2 (M12)

The doping profile can also be found from the differential capacitance in depletion as discussed in appendix A and from the SUPREM simulation package as discussed in appendix B.

Doping Densities as Determined from				
Implant Dosage	C_{INV}	Differential Capacitance	Corrected Differential Capacitance	SUPREM
$3x10^{12}$	$1.09x10^{17}$	$1.60x10^{17}$	$1.47x10^{17}$	$2.15x10^{17}$
$6x10^{12}$	$1.90x10^{17}$	$3.10x10^{17}$	$3.33x10^{17}$	$4.27x10^{17}$
$9x10^{12}$	$2.31x10^{17}$	$5.00x10^{17}$	$5.08x10^{17}$	$6.36x10^{17}$
$12x10^{12}$	$2.94x10^{17}$	$6.10x10^{17}$	$5.46x10^{17}$	$8.44x10^{17}$
$15x10^{12}$	$3.17x10^{17}$	$8.40x10^{17}$	$7.48x10^{17}$	$1.05x10^{18}$

Using both the differential capacitance and SUPREM to find the doping profile, the results give a fairly uniform profile up to the depletion width such that a uniform doping can be assumed. The table above shows the results of each of these methods. Using the inversion capacitance is an inaccurate method to find the doping density especially for higher implant doses. In future calculations, I will choose to use the doping density found by the differential capacitance using Ziegler's correction.

4.2.3 Flatband Voltage Shift

To determine the flatband voltage shift we must first find the flatband capacitance C_{FB} where

$$C_{FB} = \frac{\varepsilon_{ox}}{x_{eff} + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\lambda_D} \tag{6}$$

where λ_D is the Debye length given by

$$\lambda_D = \sqrt{\frac{kT\varepsilon_{si}}{q^2 N_B}} \tag{7}$$

The calculated values of the flatband capacitance together with the corresponding flatband voltage found from the C-V plots (Fig. 4-4) are shown in the following table.

Implant Dosage	$\frac{C_{FB}}{C_{eff}}$	V_{FB}
none	0.24	-0.76
$3x10^{12}$	0.74	-0.81
$6x10^{12}$	0.81	-0.88
$9x10^{12}$	0.84	-0.86
$12x10^{12}$	0.85	-0.86
$15x10^{12}$	0.87	-0.90

The flatband voltage is given by

$$V_{FB} = \phi_{GS} - \frac{Q_f}{C_{eff}} \tag{8}$$

where Q_f is the fixed oxide charge and

$$\phi_{GS} = \phi_G - \chi_{si} - \frac{1}{2q}E_G - \phi_B \tag{9}$$

given ϕ_G is the gate potential, χ_{si} is the electron affinity of silicon ,E_G is the energy band gap, and ϕ_B is the bulk potential where

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right) \tag{10}$$

Assuming Q_f is a fixed value then

$$\Delta V_{FB} = -\Delta\phi_B \tag{11}$$

The measured value of ΔV_{FB} agrees fairly well with the calculated value of ΔV_{FB} where the nonimplanted wafer is used as the reference (Fig. 4-5).

4.2.4 Voltage Shift at $C = 0.7\ C_{eff}$

It is also interesting to analytically verify the shift in the voltage ($V_{0.7}$) where $C = 0.7C_{eff}$. Now

$$V_{0.7} = V_{FB} + \phi_s - \frac{Q_S}{C_{eff}} \tag{12}$$

where ϕ_s is the surface potential and Q_S is the charge in the silicon. To determine ϕ_s, we can first write that

$$\frac{1}{C} = \frac{1}{1 + \frac{C_{eff}}{C_d}}$$

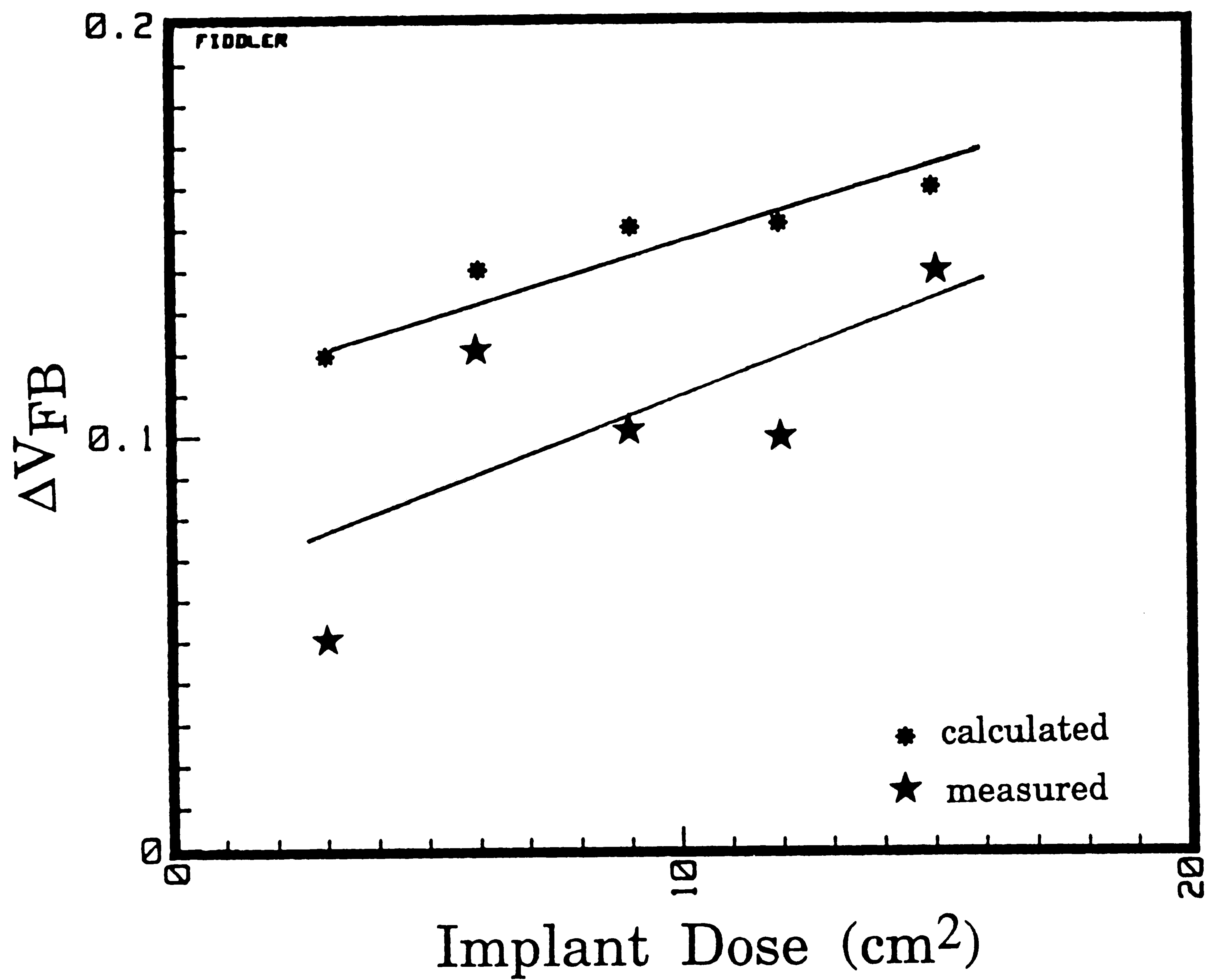


Figure 4-5: Plot comparing the change in V_{FB} for various implant doses with a reference of no implant as determined from high frequency C-V measurements and analytical calculations

$$C_d = \frac{C_{eff}}{\frac{C_{eff}}{C} - 1} \tag{13}$$

where C_d is the depletion capacitance and can be expressed using the depletion approximation as

$$C_d = \sqrt{\frac{qN_B\varepsilon_{si}}{2\phi_s}} \tag{14}$$

Combining equation (13) and (14) we find

$$\phi_s = \frac{qN_B\varepsilon_{si}\left[\frac{C_{eff}}{C} - 1\right]}{2C_{eff}^2} \tag{15}$$

Letting C = 0.7 C_{eff}

$$\phi_s = \frac{qN_B\varepsilon_{si}}{2[2.33\,C_{eff}]^2} \tag{16}$$

Also using the depletion approximation

$$Q_S = \sqrt{2\varepsilon_{si}qN_B\phi_s} \tag{17}$$

Now the change in reference voltage can be expressed as

$$\Delta V_{0.7} = V_{0.7}(2) - V_{0.7}(1) \tag{18}$$

Substituting equation (12)

$$\Delta V_{0.7} = V_{FB2} - V_{FB1} + \phi_{s2} - \phi_{s1} - \frac{Q_{S2} - Q_{S1}}{C_{eff}} \tag{19}$$

Substituting equations (5),(11),(16), and (17)

$$\Delta V_{0.7} = \frac{kT}{q}ln\left(\frac{N_{B1}}{N_{B2}}\right) + \frac{q\varepsilon_{si}(N_{B2} - N_{B1})}{2[2.33\,C_{eff}]^2} + \frac{q\varepsilon_{si}}{2.33\,C_{eff}}[N_{B2} - N_{B1}] \tag{20}$$

We cannot use this equation for the nonimplanted wafer since the depletion approximation is not valid. Yet, comparing the analytical and measured results for the remaining wafers where the wafer with an implant dose of $3x10^{12}$ is the reference gives very good agreement (Fig. 4-6).

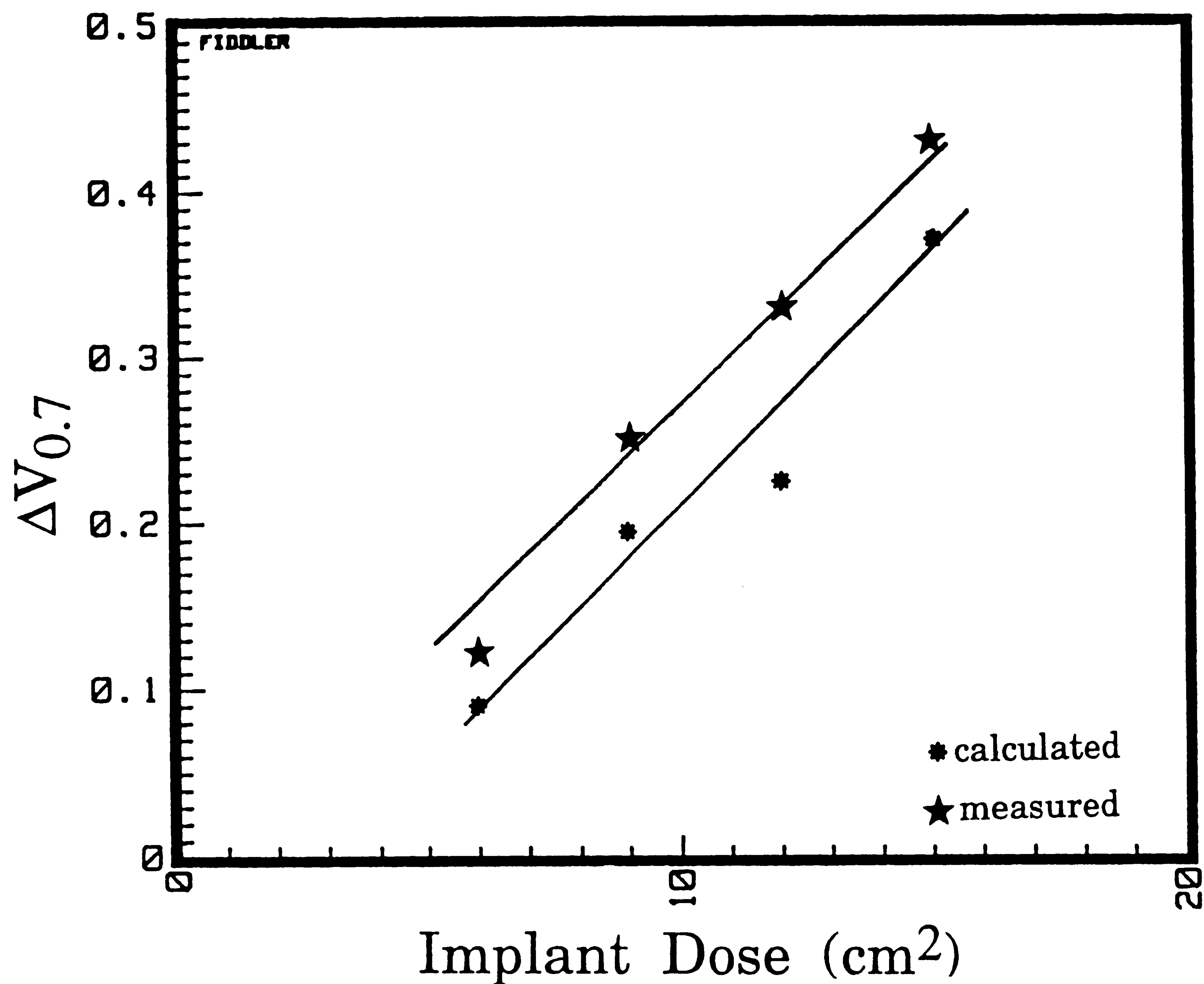


Figure 4-6: Plot of the change in $V_{0.7}$ for various implant doses with a reference dose of $3x10^{12}$ cm^2 as determined from high frequency C-V measurements and analytical calculations

4.3 Dynamic C-V Measurements of Implant Devices

4.3.1 Pulsed Capacitor Measurement Set-Up

Erase/write and retention measurements are made with a V_{FB} tracking scheme. A block diagram of the measurement set-up is shown in figure 4-7. Relays S1 through S3 and the control signals (PROG, READ, and V_{REF}) are biased by the HP 6205B power supplies which are programmed by the HP9836 computer through HP 59501A D/A convertors.

When programming the device, relay S3 is in the closed position such that the V_{FB} tracking mechanism is disconnected and relay S2 is in the "1" position such that the LO-TEST input of the Boonton capacitance meter is floating. The programming pulse is provided by the HP 8116 function generator. Relay S1 determines the pulse amplitude polarity, and the pulse width and amplitude can be adjusted from the computer. The high state of the PROG control signal will trigger the function generator after a 7ms delay.

To read the device, relay S3 is in the open position and relay S2 is in the "0" position. The device under test is connected between the TEST inputs of the Boonton capacitance meter such that $\frac{\partial V_{OUT}}{\partial V_{BIAS}} \geq 0$. Thus, an n substrate is connected to the HI-TEST input and a p substrate is connected to the LO-TEST input. The differentiator (OP1) between V_{REF} and V_{OUT} and the integrator (OP2) establish a feedback loop which converges to a capacitance value proportional to V_{REF}. V_{OUT} is proportional to the test capacitance for a given bias and V_{REF} is proportional to a reference capacitance which is usually the flatband capacitance. For further information about this measurement set-up, see Dr. Anirban Roy's Ph.D. Dissertation.[16]

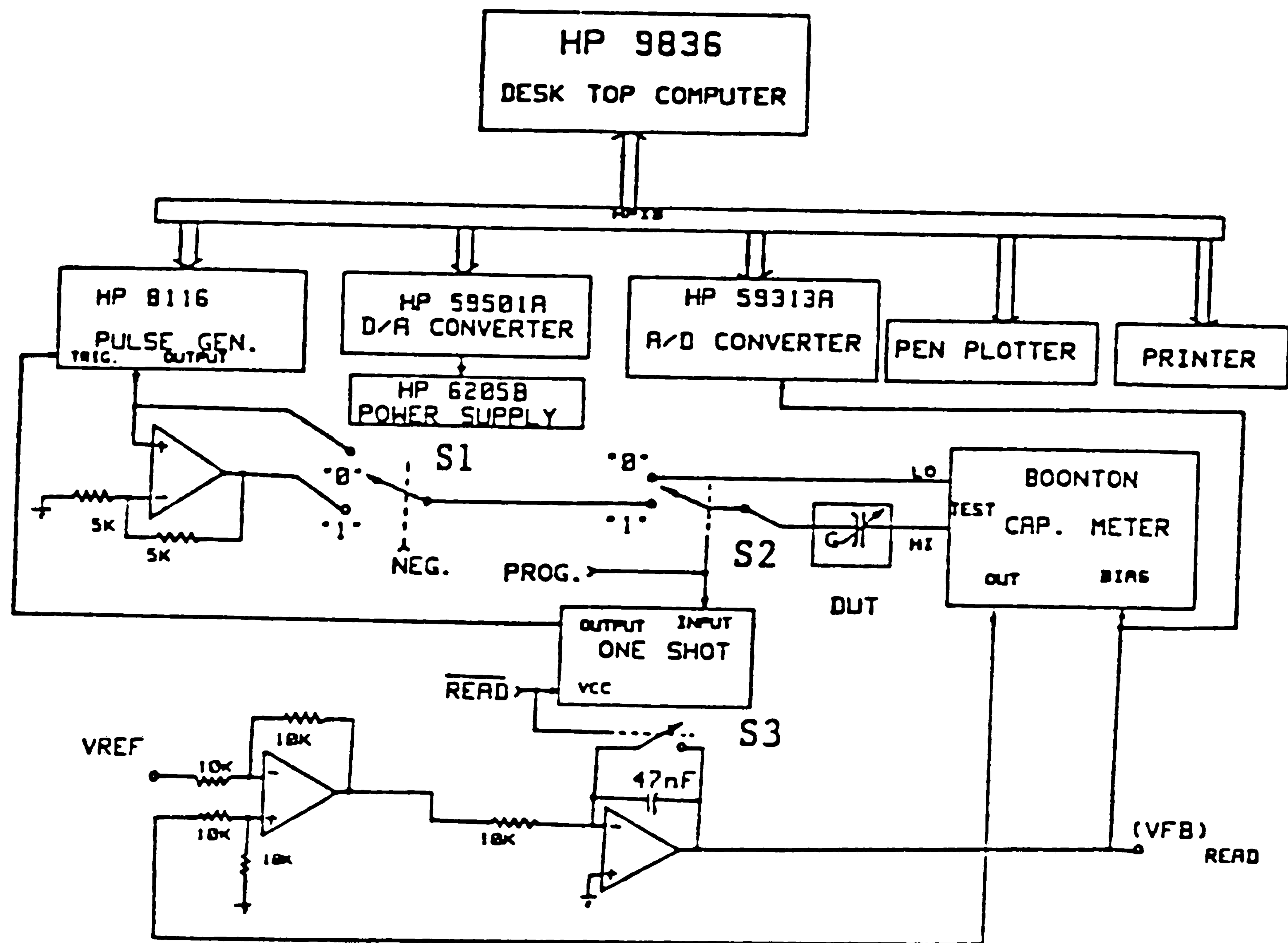


Figure 4-7: Diagram of pulsed capacitor measurement set-up

4.3.2 Retention Measurements

Initially, retention measurements are taken with $C_{ref} = 0.7C_{eff}$. The results are plotted in figure 4-8. One can see a positive shift in the memory window with implant as predicted by the measurement of V_{REF} before programming discussed in section 3.1.4. In the erased state, the voltage shift is two times more than the initial shift in V_{REF}. Yet, in the written state, the voltage shift is one-half the initial shift in V_{REF}. This latter effect is due to a lack of minority carriers. When the wafer is implanted, the decay rate is less than that of a nonimplanted device.

These measurements are taken with the capacitor in accumulation or depletion and should really be taken at flatband. Thus, the measurements are retaken with $C_{ref} = C_{FB}$ where the flatband capacitance is found using the method discussed in section 3.1.3. For the nonimplanted wafer, the memory window should shift positive in reference to the previous measurement by 0.26 volts as predicted from looking at the initial HF C-V measurements. Actual measurements indicate this shift in memory window as shown in figure 4-9. For an implant dose of $15x10^{12}$, the memory window should shift negative by 0.6 volts with respect to the measurement at $C_{ref} = 0.7C_{eff}$ and actual measurements also show this shift (Figure 4-10). When the measurements are taken in flatband, the decay of the window over time is increased as compared to measurements taken in accumulation as shown for the nonimplanted wafer and the decay is decreased as compared to measurements taken in depletion as shown for the implanted wafer. The decay rate for the implanted device is still less than that for a nonimplanted device. Thus, a Boron implant used to shift the memory window towards a more positive voltage level improves the retention characteristics of the device

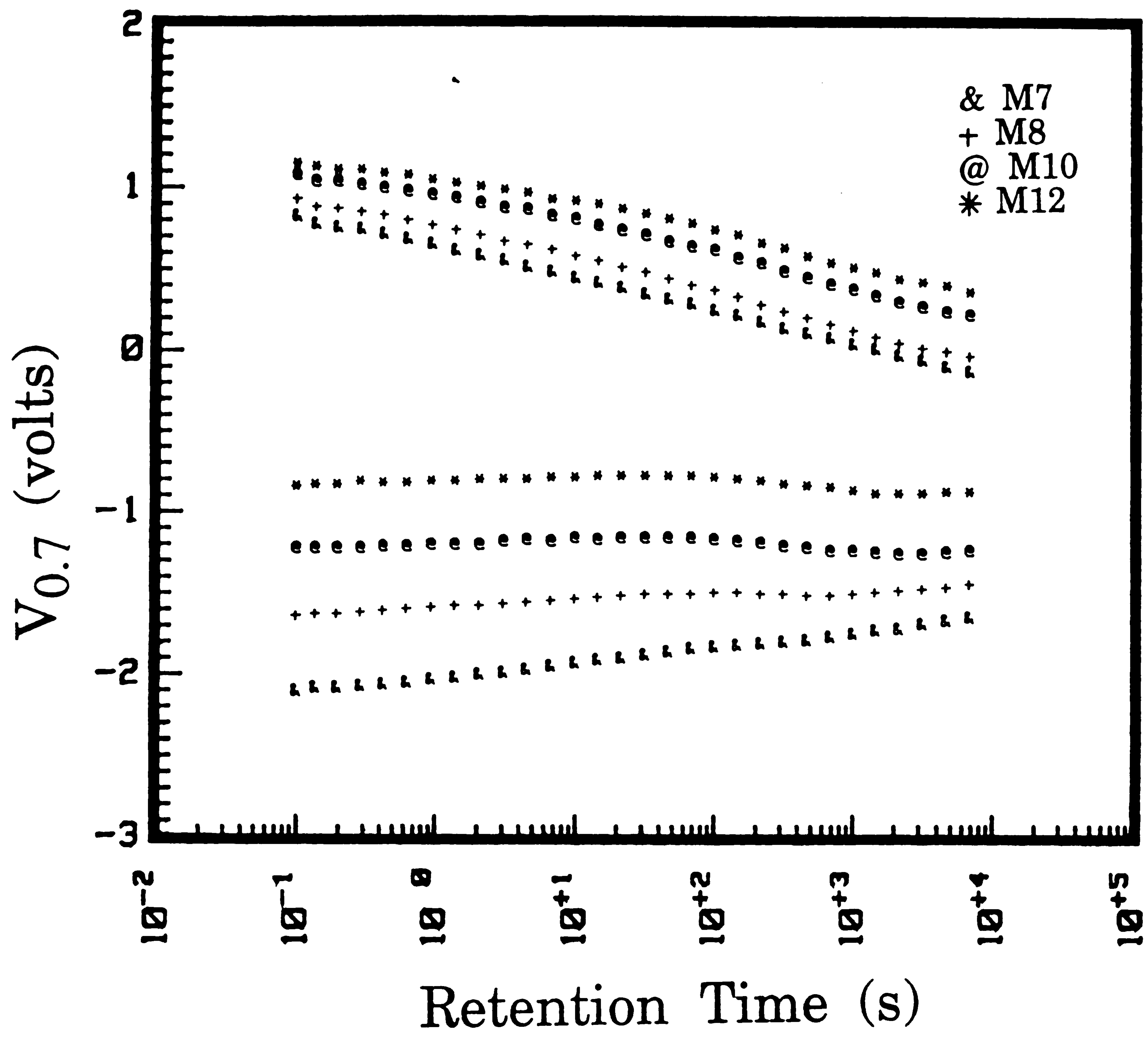


Figure 4-8: Retention measurement of MONOS capacitors taken with a programming voltage of 5 volts, a pulse width of 10ms and C_{ref}=0.7C_{eff} for no implant (M7) and an implant dose of 3x10^{12} cm^2 (M8), 9x10^{12} cm^2 (M10), and 15x10^{12} cm^2 (M12)

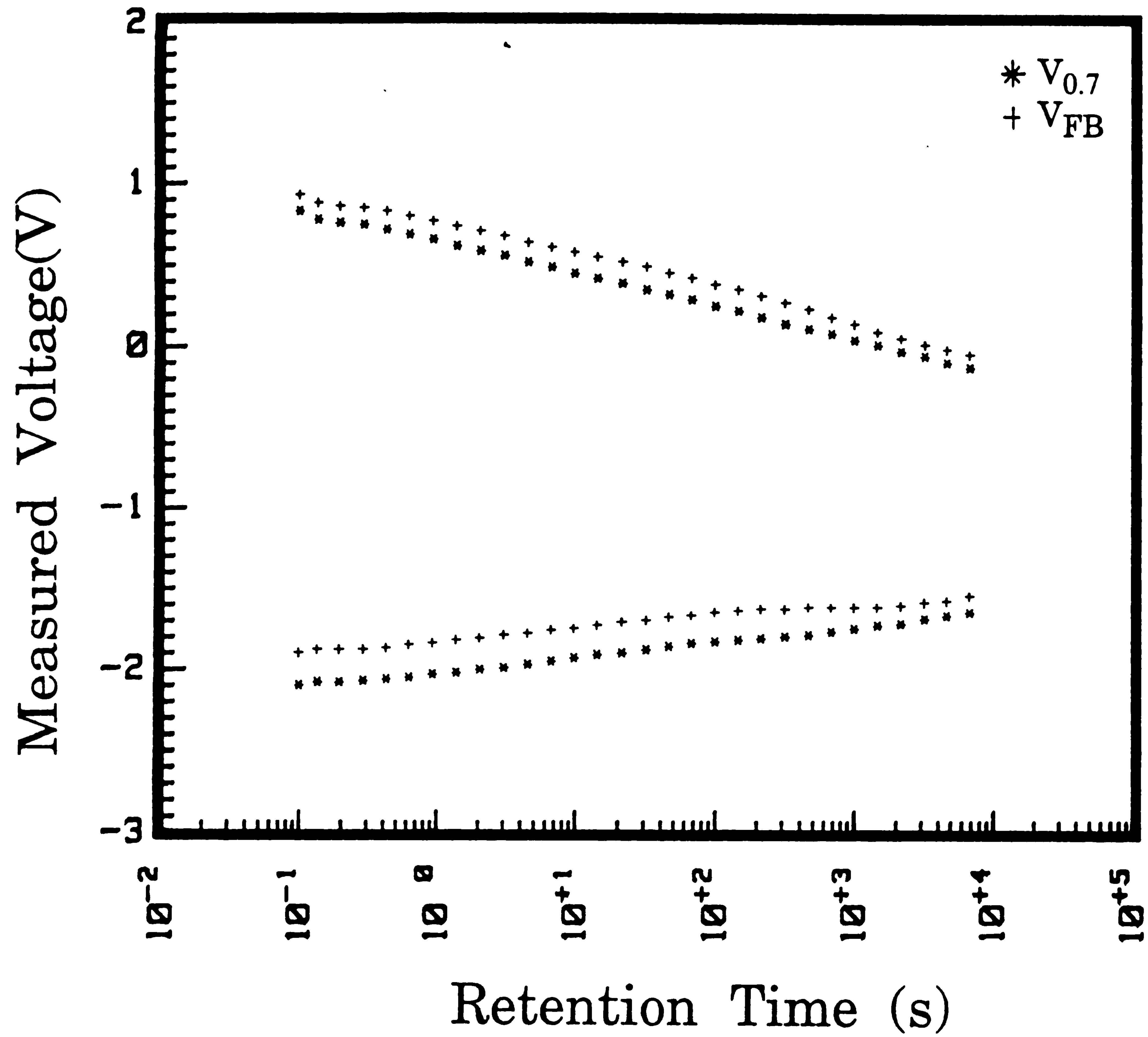


Figure 4-9: Retention measurement of a MONOS capacitor with no implant adjust taken at $C_{ref}=0.7C_{eff}$ (*) and $C_{ref}=C_{FB}$ (+) for a programming voltage of 5 volts and a pulse width of 10ms

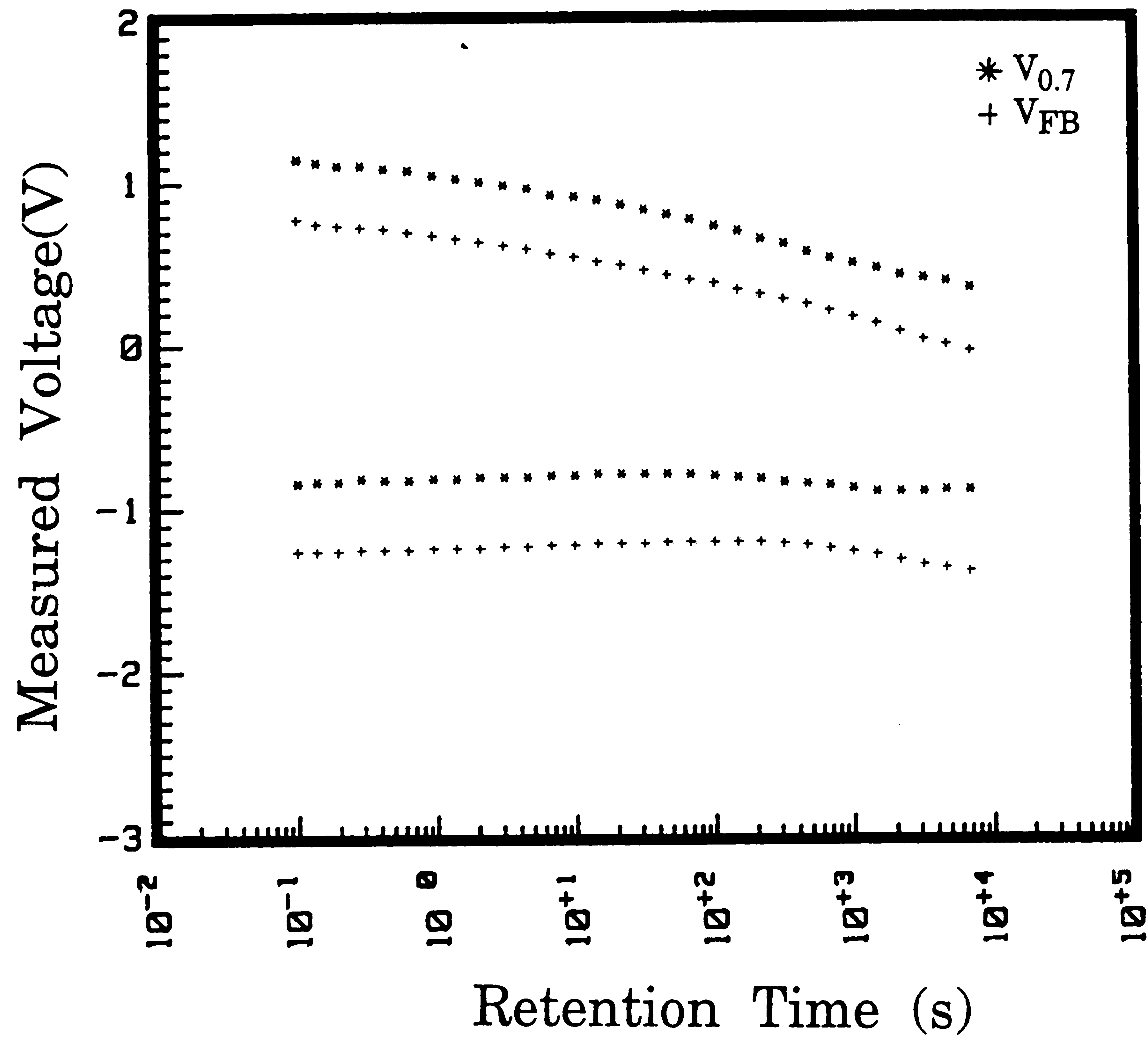


Figure 4-10: Retention measurement of a MONOS capacitor with an implant dose of $15x10^{12}$ cm^2 taken at $C_{ref} = 0.7C_{eff}$ (*) and $C_{ref} = C_{FB}$ (+) for a programming voltage of 5 volts and a pulse width of 10ms

We can now predict the memory window at V_{FB} for those wafers not measured and then calculate the memory window at V_{TH} using the equation

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_{si} q N_B \phi_B}}{C_{eff}} \quad (21)$$

A plot of the initial window for $V_{0.7}$, V_{FB}, and V_{TH} is shown in figure 4-11.

4.3.3 Erase/Write Measurements

Figure 4-12 shows the erase/write data taken with $C_{ref} = 0.7C_{eff}$. This data also shows a positive shift in the memory window with the erased state shifting more than the written state. The crossover time of the erase and write curves which is an indication of programming speed increases with implant dose from 68 ms for no implant to 316 ms for the maximum implant dose.

When the data is retaken with $C_{ref} = C_{FB}$, the memory window shifts positive for the nonimplanted device and the crossover time is increased (Fig. 4-13). The device with an implant dose of $15x10^{12}$ has a memory window which shifts negative and a crossover time which decreases (Fig. 4-14). Yet, the crossover time is still increasing between the nonimplanted and implanted devices. The crossover time is an indication of the speed of the device. thus, an implanted device will require longer programming times than the nonimplanted device. Still, the crossover time only increases by 200ms for the highest implant dose which may not be a significant problem in some applications.

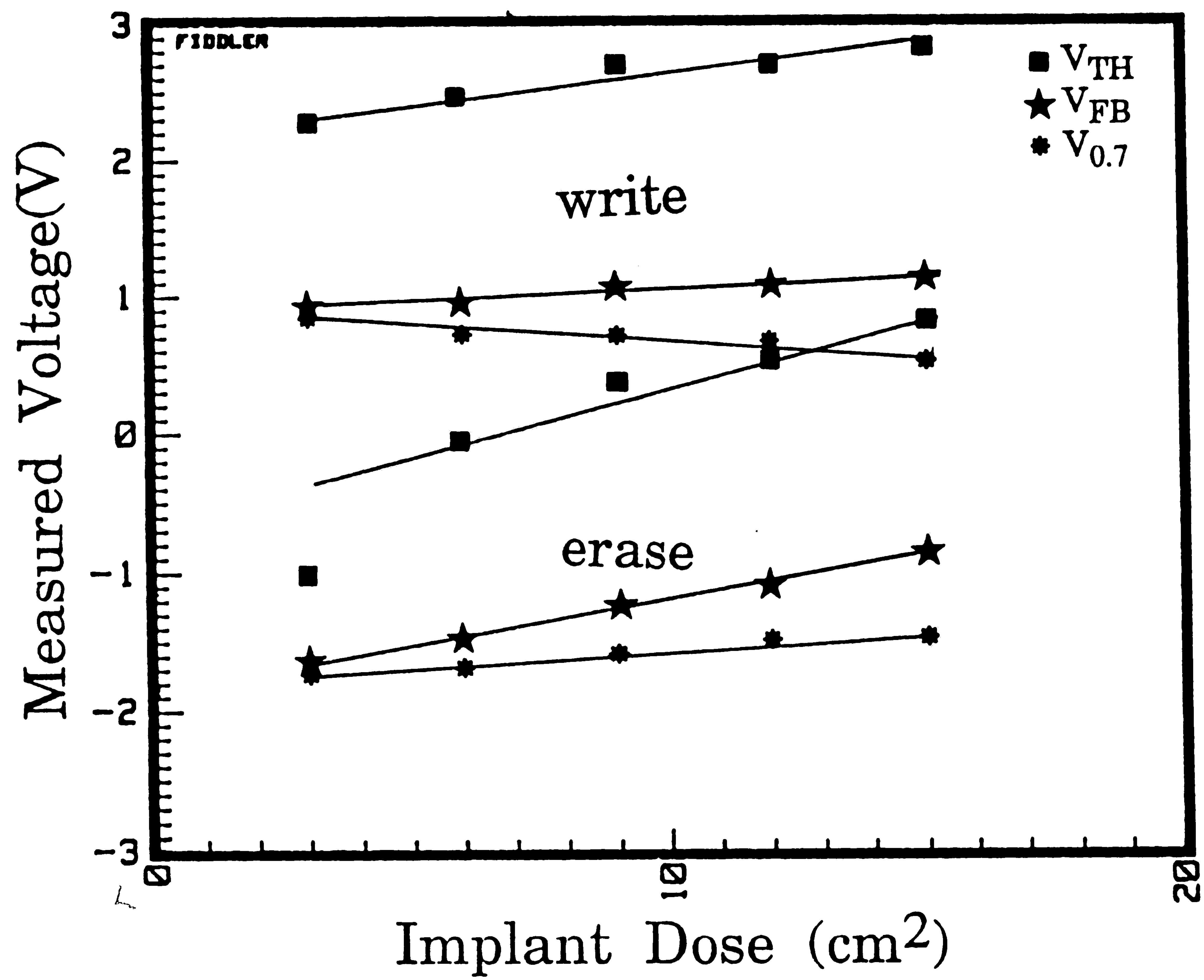


Figure 4-11: Plot of V_{FB}, $V_{0.7}$, and V_{TH} for various implant doses

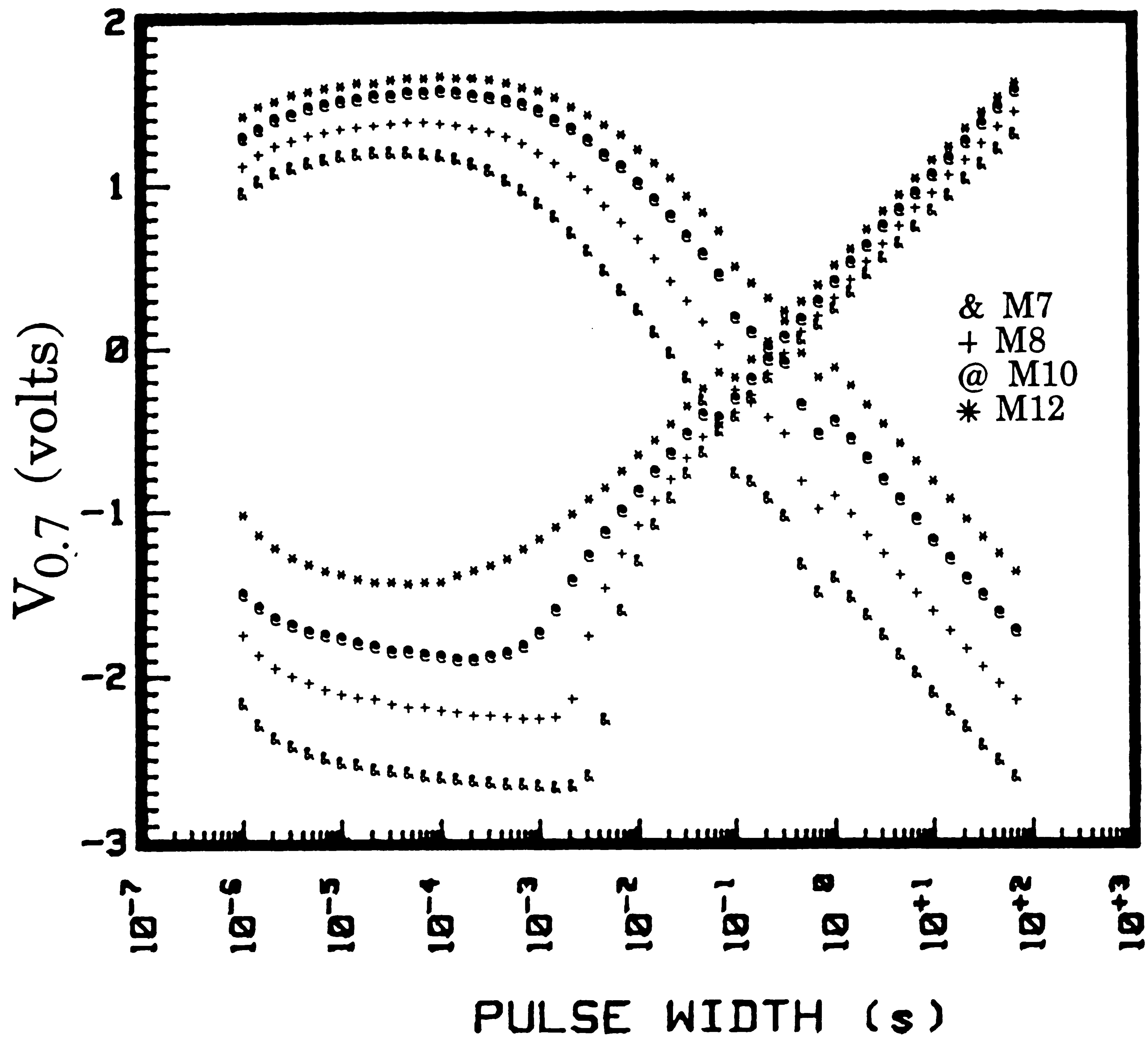


Figure 4-12: Erase/Write measurement of MONOS capacitors taken with a programming voltage of 5 volts, a pulse width of 10ms and C_{ref}=0.7C_{eff} for no implant (M7) and an implant dose of 3x10^{12} cm^2 (M8), 9x10^{12} cm^2 (M10), and 15x10^{12} cm^2 (M12)

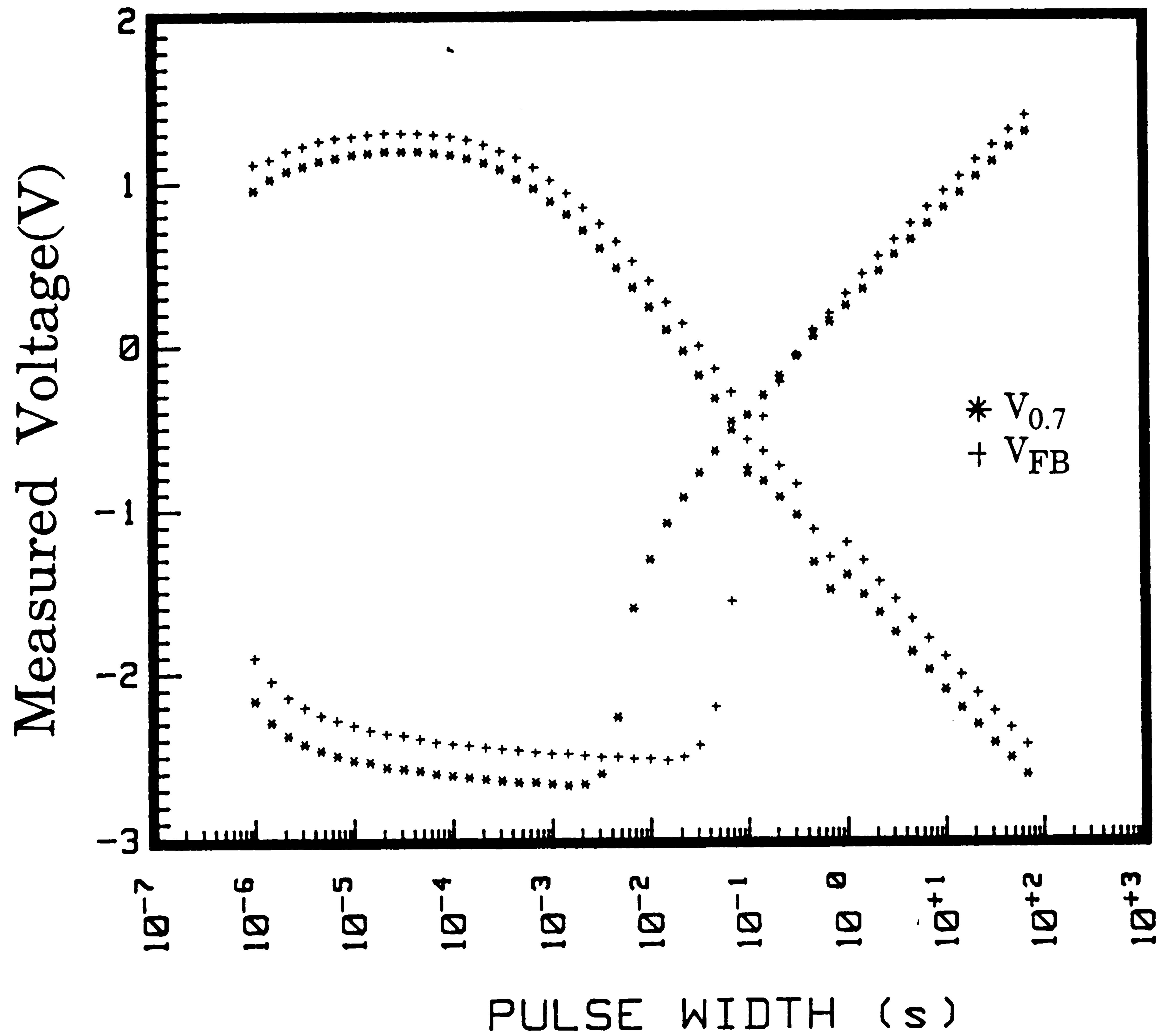


Figure 4-13: Erase/Write measurement of a MONOS capacitor with no implant adjust taken at $C_{ref} = 0.7C_{eff}$ (*) and $C_{ref} = C_{FB}$ (+) for a programming voltage of 5 volts and a pulse width of 10ms

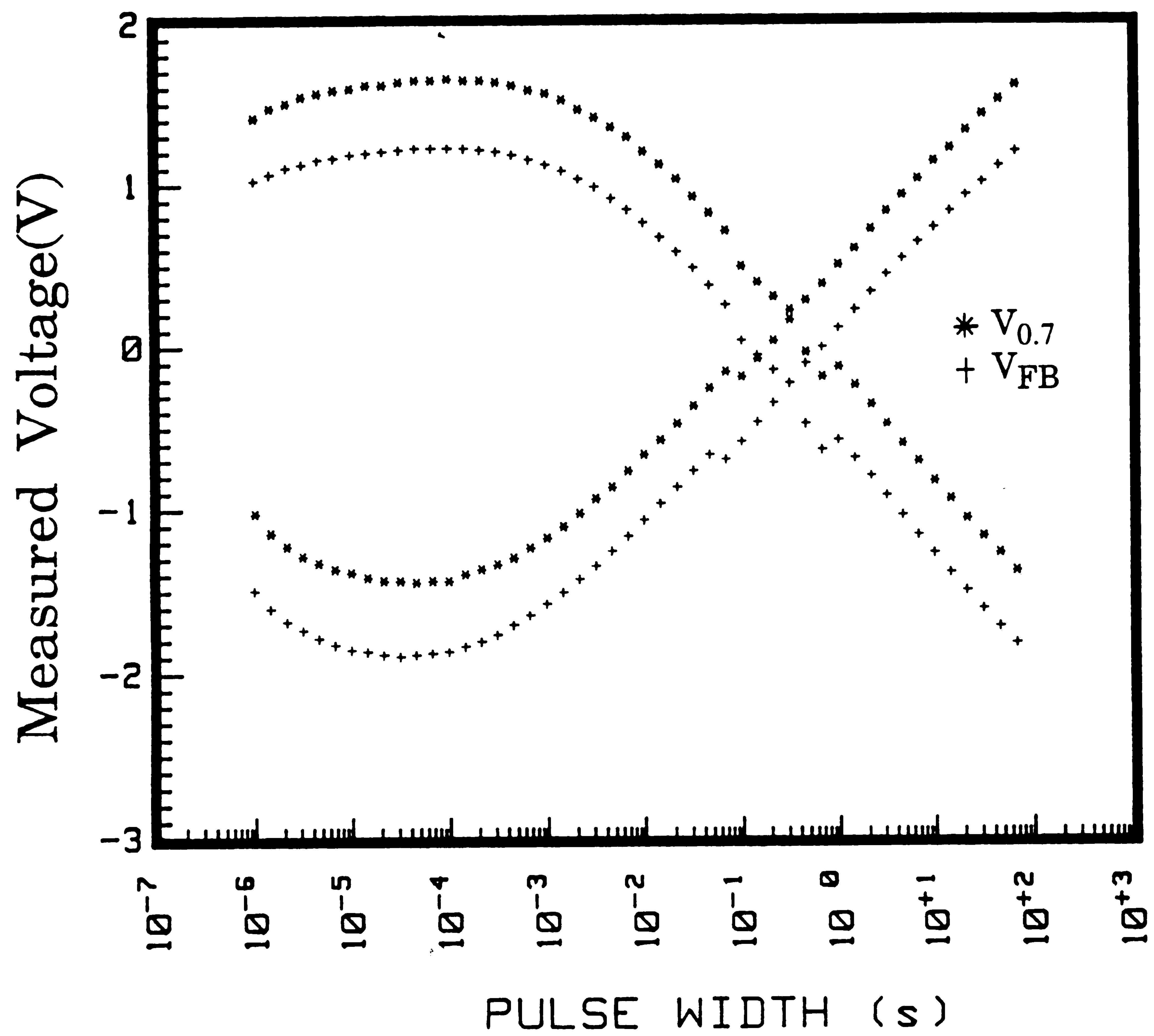


Figure 4-14: Erase/Write measurement of a MONOS capacitor with an implant dose of $15x10^{12}$ cm^2 taken at $C_{ref} = 0.7C_{eff}$ (*) and $C_{ref} = C_{FB}$ (+) for a programming voltage of 5 volts and a pulse width of 10ms

4.4 Results from the n^+/p^+ Polysilicon Gate Devices

To obtain the initial threshold voltage shift on the n^+ and p^+ polysilicon devices, linear voltage ramp measurements are taken with a ramp rate of α = 20 mV/second. To prevent any programming during the measurement, the voltage ramp is kept within ±3 volts. Looking at the results (fig. 4-15), one sees that no programming occurs since there is no change in the threshold voltage between the forward and reverse voltage sweeps of the same device. Yet, between the n^+ and p^+ polysilicon gate devices, a threshold voltage shift of 0.56 volts occurs as expected fro the shift between a heavily doped n^+ and a very lightly doped p^+ polysilicon gate.

The thicknesses of the triple dielectric layer can also be verified from the current measured in accumulation and inversion which is $2.2x10^{-12}$ amps. Using equation (1), the current corresponds to a capacitance of $1.1x10^{-10}$ F or $2.98x10^{-7}$ F/cm^2 given an area of $3.69x10^{-4}cm^2$. The effective triple dielectric thickness is 116Å which agrees closely with the thickness of 102Å measured using the ellipsometer where x_{ot} = 20Å , x_n = 95Å , and x_{ob} = 25Å . Dynamic measurements to observe the speed and retention of these devices were not taken since the p^+ polysilicon devices have a very high sheet resistance.

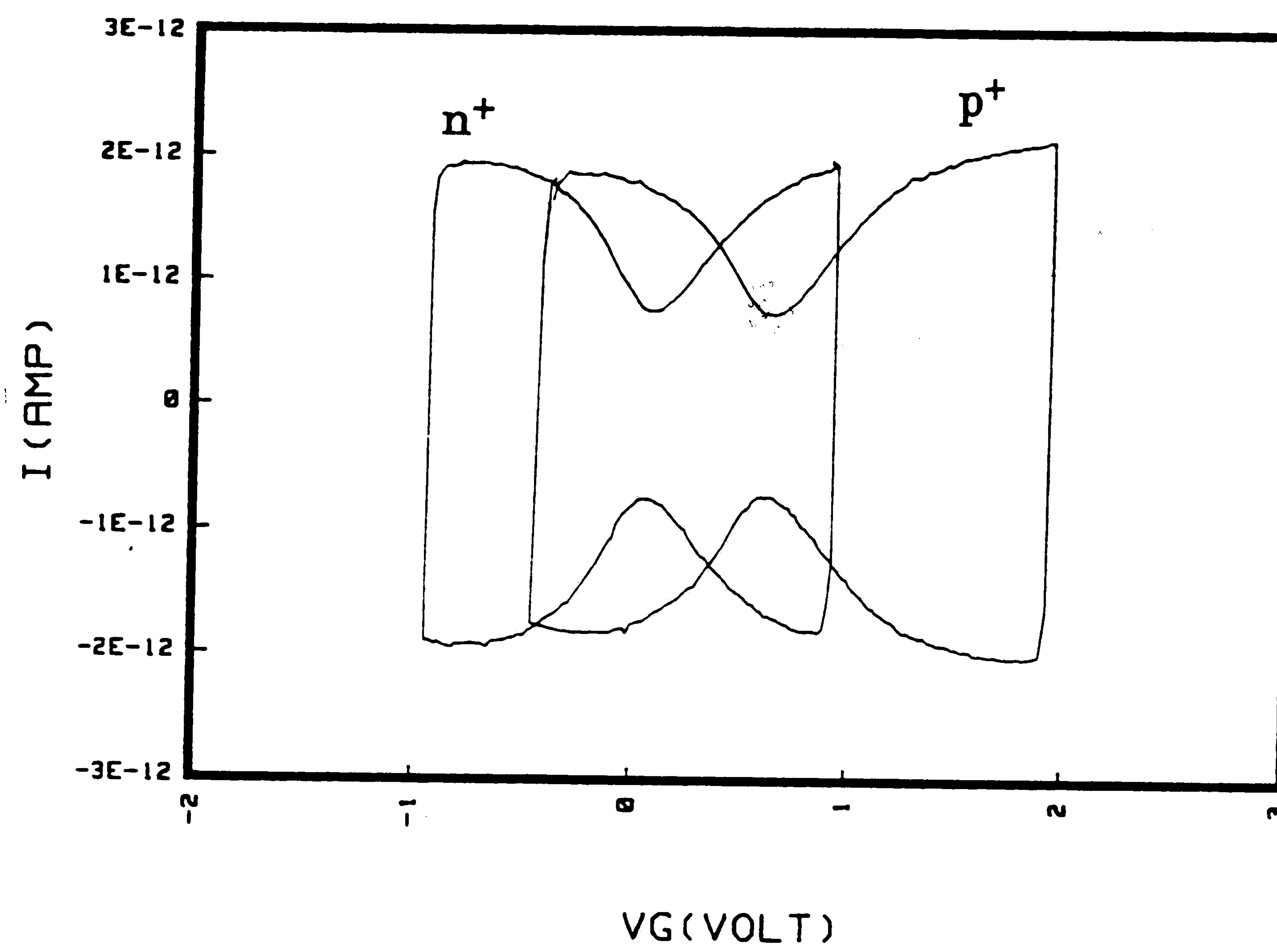


Figure 4-15: Quasi-static C-V Measurement of p^+ and n^+ polysilicon gate devices

Chapter 5
Conclusions

I have shown that the memory window can be shifted by (1) changing the gate material from n^+ to p^+ polysilicon and (2) implanting the bulk. Using the first method the window is shifted by 0.6 volts. The full expected one volt shift in the window is not achieved since the p^+ polysilicon gate was not heavily doped. Also, a complete analysis of the dynamic memory characteristics of the device could not be accomplished since the p^+ polysilicon devices had a high sheet resistance.

Further work needs to be done to achieve heavily doped p^+ polysilicon gate SONOS transistors for evaluation. The fabrication process to obtain these devices needs to be investigated. Particularly, a method to protect the p^+ doped polysilicon gate from the $POCl_3$ doping during the formation of the source and drain must be found.

For the implanted MONOS capacitors, it has been shown that a positive shift of the memory window can be achieved. The retention characteristics of the implanted devices improve significantly when compared to the nonimplanted devices, but the speed of the implanted devices is much slower. Also, the memory window position varies depending on the measurement conditions used. When the device was read from the high frequency C-V plot at a value of $C = 0.7C_{eff}$ a different window was obtained than that when the device was read at $C = C_{FB}$. Thus, the read conditions of the device are very important to the memory window position.

Further studies are also needed of the bulk implants. The devices which I studied were capacitors and the threshold voltage performance of the memory window was analytically determined from the flat band measurements. The

actual performance of the memory window measured as the threshold voltage may be different than the analytical calculations. Thus, SONOS transistors with Boron implants should be studied such that the threshold voltage measurements can be made. Further work on the implant studies should also be done for implant doses less than 3×10^{12}. Also, arsenic implants should be studied to see if one can shift the threshold voltage negative which may be desired when a p^+ polysilicon gate device is used.

Finally, for a p-type MONOS capacitor with no implant adjust and $x_{ot} = 20Å$, $x_n = 94Å$, and $x_{ob} = 34Å$, the device begins with a 3 volt window and retains a 0.3 volt window after 10^8 seconds (figure 5-1). This measurement was taken with a programming voltage of 5 volts and a pulse width of 10ms. Frank Libsch and Anirban Roy obtained a 3.5 volt initial window and a 0.5 volt final window after 10 years for a MONOS capacitor with $x_{ot} = 20Å$, $x_n = 50Å$, and $x_{ob} = 35Å$ using a 5 volt programming voltage and a 10 ms pulse width.[6] Thus, the devices in this study can still be improved with regards to retention and erase/write characteristics by optimizing the choice of the triple dielectric thicknesses.

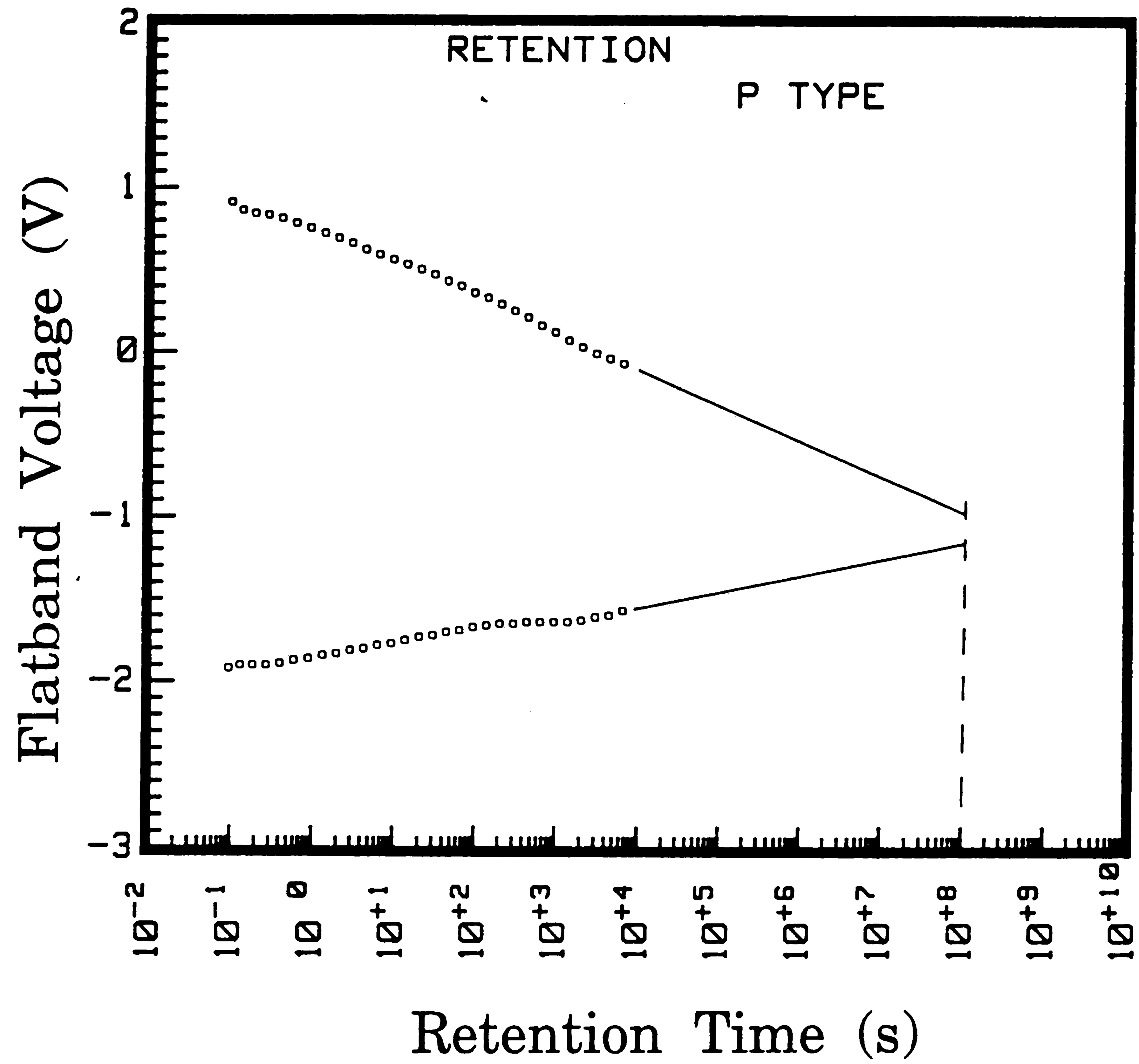


Figure 5-1: Retention measurement of a MONOS capacitor indicating a 3 volt initial window and a 0.3 volt window after 10^8 seconds

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Appendix A
SUPREM Simulations

Before actually fabricating the implant adjust capacitors, the process sequence is simulated on the computer with SUPREM II. This simulation allows me to choose an appropriate energy and dose for the Boron implants and gives an expected doping profile for the devices. The steps given to SUPREM II are shown below:

```
1	TITLE MOS CAPACITOR
2	GRID DYSI=0.01,DPTH=0.01,YMAX=4
3	SUBSTRATE ORNT=100,ELEM=B,CONC=5.8E15
4	PRINT HEAD=YES
5	COMMENT ---------- GROW FIELD OXIDE
6	STEP TYPE=OXID,TEMP=1100,TIME=60,MODL=WET0
7	COMMENT ---------- ETCH FIELD OXIDE
8	STEP TYPE=ETCH
9	COMMENT ---------- GROW PAD OXIDE
10	STEP TYPE=OXID,TEMP=950,TIME=25,MODL=DRY0
11	COMMENT ---------- VTH IMPLANT ADJUST
12	STEP TYPE=IMPL,ELEM=B,AKEV=15,DOSE=15E12
13	COMMENT ---------- ANNEAL IMPLANT
14	STEP TYPE=OXID,TEMP=950,TIME=15,MODL=NIT0
15	COMMENT ---------- ETCH PAD OXIDE
16	STEP TYPE=ETCH
17	COMMENT ---------- DEPOSIT TRIPLE DIELECTRIC
18	STEP TYPE=DEPO,TIME=0.0105,GRTE=1
19	COMMENT ---------- STEAM SIMULATION OF BLOCKING OXIDE
20	STEP PLOT TOTL=YES,WIND=0.5
21	STEP TYPE=OXID,TEMP=900,TIME=120,MODL=NIT0
22	SAVE LUNM=20,TYPE=A
```

Since the simulation package cannot do nitride depositions, an effective oxide of 105Å is deposited for the triple dielectric, line 11. Yet, this low temperature deposition will not provide a correct doping profile since the impurities will redistribute during the high temperaure steam oxidation. Thus, line 13 is added to simulate the steaming process.

The doping profiles given by SUPREM for various implant doses are shown in figure A-1. In each of these doping profiles, the doping level is uniform

at the surface and does not begin to decay until 0.03μ into the wafer which is past the maximum depletion width of the device. Thus, a uniform doping profile can be assumed.

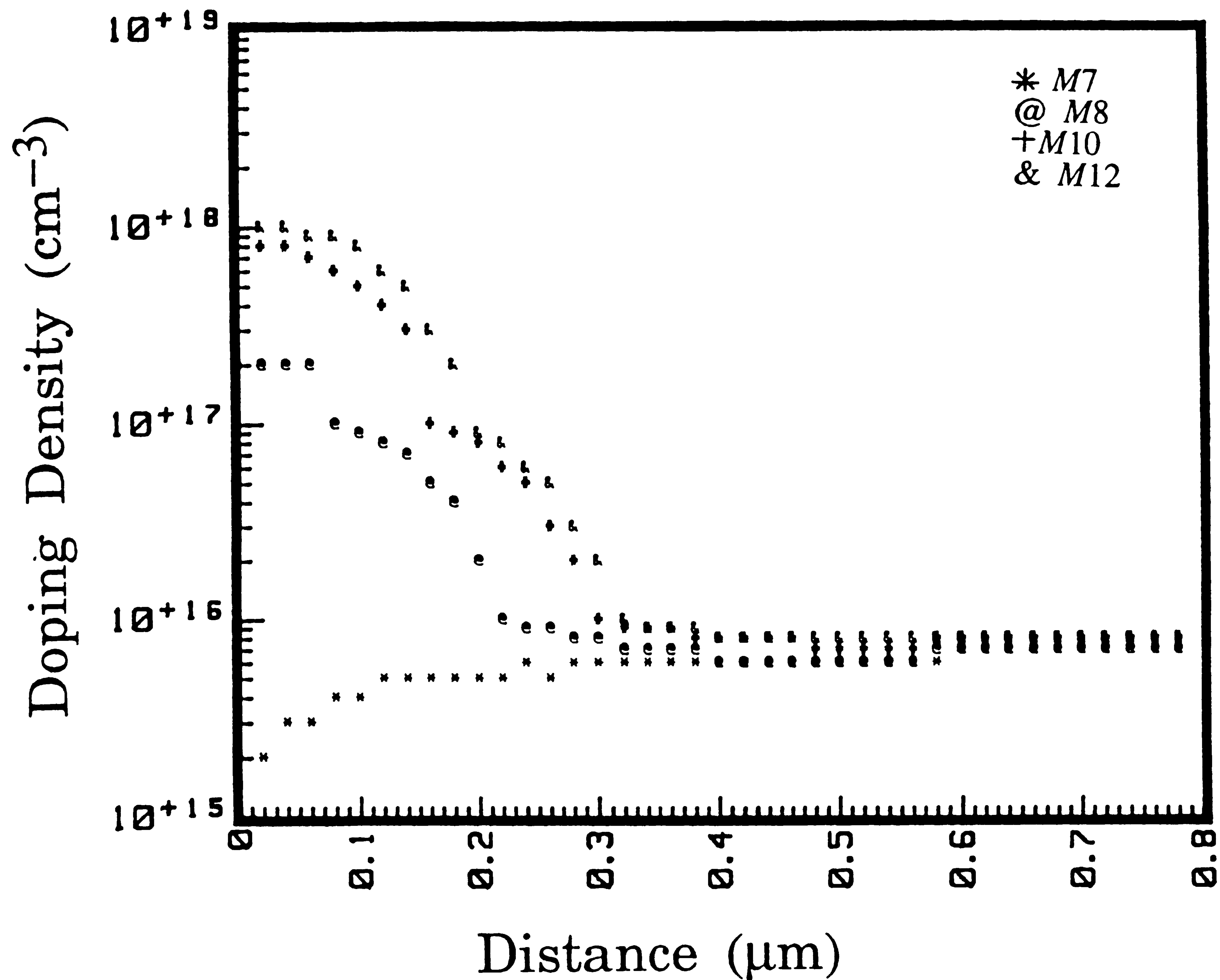

Figure A-1: Doping profiles determined by SUPREM for no implant (M7) and an implant dose of $3x10^{12}$ cm^2 (M8), $9x10^{12}$ cm^2 (M10), and $15x10^{12}$ cm^2 (M12)

Appendix B
Doping profile determined from C-V

The doping profile of the implant adjust capacitors can be extracted from the high frequency C-V plot by using the differential capacitance in the depletion region. A SONOS structure in the depletion region is illustrated in figure B-1.

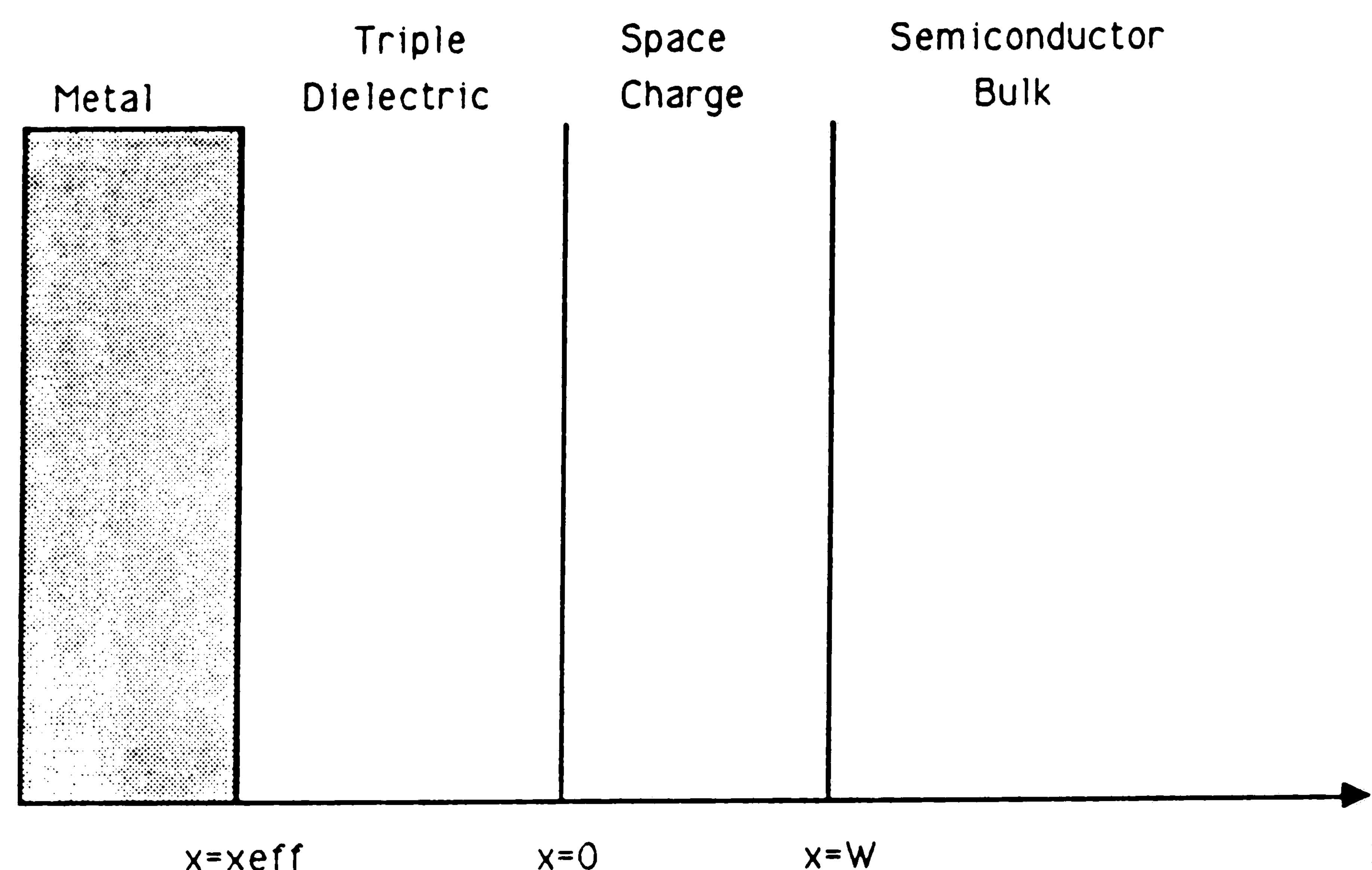

Figure B-1: SONOS structure in the depletion region

Assuming no net charge is stored in the dielectric which is achieved by taking measurements before any programming on the SONOS device occurs, the change in the gate charge dQ_G must equal the change in the space charge dQ_{sc} by Gauss' law. Thus,

$$dQ_G = -dQ_{sc} \tag{1}$$

Using the depletion approximation the space charge change is due entirely to the complete uncovering of additional ionized dopants such that

$$dQ_G = -qN(W)dW \tag{2}$$

where q is the charge of an electron and N(W) is the dopant density (atoms per cm^3) at a distance W from the tunnel oxide-semiconductor interface. By definition

$$dQ_G = C\,dV_{GB} \tag{3}$$

Equating (2) and (3)

$$dV_{GB} = -qN(W)\frac{dW}{C} \tag{4}$$

Where C represents the series combination of the effective triple dielectric capacitance $C_{eff} = \frac{\varepsilon_{ox}}{x_{eff}}$ and the depletion capacitance $C_{sc} = \frac{\varepsilon_{si}}{W}$

$$\frac{1}{C} = \frac{1}{C_{eff}} + \frac{1}{C_{sc}} \tag{5}$$

Now

$$dW = \varepsilon_{si}\,d\left(\frac{1}{C_{sc}}\right) = \varepsilon_{si}\,d\left(\frac{1}{C}\right) \tag{6}$$

Combining equations (4) and (6)

$$dV_{GB} = -qN(W)\varepsilon_{si}\frac{1}{C}d\left(\frac{1}{C}\right)$$

$$dV_{GB} = \frac{\varepsilon_{si}qN(W)}{2}d\left(\frac{1}{C^2}\right) \tag{7}$$

Rewriting the above

$$N(W) = \frac{2}{\varepsilon_{si}q}\left[\frac{d\left(\frac{1}{C^2}\right)}{V_{GB}}\right]^{-1}$$

$$N(W) = \frac{2C_{eff}^2}{\varepsilon_{si}q}\left[\frac{d\left(\frac{C_{eff}}{C}\right)^2}{dV_{GB}}\right] \tag{8}$$

To find the distance W, we go back and use equation (5)

$$\frac{1}{C_{sc}} = \frac{1}{C} - \frac{1}{C_{eff}} = \frac{W}{\varepsilon_{si}}$$

$$W = \frac{\varepsilon_{si}}{C_{eff}}\left(\frac{C_{eff}}{C} - 1\right)$$

$$W = \frac{\varepsilon_{si}x_{eff}}{\varepsilon_{ox}}\left(\frac{C_{eff}}{C} - 1\right) \tag{9}$$

The impurity profile can then be found using equations (8) and (9).

The profile for the nonimplanted wafer is shown in figure B-2 and the

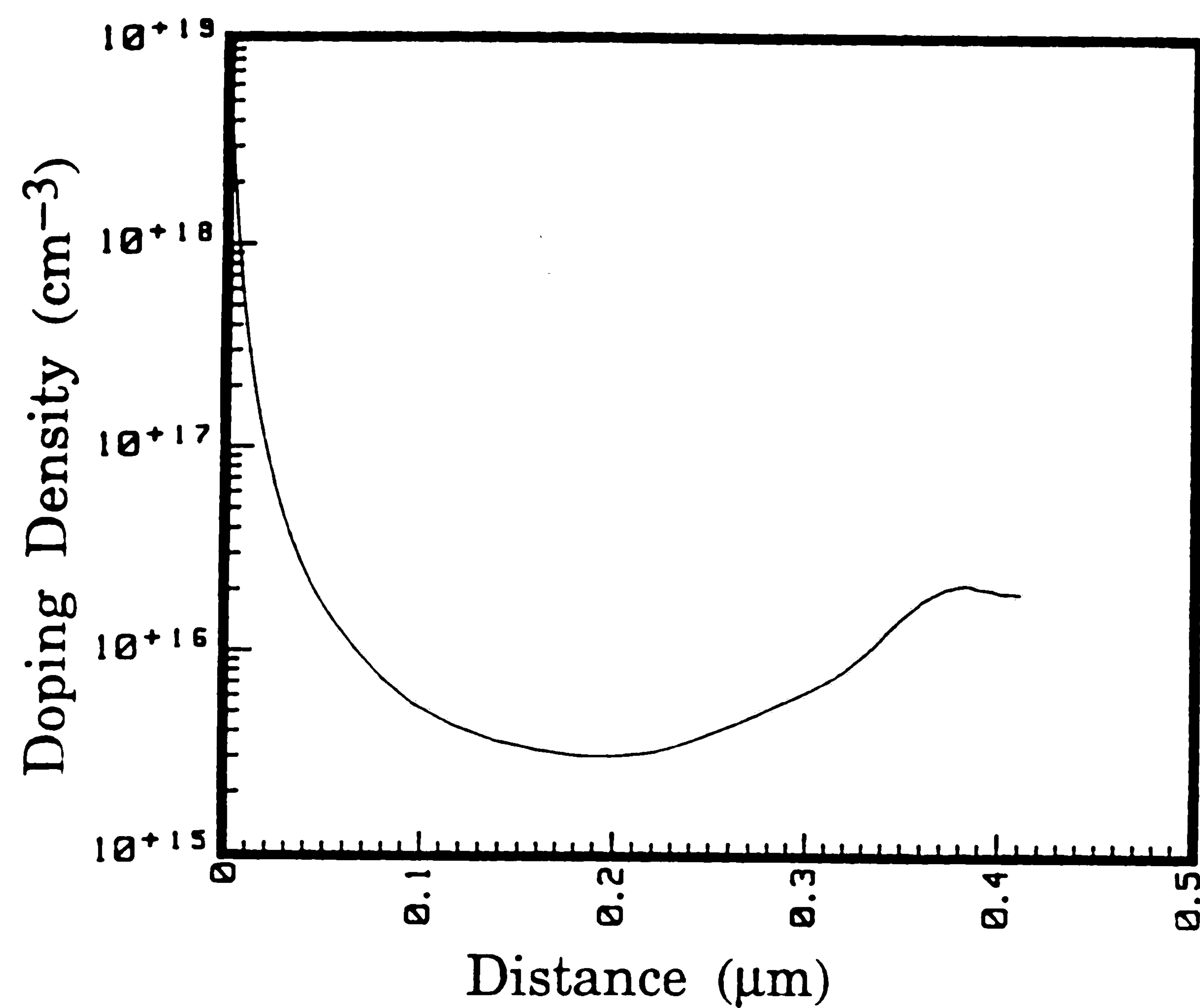

Figure B-2: Doping profile for the nonimplanted wafer found by the differential capacitance method

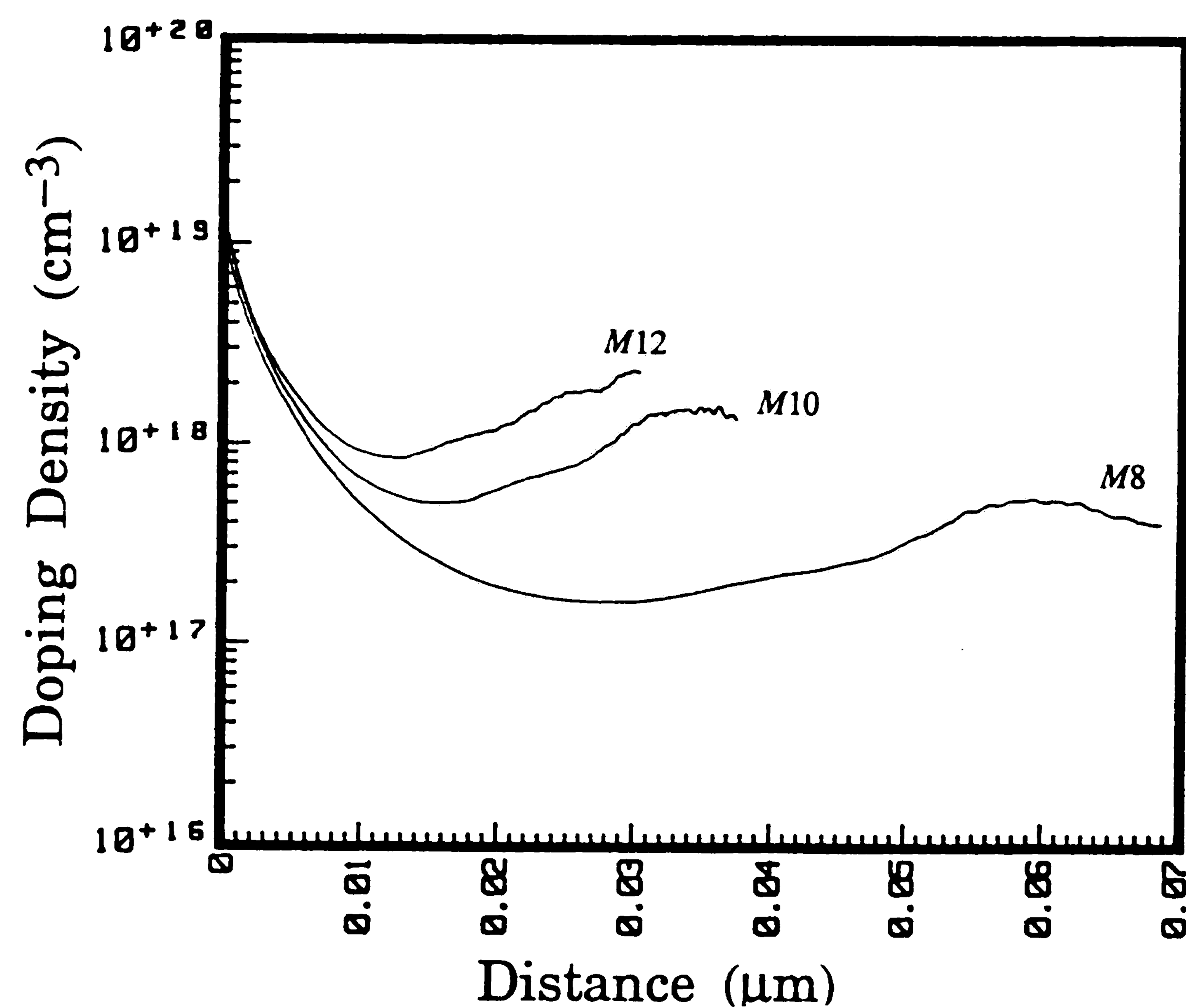

Figure B-3: Doping profiles for the implanted wafers found by the differential capacitance method where the implanted doses are $3x10^{12}$ cm^2 (M8), $9x10^{12}$ cm^2 (M10), and $15x10^{12}$ cm^2 (M12)

profiles for the implanted wafers are shown in figure B-3. Remember that these dopant profiles are only valid for the differential capacitance in the depletion region. Thus, the subsequent increase in doping away from the surface is invalid since these points are found from data when the capacitor is in inversion, and most of the steep doping profile at the surface is invalid since the capacitor is in accumulation for this data and the space charge region is not due entirely to ionized dopants. The depletion approximation is only valid for the depletion region defined by $W \geq 2\lambda_D$ where W is the distance from the semiconductor surface and λ_D is the extrinsic Debye length given by

$$\lambda_D = \sqrt{\frac{2kT\varepsilon_{si}}{q^2 N(W)}}$$

where k is Boltzmann's constant and T is the absolute temperature.

Ziegler et al[17] have developed a method to determine the doping profile right up to the surface. The corrected doping profile is

$$N(W) = \frac{2C_{eff}^2}{\varepsilon_{si} q}\left[\frac{d\left(\frac{C_{eff}}{C}\right)^2}{dV_{GB}}\right] g_2\left(\frac{W}{\lambda_D}\right) \tag{10}$$

$$W = \frac{\varepsilon_{si} x_{eff}}{\varepsilon_{ox}}\left(\frac{C_{eff}}{C} - 1\right)\left(1 - g\left(\frac{W}{\lambda_D}\right)\right) \tag{11}$$

where

$$g_2\left(\frac{W}{\lambda_D}\right) = 1 - \frac{2\left(\frac{W}{\lambda_D}\right)^2 g\left(\frac{W}{\lambda_D}\right)}{\left(1 - g\left(\frac{W}{\lambda_D}\right)\right)^2\left(1 - g\left(\frac{W}{\lambda_D}\right)\right)} \tag{12}$$

$$\left(\frac{W}{\lambda_D}\right)^2 = g\left(\frac{W}{\lambda_D}\right) - \ln\left(g\left(\frac{W}{\lambda_D}\right)\right) - 1 \tag{13}$$

The procedure for calculating both the corrected doping profile is then:

- Find $g_1\left(\frac{W}{\lambda_D}\right)$ from C-V data

$$g_1(\frac{W}{\lambda_D}) = \frac{kT}{q}\frac{1}{\left(\frac{1}{C}-1\right)^2}\frac{d}{dV_{GB}}\left(\frac{C_{eff}}{C}\right)^2 \tag{14}$$

$$g_1(\frac{W}{\lambda_D}) = \frac{1-g(\frac{W}{\lambda_D})}{(\frac{W}{\lambda_D})^2} - \frac{2g(\frac{W}{\lambda_D})}{1-g(\frac{W}{\lambda_D})} \tag{15}$$

- Calculate $(\frac{W}{\lambda_D})$ and g by solving equation (15) and (13)
- Compute g_2 where

$$g_2(\frac{W}{\lambda_D}) = \frac{g_1}{2g + g_1}$$

- Finally N(W) and W are determined from equations (10) and (11)

The corrected doping profile for the nonimplanted wafer is shown in figure B-4 and the corrected doping profiles for the implanted wafers are shown in figure B-5. To find both the uncorrected and corrected doping profiles a short subroutine is added to the high frequency CV program as follows:

```
1400 !      Subroutine: Impur
1401 !      Purpose:    Extracts the corrected and uncorrected
1402 !                  doping profile from the differential
1403 !                  capacitance
1404 !      Inputs:     Generator(2,1)  number of data points
1405 !                                  in C-V data
1406 !                  Datarray(I,4)   measured substrate
1407 !                                  voltage
1408 !                  Datarray(I,5)   measured HF capacitance
1409 !      Outputs:    Datarray(I,7)   doping profile
1410 !                  Datarray(I,8)   distance
1411 !                  Datarray(I,9)   corrected doping
1412 !                                  profile
1413 !                  Datarray(I,10)  corrected distance
1414 ! Uses Routines:   Datasmooth    finds first derivative
1415 !                  Genval2       finds minimum and maximum
1416 !
1417 !
1515 Impur:  BEEP 5000,.01 !PROFILE EXTRACTION SUBROUTINE
1516         Npts=Generator(2,1)
1517         Ks=11.7
1518         Eo=8.85E-14
1519         Q=1.6E-19
```

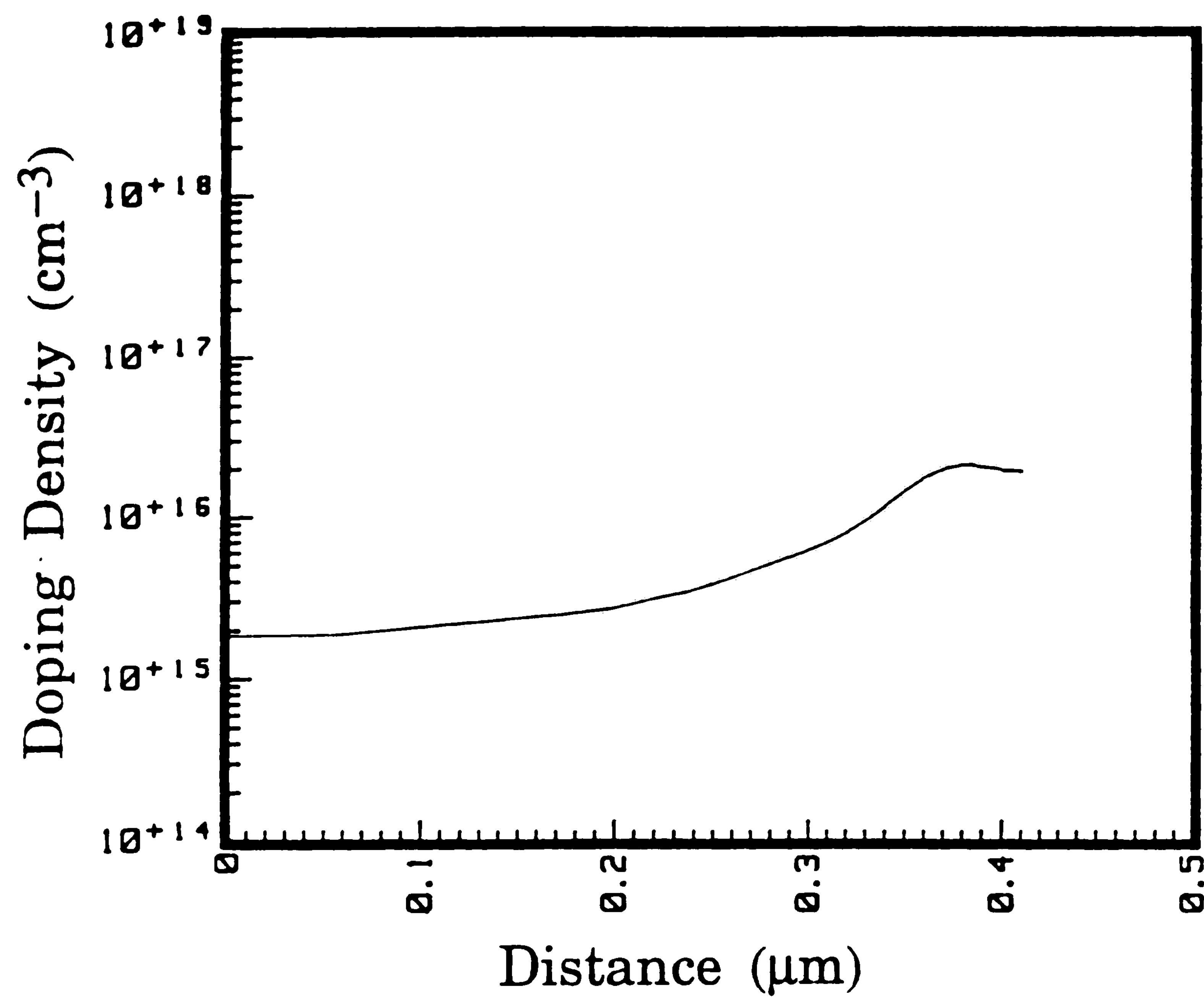

Figure B-4: Doping profile for the nonimplanted wafer found by the differential capacitance method with Ziegler's correction

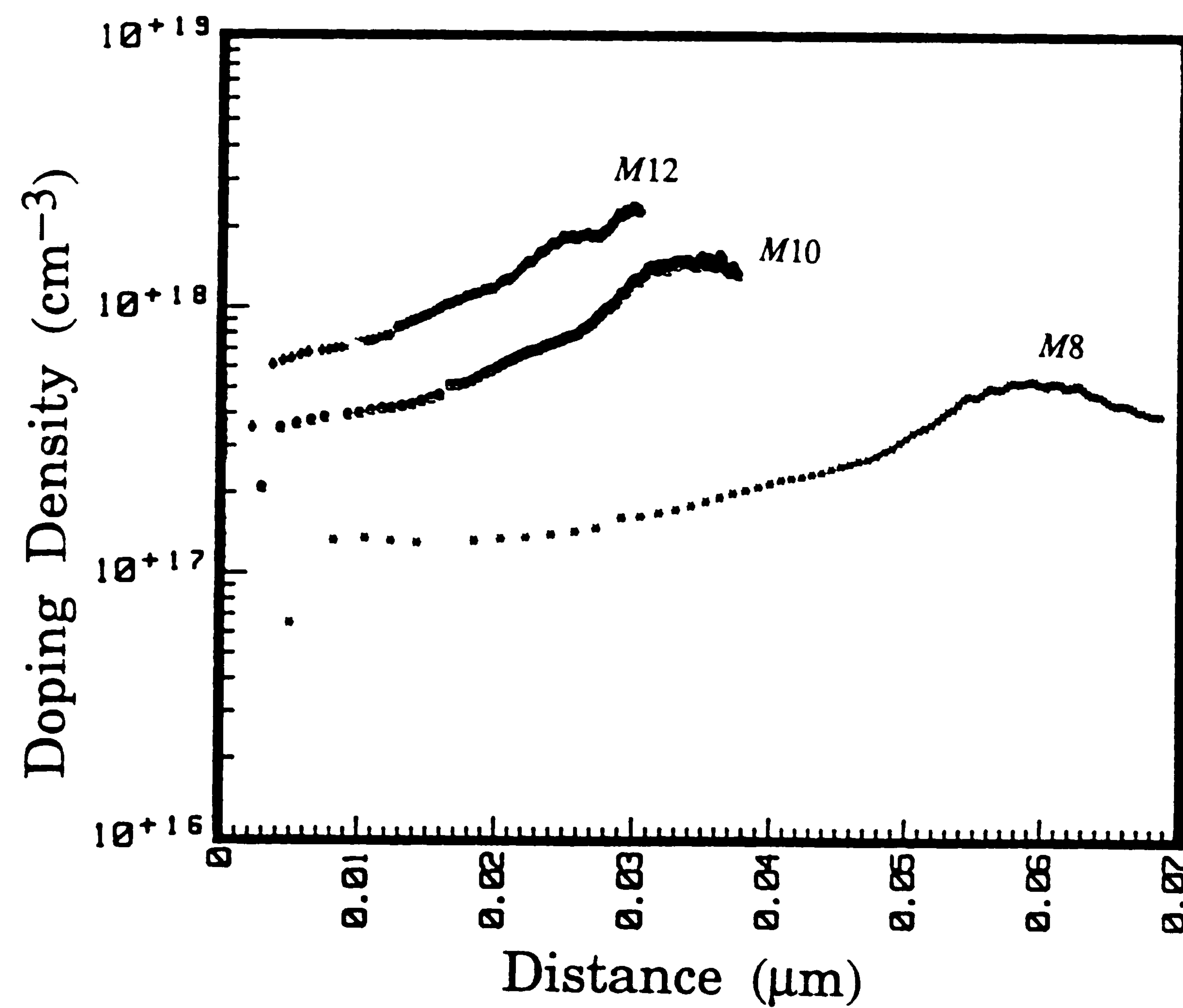

Figure B-5: Doping profiles for the implanted wafers found by the differential capacitance method with Ziegler's correction where the implanted doses are $3x10^{12}$ cm^2 (M8), $9x10^{12}$ cm^2 (M10), and $15x10^{12}$ cm^2 (M12)

```
1520          Vt=0.026
1521          INPUT "WHAT IS THE EFFECTIVE CAPACITANCE ",Co
1522          FOR I=1 TO NPTS
1523             Datarray(I,4)=1/Datarray(Npts-I+1,3)
1524             Datarray(I,5)=1/Datarray(I,4)^2
1525          NEXT I
1526          CALLGenval2(4,Npts)
1527          CALL Genval2(5,Npts)
1528          CALL Datasmooth("DERIV1",5,1,6)
1529          INPUT "MAXIMUM I",Max
1530          Sum=0
1531          FOR I=2 TO Max
1532             Datarray(I-1,7)=2*Co^2/(Ks*Eo*Q*Datarray(I,6))
1533             Datarray(I-1,8)=Ks*Eo*(Datarray(I,4)-1)/
                                   (Co*1.E-4)
1534             Ld2=2*SQR(2*Vt*Ks*Eo/(Q*Datarray(I-1,7)))*1.E4
1535             IF Datarray(I-1,8)>=Ld2 THEN GOTO Nocorr
1536             G1=Vt*Datarray(I,6)/((Datarray(i,4)-1)^2)
1537             Dg=0.001
1538             G=0.001
1539             IF G1>.7 THEN
1540                Sum=Sum+1
1541                GOTO Done
1542             END IF
1543             FOR J=1 TO 1000
1544                F=(1-G)/(G-LOG(G)-1+.001)-2*G/(1-G)-G1
1545                Fp=(-1+1/G+LOG(G))/((G-LOG(G)-1+.001)^2)
                       -2*(1+G)/((1-G)^2)
1546                Newg=G-F/Fp
1547                IF ABS(G-Newg)<1.E-3 THEN GOTO Enfind
1548                G=G+Dg
1549 Enloop:     NEXT J
1550 Enfind:     G=Newg
1551             G2=ABS(G1/(2*G+(1-G)*G1))
1552 Eng2:       !
1553             IF G2<=0.33 THEN GOTO G33
1554 Corr1:      Datarray(I-Sum-1,9)=Datarray(I-1,7)*G2
1555             Datarray(I-Sum-1,10)=Datarray(I-1,8)*(1-G)
1556             GOTO Done
1557 G33:        Datarray(I-Sum-1,9)=Datarray(I-1,7)*0.33
1558             Datarray(I-Sum-1,10)=Datarray(I-1,8)*(1-G)
1559             GOTO Done
1560 Nocorr:     Datarray(I-Sum-1,9)=Datarray(I-1,7)
1561             Datarray(I-Sum-1,10)=Datarray(I-1,8)
1562 Done:    NEXT I
1563          Max=Max-1
1564          CALL Genval2(7,Max)
1565          CALL Genval2(8,Max)
1566          Max=Max-Sum
```

```
1567        CALL Genval2(9,Max)
1568        CALL Genvel2(10,Max)
1569        PRINT "FINISHED !!!!!!!!!"
1570        RETURN
```

Vita

Margaret Larson French was born a long time ago, in a Naval Hospital far, far away. She attended Tesago Elementary School, which is even farther away than the aforementioned Naval Hospital. After a brief sentence in Middle School, she graduated from West Springfield High School, which is near said Naval Hospital, and went on to get her BS degree in Electrical Engineering from a small, but prestigious engineering school just south of the Fahy Bridge. It was at this university that she met and married a handsome Metallurgist before beginning her Masters work.

Her favorite book is either Calvin and Hobbes by B. Watterson, or The Cat Who Could Read Backwards by L. J. Braun; neither of which has any significant bearing on her graduate studies, save that one is a mystery and the other has a tenuous grip on reality at best. Her current plans are to become rich and famous while persuing her PhD at Lehigh, so that her return address will read Mr. & Dr. French.