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Surface mount device technology :

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SURFACE MOUNT DEVICE TECHNOLOGY

(An approach using an Expert System (PEX))

by

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ABSTRACT

Nowadays, the conventional dual-in-line package is no more the standard package. It has become uneconomical and unattractive due to todays densely packed applications. Surface mount components provides the necessary solutions for the growing needs of VLSI applications. They are small in size, weigh less, high yield and can be placed on both the sides of the board.

Three types of surface mount packages are available, which are, Small Outline Integrated Circuit (SOIC), Plastic Leaded Chip Carrier (PLCC), Leadless Ceramic Chip Carrier (LCCC). Various packages in each of these categories are available depending upon user requirements such as I/O pin count, thermal or electrical characteristics.

Therefore, an expert system (PEX) together with the component selection chart has been developed to aid the user in the selection of a package specific to his needs. This system is also capable of providing footprint information, solder paste selection technique, thermal resistance of various surface mount package as a function of die size and also the advantages and disadvantages of these packages.

CHAPTER 1

INTRODUCTION

The VLSI circuits require ever increasing input-output (I/O) count and constant improvements in thermal and electrical performance from the circuit package. Currently, the convential dual-in-line (DIP) package becomes unattractive over 40 pins for various reasons such as weight, size, breakage of leads, poor electrical properties and greater heat dissipation problems. Above all the cost of the DIP package increases drastically with size and weight due to greater amounts of material and gold used. The surface mount components provide the necessary advantages over convential DIP packages.

Various electronic components supplier are moving towards surface mount components so as to provide the solution for the ever growing field of VLSI and electronic packaging. To date no "cure all" package has been developed and the future trends tend to indicate development of technologies as chip on board to lead the second generation of SMC.

Today, there are basically three types of package configurations available in Integrated Circuits packaging. These are the Small Outline Integrated Circuit (SOIC), the Plastic Chip Carrier (PLCC), and the Leadless Ceramic Chip Carrier (LCCC). The advantages and disadvantages of these

packages have been explained in this paper.

A chart has been developed as a quick reference in the selection of surface mount components. This section describes various categories such s ease of manufacturing the SMC's, their shipping and handling and application categories such as military, memory and VLSI applications. Comparisons have been drawn between these categories.

A description of the knowledge based rules developed in the selection and designing of a surface mount electronic packages for specific applications follows. These rules have been incorporated into the expert system (PEX) being developed for Semiconductor Research Corporation for the selection of the packages for VLSI applications.

Selection and application criterions for solder paste is highlighted in this section. Seven important factors influencing the selection of paste is discussed in length.

Finally, the paper discusses the future trends in the packaging industry and concludes with the future course of action and a brief summary.

CHAPTER II

THE OBJECTIVES

After extensive literature review on surface mount technology the author set the following goals to achieve as his work towards the masters thesis.

2.1 Surface Mount Packages :

2.1.1 Various packages available in surface mounts are:

- Small Outline Integrated Circuit (SOIC)
- Plastic Leaded Chip Carrier (PLCC)
- Leadless Ceramic Chip Carrier (LCCC)

A brief description of each package configuration and elaborating the advantages and disadvantages of each one of them. Addressing certain key issues such as density, weight, electrical and thermal properties, reliability and the cost of each package.

2.1.2 Development of an expert system for designing and selection of surface mount packages for integrated circuit chips, by representing knowledge as supplied by the members of Semiconductor Research Corporation in the form of rules.

2.1.3 Various factors affecting the selection of packages will be described and how an application chart (Fig 1.) should help a user to select a package for his specific application. This chart clearly lists the attributes of

each of the package configurations.

2.2 Solder Paste :

2.2.1 Development of an expert system for determining the footprint requirements on the substrate for the placement of surface mount components. Also, to determine the volume of paste to be deposited onto the solder lands depending on various factors such as emulsion coating thickness, aperture size, mesh density and solder paste density.

2.2.2 Ingredients of the solder paste.

2.2.3 Particle/grain size range for various application specific solder paste.

2.2.4 Controlling of various process parameters such as :

i) Viscosity

ii) Tack time

iii) Wetting

iv) Solder balling

v) Memory property of solder paste

2.2.5 Application process selection :

i) Syringe or dispensing

ii) Printing using a metal mask (stenciling)

iii) Printing using a screen (screening)

2.3 Soldering Techniques, Solderability and Solder Joint criteria in surface mount technology.

Development of an expert system in the selection of a soldering technique such as wave or reflow soldering depending upon the configuration of the substrate assembly and describing features of each type of soldering techniques. Addressing the solderability issues such as flux, wetting and quality of solder joints.

2.4 Selection of component placement and distribution system depending upon the need of the user. Also, machines for chip replacement /reworking, and inspection, test and repair of chips and substrate assemblies.

2.5 Overall evaluation of surface mount technology and future trends.

CHAPTER III

SURFACE MOUNT PACKAGES

3.1 The Small Outline Integrated Circuit Packages :

The small outline integrated circuit (SOIC) has a longer history of use than other surface mounting packages . The SOIC is a plastic package and is similar to the dip package in shape but smaller in size. The leads are flattened with a lead spacing of 50 mils instead of 100 mils in a dip package. These leads are formed outwards in an inverted "gull wing" fashion so that the tips of the leads lie in contact with the PCB, as shown in Fig 2., instead of going down through a hole. The SOIC package is currently available in 6, 8, 10, 14 and 16 pin counts with a body width of 150 mils and in 16, 20, 24 and 28 pin counts with a wider body width of 300 mils.

3.1.1 Advantages:

Having a dual-in-line configuration the SOIC package is often easier to design into a high density layout and the flat lead configuration allows for good wetting of the leads and therefore stronger solder joints. Low weight and size of the SOIC package also allows the surface tension of molten solder to self align a device during soldering process. It has been observed that to increase the strength of the solder joint on the SOIC package a hole be placed on

the lead of the device. During soldering process the solder moves onto and around the hole thus providing a stronger joint and the hole also acts as a vent for gases thus relieving the solder joint from any void formation.

SOIC package has a relatively better heat dissipation property with thermal resistance being low. Figures 3 and 4 give the thermal resistance, Theta JA and Theta JC respectively for various SOIC packages available in the market.

The low thermal resistance for SOIC packages can be attributed to the fact that now copper lead frames are being used in place of alloy 42.

The biggest concern in the surface mount technology is the mismatch of the package's thermal coefficient of expansion with the substrate material. In the case of SOIC package , this mismatch is overcome to a large extent due to the length, shape and material of the leads of the package. The leads are flexible and can adjust to relieve any kind of thermal stresses induced in the solder joint due to the expansion of the substrate.

For this reason, the SOIC packages are preferred over LCCC as no mismatch in thermal coefficient of expansion is experienced.

3.1.2 Disadvantages :

The SOIC package has various drawbacks. This package

becomes disadvantages if used for high lead count application as the lead frame length for pins at the outer end becomes longer resulting in timing problem and low electrical performance. Secondly the size and weight of the package also increases and it would utilize a lot more space on the PC board and thus defeat the purpose of surface mount components. The "gull wing" configuration in fact occupies larger area on the board. The gull wing lead are easily damaged during shipping, handling or during assembly. Other problems with this design is the coplanarity and lead skew. Therefore, this package demands high compliance to customer's specs in order to obtain high process yield.

The smaller size of the package greatly reduces the barrier between the external world and the chip. Therefore, this package is highly susceptible to moisture penetration and subsequent corrosion and metal migration caused failures. Other greater disadvantages is the mismatch of thermal coefficient of expansion between the chip and the copper lead frame.

Summarizing the above results, we find :

Advantages :

1. Easier to design into a high density layout
2. Light weight and smaller size
3. Stronger solder joints

4. Good heat dissipation

5. Easier inspection/repair and rework

6. Preferred for low lead count applications

Disadvantages :

1. Susceptible to moisture penetration and corrosion

2. Poor properties for high lead count application

3. Leads easily damaged

3.2 Plastic Leaded Chip Carrier (PLCC)

The plastic leaded chip carrier (PLCC) was introduced in 1976 as a premolded plastic package but it was the post-molded PLCC which became famous. PLCC's are manufactured by fully automated high volume processes. They are square in shape and have "J" leads i.e the leads are folded under-neath the package as shown in Fig 5. in the shape of a "J". The leads are along all the four sides of the package and are spaced 50 mils from their centers. PLCC package is basically used in microprocessor and VLSI circuits with high pin count requirements.

3.2.1 Advantages :

PLCC package provides extensive advantages over conven-tional dip package. PLCC are almost mandatory replacements for plastic dip's, which are not practical above 40 pins because of excessive real estate requirements.

Other great advantage of a PLCC package is the compliant nature of the "J" leads. These leads are made up of the copper frame and are flexible thus take up the stresses produced at the solder joint and prevent solder joint cracking. The compliant "J" leads should not touch the plastic package which may happen due to poor design of leads, shipping and handling or planarization. This could lead to restricted movement of the leads thus rendering them non-compliant.

Copper lead frames and shorter distance from the die to PC board interface the package readily conducts heat away from the source. The thermal resistance of PLCC is low (72 deg C/W) as compared to SOIC (97 deg C/W) and comparable to DIP (68 deg C/W) which has alloy 42 lead frame.

Shipping of the PLCC is done in vacuum formed plastic "tub" type container as the standard slide tubes are not acceptable because the components can compress against each other (ref 1). Lastly, the PLCC occupies less real estate and weighs less and is less expensive than the DIP or LCCC.

3.2.2 Disadvantages :

The PLCC suffer from various disadvantages. The "J" leads configuration results in the formation of solder joints underneath the package. Therefore, the testing and inspection of these joint becomes a problem. Thus stringent

measures have to be taken at the time of solder joint formation so as to ensure absolute good quality of bond. This can be achieved by ensuring that the supply of leads meet all the required customer specs such as coplanarity (0.004 inch maximum) and avoiding lead skew.

Heat dissipation is a concern in PLCC packages, which is mainly due to the smaller body size and smaller lead frame size, therefore lesser surface area available to dissipate heat. Nowadays, to help increase the PLCC's heat dissipation capabilities a butterfly heat spreader is being used. This heat spreader is a copper mass attached at the back of the chip and protrudes out at the top of the PLCC and flushes with it. A 20 pin PLCC has average thermal resistance of 72 deg C/W (fig 6, 7) and the normal configuration at normal condition can dissipate upto one watt of energy, but with the addition of these spreaders the thermal resistance drops to 25 deg C/W and heat load increases to three watts. Other methods such as using extra number of pins e.g 44 pins for 28 I/O chip allows the heat load on the package to decreases due to the availability of extra leads (conductive area) i.e four extra leads at each corner of the package. Another method to increase heat dissipation would be through the usage of conductive epoxies instead of solder paste at the lead joints. The epoxy would help conduct heat from the PLCC to the PC board.

The problems at lead frame/plastic package interface are a major concern for any plastic package. The basic function of this interface is to ensure proper lead alignment at all times and to form an effective barrier against external environment. This interface must provide barrier against moisture penetration which can lead to corrosion and metal migration caused failures due to the presence of corroding chloride ions. During the transfer molding process, certain additives should be added to the epoxy resin so that plastic sticks to the lead frame and not to the mold cavity. When epoxies cure to solids , they shrink in volume by about 0.3 to 0.5%. Shrinkage is the mechanism that seals a plastic IC package. The resin exerts compressive forces around the chip, wires and lead frame and leads resulting in the opening of gaps as shown in Fig 8 (ref 5).

The plastic-lead frame interface is a mechanical joint whose sealing integrity can be improved by mechanical or chemical means. Mechanically the major problem is due to the mismatch of the thermal coefficient of expansion between the plastic package and the copper lead frame. During thermal-shock testing, the mismatch could lead to the bending of the package which could reach sufficient proportions to impair the operation of the device. Such bending stress can be minimized by offsetting the chip platform onto the neutral bending axis of the package (ref 5).

During reflow soldering process (219 deg C) the epoxy

resin Novolac has a very high coefficient of expansion (alpha) i.e for 150 deg C and below :- 250 X 10 ^-7 unit/unit/C, and for 50 deg C and above :- 800 X 10 ^ -7 unit/unit/C as compared to copper lead frame (alpha :- 160 X 10 ^ -7) (Fig 9). Therefore, as temperature reaches the soldering temperature the stress on the interface increases rapidly leading to loss of sealing integrity. There are techniques such as gold plating and anchoring which helps in establishing an integral interface. Gold is plated over the lead frame area which will be surrounded by plastic. Gold is soft, thus it forms a better bond between the plastic and itself. It also matches the thermal mismatch and relieves stresses when the leads are bent in "J" configuration. Only drawback is the cost and the cumbersome gold application process. Other techniques used is anchoring in which holes are incorporated into the lead frame resulting in the formation of stronger and firmer bonds at the interface. Also, the use of dimpled chip platform for locking plastic to lead frame with the elimination of stress concentration points at the edges is becoming popular in Fig 10 (ref 5).

Another problem with PLCC is due to the bending of leads. Rolling along one axis tends to align atomic or crystallographic grains in each plane in the same direction. This means that bends made with an axis of bend perpendicular to the direction of rolling are easier to make than bends with

an axis made parallel to the direction of rolling. This is called "anisotrophy". Since PLCC have four rows of leads on each side of the package, therefore two rows of leads will be easier to form than the other two.

Cleaning is another typical problem with all surface mount packages. In PLCC the typical stand off height is 5-10 mils which is way below 20 mils required for cleaning process. The flux residue underneath the package can behave as contaminant and work its way up through the gaps within the interface.

3.3 Leadless Ceramic Chip Carrier (LCCC)

Leadless ceramic chip carrier, or LCCC are usually constructed from a 90 to 96% alumina or beryllia base. As the name indicates, leadless chip carriers have no leads, instead they have gold-plated groove shaped terminations known as castellations. The LCCC are generally square in shape with their terminations brought out on all four sides. The LCCC were developed to satisfy the needs of military requirements.

3.3.1 Advantages :

The LCCC provides several advantages over other packages, therefore it has emerged as the obvious choice in the field of military applications. This package has enormous bene-

fits over DIP package due to its configuration. The DIP packages are large and have a lead spacing of 100 mils.

In a 40 pin DIP package the leads are laid out so far apart that the longest to shortest lead has a 6:1 ratio (ref 2). Long leads mean a lower circuit speed due to parasitic resistance, capacitance and inductance. Whereas in LCCC the package being square and the ratio of longest to shortest lead being 1.5:1, it provides higher circuit speeds due to lower parasitic resistance (ref 3).

The LCCC provides high density and high reliability but this leads to the problem of heat dissipation. Heat dissipation is a generic problem encountered by every surface mount package but LCCC has an edge over the other packages. This is because the thermal resistance of ceramic is much lower than plastic thus allowing rapid dissipation of heat from the chip (source) to the PC board (sink).

The LCCC configuration without leads is best suited for automated assembly. The LCCC are shipped in a plastic preformed tub and is covered by a tape reel. Since it is leadless there is no problem of lead damage during packing into reels and also in picking up and placing of these devices on the PC board using vacuum actuated robot arm. All these aspects make the LCCC ideal for handling and auto-placement.

The material properties of ceramic makes it 'the' choice for military. The military requirements are very stringent and need to operate under extreme temperature conditions and severe environment. Ceramics can withstand these extreme temperature and moisture conditions.

3.3.2Disadvantages :

The LCCC suffers from certain disadvantages. The major being the mismatch of thermal coefficient of expansion between the package and the PC board. Table 1 gives the thermal coefficient of expansion of materials commonly used in electronic packaging (ref 5).

Some of the surface mount packages have compliant leads that allow the package to absorb thermal shocks and stresses developed due to thermal mismatch. Since LCCC are leadless, therefore the common mode of failure is cracked solder joints during thermal cycling test. There are two types of thermal cycles : the process cycle, which are often high in temperature but few in number; and operations cycles, which are numerous but less extreme. Thus in process cycles at 100-200 cycles and temperature variation of -55 to 125 deg C minicracks appear at the solder joint. Thermal expansion of glass-epoxy PC board is very high as compared to the ceramic package, therefore one way of overcoming this problem is by using materials having closer

thermal coefficient of expansion.

Some of the materials being used are copper-invar-copper clad board and polymide kevlar. The only drawback is that these materials are expensive, heavier and tougher to work with than epoxy-glass PC boards.

Three basic methods for solving the coefficient of expansion problem have gained general acceptance in the industry today. The first method uses a clad metal core having a high Young's modulus value so as to dominate the TCE of the entire board. A copper-invar-copper core is often used for this purpose. This is because 16% copper - 68% invar - 16% copper will give a TCE of 6.4 ppm/C which matches with LCCC's TCE. These PC boards are strong, can withstand flexing, warpage and twisting. Since copper is a good thermal conductor it helps in dissipating heat also.

Second method is the use of fiber reinforcement material such as Kevlar with a negative coefficient of thermal expansion to lower the overall TCE of the PC board. Major disadvantages being that Kevlar fibers do not supply the same heat conductivity that the metal core substrate can, but they are inexpensive and easy to manufacture.

Third method uses a material with a low Young's modulus on the surface in order to reduce the stress transmitted to the solder joint. A composite PC board with a TCE of 9

ppm/C but that has a high Young's modulus may actually transmit more stress (Stress is proportional to Young's modulus) to the solder joint than a substrate with a TCE of 12 ppm/C that has a surface made of low Young's modulus material (ref 9).

Another problem is the power cycling i.e. the power is turned off and on which leads to faster heating up of the device (LCCC) than the PC board initially. Temperature difference of 50 deg C have been observed. This means that LCCC expands faster than PC board eventhough their TCE's are matched. Similarly when power is turned off, the LCCC cools hence shrinks faster than PC board. This action can cause stress development in the solder joint. While designing for high power cycling applications the PC board should be chosen with a slightly higher TCE than the LCCC so that both the LCCC and the board expand and shrink at the same rate.

Heat dissipation remains the major concern in any surface mount package and LCCC is no exception. Besides the reduced surface area (due to the size of the package) and high heat generation, (due to high PC board density) the LCCC faces a major problem since it does not possess a lead frame to dissipate the heat. There are basically two ways of dissipating the heat generated by the chip. First method is to conduct the heat generated by the chip on to the PC

board which gets carried away through its end connectors. Second method is becoming popular but is still unconventional. In this the heat is carried through the chip carrier and dissipated out into the air.

In order to achieve this heat transfer, the heat must pass from the chip through the die attach and out through the external package casing. Theta JC is the term used to represent the thermal resistance of the chip to lead frame interface and the external package casing. Theta JC is dependent upon the quality and type of die to package attach medium, the die size, package substrate thickness and the package material composition (ref 1). Generally die attach material is a gold/silicon eutectic and the ceramic is made of alumina Al O . Any material which reduces theta JC should be preferred therefore beryllium has been looked into as a potential replacement for alumina. Two third of the heat is conducted to the PC board via solder pads and rest through the air gap between the LCCC and the PC board. Second method of dissipating heat is through the placement of solder pads on the LCCC directly under the chip. These solder pads are usually arranged in a checkboard pattern and match up with a solder plated copper grid on the substrate. This concept is generally used with metal core substrate. The solder grid on the surface of the substrate is connected to the metal core by plated vias that lead down from the grid directly to the metal core. The heat is dissipated through the metal core and out of the system.

Just placing solder pads directly under the chip can reduce the LCCC to PC board thermal resistance from 12.3 C/watt to 2.09 C/watt. It has also been observed that by adding the array of solder pads and plated through holes the resistance can be reduced to as low as 0.07 C/watt (ref 14, 16). Third method of dissipating heat is by placing the copper ground plane as near as possible to the component surface on the board. This method is not acceptable as the thermal vias used compete with signal channels for real estate and defeat the basic purpose of surface mount packages i.e reduction of layers on board.

It seems dissipating of heat from the chip to air would be the most popular method in the future. Heat sinks, a finned metal mass, is placed on the top of the heat generating device. There are basically two problems associated with this process. Firstly, the medium used to attach the heat sink to the device must be thermally conductive or have lower thermal resistance and secondly it should be ductile enough to absorb the stress generated through TCE mismatch. Thermal conductive epoxies seems to be an obvious choice since it takes care of both the problem. To cool the system it may be necessary to cool air over the heat sink. As the cooling air flows over the first device it warms up. This reduces the temperature differential for the next component downstream causing reduced rates of heat dissipation. Thus the components lying downstream do not cool off,

therefore they either need an enlarged heat sink or flow of cooling air should be increased.

Solder joint inspection and cleaning of PC board under the LCCC is another major problem.

Advantages :

1. High density
2. High reliability
3. High operating life
4. Hermetically sealed package
5. No lead damage problem
6. Reduced electrical parasites

Disadvantages :

1. Heat dissipation problem
2. Thermal expansion mismatch
3. High cost
4. Hard to clean and inspection

CHAPTER IV

SELECTION OF A SURFACE MOUNT COMPONENET

Selecting a particular surface mount component for a particular application is getting increasing difficult due to the plethora of such devices. The user has to decide which device would be more applicable to his needs. For this purpose he needs certain guidelines for making the most appropriate choice. A chart has been outlined by Michael Neumar (Fig 1) which acts as an aid in the selection of components. These components are rated against various aspects in manufacturing, assembly and their applications.

The first category is the manufacturing and the components are rated against the ease of manufacturing the component. The ratings were dependent upon how many changes were required to be made to convert DIP into the new style of package. SOIC received a very good rating, since it utilizes the same manufacturing technology as DIP's. The only difference is the size and the leads are bent outwards at the very last steps. The LCCC and PLCC received good ratings since very few changes are required from the existing DIP's technology.

The second category is the shipping and handling. The

LCCC received the highest rating of very good as it is leadless and therefore does not have to suffer from lead damages. The PLCC received a good rating as the leads are bent inwards in the form of the letter "J" and are less prone to lead damages. SOIC packages received a rating of fair. They are by far the most susceptible to lead damages. These leads are generally bent in inverted "gull wing" position making it vulnerable to any kind of external forces. Nowadays, some of the SOIC packages are coming with leads in "J" configuration to avoid the problems just described.

In placement category the components are rated on the ease of placement of components over the PC board. The PLCC and the SOIC received fair ratings because of the lead problems. Problems related to leads such as coplanarity, lead skew and breakage can lead to difficulties in placing the component. The LCCC received a good rating since it is leadless and secondly it has a flat upper surface. Therefore, it is easier to hold the component using a vacuum actuated placement machine.

Next we discuss the solderability issues as observed during reflow process. The SOIC received a very good rating solely because it is smaller, lighter and has a gull wing lead configuration. During soldering process SOIC's can align themselves to the solder pads because of surface tension and being light in weight. The LCCC and the PLCC

received a good rating as they allow for out gasing of the solvents from the solder paste.

Inspection category refers to the ease of inspection solder joints after final assembly. Here again the SOIC received a very good rating due to its (gull wing) configuration. The leads and the solder joints are exposed to the naked eye and therefore easier to inspect. The PLCC received a good rating. The inverted "J" leads are under the components, the fillets of solder formed around them are generally exposed. This allows easier visual inspection. The LCCC received a fair rating as the solder joints formed are under the component and cannot be easily inspected. Advanced and expensive techniques have to be used to overcome inspecting problem.

Next categories deal with the application aspects starting with military applications. The LCCC receives a very good rating. Primarily, the LCCC are made up of ceramics and have no difficulty in passing the stringent hermiticity requirements. The LCCC being leadless occupies less real estate therefore promote high density and high reliability which are very important issues in military applications. The PLCC and the SOIC received a poor rating. They are made up of plastic and both have leads, therefore they cannot qualify for military applications for the reasons discussed above.

Consumer products e.g TV's, VCR and stereo system the PLCC and the SOIC received a very good rating since they are less expensive to manufacture. Material cost of plastic is very low as compared to ceramics. They are small as compared to DIP package, therefore occupy less real estate. Hence, they are ideal for consumer product applications whereas the LCCC being expensive due to high material cost is less desirable for such applications.

Next category is memory. Memory components do not have high pin counts. Therefore, the LCCC received a poor rating as it primarily deals with high pin count number and are very expensive to build. The PLCC is good for memory applications as it is cheaper to manufacture. The SOIC are the most suited for memory applications, because of low pin count number and cheaper to manufacture and small in size.

Lastly, the VLSI applications category. Due to increased demands placed by VLSI to get maximum performance out of smallest possible area. High performance means high electrical and thermal performance of the assembly i.e reduced parasitics and timing problem. The SOIC package is least desirable for high I/O requirements and the LCCC and the PLCC perform well (good rating) as compared to SOIC. Although, they both have certain limitations discussed earlier.

This chart provides the user a broad outline on deciding to select a surface mount components. This can act as a

quick reference for reducing the choice from many to a few. Once the chart has been used to narrow the field, the expert system (PEX) can be used to match the right component (which is available) to the particular needs of the applications being studied.

CHAPTER V

PACKAGING EXPERT (PEX)

PEX is an expert system which aids in the selection and designing of packages for silicon dies. This expert system is implemented in Turbo Prolog and C language. It utilizes both forward and backward chaining process. The backward chaining process is used for the selection of an existing package and reduces the search space.

In backward chaining process there is a goal-driven strategy based upon the principle of resolution. Resolution is the process of starting with an initial goal statement and resolve it with one of the hypotheses to create a new clause. This process continues until it reaches a point where the new clause can be conclusively answered. In Prolog terms, goals lead to sub-goals, and sub-goals lead to other sub-goals, etc. This process continues until the sub-goals are satisfied [ref 10].

The forward chaining process enables the design of a new package. The mode of chaining describes the way in which the rules are initiated, e.g. by matching working memory elements against one side and then processing the other side.

5.1 This system comprises of various modules related to the packaging aspect of IC manufacturing. It is user

friendly and is menu driven. The different modules are :

i) Consultant (Packaging Expert System)

ii) CAD

iii) Material database

iv) Algorithms

5.2 The consultant is basically an expert system (PEX) implemented in Turbo Prolog and deals with the selection and designing of packages. PEX uses a frame based approach in representing the knowledge. The expert system can be accessed through the user interface and the logo for the expert system is displayed. The information specific to the company is held in technology database (files). The expert system has the following menu options :

i) INPUT

ii) RUN

iii) SHOW

iv) EXPLAIN

v) SAVE

vi) EXIT

5.2.1 INPUT MODE

This mode allows the user to input details of the package requirements. The screen contains prompts for the questions in the form of pull down menus. A suitable selection can be made by hitting the enter key. For numerical input data, the user is expected to key in a value for the parameter.

The input parameters pertain to the following issues :

i) Number of I/Os

ii) Hermiticity requirements

iii) Type of circuit

iv) Physical dimensions of the die

v) Device type

vi) Technology base

vii) Technology base

viii) Desired material

ix) Type of application

Based upon the responses to the above input, the expert system can figure out a package design.

5.2.2 RUN MODE

This mode is used to process the data obtained from the input mode. The run mode is activated by selecting the RUN option and hitting F10 key. The inference engine then figures out a suitable package (if possible) from the requested knowledge base.

5.2.3 SHOW MODE

This mode gives the user the final analysis of the design without providing any reasons for arriving at the package design. It gives all the pertinent information about the package like the cavity size, the physical dimensions, wire bond information, material and number of pins etc.

5.2.4 EXPLAIN MODE

This mode provides more information than the show mode. It traces the logic structure of the expert system and gives information as to why it took a particular decision. All the rules that were fired are included in this mode.

5.2.5 SAVE MODE

This mode enables the user to store the design of a particular package that has derived from the expert system. This can be used later without having to run the software again.

5.2.6 EXIT MODE

This mode brings the user out of the expert system to the user interface.

CHAPTER VI

Description of the rules incorporated and their integration with the existing Expert System

At the PEX menu, the user selects INPUT mode and is prompted to key in or select values for the parameters from the pull down menu screen. According to the new incorporated rule, the user has to select the device type viz. Plated Through Hole (PTH) or Surface Mount Device (SMD) at the input mode. The value(dev_type, "PTH") or value (dev_type, "PTH") rule is activated depending upon the selection made by the user. Both the device types have their respective technical bases as shown below;

Device type : Plated Through Hole (PTH)

Technical base :

i) MMI

ii) JEDEC

iii) Kyocera

Device type : Surface Mount Device (SMD)

Technical base :

i) VLSI Technology

ii) Signetics

Typically the PTH device comprises of the

a) Dual-in-line package (DIP)

b) Ceramic dual-in-line package (Cerdip)

c) Pin Grid Array (PGA)

The commonly available surface mount devices are :

a) Small Outline Integrated Circuit package (SOIC).

Available in 8, 14, 16, 20, 24 and 28 dual-in-line row of lead versions and is available in two width sizes i.e. 0.15 inch and 0.3 inch. There are two possible lead configurations available, namely,

i) "Gull Wing", the leads are bent outwards in inverted gull wing format (SOG).

ii) "J", the leads are bent inwards in the form of the letter J (SOJ).

b) Plastic Leaded Chip Carrier (PLCC) :

The single row plastic leaded chip carrier is available in square FN package in 20, 28, 44, 52 and 68 lead version with the leads in "J" configuration.

c) Leadless Ceramic Chip Carrier (LCCC) :

Basically this device is leadless and made out of ceramic material. Available in 18, 20, 28, 32, 44, 52 and 68 pad versions.

d) Flat packs :

The quad flat packs are available in various body sizes, thickness and lead pitches covering pin counts of 44 through 160.

At the run mode, this input data is processed. The inference engine then figures out a suitable package (if possible) from the requested knowledge base. The user input data is stored in the slots of the frame (ic_package in our case). From then onwards the program uses backward chaining process with one of the goal being the selection of all the packages from the "smdba" database, with the number of pins atleast the same or greater than the user input. The other goal being the matching of the type of the circuit desired. Various rules such as rule (get_dimensions, ic_package), rule (set_type_circuit, ic_package), rule (get_number_pins, ic_package) and rule (body_dimensions, ic_package) are fired to obtain all the possible set of packages available in the surface mount device (SMD) database or the plated through hole database. The selected packages are then written into a display file.

Once all the possible packages are identified these packages are checked for the maximum die size that this package can encapsulate. If the user desired die dimensions lie within the available die size then that package suc-

ceeds otherwise the package fails and is discarded.

In this manner, the list of packages is short listed. Next, the user selected technology base for each of the device type (SMD or PTH) is initiated. Once the select_tech rule (for technology base) is initiated then it searches for that technology database. As technology database is selected, then depending upon the type of package and materials requirements i.e. 'Plastic' or 'Ceramic' the appropriate rule is initiated.

For example, if the device type is SMD and the technology database selected is VLSI Technology and the package and material desired is "PLCC" and "Plastic" respectively, then the appropriate rule initiated would be "vlsi_plcc".

The packages available in vlsi_plcc database is searched satisfying the following requirements;

i) Range of number of pins e.g N + 5

ii) The die dimensions have to be satisfied;

a) Die_width < body width minus peripheral margin

b) Die_length < body length minus peripheral margin.

The package which satisfies these requirements are se lected, otherwise a prompt stating that no more suitable(s) are available or the database has to be upgraded is displayed on the screen.

The selected packages provide a detailed outline of the package, describing all the dimensions while adhering to JEDEC standards. Certain data concerning the thermal resistance theta JA and theta JC is provided.

The user can also obtain the thermal resistance information through graphical files stored in the "Materials Database" module of PEX which can be accessed through the show mode interactively too. Besides providing theta values, these graphs also makes a comparison between the alloy 42 and copper frame (fig 3, 4, 6,7).

CHAPTER VII

SOLDER PASTE - SELECTION AND APPLICATION CRITERIA

The solder paste is used for attaching the leads of the surface mount devices to the solder lands on the PC board. The solder paste can be applied to the solder lands by dispensing (syringe), screening or stenciling. In the selection of solder paste, various physical and chemical properties have to be considered. Characteristics such as the fluxing agents, vehicle system, solder powder alloy, particle size, morphological characteristics and metal loading play an important role in the preparation and the selection of solder paste. The selection of the solder paste is dependent upon the nature of the application, therefore the available paste should meet the needs of the user and the desired product.

7.1 Properties desired in the solder paste :

Solder paste is essentially comprised of metal powder particles in a thickened flux vehicle. The solder paste is manufactured by quickly chilling the molten solder of desired composition over a rotating wheel to form fine solder particles (ref 6).

There are basically seven factors that affect solder paste selection, namely;

a) The metal composition of solder paste.

b) The activation level required to wet the metallization.

c) Application of solder paste.

d) The PC board layout

e) The desired working life of the paste.

f) The reflow method used.

g) The cleaning process used.

7.2 The metal composition of the solder paste :

Figure 11 gives the composition of various alloys along with their melting temperatures and other properties are described. Basically, there are four most important criteria for the alloy selection.

i) Melting joints : Substrate material on which the surface mount device is to assembled. Ceramic devices when attached on to ceramic boards require high temperature solder (>225 deg C). Whereas plastic devices when placed over epoxy-glass boards cannot handle such high temperatures, thus lower melting solders are used.

ii) The compatibility of the solder with the metallizations on the substrate and component leads (ref ray). For example, use of indium-lead alloy as solder for gold terminations against tin-lead alloy.

iii) Solder Strength : Normal tin-lead solder is considered a soft solder and work at low mechanical stress. Different solders, such as, tin-antimony alloy solders are recommended for high mechanical strengths.

iv) The cost factors plays an important role. Certain applications need the additions of silver to basic lead-tin solder composition. The percentage of silver in the solder can be adjusted without altering the overall affect and making it cheaper by reducing silver content.

The percentage of metal content in a solder drastically affects the reflowed solder thickness. Typically 88% to 90% of metal content is desired for highly reliable surface mount solder joints. Also, the fillet size and solder bridging are functions of metal content. Excess metal content leads to increased fillet size but also increases the chances for solder bridging.

The overall effect of metal content is so drastic that a 10% change in metal content of a solder paste can lead to excessive solder at the joints to insufficient solder at the same location for the same solder paste thickness.

7.3 Activation level required to wet the metallization :

The flux acts as the vehicle in the solder paste and can be classified under three categories, namely, R (rosin flux), RMA (mildly activated rosin) and RA (fully activated

rosin). The activators within the RA and RMA fluxes helps in promoting the wetting of the molten solder to the component leads and their solder lands by removing oxides and other contaminants. In other words, the degree of wettability of the metallization determines the activation level of the flux. For example, a clean, oxide-free solderable surface like clean tinned leads needs a paste with low activation level RMA paste. Whereas a thick film silver, palladium-silver or copper pads, may require higher activity level RMA paste.

Various factors influence the selection of activation level in the flux.

i) The quality of leads (purity) to be soldered.

ii) The firing of the cermet thick pastes at optimum temperature.

iii) The oxidation affect from multiple firing.

iv) Perform the reflow under an inert (Nitrogen furnace, vapor phase reflow) or, especially, a reducing atmosphere so that a lower activity paste can be used. Avoid charring the solder vehicle residue.

v) Adjustment of the metallization

7.4 Application of solder paste :

Basically, there are three types of solder paste application methods, namely, printing using a screen, printing using a metal mask and last syringe. Screen printing gives

the best definition but metal mask printing provides high reproducibility with regards to paste thickness and are more durable (ref ISHM). Syringing is applicable where high accuracy is desired and printing cannot be done e.g nonplanar surface. In screen printing, the open area of the screen mesh are 2.5 - 5 times greater than the maximum particle diameter. This is to facilitate the passage of particles of the solder powder through the mesh.

For example, in a 80 mesh screen the opening is 175-262 micron, depending upon wire diameter and the maximum particle size would be 35-52 micron for a 5 times margin, and 70-104 micron for a 2.5 times margin. It is difficult to achieve 5x margin without admitting an excessive number of fines into the powder as compared to 2.5 times. For syringing, the particle size is not important as it does not have to pass through a mesh.

7.5 The PC board layout :

The PC board layout determines the spacing of solder lands. If the solder lands are close together then the solder paste used has minimum slump. Slump is the ability of the paste to spread out after being deposited on the lands. It is dependent on the metal content in the paste. For example, if 0.125 inch wide pads are spaced 20 mils apart (0.145 inch wide centerline spacing), 15% slump can be tolerated, whereas 7% is acceptable if only 10 mils

spacing is required.

7.6 The working life :

It can be defined as the maximum time that can elapse between opening of the solder paste jar to past reflow without degradations of the paste's rheological properties. This includes the total time needed for printing, placement, baking and handling between operations.

The solvent determines the working life. For example, the boiling point, the ambient temperature and relative humidity are important factors in determining the working life of the paste. For example, high boiling point solvent has a higher working life as compared to low boiling point solvent.

7.7 The reflow method :

The reflow profile can drastically affect t the formation of solder balls, solder bridging and voids. For a low boiling point solvent, the heating through reflow should be minimized and gradual so that solvent does not explode violently leading to all the above mentioned problems.

7.8 The Cleaning Method :

To large extend, the residues under the component and circuit design determines the cleaning method to be used. The solder residues are to be cleaned using a solvent.

Nowadays, a solvent containing alcohol for removing ionic or highly polar species (from the activator) are preferred over a halogenated hydrocarbon alone.

CHAPTER VIII

CONCLUSIONS

Nowadays, the conventional dual-in-line (DIP) package is no more the standard package. It has become uneconomical and unattractive due to the todays densely packed semiconductor applications. Surface mount components provides the necessary solutions for the growing needs of VLSI applications. They are small in size, weigh less, high yield and can be placed on both the sides of the board.

Various types of packages are available to a potential user. There are basically three types of surface mount packages widely available, such as, Small Outline Integrated Circuit (SOIC), Plastic Leaded Chip Carrier (PLCC) and Leadless Ceramic Chip Carrier (LCCC). Previously, only one type of package i.e. dual-in-line package was clearly the obvious choice. Now, with the advent of new packages, the user gets a chance to weigh his options before actually investing into a new package design for his specific needs. Thus, there is a need to understand advantages and disadvantages of each design packages available in the market today.

Therefore, an expert system (PEX) together with the component selection chart have been developed to examine

all facets of both the operation and application of these packages and choose the best design for the user. The expert system goes one step further and also helps in supplying the information needed to design a new package if the required package design is not available with the sup pliers.

Major problems in the designing of packages is the thermal mismatch of the materials used for packaging and its thermal resistance. The expert system (PEX) provides the thermal resistance of various surface mount packages as a function of die size in the form of graphs.

Once the package has been selected or designed, it is necessary to obtain the footprint information. The PEX also provides the footprint information for all the surface mount package available in the market. Besides, it aids in the selection and application of solder paste onto the board.

Surface mount technology, as a whole, has a bright future. Technologies such as the solder reflow process, package placement on the board, repair and rework of packages have to be understood. The surface mount technology would be totally automated through the use of Expert System (PEX) if the above mentioned technologies can be incorporated as rules into the system. Further development of the expert system would help the Semiconductor Research Corporation members in not only selecting a component but also

to select other things e.g. appropriate solder paste, reflow ovens, placement machines and repair/reworking machines for their use.

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	MANUFACTURING	SHIPPING	PLACEMENT	SOLDERABILITY	INSPECTION	MILITARY	CONSUMER	MAIN FRAME	MEMORY	VLSI
LCCC	G	VG	G	G	F	VG	P	VG	P	G
PLCC	G	G	F	G	G	P	VG	VG	G	G
SOIC	VG	F	F	VG	VG	P	VG	VG	VG	P
OVCC	F	VG	G	G	G	G	P	VG	P	VG
RLCC	F	VG	VG	VG	VG	VG	VG	VG	P	VG

FIGURE 1 Application Chart for component selection (ref 1.)

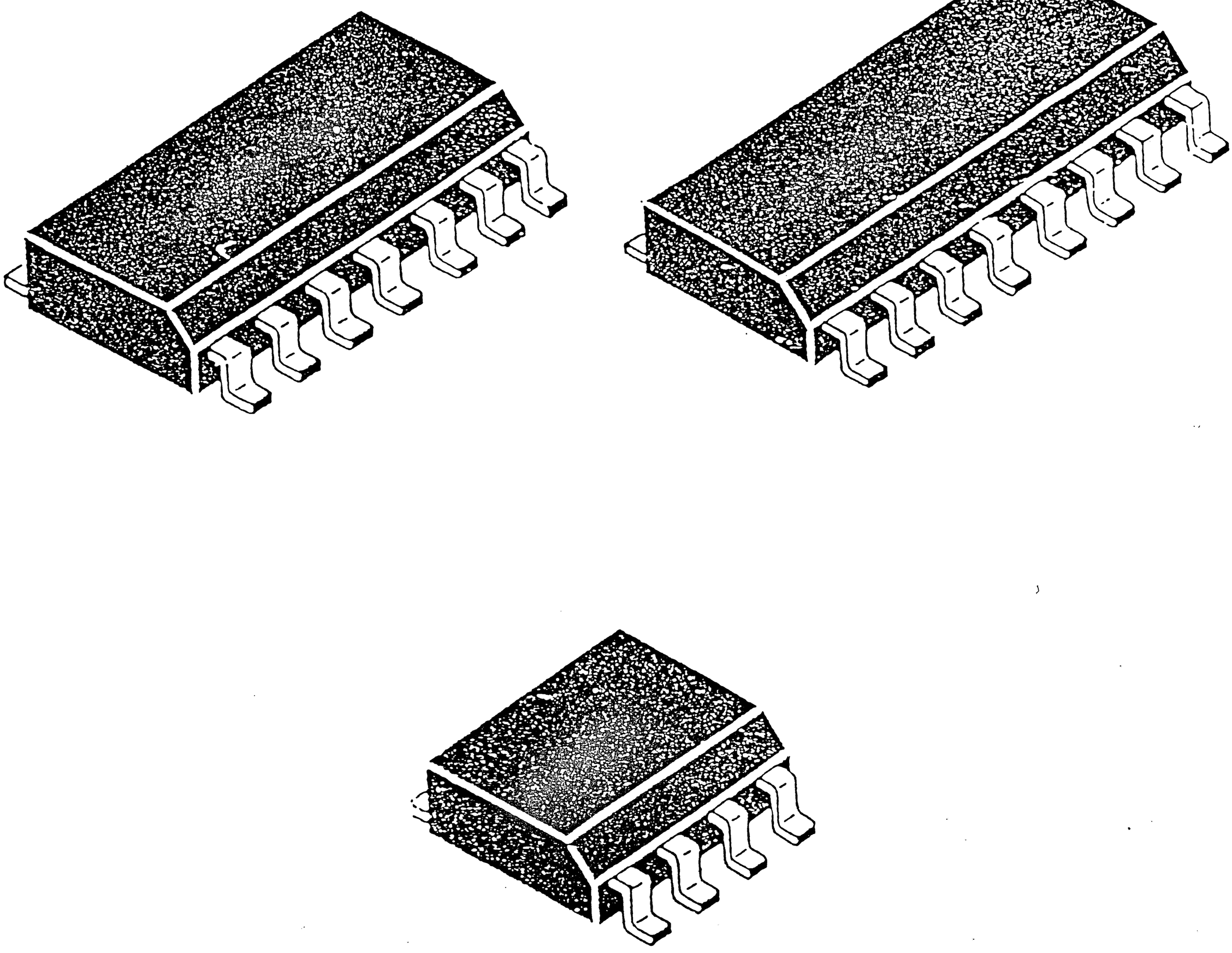
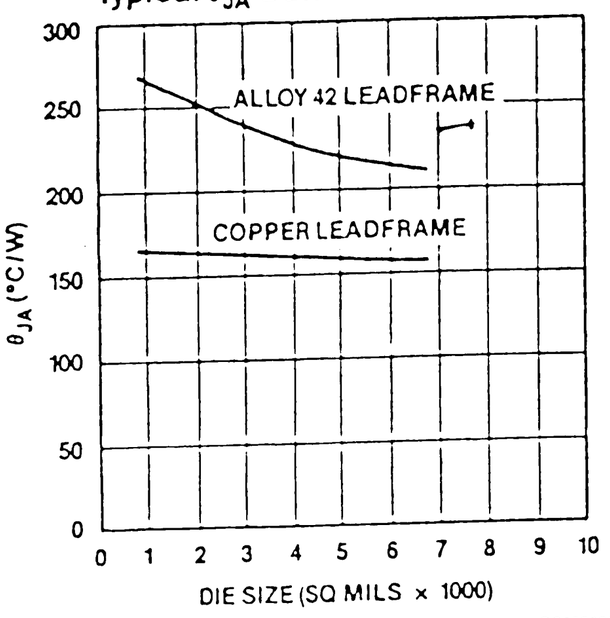


FIGURE 2

SOIC DEVICES

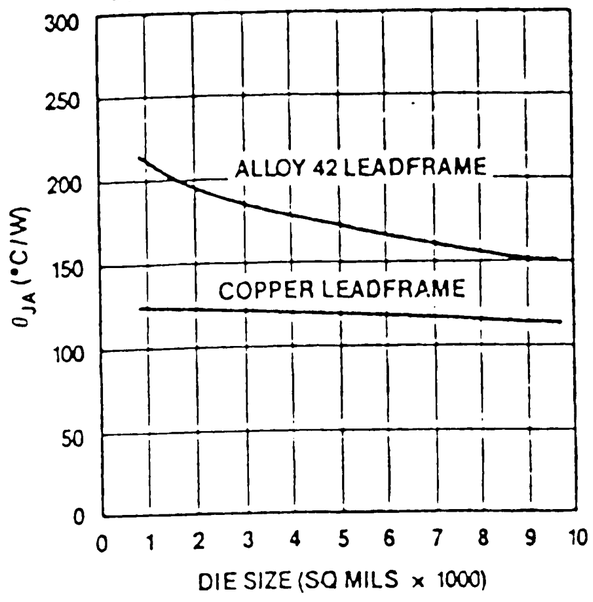
TYPICAL SMD THERMAL (θ_{JA})

Typical θ_{JA} Data SO-8[1]



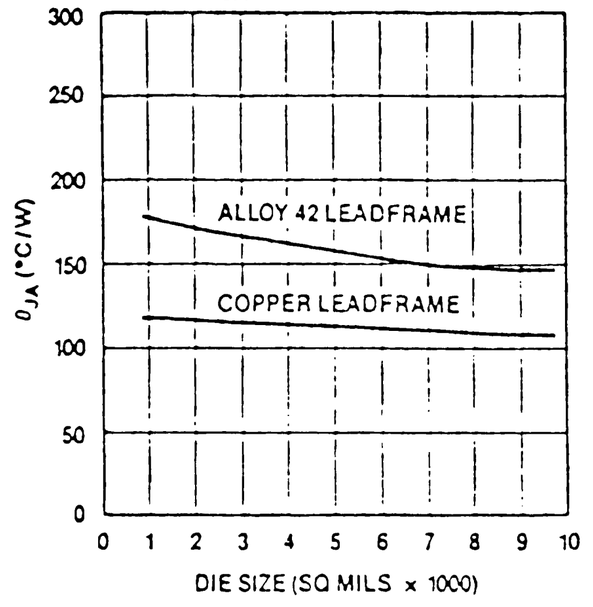
OP02380S

Typical θ_{JA} Data SO-14[1]



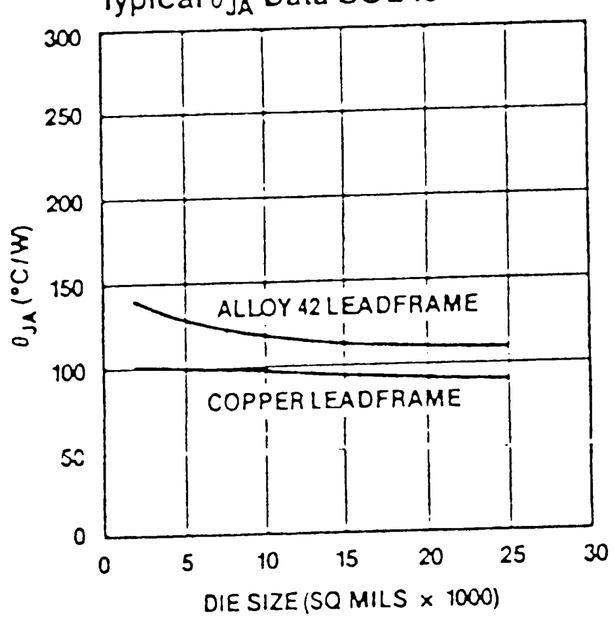
OP02390S

Typical θ_{JA} Data SO-16[1]



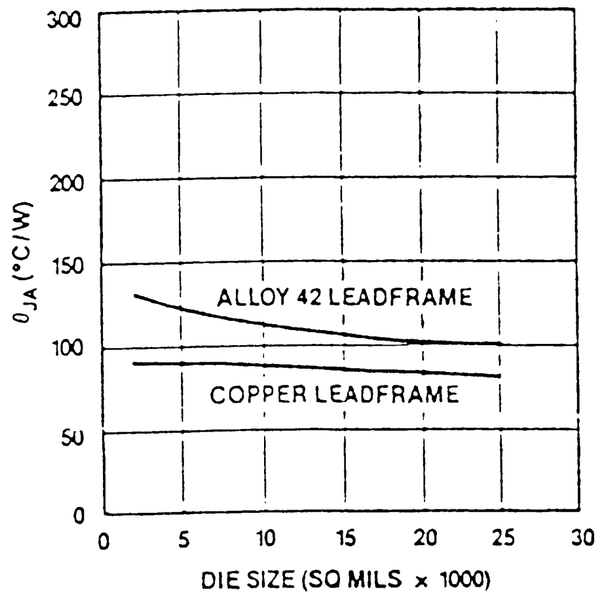
OP02400S

Typical θ_{JA} Data SOL-16[2]



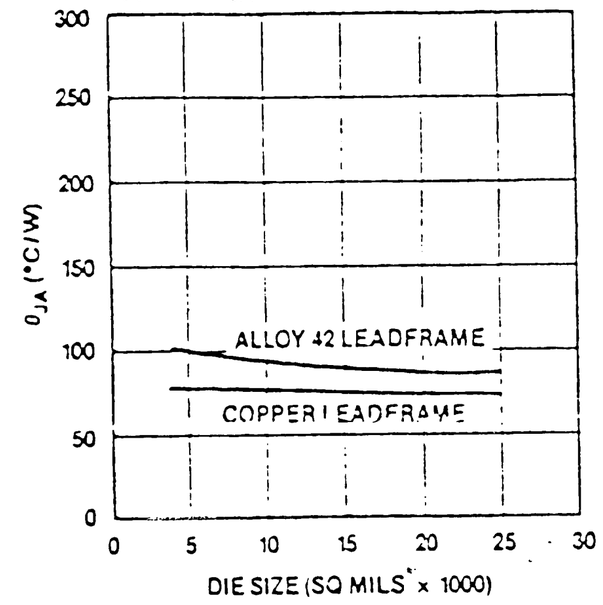
OP02411S

Typical θ_{JA} Data SOL-20[3]



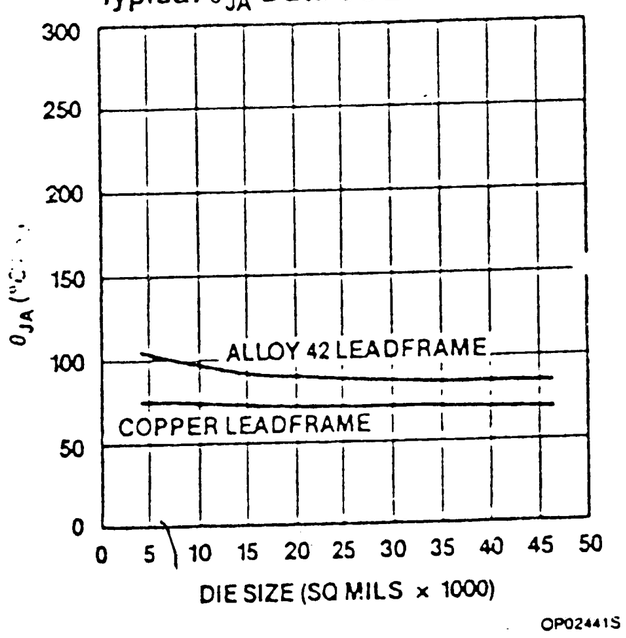
OP02421S

Typical θ_{JA} Data SOL-24[3]



OP02431S

Typical θ_{JA} Data SOL-28[3]



OP02441S

NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12" × 0.75" × 0.059")
Accuracy:	±15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

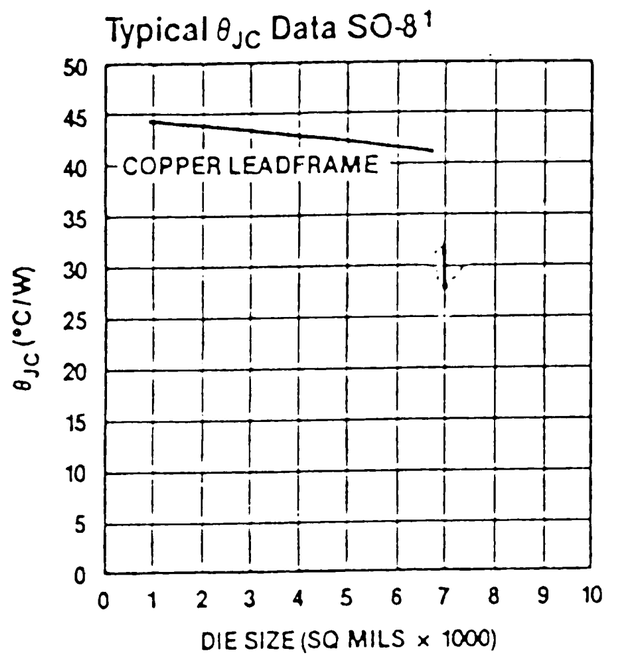
3. TEST CONDITIONS:

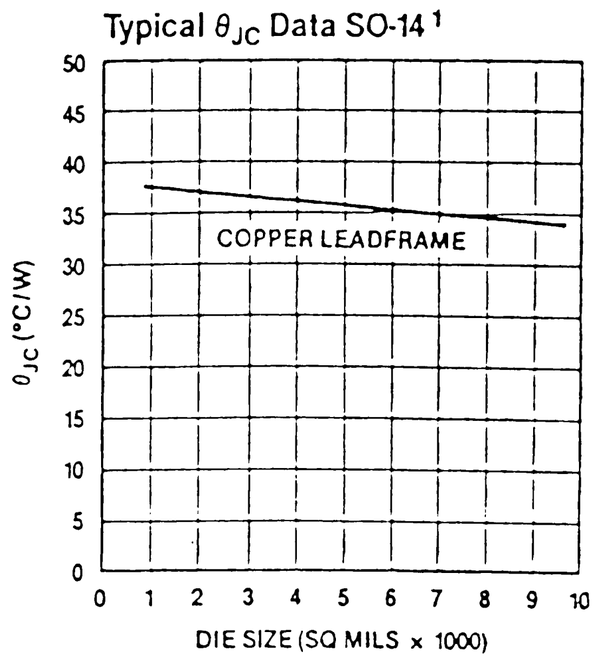
Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

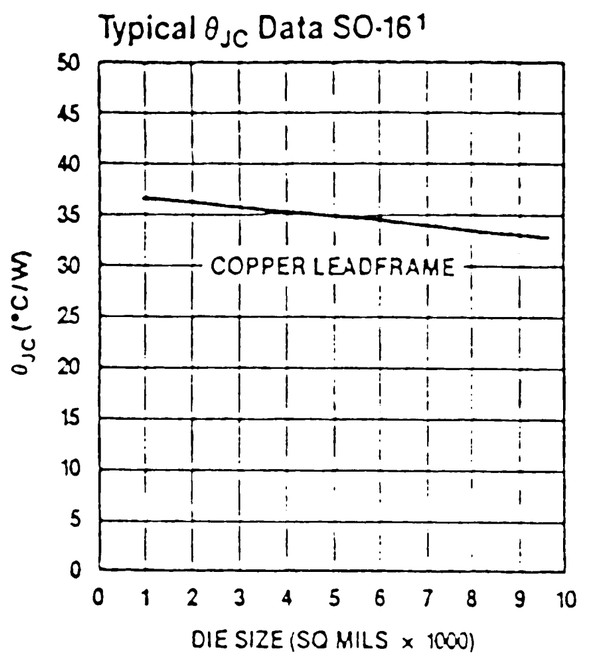
FIGURE 3

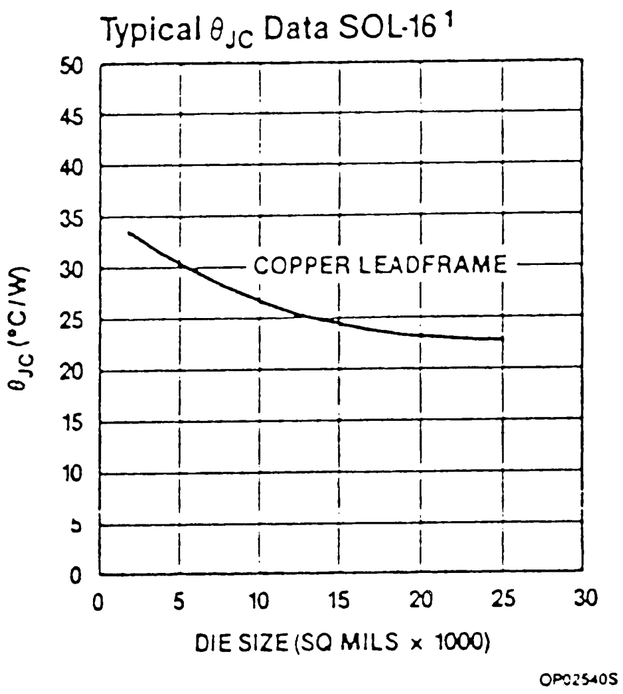
Thermal Resistance for SOIC Devices (courtesy Signetics)

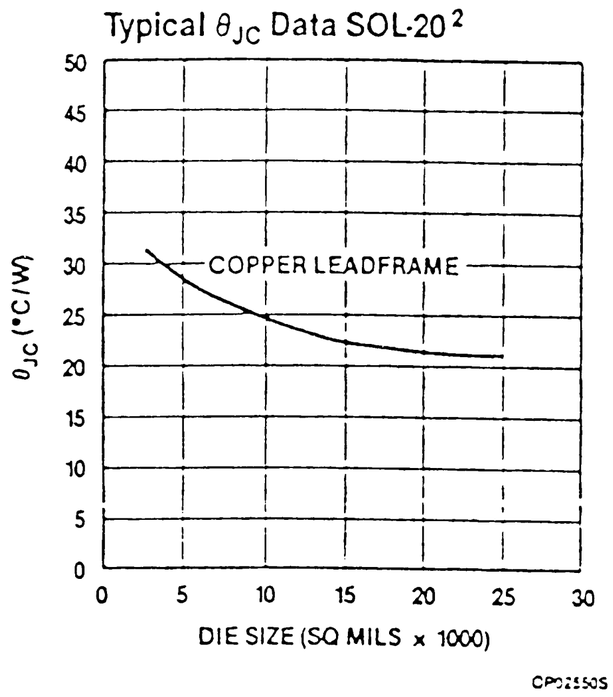
TYPICAL SMD THERMAL (θ_{JC})

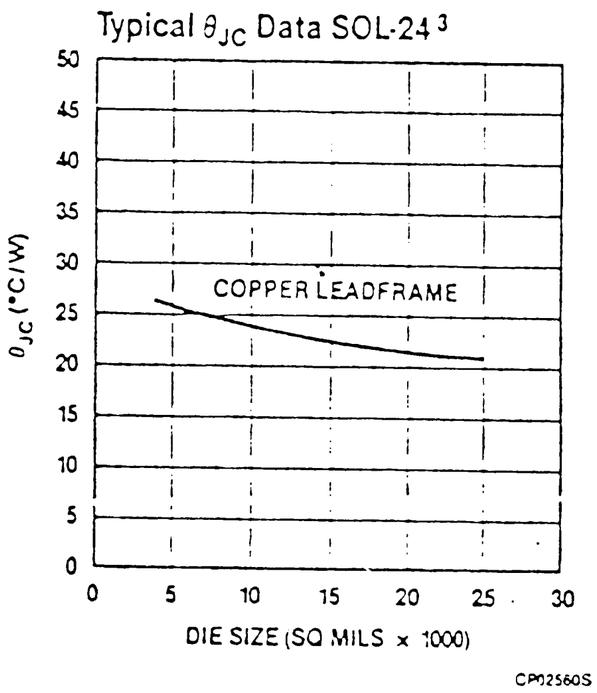


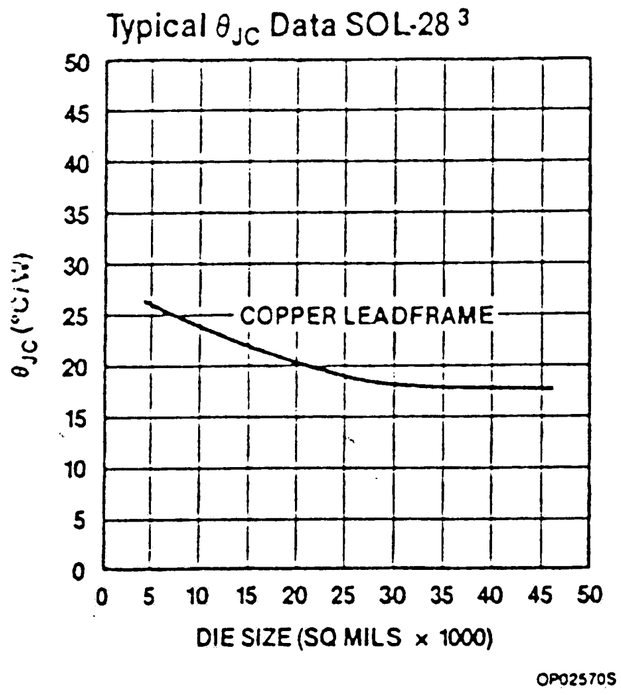












NOTES:

1. TEST CONDITIONS:
   Power dissipation: 0.5W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

2. TEST CONDITIONS:
   Power dissipation: 0.7W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

3. TEST CONDITIONS:
   Power dissipation: 1.0W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

FIGURE 4
Thermal Resistance for Soic Devices (courtesy Signetics)

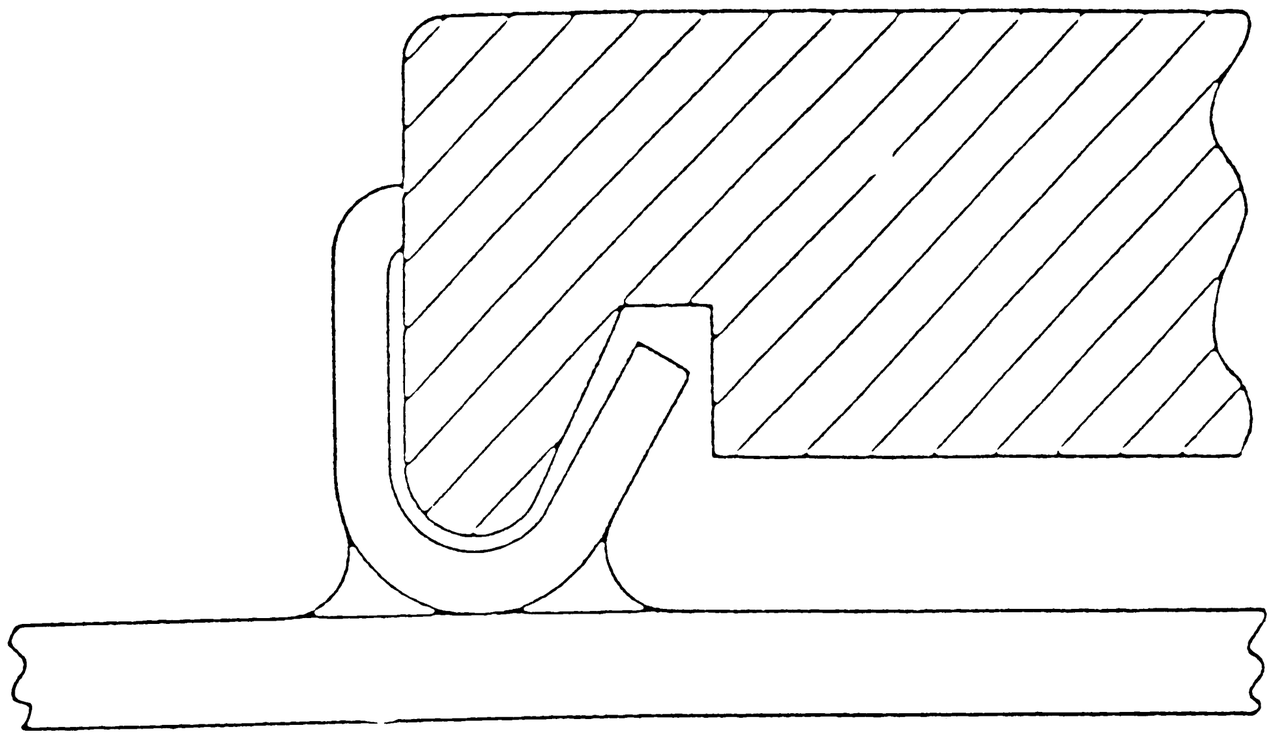
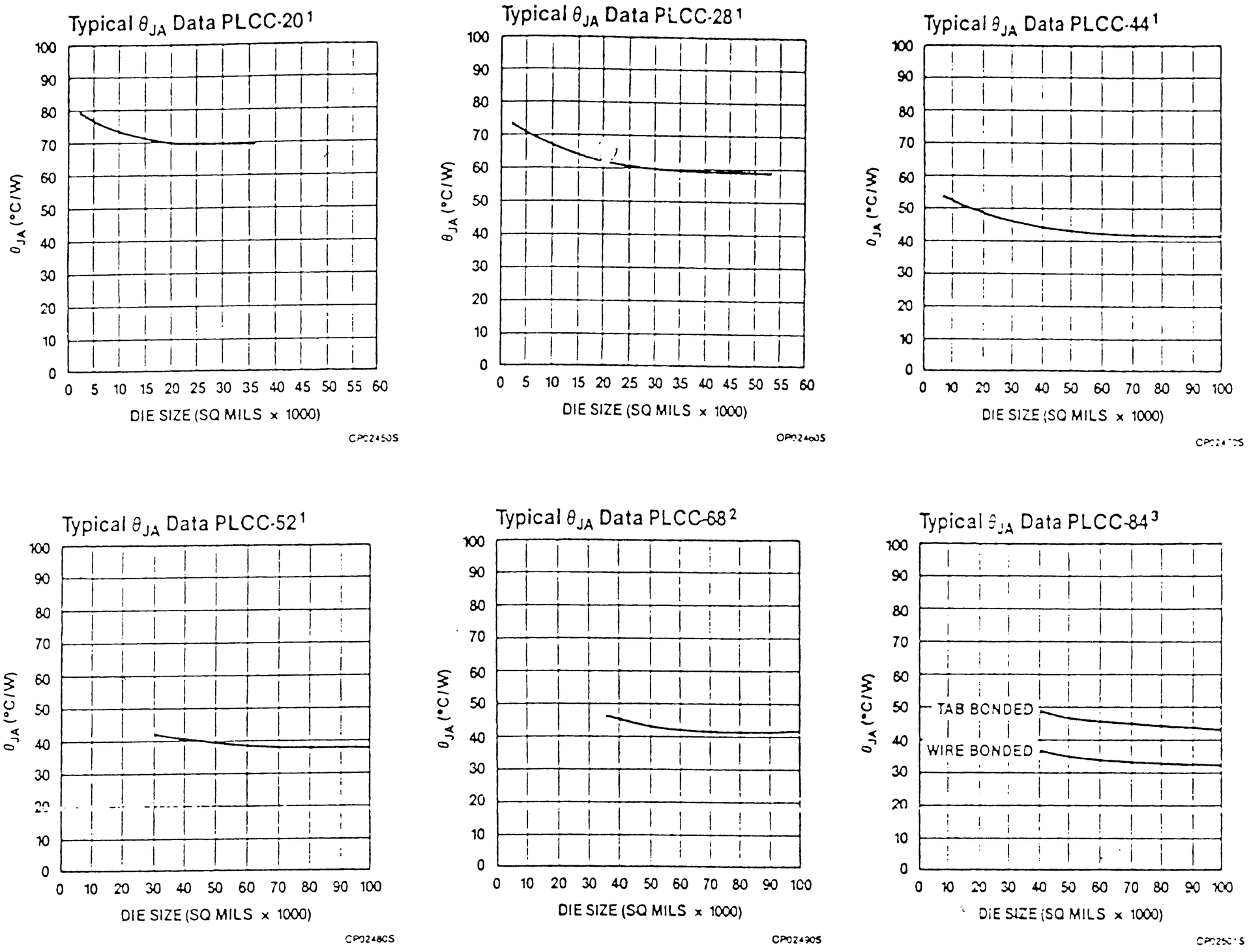


FIGURE 5

PLCC "J" LEAD
CONFIGURATION

TYPICAL SMD THERMAL (θ_{JA})



NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	± 15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	± 15%

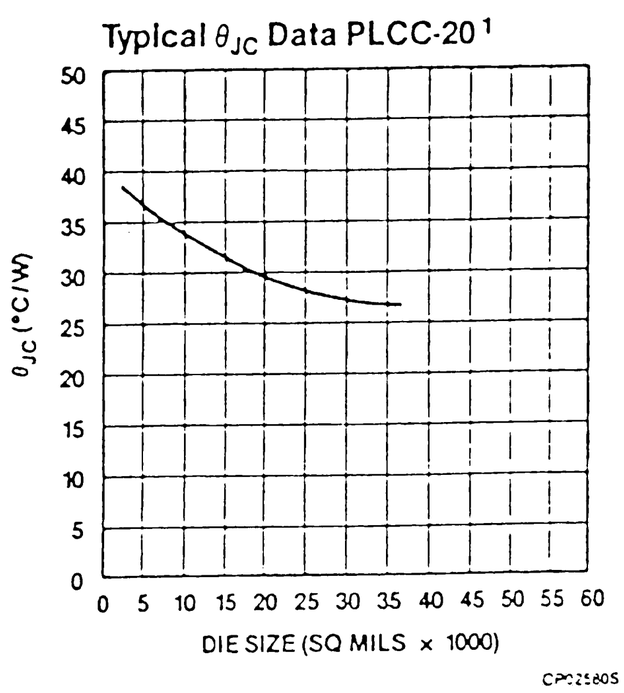
3. TEST CONDITIONS:

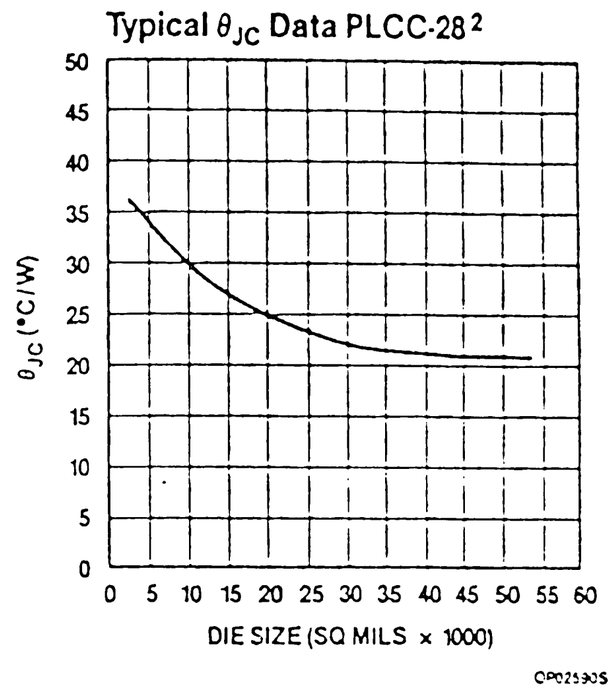
Test ambient:	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	± 15%

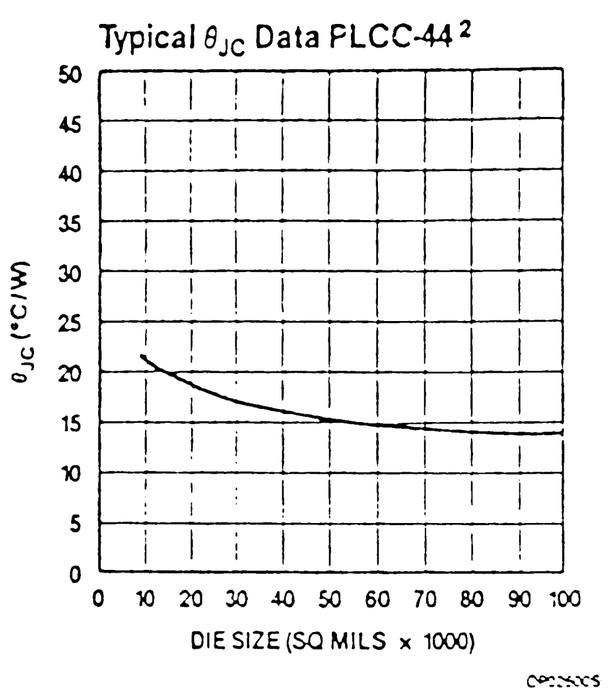
FIGURE 6

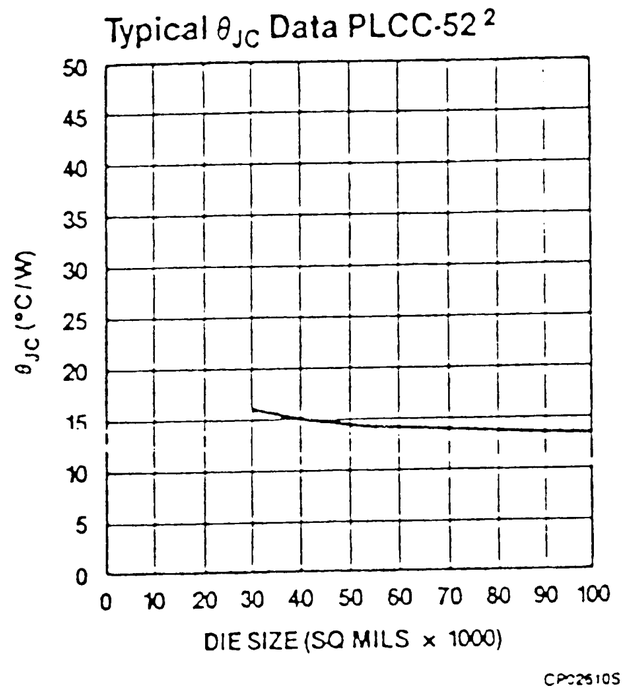
Thermal Resistance for PLCC Devices (courtesy Signetics)

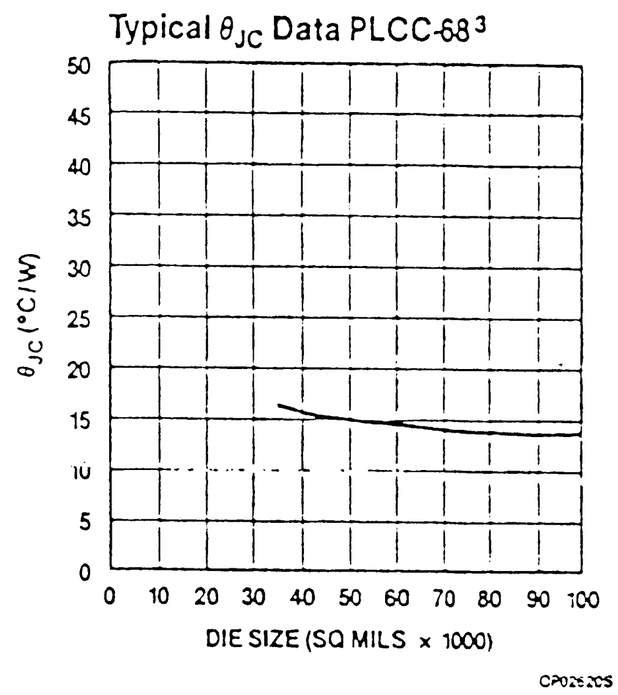
TYPICAL SMD THERMAL (θ_{JC})

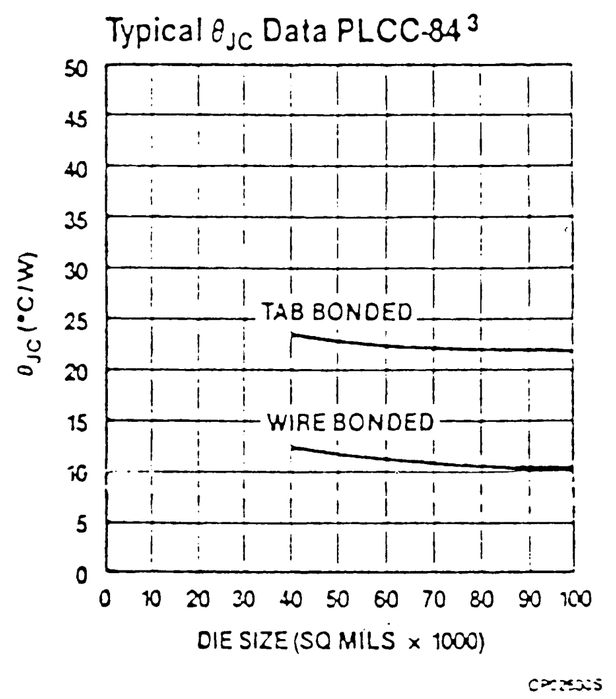












NOTES:

1. TEST CONDITIONS:
   Power dissipation: 0.75W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

2. TEST CONDITIONS:
   Power dissipation: 1.0W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

3. TEST CONDITIONS:
   Power dissipation: 2.0W
   Test fixture: "Infinite" heat sink
   Accuracy: ± 15%

FIGURE 7

Thermal Resistance for PLCC Devices (courtesy Signetics)

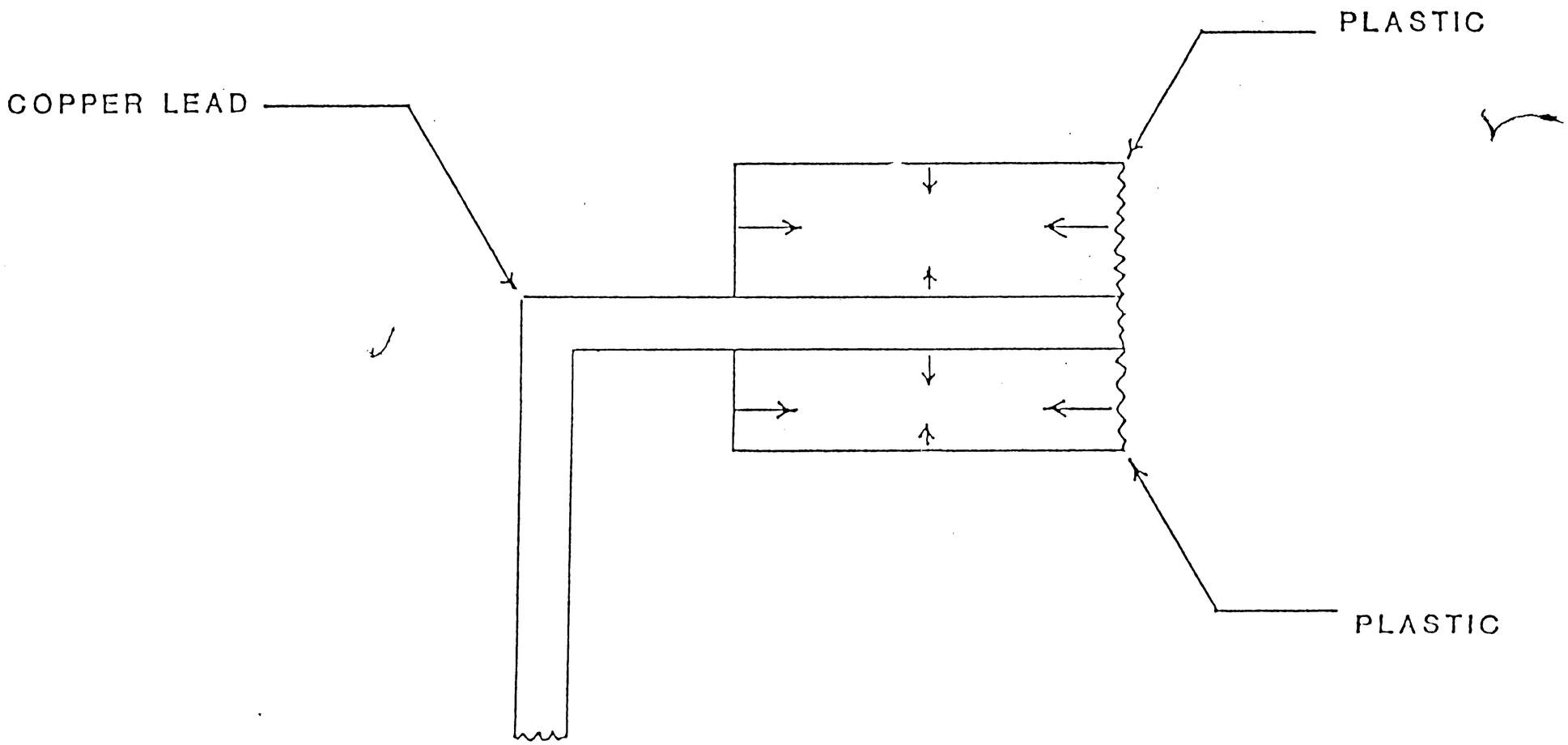


FIGURE.8

STRESS AT PLASTIC/LEAD INTERFACE

COEFFICIENT
OF
EXPANSION

UNIT/UNIT/°C

α CU=160 X10 $^{-7}$

α 1=250 X 10 $^{-7}$

α 2=800 X 10 $^{-7}$

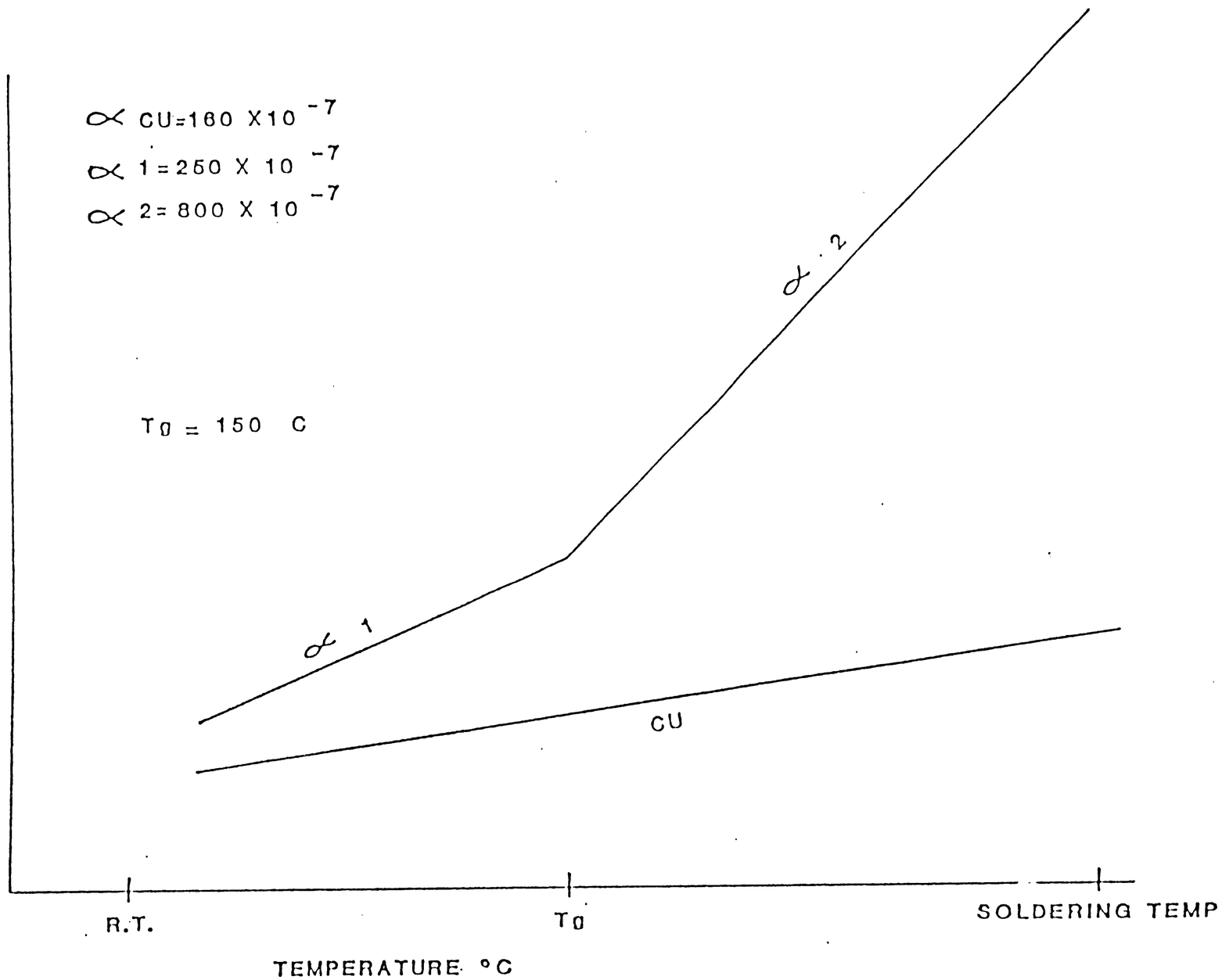


FIGURE 9

PLASTIC'S TWO TIER TCE

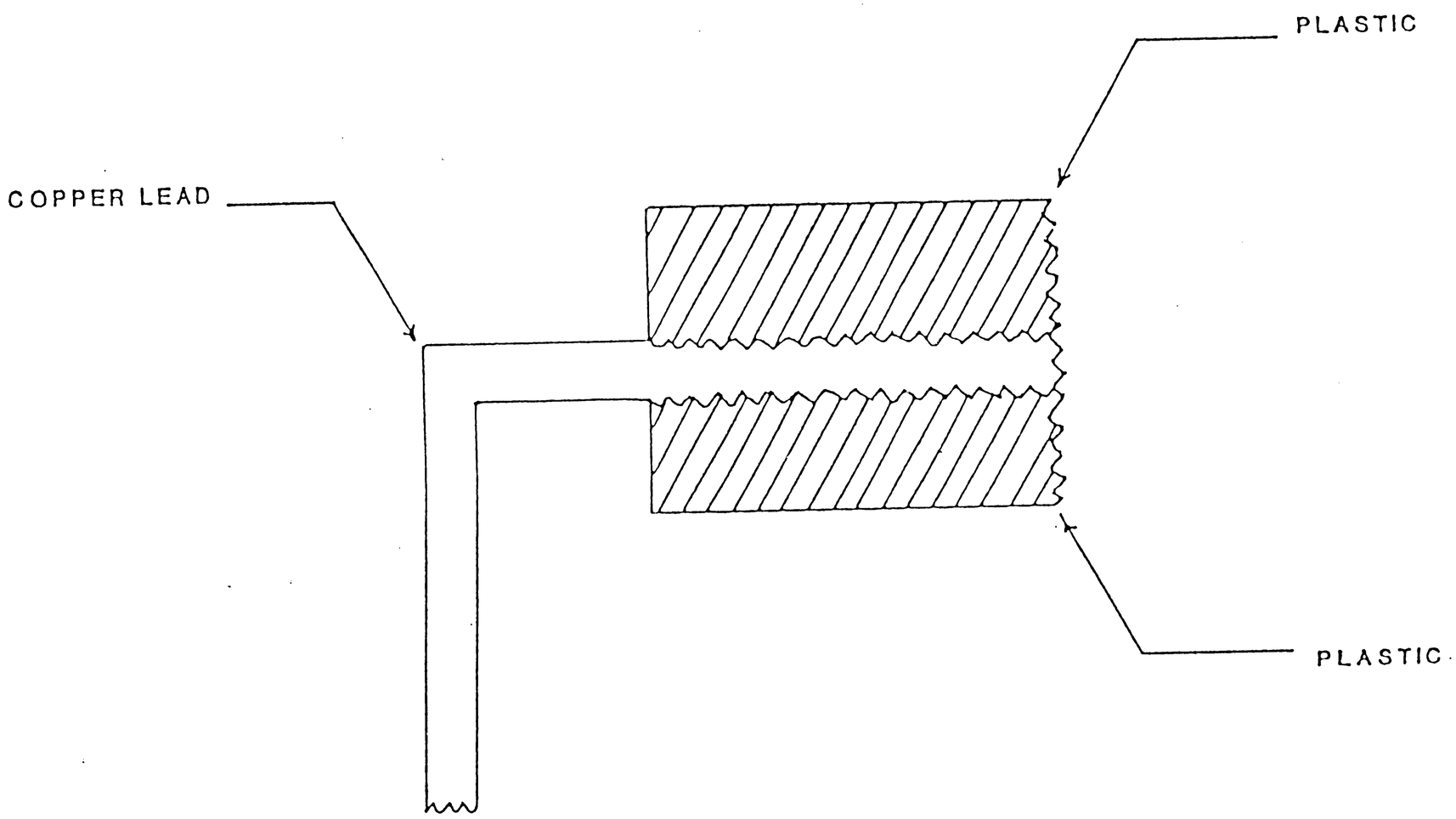


FIGURE 10

JAGGED EDGE LEAD FRAME