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THE DEVELOPMENT OF

A MERGED

BIPOLAR - CMOS TECHNOLOGY

by

Joseph R. Radosevich

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

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Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

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(date)

Professor in Charge

Chairman of Department

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ABSTRACT

A process merging a bipolar transistor with an existing CMOS technology is described. With the development charter specifying that there be no modifications to the existing CMOS process parameters, there were many constraints placed on the development of the integrated process. Computer simulations were performed, test patterns created and experiments designed to determine the proper bipolar parameters. By settling for a moderate performance *npn* bipolar transistor, however, the number of added processing steps was minimized and a low cost manufacturable product achieved.

The key factors of this process include using the CMOS *n*-tub as the collector of the bipolar transistor, implanting boron into the collector and driving it in to form the base and using the CMOS source/drain implants for the emitter and n^+-contact to the collector. Contact to the active base diffusion is formed concurrently with the source/drain boron difluoride implant of the *p*-channel transistors. The tantalum silicide/ *n*-polysilicon CMOS gate structure is used as a spacer to separate the n^+-emitter from the p^+-base contact. To guard against emitter to collector punch-through, the silicide/gate oxide spacer is also used to separate the n^+-emitter from the heavy channel stop doping under the collector field oxide. Although transistors were fabricated with common-emitter dc current gains in the range of 50-100 with acceptable break-down voltages, a problem with decreased gain at small collector currents was observed on many devices. To overcome this effect, it was experimentally determined that an additional mask step was required to block out the CMOS phosphorus graded junction implant from the bipolar emitter structure.

1. INTRODUCTION

1.1 Background

Combining high performance bipolar and MOS transistors on the same integrated circuit is attractive to the VLSI designer. MOS transistors maintain an edge in packing density and the ability to integrate large complex functions with high yields. CMOS circuits have the additional advantage of low power dissipation and large noise margins. The bipolar transistor has an advantage in switching speed, better noise performance, superior analog performance and greater current drive per unit area than an MOS transistor.

Optimization of MOS transistors implies reducing gate oxide thicknesses, junction depths, polysilicon or polycide sheet resistance and gate lengths, lower process temperatures and more stringent lithographic capabilities. These trends are consistent with bipolar VLSI technology. For enhanced bipolar performance, polysilicon emitters, walled emitters, Schottky diodes and thin epitaxy with buried layers are necessary components. A common need of both technologies is a high density multilayer interconnect scheme.

By judiciously mixing the two technologies, the performance of high speed digital/analog systems can exceed circuits based on either technology alone. As many of the features distinguishing bipolar and MOS technologies are becoming less distinct in VLSI, the advantage of having both transistors on the same integrated circuit will increase. Thus, there has been a great deal of interest shown in the combined bipolar-CMOS process usually known as BiMOS or BiCMOS.

The BiCMOS technology has begun to be used widely in many kinds of integrated circuits ranging from linear ICs, Power ICs [1] and analog-digital mixed LSIs [2] [3] to high speed digital VLSIs. High speed low power logic and memory applications include high speed gate arrays, [4] [5] microprocessors and static RAMs.[6] [7] While the speed of BiCMOS circuits can come close to that of bipolar ECL devices, the power consumption remains at a level similar to

a CMOS device. BiCMOS is, therefore, regarded as a suitable technology for realizing both high speed and high density at the same time.

The first 2.0μm design rule BiMOS products, with twice the speed advantage over CMOS, appeared on the market place in 1985. It was two years after 2.0μm CMOS but one year ahead of the next generation, 1.3μm CMOS products. The first 1.3μm BiCMOS products were introduced in 1987 with CMOS products of the same performance expected in 1990. [5] BiCMOS can smooth cycles in the integrated circuit industry by working between new generation CMOS introductions. It may provide a way to increase circuit performance without shrinking process design rules and thereby extend the the life of each CMOS technology.

1.2 Historical Review Of BiCMOS

As early as 1968, merged CMOS and bipolar devices had been proposed and a paper published by Lin .et.al.[8] In this early attempt, common-collector *npn* transistors were fabricated using a diffused n^+ source-drain region as emitter, a diffused p^- isolation region as a base and a n^- substrate as a collector. With the common-collector bipolar transistor being unsuitable for many circuit applications, the approach did not progress.

Two paths of technology integration were then pursued. One approach involved adding CMOS capability into existing bipolar processes.[9] [10] These technologies involved epitaxial layers and isolations so that process complexity is too high and circuit density too low for large-scale integration.[11] Since a relatively thick epitaxial layer is used to admit the deep well diffusion of the CMOS process, the cut-off frequency (f_t) of the bipolar transistor is also compromised.

A more attractive solution to the compatibility problem of MOS and bipolar transistors was offered when a CMOS extension of NMOS technology was demonstrated by utilizing a lightly doped *p*-type substrate and placing the *p*-channel transistors into an *n*-well.[12] [13] Tripple-

diffused, self-isolated bipolar transistors using the *n*-well as the collector were described for this process by Black .et.al[12] in 1976 but unfavorable tradeoffs between device parameters were necessary. Some of these problems were resolved by Hoefflinger .et.al [14] in a later fully ion implanted process with a two-step implanted base. The two-step implanted base, one for the active base with low dose and the other with low energy and high dose for the inactive base, was introduced to allow the independent adjustment of the bipolar transistor parameters. With a strong forward-active gain (β_f) dependence on collector current, limited active base profile optimization and large device geometries associated with these technologies, efforts continued to achieve better bipolar characteristics.

These approaches to BiCMOS technology are oriented to fabricating bipolar transistors in CMOS LSI's without drastically changing the CMOS processes they are based upon. [3] [15] [16] [17] [18] By using the *n*-MOS threshold adjust step as the bipolar base implant, Momose .et.al [15] and Miyamoto .et.al[16] developed technologies which do not require any additional processing or mask steps to fabricate the bipolar transistor. Zeitzoff .et.al [18] uses the p^+ source and drain implant to act as the base dopant, again manufacturing a bipolar transistor with the addition of no extra processing steps. Yue .et.al [17] and Reich .et.al [3] used an active-base photomask to mask the active area of the *npn* transistor. While adding additional steps to the process, this enhancement allows adjustment of the bipolar transistor parameters independently from the CMOS parameters.

In order to improve MOS LSI drive ability and speed, CMOS LSI's began adopting these bipolar transistors in special circuits such as output drivers and sense amplifiers. Having bipolar transistors with wide base widths and large collector resistance restrains the performance with respect to maximum collector current and cut-off frequency and is poor in comparison with that of bipolar LSIs. As a result, circuit performance itself had not shown remarkable improvement.[19]

With performance of earlier BiCMOS being dominated by the individual characteristics of bipolar drivers and CMOS logic circuits, its applications had been limited to specific fields. High performance BiCMOS opens new fields by placing bipolar and CMOS devices on the same chip in an uncompromised form and combining them in unit circuits rather than limited to separate areas of the chip.

High performance BiCMOS technologies were introduced as CMOS processes moved below 2.0μm design rules. Epitaxial structures were generally adopted and the addition of a buried layer to the BiCMOS process was introduced by Walczyk .et.al [20] and Momose .et.al. [6] This was immediately followed by integrating these features with the twin-well CMOS process by Kobayashi .et.al.[21] Watanabe .et.al [22] and Ikeda .et.al [23] further extended the bipolar transistor optimization with the addition of polysilicon emitters.

To increase the operating speed and high integration even further, scaling down of the BiCMOS devices into the submicron range is desirable. Based on a 0.8μm twin-well CMOS processes, the first submicron BiCMOS processes were introduced in December, 1987 by Iwai .et.al [24] and Havemann .et.al [7] In the first technology, an ion-implanted emitter was chosen to minimize the production cost and limit the additional mask count to three.[24] By optimizing the bipolar transistor, sufficiently high performance for BiCMOS gates was obtained. The second process requires an extra mask count of four but has a polysilicon emitter for improved bipolar performance.

There was some concern that in scaling further down to half-micron dimensions, BiCMOS could loose its advantage of higher driving capability relative to CMOS. In a study by Momose .et.al, [25] a scaled 0.5μm BiCMOS was fabricated with electron beam lithography. It generally follows the trend of earlier processes with three additional mask steps and ion implantation for the n^+ buried layer, collector contact and active base regions. The feasibilities and capabilities of the process were evaluated in terms of device characteristics and

propagation delay time of ring oscillators. This data indicates BiCMOS is still effective at a half micron technology. With a load of 1.0pf they found the BiCMOS delay time to be 66% of that of pure CMOS.

Although BiCMOS has evolved into the sub-micron range, processes based on the evolution of a CMOS process generally produce bipolar devices that are greatly inferior to the state of the art super self-aligned bipolar device. Chiu .et.al [26] describe a non-overlapping super self-aligned structure that is optimal for both MOS and bipolar. Their approach realizes high speed by minimizing parasitic capacitances and resistance. Source/drain and emitter/extrinsic base junctions are formed and contacted by doped polysilicon, thin epi grown on arsenic buried layer and a fully recessed oxide isolation scheme are additional features of the technology.

1.3 Purpose Of The Work

There has been a demonstrated commitment to BiCMOS technologies observed in the literature. The advantages to having bipolar and CMOS transistors on the same integrated circuit chip have been noted.

A process merging a *npn* vertical transistor with the Twin Tub CMOS III technology will be described. Several minimum size bipolar transistor designs were developed, fabricated and used as a basis for a complete test chip. After the initial simulations and studies, experiments were performed to characterize and optimize the base parameters. A problem encountered with the performance of the bipolar transistor will be discussed.

The work presented in this thesis documents the development effort and process optimization performed to integrate a functional *npn* device into the Twin Tub III CMOS process.

2. THEORY AND MODELING OF THE BIPOLAR TRANSISTOR

2.1 Uniformly Doped Transistor

Figure 1 [27] is a simple one dimensional realization of a structure showing the action of an *npn* bipolar transistor.

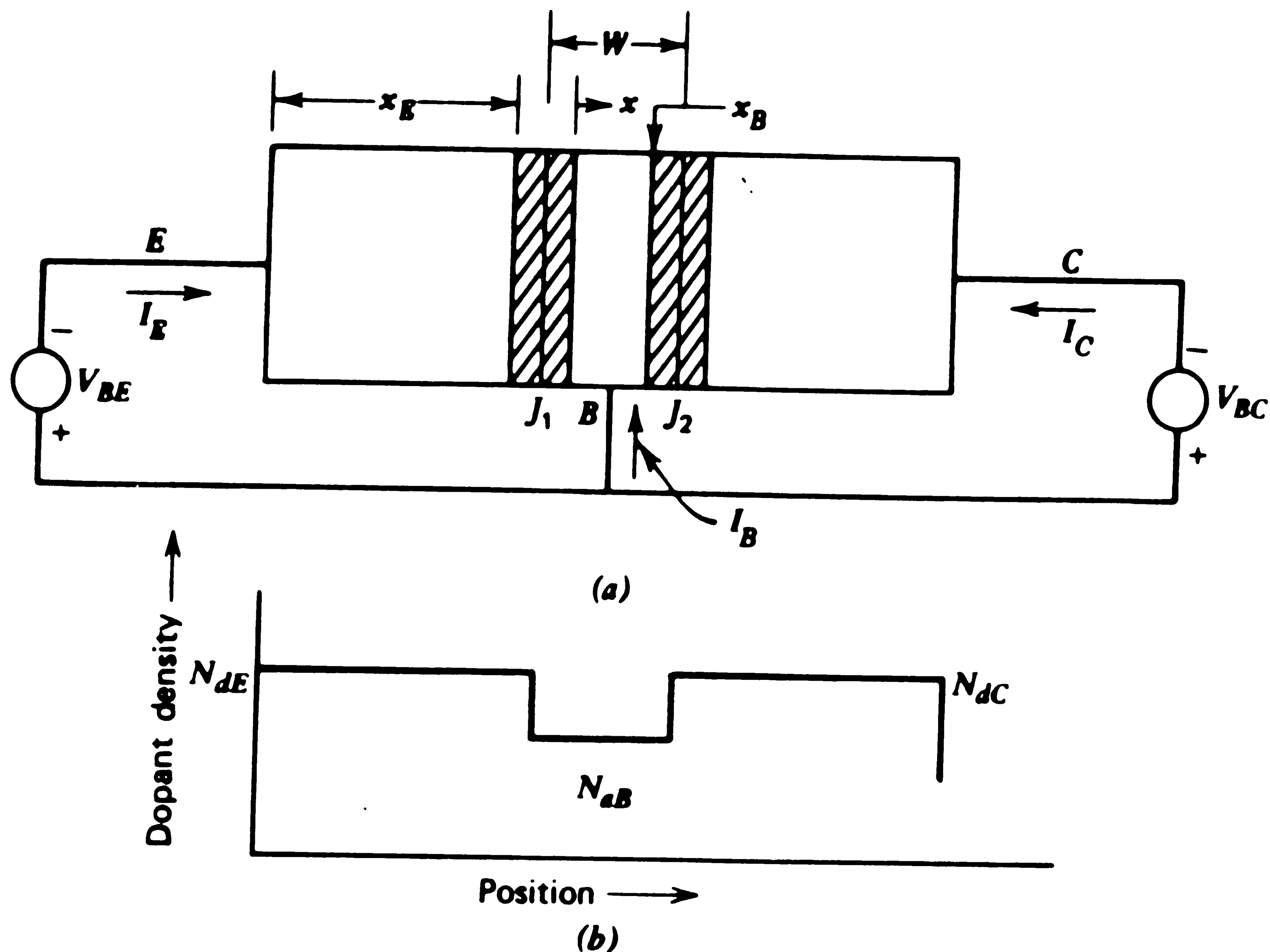


Figure 1. (a) A diagram of a bipolar transistor showing two *pn* junctions spaced W units apart (b) Doping density versus longitudinal position for the bipolar transistor above[27] "

A bar of semiconductor material with a cross-sectional area A is shown with two *pn* junctions spaced a distance W apart. W is small enough so that electrons injected across Junction 1 (V_{BE} positive) are in the vicinity of Junction 2 and the loss of electrons by recombination in the middle base region is minimal. It is also assumed that electron recombination or generation in the base region is not significant and there is a negligible flow of holes (base majority carriers) between the junctions into the base. Defining the longitudinal dimension as x, the expression for hole current in the x direction (assuming no recombination) can be written

$$J_p = 0 = q\mu_p p E_x - qD_p \frac{dp}{dx} \quad (1)$$

Solving for the electric field E_x gives

$$E_x = \frac{D_p}{\mu_p} \frac{1}{p} \frac{dp}{dx} \quad (2)$$

by using the Einstein relationship

$$D_p = \left(\frac{kT}{q} \right) \mu_p \quad (3)$$

it can be written in the form

$$E_x = \frac{kT}{q} \frac{1}{p} \frac{dp}{dx} \quad (4)$$

This the built-in electric field from free carriers and fixed impurities.

The electron current is written

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \quad (5)$$

From the earlier calculations of base current there is an expression for the electric field

$$E_x = \frac{D_p}{\mu_p} \frac{1}{p} \frac{dp}{dx} \quad (6)$$

Substituting for E_x in equation 5 then gives

$$J_n = kT\mu_n \frac{n}{p} \frac{dp}{dx} + qD_n \frac{dn}{dx} \quad (7)$$

By using the Einstein relationship the following expression for the current density is obtained.

$$J_n = \frac{qD_n}{p}\left[n\frac{dp}{dx} + p\frac{dn}{dx}\right] \qquad (8)$$

This can be expressed as

$$J_n = \frac{qD_n}{p}\frac{d(pn)}{dx} \qquad (9)$$

An integral form of the above equation is written with arbitrary limits x and x' and recombination treated as negligible so that J_n can be removed from the integral.

$$J_n\int_x^{x'}\frac{p}{q}\frac{dx}{D_n} = \int_x^{x'}\frac{d(pn)}{dx}\,dx \qquad (10)$$

Since the right-hand side of the above equation is a perfect differential this can be written

$$J_n\int_x^{x'}\frac{p}{q}\frac{dx}{D_n} = p(x')n(x') - p(x)n(x) \qquad (11)$$

Using the junctions as boundaries of the regions then $x = 0$ becomes the lower limit and $x' = x_B$ the upper limit of the integrals. The carrier densities at either side of a biased *pn* junction are dependent upon the applied voltage according to the relationship

$$pn = n_i^2 e^{\frac{qV_a}{kT}} \qquad (12)$$

where V_a is the applied voltage. From this equation the *pn* products at the boundaries can then be related to the junction voltages.

$$p(0)n(0) = n_i^2 e^{\frac{qV_{BE}}{kT}}$$

$$p(x_B)n(x_B) = n_i^2 e^{\frac{qV_{BC}}{kT}} \qquad (13)$$

Thus the electron current in the base can be expressed as a function of the junction voltages V_{BE} and V_{BC}.

$$J_n \int_0^{x_B} \frac{p}{q} \frac{dx}{D_n} = n_i^2 \left(e^{\frac{qV_{BC}}{kT}} - e^{\frac{qV_{BE}}{kT}} \right) \tag{14}$$

Rearranging terms, the following expression for electron current density is obtained.

$$J_n = \frac{qn_i^2 \left(e^{\frac{qV_{BC}}{kT}} - e^{\frac{qV_{BE}}{kT}} \right)}{\int_0^{x_B} \frac{p}{D_n} dx} \tag{15}$$

D_n is frequently a weak function of position in the base and can be expressed as an average value $\tilde{D}_n$ and removed from the integral in the denominator of the right-hand side of the last equation. With D_n removed, the integral expresses the total majority-carrier charge in the base. Multiplying by qA will convert this density into the total majority carrier charge in the base. We now define the majority carrier charge in the base as Q_{B0}.

$$Q_{B0} = qA \int_0^{x_B} p dx \tag{16}$$

The electron current flowing from the first to the second junction can be expressed as

$$I_n = I_S \left(e^{\frac{qV_{BC}}{kT}} - e^{\frac{qV_{BE}}{kT}} \right) \tag{17}$$

where

$$I_S = \frac{q^2 A^2 n_i^2 \tilde{D}_n}{Q_{B0}} \tag{18}$$

From equation 17 the relationship between the junction voltages and current is clearly seen.

The condition V_{BE} positive and V_{BC} zero or negative is known as forward-active bias for an *npn* transistor. This bias results in electron injection at the emitter-base junction and electron collection at the base-collector junction. With V_{BC} negative and $V_{BE} \gg kT/q$ it is seen from equation 17 that an electron current of

$$I_n \approx -I_S\, e^{\frac{qV_{BE}}{kT}} \tag{19}$$

will flow from left to right across the collecting junction J_2 of figure 1. Equation 19 shows that under forward-active bias conditions, collector current is exponentially related to emitter-base voltage. Experimentally, this relationship is found to hold over many decades of collector current. Figure 2 [27] shows a logarithmic plot of the collector current I_C as a function of the base-emitter bias V_{BE}. The intercept of an extrapolated line drawn through the collector current measurements with the current axis at $V_{BE} = 0$ yields a value for I_S in equation 19. Once I_S is known, the built-in base charge in the quasi-neutral region can be obtained from equation 18 since all the other parameters are known.

Q_{B0} represents the total hole charge in the quasi-neutral base as the base-emitter bias tends to zero and is given by

$$Q_{B0} = \frac{q^2 A^2 n_i^{\,2} \tilde{D}_n}{I_S} \tag{20}$$

This charge is built in during processing of the transistor.

Determining a value of Q_{B0} through current-voltage measurements on the transistor was first described by H. K. Gummel[28]. The number of base dopant atoms (per cm^2) in the quasi-neutral region given by

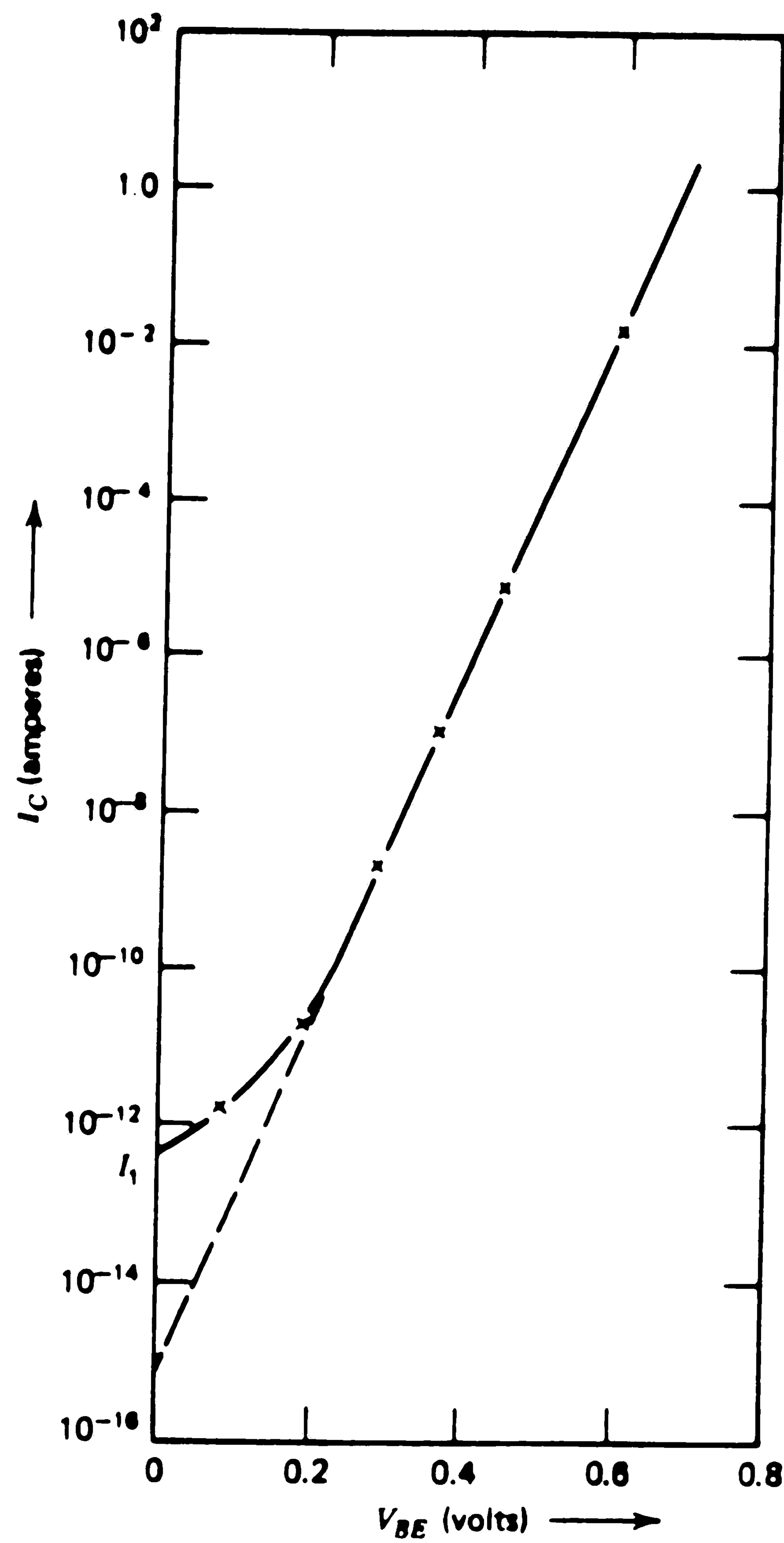


Figure 2. Semilogarithmic plot of collector current versus base-emitter voltage for a forward-active biased *npn* transistor [27]

$$\int_0^{x_B} N_a(x)dx = \frac{Q_{B0}}{qA} = \frac{qAn_i^2\bar{D}_n}{I_S} \tag{21}$$

is often referred to as the *Gummel* number. Equation 21 shows that I_S, the multiplying factor for transistor current at a given bias, is inversely proportional to the Gummel number, or total base doping. The lower the total base doping, the higher is the current at a given bias. Control of Q_{B0} during processing is of primary concern in obtaining reproducible transistor characteristics.

2.2 *Recombination Theory*

Recombination in the base-emitter space-charge region can account for added base-emitter current observed at low biases. The equations describing generation and recombination in the space-charge zone through localized states or recombination centers were originally described by Shockley and Reed [29] and by Hall [30]. The process is referred to frequently as Shockly, Read, Hall (SRH) recombination. From their analysis, an equation describing the recombination current J_r can be written

$$J_r \approx \frac{q x' n_i}{2\tau_0} e^{\frac{qV_a}{2kT}} \tag{22}$$

where $\tau_0 = 1 / N_t \sigma v_{th}$, the distance x' is a portion of the space-charge region thickness x_d and V_a is an applied bias. τ_0 is the lifetime associated with the recombination of excess carriers in a region with a density N_t of recombination centers. From this equation it is seen that the current arising from recombination in the space-charge region varies with applied voltage as $e^{\frac{qV_a}{2kT}}$. Assuming x' is a weak function of voltage, it can be approximated by the entire space-charge region width x_d. With this approximation, the ratio between the ideal diode current J_t

$$J_t = qn_i^2 \left(\frac{D_p}{N_d L_p} + \frac{D_n}{N_a L_n} \right) \left(e^{\frac{qV_a}{kT}} - 1 \right) = J_0 \left(e^{\frac{qV_a}{kT}} - 1 \right) \tag{23}$$

and the space-charge zone recombination-current J_r under forward bias is given by

$$\frac{J_t}{J_r} = \frac{2n_i}{x_d} \left(\frac{L_n}{N_a} + \frac{L_p}{N_d} \right) e^{\frac{qV_a}{2kT}} \tag{24}$$

where $L_p = \sqrt{D_p \tau_p}$ is the diffusion length of a hole in a *n*-type region and L_n is the diffusion length of an electron in a *p*-type region. From the above relationship it is apparent that J_r is less significant relative to the ideal diode current as bias increases. Also, the more defect-free

the material, the longer the diffusion lengths and the more dominant is J_t over J_r.

A semilogarithmic plot of I_C and I_B as a function of the base-emitter voltage illustrates this behavior. Typical data for an *npn* transistor is given in figure 3 [27].

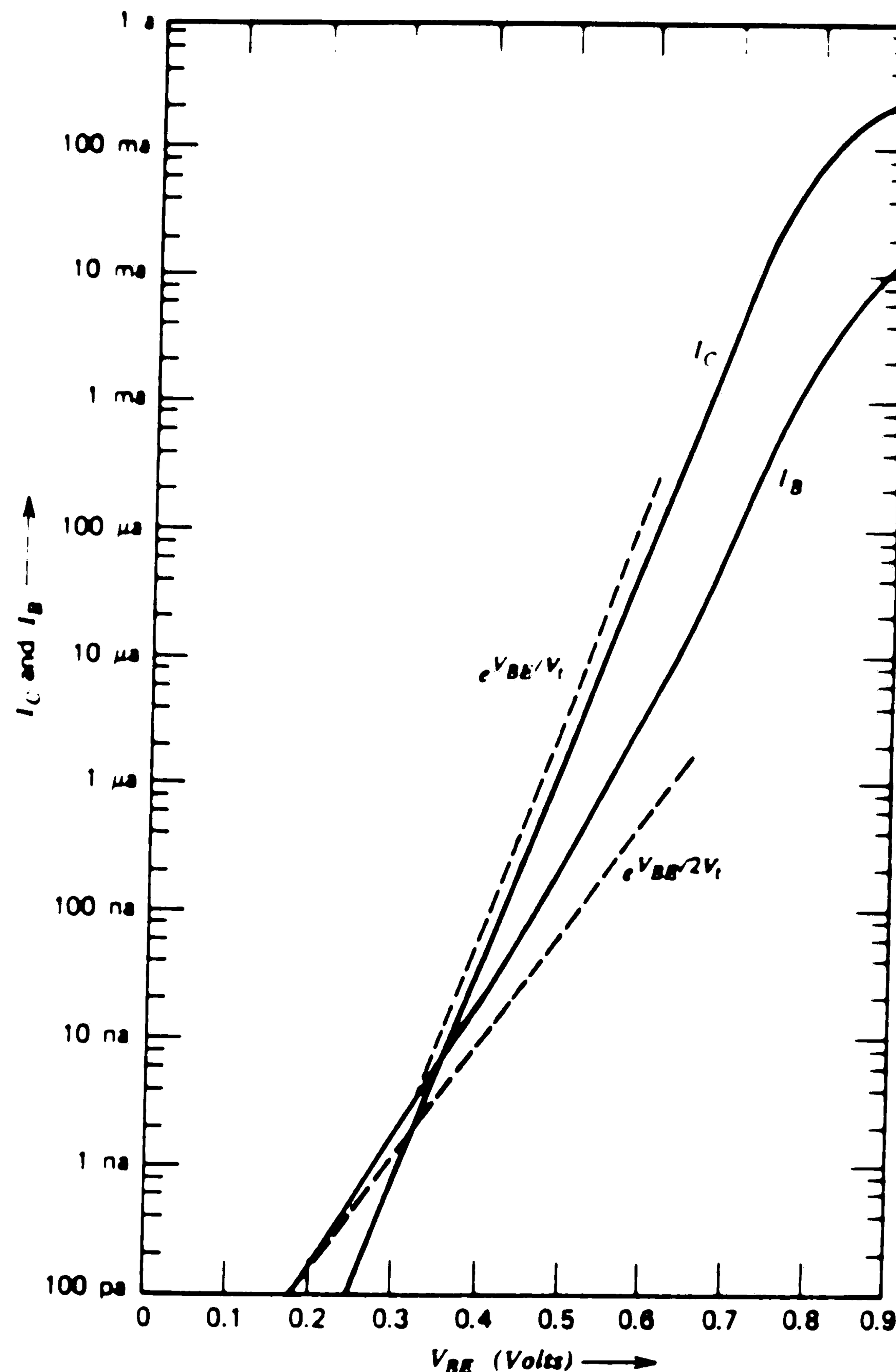


Figure 3. Measured collector and base currents plotted as a function of base-emitter voltage [27]

The excellent fit of the data to straight lines over the mid-range of currents is consistent with the exponential nature of the equations describing the current-voltage dependence. It can be seen that the collector current is "ideal" over a wider range than the base current. At low base-emitter voltage there is a change in the slope of the straight line variation of log I_B with V_{BE}. The experimental data fits a curve that is represented by

$$I_B = I_0 \, e^{\frac{qV_{BE}}{nkT}} \tag{25}$$

as V_{BE} goes to zero. The parameter n is generally found to be between one and two and I_0 is larger than is the corresponding multiplier for an exponential form fitting the data at intermediate bias values. The equation for recombination current in the space-charge region derived from Shockley-Read-Hall theory has the same voltage dependence if n is equal to 2. Values for n between 1 and 2 would be indicative of variations of parameters affecting recombination within the space-charge region.

The loss of carriers to recombination in the base is measured by the base transport factor α_T

$$\alpha_T = \frac{I_{ne} - I_{rb}}{I_{ne}} = 1 - \frac{I_{rb}}{I_{ne}} \tag{26}$$

where I_{rb} is the recombination current in the base and I_{ne} is the electron current injected from the emitter. For a uniformly doped base

$$\alpha_T = 1 - \frac{x_B^2}{2D_n\tau_n} = 1 - \frac{x_B^2}{2{L_n}^2} \tag{27}$$

2.3 Emitter Efficiency

The effectiveness of an emitter junction in injecting electrons into the base is measured by the emitter efficiency γ

$$\gamma = \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{1}{1 + \frac{I_{pE}}{I_{nE}}} \tag{28}$$

With $I_{nE} + I_{pE}$ being the total emitter current, the electron current crossing the emitter-base

junction (I_{nE}) is γI_B. For the simple prototype transistor with constant doping

$$\gamma = \frac{1}{1 + \dfrac{x_B N_{aB} D_{pE}}{x_E N_{dE} D_{nB}}} \tag{29}$$

where x_E is the emitter region width, x_B the base quasi-neutral width, N_{dE} the average emitter doping, N_{aB} the average base doping, D_{pE} the diffusion constant of holes in the emitter and D_{nB} the diffusion constant for electrons in the base. Values for this number are typically very close to unity.

2.4 Forward-Active Current Gain

The ratio of the collector current I_C to the emitter current I_E is given by the symbol α_F. α_F is the product of the emitter efficiency γ and the base transport factor α_T. By Kirchoff's current laws, all the currents into the transistor must sum to zero such that

$$I_B + I_E + I_C = 0 \tag{30}$$

$$I_B - \frac{I_C}{\alpha_F} + I_C = 0 \tag{31}$$

and

$$I_C = \frac{\alpha_F I_B}{1 - \alpha_F} = \beta_F I_B \tag{32}$$

where $\beta_F \equiv I_C / I_B$ is the forward active current gain. Since α_F is very nearly unity, β_F is very large. Small changes in α_F caused by process variations in fabricating the transistor are magnified to large changes in β_F.

To the extent that γ and α_T depart from unity represents a hole current that must be supplied from the base contact. For transistors with base widths much less than the diffusion length, α_T has a value very close to unity and the current gain is given almost entirely by the emitter efficiency. With $\alpha_T = 1$

$$\beta = \frac{\gamma}{1-\gamma} \approx \frac{N_E}{N_B} W = \frac{N_E}{\frac{Q_{B0}}{qA}} \tag{33}$$

where N_E and N_B is the emitter and base doping respectively and Q_{B0} is the Gummel number defined earlier. Therefore, for a given emitter doping, the common-emitter current gain is inversely proportional to Q_{B0}. Figure 4 shows this relationship for ion implanted transistors having the same emitter doping.

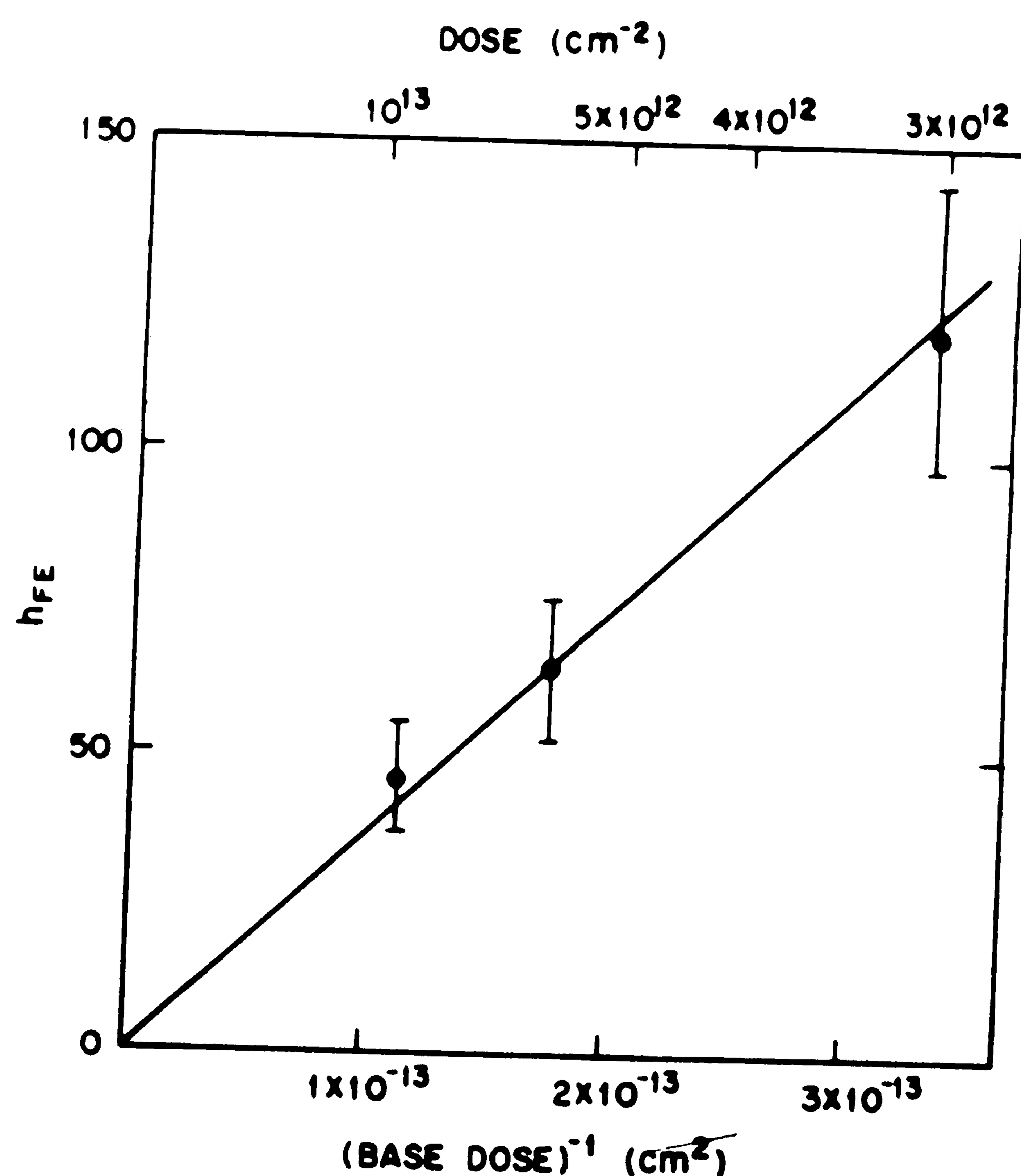


Figure 4. Common-emitter current gain versus the inverse of the base implant dose for all implanted transistors [31]

The base dose is directly proportional to the Gummel number Q_B and it is seen that as the dose decreases the β increases. In equation 33 there is another dominant factor in addition to the Gummel number, the emitter doping concentration N_E. To improve the gain (h_{FE} or β), the emitter should be much more heavily doped than the base, that is $N_E / N_B \gg 1$.

The importance of the recombination component relative to the injection components into the quasi-neutral base region increases as voltage is reduced. Recombination current in the space charge region flows only in the base-emitter leads. Collector current, consisting of collected electrons injected from the base-emitter junction is unaffected. Thus, at low biases the collector current is a smaller fraction of emitter current than it is in the intermediate bias range.

A plot of I_C / I_B (or β_f) shows this behavior clearly (figure 5).

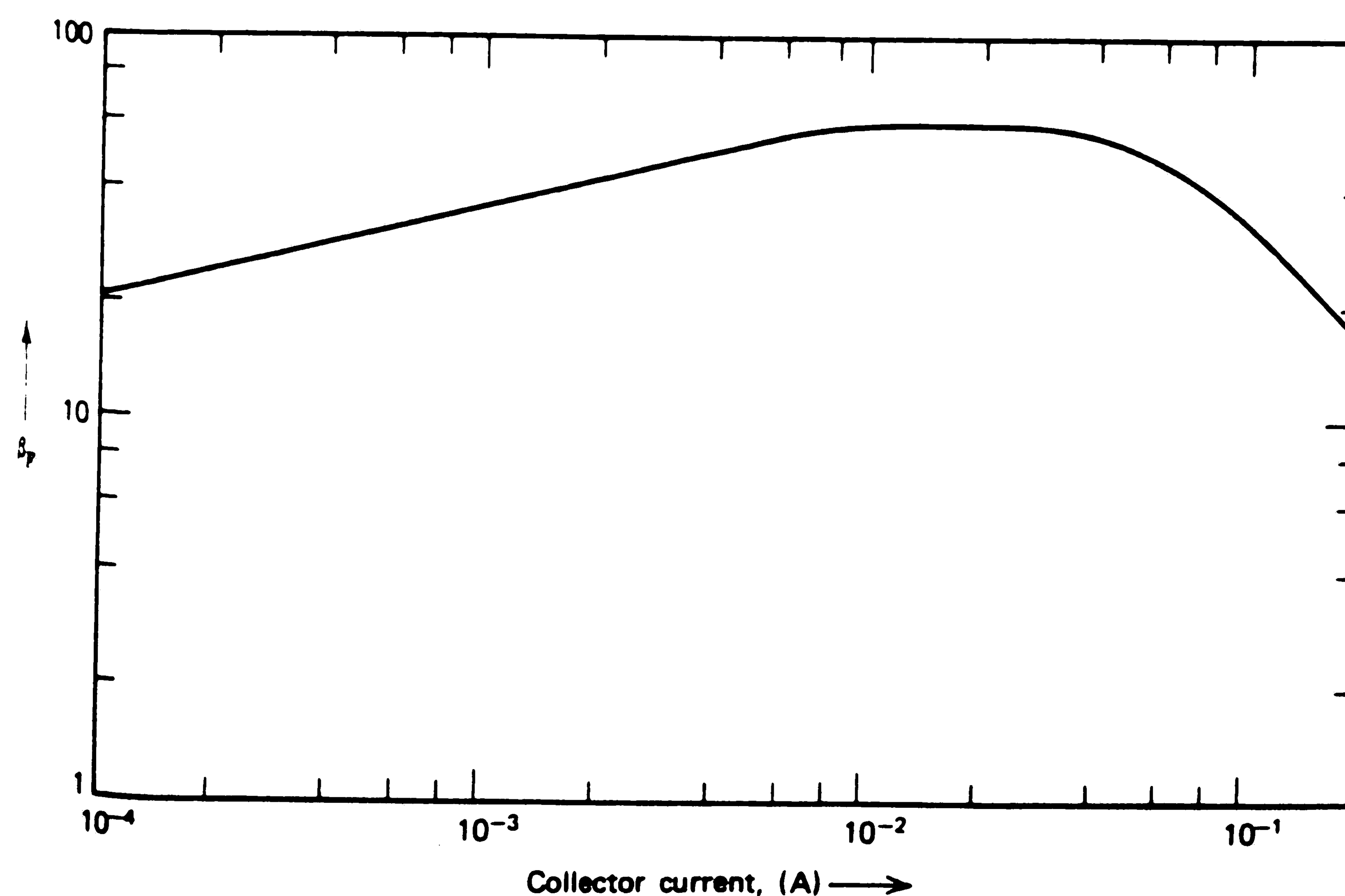


Figure 5. Forward active current gain (β_F) as a function of collector current [27]

The decrease in β as V_{BE} decreases represents a limitation to many circuit applications of the transistor. To improve the current characteristic in the low-current region, the trap densities in the depletion region and at the semiconductor surface must be reduced. During manufacture it is important to try and maintain as high a lifetime as possible within the base-emitter space charge region. At low collector current levels, the contribution of the recombination current in the emitter depletion region and the surface leakage current may be large compared with the diffusion of minority carriers across the bases making the efficiency low. By minimizing the bulk and surface traps, β can be improved at low current levels. As the base current reaches the "ideal" region β increases to a high plateau. At higher collector currents the injected minority-carrier density in the base approaches the majority-carrier density there (high level injection condition) and the injected carriers effectively increase the base doping, which, in turn, causes the emitter efficiency to decrease.

2.5 Graded Base Transistor

In the previous analysis of current gain, it was assumed that the impurity concentration in the base region was uniform. We will now consider, a *npn* junction transistor model having a step emitter junction and a graded base layer given by the impurity distribution $N_{(x)}$. This is a general impurity distribution where N_B denotes the impurity concentration at the base side of the emitter junction decreasing to zero at $x=W$, the base / collector junction. With the carrier concentration in the base being non-uniform, the energy bands will bend in accordance with the grading $N_{(x)}$. In the constant doped base model, the electrostatic potential Ψ is constant within the base region, so that the term $d\Psi / dx$, which is the electric field, is zero in the base region. For the graded base the potential Ψ is higher at the emitter than at the collector. Therefore, $d\Psi / dx$ has a finite value indicating the existence of an electric field within the base region. This is a built-in field arising to prevent the majority carriers from diffusing because of their

concentration gradient $dN_{(x)} / dx$. This field, which keeps holes in their place, is in a direction to aid the transport of injected electrons. Thus, for the condition of low level injection, the electrons will move both by diffusion and drift.

From equation 11 we can express the base doping, N as a function of x and inserting the boundary conditions that $p = 0$ at x = W, the collector, the following expression is obtained for the injected electron concentration

$$n = \frac{J_n}{qD_n} \frac{1}{N_{(x)}} \int_x^W P_{(x)} dx \tag{34}$$

The result gives the electron concentration as a function of distance in the base layer. If this equation is evaluated at $x = 0$ where $N_{(x)} = N_B$ then we obtain the injected electron concentration

$$n = \frac{J_n}{qD_n} \frac{1}{N_B} \int_0^W P_{(x)} dx \tag{35}$$

Using the quasi-Fermi-level argument

$$n = n_{pb} e^{\frac{qV_{EB}}{kT}} = \frac{n_i^2}{N_B} e^{\frac{qV_{EB}}{kT}} \tag{36}$$

with n_{pb} being the equilibrium electron concentration in the *p*-type base region. Setting the last two equations equal to each other, J_n becomes

$$J_n = \frac{qD_n n_i^2 e^{\frac{qV_{EB}}{kT}}}{\int_0^W N_{(x)} dx} \tag{37}$$

The emitter efficiency γ, can be expressed as

$$\gamma = \frac{1}{1 + \frac{J_p}{J_n}} \qquad (38)$$

For a uniform emitter with impurity concentration N_E, the hole current density can be expressed as

$$J_p = \frac{qD_p p_{ne}}{L_{pe}} e^{\frac{qV_{BE}}{kT}} = \frac{qD_p n_i^2}{L_{pe} N_E} e^{\frac{qV_{BE}}{kT}} \qquad (39)$$

where P_{ne} equals the hole concentration in the *n*-type emitter and L_{pe} is the hole diffusion length in the emitter. Substituting the expressions for J_n and J_p into γ we obtain

$$\gamma = \frac{1}{1 + \frac{D_p}{D_n} \frac{1}{L_{pe} N_E} \int_0^W N_{(x)} dx} \qquad (40)$$

replacing the ratio D_p / D_n with μ_p / μ_n and multiplying the integral expression by q / q gives

$$\gamma = \frac{1}{1 + \frac{q\mu_{pE} \int_0^W N_{(x)} dx}{q\mu_{nB} N_E L_{nE}}} \qquad (41)$$

This equation can be written in the form

$$\gamma = \frac{1}{1 + \frac{R_{EE}}{R_{BB}}} \qquad (42)$$

where

$$R_{EE} = \frac{1}{q\mu_{nb} N_E L_{ne}} = \frac{\rho_E}{L_{ne}}$$

$$R_{BB} = \frac{1}{q\mu_{pe}\int_0^W N(x)dx} = \frac{\rho_{B(x)}}{W}$$

The terms R_{EE} and R_{BB} are referred to as sheet resistances and defined as the ohmic resistances as measured from edge to edge of a square sheet of material of a certain thickness x. Thus, R_{EE} is the sheet resistance of the emitter having a uniform resistivity ρ_E and a thickness equal to L_{nE}. R_{BB} is the sheet resistance of a base having a graded resistivity $\rho_{B(x)}$ and a thickness W. For the uniform doped base, $R_{BB} = \rho_B / W$, and equation 42 reduces to equation 29.

R_{BB} increases as a result of a graded impurity distribution, thus, the emitter efficiency is increased when the base region is graded. Regardless of the base impurity distribution, it is still required that the emitter doping be as heavy as possible for high emitter efficiency so that the sheet-resistance ratio R_{EE} / R_{BB} remains small.

From equation 33, the forward-active current gain, β is related to emitter efficiency γ by

$$\beta = \frac{\gamma}{1 - \gamma}$$

Substituting equation 42 for γ yields

$$\beta = \frac{\gamma}{1 - \gamma} = \frac{R_{BB}}{R_{EE}} \tag{43}$$

for the graded base transistor. Since integrated circuit processing involves diffused structures, it should be the equations derived for the graded base transistor that better describe the manufactured devices.

3. EXPERIMENTS

3.1 CMOS FABRICATION

The core process used for BiCMOS development is the third generation Twin-Tub CMOS Technology.[32] [33] [34] The two tub approach is used with a lightly doped epitaxial substrate to suppress latch-up and enable separate optimization of the *n*- and *p*-channel transistors. Although a *p*-epi over p^+-substrate is used, the technology is compatible with *n*-epi substrates since the active doping levels are established by implantation. The 5.0 volt transistor structures use a nominal 250 Å gate oxide, tantalum silicide over *n*-poly gate and 1.3μm nominal channel lengths. The threshold voltages of the *n*- and *p*-channel device are 0.70V and -1.10V.

The critical dimensions of this 1.75μm design rule technology are outlined in table 1.

Critical Dimensions (μm)		
	Line	Space
Active	1.5	2.5
Polycide	1.75	1.75
Gates	2.25	
Windows	1.75	
Metal	1.75	1.75

TABLE 1. Critical dimensions of the Twin-Tub III CMOS technology

Photolithography is accomplished with 5x direct step on wafer (DSW) printing and all levels are reactive sputter etched. There are eight mask levels in the Twin-Tub III technology. The digital CMOS process sequence is now discussed along with a cross-sectional development of CMOS transistors.

A self-aligned process is used to form the two tubs. An oxide-nitride sandwich is deposited and etched (figure 6). The exposed silicon is implanted with phosphorus and

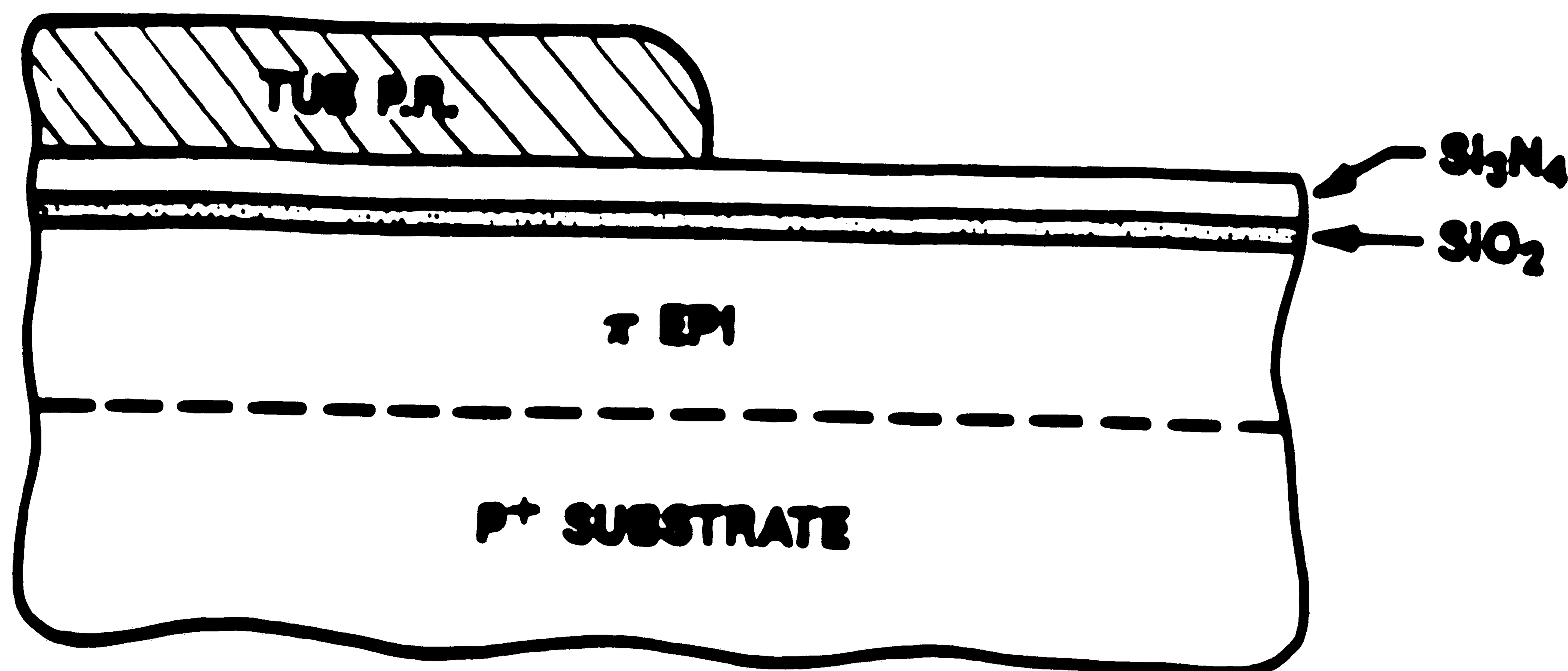


Figure 6. Mask 1: *n*-tub formation

selectively oxidized to form the *n*-tub. The masking nitride is now removed and the *p*-tub is implanted, self-aligned to the oxide masked *n*-tub. Both tubs are driven to a depth of 4-5 μm. A second oxide-nitride sandwich is deposited and etched (figure 7) to define the active gate regions. A blanket boron implant is performed followed by a masked phosphorus implant (figure 8) to achieve self-aligned channel stops. Device isolation is completed with a LOCOS field oxidation. The masking oxide-nitride layer is removed and a sacrificial oxide is grown. A non-selective boron implant is performed to define the threshold voltages of both the *n*- and *p*-channel transistors. After removal of this oxide, a 250 Å gate oxide is grown, polysilicon deposited and doped with phosphorus. A composite layer of $TaSi_2$ over n^+-polysilicon is created to give a gate sheet resistance of 2.5 Ω/□. The composite structure is etched with an anisotropic reactive sputter technique (figure 9).

A selective arsenic/phosphorus implant is used for the doping of n^+-source and drain areas to obtain a graded junction (figure 10). In order to save another mask step, a blanket BF_2

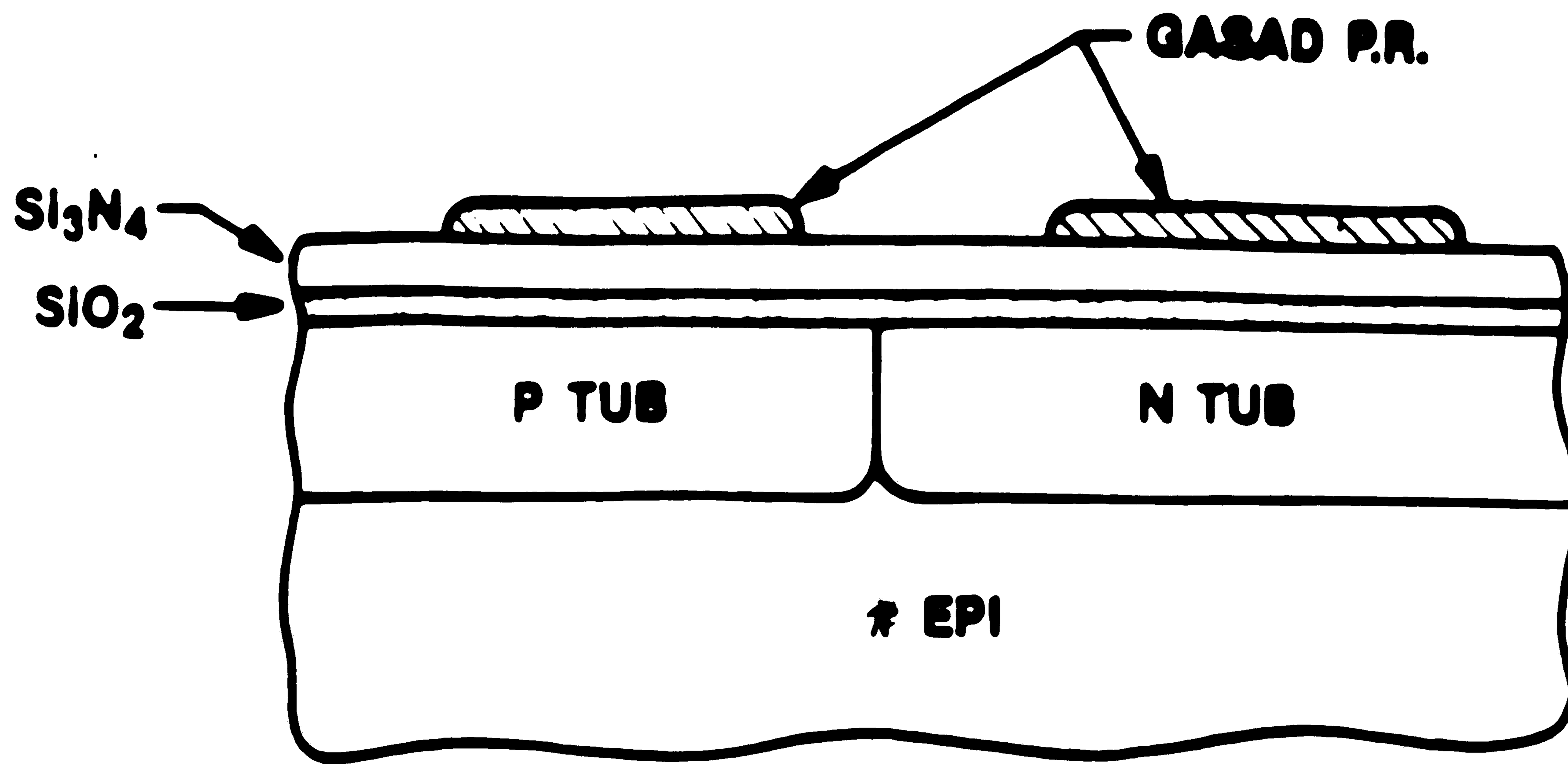


Figure 7. Mask 2: Active gate region definition

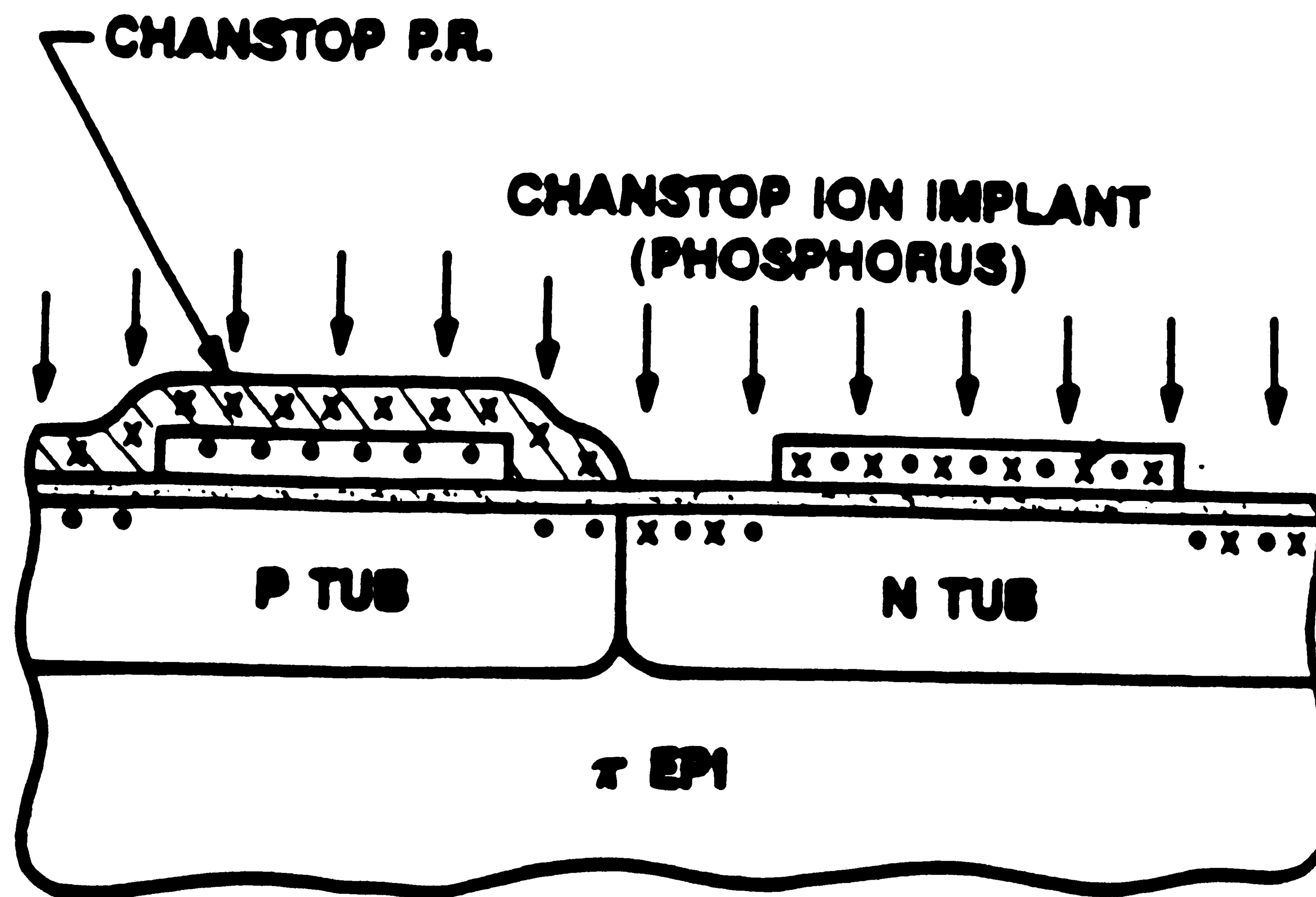


Figure 8. Mask 3: Phosphorus channel-stop implant

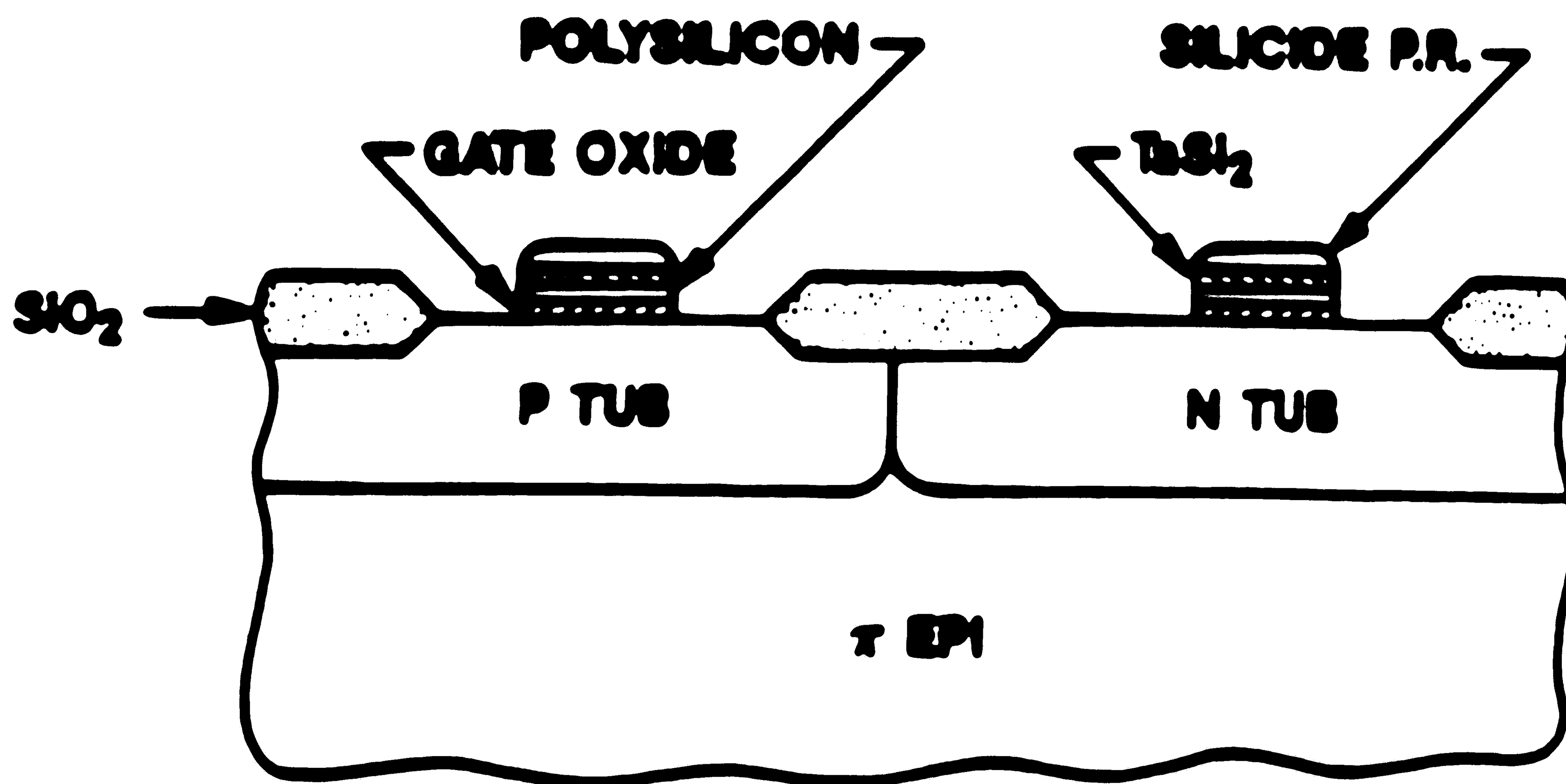


Figure 9. Mask 4: Gate definition

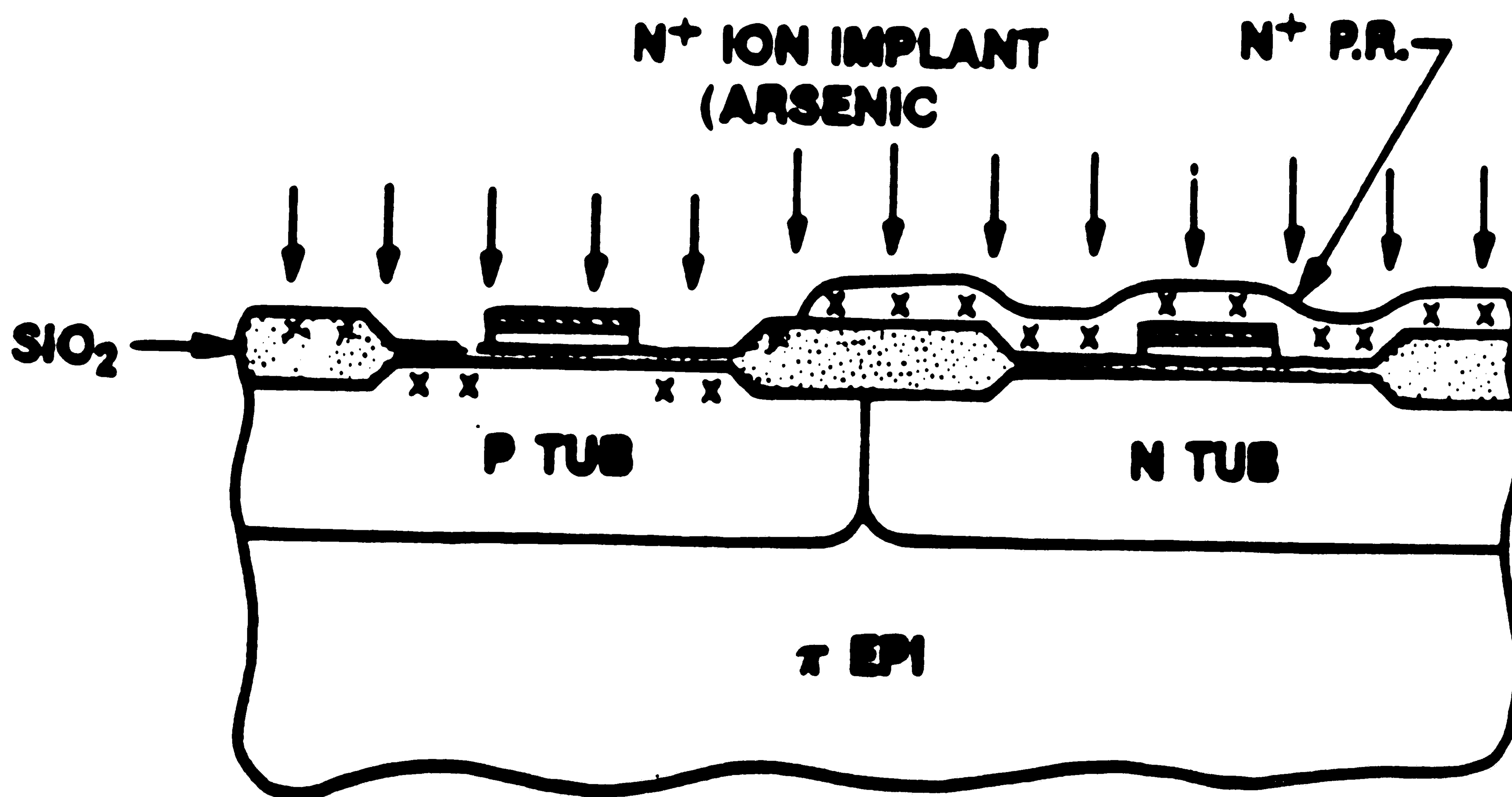


Figure 10. Mask 5: *n*-channel source/drain formation

implant is performed.

In order to achieve glass flow under the temperature restrictions of the process a Boro-Phospho-Silica Glass (BPSG) is used as the interlevel dielectric. Contact windows are formed (figure 11), the metal layer applied and patterned (figure 12)

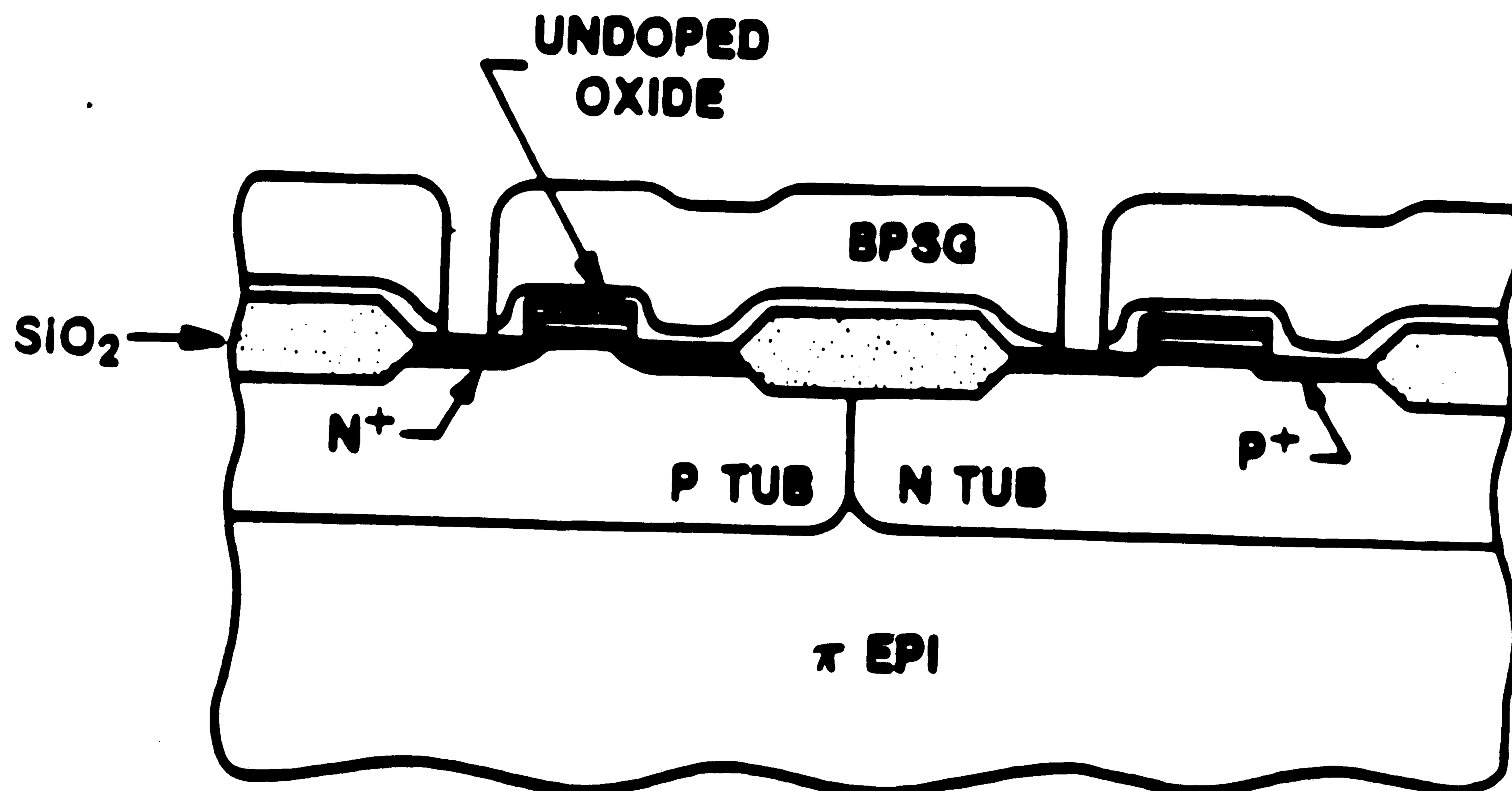


Figure 11. Mask 6: Contact window formation

and a final SINCAPS passivation layer applied and patterned (figure 13).

Table 2 lists some of the key parameters of the technology.

The border of the tubs is a critical region. A design rule for n^+-diffusion to p-tub edge has been established to account for the out-diffusion of the p-dopant at the edge of the tub.

The p- and n-channel threshold voltages are sensitive to tub and threshold adjust dosages. With the threshold adjust counter doping the n-tub surface, the p-channel threshold voltage responds strongly to both the n-tub and threshold adjust implants. The n-channel threshold voltage is dominated by the adjust implant which essentially sets the surface concentration.

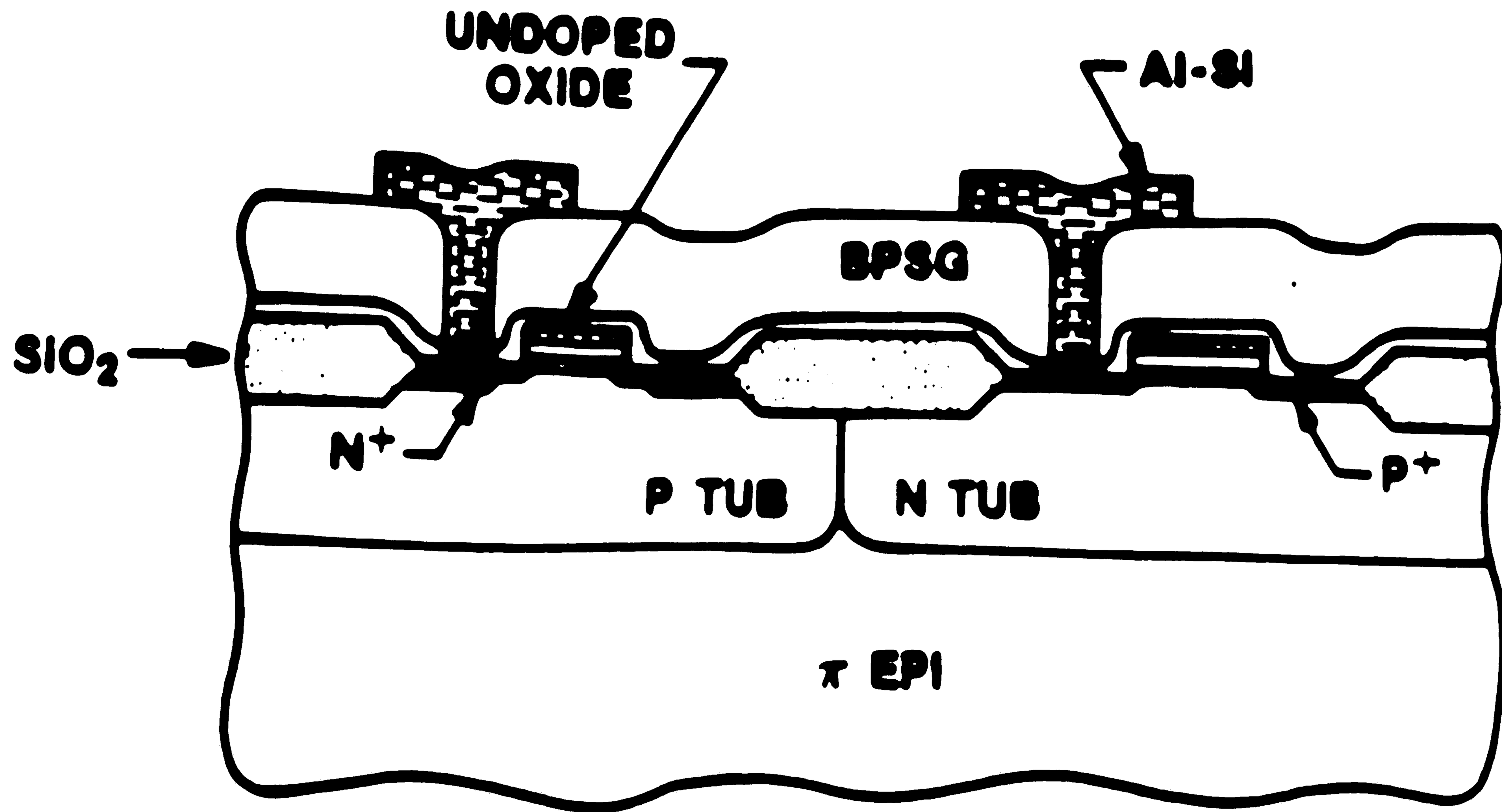


Figure 12. Mask 7: Metal interconnections formed

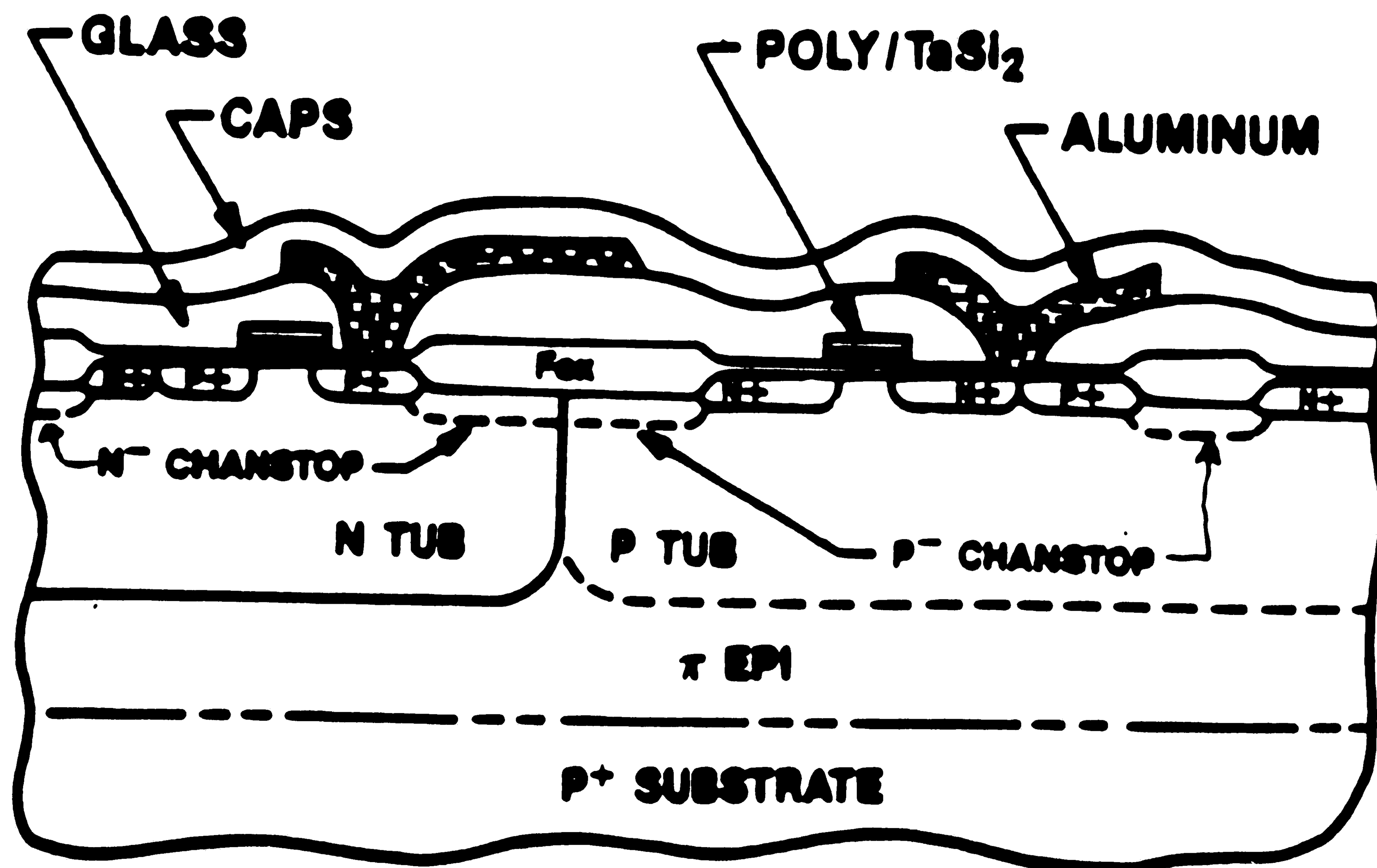


Figure 13. Mask 8: Encapsulation - completed device

Key Parameters	
Gate Oxide	
Nominal $L'_{n,p}$	1.3 μm
V_{tn}	0.7 V
V_{tp}	-1.0 V
B_n	75 $\mu A/V^2$
B_p	27 $\mu A/V^2$

TABLE 2. Key parameters of the Twin-Tub III CMOS technology

Hot carrier effects are suppressed by the grading of the n^+-junctions. The aluminum is doped with silicon to achieve non-spiking metalization.

3.2 Determination Of Base Parameters

The 1.75μm Twin-Tub III CMOS technology[34] was examined to study the feasibility of producing a moderate performance *npn* vertical bipolar transistor compatible with CMOS processing. The development charter specified that the CMOS parameters remain unchanged and the total process be cost effective. Following the general approach to integrating bipolar transistors with *n*-well CMOS first outlined by Hoefflinger .et.al,[14] the MOS *n*-tub is used as the collector, the n^+ implant as an emitter and the p^+-source and drain implant as the inactive base.

Momose .et.al[15] and Miyamoto .et.al[16] used the MOS threshold adjust step as the bipolar implant. At this point in the process the tubs have been set by the high temperature tub drive-in and the field oxide isolation, with its associated channel stop doping, is complete. With these deep diffusions now in place they will not be changed substantially by any additional bipolar processing. It is, thus, a very advantageous point in the process to insert the active base implant. Since, however, the CMOS characteristics must not be altered by the bipolar

process it was decided to also follow the approach of Yue .et.al[17] and Reich .et.al[3] in using a separate photomask for the bipolar base processing. While adding additional steps to the process, it provides the capability of adjusting bipolar transistor parameters independent of the CMOS parameters.

Table 3 describes the proposed flow of the BiCMOS process.

CMOS BASELINE FLOW	STEPS FOR BIPOLAR
p^+ Substrate	
p^- Epitaxial Layer	
n-Well With Self-aligned p-Well	(Collector)
Well Drive-in	
LOCOS/Chanstop Isolation	
Threshold Adjust Implant	
	Pattern Base
	Implant Base
	Drive-in Base
Gate Oxidation	
Gate Deposition/Definition	
Pattern/Implant n^+ Source/Drain	(Emitter)
Blanket Implant p^+ Source/Drain	
Deposit Interlevel Oxide	
Flow Interlevel Oxide/Drive-in Source/Drain	
Define Contact Windows	
Deposit/Define Metalization	

TABLE 3. Proposed flow of the Twin-Tub III BiCMOS technology

A few details of the process are worth noting. With the use of LOCOS field oxide and the associated Kooi effect[35], a 900Å sacrificial oxide is grown to obtain a quality surface for the subsequent MOS gate oxide. It is through this oxide that the non-selective boron CMOS threshold adjust dose is implanted. The boron base implantation is also carried out through

this oxide layer in order to avoid degradation of device performance by the formation of stacking faults during annealing.[36] To maximize the annealing of the implant damage in the base region, a dry nitrogen ambient was chosen for the base drive-in.[37]

With the p^+-substrate being heavily doped with boron, the p^--epitaxial layer is grown very thick (17μm) in order to insure there is no problem with out diffusion of boron from the substrate during the high temperature well (tub) drive-in. This does not allow the addition of a n^+-buried layer for increased bipolar performance. Since the CMOS parameters must remain unaffected by bipolar processing and the total BiCMOS process remain cost effective, a wholesale redesign of the well structures is not a development option. The collector will therefore, be wholly defined by the properties of the CMOS n-well. For these same reasons the properties of the emitter will be defined by the existing CMOS n-channel source and drain processing. The steps dealing with the base process are thus the only parameters available for bipolar transistor optimization. These parameters are the ion implant energy the ion implant dose and the thermal drive-in schedule.

An appropriate ion implant energy for the base was chosen by checking the projected range statistics into silicon dioxide.[38] The projected range for a 100 keV boron implant is 3104Å with a projected standard deviation of 710Å. This implant energy is adequate to penetrate the 900Å oxide screen. It is important to realize, however, that thickness variations in the sacrificial and final oxides will allow this implant energy to affect reproducibility. Since the base is implanted through the sacrificial oxide, its thickness influences how much of the boron goes through the oxide and into the silicon. With the subsequent growth of the final gate oxide, boron is removed from the silicon through segregation effects of the growing oxide. A variation in this oxide thickness will thus affect how much boron is lost from the silicon. Using a high base implant energy will put more of the boron deeper into the silicon, making both of these effects less important.

A base anneal / drive–in of 900°C for 60 minutes was chosen for the initial process. The ambient is inert dry nitrogen to maximize the annealing of the implant damage. This is a commonly used drive-in schedule already in place in the CMOS processes to anneal devices after implantation and was chosen for process commonality.

With the ion implant energy and drive-in schedule now specified, it is the ion implant dose that will be the variable to identify in obtaining the desired bipolar characteristics.

It has been shown that for a transistor with constant doping, the forward-active current gain, β, is approximately equal to N_E / Q_{B0} where N_E is the emitter doping and Q_{B0} is the total amount of charge in the base (Gummel number). Diffused transistors, however, will have a graded impurity profile. The gain, β, for graded base transistors is given by $\beta = R_{BB} / R_{EE}$ where R_{BB} and R_{EE} are the sheet resistances of the active base and emitter respectively. With the emitter doping defined by the CMOS process and thus held constant, the gain of the bipolar transistors is thus determined by R_{BB} which is defined by the base implant dose.

It should be noted, however, that in the calculations for the graded base device it has been assumed that the emitter / base junction is a step junction. In the Twin Tub III CMOS process the n^+-source / drain junction has been purposely graded, by way of a large dose phosphorus implant, to guard against hot carrier effects. The maximum impurity concentration in the base does not occur at the emitter / base metallurgical junction, but is shifted slightly towards the collector. There exists, therefore, an impurity gradient in the vicinity of the emitter junction which is opposite in slope to the aiding built-in field. This opposite impurity gradient establishes, in the base region close to the emitter junction, an electric field which is retarding the flow of injected minority carriers. This effect will lower the emitter efficiency, γ, as predicted by the graded base model.

AT&T Bell Laboratories has developed a computer program for the calculation of doping profiles of semiconductor devices called BICEPS.[39] By inputing information relating to the

oxidations, thermal drive-ins, implantations, depositions and etchings information relating to the resultant dopant concentration profiles are obtained. Since BICEPS calculates a net dose and sheet resistance for the metallurgical junctions, it provides a means to study various base implant and / or drive-in schedules and correlate them to device characteristics. The BICEPS calculation of particular interest is sheet resistance expressed in $\Omega/\square$ Given an indication of emitter, base and active base sheet resistance (base pinch sheet resistance) allows the experimental measurements on Van der Pauw test structures to be correlated with the theoretical and simulated results.

The sheet resistances calculated by the BICEPS simulation program do not, however, take into consideration any depletion layer effects. Values of active base sheet resistance would therefore be somewhat higher than that calculated. Also, the simulations are a development tool and are not absolute in predicting diffusion profiles. When trying to determine the active base dopant concentration, we are dealing with the net difference of several impurity profiles where the tails of distributions take on added significance. It is not unusual, therefore, to expect some systematic errors in matching the output of the simulations to the manufactured device.

A current gain (β) of between 50 to 100 was defined to be a good value for a general purpose *npn* transistor and the goal of the process development. The BICEPS simulation program calculations for the sheet resistance of the emitter and active base areas were then compared to see what value of R_{BB} was necessary to achieve the proper gain. With the emitter sheet resistance being defined by the CMOS n^+-source and drain process and thus fixed at $R_{EE} \approx 25\Omega/\square$, the active base sheet resistance should be on the order of $R_{BB} \approx 2000\Omega$ / square according to the equations derived for the graded base transistor.

Values for various base implant doses were input to the BICEPS simulation program and a dose of 5.0×10^{14} cm^{-2} found to give a value of $2650\,\Omega/\square$ for the active base sheet resistance.

With the limitations of the simulations and derived equations stated previously, it was anticipated that the active base sheet resistance, as simulated, should be higher than this amount. It was decided, therefore, to use this value of implant dose as an upper level and to systematically decrease the dose over a wide range in an effort to obtain devices with the desired current gains.

An experimental wafer lot was then started with base doses varying from 5.0×10^{14} cm^{-2} to 8.0×10^{-2}. The measured active base sheet resistance and the common emitter forward-active current gain (β) for the experimental cells are given in table 4.

Experimental Cell	Base Implant Dose @ 100 keV	Active Base Rs ($\Omega/\Box$)	β @ 10μA
1	8.0×10^{13} cm^{-2}		
2	1.0×10^{14} cm^{-2}		
3	2.0×10^{14} cm^{-2}	34,700±5,200	503±368
4	3.0×10^{14} cm^{-2}	9,834±1,527	116±39
5	4.0×10^{14} cm^{-2}	5,591±552	45±8
6	5.0×10^{14} cm^{-2}	3,850±365	31±1

TABLE 4. Test results from the first experimental wafer lot - base drive-in at 900°C for 60 min

Base implants of 8.0×10^{13} cm^{-2} and 1.0×10^{14} cm^{-2} did not produce functional bipolar transistors. The graded phosphorus implant of the emitter overcompensated these boron implants resulting in the absence of an active base region. Although a dose of 2.0×10^{14} cm^{-2} did result in working devices, their β of 500 was not representative of our defined goals and with a range of ±368 was clearly not a controllable manufacturing process.

Cells number 4 and 5, with base doses of 3.0×10^{14} cm^{-2} and 4.0×10^{14} cm^{-2} did produce transistors in the range of the desired β of 50 to 100. Cell number 6, with an implant of

5.0×10^{14} cm^{-2} produced transistors with gains lower than the design goals and were thus not characterized extensively.

Based on the previous discussion on the limitations of the simulations and derived equations, it is not surprising that somewhat lower base implant doses than the predicted 5.0×10^{14} cm^{-2} produced transistors with the specified gains.

The second wafer lot, builds on the information gathered from it's predecessor. The experimental cells of 3.0×10^{14} cm^{-2} and 4.0×10^{14} cm^{-2} which gave reasonable bipolar transistors were repeated. Doses of 3.3×10^{14} cm^{-2} and 3.7×10^{14} cm^{-2} were added to home in on the desired transistor parameters. Some wafers with these last two doses were given an additional 950°C 69 minute base drive-in to simulate heat treatments associated with the 1.75 μm analog CMOS process.

The key electrical parameters for each experimental cell are listed in table 5.

Experimental Cell	Base Implant Dose @ 100 keV	Active Base Rs (Ω/□)	β @ 10μA
1	3.0×10^{14} cm^{-2}	13,126±3,390	155±59
2	3.3×10^{14} cm^{-2}		
2a	Single poly	10,491±2,120	116±24
2b	Double poly	7,302±1,340	84±22
3	3.7×10^{14} cm^{-2}		
3a	Single poly	7,637±1,861	76±24
3b	Double poly	5,454±825	59±14
4	4.0×10^{14} cm^{-2}	6,355±886	59±14

TABLE 5. Test results from the second experimental wafer lot - base drive-in at 900°C for 60 min

The gain versus the reciprocal of the base implant dose for the four experimental cells with a common base drive of 900°C 60 minutes are plotted in figure 14.

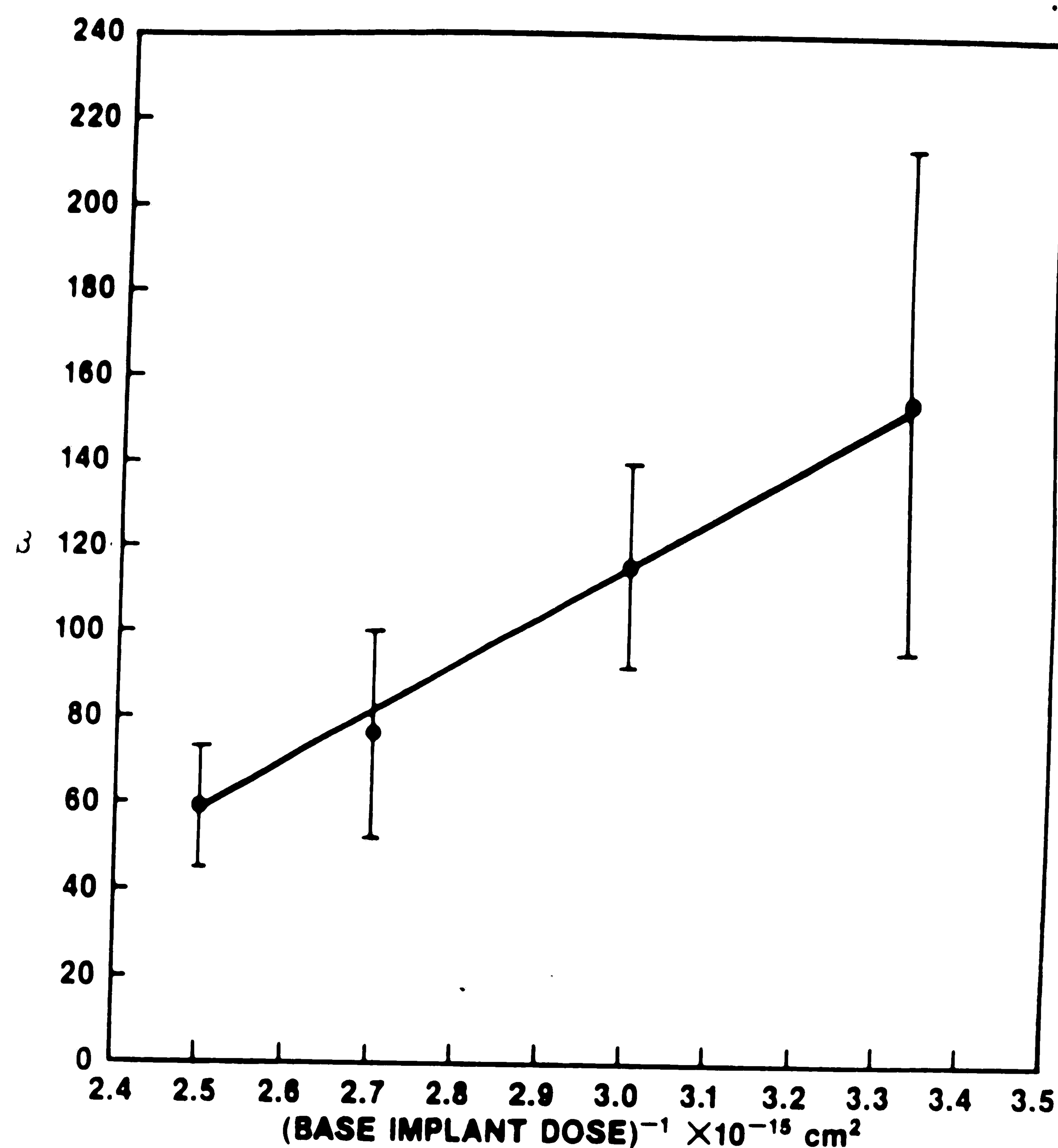


Figure 14. A plot of current gain versus the reciprocal of the base implant dose for the experimental cells of the second wafer lot

Some general comments on these results are in order. As the base implant dose increases the effective base width increases and the bipolar gain decreases. This effect is clearly seen in the data displayed in figure 14 where the error bars represent twice the standard deviation of an experimental cell. That the distribution of the gains also becomes tighter should be expected. A deeper base junction is less susceptible to the normal process variations any given lot of wafers experiences. Thus it is not surprising that there is much closer agreement between two

lots at a dose of 4.0×10^{14} cm^{-2} than 3.0×10^{14} cm^{-2}.

It has been shown that the electron current flowing into the collector junction of a *npn* transistor under forward active bias is

$$I_n \approx -I_S\, e^{\frac{qV_{BE}}{kT}} \tag{19}$$

where

$$I_S = \frac{q^2A^2{n_i}^2\tilde{D}_n}{Q_B} \tag{18}$$

Figure 2 shows a logarithmic plot of the collector current I_c as a function of the base-emitter bias V_{BE}. The intercept of an extrapolated line drawn through the collector current measurement with the current axis at $V_{BE} = 0$ yields a value of I_S in equation 19. Once I_S is known, the built-in base charge in the quasi-neutral region can be obtained from equation 18 since all the other parameters are known.

Q_{B0} represents the total hole charge in the quasi-neutral base as the base-emitter bias tends to zero and, by rewriting equation 18, is expressed as

$$Q_{B0} = \frac{q^2A^2{n_i}^2\tilde{D}_n}{I_S} \tag{20}$$

The number of base dopant atoms (per cm^2) in the quasi-neutral region is given by

$$\int_0^{x_B} N_a(x)dx = \frac{Q_{B0}}{qA} = \frac{qA{n_i}^2\tilde{D}_n}{I_S} \tag{21}$$

Substituting values of $q = 1.6\times10^{-19}$ C, $n_i = 1.45\times10^{10}$ cm^{-3}, $\tilde{D}_n = 20$ cm^2/ sec and $A = 22.56\times10^{-8}$ cm^2 into equation 21 yields

$$\text{Active base doping} = \frac{Q_{BO}}{qA} = \frac{1.52\times10^{-4}}{I_S}\ \text{cm}^{-2}$$

Equation 21 also shows that I_S, the multiplying factor for transistor current at a given bias, is inversely proportional to the total base doping. The lower the total base doping, the higher is the current at a given bias.

Transistors from the four experimental cells of the second wafer lot were further characterized to demonstrate the validity of these relationships. With the CMOS processing common to all cells, there should be no difference in the collector and emitter formation except that of normal process variation. The base implant energy and drive-in schedule were also kept constant with the base boron ion implant dose being the only process variable. It should be possible, therefore, to measure the collector current over many decades and obtain I_S from the intercept with the current axis at $V_{BE}=0$. Once I_S is known, the active base doping (Q_{B0}/qA) can be calculated and compared to the actual boron dose used for each device.

The transistors were characterized by measuring the forward-active gain (β) versus base-emitter bias (V_{BE}), the logarithm of collector current (I_C) and base current (I_B) versus base-emitter bias (V_{BE}) and the collector current (I_C) versus collector-emitter bias (V_{CE}) over a range of base current (I_B). All measurements were done with an Electroglas 1034X probe station interfaced to a Hewlett Packard 4145B Semiconductor Parameter Analyzer.

The forward-active gain (β) versus base-emitter bias (V_{BE}) was first measured in order to locate a device with a gain close to the average of the experimental cell and free of the β roll-off problem exhibited on many transistors. A plot of the gain versus V_{BE} for each of the four devices selected is shown in figure 15. With V_{BE} ranging from 0.4V to 0.9V, the collector current will vary from less than a nano ampere to more than a milli ampere. Very little β_f degradation was observed over this wide range of collector current for curves a, b and d. Curve c shows some of the effect of the β_f degradation due to the presence of recombination

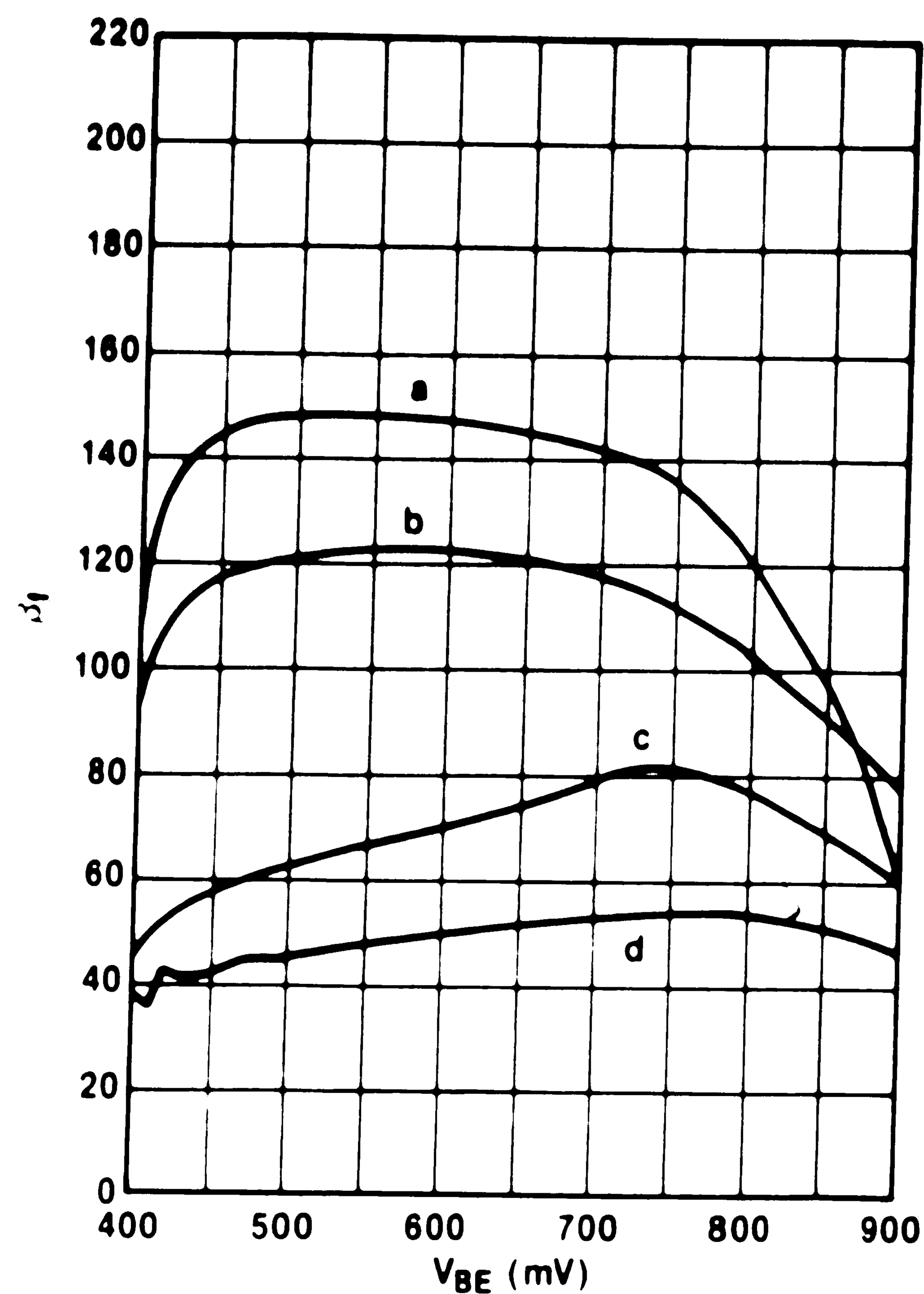


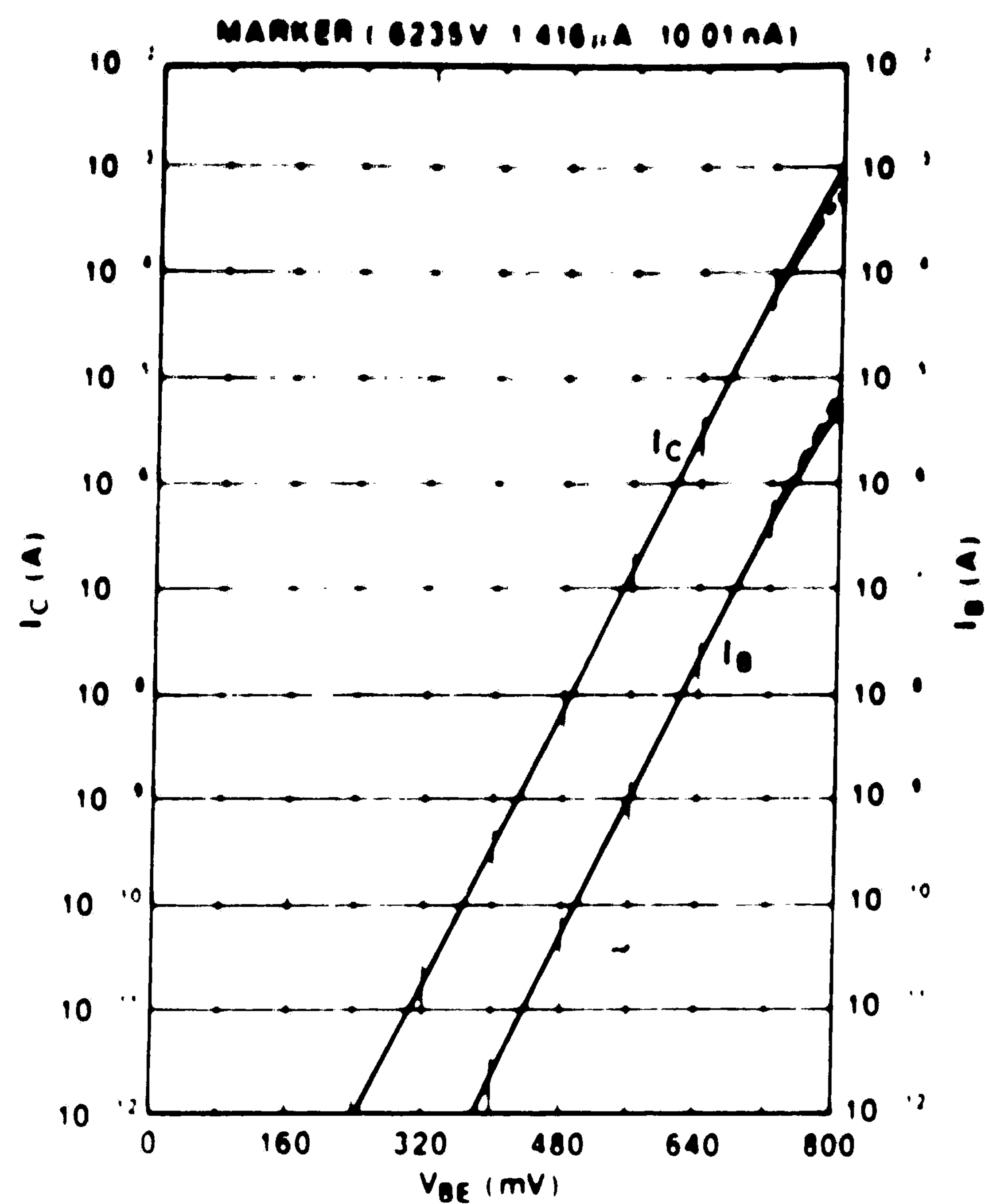
Figure 15. β_f versus base-emitter bias (V_{BE}) of the bipolar transistor for the active base implant conditions a) 3.0×10^{14} cm^{-2} b) 3.3×10^{14} cm^{-2} c) 3.7×10^{14} cm^{-2} and d) 4.0×10^{14} cm^{-2}. The emitter size is 4.75µm × 4.75µm.

centers in the emitter-base space charge region of the device.

When plotting V_{BE} versus log I_C with V_{BC} = 0V (figure 16), a linear relationship over nearly eight decades of current was observed. The average slope of the four transistors was 61.6 mV/decade, very close to the voltage change for an ideal diode of 59.6 mV/decade. If the collector current, I_n, is expressed as

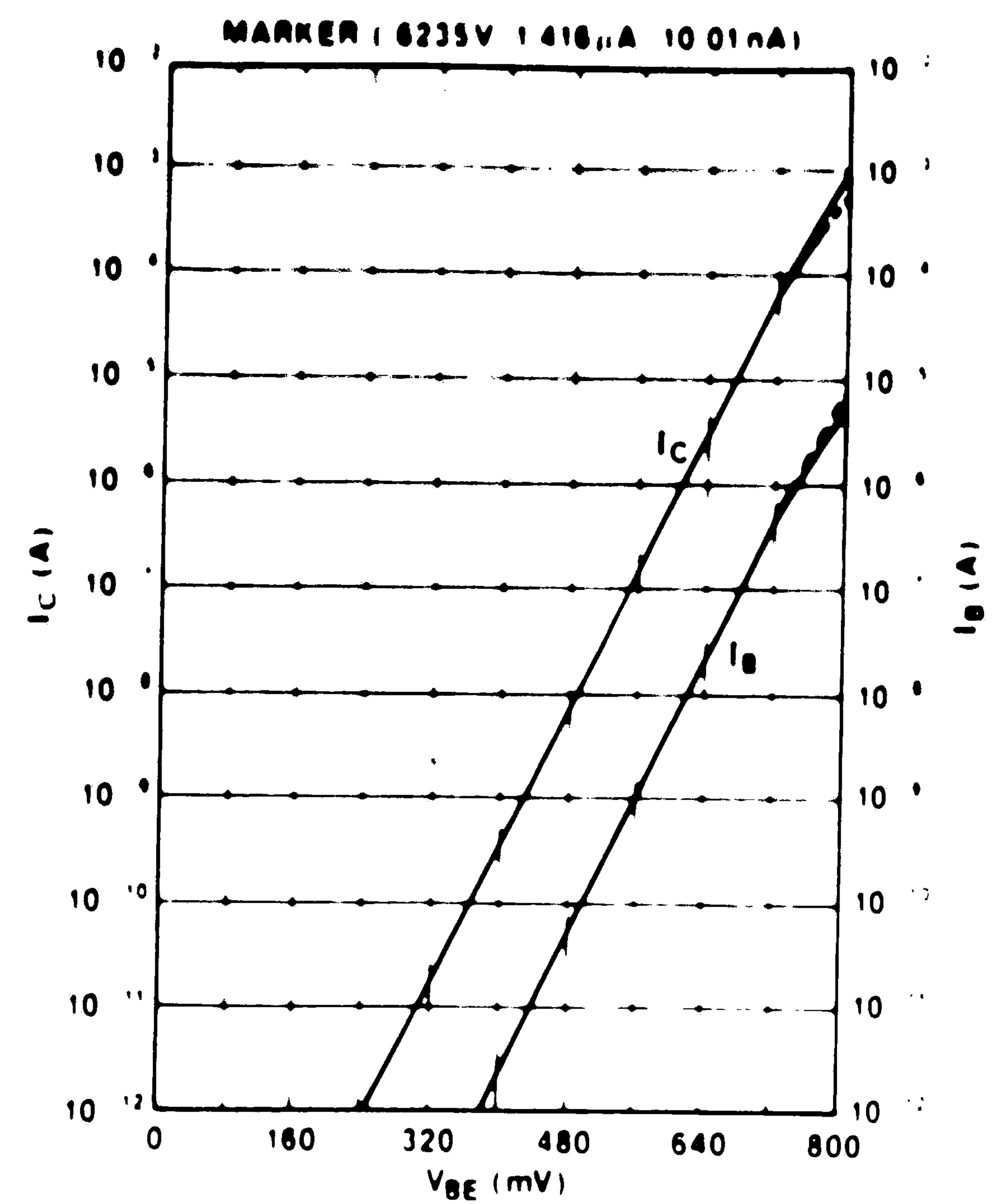
$$I_n \approx -I_S\, e^{\frac{qV_{BE}}{kT}} \tag{19}$$

where q is the electronic charge and kt the Boltzman energy, I_S can be measured from the plot of log I_C versus V_{BE}. These measurements and the extrapolations of collector current to the current axis at V_{BE} = 0 are shown in the next figure with the results summarized in table 6.



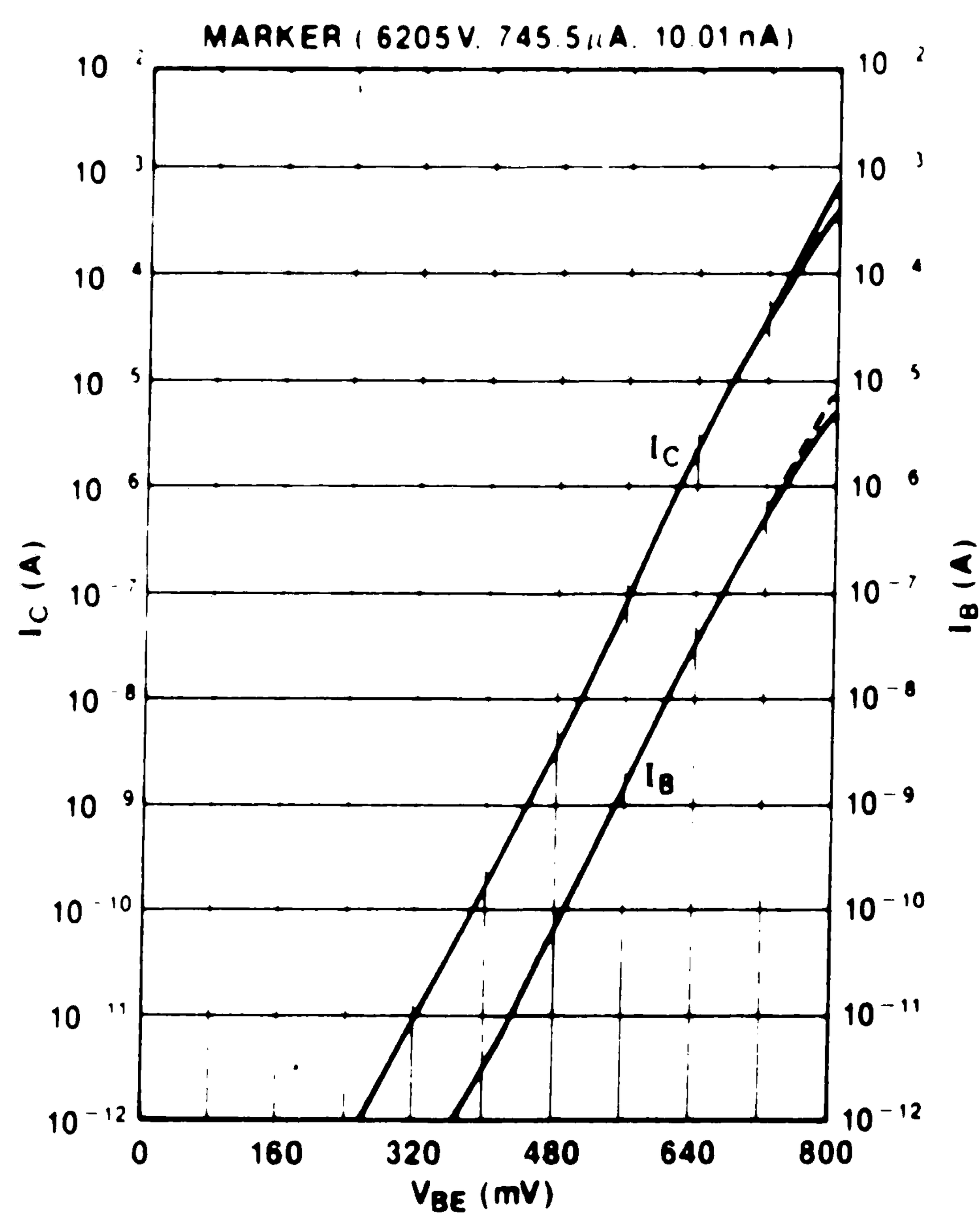
	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.1E+00	62.1E−03	987E−03	133E−18
LINE 2	16.4E+00	61.1E−03	1.11E+00	630E−21

a



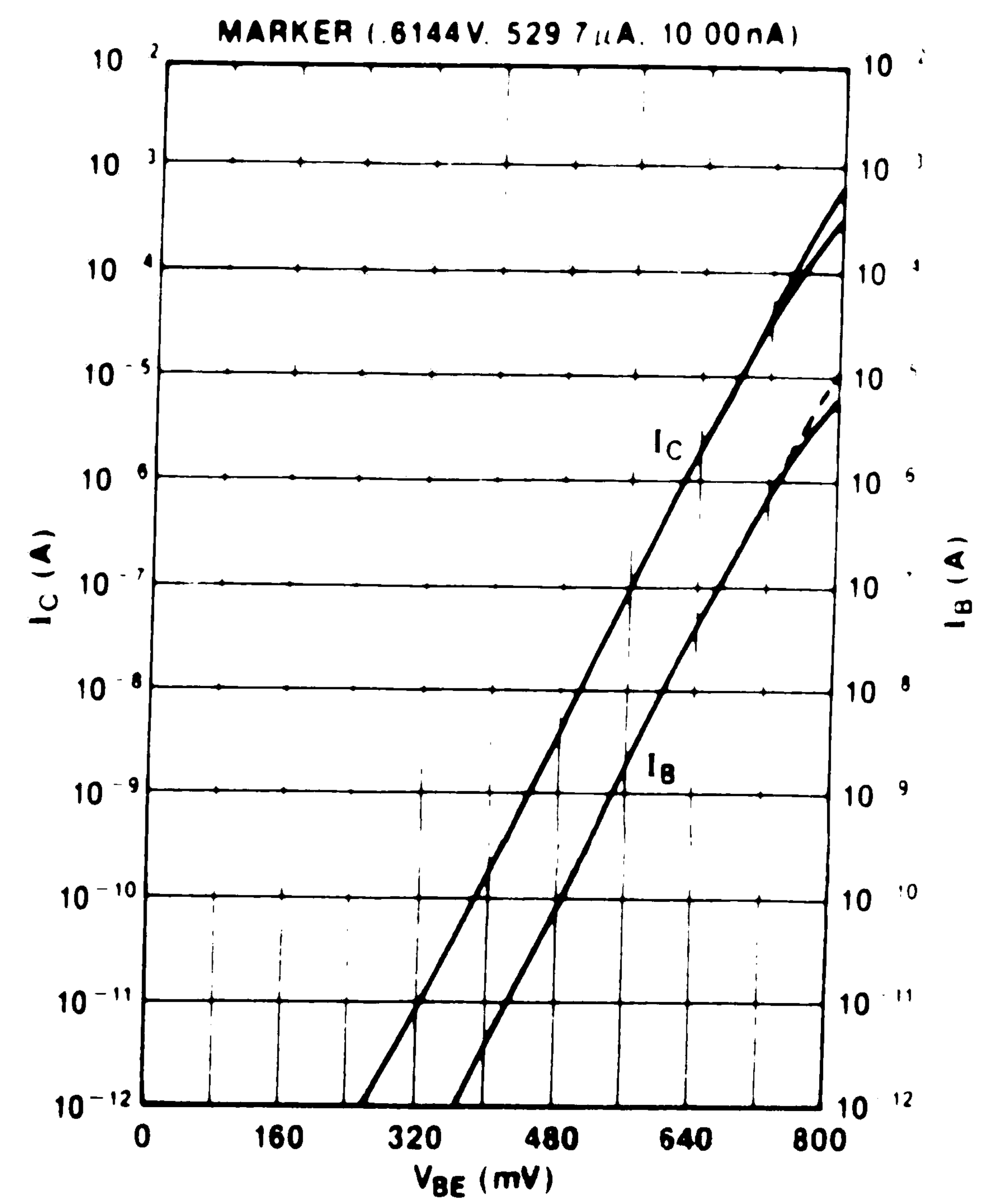
	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.1E+00	62.1E−03	987E−03	133E−18
LINE 2	16.4E+00	61.1E−03	1.11E+00	630E−21

b



	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.2E+00	61.5E−03	99E−03	59.2E−18
LINE 2	16.0E+00	62.6E−03	1.12E+00	1.24E−18

c



	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.4E+00	61.1E−03	998E−03	46.7E−18
LINE 2	16.2E+00	61.7E−03	1.11E+00	1.12E−18

d

Figure 16. Collector current I_C and base current I_B versus base-emitter voltage V_{BE} for a bipolar transistor with an active base doping of a) 3.0×10^{14} cm^{-2} b) 3.3×10^{14} cm^{-2} c) 3.7×10^{14} cm^{-2} and d) 4.0×10^{14} cm^{-2} . The emitter size is 4.75μm ×4.75μm.

Base Implant Dose @ 100 keV	β @ $10\mu A$	$\frac{1}{GRAD}$ for I_C (mV/decade)	Y Intercept or I_S (A)	$\frac{Q_{B0}}{qA}$ (cm^{-2})
3.0×10^{14} cm^{-2}	141	62.1	133.0×10^{-18}	1.14×10^{12}
3.3×10^{14} cm^{-2}	116	61.6	85.8×10^{-18}	1.77×10^{12}
3.7×10^{14} cm^{-2}	75	61.5	59.2×10^{-18}	2.57×10^{12}
4.0×10^{14} cm^{-2}	53	61.1	46.7×10^{-18}	3.25×10^{12}

TABLE 6. Measurements of forward active current gain (β_f), collector current slope, and I_S with calculated values of Q_{B0}/qA for each base implant dose of the second experimental wafer lot.

A graph of Q_{B0}/qA versus base implant dose, figure 17, clearly shows the direct relationship of the total hole charge in the quasi-neutral base region (Q_{B0}) to the total base doping.

From equation 33 we know that the common-emitter current gain

$$\beta \approx \frac{N_E}{\frac{Q_{B0}}{qA}} \tag{33}$$

where N_E is the emitter doping and Q_{B0} is the total base doping in the quasi-neutral base. The inverse relationship between the common-emitter current gain and doping in the quasi-neutral base region is shown in figure 18 where B_f is plotted against Q_{B0}/qA for the four measured transistors of the second experimental lot. Since the emitter charge, base ion implant energy and thermal drive-in schedule are constant the gain of the bipolar transistor is inversely proportional to base Gummel number or active-base implant dose. The relationship given by equation 33 is verified in figure 18.

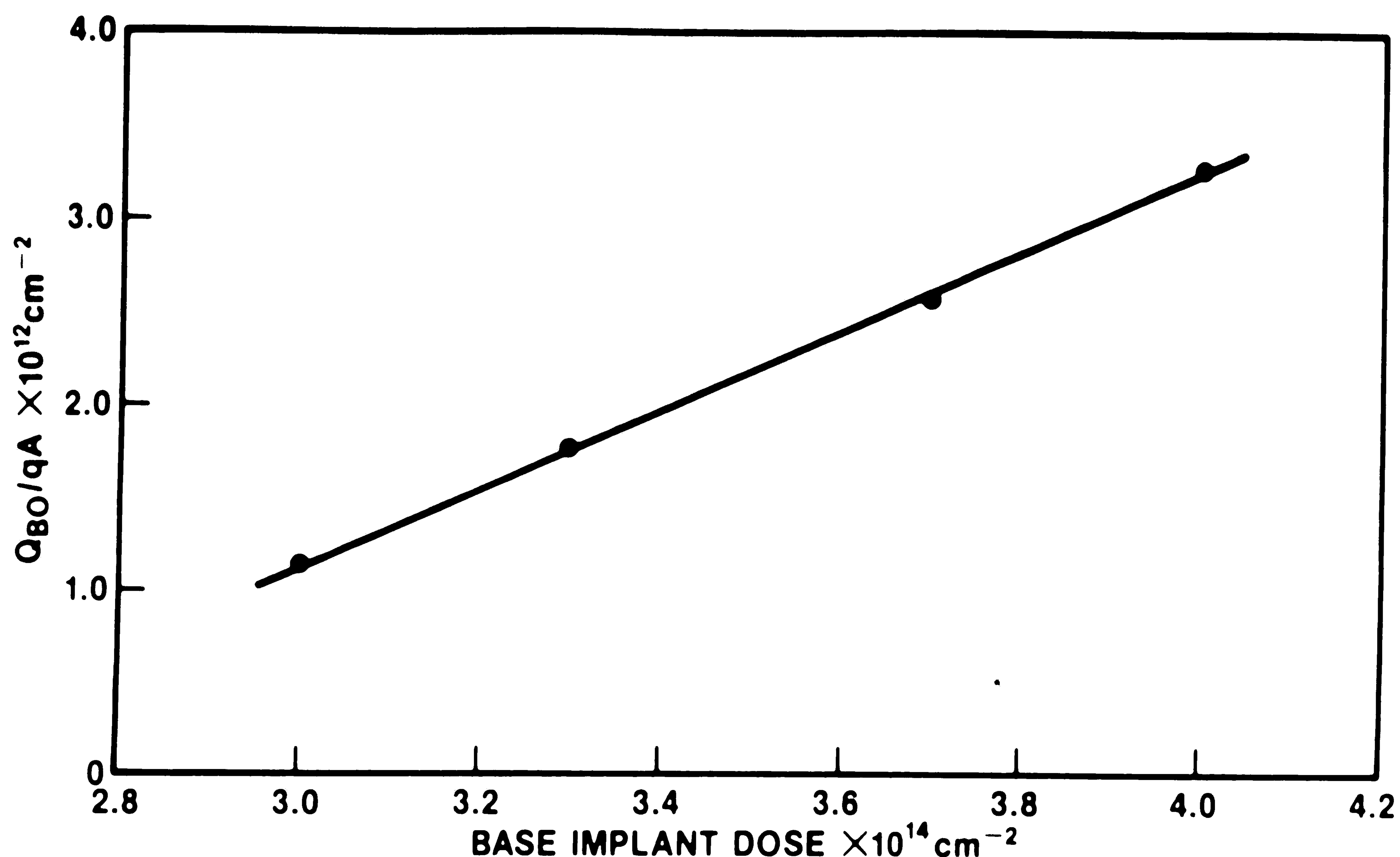


Figure 17. A plot of the total hole charge in the quasi-neutral base region Q_{B0}/qA versus base implant dose

The output characteristics of the four measured devices are shown in figure 19. The collector saturation resistance R_C is large since there is no buried collector region in the structure. The noticeable slope in the nearly horizontal portion of the curves of figure 19a is due to enhanced base-width modulation caused by the reduced boron concentration the base of the high gain device. As the gain of the devices decreases from 142 to 116, 75, and 53 (measured at $I_B = 10nA$) for curves a to d of figure 19, the magnitude of the collector current decreases accordingly. On the characteristic curves, β_f is measured by the difference between adjacent I_C curves. It can be seen that the high gain device of curve 19a has a greater spacing than the lower gain devices.

The effect of the additional 950°C 69 minute drive-in can be seen in the results from the middle two experimental cells. For 3.3×10^{14} cm^{-2} the gain changed from 116 ± 24 to 84 ± 22

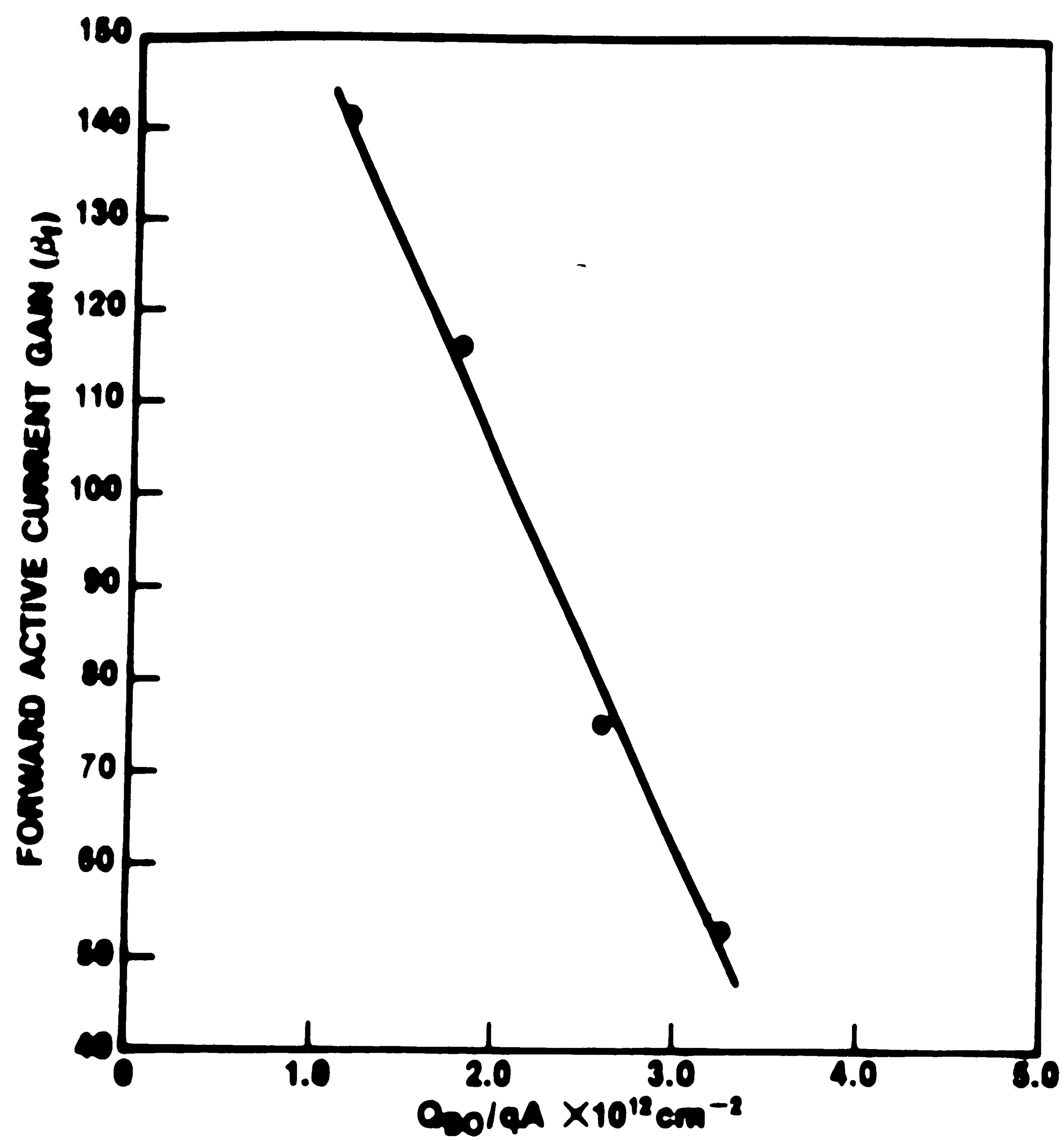
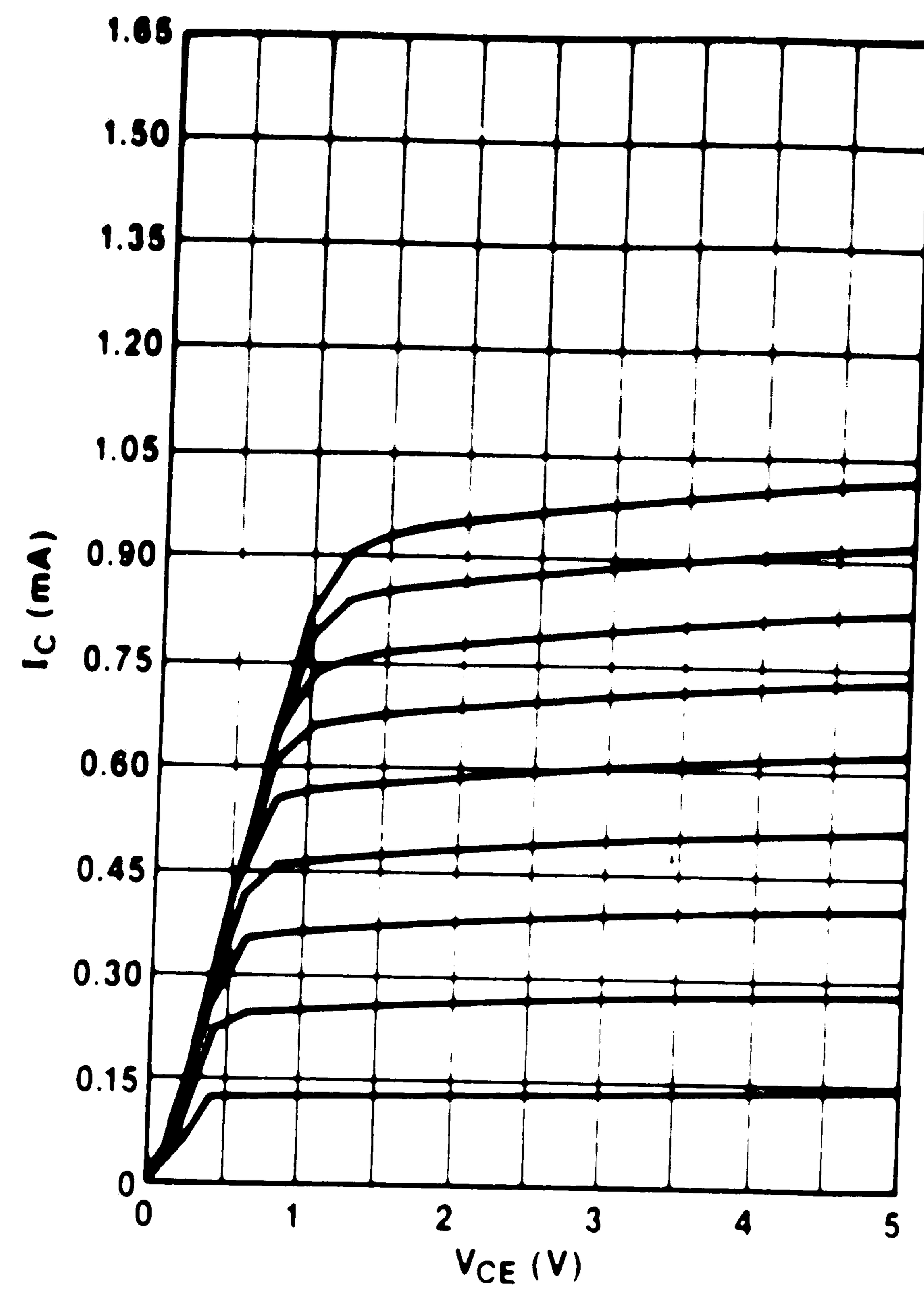
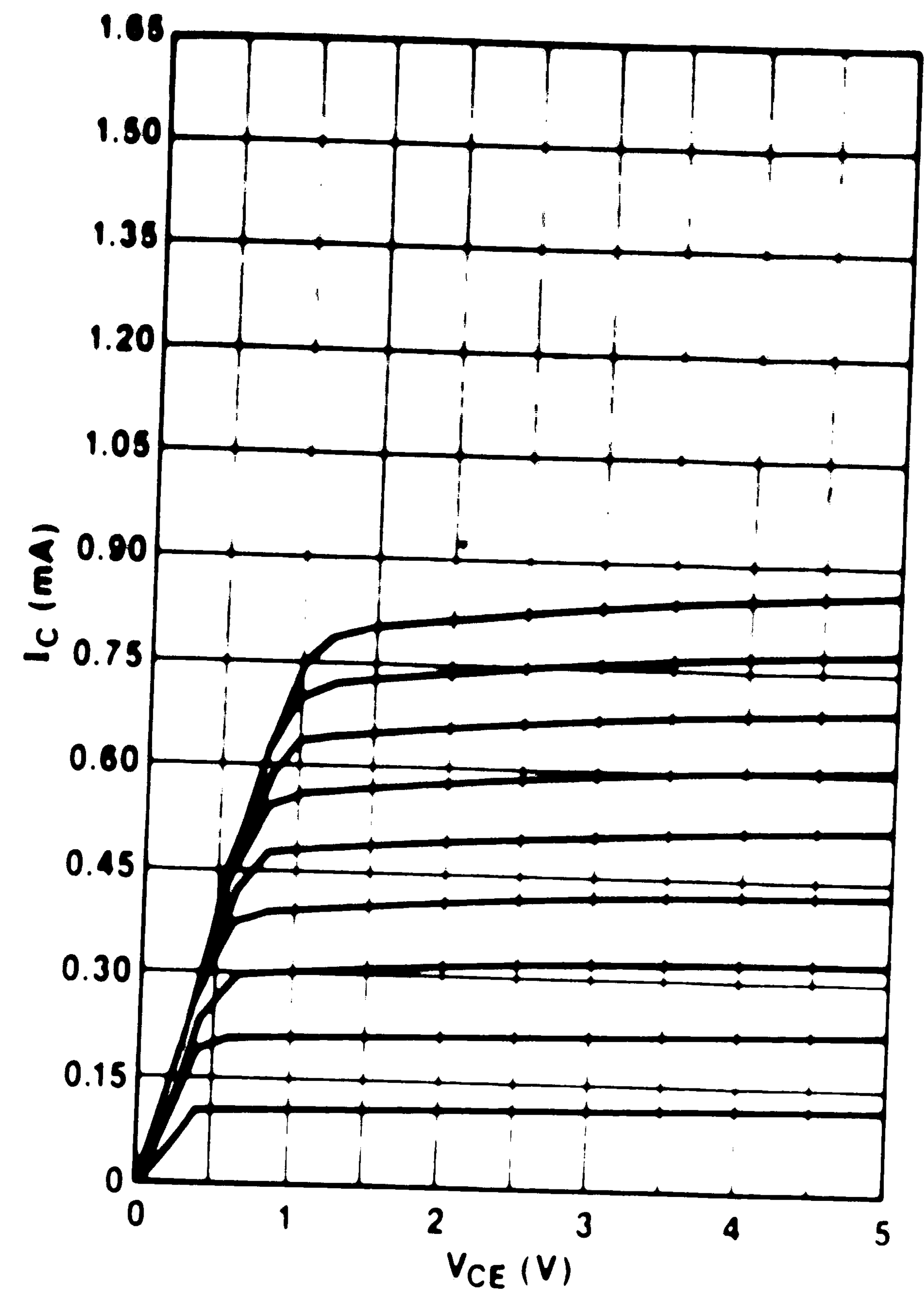
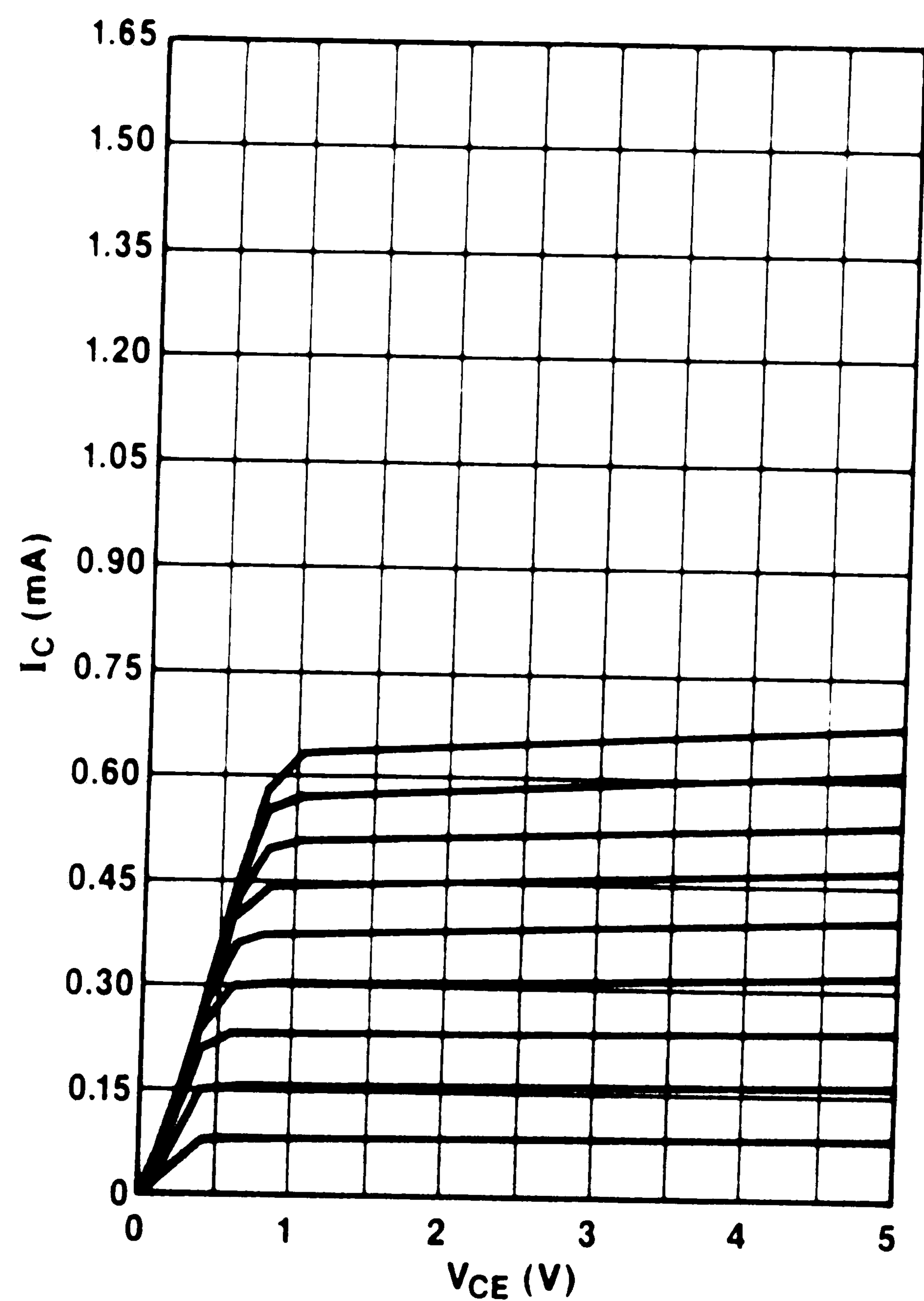


Figure 18. A plot of common-emitter current gain versus base doping in the quasi-neutral base region Q_{B0} / qA for the measured wafers from the second experimental lot.







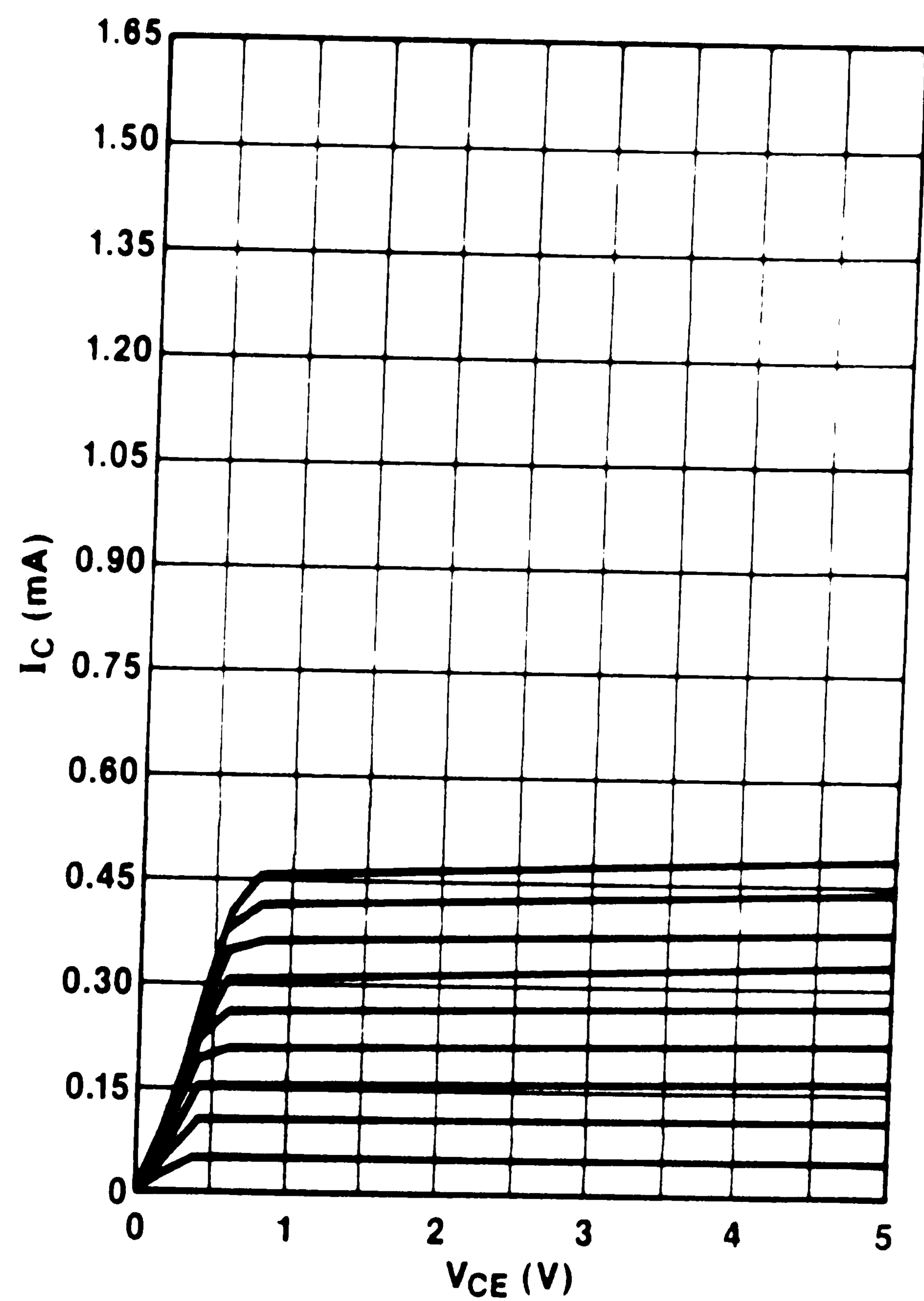


Figure 19. Collector current I_C versus collector voltage V_{CE} for a bipolar transistor with an active base doping of a) 3.0×10^{14} cm^{-2} b) 3.3×10^{14} cm^{-2} c) 3.7×10^{14} cm^{-2} and d) 4.0×10^{14} cm^{-2}. $I_B = 1.0\mu A$ per step, 9 steps, the emitter size is 4.75μm ×4.75μm.

and for the heavier implant of 3.7×10^{14} cm^{-2} from 76 ± 24 to 59 ± 14. Note that for the higher implant dose the percentage decrease of gain is less. This again is attributable to the deeper base junction associated with the heavier implant dose.

A third wafer lot was started after the second but prior to it's completion. The lot seeks to expand on information in the region of interest defined by the completed experiments. By specifying experimental cells with base doses of 2.9×10^{14} cm^{-2}, 3.2×10^{14} cm^{-2}, 3.5×10^{14} cm^{-2} and 3.8×10^{14} cm^{-2} it augments the doses already selected for processing lot number two. There was also an experiment performed to examine the effect of varying the base implant energy and the properties of the bipolar transistor. In addition to the standard 100 keV energy, implants of 3.2×10^{14} cm^{-2} boron were done at 80 keV and 120 keV. The gain and active base sheet resistance for each experimental cell are listed in table 7.

Experimental Cell	Base Implant Dose @ 100 keV	Active Base Rs (Ω/□)	β @ 10μA
1	2.9×10^{14} cm^{-2}	9,214±1,319	123±30
2	3.2×10^{14} cm^{-2}		
2a	80 keV	23,866±4,732	334±117
2b	100 keV	7,129±1,054	92±41
2c	120 keV	3,912±752	47±13
3	3.5×10^{14} cm^{-2}	6,382±940	77±15
4	3.8×10^{14} cm^{-2}	5,106±769	55±16

TABLE 7. Test results from the third experimental lot - base drive-in at 900°C for 60 min

The gain versus the reciprocal base implant dose for the four experimental cells with a common 100 keV implant energy are plotted in figure 20.

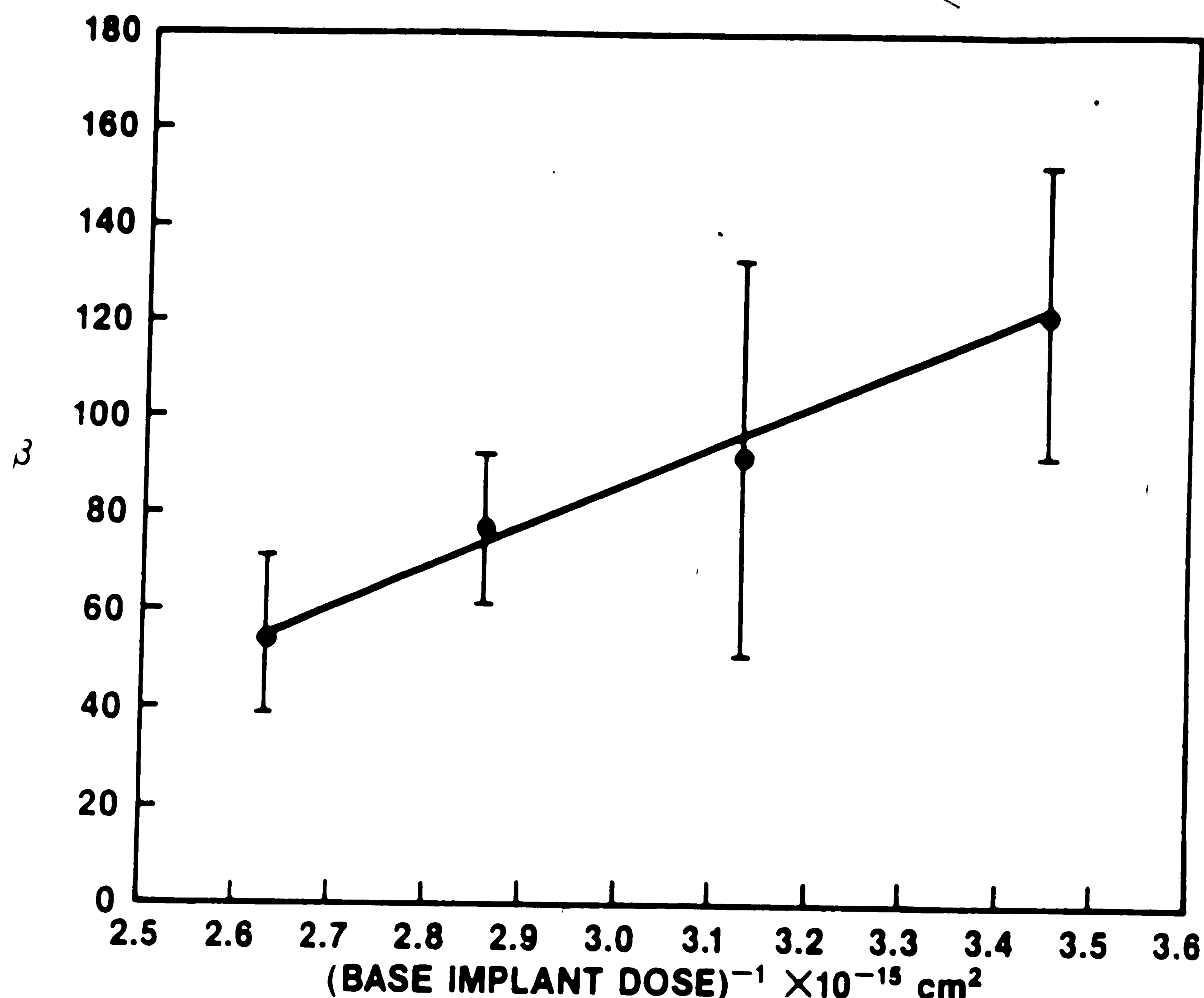


Figure 20. A plot of gain versus reciprocal base implant dose for the experimental cells of wafer lot number three

The same trends of gain and distribution of the gains seen in earlier data continues.

By keeping the base implant dose and drive-in constant, the effect of varying the implant energy is clearly seen in experimental cell number 2. With a dose of 3.2×10^{14} cm^{-2} at 100 keV an average gain of 92 was realized. By decreasing the base implant energy to 80 keV the transistor gain raises to 334. The results from the first experimental lot suggest gains of this value would be associated with a dose closer to 2.0×10^{14} cm^{-2}. This trend of an apparent loss of boron in the net active base region is consistent with the arguments presented earlier regarding the original base implant energy. There is evidently, quite a large amount of the implanted boron being left in the 900Å sacrificial oxide or lost by segregation in the

subsequent 250Å gate oxidation with the lower energy implant. The 120 keV result of an average gain of 47 further substantiates this argument.

3.3 Manufacturing Difficulties

The BiCMOS process behaves in a predictable manner with respect to base implant dose versus forward-active common-emitter current gain and devices were fabricated with gains in the desired 50 - 100 range. These transistors had acceptable break-down voltages and were fabricated with no changes to the CMOS characteristics. There was observed, however, a problem with decreased gain at small collector currents. The problem appears randomly within a test site and across a wafer and it is not unusual to appear on the majority of transistors tested. The phenomenon is present in each lot of wafers processed over several manufacturing facilities and does not appear to be related to the base dose or implantation energy. Since the β fall-off phenomenon adversely impacts the value of β at the reported 10μA base current, only those sites unaffected by the problem were used in the formulation of the data tables presented thus far. This was done to facilitate the correlation of experimental data to the process modeling.

A plot of the forward-active current gain ($\beta_f = I_C/I_B$) as a function of base-emitter voltage (V_{BE}) for two transistors with the same processing is shown in figure 21. Very little degradation of gain over a wide range of bias is observed on curve 21a, a device with near ideal current-voltage characteristics, while curve 22b demonstrates a major fall-off of gain throughout the low and intermediate ranges of bias.

As detailed in section 2.2 Recombination Theory, recombination in the base-emitter space-charge region can account for added base-emitter current observed at low biases. The equations describing generation and recombination in the space-charge zone through localized states or recombination centers originally described by Shockley, Reed and Hall showed the

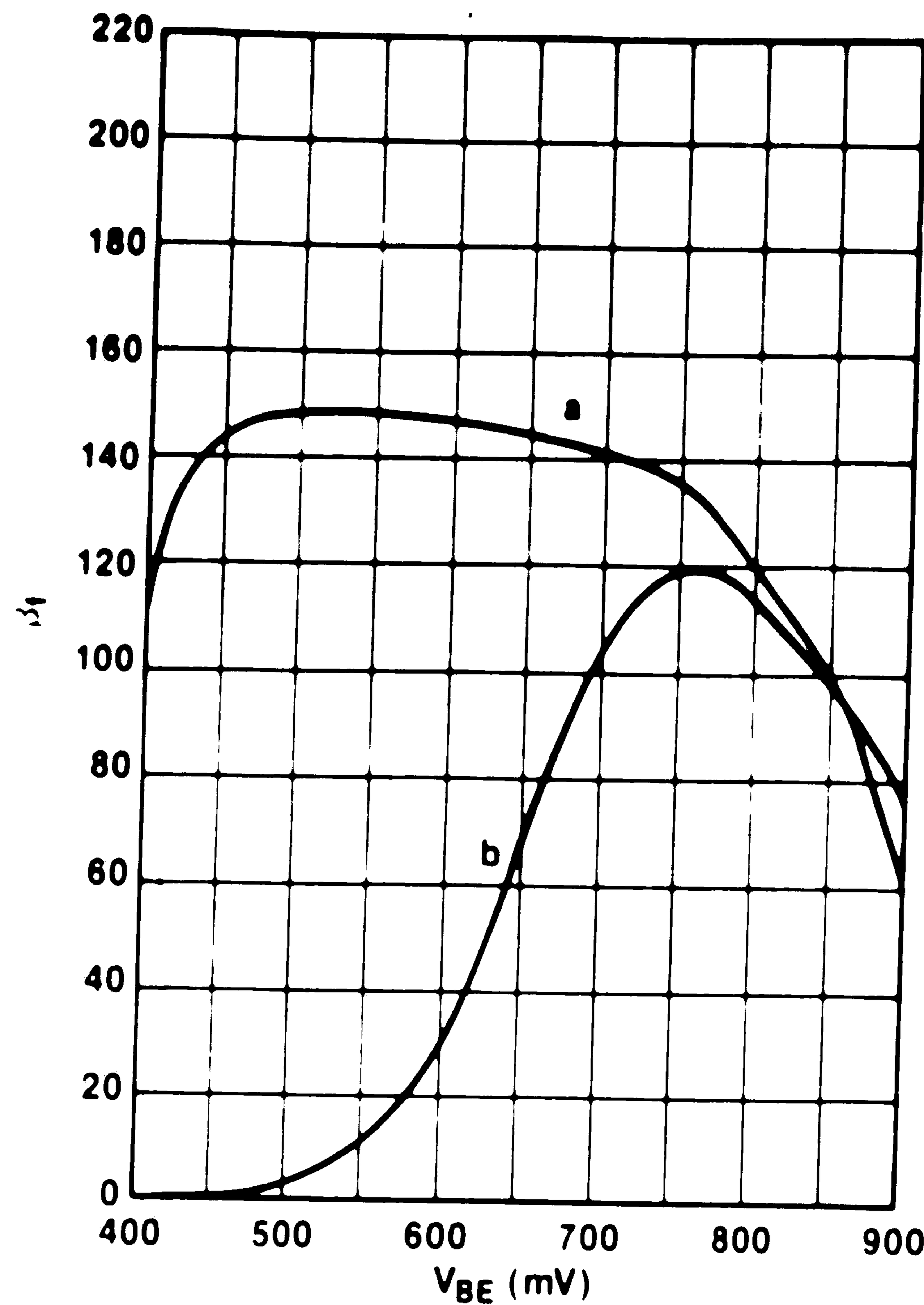


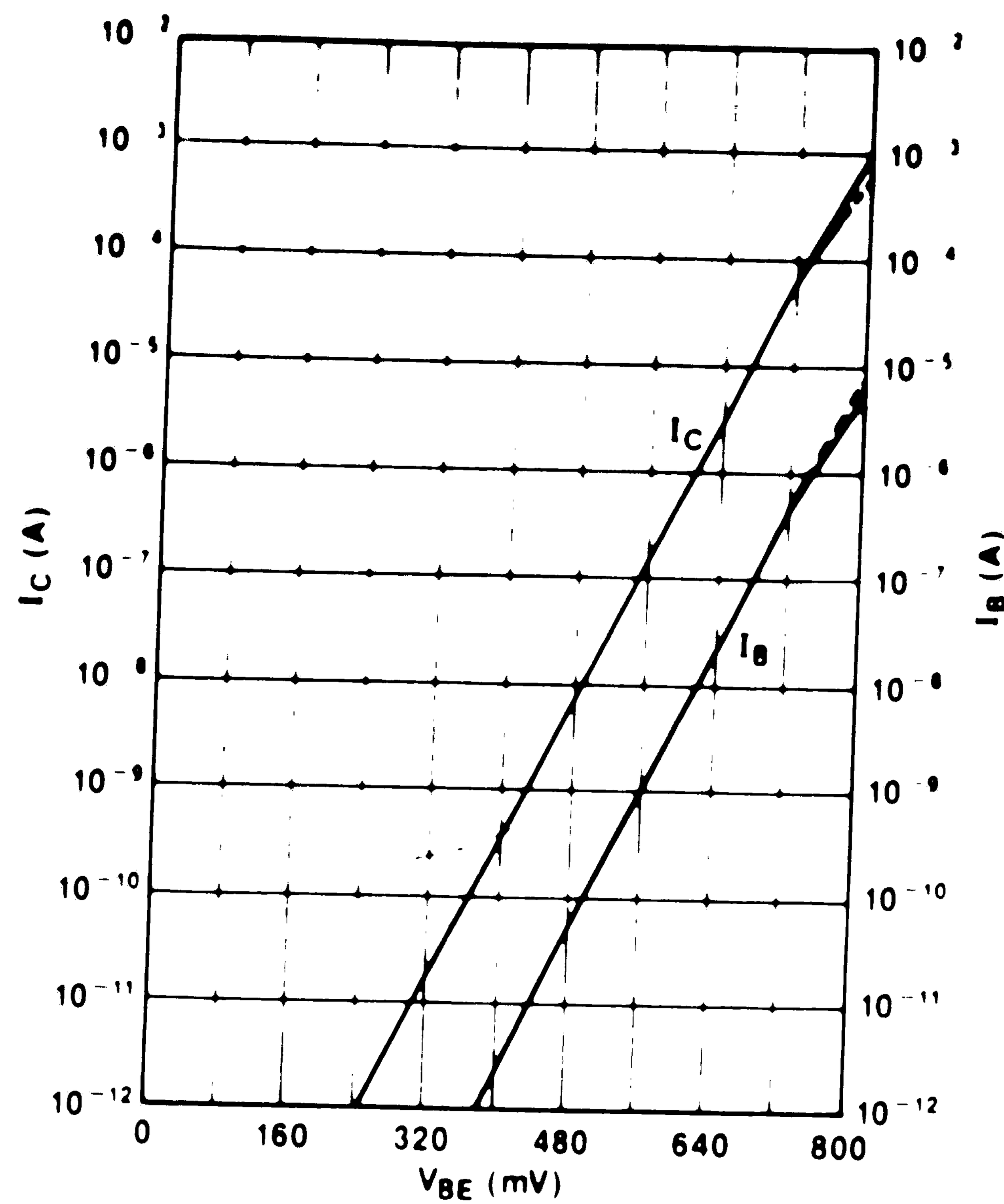
Figure 21. β_f versus base-emitter bias (V_{BE}) for two devices with the same processing conditions a) a device with near ideal characteristics b) a device with significant base recombination current.

current arising from recombination in the space-charge region varies with applied voltage as $e^{\frac{qV_a}{2kT}}$. The ratio between the ideal diode current J_t and the space-charge zone recombination-current J_r under forward bias is given by

$$\frac{J_t}{J_r} = \frac{2n_i}{x_d}\left(\frac{L_n}{N_a} + \frac{L_p}{N_d}\right) e^{\frac{qV_a}{2kT}} \tag{24}$$

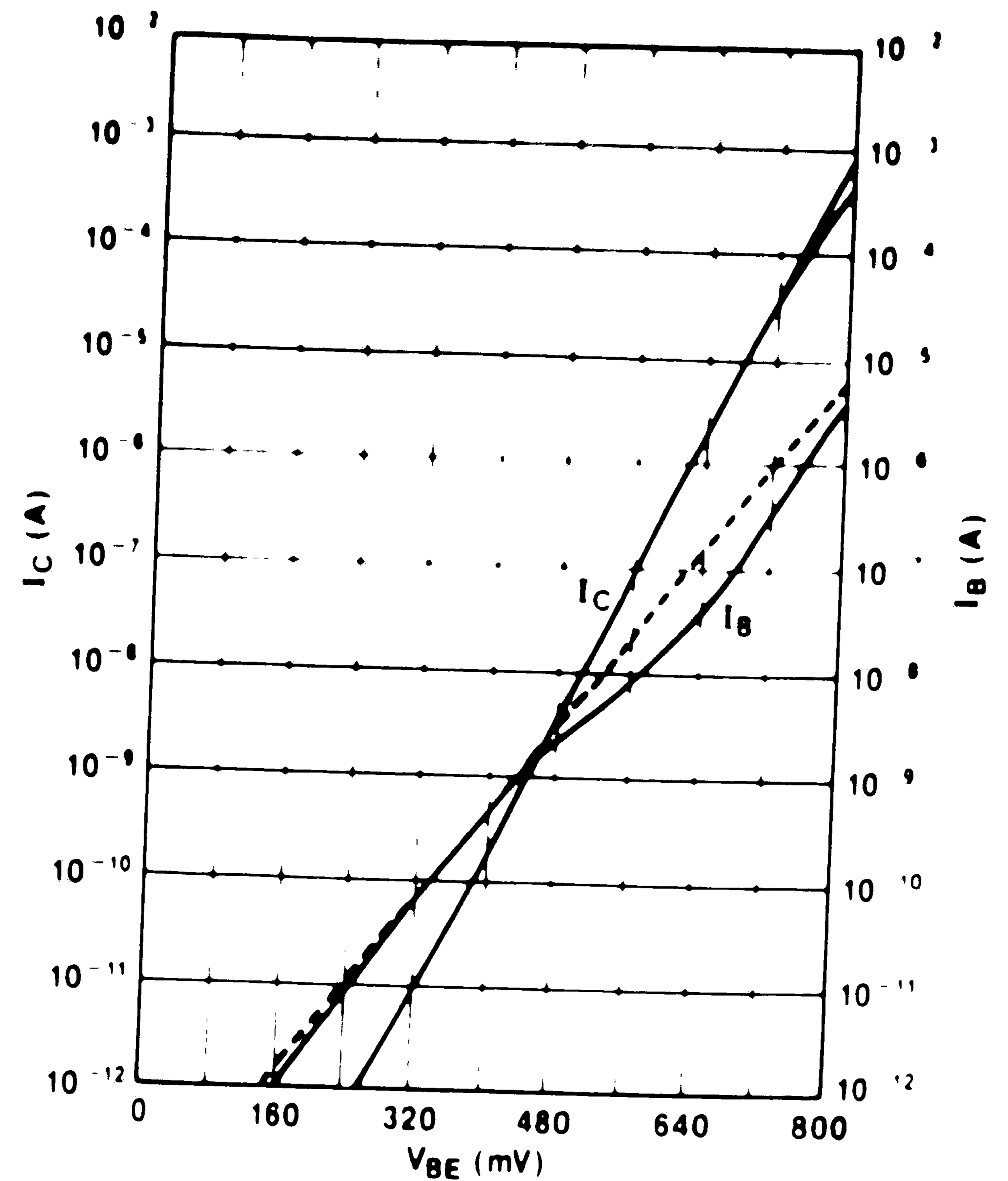
where $L_p = \sqrt{D_p \tau_p}$ is the diffusion length of a hole in a *n*-type region and L_n is the diffusion length of an electron in a *p*-type region. From the above relationship it is apparent that J_r is less significant relative to the ideal diode current as bias increases. Also, the more defect-free the material, the longer the diffusion lengths and the more dominant is J_t over J_r.

A plot of the base-emitter bias (V_{BE}) versus the log of collector current (I_C) with $V_{BC} = 0$ V for the same two devices of figure 21 is shown in the next figure.



	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.1E+00	62.1E−03	987E−03	133E−18
LINE 2	16.4E+00	61.1E−03	1.11E+00	630E−21

a



	GRAD	1/GRAD	X INTERCEPT	Y INTERCEPT
LINE 1	16.6E+00	60.3E−03	987E−03	42.4E−18
LINE 2	10.3E+00	97.0E−03	1.31E+00	34.1E−15

b

Figure 22. Collector current I_C and base current I_B versus base-emitter voltage V_{BE} for a bipolar transistors with a) near ideal characteristics and b) exhibiting large recombination components.

With the collector current displayed on the vertical logarithmic axis, β_f is obtained directly from the plot as the distance between the I_C and I_B curves. By examining the data in this plot the reason for the variation of β_f with I_C is now evident. In the low and intermediate current range, β_f is governed by additional components of I_B. The straight lines drawn on the collector and base current plots of figure 22a show that these currents nearly follow the ideal ($n = 1$) current-voltage dependence of 59.6 mV/decade of current. While the collector current of the device shown in figure 22b is also consistent with the ideal diode behavior suggested by equation 19, the base current shows a significant deviation of slope over the same range of bias. Only at the high level injection condition, where the collector current is very large, do

the slopes of the two curves come close to resembling each other.

If the extra components of base current are caused by the recombination of carriers at the surface or in the emitter-base space-charge region then the experimental data of figure 22b should fit a curve represented by

$$I_B \approx I_0 \, e^{\frac{qV_{BE}}{nkT}} \tag{25}$$

where n is generally found to have a value between one and two depending on the amount of recombination current present and I_0 is larger than the corresponding multiplier for an exponential form fitting the data of a device with ideal characteristics.

The straight line drawn on the plot of base current of figure 22b represents a reasonable fit to the curve over values of V_{BE} = 0.20V to V_{BE} = 0.44V. The 1/GRAD value of 97.0E-3 seen on the same figure represents a value of n = 1.63 in equation 25 while I_0 is given by the y-intercept value 34.1E-15 A. As recombination theory suggests, this value is substantially larger than the I_0 = 630E−21 A shown on the good device of figure 22a. Substituting values of $I_0 = 34.1\times10^{-15}$ A, q/kT = 0.0259 V, n = 1.63 and V_{BE} = 0.20 V and V_{BE} = 0.44 V into equation 25 yields

$$I_B \approx 34.1\times10^{-15} \, e^{\frac{0.20}{(1.63)(0.0259)}} = -3.89\times10^{-12}\,\text{A}$$

and

$$I_B \approx 34.1\times10^{-15} \, e^{\frac{0.44}{(1.63)(0.0259)}} = -1.15\times10^{-9}\,\text{A}$$

These calculations of base current are in good agreement with the values seen on the plot of figure 22b. Further examination of the plots show that at higher bias values n would be lower than 1.63 approaching the ideal value of n = 1. These experimental results are consistent with

those predicted by Shockley Reed Hall recombination theory.

As has been shown, collector current is an exponential function of base-emitter voltage since a forward bias on the base-emitter junction causes electron injection into the base to vary exponentially. Under active bias, these electrons are collected efficiently by the field at the base-collector space-charge region. Current flowing between the collector and the emitter represents the output current in an active-biased transistor. When injected electrons from the emitter do not diffuse through the base and recombine with holes, a current which is not collected flows out of the base region. The smaller the current that flows through these terminals for any given positive V_{BE}, the more effectively the transistor will act as an amplifier since the input power (the product of V_{BE} and the base-emitter current) will be lower.

In circuit applications in which the input current swings over a wide range, differences in the $I-V$ characteristics results in highly nonlinear operation, distorting the collector output signal. It is good design practice, therefore, to keep current gain as a function of I_B as constant possible over the allowable range of emitter currents. For those circuits requiring amplification of very small a-c signals, it is desirable that α_T, the base transport factor, peak rapidly with emitter current, in order that the smallest possible d-c base bias current be used for minimum power supply drain. The concern with the effect of input current swings over a wide range is addressed by examining the common-emitter output characteristic $I-V$ curves.

A typical family of curves for the devices shown in the last two figures is drawn in figure 23. The output curves are plots of collector current, I_C, versus collector to emitter voltage, V_{CE}, for different values of base current. Although the plots are of V_{CE}, V_{CE} is almost the same as the collector-base voltage, V_{CB}, for bias in the active region with $V_{CE} \approx V_{CB} + 0.7$ V. With the base current equal to zero, a $I-V$ curve at $I_B = 0$ would correspond to the I_{CEO} current as a function of voltage and is similar to the reverse saturation characteristics of a p-n junction. Since the effective base thickness varies as the collector depletion layer widens with

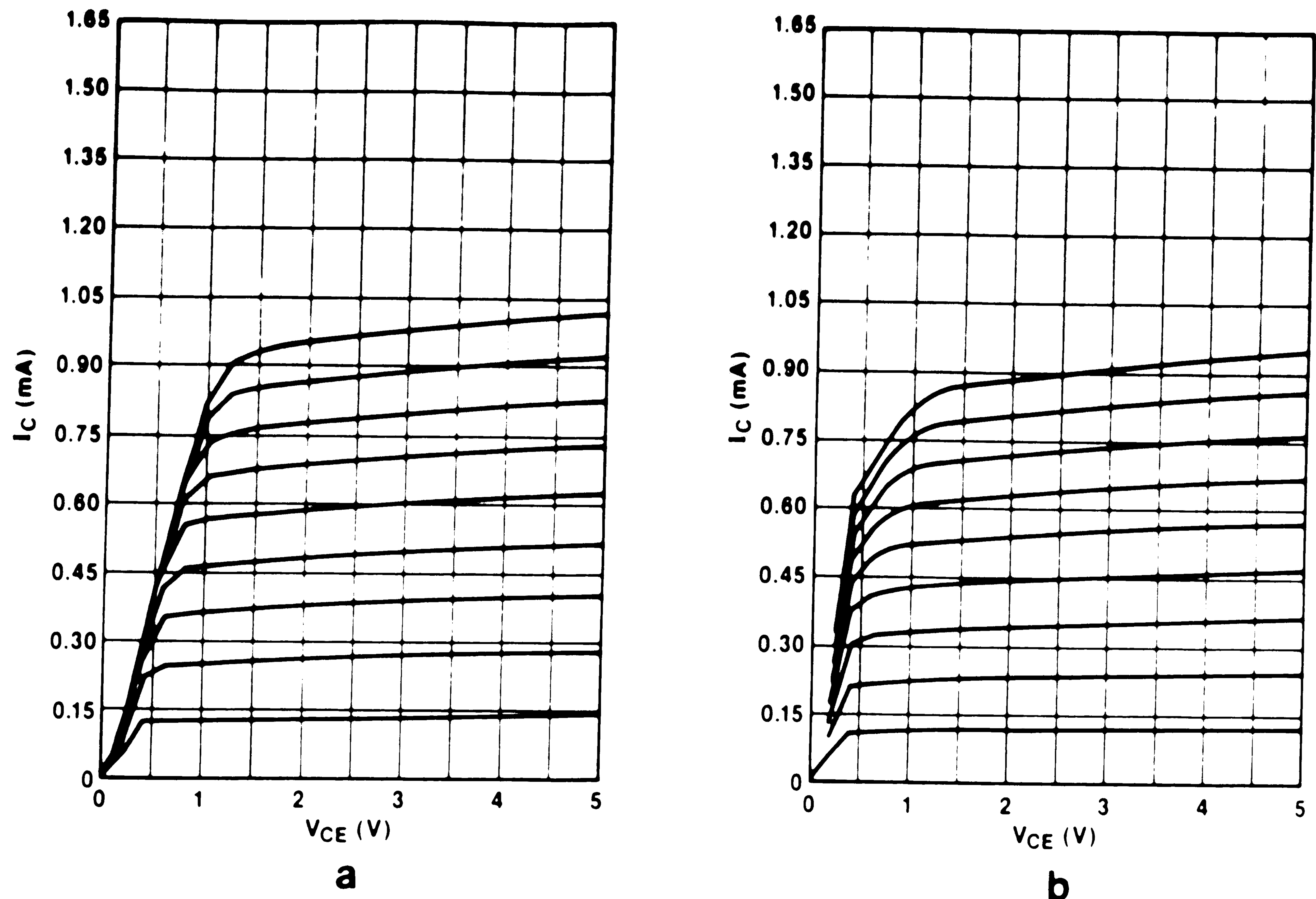


Figure 23. Collector current I_C versus collector voltage V_{CE} for bipolar transistors with a) near ideal current-voltage characteristics and b) significant base recombination current. Base current $I_B = 1.0\mu A$ to $9.0\mu A$, $1.0\mu A$ steps.

voltage, a small increase in α_T is expected to occur. Beta, being quite sensitive to small changes in α_T ($\beta_f = \gamma\alpha_T / 1-\gamma\alpha_T$), increases at a much faster rate. It is for this reason that the curves slope upward. Similarly, the sensitivity of beta to changes in α_T also creates a more rapid fall-off of beta with emitter current density as emitter efficiency, γ, decreases. This accounts for the more pronounced crowding of the I – V characteristics at the higher input base currents.

At the base current levels injected into the near ideal device of figure 23a, $I_B = 1.0\mu A$ corresponds to a bias of $V_{BE} = 0.74$ V and $I_B = 9.0\mu A$ corresponds to a value of $V_{BE} > 0.80$ V (V_{BE} values taken from the plots of figure 22a). In this regime of operation the bias is moving away from the near ideal current-voltage relationships due to expected high current effects. While seen in the turning down of the curves of figure 22a, the β_f fall-off is more evident in

figure 21a where the range of bias was extended to 0.9 V. With $\beta_f = \Delta I_C / \Delta I_B$ and $\Delta I_B = 1.0 \mu A$, a constant, the same β_f fall-off present in curve a of figure 21 is seen in figure 23a as the compression of the I_C curves at the highest levels of base injection.

The family of curves for the device with significant recombination current is shown in figure 23b. At these high levels of base current injection, the range of bias is the same as that of figure 23a, $V_{BE} = 0.74$ V to greater that 0.80 V. An examination of figure 22b shows that over this range of bias, the slope of the I_B curve comes closest to that of the near ideal I_C curve (n=1). Thus it is not surprising to find almost identical I−V characteristics to that of the near ideal device of figure 23a.

This similarity of I−V characteristics for the two devices does not, however, extend to lower levels of base current injection. Figure 24 shows the family of curves over the much lower range of $I_B = 1.0$nA to 91nA. On the near ideal device of figure 24a, this corresponds to biases of $V_{BE} = 0.56$ V to $V_{BE} = 0.68$ V. The curves of figures 21a and 22a show no deviation from ideal behavior and the equally spaced curves of figure 24a confirm this relationship.

Although the device of figure 24b has the same levels of injected base current, the associated range of bias (0.44 V to 0.66 V), starts off at a lower level than the 0.56 V of the near ideal transistor. This is due to the large recombination component of base current present on the device tested in figure 24b not seen in the device of figure 24a. The fall-off of β_f seen over this voltage range in figures 21b and 22b is evident in the decreased space between subsequent I_C curves evident at the lower values of I_B.

These curves clearly demonstrate that circuit performance would suffer from operating a transistor with large recombination currents in this regime of bias. The decrease in β_f as base-emitter bias decreases represents a clear limitation to the application of transistors for the amplification of low voltages. These applications would include hearing-aid amplifiers and pacemaker circuits which depend on achieving adequate performance at the lowest possible

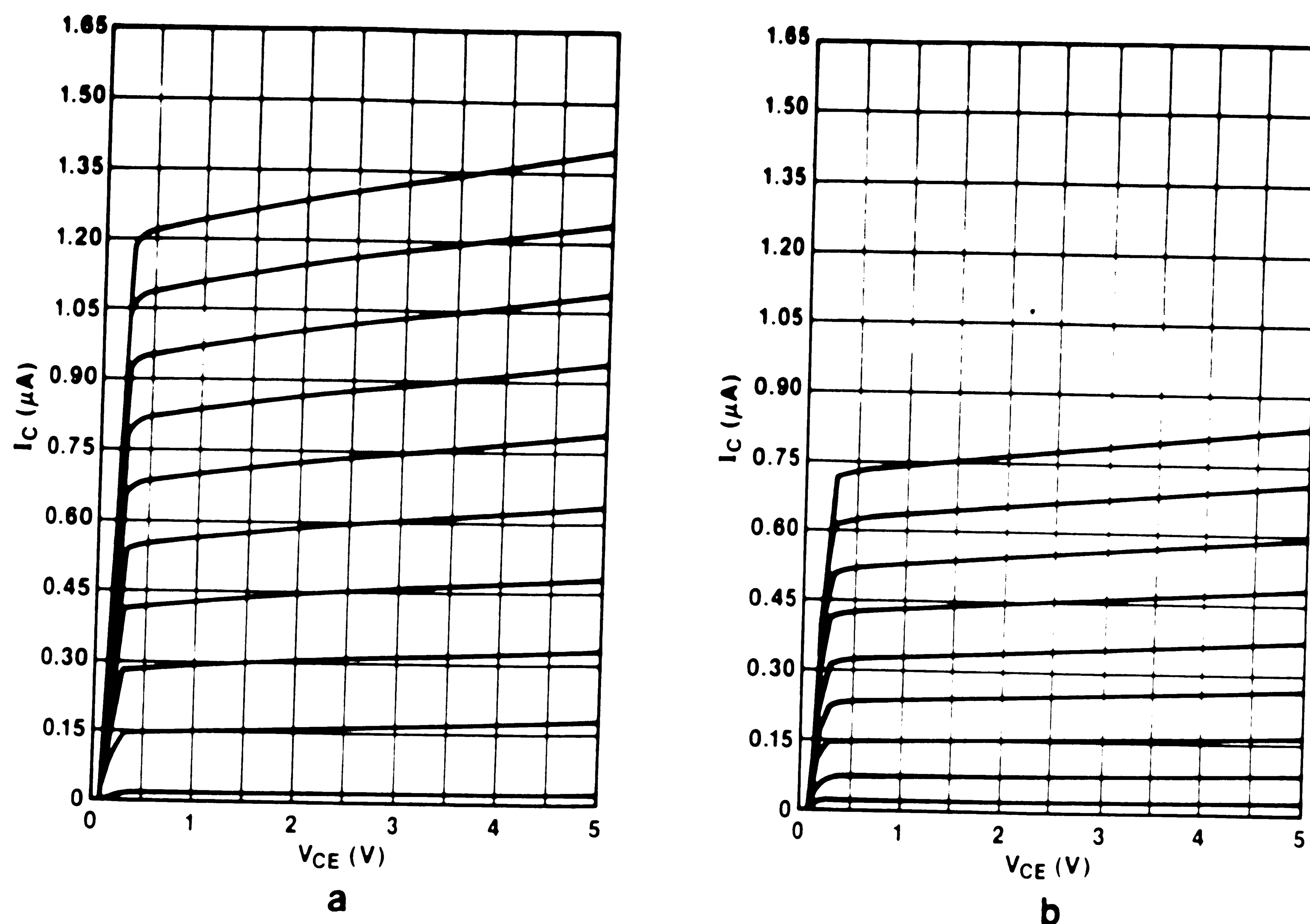


Figure 24. Collector current I_C versus collector voltage V_{CE} for bipolar transistors with a) near ideal current-voltage characteristics and b) significant base recombination current. Base current $I_B = 1.0$nA to 91nA, 10nA steps.

current levels. With large levels of recombination current present, this non-linearity of operation would also extend to intermediate bias conditions and effect circuit performance over a broader range of application.

As discussed earlier, electrically active defects in the emitter-base space-charge region can act as recombination centers for electrons injected from the emitter resulting in higher base currents at low collector current levels and thus accounting for the observed decreased gain. The BiCMOS process flow was examined to identify possible sources of material defects.

The emitter implants were highly suspect. The major advantage of ion implantation technology is the capability of precisely controlling the number of implanted dopant atoms. There can be, however, drawbacks to this technique. Heavier atoms, such as arsenic and the BF_2 molecule, have a large nuclear stopping power. It is the nuclear collisions which transfer

sufficient energy to the lattice so that host atoms are displaced resulting in lattice disorder (damage). When the displaced atoms per unit volume approach the atomic density of the semiconductor, the material becomes amorphous. Within the damaged region, semiconductor parameters such as mobility and lifetime are severely degraded. In order to restore the crystalline lattice and to move the implanted ions into substitutional sites, the semiconductor must be annealed for an appropriate combination of temperature and time. Although the amorphous area recrystallizes in subsequent anneals, there can remain a large density of crystal defects.[40]

Concentrating on the ion implant damage theory, the next two processing lots removed the CMOS p^+ source/drain BF_2 implant from the bipolar emitter. There was also a nitrogen anneal added to the process immediately after the implants to try and negate any damage present at that time. The standard process flow had also changed with the BiCMOS effort now being directed to the analog process. The base drive-in was altered to 950°C 120 minutes followed by an additional 950°C 69 minutes associated with an extra processing step not present in the CMOS core process. As this drive-in cycle was substantially different from the 900°C 60 minutes used in previous characterizations, process simulations were performed to determine an appropriate base dose. The effects of these experiments on the gain (β) versus collector current density (J_C) can be seen in tables 8 and 9.

As can be seen from the data, the standard experimental cells of both wafer lots exhibited the problem. Although the wafers in lot number four received a base dose of 2.8×10^{14} cm^{-2}, yielding an average gain of 126, and wafer lot number five received a larger base dose of 3.2×10^{14} cm^{-2} and a correspondingly lower gain of 65, there is no apparent difference on the β roll-off phenomena with respect to base width. These results are consistent with the data seen on earlier process refinement lots in which transistors made with varying base dose, implant energy, and drive-in schedules all exhibited the β degradation problem.

Experimental Cell	β vrs Jc		β @ 10μa
	Bad	Total Tested	
1 STD	26	68	126±34
2 STD & ANNEAL	8	25	151±39
3 NO BF_2	16	66	296±129
4 NO BF_2 & ANNEAL	9	29	253±115

TABLE 8. Gain and gain versus collector current density for the experimental cells of wafer lot number four - base dose 2.8×10^{14} cm^{-2}

Experimental Cell	β vrs Jc		β @ 10μa
	Bad	Total Tested	
1 STD	31	82	65±10
2 NO BF_2			
2a NO ANNEAL	25	44	116±26
2b ANNEAL	13	36	114±25

TABLE 9. Gain and gain versus collector current density for the experimental cells of wafer lot number five - base dose 3.2×10^{14} cm^{-2}

Removing the BF_2 implant from the emitter region did not impact on the occurrence of the β versus J_c phenomena. It was quite evidently not the source of the extra recombination centers theorized to be at the root of the gain degradation problem.

It was also theorized that the added anneal may be more effective in recrystallizing the implanted surface than the normal thermal cycle of the 1.75μm design rule process. Once again, the data shows no advantage in adding the annealing operation to the process flow. These results hold true with and without the BF_2 implant present in the bipolar emitter.

Although none of the preceding experiments managed to correct the β fall-off problem, it was still believed the original premise of crystalline defects was correct. The theory that crystalline defects, induced by processing, were responsible for the large base currents observed in testing continued to drive the next investigations.

Previous experiments had eliminated the BF_2 implant as the cause of the problem, so attention was now shifted to the remaining arsenic and phosphorus. A relatively straight forward process change would be to eliminate, one by one, the CMOS source and drain implants from the bipolar emitter. As BF_2 had been removed in earlier experiments, one experimental cell now eliminated the graded phosphorus implant leaving the arsenic and BF_2 in the emitter. Another experimental cell further removed the BF_2 so that the emitter structure now contained only the arsenic implant. With these experiments, no other changes were made to the Twin Tub CMOS process. Since changing the net emitter doping changes the emitter junction depth, the bipolar characteristics are significantly affected. Each proposed experiment was modeled with the BICEPS process simulation program and a range of implants selected to better insure obtaining a functional bipolar transistor.

Another set of experiments focused on the lower energy arsenic implantation of the LDD CMOS source and drain into bare silicon. There were two areas of concern, first was the issue of implanting through a screen oxide and second the energy of the implants. In the "NO S/D OXIDE" (no source and drain oxide) experiment the p^+ implant was separated with an extra mask step, the source and drain screening oxide removed and the bipolar emitter implanted at lower energies. One group of wafers received the normal dose of arsenic and phosphorus used to grade the CMOS *n*-channel junctions while the second group received only the arsenic implant. Each of these experiments were once again modeled and split over a range of base implants to increase the probability of obtaining functional transistors.

The next experiment added an oxide spacer to the transistor structure, again implanting the

dopants at a lower energy into bare silicon. It was believed there may be some beneficial effect to the presence of the spacer during the emitter implants with respect to the creation of defects along the edge of the polysilicon layer. As the spacer formation was expected to have no effect on the effective base width of the device, the base implant doses used were identical to those of the previous experiment.

As is customary with each lot of wafers processed, there is also a group of wafers receiving the standard defined process. The results of these experiments with respect to the gain fall-off problem are summarized in table 10.

Wafers were completed with functioning transistors in each of the experimental cells. With the rather substantial deviations from the standard process used in some of the experimental cells this result, by itself, is quite remarkable. What is even more dramatic is the common theme presented by the test results; whenever the CMOS graded phosphorus implant is removed from whatever process listed in table 10, the transistors do not have a gain fall-off problem. This says that implanting the emitter through the screening oxide, the lower implant energy used or the LDD oxide spacer do not play the deciding role in causing the large base recombination currents observed. These experimental cells with the phosphorus removed are the first wafers to be processed without the β fall-off observed on some number of test sites.

Although the various experiments had achieved their goal of identifying the source of the β degradation problem, there now remained the problem of integrating a viable solution into the CMOS process. If solving the problem with the bipolar transistors altered the CMOS characteristics, or added such complexity as to make the BiCMOS process too costly, then one problem has been merely replaced by another. With these constraints in mind, the data of the last set of experiments was further examined. Since good devices were obtained by implanting the emitter through the source and drain screen oxide, there is no reason to perform an extra etch to remove the oxide and risk any adverse effects by doing so. This same argument

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Experimental Cell & Base Implant	β vrs Jc		β @ 10μa
	Bad	Total Tested	
1 STANDARD 2.8×10^{14} cm^{-2}	9	17	51±08
2 NO PHOSPHORUS			
2a 3.5×10^{13} cm^{-2}	0	5	174±11
2b 5.5×10^{13} cm^{-2}	0	12	93±05
3 ARSENIC ONLY			
3a 5.5×10^{13} cm^{-2}	0	12	126±06
3b 7.5×10^{13} cm^{-2}	0	11	91±05
4 NO S/D OXIDE			
4a ARSENIC + PHOSPHORUS			
4a.1 3.7×10^{14} cm^{-2}	12	15	49
4a.2 4.5×10^{14} cm^{-2}	10	12	32
4b ARSENIC ONLY			
4b.1 5.5×10^{13} cm^{-2}	0	17	160±24
4b.2 7.3×10^{13} cm^{-2}	0	17	120±14
5 NO S/D OXIDE + SPACER			
5a ARSENIC + PHOSPHORUS			
5a.1 3.7×10^{14} cm^{-2}	5	11	60
5a.2 4.5×10^{14} cm^{-2}	5	10	34
5b ARSENIC ONLY			
5b.1 5.5×10^{13} cm^{-2}	0	11	166±25
5b.2 7.3×10^{13} cm^{-2}	0	16	105±24

TABLE 10. Gain and gain versus collector current for the experiments on wafer lot number six

applies to the much more complex spacer processing sequence which, never being a viable Twin Tub III BiCMOS process, was performed solely to gain insight into the gain fall-off phenomena.

Of the processes that have produced good gain characteristics, the straight forward removal of the CMOS graded phosphorus implant from the bipolar transistors is the most acceptable process. Although this would mean adding the cost of an additional reticle and another

photolithographic step to the process, there is the advantage of having no impact on the CMOS devices.

The next set of experiments was designed to insure the successful results found by removing the phosphorus implant from the emitter would be repeated. So, once again, there is a standard process cell for comparative purposes and one with no phosphorus in the emitter area.

One additional thought was also pursued. After the growth of the screen oxide, the CMOS source and drain sequence performs a photolithographic operation opening the *n*-channel devices to the *n*-dopants. The arsenic is implanted first, immediately followed by the graded phosphorus. It was postulated that the n^+ arsenic implant, by means of the heavy atomic mass and large dose, was making the silicon surface amorphous. Therefore, the phosphorus implant does not see a crystalline surface, but is placed into an environment with extensive damage. It was thought there may be some advantage to performing the lighter atomic mass and dose phosphorus implant first, following with the arsenic. If this reversal of sequence of the emitter implants worked it would be an elegant no cost solution to the gain degradation problem.

The results of these final experiments are displayed in table 11.

The standard processing cell again shows the presence of the β degradation while the transistors fabricated without phosphorus in the emitter region all tested with a flat gain response. There does not, however, appear to be any advantage to implanting the phosphorus before the arsenic.

3.4 Determination Of New Base Parameters

Once the problem of the β fall-off had been eliminated, other aspects of the BiCMOS process could be examined. The analog CMOS design community had expressed the greatest

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Experimental Cell & Base Implant	β vrs Jc		β @ 10μa
	Bad	Total Tested	
1 STANDARD 100keV 2.8×10^{14} cm^{-2}	3	17	79±9
2 NO PHOSPHORUS 100keV 5.5×10^{13} cm^{-2}	0	42	87±6
3 PHOSPHORUS IMPLANTED 1ST 100keV 2.8×10^{14} cm^{-2}	3	24	69±9

TABLE 11. Gain and gain versus collector current for the experiments investigating β fall-off on wafer lot number seven

interest in the BiCMOS process. The analog process, like BiCMOS, is an add-on to the digital CMOS core. Capacitors and resistors are formed with the addition of a second polysilicon layer prior to gate level processing. The combined bipolar analog CMOS process is detailed below.

The standard CMOS process is followed through field oxidation and the threshold adjust implant performed through the sacrificial gate oxide. Base level photoresist is applied and exposed such that the bipolar thin oxide areas are open in resist. The boron is then implanted at 100 keV with a dose of 5.5×10^{13} cm^{-2} and the masking photoresist removed. A nitrogen drive-in at 950°C for 120 minutes activates the dopant and sets the junction ahead of the subsequent emitter. With the analog process, a polysilicon layer is now deposited (poly0) and doped with phosphorus. The poly0 level is then patterned and etched, the residual sacrificial oxide removed and the gate oxide grown. Polysilicon is again deposited (gate level poly or poly1) and doped with phosphorus. After definition of the gate level polysilicon the source and drain screening oxide is grown. Photolithography is performed to open the CMOS *n*-channel devices and bipolar emitter and collector areas to the arsenic implant. With the new BiCMOS process the photoresist is now removed after implantation and reapplied to expose

only the CMOS *n*-channel devices to the graded phosphorus implant. After this photoresist is removed the wafers experience the blanket BF_2 p^+-source/drain implant and the normal CMOS process continues.

As discussed earlier, it is important to drive-in the base implant with an inert ambient prior to it seeing an oxidation to insure good junction characteristics. The first oxidation after the base implant in the BiCMOS process is the MOS gate level oxide. Examining the analog process reveals there is a thermal drive-in associated with the doping of the poly0 level that occurs after the base implantation and prior to the first oxidation. The polysilicon is doped in an atmospheric pressure furnace tube at 950°C for a total cycle time of 69 minutes. The ambient can be considered inert since the surface is completely covered with the polysilicon. Since this time and temperature are very similar to that used in earlier experiments, it was decided to investigate using this function as the bipolar base drive-in. By this method a process step is saved thereby helping to offset the negative impact of having to perform the extra photolithographic step at n^+-source and drain. Model files were created for the shortened process, run through the BICEPS simulation program and base implant doses selected. The results of the experiment are shown in table 12.

The center dose of $6.0{\times}10^{13}$ cm^{-2} most clearly approximates the gain achieved with the standard cell. This was the base dose indicated by the process simulations as being correct for the shortened process. As is common in experimentation, doses greater than and less than the simulated doses were used to better insure obtaining data in the range of interest and to characterize the process. Since the process simulations indicated it was feasible to use the dose obtained with the longer base drive of the standard process, it was included in the experiment. Thus the effects of the shortened base drive-in can be seen directly in the data of cell 6a where the identical implant dose was used for both processes. Although the "No Phosphorus" standard cell sees an extra 120 minutes at the 950°C drive-in temperature, the effects on the

Experimental Cell & Base Implant	β @ 10μa	Breakdown Voltages			
		BVceo (V)	BVces (V)	BVcbo (V)	BVebo (V)
5 NO PHOSPHORUS 5.5×10^{13} cm^{-2}	87±6	12.2±0.3	17.5±0.1	17.6±0.1	6.4±0.04
6 NO PHOSPHORUS & POLY 0 DRIVE					
6a 5.5×10^{13} cm^{-2}	94±12	11.9±0.3	17.0±0.1	17.1±0.1	6.3±0.04
6b 6.0×10^{13} cm^{-2}	88±7	11.9±0.2	17.0±0.1	17.0±0.1	6.2±0.02
6c 6.5×10^{13} cm^{-2}	76±8	12.4±0.3	16.8±0.1	16.9±0.1	6.1±0.02

TABLE 12. Bipolar transistor characteristics of the no phosphorus and no phosphorus poly0 drive experiment

transistor characteristics are not dramatic. As expected, the β of cell 6a is somewhat higher since the effective base width is narrower due to the shorter time at temperature. The bipolar transistor breakdown voltages are not adversely effected by the new processes.

The emitter structure now consists of the CMOS arsenic and BF_2 implants. With the heavier dose arsenic implant overcompensating the boron, it will determine the emitter-base junction characteristics. The characteristicly steep fall-off of the arsenic diffusion profile will now better approximate the step junction assumed in the derivation of the graded base transistor. A plot of β versus the reciprocal base implant dose is shown in figure 25. There is an excellent straight line fit to the data over the range of the experiment.

4. CONCLUSIONS

A process merging a *npn* bipolar transistor with an existing CMOS technology has been described. The number of additional steps was limited to two photolithographic levels and one implant in an effort to achieve a low cost manufacturable product. The process behaves in a predictable manner with respect to base parameters versus the forward-active common emitter-current gain. Devices were manufactured with current gains in the desired 50 to 100 range. These transistors had acceptable break-down voltages and were fabricated with no changes to the CMOS device characteristics.

The approach taken in combining a bipolar and CMOS process has proved successful. By implanting the active base at the CMOS threshold adjust step and utilizing a subsequent processing step as a thermal drive, no changes occur to the CMOS transistors. Since a moderate performance device is acceptable, the CMOS *n*-well and arsenic n^+-source and drain were utilized as the collector and emitter respectively. The layout of a minimum size *npn* transistor with an associated cross-sectional diagram is shown in figure 26.

The gate level spacer functioned well in separating the inactive base from the emitter. With the emitter junction terminating under an oxide and against the concentration gradient of the active base implant, there is less emitter-base junction capacitance and no problems with surface conduction or low emitter-base reverse bias breakdown volt ages are observed. By extending the gate level spacer to cover the inactive base / field oxide interface, problems with emitter-to-collector punch-through at the emitter periphery are avoided.

Using the CMOS p^+-source and drain implant as an inactive base dopant lowers the base resistance and insures good ohmic contact. By placing a ring of n^+-diffusion completely surrounding the *n*-well, the collector resistance is lowered and latch-up protection is enhanced. The final flow of the BiCMOS process is outlined in table 13.

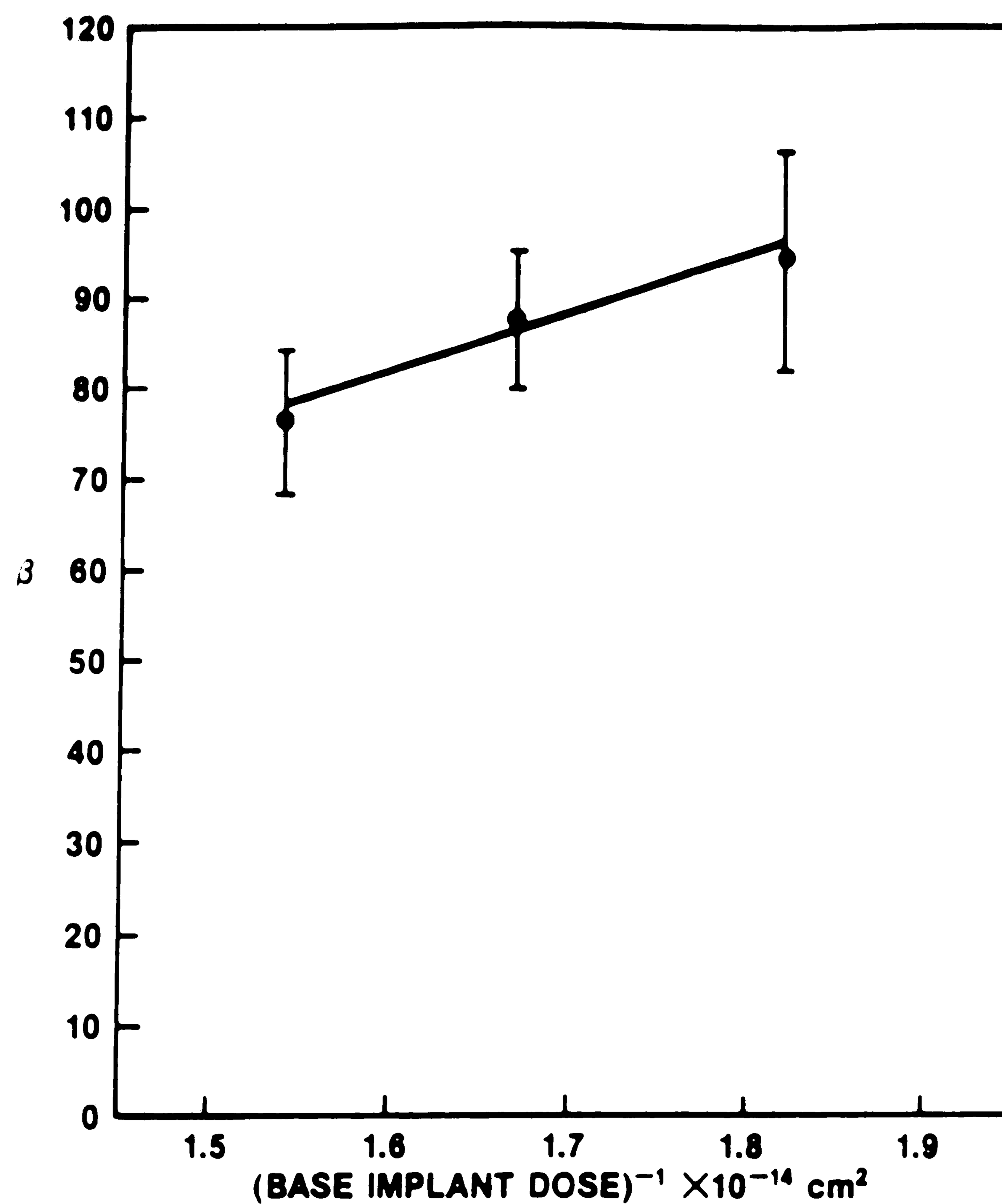

Figure 25. A plot of current gain versus 1 / base implant dose for the no phosphorus and poly0 drive experiment

Modeling equations relating to the process parameters have been presented. The graded base models relating to current gain and implant dose match fairly well with experimental results. The best predictions were made with the arsenic emitter because of its step-junction diffusion profile. Process simulation tools were used successfully with the model equations to select base parameters for experimentation.

The base implant dose has been used to control the base Gummel number. Assuming that the emitter charge is constant, the gain of the bipolar transistor is inversely proportional to the base Gummel number or the base implant dose. The experimental data has been shown to

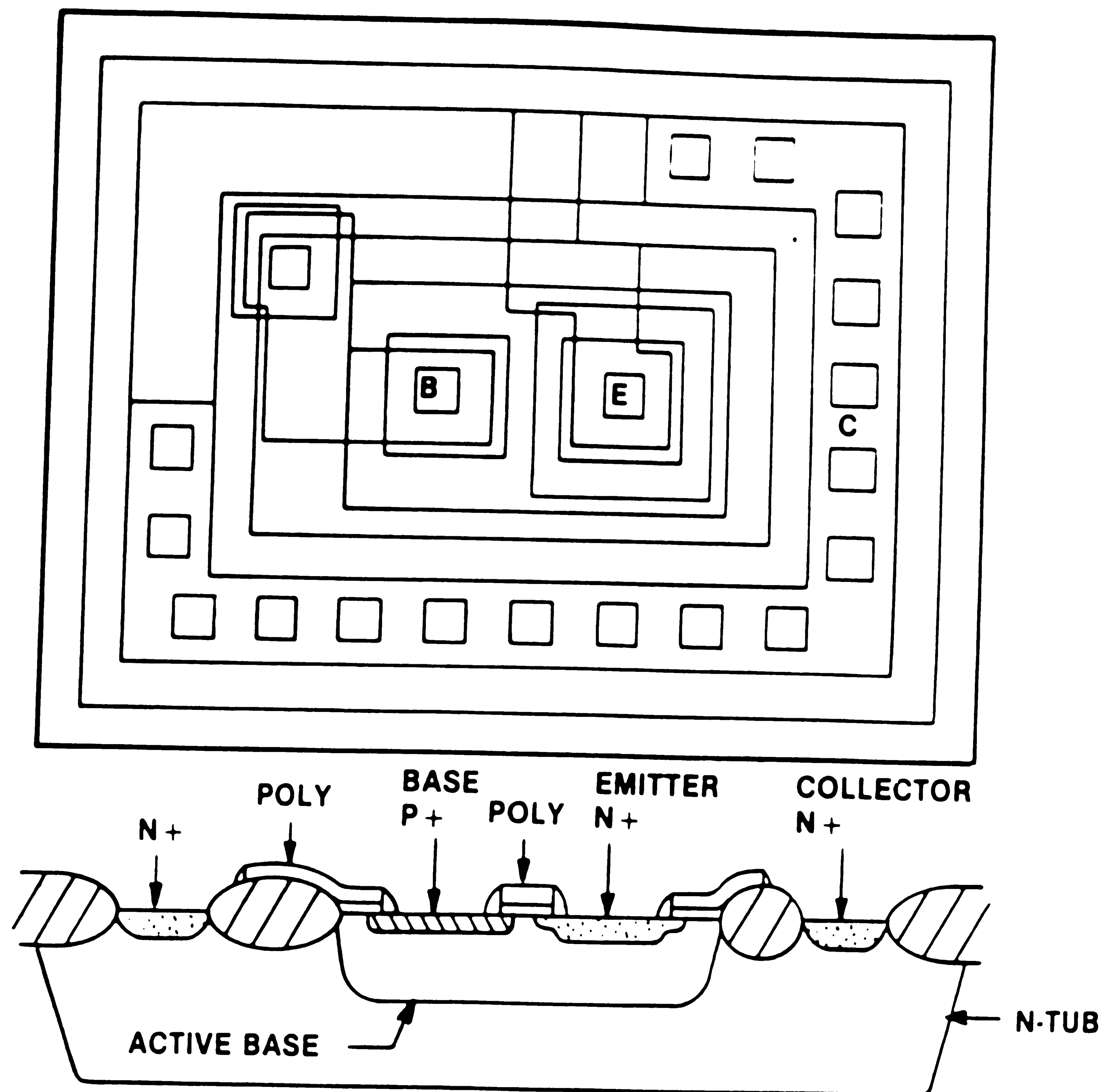

Figure 26. A layout and cross-section of a *npn* transistor

affirm this relationship.

During manufacture a problem with decreased gain at lower collector currents was observed. According to bipolar modeling theory, this behavior was attributed to excess base recombination currents. With the quality of the oxide / silicon interface showing no problems with the CMOS devices, it was felt the excess recombination current was being generated within the emitter-base space-charge region and not at the surface of the device. It was believed there were electrically active material defects caused by processing acting as

CMOS BASELINE FLOW	STEPS FOR BIPOLAR
p^+ Substrate	
p^- Epitaxial Layer	
n-Well With Self-aligned p-Well	(Collector)
Well Drive-in	
LOCOS/Chanstop Isolation	
Threshold Adjust Implant	
	Pattern Base
	Implant Base
Analog Poly Deposition/Definition	(Drive-in Base)
Gate Oxidation	
Gate Deposition/Definition	
Pattern/Implant Arsenic n^+-S/D	(Emitter)
	Pattern Phosphorus n^+-S/D
Implant Phosphorus n^+-S/D	
Blanket Implant p^+-S/D	
Deposit Interlevel Oxide	
Flow Interlevel Oxide/Drive-in S/D	
Define Contact Windows	
Deposit/Define Metalization	

TABLE 13. Final process flow of the Twin-Tub III BiCMOS technology

recombination sites within the space-charge region.

Several experiments were conducted before it was determined that the graded phosphorus implant of the Twin Tub CMOS III process was the determining factor. Since there is a long history of bipolar devices manufactured with implanted phosphorus emitters, it was felt that this implant, by itself, was not the cause of the recombination centers. Experimental evidence with this process shows emitter structures implanted with arsenic alone or in conjunction with the CMOS BF_2 implant produce good bipolar transistor characteristics. The conclusion therefore is that the combination of arsenic and phosphorus lead to the observed problem.

Although beyond the scope of this work, the joint implantation / diffusion of arsenic, phosphorus and boron (from BF_2), reflect some interesting interactions.

From similar work done on the Twin Tub IV CMOS process, bipolar devices have been made with emitters containing arsenic and phosphorus. The phosphorus is used in the lightly doped drain (LDD) process to provide a conductive path from the CMOS gate to the spacer separated arsenic diffusion. Although performing a similar function in grading the source / drain junction, it is over an order of magnitude lighter dose than that used in the Twin Tub III technology. This would suggest there may be some threshold amount of phosphorus at which the electrically active defects are formed. The threshold dose would be somewhere between $\approx 10^{13}$ cm^{-2} and 1×10^{15} cm^{-2} where the problem is known to occur. A second explanation is that it may not be the lighter dose phosphorus of the LDD process but that the implant sees a nitrogen anneal prior to the arsenic implant.

The presence of the BF_2 implant retards the diffusion of the other species. The experimental evidence of this effect with the arsenic / phosphorus emitter can be seen in the data presented in tables 8 and 9. With the same base dose and processing, removing the BF_2 from the emitter structure changed the average gain from 126 to 296 and 65 to 116 on the two wafer lots. Having the same base profile, the gain is higher because the emitter diffused deeper yielding a smaller net active base doping. The same effects are also seen in table 10 comparing the "ARSENIC ONLY" and "NO PHOSPHORUS" experimental cells. With a common dose of 5.5×10^{13} cm^{-2}, the "NO PHOSPHORUS" cell (arsenic and BF_2) had a gain of 93 while the "ARSENIC ONLY" emitter yielded a gain of 126. The process simulator did not handle this diffusion retarding effect with great accuracy.

Once the problem of the β fall-off had been solved, a new process flow was formulated and appropriate base parameters determined. Although though the final process is somewhat more complex than desired, it has the advantage of a shallower step-junction like emitter which is

more straight forward to model, should have a tighter distribution of gains during manufacture and have a somewhat lower collector resistance.

VITA

Joseph R. Radosevich was born on June 11, 1948 to Rudolph and Inez Radosevich in Baltimore, Maryland. He attended the Worcester Polytechnic Institute in the fall of 1986 and graduated with a Bachelor of Science in Electrical Engineering in 1970. In that same year, he was employed by the Western Electric Company, transferring to AT&T Bell Laboratories in 1981. Graduate study at Lehigh University was begun in the fall of 1982.

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