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A direct digital frequency synthesizer :

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**A Direct Digital Frequency Synthesizer:
Theory and Design**

by

Barry L. Kramer

A THESIS

PRESENTED TO THE GRADUATE COMMITTEE

OF LEHIGH UNIVERSITY

IN CANDIDACY FOR THE DEGREE OF

MASTER OF SCIENCE

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Lehigh University

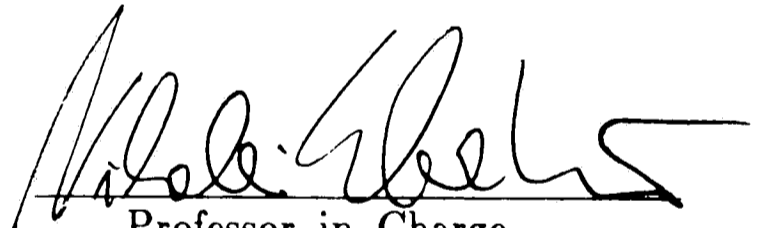
1988

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

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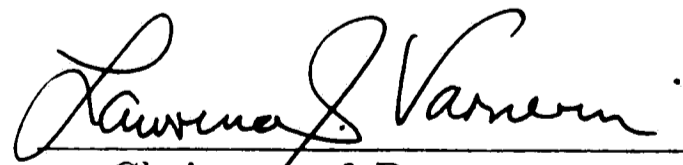

Chairman of Department

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Abstract

This document describes the theory and operation of a circuit to synthesize a sinusoidal waveform for use as a frequency reference. The direct digital frequency synthesizer features extreme stability, frequency accuracy and resolution, a microprocessor-compatible means of setting or rapidly changing the output frequency, and the ability to produce any periodic waveform by simply changing a ROM.

Chapter 1

Introduction and Purpose of Design

Many applications, particularly in the field of microprocessor-controlled and other automated test equipment, require a very accurate yet highly flexible frequency reference. A very good example of such an application, in fact the one that originally led to the development of the circuit on which this thesis is based, arises from the need of cable television system operators to be able to test the quality and characteristics of their signals at various points in the field.

Cable And Local Area Networks, Incorporated (CALAN), manufactures a device unique to the cable television industry. It is a portable unit which permits one to do frequency sweeping and other tests on video signals. By allowing the user to select what frequencies are skipped during sweeps, interference with the video images a customer receives is eliminated, yet complete data on signal strength can be obtained by sweeping at the lower and upper edges of the "area" in question. Other problems, including accidental deactivation of subscription decoders, are eliminated as well.

A direct digital frequency synthesizer (DDFS), using a slow 8-bit digital to analog (D/A) converter, was used in the original design. I was asked to design a new circuit that could directly replace the existing one, yet provide improvements based on a number of priority-ordered criteria, including signal to noise ratio (S/N), maximum operating frequency, frequency resolution, and power consumption. Other factors, including cost and method of construction, were to be considered somewhat less important.

The final design based on these factors was a 1.24 volt (P-P) sinusoidal waveform synthesizer, having a maximum output frequency of 2.1 MHz, signal

to noise ratio of 72 dB, power consumption not to exceed 2000 mW, and able to change output frequency on command by a microprocessor. The DDS is imbedded in a phase-locked loop (PLL) frequency multiplier circuit that generates the video frequency final output. The PLL arrangement multiplies the DDS output by a factor of 285.714, so to produce the specified 150 Hz frequency resolution at the output (needed for a future application), the DDS output needed to be programmable in 0.525 Hz increments. For simplification, this figure was rounded to 0.5 Hz.

This circuit as designed would operate to these specifications. However, due to board layout constraints, it was operated at one-quarter and one-eighth the 8.4 MHz clock speed for testing and evaluation purposes. The remainder of the theoretical discussion will continue to assume it will be operated at the rated 8.4 MHz speed, as a properly designed board would result in correct function at that speed. Chapter 4 will then elaborate on the actual operation at the reduced speeds.

1.1 Theory of Operation

The name *direct digital frequency synthesizer* arises from the nature of the circuit, which produces an analog waveform from a digital representation through use of a digital to analog converter. The output frequency is a simple function of a single necessary *clock signal*, used as a time reference. Recent advances in integrated circuit technology, particularly the availability and features¹ of the extremely fast Advanced CMOS logic family, high speed converters, as well as the decreasing cost of larger, faster Read-Only Memories (ROMs) have made direct digital frequency synthesis more useful. Frequency limits, previously on the order of 100 KHz, are now well into the MHz range,

and the availability of 16-bit digital to analog converters (DAC's) allows signal to noise ratios as good as 96 dB.

Because the direct digital frequency synthesizer uses previously-generated finite-precision representations of the output waveform, it is appropriate for use at any time a periodic waveform is required. A computer program, using any desired algorithm or mathematical equation, is normally required to make this representation. Since a sinusoidal signal was needed in this application, a simple Pascal routine utilizing a built-in function adequately served the purpose. By proper selection of the method of digitization, and the amount of memory in the DDFS, an output waveform of essentially any quality can be produced.

1.2 DDFS Design Theory

In direct digital frequency synthesis, the function $\sin(\omega t)$ is approximated by outputting the function $\sin(\omega nT)$ ($n = 0, 1, 2, \dots$) where T is the rate at which digital words are converted in the D/A converter; $\frac{1}{T}$ is the clock frequency f_c .

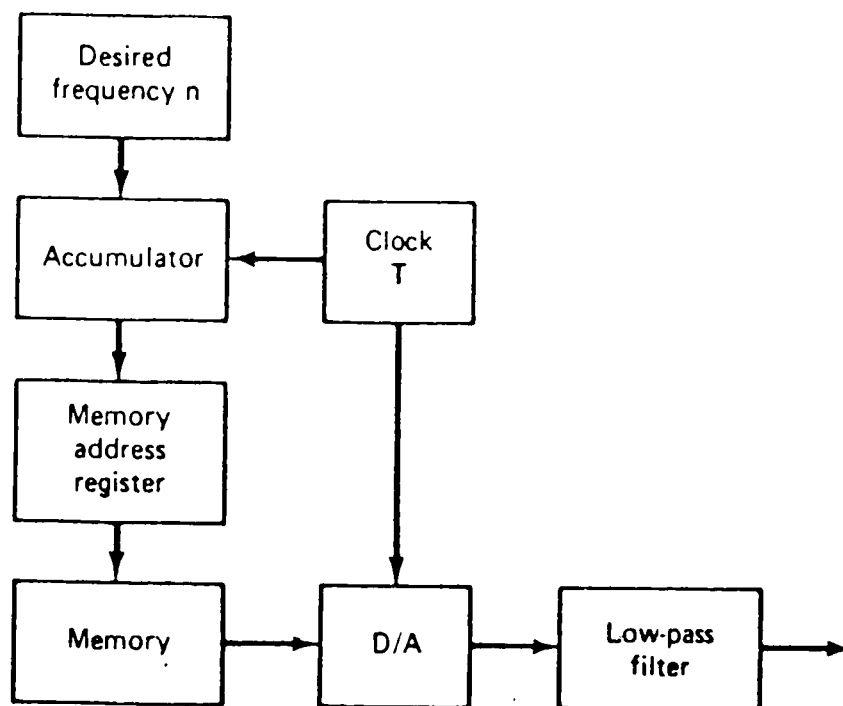


Figure 1-1: Block Diagram of a Direct Digital Frequency Synthesizer

The functional block diagram of a direct digital frequency synthesizer can be seen in Figure 1-1.

The output of the converter is an exact sinusoid corrupted with deterministic noise due to the truncation caused by the finite length of the digital words. An n -bit word applied at the input of the DAC will produce a worst-case noise power due to truncation of $\sigma^2 = \frac{1}{2^n - 1}$ or $-6(n - 1)$ dB.² For each bit added to the input word length, the spectral purity improves by 6 dB. One must then select a DAC having enough data inputs to meet the design requirement. In this design, $n=12$ bits are required to obtain the required 72 dB S/N.

Another consideration when selecting a DAC is that it must be able to convert input words to output voltages sufficiently fast. Since at the highest frequency, a minimum of four points in the desired output waveform must be converted to obtain an accurate reproduction, the DAC must be able to be clocked at least four times the maximum frequency needed at the output, and its output must become stable before the next clock pulse occurs, since at that time the input word may change. Otherwise, the output will contain many harmonics of the generated frequency which will not be removed sufficiently by the low pass filter that follows the output.

1.3 Frequency Select Block

A frequency control number must be presented at the input of the accumulator. This number, typically referred to as K , will uniquely determine the frequency that will appear at the output. In the synthesizer implementation, this number is binary and has no more than two bits less than the accumulator does. The reason for this is explained in the next section. The frequency control number represents a phase-angle increment which is added

to the contents of the accumulator at each clock time. Recall that since the synthesized waveform is periodic, the phase-amplitude relationship applies.

1.4 Accumulator

The phase accumulator is perhaps the most important part of the design in that it determines the frequency range and resolution of the system. It is implemented as a set of latches holding N bits. This N -bit binary accumulator's purpose is to store (and present to the next block) the phase of the wave shape at any point in time. At each clock time, the frequency control number K is added to the contents of the accumulator, and the result is placed back into the accumulator. In this way, a digital frequency control number K will shift the phase of the accumulator output by $\frac{2\pi K}{2^N}$ radians per clock cycle. Figure 1-2 and Section 1.5 aid in the understanding of the concept of how phase is relevant in this design.

Since a minimum of four points will be taken per cycle of the generated wave (see section 1.2), the frequency control number must always have a value of not more than a quarter of the accumulator's maximum value. This corresponds to a binary number representable with $N - 2$ bits. Of course, if the synthesizer did not need to operate at that high a frequency, correspondingly fewer bits in the control number would be needed.

As the contents of the accumulator are increased, it will periodically overflow. This occurs corresponding to a phase change from 359 to 0 degrees. The rate of overflow is equal to the output frequency f_0 . The following equation relates the output frequency to the clock frequency, accumulator length, and frequency control number K : $f_0 = \frac{Kf_c}{2^N}$

Since K can only have discrete integer values, the output frequency is an integer multiple of $\frac{f_c}{2^N}$. This value is termed the *frequency resolution* of the system. Clearly, the frequency resolution is also the lowest nonzero frequency which can be produced ($K = 1$).

By selecting a clock frequency of four times the maximum output frequency, one is able to immediately determine the accumulator length needed for any resolution. In this design, the accumulator length N is 24, the minimum value required for $\frac{f_c}{2^N} \leq 0.5$ Hz. Recall that since f_0 was specified in the design (Section 1) as 2.1 MHz, $f_c = 4f_0 = 8.4$ MHz.

1.5 Phase to Amplitude Converter

This block is essentially a read-only memory (ROM) that is programmed to contain amplitude information representing the desired waveform. To address the ROM by M bits is equivalent to dividing the 0-to-360 degree phase circle (see figure 1-2) into 2^M parts.³ The exact angles stored in the ROM are not important; they must, however, be uniformly spaced. The program used to generate the ROM programming data stores the entire sine wave in ROM with the 0° value at address 0 and the 360° value at address 16383, the highest possible value for the ROM chosen. The value of the number stored at any location is given by the equation $\sin \left[2\pi \left(\frac{\text{address}}{\text{highest address}} \right) \right]$ first shifted by +1 so the result is nonnegative, and then scaled by 2^{n-1} . The scale factor is not 2^n because the sine term has a maximum value of 2 and could not be digitized into only n bits if scaled that much.

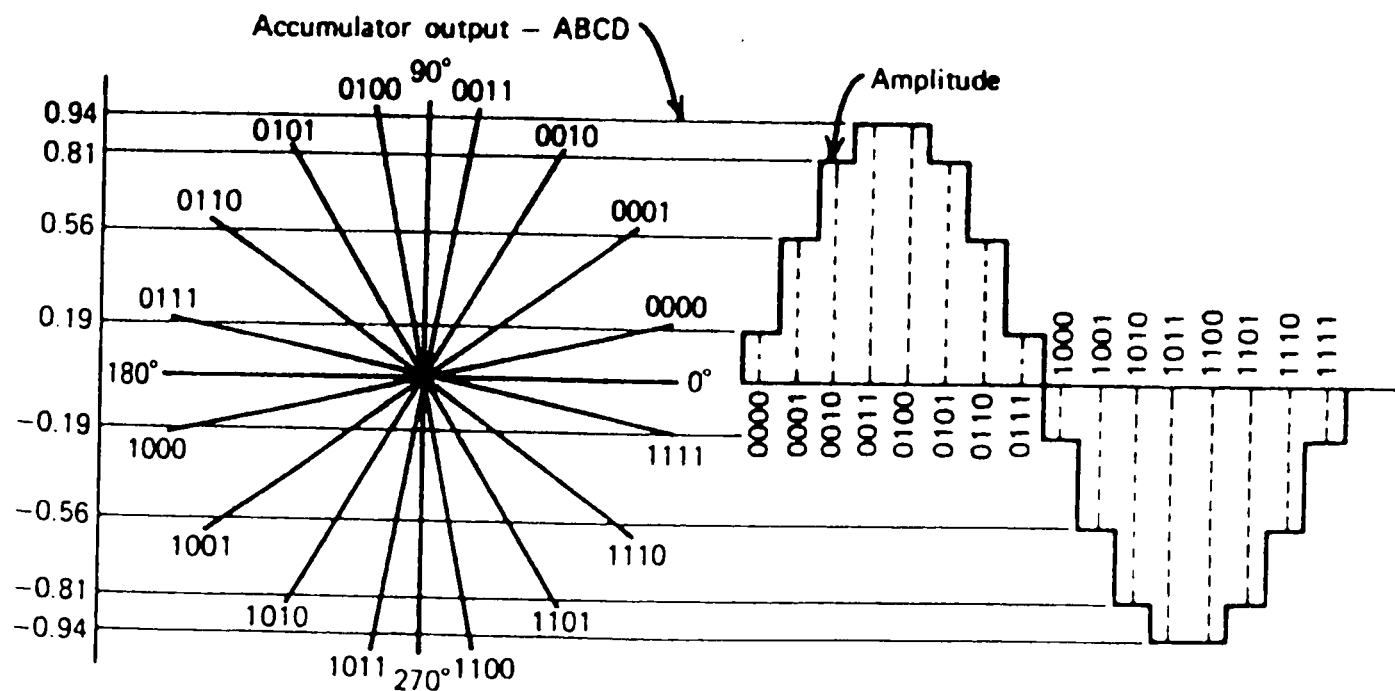


Figure 1-2: 4-bit synthesized sine waveform.

1.5.1 Memory requirements

It has already been shown that ROM width is determined by system signal to noise ratio requirement. A specification must now be developed for ROM length requirements.

Figure 1-3 shows how the generated sinusoid is made up of discrete points. The number of points P in the lowest frequency waveform which can be generated is clearly the number of conversions made in the time it takes to traverse all 360° of the wave. Mathematically, incrementing the accumulator by the lowest possible value each cycle, $\frac{f_c}{2^N}$ increments (and conversions) occur before the output has seen a full cycle and the accumulator has overflowed (assuming it started in a zero state). In the strictest implementation of the DDFS, where there is a memory location for each digitized point of the sinusoid, this is the number of words of amplitude information which must be stored in memory for presentation to the converter. However, when the output waveform has symmetry, or when spectral purity requirements are not extremely severe, it is possible to substantially reduce the length of the memory from this

value. Address lines of ROMs are always connected to the high order bits of the accumulator.

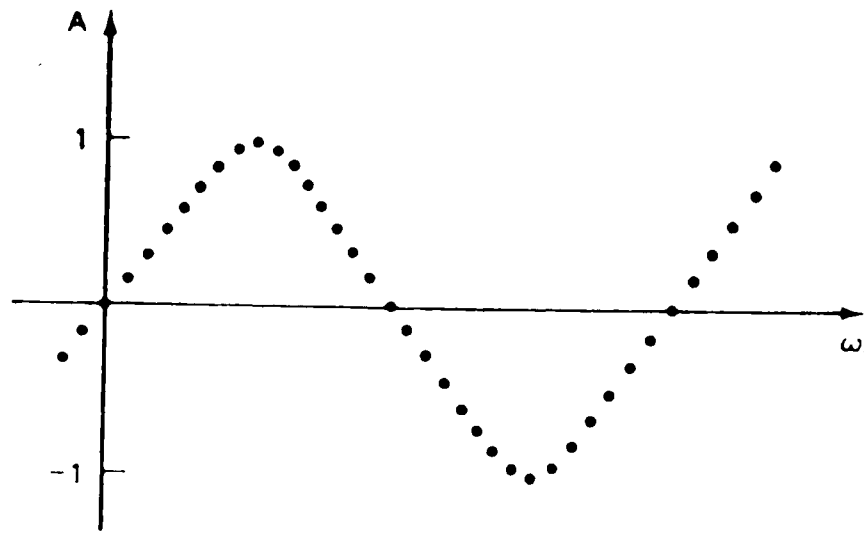


Figure 1-3: Digitized sinusoid.

1.5.2 Reduction of required memory by relaxed spectral purity

This design specified a spectral purity of 72 dB, corresponding to 12 bit digitization of the sinusoid. Because this is not extremely severe, memory can be reduced until there are just enough locations such that no two adjacent digitized points differ by more than one bit in amplitude. This restriction prevents undesirable harmonic content in the output.

Since for a sine wave, $\frac{dy}{dx}$ is a maximum at zero, if the first two points in memory are only one bit apart, the memory is sufficiently large. 12 bit digitization, as mentioned in section 1.5, gives a scale factor of 2^{11} . Solving $2^{11} \sin\left(\frac{2\pi}{\text{maximum address}}\right) \leq 1$ one finds that the highest address must be at least 12867.96. The smallest standard memory with at least that many locations is a 16K. Symmetry, as discussed in the next section, can further reduce this requirement.

when the signal is in quadrants III and IV. Note also that his implementation must use a DAC whose inputs accept sign-magnitude format, and also that the inverter on the MSB is not needed for the circuit to operate (although its removal makes the table of values in his text invalid).

Even though the addition of logic to reduce memory requirements may be possible due to symmetry of the generated waveform, there are circumstances where it is not wanted. When overall power consumption is to be minimized and there are many bits addressing the ROM and feeding the DAC, as in this design, the addition of logic on all those lines becomes undesirable. A 16K ROM was required in this design if no symmetry was to be exploited. A careful look at the available 4K, 8K, and 16K devices revealed that power consumption was relatively constant over this size range, and the larger memories were not considerably more expensive, so a decision was made to store the entire waveform and completely eliminate the extra logic.

1.6 Digital to Analog Converter

The DAC used in this design is a Brooktree BT105, which features 40ns maximum settling time, 12-bit accuracy, and a registered input. Its fast conversion time was more than adequate for the required 2.1 MHz output, and the 12-bit latch on the input eliminated the need for additional circuitry between it and the ROM. Since the bit outputs of the ROM will not necessarily change at exactly the same time, some type of latch is always needed so the DAC will not have its inputs changing before the conversion can be completed. The advantages of this device are discussed again briefly in Section 3.2.3.

The input word of this device is in straight binary format. All bits

represent amplitude information which increases monotonically as the value of the binary input increases from 0 to $2^{12} - 1$. Other formats for input words include sign-magnitude, 2's complement, and offset binary (all bipolar codes) and 8-4-2-1 BCD (a unipolar code).⁴

The BT105's current and voltage characteristics and required external component values were calculated from the equations given in the data sheet⁵ as follows: range of output $V_x = 1.24$ V (given in specification)

$$R_1 \leq 50\Omega \text{ (given in data, p. 2)}$$

$$\text{select } R_1 = 47\Omega$$

$$\text{by Ohm's law, } I_{\text{out}} = \frac{V_x - 0}{R_1} = \frac{1.24}{47} = 26.383 \text{ mA}$$

$$R_{\text{set}} = \frac{5367}{I_{\text{out}} \text{ (mA)}} = \frac{5367}{26.383} = 203.426\Omega$$

Since the internal voltage reference can vary by 10%, R_{set} was selected as the standard value 220 Ω . Experimental results on the output voltage, presented in more detail in Chapter 4, were actually within 8.9% of the calculated 1.24 volts.

1.7 Low Pass Filter

A low pass filter must follow the current output to remove high frequency noise caused by internal switching in the DAC. The cutoff frequency of this circuit is to be $\frac{f_c}{4}$ for maximum effectiveness yet acceptable attenuation of the highest frequency outputs.

Although active filtering is possible, the high gain-bandwidth product needed makes it very difficult to find suitable devices at this time. Using the equations for design of first order passive low-pass filters (which follow), a simple RC circuit (see Figure 1-5) was developed:

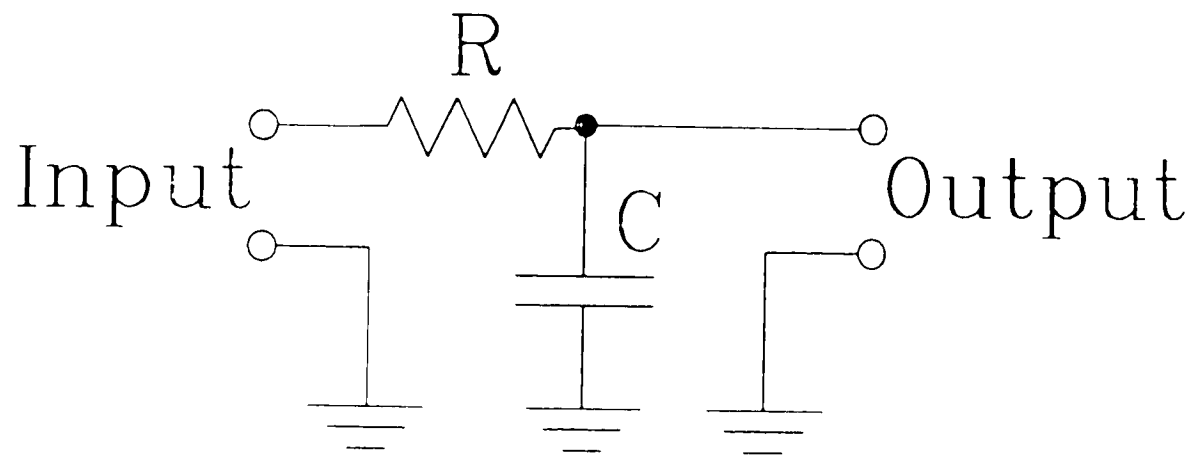


Figure 1-5: First order LPF for filtering DAC output.

$$\omega_0 = 2\pi f_0 = 2\pi (2.1 \times 10^6) = 1.3195 \times 10^7$$

$$\omega_0 = \frac{1}{RC} \text{ or } R = \frac{1}{\omega_0 C}$$

Table 1-1 shows the R values calculated by setting C to some standard values. Several RC combinations were used; this data appears in Section 4.5 and the frequency response of the filter demonstrating the best characteristics (marked with an asterisk in the table of values) appears in Figure 4-14. This is discussed in detail in Section 4.5.

Low Pass Filter Component Values			
C	R (1.05 MHz clock)	R (2.1 MHz clock)	R (8.4 MHz clock)
0.01 μF	60.632	30.315	7.579
0.005 μF	121.264	60.632	15.158
0.001 μF	606.304	303.152	75.788
* 2000 pF	303.152	151.576	37.894
1000 pF	606.304	303.152	75.788
470 pF	1290.00	645.004	161.251
330 pF	1837.28	918.640	229.66
220 pF	2755.92	1377.96	344.49
100 pF	6063.04	3031.52	757.88
47 pF	12900.1	6450.04	1612.51
18 pF	33683.5	16841.76	4210.44

Table 1-1: Table of some possible values for components in the first order LPF, which were tested during evaluation.

Chapter 2

Digital to Analog Converters

2.1 Types of Converters

There are four major ways for manufacturers to implement D/A converters.⁶The first two, the *Weighted Resistor* variety and the *R-2R Converter* normally have voltage outputs (and are inherently slower due to finite gain-bandwidth of the output amplifiers present within the devices). The *multiplying* converter as well as the *current-steering* variety may have either current or voltage outputs.

2.1.1 Weighted Resistor D/A Converter

The weighted resistor converter operates by selectively closing a set of switches, which applies a voltage reference, often internal, through an appropriate number of binary-weighted resistors to a summing amplifier at the output. This is presented in Figure 2-1. Internally, such a device has one switch and one resistor for each bit, a reference voltage generator, and a summing element (typically an operational amplifier).

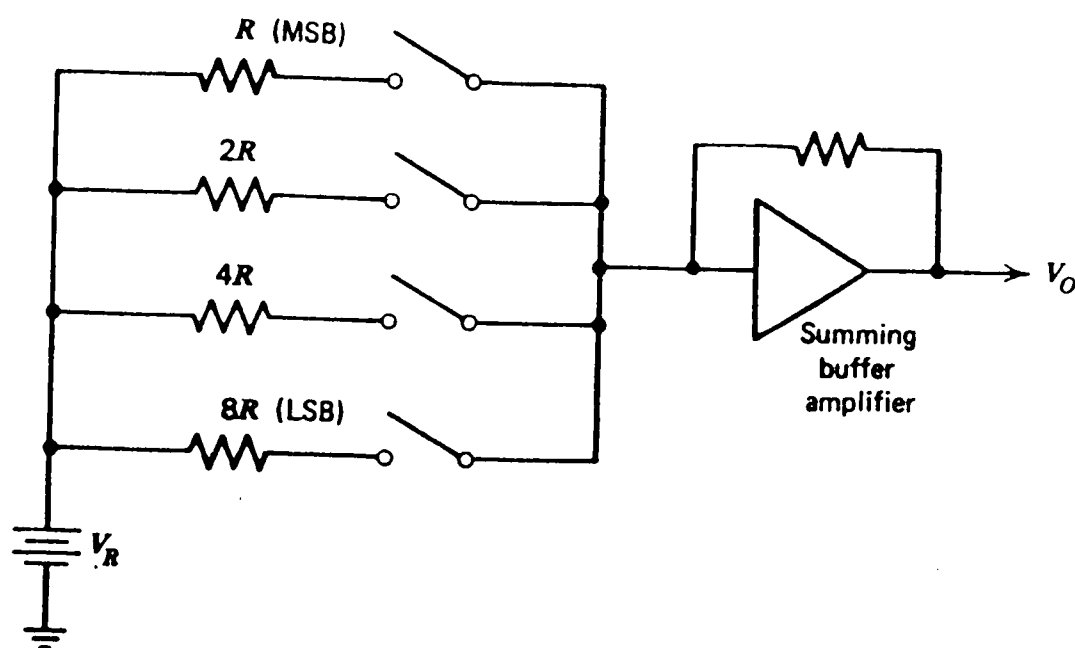


Figure 2-1: Weighted resistor D/A converter's internal arrangement.

In this example, a switch is closed if the appropriate input bit is a 1; otherwise the switch remains open. When a switch closes, current flows into the summing node. The amount of current is greatest for the msb and decreases by a factor of two for each lower order bit.

For the purpose of analysis of this type of converter, one first assumes that the switches have zero resistance when closed, a reasonable approximation for most applications. As shown in the example, the switches have values such as to make the current flow into the summing node proportional to the binary weight of the respective input bit a_i . The resistor in the msb position has the value R and the value is halved for each less significant bit. The current I flowing into the summing node in terms of the resistances and the reference voltage V_R is $I = \frac{a_{n-1}V_R}{R} + \frac{a_{n-2}V_R}{2R} + \dots + \frac{a_1V_R}{2^{n-2}R} + \frac{a_0V_R}{2^{n-1}R}$

This equation may be rewritten as

$$I = \frac{V_R}{2^{n-1}R} \left[a_{n-1}2^{n-1} + a_{n-2}2^{n-2} + \dots + a_12^1 + a_02^0 \right]$$

$$= \frac{V_R}{2^{n-1}R} \sum_{i=0}^{n-1} a_i 2^i$$

The highest output current flows when all a_i coefficients are 1 and has value $I_{max} = \frac{V_R 2^{n-1}}{R 2^{n-1}}$

This type of converter is relatively inexpensive although it would not have been suitable for use in this design. In order to have 12-bit resolution, 12 resistor values spanning a range of R to $2^{12}R$ or 4096 times that would be needed in the device. Although new laser trimming procedures allow better control over resistor values during device fabrication, monolithic manufacturing of all 12 values is completely impractical due to the layout area required.

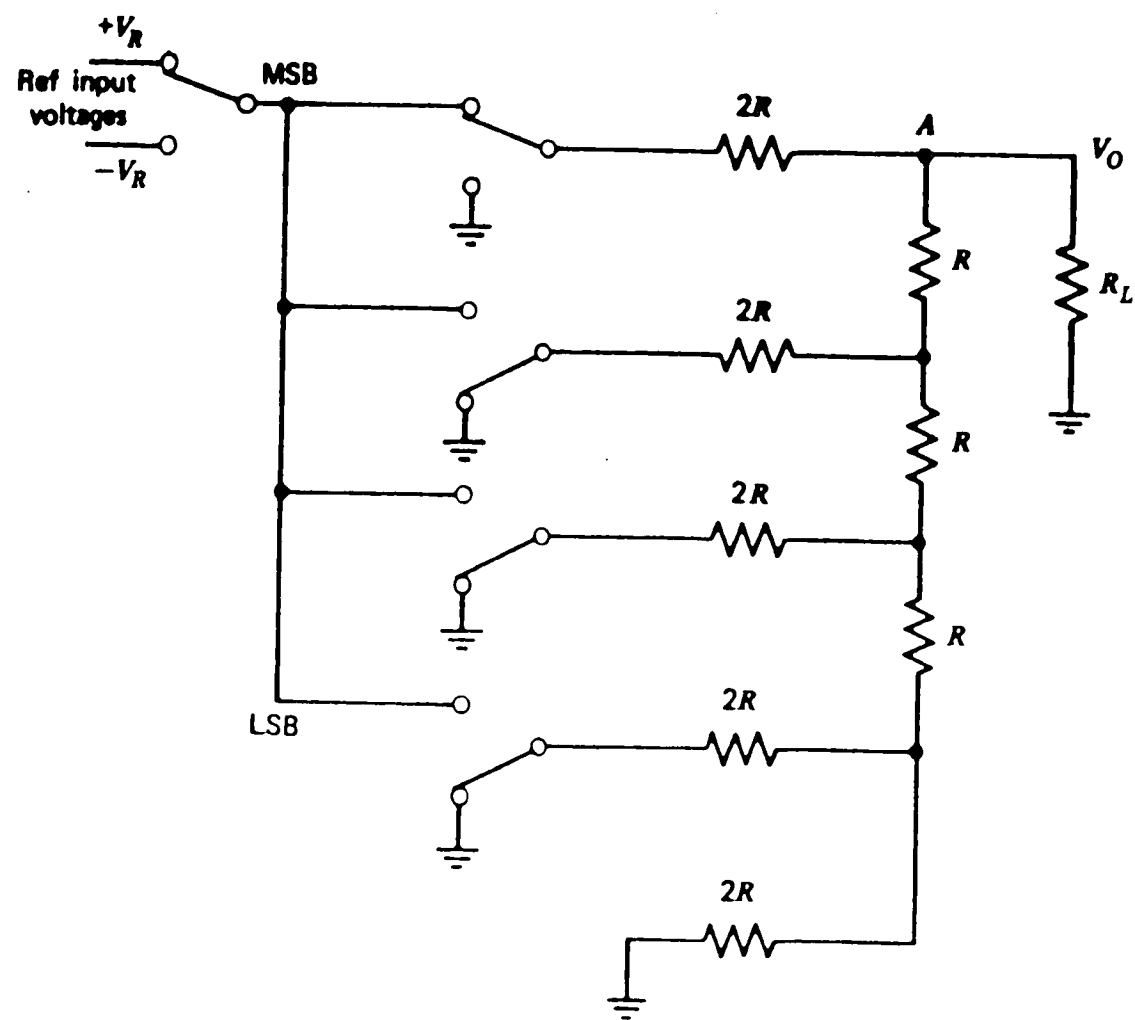
Although external resistors could be used, cost and size are significantly increased, errors in matching component values become involved, different temperature-dependent characteristics of the resistors contribute to inaccuracies, and finally, the summing buffer amplifiers located in these converters are often too constrained by their gain-bandwidth product to operate at the specified frequency.

2.1.2 R-2R Converter

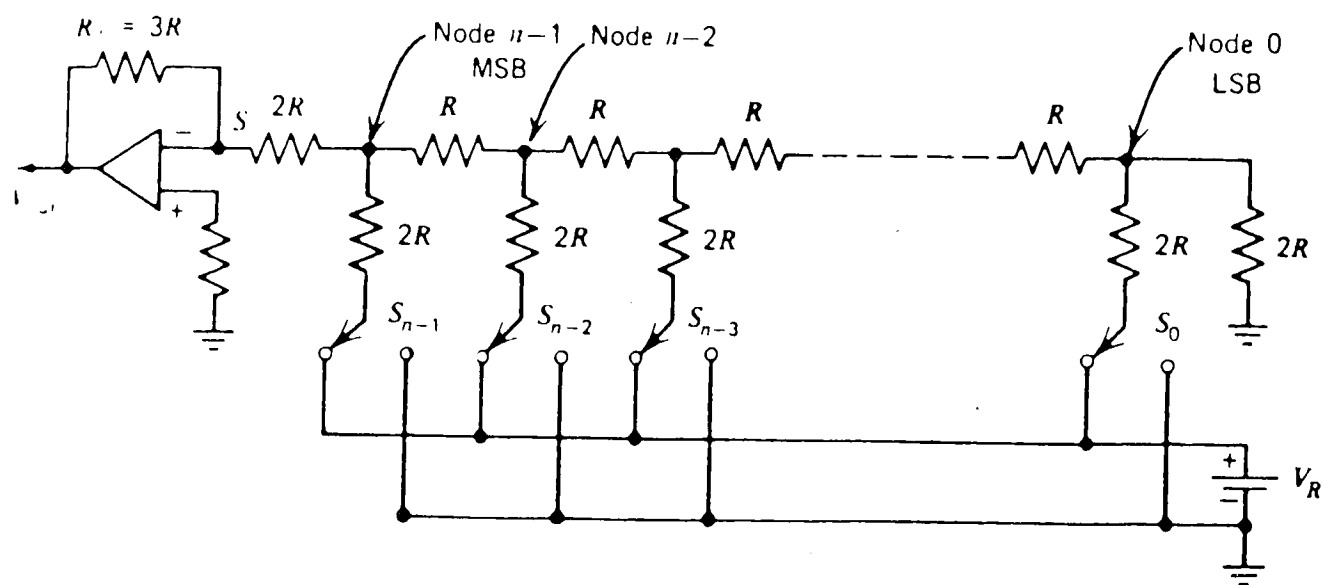
This type of digital to analog converter, which is also referred to as a ladder network, uses only two resistor values in its construction: R and $2R$. The primary advantage of this type is that it is easily constructed monolithically. It does, however, require one more resistor per bit than the binary weighted converter.

Figure 2-2 shows the ladder network used in an R-2R D/A converter. Often, the $2R$ value is constructed of two R values in series. If the converter is to operate over a temperature range, the resistors must be of the same type (in order that they have the same temperature coefficients), and this method works quite effectively in matching components (although it does increase the parts count).

In addition to the usual converter defects of resistor errors and mismatched temperature coefficients, this type is also susceptible to stray capacitance which introduces delay in response, particularly with high resistance values. Low resistance values tend to get errors from voltage drops across the switches. These voltage drops are difficult to match because the switch currents are different, but this is usually only significant in the higher order bits. High accuracy converters are sensitive to noise from both resistances as well as



(a) 4-bit example.



(b) General case.

Figure 2-2: R-2R D/A converter's internal arrangement.

inductive and coupling effects.

The $R-2R$ converters require a larger conversion time for increasing number of bits, because the inductive and capacitive elements in the circuit raise the settling time. Finally, internal voltage reference errors, if present, will directly affect the output. Converters designed for use with a varying externally applied reference (often referred to as the *analog input*), called multiplying

converters, will be more accurate because they do not include reference voltage errors. The accuracy of the signal as applied will directly determine the amount of voltage reference error that will appear in the output.

2.1.3 Multiplying D/A Converter

The multiplying converter has an output directly proportional to the product of the digital input and a variable analog reference voltage. This type of device is useful for such applications as analog display driving or graphic displays where vector multiplications must be generated.⁶

Multiplying converters can be classified as one of four types: one quadrant, two quadrant digital, two quadrant analog, and four quadrant. These categories state the range of permissible digital and analog inputs for which the output remains correct. A one quadrant converter requires a nonnegative analog input and considers the digital input always positive, resulting in a consistently nonnegative output; a two quadrant analog device allows any polarity of analog input and treats the digital input as a proportionality constant; the output of a two quadrant digital one may have the polarity of the analog input controlled digitally but always requires a nonnegative analog input; and a four quadrant device accepts all possible input combinations.

2.1.4 Current Steering D/A Converter

As stated previously, digital to analog converters are available with either current outputs or voltage outputs. The former do not include internal output amplifiers and are not subject to bandwidth restrictions normally imposed by them. DACs of this variety are very suitable to applications where high speed is important, such as in this frequency synthesizer. The device used in this

design is based on a current steering type of architecture.

One of the fastest types of D/A converters are those that use this current steering architecture. These converters use switches controlled by the numerical input to direct current sources to the output or to ground. A complete discussion of this type of DAC follows.

2.2 Detailed Description of Current Steering DAC Architecture

This type of converter is implemented in complimentary MOS technology because, as stated, it operates on the principle of discretely switching current sources. The switching devices are field-effect transistors, and they will connect the current sources either to the output terminal or the ground plane depending on the digital input.

The Brooktree BT105 is a typical high-quality example of a current steering DAC, and it will (as discussed in Section 3.2.3) be used in the physical implementation of this synthesizer. It is a monolithic CMOS device whose functional block diagram is presented in Figure 2-3.

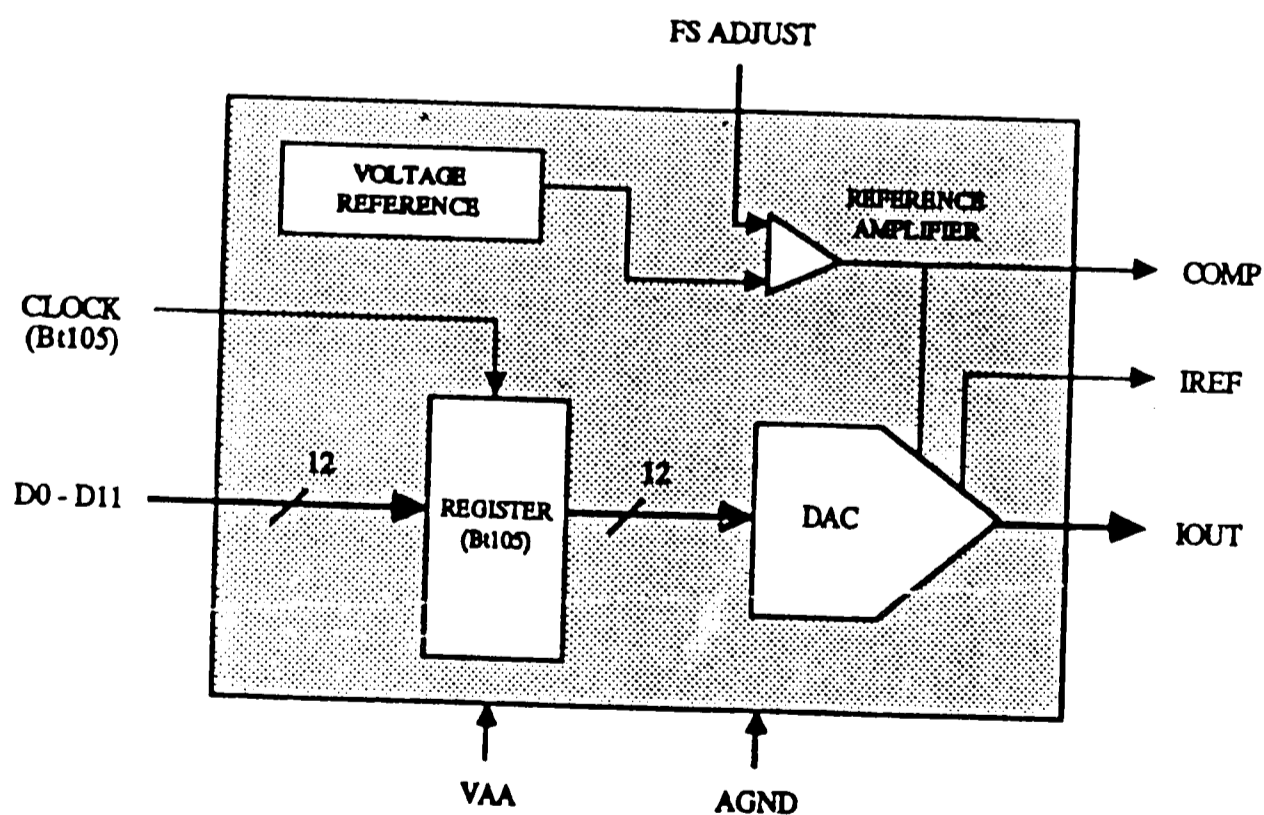


Figure 2-3: Block Diagram of a Current Steering DAC.

Although the internal structure of the device is not discussed in the data other than to state that it is "a segmented architecture in which bit currents are routed to either IOOUT or AGND by a sophisticated decoding scheme," some things are known. The device contains a 12-bit latch which store the digital inputs for conversion between clock pulses. It is likely that it biases a group of internal transistors in their region of operation where they appear as current sources, and uses the output of a demultiplexor connected to the latch to control other transistors which act as mutually exclusive switches to send the fixed current to the appropriate terminal. The device is said to use identical current sources, and although there will probably be a few resistive components inside, there is no need for precision resistor matching as in other types of converters. This type of converter design by definition produces the excellent range of supply voltage and transfer characteristics representative of all CMOS devices.

2.2.1 Equivalent Circuits

The Brooktree data sheet shows a few equivalent circuits describing some of its internal arrangements, which are often useful in representing inputs, outputs when it is utilized in a system.

Figure 2-4 is the equivalent circuit for the digital inputs. It indicates that regardless of the state of the input, there will be virtually no input current and the input will see an extremely high impedance, as the gate terminal of MOSFETs is almost completely isolated from its source and drain with the exception of a very small capacitance that generally is only considered at extremely high frequencies.

Figure 2-5 shows the equivalent circuit of the reference amplifier, which

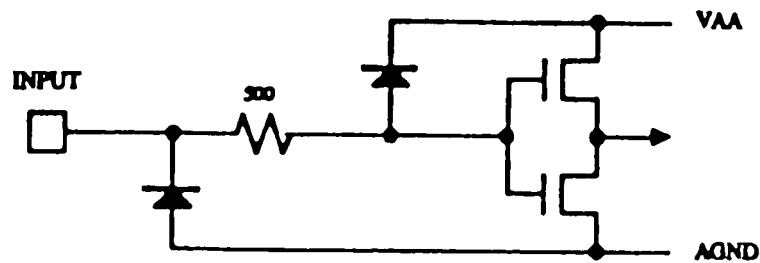


Figure 2-4: Equivalent circuit of the BT105 digital inputs.

stabilizes the full scale output current against temperature and power supply variations. Measurements (presented in Sections 4.1.2 and 4.3.2) show that it is very effective in achieving this.

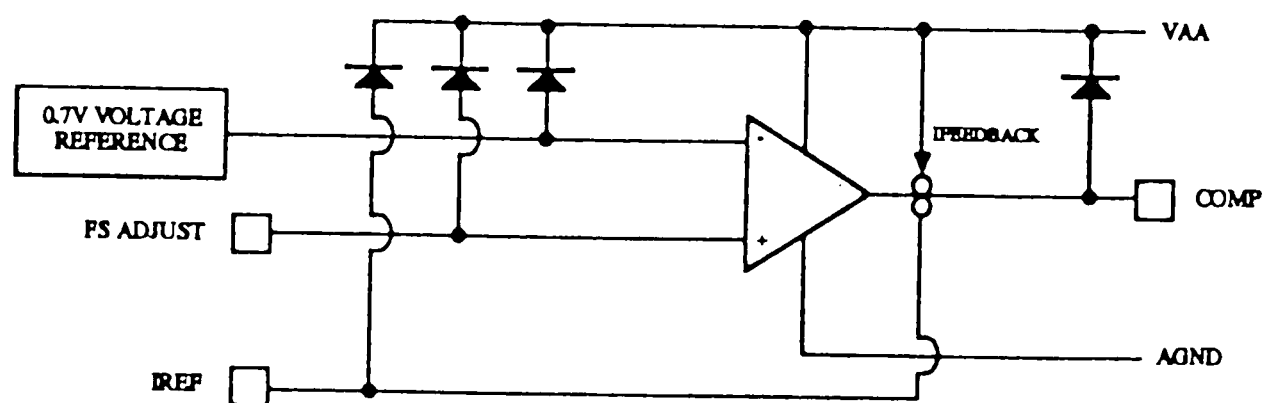


Figure 2-5: Equivalent circuit of the BT105 reference amplifier.

Figure 2-6 indicates the value of parasitic internal capacitance on the current output of the device. Since one can approximate the value of the stray and load capacitance by measurement or knowledge of the equivalent circuit of the input of any devices which happen to follow, and knows by design the value of the load resistor (which converts the current output to a voltage), a reasonable estimate at maximum operating frequency can be made. The load resistance in this circuit is 47Ω . If the stray and load capacitance were kept below about 110 pF , the device could still operate to its maximum rated frequency of 25 MHz .

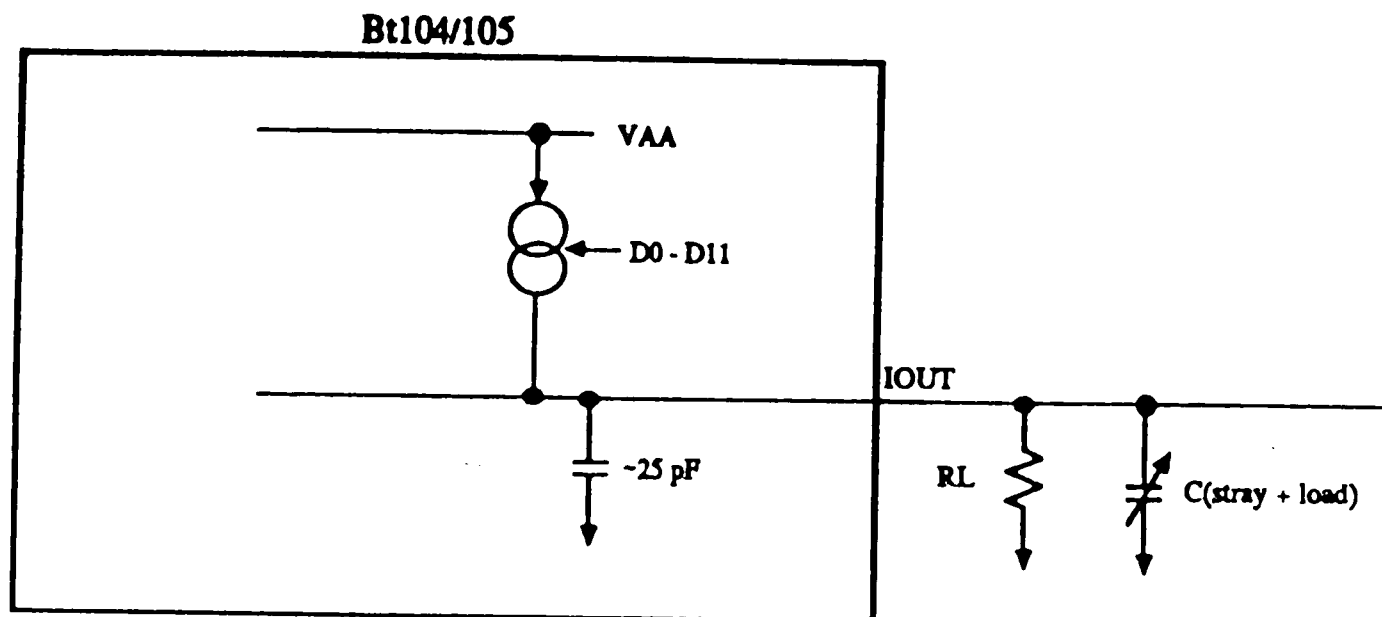


Figure 2-6: Equivalent circuit of the BT105 current output.

Chapter 3

Construction

The complete schematic diagram for this waveform synthesizer is shown in Figure 3-1. The clock signal was provided from a simple CMOS circuit (shown in Figure 3-2), based on a Schmitt-trigger inverter, driven by a sinusoidal voltage from a signal generator.

3.1 General Construction Considerations

Several important factors had to be considered during the construction of this circuit which are not immediately apparent in the schematic. Perhaps the most important of these is that of power supply decoupling, although experimental results showed that an efficient layout of the board is essential in reducing noise in the output.

3.1.1 Power Supply Decoupling

High speed and advanced CMOS integrated circuitry of the nature used in this synthesizer differs from other logic families, TTL for example, in that very large current spikes are drawn from the power supply during transition times. When CMOS gates switch, there is a brief period (on the order of a nanosecond)⁷ during which both transistors in the gate output buffer are partially on. During this interval, the device draws a substantial supply current, producing a current spike on the V_{cc} and ground leads to the device. Such a current spike may exhibit $\frac{di}{dt}$ as high as 5000 A/s.⁷ Note that most of the device's power consumption occurs as a result of these spikes. The number and magnitude of the spikes increase with the number of gates in the package

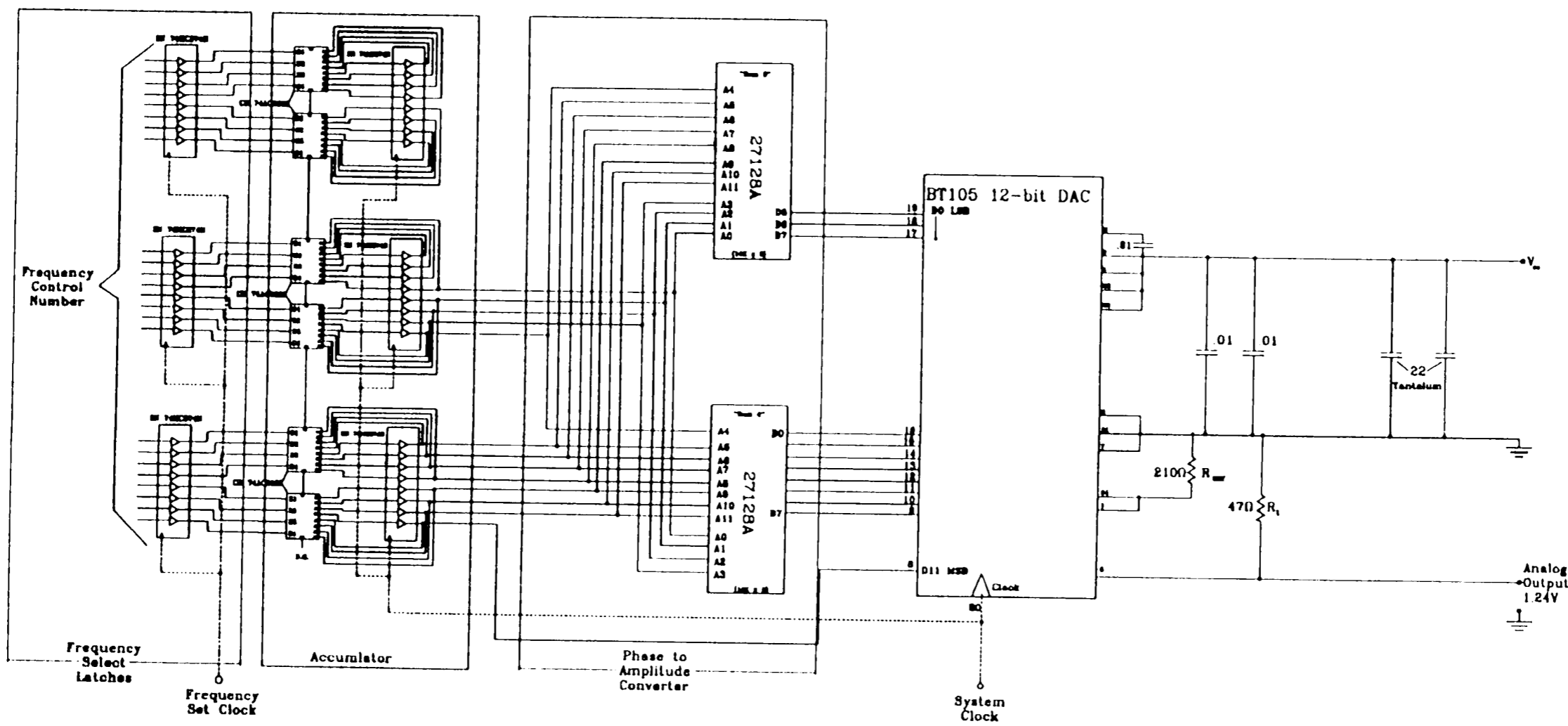


Figure 3-1: Schematic Diagram of Direct Digital Frequency Synthesizer.

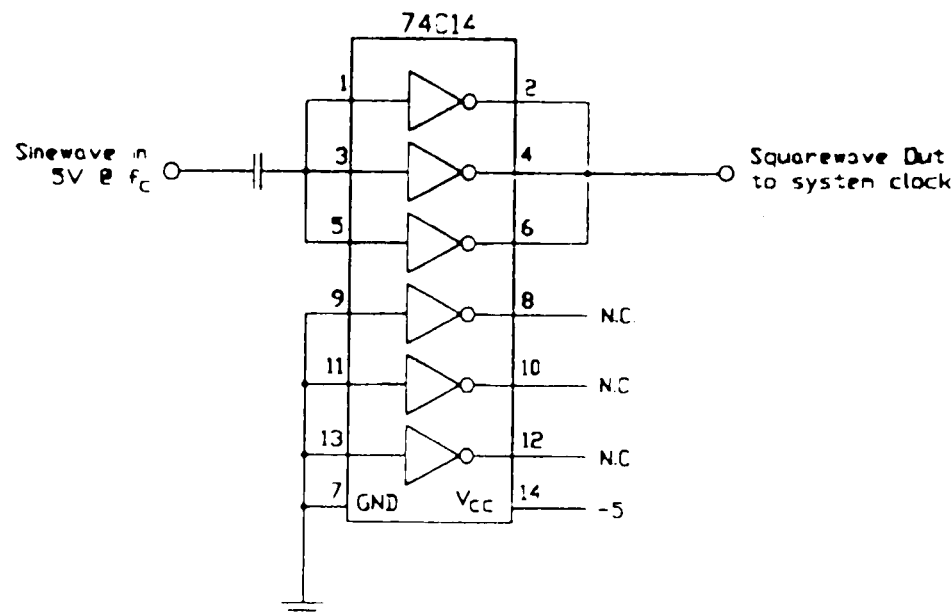


Figure 3-2: Schematic Diagram of Clock Generator.

that are changing state, and in general, there will be more transitions, and thus higher power consumption, as the clock speed goes up. A disturbance of the magnitude of these spikes will react with the distributed inductance of the supply wiring, producing significant voltage transients on the positive supply and ground lines. Consequently, power supply decoupling capacitors are needed to reduce these transients so they do not appear in the output due to imperfect power supply rejection, and also so they do not lower the supply voltage at any point in time to below the device's operational range.⁸

Despite the precautions of using a rather large ($0.1 \mu\text{F}$) high frequency ceramic disc capacitor on each chip used in the design, significant voltage deviations were measured along the supply rails on the board. The actual figures on peak levels are presented in Section 4.1.1.

3.1.2 Unnecessary power consumption

All unused CMOS inputs will be connected to either of the supply rails to prevent the input from floating. Floating inputs will always cause the power consumption of the device to increase.

3.2 Physical Implementation

This circuit was constructed on a protoboard with particular attention to minimizing the length of wires in the circuit. In addition to careful placement of the integrated circuits on the board, the program which generated the data for the ROMs rearranged the positions of the bits at the output so they more closely match the inputs on the DAC.

3.2.1 Accumulator

The accumulator section was implemented by using three 74AC374 8-bit latches manufactured by Fairchild Semiconductor⁹ as the memory element storing the current phase of the output waveform. Advanced CMOS integrated circuitry was used because the design specification for maximum clock frequency could not be met with high-speed CMOS. However, HCMOS was used to store the current frequency because that set of latches was only clocked occasionally, when the output frequency needed to be changed. The contents of the frequency select latches are added to the contents of the accumulator at each clock time by six 74AC283 4-bit adder chips. At the time of construction, RCA Solid state was the only company that manufactured that device.¹⁰

3.2.2 ROM selection

The phase to amplitude converter section was implemented using two Intel 27128A 16K×8 EPROM chips. It must be noted that to minimize power consumption and maximize speed and performance, these are *not* the best choice. Unfortunately, the availability of equipment to program the memory devices of choice was not sufficient to allow their use. Unusual programming voltages and times were often required, and in order to proceed with construction, the Intel

devices (which each consumed more power than any other component on the board, and nearly twice as much as the next lower one) had to be used. Many other suitable devices may be located.¹¹ If one were actually going to take advantage of the symmetry as described earlier, a shorter memory would be adequate. Some wider CMOS EPROMs, such as a 4096x16 manufactured by Waferscale Integration,¹² would eliminate the need for two chips, and operate with much faster access times and consume only a small fraction of the power. In a practical application, different memory chips would be a definite necessity.

In the current design, there were five unused data outputs on one of the memory chips, because 12-bit conversion required only 11 data bits from the output of the memory. Therefore, if the circuit were ever extended to operate at 16 bits, the extra data lines would be immediately available: reprogramming the EPROM and connecting the data bits would be the only necessary change.

3.2.3 Digital to analog converter

The final section of the design is the device to change the digital amplitude information into an analog voltage. Because the frequencies to be generated were very high, only a limited number of converters would be useful. After examining an extensive list of what was available, the Brooktree BT105 was selected because it had more than adequate settling time to produce an excellent quality signal, and its power consumption (since it is a CMOS device) is very low compared to most other converters. Additional power was saved because it had registered inputs, so the latches normally needed between the ROM and the converter were already present in the device. Although it was rather expensive, its other specifications, particularly linearity and physical size of the package, were equally attractive.

Chapter 4

Experimental Results

All of the experimental measurements taken on the circuit of Figure 3-1 are presented in this chapter. Measurements were taken while operating at a clock frequency of both 1.05 MHz and 2.10 MHz, both binary fractions of the original design speed.

In addition, it was determined that the circuit functioned much better in general when the supply voltage was reduced from 5 to 3.6 volts. The 74AC374 latches changed state much more reliably when the supply voltage was below 4.8 volts, and signal to noise improved gradually as supply voltage was decreased. Therefore, data will be presented against supply voltage as well as operating and generated frequency.

One can draw several conclusions about the circuit as a result of the data presented in this chapter. First, the circuit should be operated below 5 volts; preferably at 3.6 for both signal to noise ratio and power consumption. Second, the circuit and its filter both function better at higher clock frequencies, and should perform much better at its designed speed, although probably not with its theoretical S/N figure. Finally, very careful attention must be given to reducing power supply noise spikes, high frequency inductive effects of board layout, and cross coupling of clock, logic, and output signals, or the output signal quality will be seriously degraded, and 12-bit conversion may be pointless.

4.1 Static Output Waveform Characteristics

As this circuit is designed to operate as a frequency reference, a substantial amount of data was taken while it was operating at a constant frequency.

4.1.1 S/N ratio

The construction of this circuit on a protoboard instead of a well-designed printed circuit board substantially degraded the signal to noise ratio of the output signal. Actual RMS signal to noise will be better than what is measured, because peak noise voltages were used in calculations because of the lack of a reasonable way to measure its RMS value. Coupling effects in the metal parts of the board caused a significant amount of the clock signal to appear in the output waveform. In addition, the frequency of the clock (particularly when run at 2.1 MHz) began to make inductive effects in the board noticeable in the power supply and logic signal lines. Power supply spikes were not reduced by the decoupling capacitors to levels necessary to achieve theoretical signal to noise figures. The noise on the power supply rails appeared as ringing with an initial peak which was about 25% larger than the mean noise level. The noise varied positionally along the rail. At low output frequencies, the 74AC374 latches were the noisiest chips, but as output frequency increased, the adders became active and surpassed the latches in noise levels measured on the supply lines. The DAC had about as much noise as the ROM over the entire range of output frequency, and they became noisier than all the other chips when the circuit was operating at or above half its maximum frequency. The peak levels of the power supply noise for each chip in the circuit are presented in Table 4-1. Changing the value, type, or amount

of capacitors used to decouple the supply didn't affect the measured supply rail noise very much, indicating that the noise was mostly a result of high frequency effects, and not inadequate decoupling. In fact, the decoupling capacitors used are an order of magnitude larger than some CMOS design information indicate are necessary.¹³ The noise on the ground rail virtually the same as that on the positive supply. In order to attain the theoretical output quality, this noise would have to be eliminated by the use of ceramic chip capacitors located below the actual integrated circuits, thereby reducing the inductive effects of needlessly increased lead lengths. These effects become increasingly severe when more gates are included in one device, as well as when the distance from the decoupling capacitor increases.⁷

Measurements were taken on the circuit when it was not being clocked and compared to those taken when the circuit was being clocked but set to generate a DC output to determine exactly how much of the noise in the output signal was a result of the clock. The frequency of the noise (again of a ringing nature) was twice that of the clock. These figures, taken at $V_{cc}=5.0$ V are summarized in Table 4-2.

Unfiltered signal to noise ratio was somewhat improved with increasing supply voltage. This effect was only seen at the lower frequencies (incrementing bits below 11 or 12 only; above that, there was virtually no change) and amounted to an improvement in the output signal as voltage increased from 3.6 to 4.5 volts of almost 5 dB (from 27.66 to 32.35 dB S/N), but the degradation in filter performance at all frequencies as a result of increasing the supply voltage made it counterproductive.

S/N was not only a function of supply voltage, but also output frequency.

Power supply noise (peak values)			
IC	Clock Freq.	Noise (volts)	Comments
74AC283	1.05 MHz	0.18	0 Hz output
74AC283	2.10 MHz	0.18	0 Hz output
74AC283	1.05 MHz	0.44	A ₀ incrementing
74AC283	2.10 MHz	0.48	A ₀ incrementing
74AC283	1.05 MHz	0.44	A ₇ incrementing
74AC283	2.10 MHz	0.48	A ₇ incrementing
74AC374	1.05 MHz	0.275	0 Hz output
74AC374	2.10 MHz	0.290	0 Hz output
74AC374	1.05 MHz	0.44	A ₀ incrementing
74AC374	2.10 MHz	0.40	A ₀ incrementing
74AC374	1.05 MHz	0.44	A ₇ incrementing
74AC374	2.10 MHz	0.40	A ₇ incrementing
27128A	1.05 MHz	0.12	0 Hz output
27128A	2.10 MHz	0.13	0 Hz output
27128A	1.05 MHz	0.26	A ₀ incrementing
27128A	2.10 MHz	0.34	A ₀ incrementing
27128A	1.05 MHz	0.50	A ₇ incrementing
27128A	2.10 MHz	0.55	A ₇ incrementing
BT105	1.05 MHz	0.12	0 Hz output
BT105	2.10 MHz	0.13	0 Hz output
BT105	1.05 MHz	0.26	A ₀ incrementing
BT105	2.10 MHz	0.34	A ₀ incrementing
BT105	1.05 MHz	0.52	A ₇ incrementing
BT105	2.10 MHz	0.54	A ₇ incrementing

Table 4-1: Peak power supply noise measured at each integrated circuit under various output conditions.

Effects of clock signal on S/N	
Clock Freq.	S/N figure
0 Hz	33.74 dB
1.05 MHz	14.26 dB
2.10 MHz	13.91 dB

Table 4-2: Signal to noise ratio as related to clock frequency for a DC output.

Therefore, the supply voltage was set to its optimum level for a filtered output (3.6 volts) and two sets of readings (one for each standard test clock frequency) were taken against output frequency. These plots are graphed in Figure 4-1. The signal to noise ratio measured before and after the addition of a filter as a function of frequency is given in Figure 4-2.

Signal to noise ratio

vs. output frequency

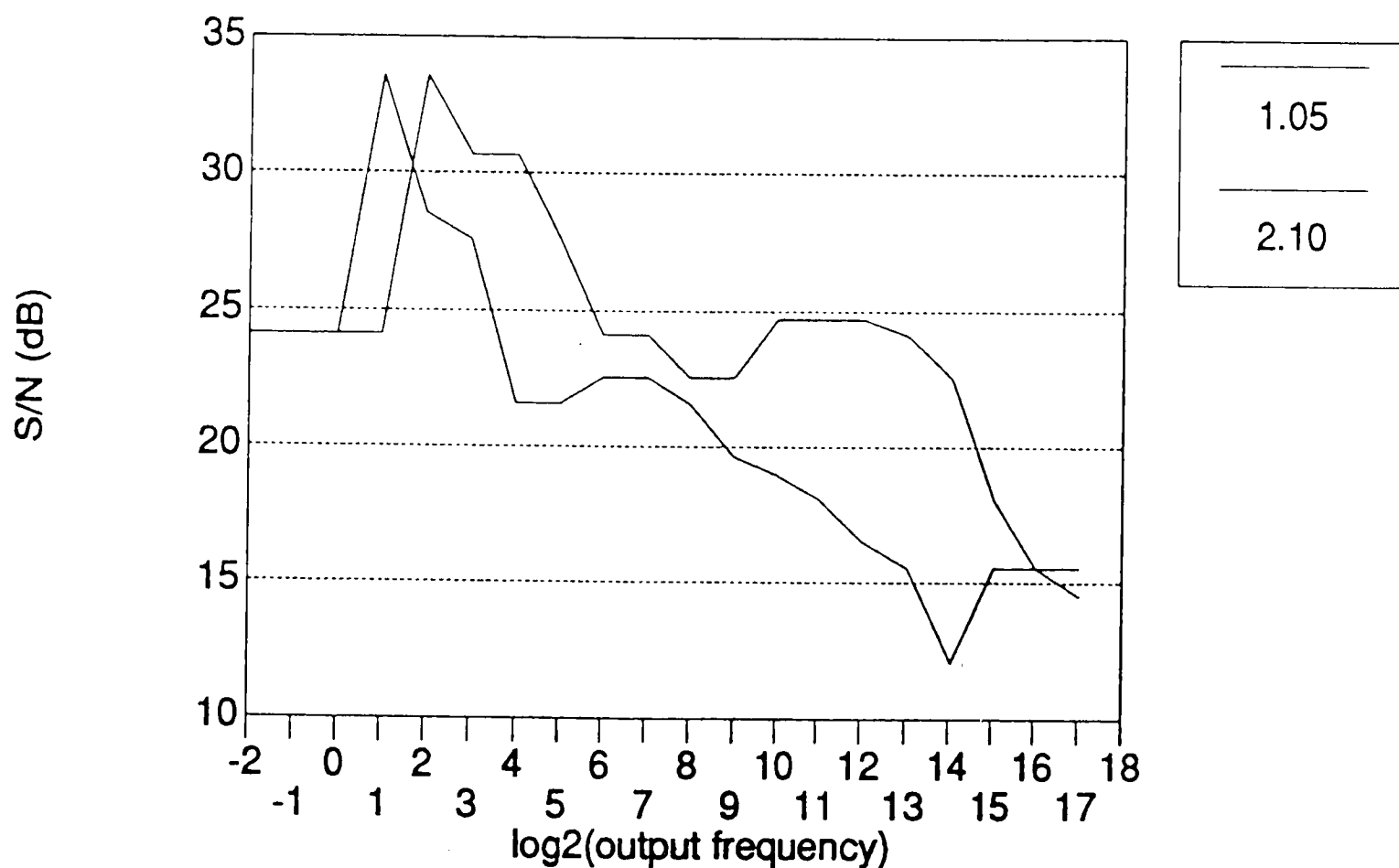


Figure 4-1: Unfiltered signal to noise vs. output frequency at both test clock speeds.

Signal to noise ratio

vs. output frequency

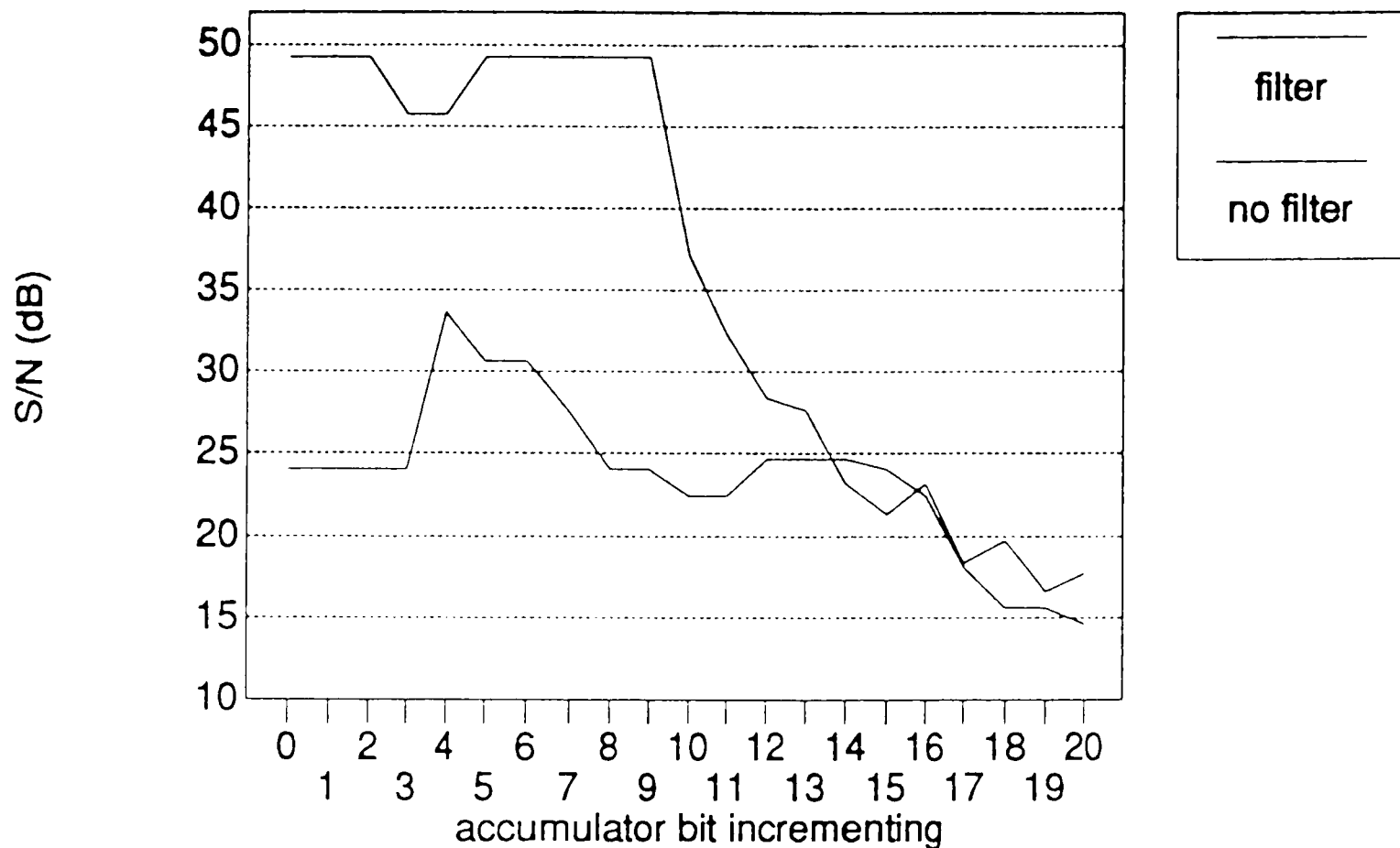


Figure 4-2: Signal to noise vs. output frequency before and after the addition of a low pass filter at $V_{cc} = 3.6$ V and $f_c = 1.05$ MHz.

4.1.2 Frequency stability

The frequency stability and phase continuity of this circuit should be consistent against both time and temperature. No observable deviation in frequency was evident regardless of the output being generated across time: output is consistent as long as the circuit's frequency control latches remained in the same state and the clock is stable. This proves that not only was the clock circuit used adequate to test this circuit, but also that there were no detectable errors in generating the next phase angle and updating contents of the accumulator. The specifications of the devices used in the design would indicate this would be the case well beyond the original designed output

frequency.

As a test to determine usefulness of this circuit under field conditions, the entire board was cooled with component freezing spray to below $= 60^{\circ}$ F. There was no detectable effect on circuit operation at any frequency.

4.1.3 Frequency accuracy

The performance of this circuit in the area of frequency accuracy may be evaluated in terms of two criteria: frequency resolution, the smallest increment by which the output can be controlled; and frequency predictability, the ability to predict the output frequency that will be generated when more than one bit of the frequency select latch is set by adding together the previously measured output frequencies that each incrementing bit generated. This predictability serves to prove the linearity of the output frequency: the output frequency given any multi-bit number in the frequency select latch is always the sum of the individual output frequencies associated with the select latch bits that are set.

The frequency resolution of the design was measured to be within 0.208% at both clock frequencies, corresponding to a difference in frequency from the design specification in the fourth decimal place. The output signal frequency at both clock speeds is plotted on a base-2 log scale in Figure 4-3. The graph indicates that the output signal is a more linear function of input when the clock frequency more closely matches that at which the circuit was designed to operate. The endpoints on the graph correspond to frequencies of 0.12526 Hz and 66.667 KHz (1.05 MHz clock), and 0.25052 Hz and 133.333 KHz (2.10 MHz clock). The full range of output frequencies produced when exactly one bit of the accumulator is incrementing is given in Appendix B.

The accuracy of this circuit in terms of frequency predictability is very

Generated output frequency

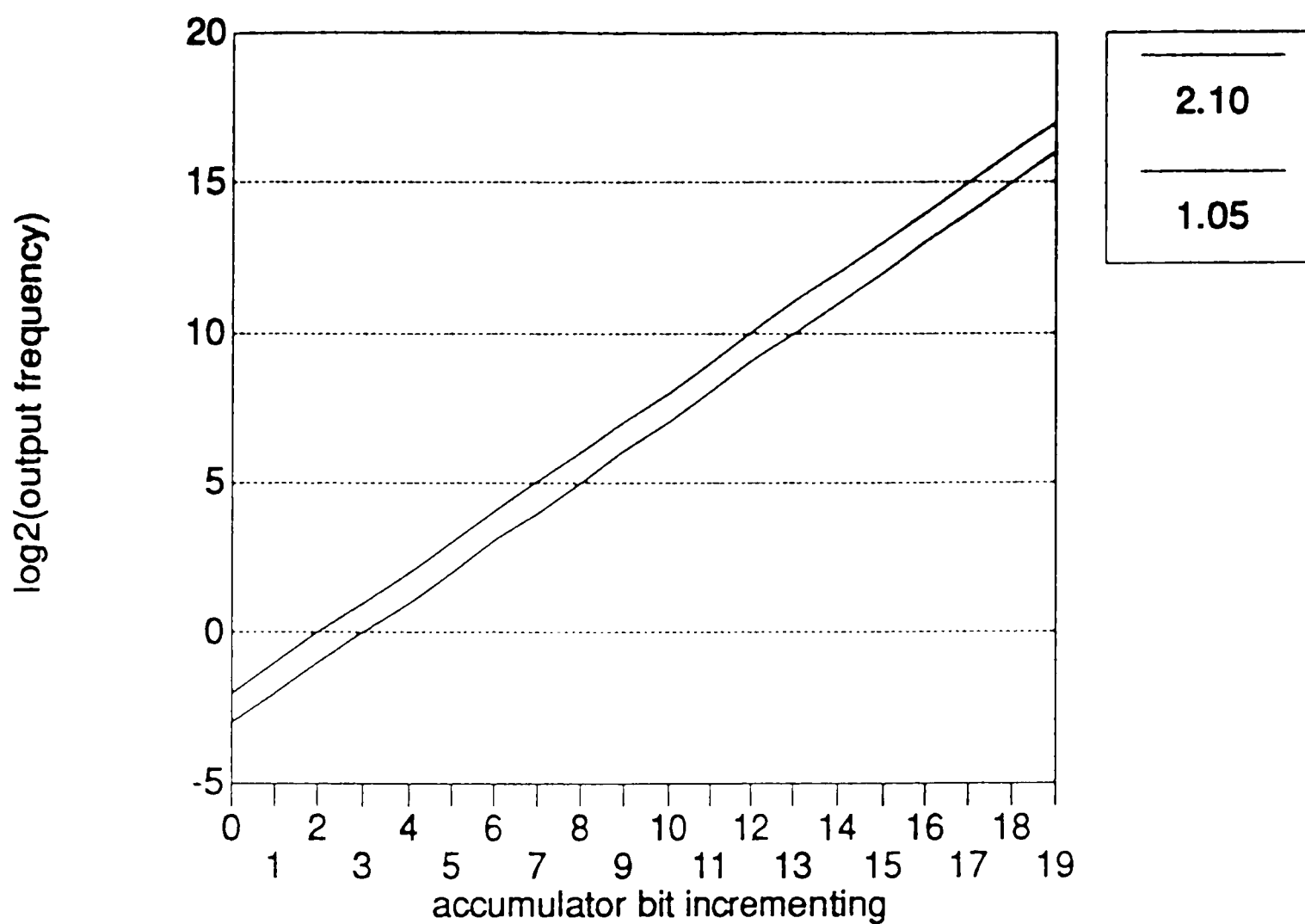


Figure 4-3: Output frequency vs. digital input at $V_{cc} = 3.6$ V.

high. All tested combinations of two and three bits showed that the output as measured was within 3% of the sum of the generated output frequencies measured when only one bit was incrementing. Table 4-3 contains a representative section of this data.

4.1.4 Distortion

Although no figures were taken on total harmonic distortion because of the difficulty in generating an exact sinusoid in phase with the output, it was apparent when the output waveform was visibly distorted.

For an unfiltered output ($V_{cc}=3.6$), a granular characteristic could be noticed when bit 16 (128 samples per cycle) was incrementing (at both the 1.05 and 2.1 MHz clock speeds). The waveform began to have noticeable ringing

Frequency predictability data				
1st bit	2nd bit	Output frequency	Predicted output	Deviation (%)
10	11	387.60	398.25	- 2.674
10	12	649.35	664.91	- 2.340
11	12	780.64	800.00	- 2.420
09	13	1111.11	1097.59	+1.232
12	13	1550.39	1564.25	- 0.886
11	14	2322.88	2328.57	- 0.244
13	14	3115.26	3092.80	+0.726
12	15	4750.59	4700.03	+1.076
14	15	6172.84	6228.60	- 0.895
12	16	8912.66	8866.66	+0.519
15	16	12422.4	12500.0	0.621
09	17	16666.7	16733.3	- 0.398

Table 4-3: Predicted and actual outputs generated by adding a binary word containing exactly two 1's to the accumulator at each clock cycle.

noise and exhibit stepwise changes in level as bit 17 (1.05 MHz) or bit 18 (2.1 MHz) was incrementing. Incrementing bit 18 (1.05 MHz) or bit 19 (2.1 MHz) caused the output to change level in a sufficiently discrete manner to allow one to count the number of samples per cycle (32 and 16 respectively). Without a filter, there was no useful output above those frequencies.

The effect of adding the passive low pass filter was tested while clocking the circuit at 1.05 MHz. In addition to improving signal to noise ratio, discussed later in Section 4.5, it drastically improved distortion, and the following observations relating the incrementing bit to the appearance of the output were made:

0-18 No apparent distortion (notice that the frequency where

distortion first appears has doubled).

- 19 Discrete samples are visible, but waveform is not significantly distorted.
- 20 Waveform is distorted, but *much* more sinusoidal, and might be useable in some applications.
- 21 Waveform may be useful in some applications as a direct result of the addition of the filter. Some DC first appears in the output (output now varies between 0.25 volts and 1.0 volts with some clipping on both peaks).
- 22 Filter converts a square wave (2 samples per cycle) with ringing into a triangular wave with a DC offset (output ranges from 0.4 to 0.8 volts). The square wave ranges from 0.0 to 0.7 volts.

A good filter (probably active) should improve performance further. In a critical application, however, it seems unlikely that a useful waveform could be generated which contains only 4 samples per cycle as the theory states should be possible. 8 samples per cycle should be more than adequate, at least in terms of distortion.

4.1.5 Output level accuracy vs. frequency

The peak to peak voltage of the output ($v_{cc}=3.6$) was measured against frequency at both test clock speeds. This information is graphed in Figure 4-4. At 1.05 MHz, the minimum voltage (1.195 V) represented a deviation of -3.629% of the designed 1.24 V; the maximum voltage (1.350 V) exceeded the design by +8.871%, while the average voltage (1.242 V) was only off by +0.181%. The standard deviation of the voltages at this clock frequency was

Generated output voltage

(vs. output frequency)

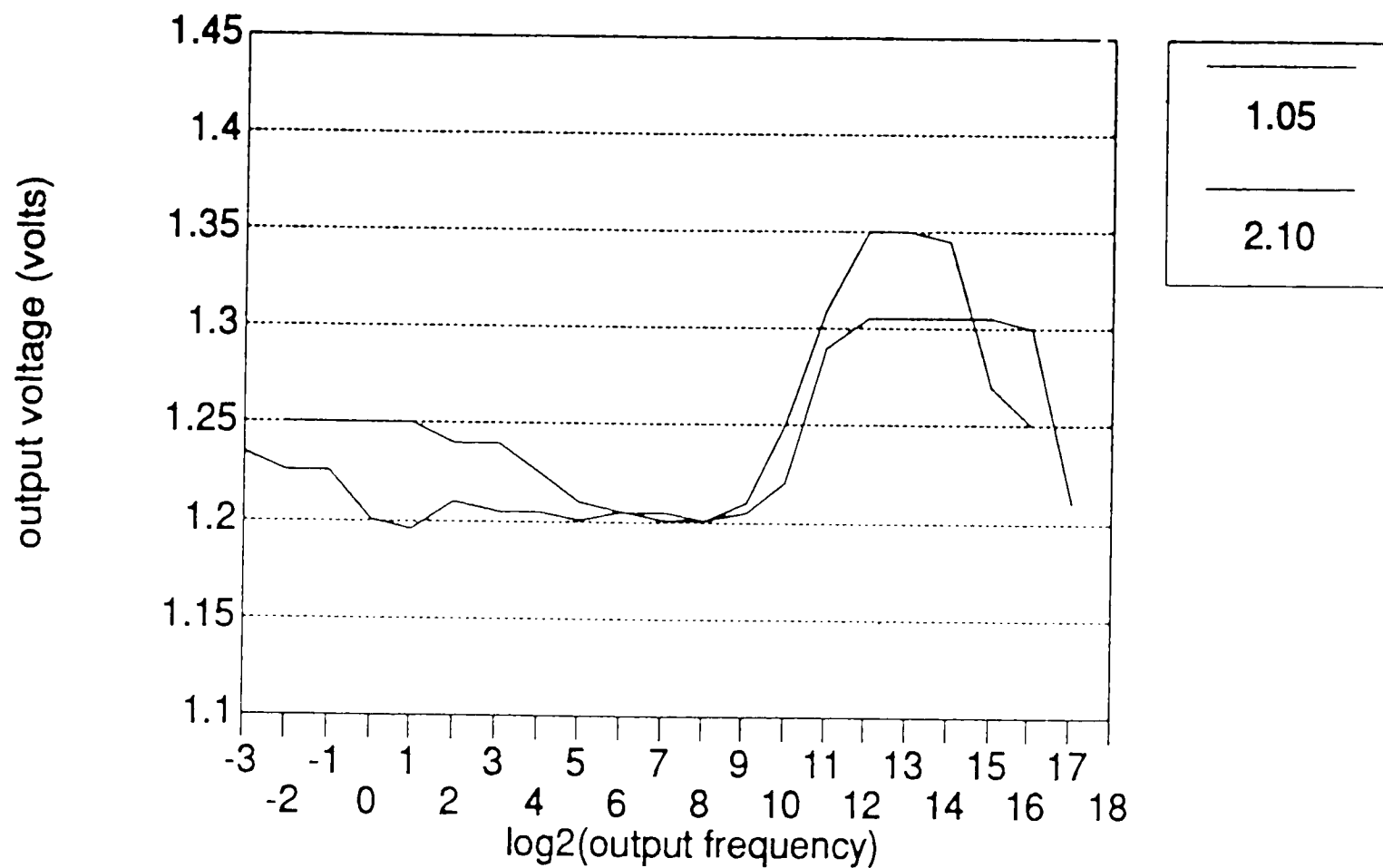


Figure 4-4: Output voltage vs. output frequency at $V_{cc} = 3.6$ volts.

0.0539.

At 2.1 MHz clocking speed, the minimum voltage (1.200 V) represented a deviation of -3.226% of the designed 1.24 V; the maximum voltage (1.305 V) exceeded the design by $+5.242\%$, while the average voltage (1.2482 V) was incorrect by $+0.665\%$. The standard deviation of the voltages at 2.1 MHz was 0.0398.

The P-P output voltage generated is independent of the supply voltage, which reinforces that the converter produces current, and not voltage, outputs accurately over its range. However, as described in Section 4.4.2, varying the supply voltage did have a noticeable effect on its zero offset.

4.2 Dynamic Output Waveform Characteristics

4.2.1 Rate of change of frequency (settling)

This circuit, as expected, demonstrated the ability to change its output frequency without any discontinuities, noise, or voltage spikes in the output signal, beginning at the next clock cycle after the value in the frequency select latch was changed. The filter that followed the output had a sufficiently high cutoff that no delay due to charging of the filter capacitor could be observed.

4.3 Power Supply Aspects

Since one of the more useful characteristics of this design is its low power consumption, data was collected on each integrated circuit component against clock frequency, output frequency, and supply voltage.

The standard advantages to using CMOS components was quite clear in static situations. A general trend that was observed is that power consumption increased with increasing number of high outputs.

4.3.1 Power consumption

The power consumption of the circuit was measured for each integrated circuit on the board against both V_{cc} and output frequency. With the exception of the negligible power drawn by the frequency select latches (which were nearly always in a static condition, and whose power use would only be significant if for some reason the rest of the circuit was unpowered and their state was to be maintained for long periods by battery), the adder chips used the least amount of power. The six chips each required a different amount of power, and the consumption of the ones drawing the most and least against supply voltage for both test clock frequencies are presented in Figures 4-5 and

Power Consumption vs. Vcc

(lowest power adder)

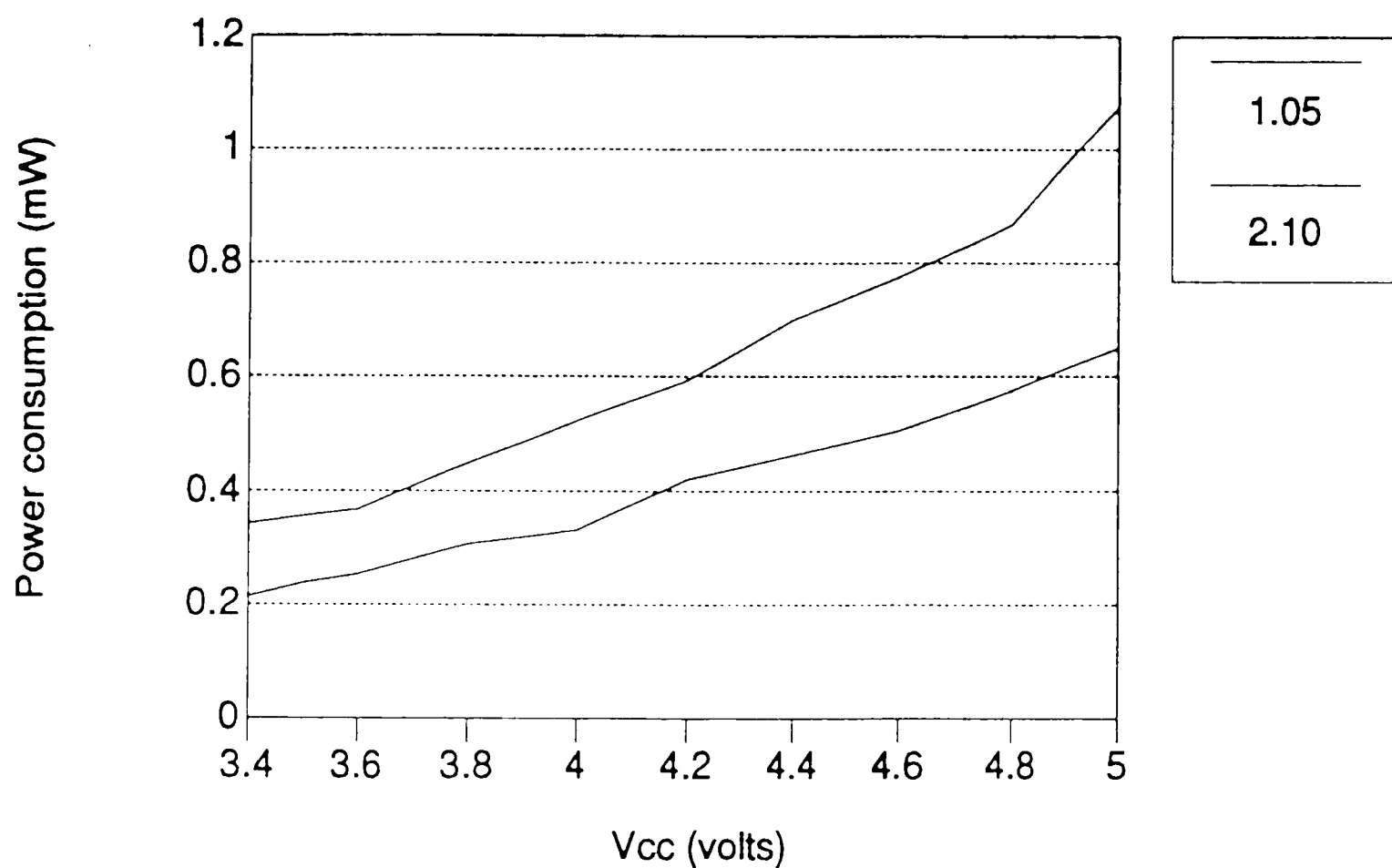


Figure 4-5: Power consumption vs. supply voltage for the 74AC283 adder chip drawing the least power.

4-6 respectively. The power consumption of the 74AC283 adder chips is independent of the output frequency.

The IC ranking next in power requirements was the 74AC374 latches used in the accumulator. Although its power consumption was affected only slightly by varying V_{cc} , it was greatly affected by the clock frequency as well as whether any bits were incrementing (that is, whether a non-DC output frequency was being generated). Table 4-4 shows the important ranges of power consumption for these latches operating at $V_{cc}=3.6$ volts. The latch power is an almost linear function of how many of its outputs are changing. The static power consumption of these devices is negligible.

The power consumption of the digital to analog converter was higher yet,

Power Consumption vs. Vcc

(highest power adder)

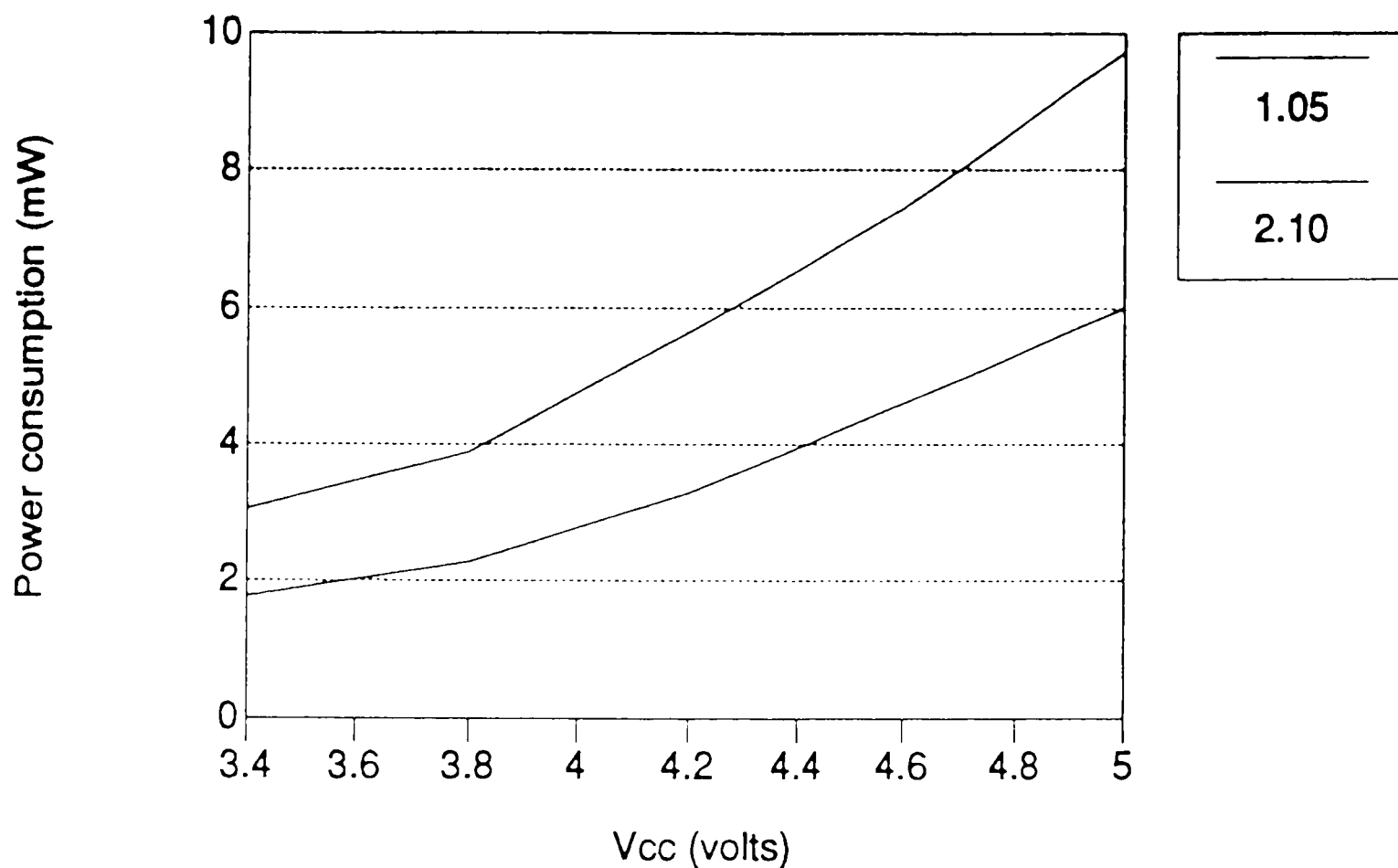


Figure 4-6: Power consumption vs. supply voltage for the 74AC283 adder chip drawing the most power.

74AC374 latch power consumption figures			
clock freq.	hold clear power	one bit incrementing	maximum power
1.05 MHz	Latch 1: 2.81 mW	Latch 1: 45.36 mW	Latch 1: 57.60 mW
	Latch 2: 7.13	Latch 2: 11.52	Latch 2: 100.8
	Latch 3: 0.76	Latch 3: 86.40	Latch 3: 104.4
2.10 MHz	Latch 1: 2.81	Latch 1: 45.36	Latch 1: 65.52
	Latch 2: 7.13	Latch 2: 11.52	Latch 2: 143.6
	Latch 3: 0.76	Latch 3: 86.40	Latch 3: 129.6

Table 4-4: 74AC374 latch power consumption in some significant operating conditions.

and remained constant within 3.6% over the entire range of output frequencies given fixed V_{cc} and clock frequency. Its power requirements did increase greatly as the supply voltage was increased, but clock frequency had an almost

Power Consumption vs. Vcc

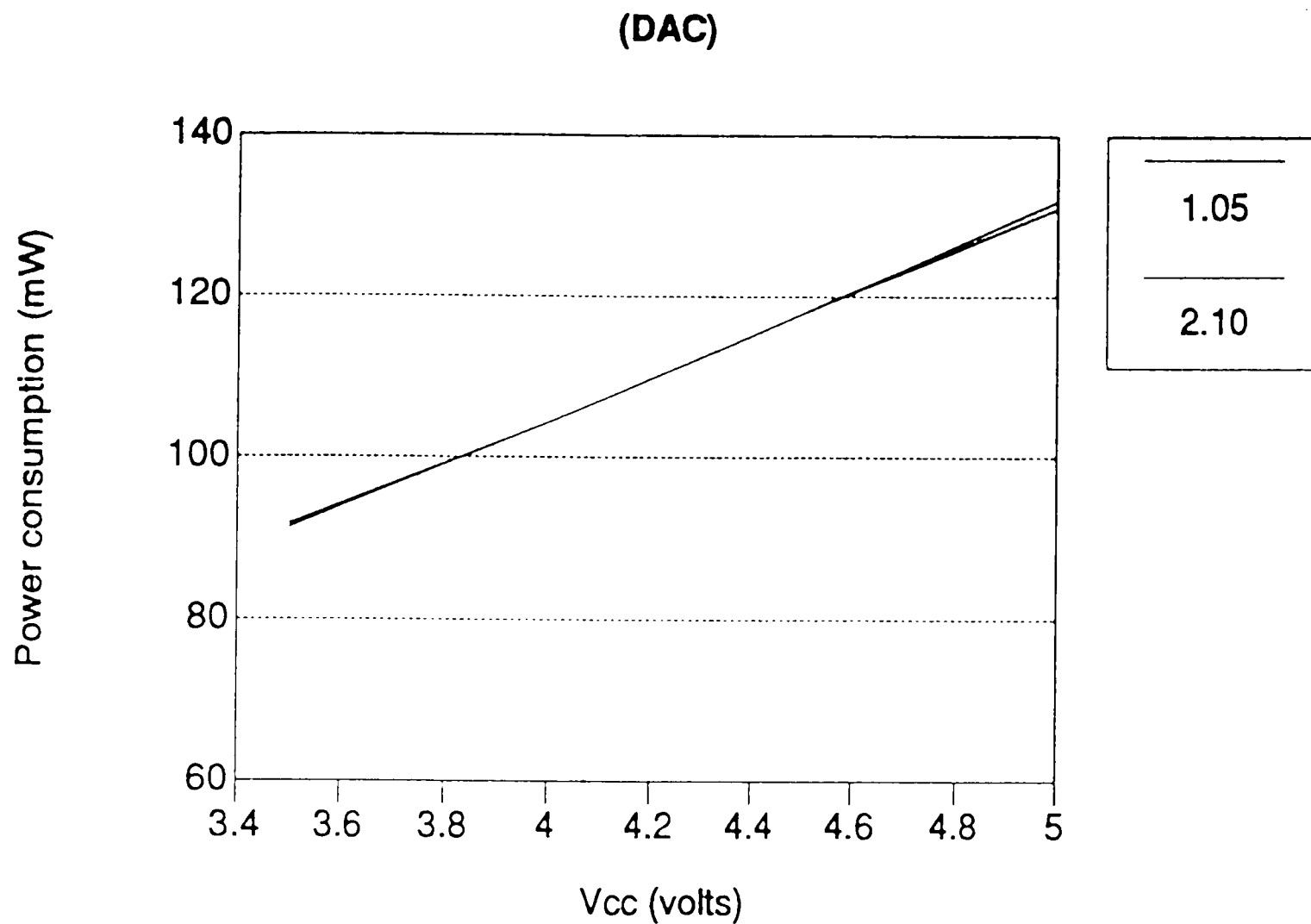


Figure 4-7: Power consumption of the converter as a function of supply voltage.

negligible effect. This information is presented graphically in Figure 4-7.

Although the situation would be much different had a different ROM been used (such as one selected on the basis of the design criteria instead of the ability to program it), the power consumption of *each* ROM chip was nearly twice that of even the converter, making the actual implementation of this circuit completely inappropriate to its original intended use in a portable application. The power consumption of the ROM chips was independent of output frequency and clock speed, and was only a function of supply voltage. The figures for both memory chips in the design are presented in Figure 4-8.

Power Consumption vs. Vcc

(ROM chips)

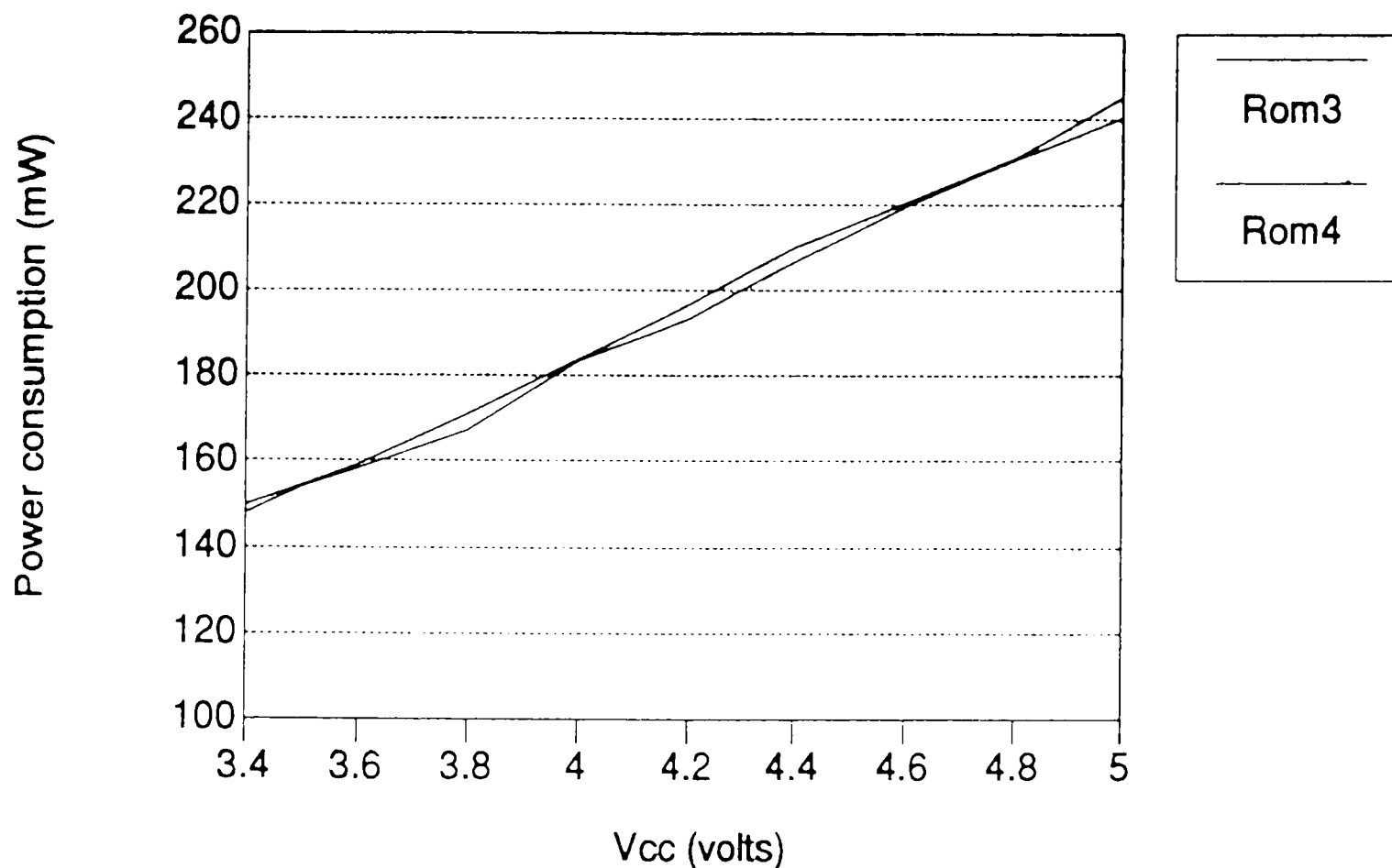


Figure 4-8: Power consumption of the ROMs as a function of supply voltage.

4.3.2 Power supply rejection

The ability for the circuit to ignore noise on the power supply line was tested by the application of a sinusoidal voltage onto the positive rail near the converter. The noise that appeared at the output as a result of this was somewhat greater than what would be expected according to the data sheet had it only been applied to the converter. The rejection of disturbances on the power supply changed as the frequency of the applied noise voltage; this data is expressed in Table 4-5. Note that the last column of the table contains the predicted value of the voltage that must be added to the power supply to achieve a noise figure of 1% of the generated output signal voltage, assuming

Frequency (Hz)	PSRR (dB)	Noise level for 1% of output signal (volts)
100	30.14	0.386
1000	26.02	0.248
10000	36.48	0.933

Table 4-5: Effects of applied power supply noise on the output signal.

that the V_{cc} noise is added linearly.

4.3.3 Maximum clocking frequency

The maximum speed of the clock for this circuit has not been determined. Note that the circuit of Figure 3-2 is *not* satisfactory for operating at the original design speed because it uses a normal (not advanced) CMOS device. However, because the clock signal was specified as being available from elsewhere in the original microprocessor system this circuit was to be a part of, this was considered unimportant.

4.4 DAC Parameters

The power consumption of the converter has previously been graphed (Section 4.3.1).

4.4.1 DAC linearity

The linearity of the converter is defined as how accurately a given constant incremental change in its digital input will produce a constant incremental change in its analog output. It is a direct measurement of the quality of a converter, as nonlinearity will always have a negative effect on the performance of a circuit. Because of the importance of knowing how linear the DAC is, five different linearity measurements were taken. The first two

(Figures 4-9 and 4-10) show the linearity of the DAC as the input word changes in the low order bit, at the low and high end of the converter range respectively.

DAC Linearity

(at low end of range)

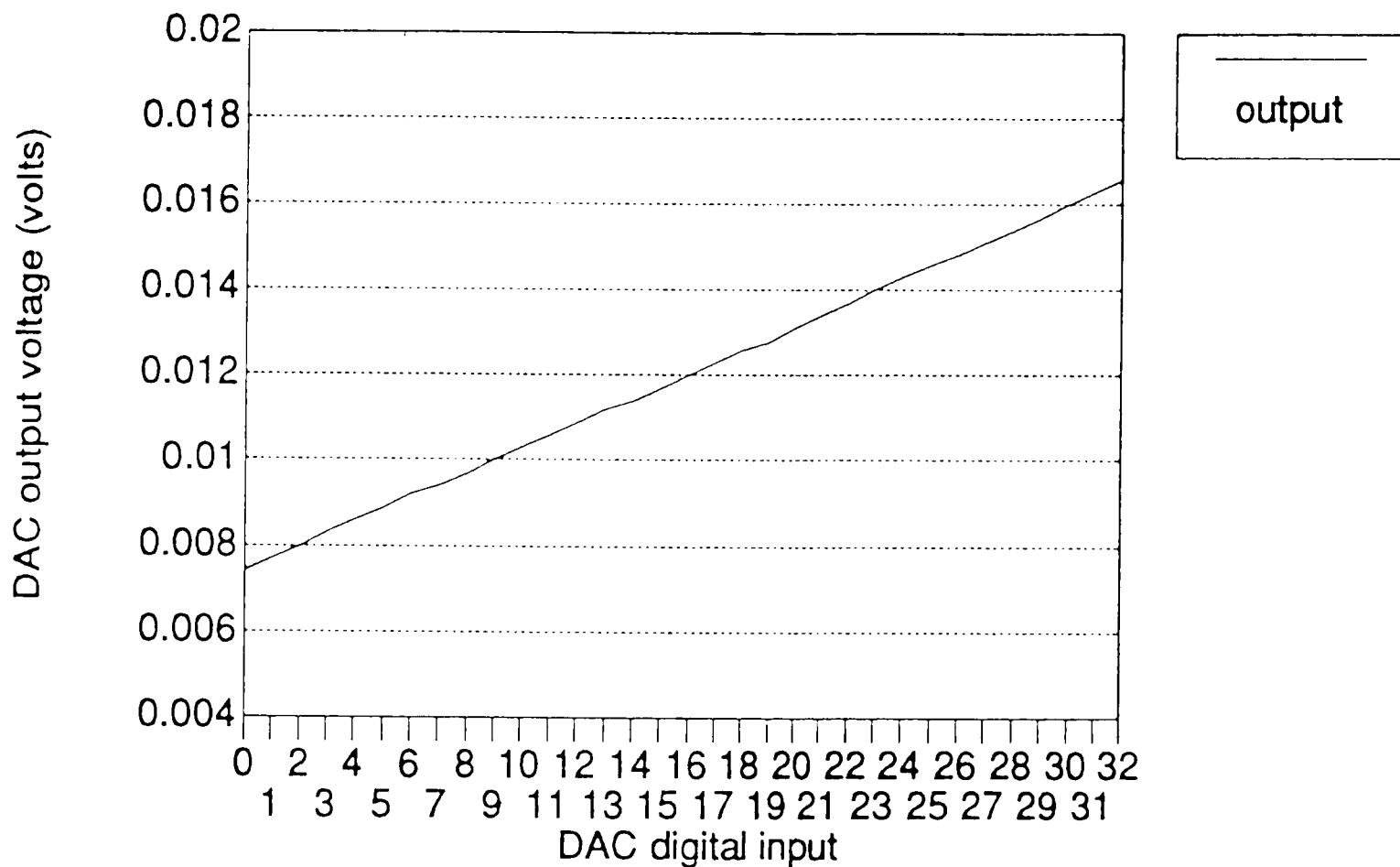


Figure 4-9: Converter output voltage vs. input value, incremented by 1, at the low end of its range.

Figures 4-11 and 4-12 show the linearity as the input is changed by 32, at the low and high end of the converter range. Figure 4-13 shows converter linearity as the input word changes from zero to its maximum value by an increment of 256.

Examining the graphs, one recognizes that the converter is extremely linear in all of the tested ranges. The best fit to a straight line exists in Figure 4-13, where scale allows the entire converter range to be displayed. It seems to function best in all respects when the output voltage is near its upper limit: the

DAC Linearity

(at upper end of range)

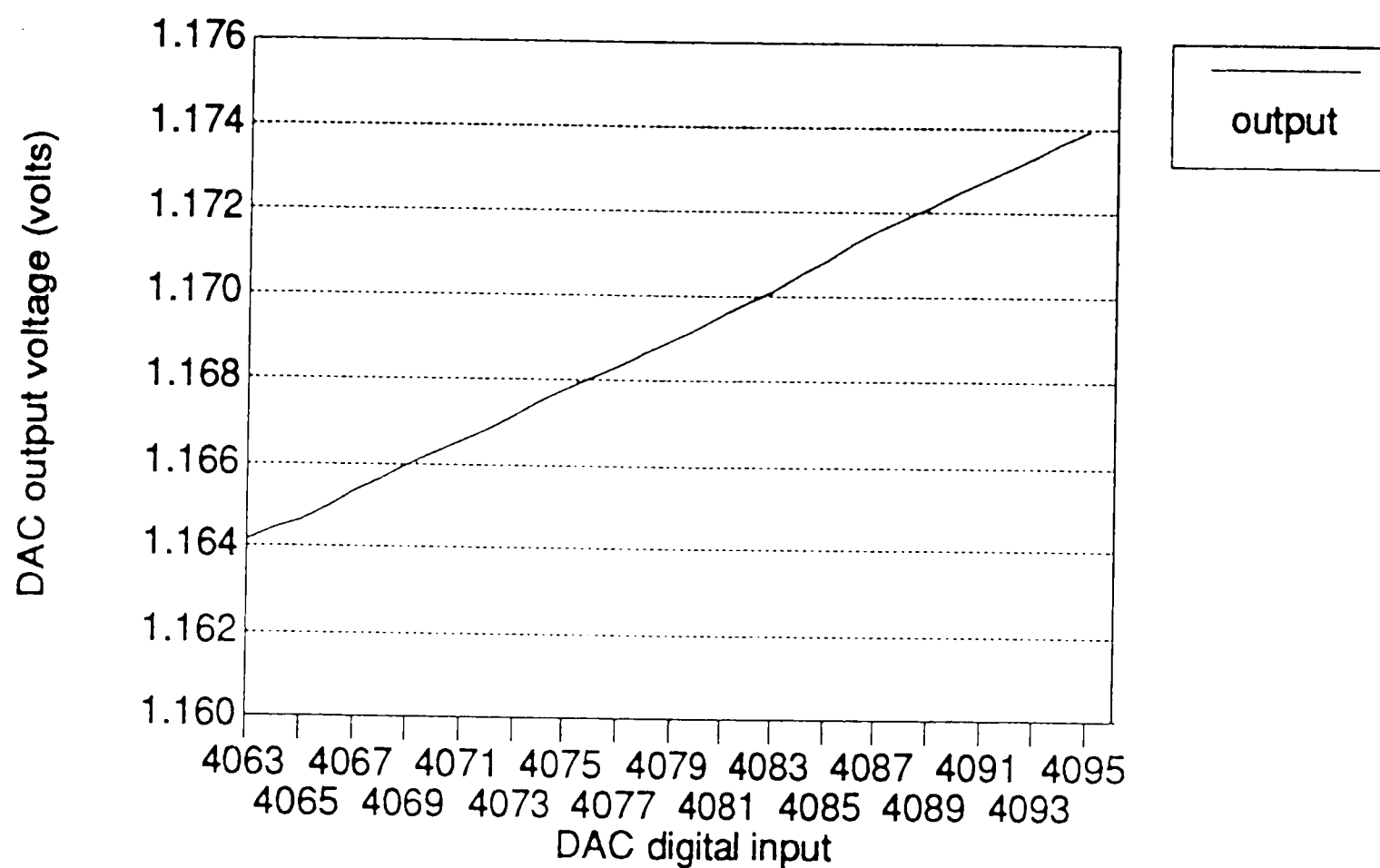


Figure 4-10: Converter output voltage vs. input value, incremented by 1, at the high end of its range.

remaining linearity graphs will reveal, on close examination (more easily when the graph is not reduced), that there are less "discontinuities" and that they are lower in magnitude at the higher end of the converter's range. However, the performance of the converter overall is excellent, as shall become evident in the following sections, and it was a very good choice for this application.

4.4.2 Effect on the converter of varying the supply voltage

As stated in Section 4.3.2, the converter's operation is very consistent as supply voltage is adjusted. It rejects power supply noise quite well, and its current output is constant over a wide range of V_{cc} . The only effect that changing the supply voltage had on the converter other than the contamination

DAC Linearity

(at low end of range)

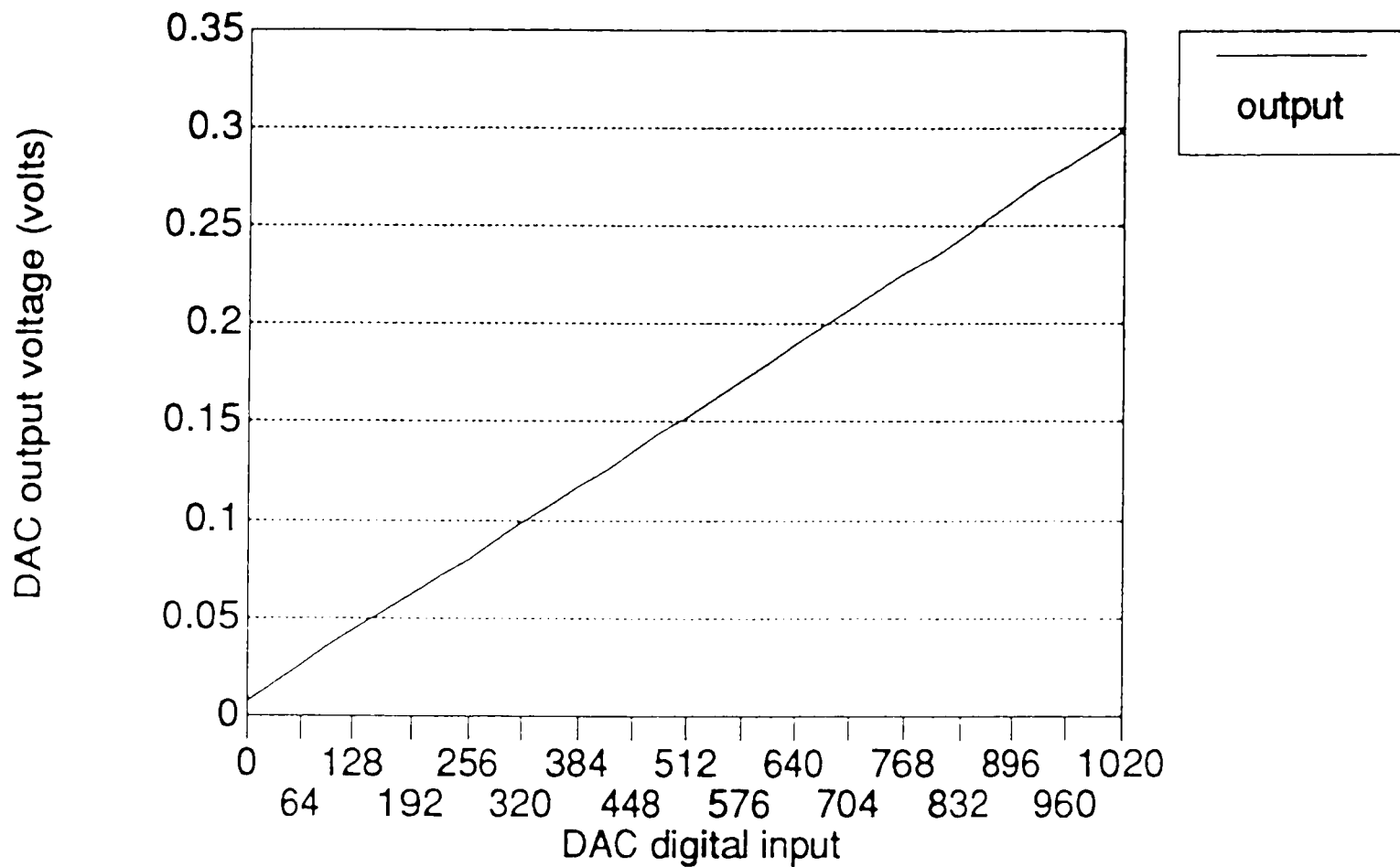


Figure 4-11: Converter output voltage vs. input value, incremented by 32, at the low end of its range.

of the output already discussed was that its zero offset voltage was changed slightly. This deviation appeared as the input to the converter was held at zero (or some other fixed value) and its output voltage was measured as the supply voltage was adjusted. The converter's output voltage for zero input increased by 6.757% as the supply voltage was increased by 38.89% from 3.6 to 5.0 volts, but the output voltage for all input bits set increased by only 0.366% over the same range.

DAC Linearity

(at upper end of range)

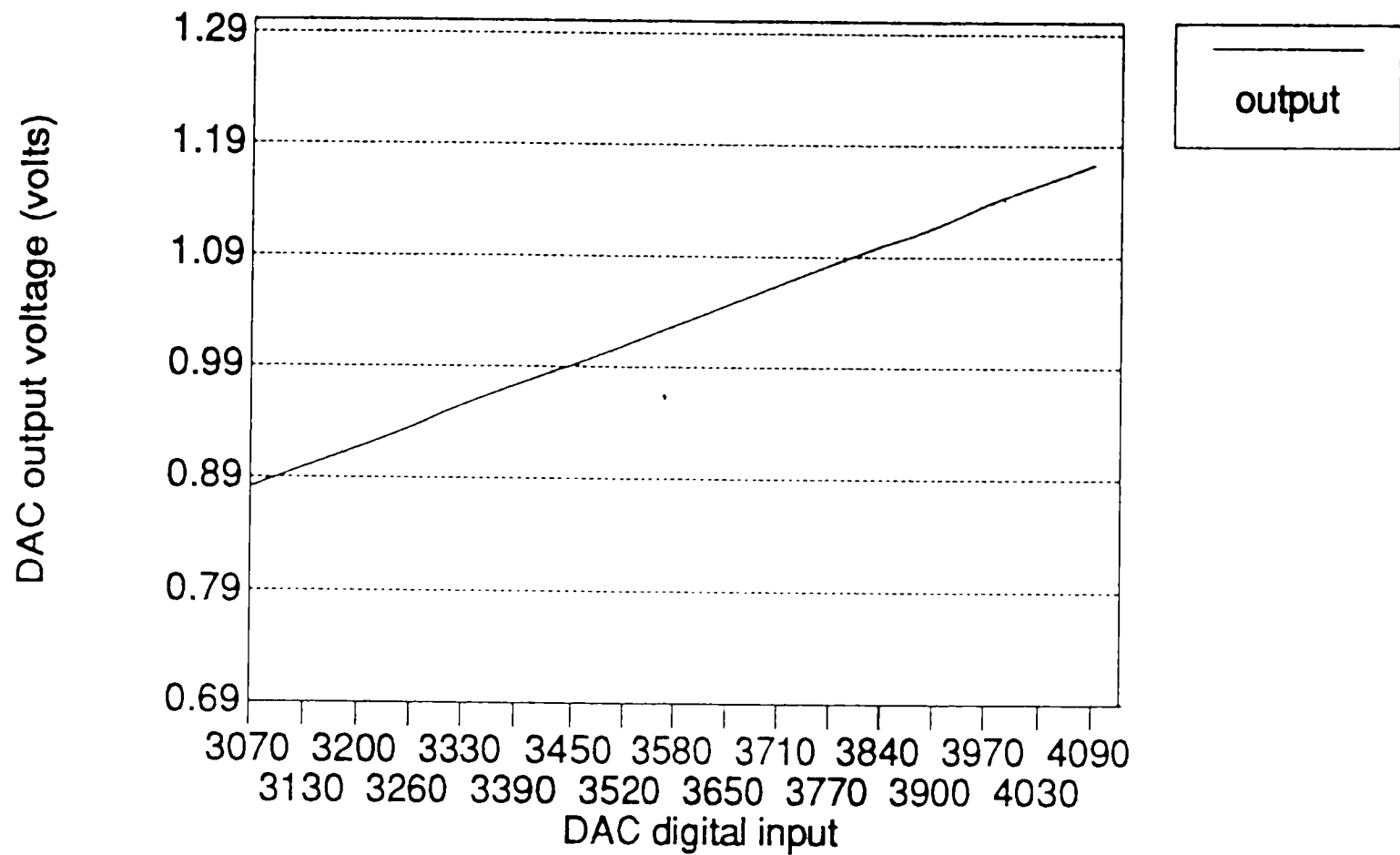


Figure 4-12: Converter output voltage vs. input value, incremented by 32, at the high end of its range.

4.4.3 Delay for full scale voltage change (DC)

To determine the ability for the converter to change its output quickly, the input to the device was varied alternately between its minimum and maximum value (0 and $2^{12} - 1$) at each clock cycle. The converter was able to change its output full scale and settle in $0.5\mu\text{s}$ with overshoot of 4.48% .

DAC Linearity

(across entire range)

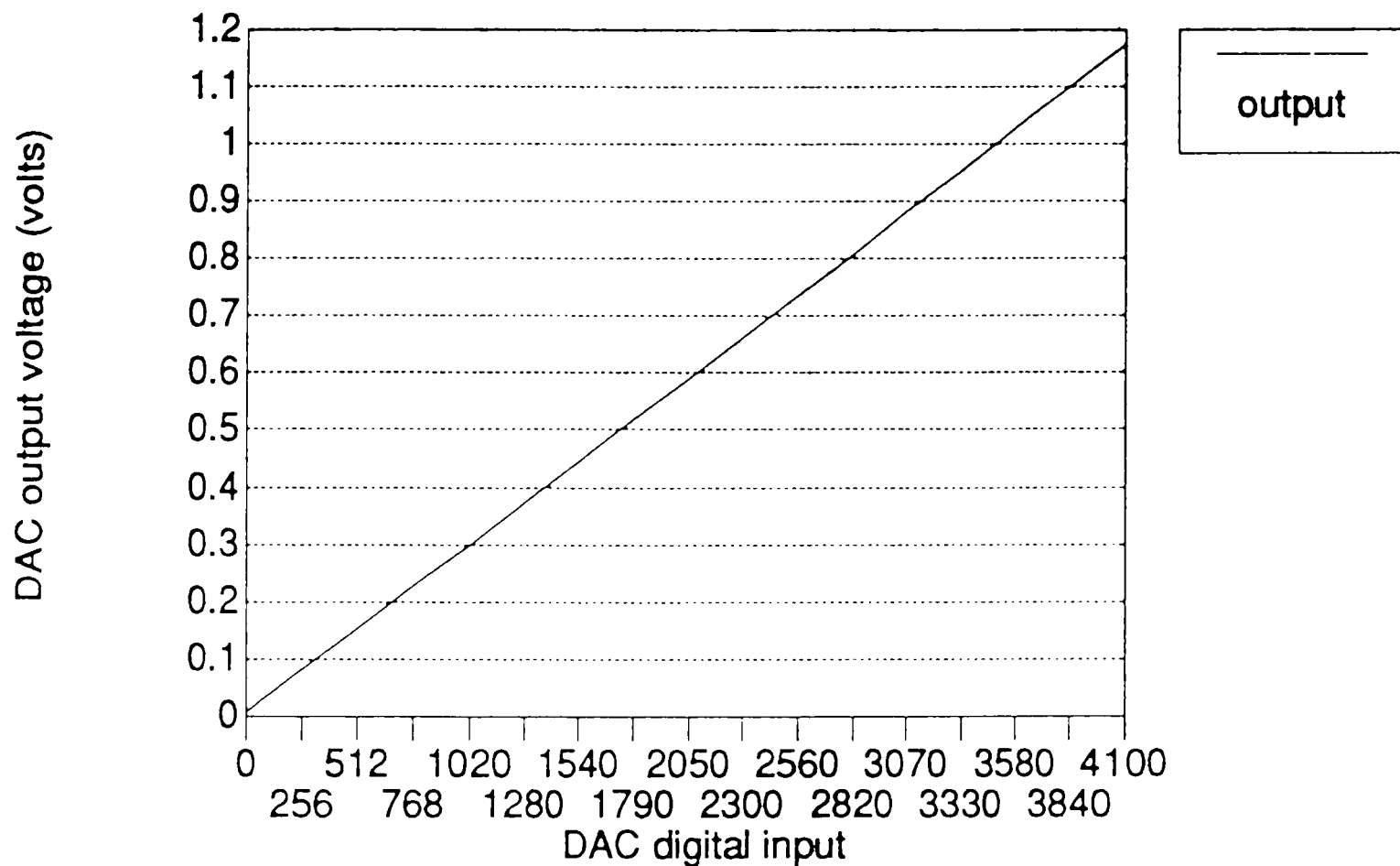


Figure 4-13: Converter output voltage vs. input value, incremented by 256, over its entire range.

4.4.4 Overshoot vs. frequency

The overshoot of the DAC, that is, how far above or below the correct and stable voltage level its output deviates as it attempts to change in response to a new digital input. Rather than testing the DAC directly, the overshoot was measured on the output waveform as a function of the output frequency. This information is presented in Table 4-6. Overshoot for this converter is not observable below the first entry in the table, but then indicates a general improvement as the output frequency increases.

Overshoot vs. output frequency		
bit incrementing	Overshoot voltage	Percent overshoot
15	0.02 to 0.2 volts	1.49 to 14.9
16	0.02 to 0.2	1.49 to 14.9
17	0.02 to 0.14	1.49 to 10.45
18	0.04 to 0.14	2.99 to 10.45
19	0.02 to 0.1	1.49 to 14.9
20	0.08	5.97

Table 4-6: Overshoot measured at the output as a function of generated frequency at the 1.05 MHz clock speed.

4.5 Low pass filter

The degree of improvement in signal to noise ratio which appeared in the output as a result of the use of a filter was found to be dependent on three factors: output frequency, clock frequency, and supply voltage. The best filter performance was observed at low V_{cc} (2.8 volts for 1.05 MHz, and 3.4 volts for 2.1 MHz), low clock frequency, and low output frequency (although the use of a filter reduces distortion, producing a potentially useful waveform for an additional two bits, near the upper limit of operation).

The filtered and unfiltered s/n ratios have already been plotted against frequency in Figure 4-2.

The best overall circuit performance was achieved when using the filter indicated in Table 1-1 at $V_{cc}=3.6$ volts and clocking at 1.05 MHz. Its frequency response is presented in Figure 4-14. Under the same conditions except clocking at 2.1 MHz, the circuit worked slightly better at low output frequencies but slightly worse at high output frequencies with the filter utilizing the 220 pF capacitor. None of the other filters functioned particularly well.

Low Pass Filter

Frequency Response

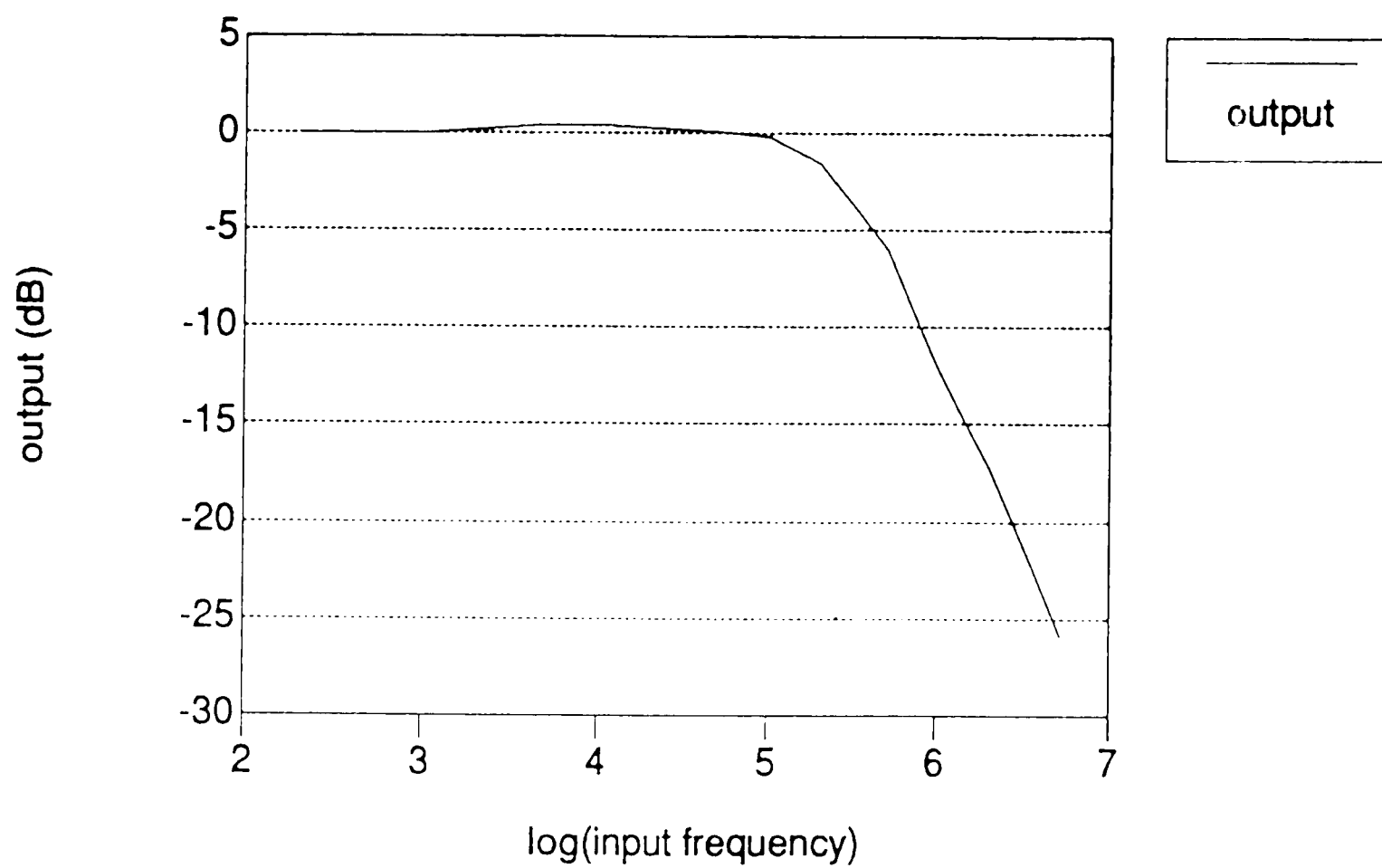


Figure 4-14: Measured LPF frequency response.

Chapter 5

Modifications and Application

5.1 Generation of alternate waveforms

Alternate waveforms could be generated by this circuit simply by replacing the existing sine-ROM's with ROM's containing the new information. Addition of more ROM/converter sets would allow one to generate a number of waveshapes at the output simultaneously.

Certain waveforms, specifically square, triangular, and sawtooth, are even easier to implement. A square wave can be obtained at the output by using the most significant bit of the accumulator directly. A sawtooth wave results when the output of the accumulator is applied directly to the DAC. Use of the msb of the accumulator to complement the other accumulator bits (then presented to the DAC) produce a triangular wave.

This flexibility in changing output waveforms make this circuit very useful in the area of test equipment. By simply adding a binary counter to control the frequency, a sweep generator can be made.

5.2 PC Board layout considerations

At frequencies at or above those now being used in this circuit, a designer should be aware of some potential problems in manufacturing a printed circuit implementation. One should certainly expect noise effects and signal degradation effects similar to those documented in Chapter 4. Some recommendations for printed circuit layout¹⁴ include:

1. Keep lead lengths between groups of power pins at a minimum to reduce inductive ringing.

2. Maintain separate power and ground planes for the digital and analog signals. The analog ground plane area should encompass all the converter ground pins, any external voltage reference circuitry, power supply bypass circuitry for the converter, the analog output traces, and any output amplifiers. The regular ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the converter. The analog ground plane should be connected to the regular ground plane at a single point through a ferrite bead. The same holds true for connection of the analog and regular power planes.
3. Exercise care to prevent portions of the regular power and ground planes do not overlay portions of the analog power or ground planes unless they can be arranged such that the plane to plane noise is in common mode, to reduce interplanar noise coupling.
4. Decouple the power supply by placing chip capacitors under the converter to remove noise spikes on the analog power and ground planes. Although the BT105 contains circuitry to reject power supply noise, the rejection decreases with frequency. The recommended layout of capacitors around the converter is presented in Figure 5-1.
5. Connect active termination resistors for the digital inputs, if any, to the regular power and ground planes.

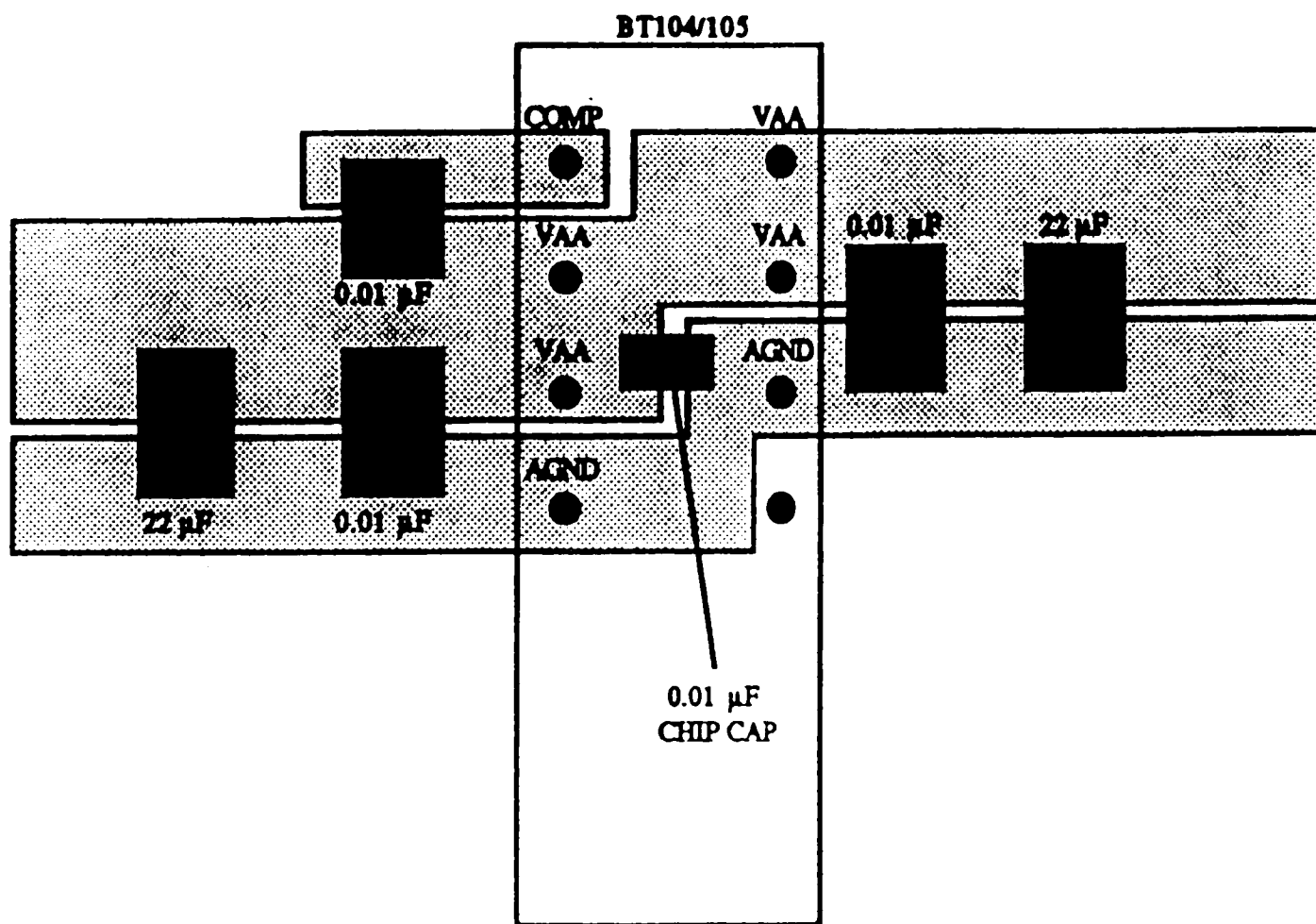


Figure 5-1: Suggested locations of decoupling capacitors in the vicinity of the BT105.

6. Isolate the digital inputs of the converter from the analog outputs and other analog circuitry. Do not allow the digital input signals to overlay the analog ground and power planes.
7. Place any external output amplifier (converting the current outputs to a voltage) as close as possible to the converter. Connect the amplifier's power terminals, as well as any power terminals of external voltage references, to the analog planes.
8. Maximize high frequency power supply rejection by having the output signal overlay the analog ground plane and not the analog power plane.

Another means of minimizing noise would be to implement the circuit in surface mount technology.¹⁵ Unfortunately, at the time this circuit was constructed, most of the devices were still in the evaluation stage and were unavailable in surface mount. Brooktree was still considering whether it would package the converter that way at all. The other major ACL manufacturers were also having serious difficulty agreeing on pin assignments for the device, because some felt that performance would be best if the power pins were kept in the corners, while others would relocate them to the center.¹⁶ In fact, to avoid a collision with current standards, TI was forced to change its numbering series for the devices because it chose to use the centrally located power pins. Their current ACL series numbers are 74AC00 for corner-pin devices, and 74AC11000 for center-pin devices.

5.3 Filter Improvements

Filtration of the output to remove high frequency noise generated by the conversion is necessary for the highest quality signal. A first order filter, used in this design, would probably not be the best choice if one was going to produce a number of units for industry. Although it has been stated earlier that many active filters are unsuitable due to gain-bandwidth restrictions, a higher-order filter using discrete transistors would not, with proper device selection, be subject to such restrictions over the circuit's operational range. If the required output frequency is not extremely high, a good op amp would work well. Output signal quality can be expected to improve significantly, because the converter is actually designed to drive a virtual ground, and it is not.

5.4 Synthesis of higher frequencies

This type of waveform synthesizer is limited to operation beginning at DC and increasing to a quarter of its clock frequency. In many applications, including the sweep analyzer manufactured by CALAN, an offset range, perhaps beginning at a few hundred megahertz and extending upward from there by a quarter of the clock frequency, is needed. Fortunately, high speed phase-locked loops (PLL's) and frequency multipliers exist which enable this to become reality.

5.5 Ability to set or change phase or frequency at any time

The direct digital frequency synthesizer in the form presented has no phase discontinuities in the output, even when the frequency is changed by modifying the frequency control number. However, the circuit immediately lends itself to applications where one needs to be able to *set* the phase of the output to a specified value. Implementing the accumulator with latches having set/reset control would accomplish this if one could locate the parts. Another method, probably more useful in a practical situation, would be to have two complete accumulators enabled in a mutually exclusive fashion. The one not selected would have the desired starting phase value clocked into it just before it was selected. By simply changing which accumulator addressed the ROM, synthesis of a waveform beginning at any preset phase would be possible. Phase discontinuities, when needed, are thereby achieved. Similarly, an adder placed between the accumulator output and the phase to amplitude converter (ROM) would allow one to phase shift the output by changing that value added to the accumulator before its output drives the ROM's address lines. The user can *exactly* control every aspect of the output.

The versatility of this circuit, combined with technological changes in speed, cost, and availability of logic, memory, and converters make it the only logical choice for high accuracy, high resolution frequency references in test equipment.

Appendix A

S/N to Noise Voltage Table

Desired S/N (dB)	Max. noise (mV)
10	392.12
16	196.53
20	124.00
24	78.239
30	39.212
32	31.147
40	12.400
48	4.9365
50	3.9212
56	1.9653
60	1.2400
64	0.7834
70	0.3921
72	0.3114
80	0.1240
90	0.0392
96	0.0197

Table A-1: Noise voltages required for a given signal to noise figure.

Appendix B

Generated Frequency Table

Freq. select latch to output freq. relation		
Accum. bit incrementing	Output freq. (1.05 MHz)	Output freq. (2.10 MHz)
00	0.1253 Hz	0.2505 Hz
01	0.2506	0.5008
02	0.5007	1.0010
03	1.0010	2.0013
04	2.0027	4.0000
05	4.0000	8.0645
06	8.3333	16.260
07	16.129	32.787
08	32.258	64.267
09	66.667	133.33
10	131.58	261.43
11	266.67	524.93
12	533.33	1046.0
13	1030.9	2105.3
14	2061.9	4184.1
15	4166.7	8333.3
16	8333.3	16667.
17	16667.	33613.
18	33333.	66667.
19	66666.	133333

Table B-1: Table representing the source of the graph of Figure 4-3.

Appendix C

Notes on Schematic

The notes in this appendix apply to the schematic diagrams shown in Figures 3-1 and 3-2.

1. Pin numbers, power supply connections, and $0.1 \mu\text{F}$ decoupling capacitors on every chip not shown except as noted. The power supply connections are as follows:
 - 27128A ROM: V_{cc} = pin 24; GND = pin 12.
 - 74AC273: V_{cc} = pin 20; GND = pin 10.
 - 74AC283: V_{cc} = pin 16; GND = pin 8.
 - 74HC374: V_{cc} = pin 20; GND = pin 10.
2. All capacitors in μF unless otherwise noted.
3. All capacitors on the schematic are ceramic disc unless otherwise noted.
4. All resistors in Ω unless otherwise noted.
5. See BT104/105 data sheet, Figure 5, for decoupling capacitor layout. $0.01 \mu\text{F}$ ceramic chip capacitor not used in test design.
6. R_1 on the main schematic is a 1% metal film device. R_{set} may, in some designs, need to be adjusted above or below its calculated value by 10% to compensate for internal differences in the converter.
7. Chip enable/select connections are not shown on the main schematic. The label given by the manufacturer, the pin number, and its connection is listed below.
 - 27128A ROM: CS2 (18) = V_{cc} ; $\overline{\text{CS1}}$ (20) = GND.
 - 74AC273: $\overline{\text{MR}}$ (1, chip clear terminal) = V_{cc} .
 - 74HC374: $\overline{\text{OC}}$ (1, output enable) = GND.

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Vita

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