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Some Electrical and Material

Characteristics of Fluorine Implanted

Metal-Oxide-Semiconductor Capacitors

by

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Abstract

A fundamental experiment pertaining to the effects of implanted fluorine on MOS capacitors. Background information concerning the fundamental theory and application of MOS capacitors related to fluorine ion implantation is duscussed. All phases of the experiment are described and the results are presented. Experimental conclusions and comments are included. Some future directions of this experiment are discussed.

Chapter 1
Introduction

In this chapter, a basic understanding behind metal-oxide-semiconductor (MOS) capacitor research is presented in combination with the use of the element fluorine as an implanted species. Some of the how's and why's as to the nature of the fluorine within the MOS devices are given and are tied to some of the current research being carried on here at Lehigh University. An explanation of the thesis experiment and its relationship to the above mentioned topics is covered in an attempt to clearly define the problem(s) to be attacked.

1.1 Importance of MOS Capacitor Research

Many of today's microelectronic circuits and components utilize the MOS capacitor as their building block. For example, charged-coupled array devices (CCD's), and metal-oxide-semiconductor field-effect-transistors (MOSFET's), rely essentially on the response of an MOS capacitor to a variety of applied gate biases, (commonly considered to be a gated structure, discussed in detail in Chapter 2) and act primarily in the controlling of charge and current flow within a particular device. With such a powerful capability at its fingertips by structural design, it becomes necessary to more fully understand the MOS capacitor by imposing slight alterations within the device and researching the changes that occurred during the experimentation.

For this reason, much effort within the area of applied solid state research is concentrated on the MOS capacitor as a test element. Although the structure may appear quite simple, unlocking all of its secrets is a true challenge for the device engineer. In addition, the proper utilization of the MOS capacitor takes on a vital role in fundamental research and circuit design.

1.2 Fluorine Implantation Measurements and Studies

As stated previously, the alteration of the MOS structure from its norm is a basic experimental practise used for procurring fundamental knowledge in order to improve upon existing device designs. With the advent of specialty implants, many different elements and various compounds have been tried in hopes of gaining information about the Si/SiO_2 layers, or to achieve a special effect. Alot of emphasis has been directed towards halogen implantation studies[1,2], and although chlorine was the frontrunning halogen earlier on, recently fluorine seems to be the Group VIIA element receiving more attention with regards to implantation into silicon and silicon-based devices.

Studies of implanted fluorine have occurred on various levels for different reasons in order to gain pertainent knowledge of this element's capabilities. Fluorine has been implanted into the insulator-substrate structure[1,3], and then turned into a device, as well as being implanted through the entire MOS capacitor to observe the gate dielectric effect[4]. Both Si-bulk[5,6] and Si/SiO_2 interface[7-10] studies with fluorine have been successfully carried out and provide useful information about this element and its potential use in microelectronic fabrication. It has been shown[10-12], that during the growth of oxides on Si-

wafers, diffused and implanted fluorine can alter the oxidation rate and also reduce oxidation-induced stacking faults[2,9] (OISF's). Fluorine is slowly earning a place among one of the unique atoms to be considered for novel device design, and the processing of silicon-based technology. This will be described in greater detail in Chapter 2.

1.3 Fluorine-Ion Studies

Of course, once implanted in the silicon structure, the question arises about electrical activation of fluorine, and the possibility of mobile F^- ions within an MOS device. Once again, many bulk[5,6] and device-based[1,3,4,7,8] studies have been carried out in order to answer this question concerning fluorine after it enters the Si/SiO_2 system. Some investigate the trapped interface charge, while others compare fluorine with alkali mobile ions such as sodium (Na^+) and potassium (K^+), but obviously with a different charge nature state its ionic character is negative, representative of the halogen group elements.

Hydrofluoric acid (HF) is a widely used etchant in silicon processing. Fluorine residue could be left behind if it dissociates from hydrogen and thus leaving F^-. If this occurs[7], then the studies of implanted fluorine important. Moreover, the ionic radius of fluorine is less than silicon's and this is not the case with ionic chlorine. This suggests that the mobility of fluorine within silicon-based lattice structures is significant and well worth investigation because ionic elements, mobile or fixed, have always played a major role in the fundamental research of MOS systems.

1.4 Purpose of the Experiment

This experiment has been designed to provide information concerning implanted fluorine within the simple test structure of an MOS capacitor by way of fundamental capacitance versus voltage (C-V) measurements. The study of fluorine in silicon has been of some interest to the researchers at The Sherman Fairchild Solid State Laboratory at Lehigh University, and the element's effect on the MOS structure by means of ion-implantation, may produce some results not yet determined by this lab's previous work. It can be stated that this thesis project has been constructed to challenge a current topic of MOS device research, while providing the student with complete hands-on processing from start to finish. The comparison of unimplanted samples to implanted ones is used for this work and is an effective technique to draw conclusions as to the effect fluorine has when it exists in the midst of the Metal/SiO_2/Si structure.

Chapter 2
Theory and Background

This chapter is broken into three areas of information in order to more fully understand the experiment itself as described within Chapter 3. First the general low frequency and high frequency MOS capacitor theory is explained by way of energy band diagrams, ideal C-V curves, and equivalent circuit models. Second a fundamental definition of ion implantation and ion implantation systems is presented as a means to expose the reader to the central experimental tool used in this thesis project. Third a discussion of fluorine as both an element and an ion and its relative importance to ion implanted MOS devices. The background material is essentially focused towards a specific problem tackled in MOS capacitive research, and should more clearly define the direction of the experiment which was carried out in this thesis.

2.1 Frequency Response of MOS Capacitors

The basic configuration of an MOS capacitor is shown in Figure 1 and by design is just a sandwich of different materials between two metal plates. This fabrication process is carried out in general, by thermally growing an oxide on top of an n or p-type silicon substrate, which is then metallized front and back, usually with aluminum, to form both gate and substrate contacts on the device structure. The details of this procedure in conjunction with the remainder of the

thesis experiment are clearly laid out in Chapter 3, and will be taken up again at that time. Now that the device is completed, it becomes important to understand its behavior as a test element.

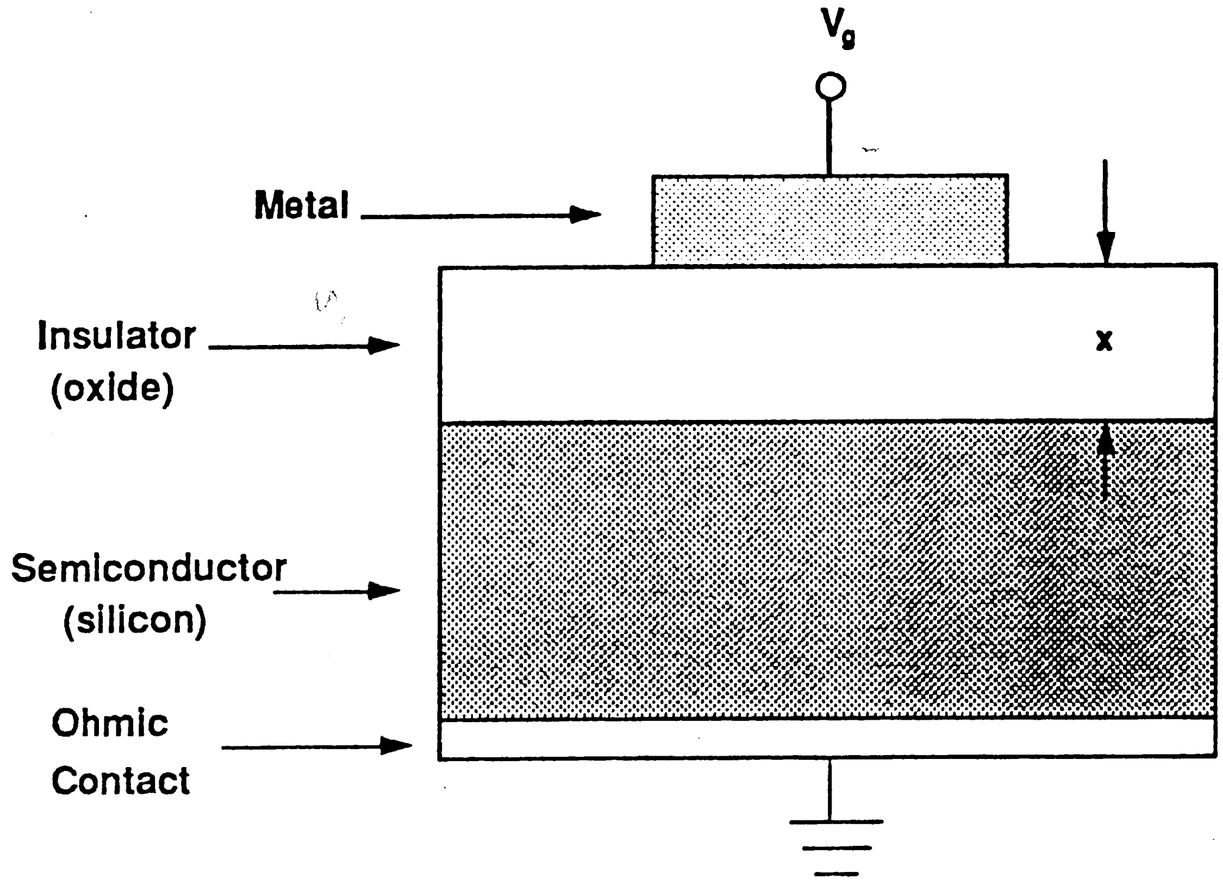


Figure 1. MOS Capacitor's Fundamental Structure[13]

The most fundamental means in which one can determine both the charge storage capabilities and the charge response or activity within the MOS capacitor is by the use of an AC/DC coupled system. A ramped DC voltage is applied to the gate of the device while a small amplitude AC signal of constant frequency superimposed. The ramp voltage is needed to create a varying electric field within the MOS system and the AC signal is an indicator of the response of the electrical carriers under the applied $\mathcal{E}$-field. The capacitance of the test structure can then

be determined for a given AC frequency.

It becomes obvious that the capacitive response is mostly dependent upon the AC frequency and complete testing must occur at both high and low AC frequencies. Two levels of frequency measurement have been set by industrial research as a way to fully comprehend the capacitor's performance capabilities. Low frequency ($\simeq$ 10 Hz), allows the observer to determine whether or not the surface can be inverted to a capacitance level of the oxide, while at high frequency ($\simeq$ 1 MHz), the minority carriers cannot respond to the rapid AC signal and therefore do not contribute to the measured capacitance. Each one of these particular cases will now be explained by the use of device Physics applied to MOS capacitors.

Finally before formally addressing the frequency analysis, two capacitances should be defined for the MOS system. The first is known as the static capacitance given as

$$C_{STAT} \equiv \frac{Q_T}{V_G} , \qquad (2-1)$$

where Q_T is the total charge density on the capacitor, all that comes between the two metal plates as viewed in Figure 1, and V_G is the gate bias applied to it. The second type is named the differential capacitance defined as

$$C \equiv \frac{d\,Q_T}{d\,V_G} . \qquad (2-2)$$

It should be noted that these two capacitances will not be alike since the charge

on the MOS capacitive structure can vary nonlinearly with voltage. For this reason, the differential capacitance plays a more important role in MOS capacitor measurements because the small-signal data truly determines the rate of charge change with respect to the gate voltage. On this premise, both the ideal C-V curves and the expressions for the small-signal differential capacitance of the MOS structure can be derived.

2.1.1 Ideal Small-Signal Equivalent Circuit

In deriving an accurate small-signal equivalent circuit for an MOS capacitor, it becomes important to separate those terms which are time-dependent with regards to the AC signal and those which are not time-independent. Therefore, two simple analyses are required in order to determine all the components needed for complete modeling is the ideal case. It essentially stems from the differential capacitance and can be calculated from the non-equilibrium and equilibrium conditions of Gauss' law applied to the charge in the silicon and the field within the oxide. The result is the total capacitance inside the MOS structure consisting of both a bias dependent component element and a non-bias dependent component element.

First begin with a definition of the differential capacitance relating the silicon surface charge density, Q_S, to the small-signal AC gate bias, V_G, or

$$C \equiv - \frac{\Delta Q_S}{\Delta V_G} . \qquad (2-3)$$

As one will notice, Δ 's are used to indicate the affectation brought about by

small amplitude time-varying voltage. This formula can be further subdivided into the product of two Δ-expressions as follows,

$$C = -\frac{\Delta Q_S}{\Delta \Psi_S}\frac{\Delta \Psi_S}{\Delta V_G} , \qquad (2-4)$$

where Ψ_S is the silicon band bending surface potential established by V_G. Of these expressions, it should be clear that $-\Delta Q_S/\Delta \Psi_S$ is time-dependent since the change in the surface potential is directly affected by variations in the gate voltage which in turn affects the rate of change of charge. This indirect relationship possesses the common link of time which is suppplied by the AC signal. On the other hand, $\Delta \Psi_S/\Delta V_G$ are in direct relation to each other because it is one voltage creating another and the need for time dependence is not necessary.

Bearing this in mind, consider a time-dependent equation of Gauss' law which now relates the charge per unit area in the silicon to the field in the oxide such that,

$$C_{ox}[V_G(t) - \Psi_S(t)] = -Q_S(t) , \qquad (2-5a)$$

and C_{ox} is known as the oxide capacitance which will be defined explicitly in a later section, and the voltage difference between $V_G(t)$ and $\Psi_S(t)$ is the voltage across the oxide. By employing a Δ-variation to each time dependent term, that is to say for example, the Δ corresponds to a small AC voltage on the gate bias, V_G, or

$$V_G\ (t)\ = V_G + \Delta\ V_G\ (t)\ \ . \qquad (\ 2\ -\ 6a\ )$$

The same can be applied to both the band-bending, $\Psi_S(t)$, and the surface charge density, $Q_S(t)$, in the silicon. It can be shown[14] that in the small-signal regime a first term Taylor series expansion may be utilized to equilibrate the silicon surface charge density to the capacitance per unit area in the silicon, $C_S(\Psi_S)$, as the following Δ-expression,

$$C_S(\ \Psi_S) \equiv\ -\ \frac{\Delta\ Q_S}{\Delta\ \Psi_S}\ \ . \qquad (\ 2\ -\ 7\ )$$

The result is a bias dependent capacitance affected by a time varying input signal.

Now consider the other case in which formula (2-5a) is modified slightly to what can be called an equilibrium or a no AC excitation condition is then written as,

$$C_{ox}\ (V_G\ -\ \Psi_S\ ) = -\ Q_S\ \ . \qquad (\ 2\ -\ 5b\ )$$

If the Δ substitutions are employed again into (2-5a), but in an equilibrium state (time-independent), that is to say, that equation (2-6a) would be altered to look like

$$V_G\ (t) = V_G + \Delta V_G\ \ , \qquad (\ 2\ -\ 6b\ )$$

which contains no time dependence for its approximation as prescribed. A new Δ-expression can now be derived[14] by making all the necessary changes in (2-5a) to follow suit as in (2-6b) and along with the remainder of the analysis previously described. By subtracting (2-5b) from the new-found version of (2-5a) one can arrive at

$$\frac{\Delta \Psi_S}{\Delta V_G} = \frac{C_{ox}}{[C_{ox} + C_S(\Psi_S)]} , \qquad (2-8)$$

which is the equilibrium Δ relation needed to complete the model.

Realizing that formula (2-4) can now be redefined in terms of two capacitances, it is rewritten as

$$C = \frac{C_S(\Psi_S)\, C_{ox}}{C_{ox} + C_S(\Psi_S)} . \qquad (2-4)$$

This however, is just the formula for two capacitors in series and the inverse of the total capacitance is just the sum of the its individual inverses or,

$$\frac{1}{C} = \frac{1}{C_S(\Psi_S)} + \frac{1}{C_{ox}} . \qquad (2-9)$$

This simple circuit makes up the ideal MOS capacitor model and is depicted in Figure 2. Due to its bias dependent nature, $C_S(\Psi_S)$, is shown as a variable capacitor. The ideal MOS capacitor circuit is now investigated at both low and high AC frequencies and its capacitive response is plotted against a DC ramped voltage applied at the gate for a greater understanding of the charge nature

associated with the device.

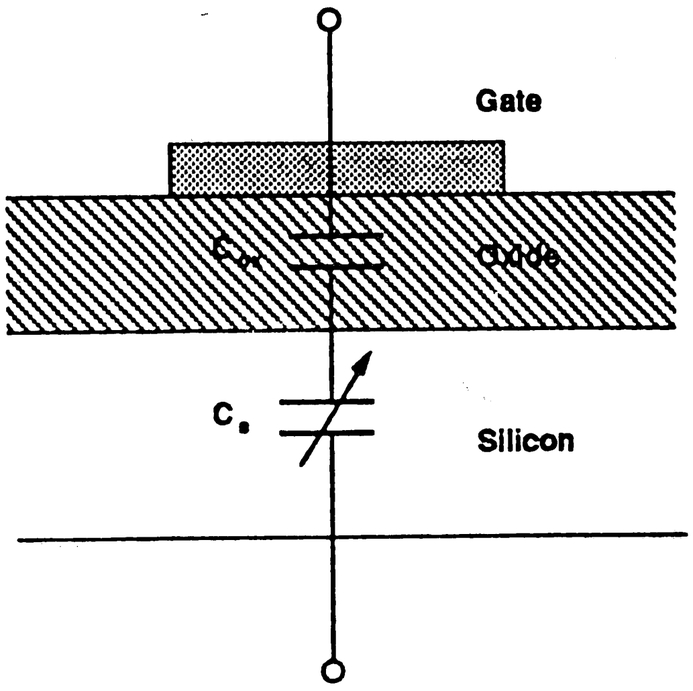


Figure 2. MOS Capacitor's Small-Signal Equivalent Circuit[15]

2.1.2 MOS Capacitors at Low Frequencies

As stated earlier, previous workers have used 10 Hz for the low frequency electrical characterization. There are three conditions associated with the low frequency C-V in response to the gate voltage sweep. They are: 1) accumulation, 2) depletion, and 3) inversion. They can be understood as a function of gate bias, formulas related to the theory for the device, and MOS energy band diagrams which depicts the electrical carrier distributions at selected points during the sweep. The theory is compared to the experiment for the case of a p-type silicon in Chapter 3.

First consider the MOS capacitor having a negative DC voltage applied to its gate. The negative bias implies that the semiconductor surface potential, Ψ_S, is also negative. This tends to attract holes (majority carriers) within the silicon

substrate (p-type) to its surface. If the hole population is great enough at the Si/SiO_2 interface; that is, if the hole density at the Si-surface exceeds the Si-bulk hole density by a sizeable amount, one can then say that the MOS capacitor is in an accumulated state. Considering the limiting case of the total capacitance formula (2-4), the gross density of holes at the substrate surface produces a large differential capacitance; thus C_S can be thought of as being much greater than C_{ox} ($C_S \gg C_{ox}$) and the capacitance per unit area in accumulation is just that of the oxide capacitance or,

$$C_{accum.} = C_{ox} = \frac{\epsilon_{ox}}{x_{ox}} . \qquad (2 - 10)$$

In this formula, ϵ_{ox} is known as the permittivity of the oxide so for SiO_2, ϵ_{ox} is 3.9 times that of the permittivity of free space ϵ_o. The remaining term, x_{ox}, is simply the oxide thickness of the sample which sits beneath the metal gate.

Figure 3 is a drawing of the MOS capacitor's energy band structure during accumulation. As one can see, the higher concentration of holes near the semiconductor surface bends the valence band (E_v) upward toward the Fermi level (E_{Fs}) and causes a similar bending in both the intrinsic band (E_i) and conduction band (E_c) energy levels. This is an obvious response to the initially applied negative gate voltage whose electron energies are now at a higher level in the metal than in the semiconductor. Therefore, the Fermi level within the metal (E_{Fm}) is displaced from its equilibrium position by the applied potential of qV. The offset that now exists between E_{Fm} and the Fermi energy level in the semiconductor (E_{Fs}) has created as oxide conduction band tilting, which increases

as one moves closer to the interface of the metal gate and the silicon dioxide. The name applies to the resulting electric field within the oxide whose directional arrow points to the rise in electron potential.

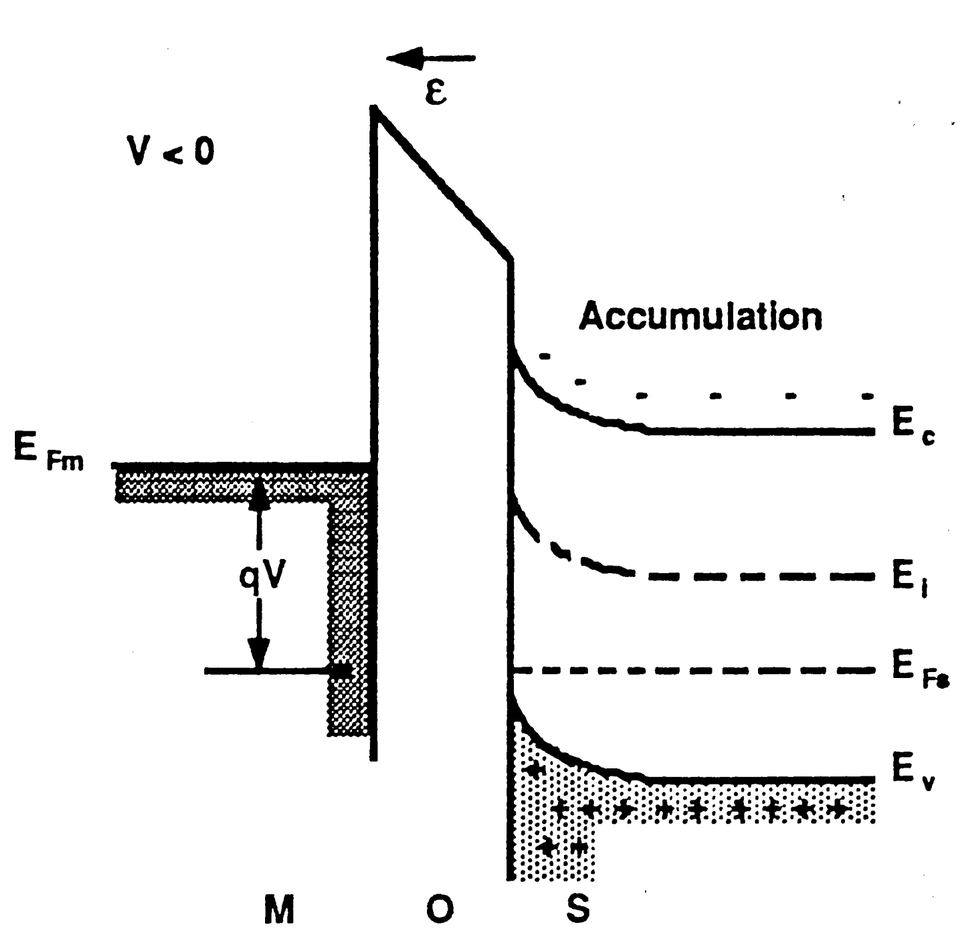


Figure 3. MOS Capacitor in Accumulation[16,17]

As one decreases the magnitude of the gate bias, the surface hole density decreases, corresponding to a smaller C_S and a total C which is below C_{ox}. At the same time, the degree of band tilting in the oxide and band bending in the semiconductor becomes less and less pronounced until an applied gate voltage exists which flattens out the set of bands completely. This particular bias is known as the flat-band voltage, or V_{FB}. In an ideal situation this value should be zero ($V_G = V_{FB} = 0$) in addition to a semiconductor surface potential of the same value ($\Psi_S = 0$).

Due to the dependence of C_S on Ψ_S a flat-band condition capacitance can be defined generally as,

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_S(\Psi_S = 0)} \ , \qquad (2\text{-}11)$$

where $C_S(\Psi_S = 0)$ is known as the semiconductor flat-bnd capcitance (C_{FBS}) more specifically defined in the following way,

$$C_S(\Psi_S = 0) = C_{FBS} \frac{\epsilon_s}{\lambda_p} \ , \qquad (2\text{-}12)$$

where ϵ_s is the permittivity of the semiconductor (in silicon, ϵ_s is 11.7 times that value of ϵ_o) and λ_p is the extrinsic Debye length in a p-type semiconductor. This term can be further defined,

$$\lambda_p = \left(\frac{\epsilon_s \ kT}{q^2 \ N_a}\right)^{1/2} \ , \qquad (2\text{-}13)$$

and is determined by semiconductor parameters (ϵ_s, N_a) and the temperature of operation. Although the flat-band condition occurs at only one particular gate bias, it will become more apparent how important it is in analyzing the experimental MOS capacitor's deviation from the ideal as the results are presented in Chapter 4.

Next the condition of depletion occurs when the gate voltage is more positive than the flat-band voltage and begins to repel holes away from the surface of the silicon. The total capacitance is once again the series combination

of C_{ox} and $C_S(\Psi_S)$ but now the semiconductor surface potential is greater than zero, or

$$\frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{1}{C_S(\Psi_S > 0)} , \qquad (2 - 14)$$

where $C_S\ (\Psi_S > 0)$ is explicitly defined as,

$$C_S(\Psi_S > 0) = \frac{\epsilon_S}{x_d} . \qquad (2 - 15)$$

So the capacitance being measured within the silicon is just the capacitance across the region, x_d, which is similar to a n^+- p abrupt junction for which the depletion region extends almost entirely into the p region (similar to the p-type substrate),

$$x_d = \left(\frac{2\epsilon_S \Psi_S}{q N_a}\right)^{1/2} . \qquad (2 - 16)$$

It should be understood that the case of depletion in an MOS capacitor only occurs within the boundary of Ψ_S being greater than zero or less than Ψ_p ($\Psi_p > \Psi_S > 0$). Note that Ψ_p, the built-in bulk potential of a p-type substrate is given by,

$$\Psi_p = \frac{kT}{q} \ln\left[\frac{N_a}{n_i}\right] , \qquad (2 - 17)$$

and is essentially determined by temperature and doping density. This range of potentials will correspond to a small range of V_G 's which appear on a standard

C-V plot and can be sighted as the region of depletion capacitance.

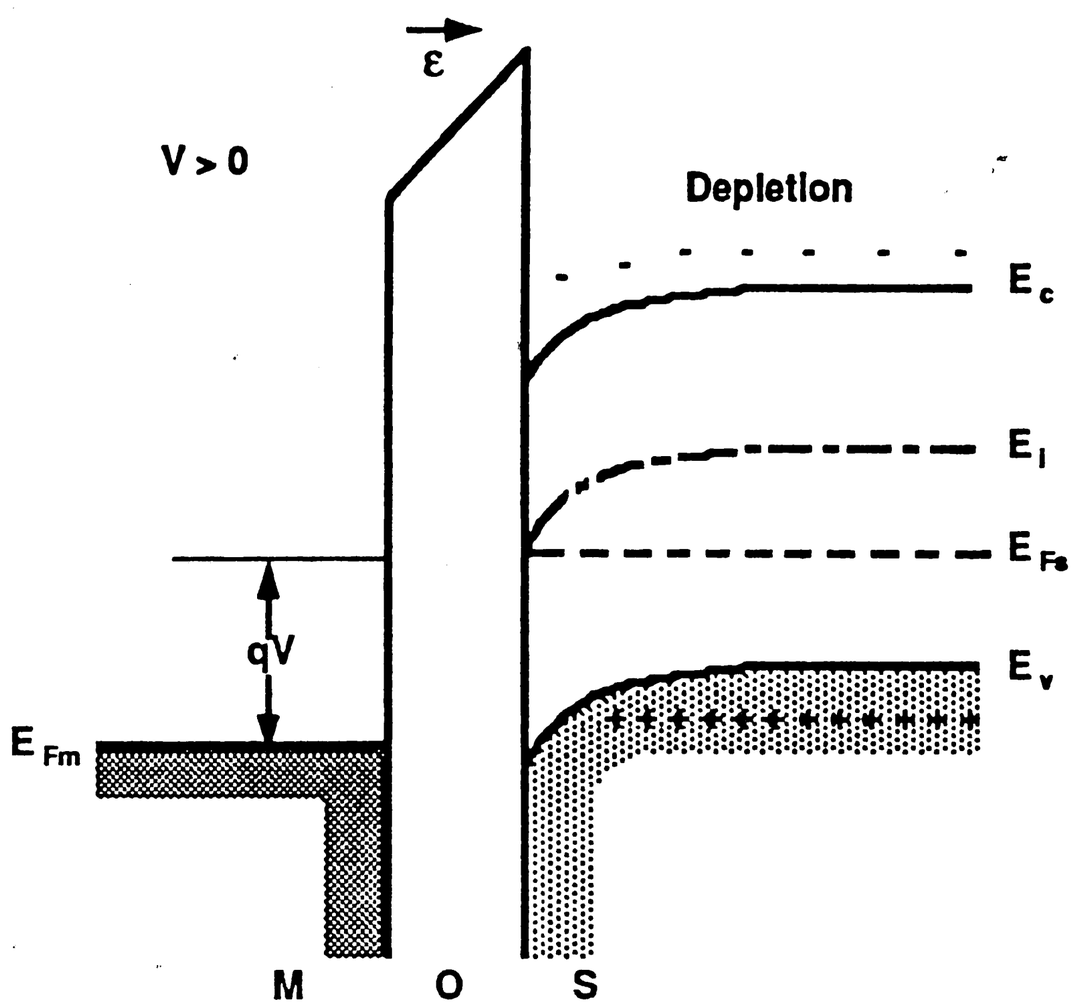


Figure 4. MOS Capacitor in Depletion[16,17]

Depletion is depicted with an MOS energy band structure in Figure 4. It describes the condition stated above, the positive applied voltage depletes the surface of the positive charge in the valence band. With the advent of the positive gate bias, the Fermi level E_{Fm} is below E_{Fs} which results in a situation opposite to that of accumulation. The band bending in the silicon is now downward, an indication of depleted positive surface charge within the semiconductor $\mathcal{E}$-field in the oxide is in the opposing direction causing the conduction band in the oxide to be tilted upward towards the silicon.

Finally, inversion of the semiconductor surface arises for larger positive values of gate voltage. The minimum voltage required is Ψ_p, which is known as

the onset of inversion. However, in a practical sense, in order to have a true n-type conducting channel existing at the surface, it is recommended that Ψ_S be equal to twice the value of Ψ_P. This is considered to be strong inversion and this will be used as the threshold for our calculations.

As stated previously as is evident from formula (2-16), x_d will increase as Ψ_S increases. By the time $\Psi_S(\text{inv.}) = 2\,\Psi_P$, the maximum depletion region width for steady-state conditions has been achieved,

$$x_{d\,max} = \left(\frac{2\epsilon_s\,\Psi_S\,(\text{inv.})}{q\,N_a}\right)^{1/2} \qquad (2-18)$$

$$= \left(\frac{4\,\epsilon_s\,kT\ln\,(N_a/\,n_i)}{q^2 N_a}\right)^{1/2},$$

the second equation is derived by using the above expression for $\Psi_S(\text{inv.})$ and equation (2-17). The corresponding relations for the capacitance in the semiconductor and the total capacitance under the condition of inversion are easily stated,

$$C_S\,(\,\Psi_S\,(\text{inv.})) = \frac{\epsilon_s}{x_{d\,max}}\,, \qquad (2-19)$$

and

$$\frac{1}{C_{inv}} = \frac{1}{C_{ox}} + \frac{1}{C_S\,(\Psi_S(\text{inv.}))}\,. \qquad (2-20)$$

The pictorial view of inversion is given in Figure 5 and clearly shows much greater upward oxide conduction band tilting toward the semiconductor, and extreme downward band bending within the silicon due to the much higher

applied gate voltage.

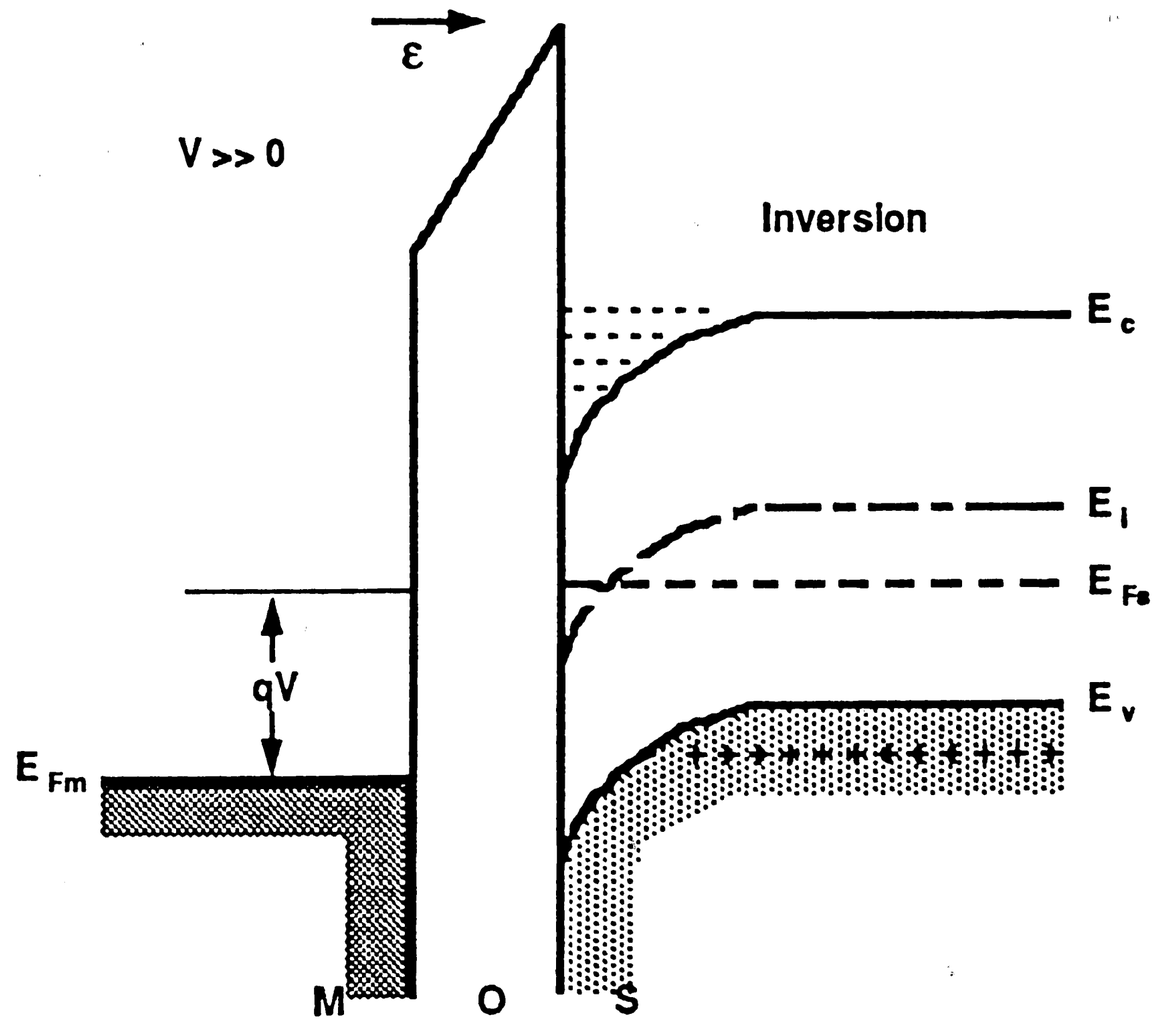


Figure 5. MOS Capacitor in Inversion[16,17]

In fact, the diagram indicates that E_i is below E_{Fs} which results in a large electron population in the conduction band of the silicon. This surface layer of electrons is similar to n-type semiconductor. Note that these electrons are minority carriers within the p-type semiconductor, which as a result of the gate bias form the inverted layer of n-type charge at the p-type substrate surface.

This concludes the basic low frequency analysis of MOS capacitors in generating C-V curves. The topic will be brought up again at the end of the next section in order to compare the high frequency response to the low frequency response. This will reveal the unique and characteristic properties of each test frequency and why both are necessary in understanding the capacitive-voltage

behavior of this device test structure.

2.1.3 MOS Capacitors at High Frequencies

High frequency operation, that is as AC small signal of 1 MHz, has both similar and different C-V responses in comparison to the low frequency C-V. There exists no discrepency for the first two conditions described in subsection 2.1.2, which states that at high frequencies an MOS capacitor will accumulate and deplete, as one recalls, these cases describe the actions of majority carriers (holes) at a p-type silicon substrate surface in response to an applied gate voltage. However, for inversion, minority carriers, and in this case electrons are the active element at the semiconductor surface.

In order to properly form as inversion layer it becomes clear that a certain amount of time is required for the minority carriers to populate the surface creating an n-type region. It has been shown[18] that a characteristic inversion layer formation time for an MOS capacitor biased in inversion is on the order of

$$t_{(inv.)} \simeq \frac{2\,N_a\,\tau_o}{n_i}\,, \qquad (2-21)$$

where τ_o is the minority carrier lifetime at the surface. Since this is inversely proportional to frequency there exists an obvious correlation between the formation time and the AC small-signal frequency applied to the metal. Using a typical[18] lifetime value of $1\mu s$ and the doping concentration of experimental wafers ($2 \times 10^{15}/cm^3$), the time is calculated roughly to be 0.28 s. This indicates that a very slowly changing (low frequency) small--signal measuring voltage is

needed to achieve an inversion condition. Otherwise, the surface does not invert and the result is the high frequency C-V curve depicted in Figure 6. The capacitance levels out at the minimum given by formula (2-20), the series combination of the oxide capacitance and the substrate capacitance with its depletion width at its maximum ($x_{d\ max}$).

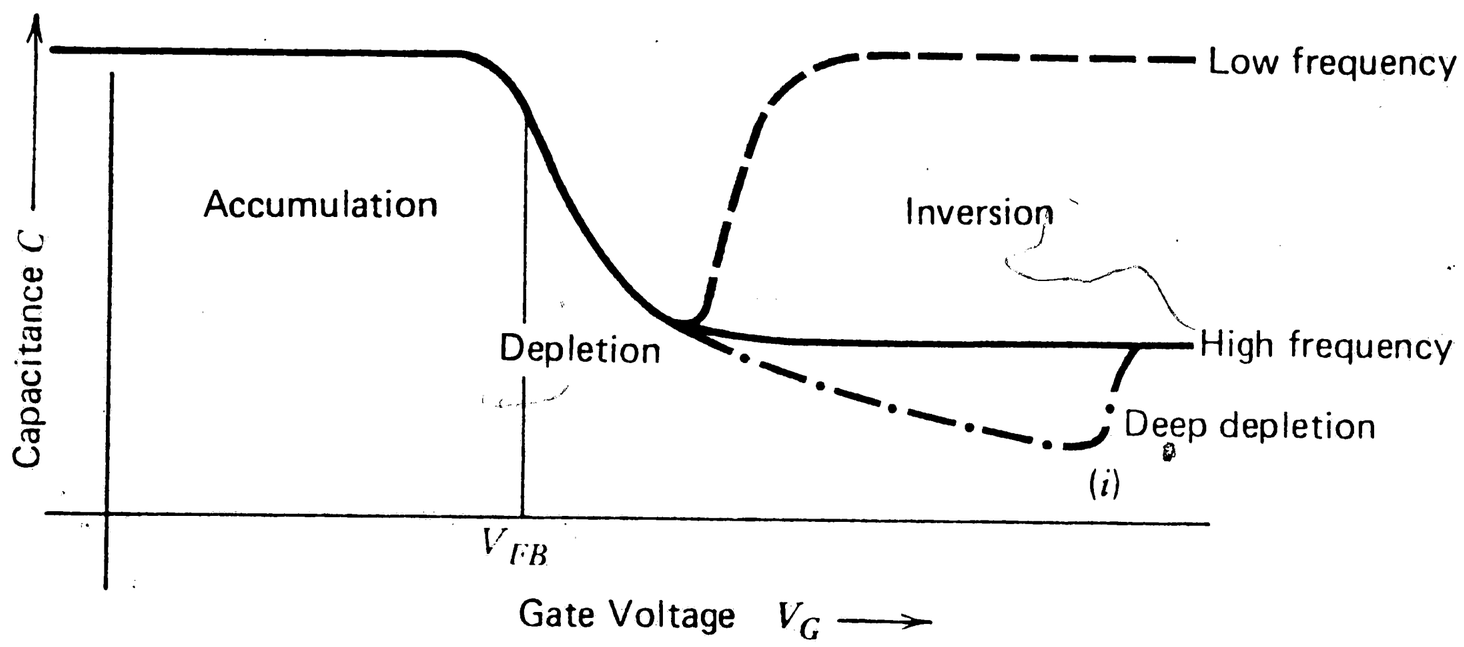


Figure 6. Ideal C-V Curves of an MOS Capacitor[19]

It is now seen from the figure that three conditions stem from the cases of inversion based upon their response to the gate bias. First, when the frequency is approximated by the inverse of formula (2-21), the inversion-layer population can follow both the AC small-signal voltage and the DC gate bias, producing a level of capacitance ideally equal to C_{ox}. This is because the signal sampling in the semiconductor only occurs at the surface and not through the depletion region and the result is similarto that of a parallel plate capacitor of value C_{ox} just as in accumulation. Second, as the AC frequency is pushed to a high enough level so as

not to form a minority carrier inversion but still reponds to the DC gate voltage, then the high frequency minimum capacitance level is achieved. This is set by the positive metal bias needed to maximize the depletion width within the substrate. Third, if the MOS capacitor reaches a point where both the gate bias and the small-signal voltage vary at a faster rate than can be accommodated by the device, deep depletion will occur and the capacitance never reaches a minimum. The reason is that the depletion width is now wider in distance than even $x_{d\ max}$, which exceeds the conditions of inversion.

As one shall see, these characteristics are not uncommon to experimental data and will be discussed again in Chapter 4. It should be noted that at very high biases, the deep depletion curve may relax to the constant minimum capacitance (as shown in the figure by (i)) set by the high frequency inversion case. This completes all of the ideal conditions of an MOS capacitor at high and low frequencies and should provide enough of a background to comprehend the device analysis of the results in a later chapter.

2.2 Oxide and Interface Charge

Up until now, the information concerning MOS capacitors and C-V curves has been strictly ideal is its analysis. That is to say, both the oxide grown and the semiconductor surface and bulk have been void of any defects or nonuniformities. This is not the case with regards to the processing world and can become quite a problem in device testing and electrical characterization since any kind of abnormality will cause a stray from the ideal. This section is devoted to defining some of the variations occuring within the SiO_2 layer, at the Si/SiO_2

interface, and inside the Si-bulk. Their effects will be explained by the use of an MOS structured diagram, a C-V curve, and a circuit model more advanced than that of Figure 2, employing an R-C network for its design.

It is best to begin by defining the types of defects existing within the MOS capacitive structure and the effects they have in altering C-V measurements. Figure 7 depicts all the major charge catagories of an MOS device and their corresponding numerical densities (for example, $N_m = Q_m/ q$) and listed here as follows with a brief explanation. They are:

a) Mobile ionic charges (Q_m, N_m) such a sodium (N_a^+), or other alkali elements which are absorbed into the silicon dioxide during the application of the metallizing process. Their ability to drift is caused by both $\mathcal{E}$-field and temperature dependent and influences the flatband voltage change (ΔV_{FB}). It should be noted the fluorine (F^-) is pictured on this diagram because this thesis suggests the presence of a mobile fluorine ion.

b) Oxide-trapped charges (Q_{ot}, N_{ot}) are positive (holes) or negative (electrons) charges which have been literally trapped within the bulk of the oxide. This results from irradiation which injects electrons or photons into the insulator layer.

c) Fixed oxide charges (Q_f, N_f) are the positive charges lying within the native oxide layer (SiO_x) which is about 25 Å thick and sits on top of the semiconductor-oxide interface. These are due to structural defects correlated to the oxidation process where interfacial dangling or uncompleted silicon-to-silicon bonds may exist.

d) Interface trapped-charges (Q_{it}, N_{it}, D_{it}) appear directly at the Si/SiO_2 interface and have energy levels distributed within the forbidden-gap region (between E_V and E_C). These positive and negative charges are due to silicon surface defects and wafer processing steps which results in the formation of extra allowed energy levels not normally present within the bulk of the crystal. However, a trapped interface charges in contact with the semiconductor substrate can have their charge state altered by charging the surface potential (Ψ_S).

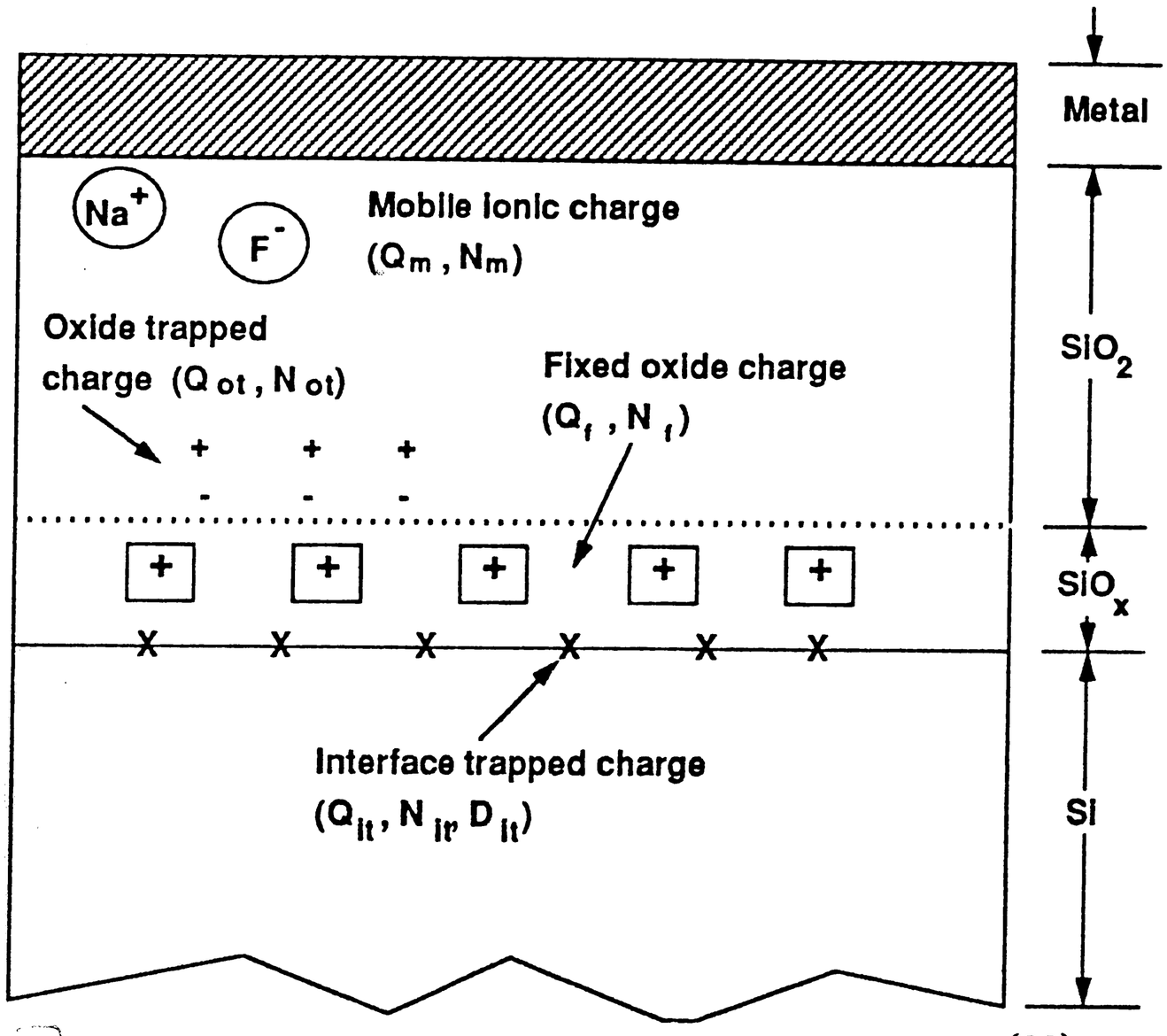


Figure 7. Charge Definition in an MOS Capacitor[20]

The capacitance-voltage (C-V) dependence upon trapped and mobile charges within the MOS structure branches into two cases, both of which affect the flat-band voltage. One case refers to stable charges resulting in a direct translation of the C-V curve along the gate voltage (V_G) axis. The other case

speaks of unstable charges causing distortions in the C-V curves and the dependency of these charges to the applied V_G.

With reference to stable charge analysis, one includes the effect of fixed interface charge density (Q_f), oxide trapped-charge density (Q_{ot}), and mobile ionic charge density. This makes for two terms, one associated with the Si/SiO_2 interfacial layer, and the other a lumped oxide charge term which is generalized for an arbitrary distribution of charge ($\rho(x)$). Both effects superimpose and change the flat-band voltage. This is expressed as follows;

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x)\, dx \ , \qquad (2 - 22)$$

where Φ_{MS} is the ideal definition of the flat-band voltage and results from the difference of two material work functions ($\Phi_M - \Phi_S$), Q_f / C_{ox} is the fixed interface charge term of the native oxide, and the integral term is the centroid weighted effect of the distributed charge. Since the discussion deals with stable charges, the result is a rigid shift in the C-V curve along the V_G-axis as depicted by the dashed curve of Figure 8. Thus the shift in the flat-band determines the new range of voltage values at which the MOS capacitor's regions of operation are defined.

On the other hand, when the analysis includes interface trapped-charge density (Q_{it}), the introduction of unstable charges comes into play and distortive effects within the C-V curve arise (the dotted curve of Figure 8). This is because of the voltage dependence associated with this interface charge. A change in gate bias produces variations in Ψ_S and can charge or discharge these energy levels at

the surface.

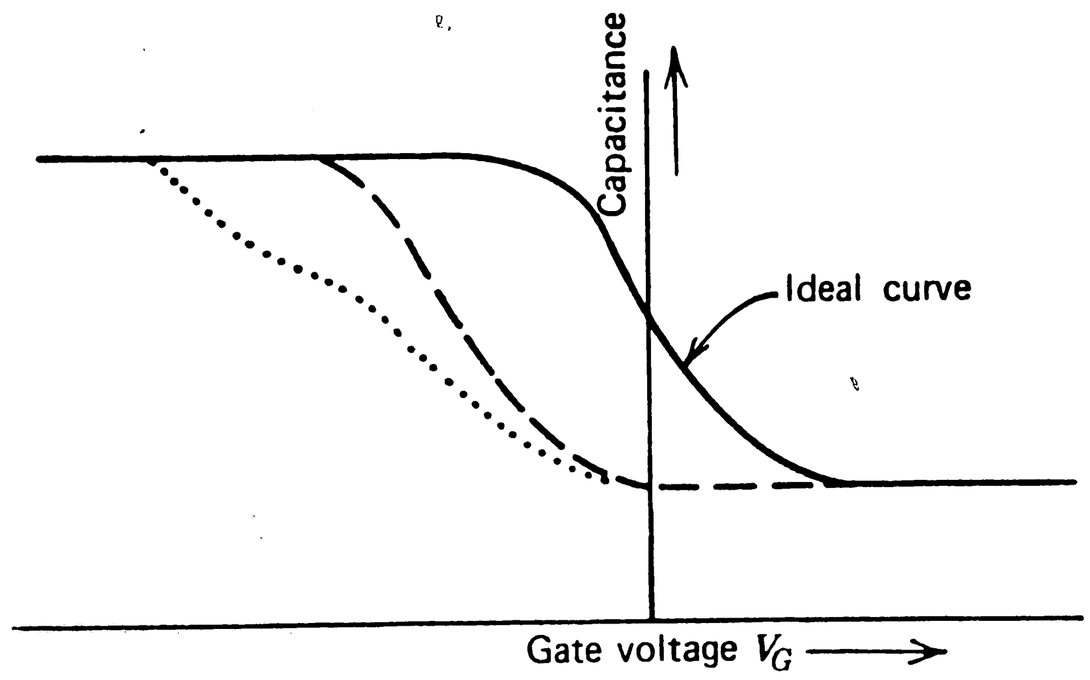


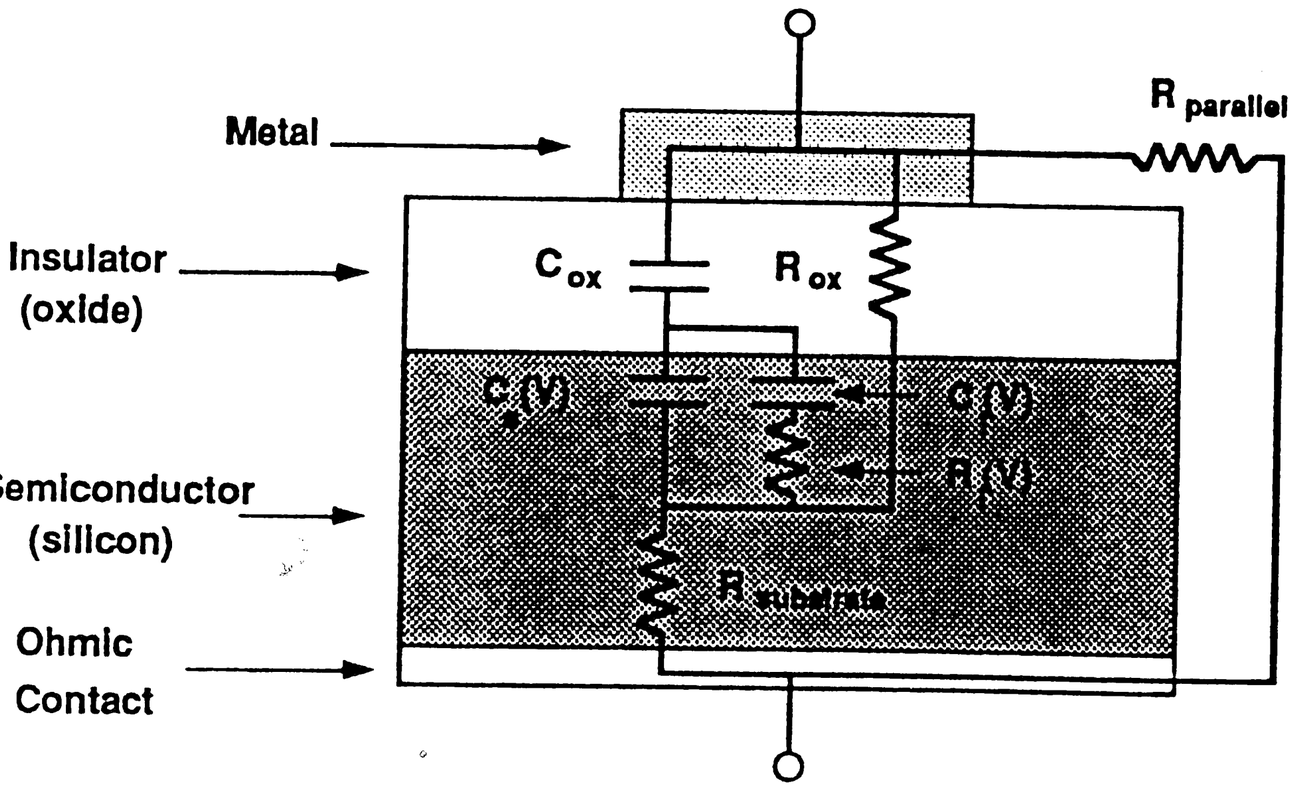
Figure 8. Alterations of the Ideal C-V Curve Due to Charge Formation[21]

This introduces the term Q_{it}/ C_{ox} which when included into equation (2-21) results in a V_{FB} being dependent upon V_G or,

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x)\, dx - \frac{Q_{it}}{C_{ox}} \quad . (2 - 23)$$

Note that the reduction of the density of interface-trapping states (D_{it}) is carried out by a process known as annealing and will be defined and related to this thesis later.

Now that non-idealities of the MOS structure have been defined and their effects on the C-V curve viewed, it becomes clear that this ideal capacitive circuit model of Figure 2 is not complete. Figure 9 offers a suitable R-C network and includes most of the conditions described previously and a few more which shall be addressed at this time.



C_{ox}	Oxide (insulator) capacitance	R_{ox}	Oxide (insulator) leakage resistance
$C_s(V)$	Substrate capacitance (voltage dependent)	$R_{substrate}$	Substrate series resistance
$C_i(V)$	Lumped inversion and trap capacitance and resistance (voltage dependent)	$R_{parallel}$	Device parallel leakage (moisture, contamination)
$R_i(V)$			

Figure 9. Modified R-C Network of an MOS Capacitor[22]

The lumped series branch of $R_i(V)$ and $C_i(V)$ represents a more complicated distributed RC system related to minority carrier generation (inversion) and recombination (interface-trapping) for various voltages. R_{ox} and $R_{parallel}$ can be the results of poor device processing, wafer contamination and moisture problems. $R_{substrate}$ becomes large if the semiconductor resistivity is high and can cause measurement nonlinearities. By placing all of these elements together, a more exact circuit model of a physical MOS capacitor is possible and

most of the non-idealities can be accounted for when comparing the actual to the ideal.

2.3 Ion Implantation

The technique of ion implantation is the introduction of ionized projectile atoms into semiconductor targets with a high enough energy to penetrate beyond the surface regions. Acting as an alternative processing technique to the diffusion of dopants, ion implantation offers a highly controlled means by which impurities can be placed into substrates to alter their electronic properties. This section is devoted to the general understanding of ion implantation in both theory and practice. The fundamental equations of implantation are presented and explained with regard to the actions and results caused by employing this unique device fabrication system. Next the ion implantation machine itself is described and the specific design of the ion implanter system at the Sherman Fairchild Laboratory on the Lehigh University campus is discussed. This background material will assist the reader in comprehending the reasons behind the experiment's design (Chapter 3) as well as interpretation of any results or effects from the tested MOS capacitors (Chapter 4).

2.3.1 Ion Implantation Fundamentals

The methodology associated with ion implantation is to take an energized gaseous source, select from it a particular element or compound known as an ion species, finely focus the species into a beam for high voltage acceleration, and deflect this beam in both the x- and y-directions so that it systematically scans a

defined target area where the Si-wafer is seated. Obviously there is a great deal of equipment involved with this process, all of which together makes up an ion implanter system. This will be handled with both schematics and detailed explanations in the next subsection, but having a basic grasp of the theory is required for a complete understanding.

It had been mentioned that the accelerated ion beam scans a defined area within the silicon substrate. A controlled amount of ions forms a beam which is uniformly deposited onto the surface of the wafer. This controlled amount of surface depostion is known as the dosage, ϕ , defined as

$$\phi \equiv \frac{Q}{m\ q\ A} \ , \qquad (2 - 24)$$

and is in terms of atoms/cm^3. The integrated charge, Q, is related to the current (I) generated by the ion beam as it scans for a particular time (t), or

$$Q = \int I\ dt \ . \qquad (2 - 25)$$

The term mq is associated directly with the selected ion species, m, dealing with the ion's charge state (to be discussed again in Chapter 3) and q being the charge on an electron. The term A is simply the defined area over which the beam sweeps. This means an accurate control of the dosage can be obtained and when coupled with a variable high energy acceleration unit, tailor-made device junctions and custom concentration profiles of impurity atoms can be achieved since there exists a direct correlation of ion beam energy and the penetration distance into

the silicon.

As mentioned previously, energy is required not only to ionize the gas source, but also to accelerate the ion beam so that it implants the impurity ions at the proper incident energy. These energetic ions come to rest inside the semiconductor by way of two basic stopping mechanisms. The first stopping mechanism occurs as an energy transfer to the target nuclei, deflecting the projectile ions and dislodging of the target nuclei from their original sites. Allowing E to be the energy of the projectile ion at any distance x within the silicon, one can define what is known as the nuclear stopping power,

$$NS(E)_{nuc.} \equiv N \int_0^{T_m} T \, d\sigma = \left(\frac{dE}{dx}\right)_{nuc.} . \qquad (2-26)$$

The term N is the number of target atoms/cm^3 . The term T is known as the transferred energy and is a function of the incident energy E, the masses of both the incoming ion (M_1) and the target atom (M_2), and the scattering angle, (Θ). The function T is maximum for a head-on collision ($\Theta = 180^\circ$) and is denoted by T_m within the integral. Finally $d\sigma$ is the differential cross section, the effective area presented by the nucleus as a target for the bombarding particles.

The second stopping process concerns the interaction of the ion with both bound and free electrons within the target. As energy is lost by the moving ion the generation of electron-hole pairs is possible. This process, similar to stopping in a viscous medium, can be characterized by the electronic stopping power,

$$NS(E)_{elec.} = \left(\frac{dE}{dx}\right)_{elec.} = k_e E^{1/2} , \qquad (2-27)$$

where k_e is a relatively weak function of elemental prameters such as the atomic numbers and masses for both the incident and target atoms. For example, with an amorphous target such as silicon, the value of k becomes relatively independent of the projectile ($k_{Si} \simeq 0.2 \text{ X } 10^{-15}$ $(eV)^{1/2}$ cm^3) and the approximate value is used.

The two energy loss mechanisms can now be used together to determine what is known as the range of an ion and result in the Lindhard, Scharff, and Schiott (LSS) theory.[23] Their theory states that the two energy functions are recognized as independent of each other and are additive. Thus the total energy loss per unit length is,

$$-\frac{dE}{dx}\Big|_{tot} = \frac{dE}{dx}\Big|_{elec.} + \frac{dE}{dx}\Big|_{nuc.} \qquad (2-28)$$

$$= NS(E)_{tot} \quad .$$

This term is then integrated over the intial incident ion energy to yield,

$$R(E) = \int_0^E \frac{dE}{(dE/dx)_{tot}} \equiv \frac{1}{N} \int_0^E \frac{dE}{S(E)_{tot}} \quad , \qquad (2-29)$$

which the total distance travelled by an ion before coming to rest, or more commonly known as R, the range of ions. Figure 10 gives a two-dimensional view of the ion range (R) along with some of the statistical values which aid in determining the actual depth profile of the implanted impurities mathematically in

a single and multiple dimensions. Using the projected range R_p, and the uncertainty in R_p, better known as the projected straggle ΔR_p, the one-dimensional concentration profile (n(x)), can be calculated. The term $\Delta R\perp$, the transverse (lateral) straggle, is employed in two- and three-dimensional (lateral) depth distribution functions and in particular the analysis of ion implantation through a gate mask (device fabrication technique).

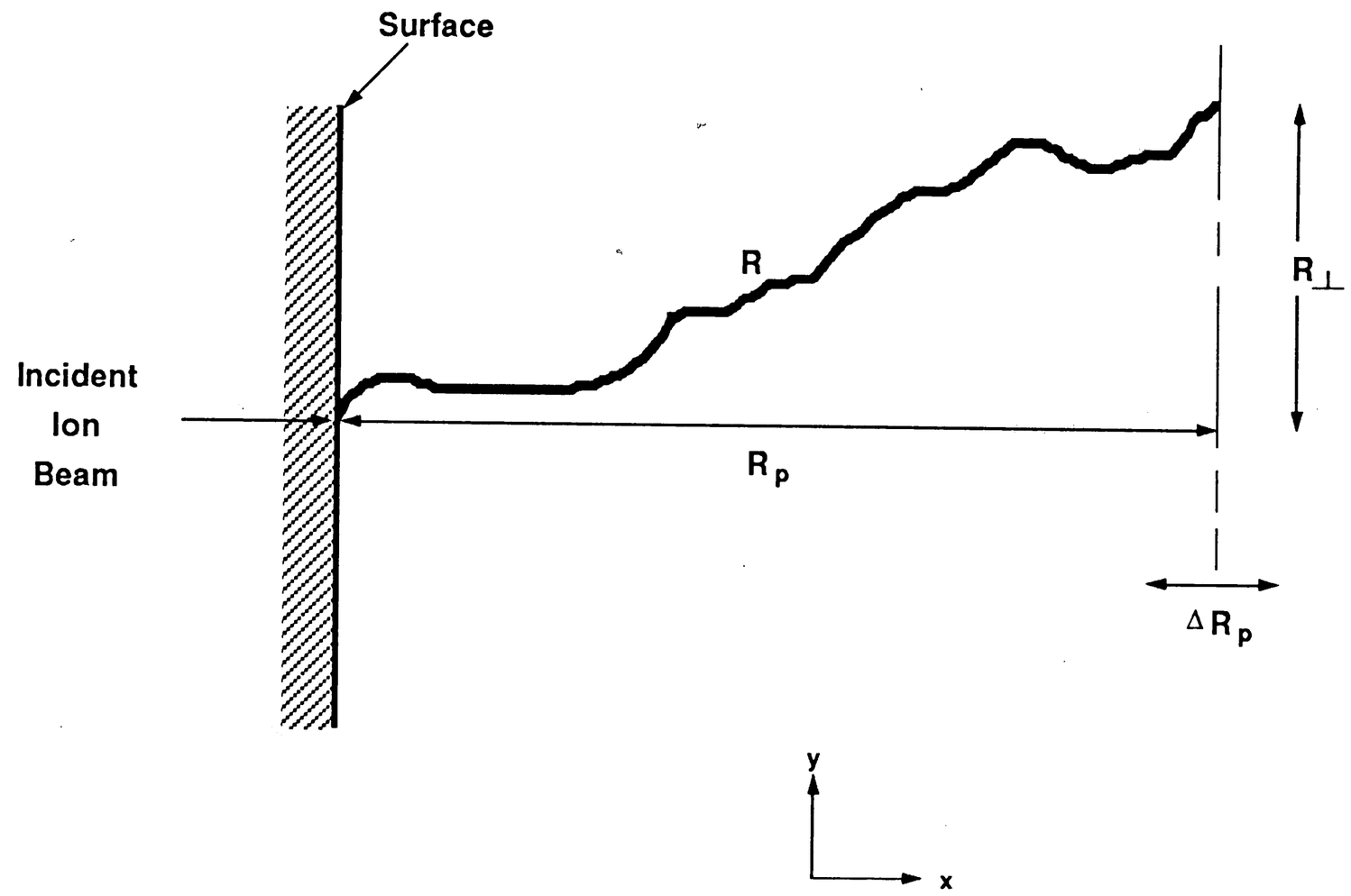


Figure 10. Pictorial Range and Straggle Terms of Ion Implantation[24]

For the time being, a one-dimensional analysis is sufficient. This analysis describes the implanted concentration using a one-dimensional Gaussian distribution function of position x,

$$n(x) = n(R_p) \exp \frac{-(x - R_p)^2}{2 \Delta R_p^2} \quad . \qquad (2 - 30)$$

The leading term, $n(R_p)$, is the maximum concentration occuring at $x = R_p$ and ΔR_p is the projected straggle for the distribution. It is more accurately defined in terms of the dosage, ϕ , and ΔR_p as,

$$n(R_p) = \frac{\phi}{(2\pi)^{1/2} \Delta R_p} \quad . \qquad (2 - 31)$$

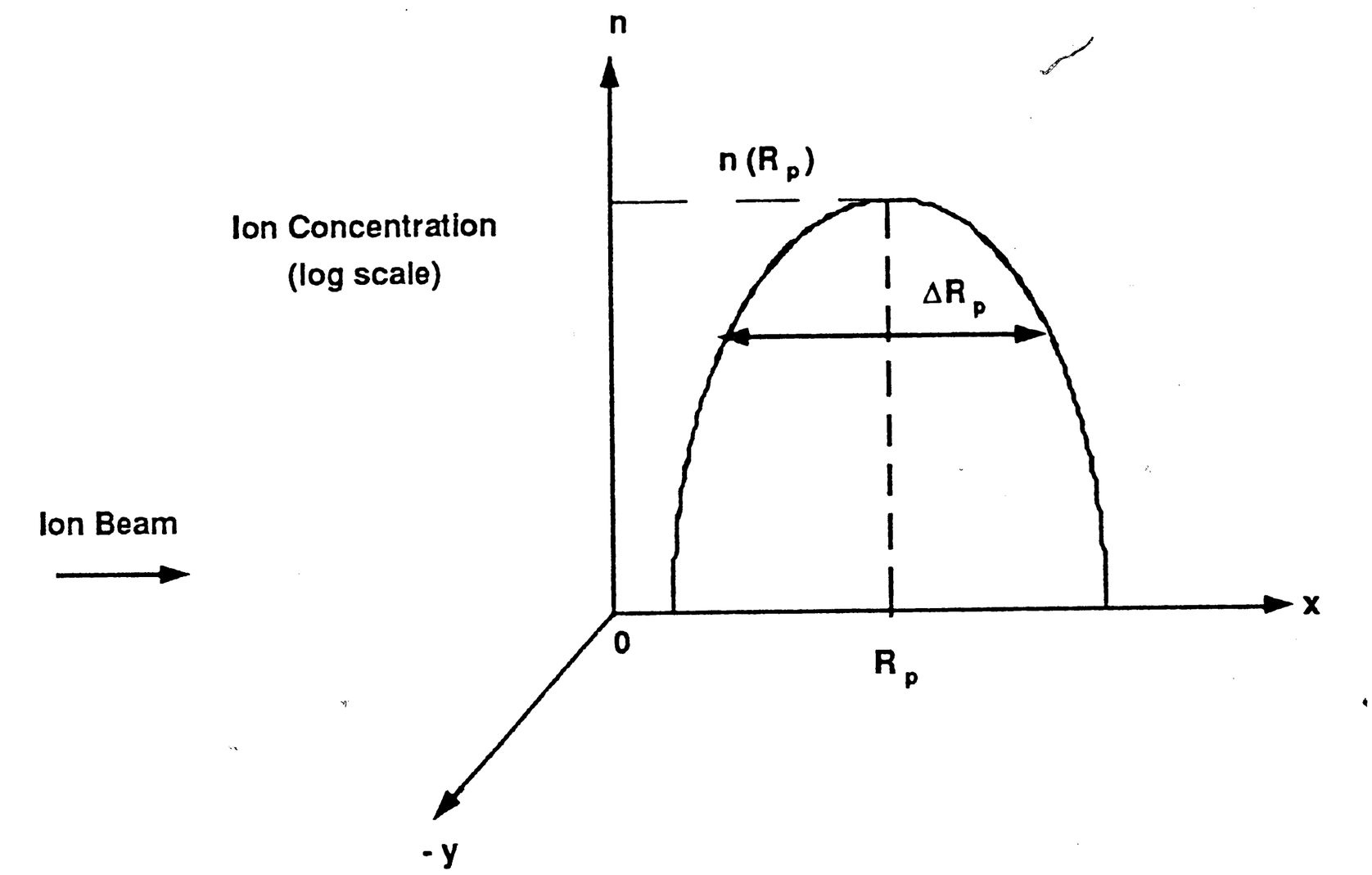


Figure 11. Two-Dimensional Gaussian Concentration Profile[25]

A Gaussian profile is shown in Figure 11 and one should notice how the function is symmetric with respect to R_p along the x-axis. A physical concentration profile of an implant is in most cases asymmetric and therefore the Gaussian becomes inadequate for modeling purposes.

To date, the best simulation uses a Pearson distribution, which is based on the following differential equation,

$$\frac{d\,h(x)}{d\,x} = \frac{(x' - a)\,h(x')}{b_2\,x'^2 + b_1\,x' + b_0}\ , \qquad (2-32)$$

where h is the normalized distribution function. The term h(x) satisfies $\int_{-\infty}^{+\infty} h(x)\,d\,x = 1$, and $x' \equiv x - R_p$. The four constants of this differential equation (a, b_0, b_1, b_2) are defined in terms of four moments and thus the distribution function receives the name Pearson-IV. These four moments are:

1) R_p, the mean range

2) ΔR_p, the projected straggle

3) γ_1, the normalized skewness, and

4) β, the normalized kurtosis.

As from before, R_p and ΔR_p define the Gaussian function while γ_1 accounts for the asymmetry of the profile and β handles the tail of the profile. Thus the Pearson-IV is a Gaussian modified to fit an implanted distribution by way of these four moments. As one will see in Chapter 4, the simulated depth distribution compared to the actual concentration profile provides an excellent fit.

2.3.2 Light Ion Implantation Damage and Annealing

Energetic ions will have many collisons with silicon lattice atoms before coming to rest. The amount of energy transferred to the lattice may cause many

atoms to be displaced, resulting in a cascade of atomic collisions often imparting considerable energy. This bombardment/disorder-forming process is better known as implantation damage, which appears to be deleterious. However the understanding of the lattice damage as related to ion implantation allows for the practical exploitation of this technology.

The nature of the damage created by an incident ion is dependent upon whether it is lighter or heavier than the lattice atoms. Since the thesis revolves around implanting fluorine, an element lighter than silicon, the explanation of damage will only cover light ion implantation. Fluorine implantation into Si-substrates and MOS devices will be addressed specifically in the next section and some of its experimental effects presented later on in this manuscript.

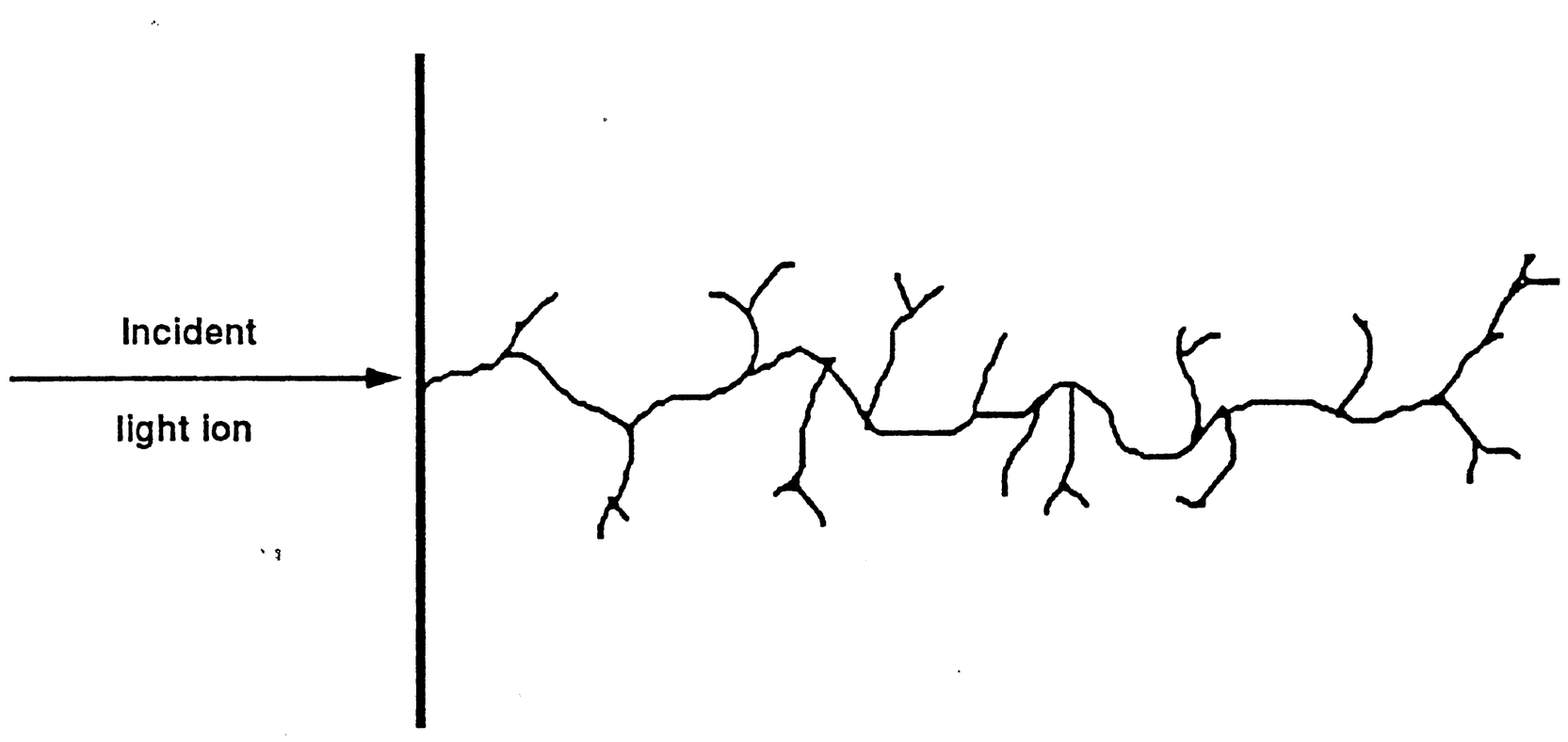


Figure 12. Branching Dislocation from Light Ion Implantation[26]

A light ion transfers a small amount of energy during each target

encounter and is deflected through a large scattering angle. Those target atoms which are displaced generally do not have enough energy to create more displacements by themselves. Figure 12 depicts the damage of a light incident ion in the form of what is known as a branching dislocation track and creates disorders called point defects. Much of the energy that the light ion transmits to the lattice is through the electronic stopping processes. Thus there is little damage to the crystal, with a comparatively large range (energy and mass dependent) and the damage becomes spread out.

It is clear that the introduction of impurities by ion implantion brings a considerable amount of disorder to the silicon. However, a technique was devised which not only corrects most of the damage, but can allow the ions to become electrically active in substitutional sites throughout the substrate lattice. This process, known as annealing, is a temperature/time treatment step commonly practiced after implantation. Much information[27,28] has been compiled in order to determine both the minimum temperature and the time required to heal as much of the crystal as possible with minimal impurity diffusion (temperature activated) in order to preserve the original implanted profile.

Temperature and time parameters are dependent upon the dosage, the character of the ion species, and in the case of microelectronics, device performance capabilities. Most anneal cycles last between 15 - 30 minutes and can have a temperature range from 400° C (metallized devices) to 1200° C (bare silicon). This procedure is usually performed in an inert gas (H_2, N_2) to limit more reactions from occuring when the substrate is heated. The details regarding the annealing of the F^- implanted MOS capacitors are described in the

experimental portion of this thesis (Chapter 3). This process removes the damage caused by the fluorine implant and can produce additional unique device characteristics.

2.3.3 Ion Implantation Systems

An ion implanter is a uniquely complex integrated circuit/semiconductor device processing tool containing many intricate subsystems which uses both machinery and electronics in its design. This versatile piece of equipment utilizes an ion source, an atomic mass accelerator, and the means by which the implanting beam can be purified and controlled. A schematic diagram of a commercial ion implanter system with its major components enumerated and labeled is given in Figure 13. A brief explanation and/or description for each of the essential parts accompanies the drawing below. Here are an ion implanter's main subsections:

1. A gaseous source feeds an appropriate impurity material (BF_3, AsH_3, or $SiCl_4$) to the ion source by way of controlled amounts (valving system).

2. A power supply of a high potential V energizes the ion source.

3. The ion source, utilizing its own power supply and pump, produces a plasma (containing a particular ionized species $^{+}As^{75}$, $^{+}B^{11}$, $^{-}F^{19}$) at relatively low pressures ($\simeq 10^{-3}$ torr) for reduced ion-gas scattering.

4. An analyzer magnet extracts ion species of interest by its mass and forms the ions into a beam as it passes through the resolving slits (aperture) en route to the acceleration table.

5. The acceleration tube which applies very high voltages to the ion beam,

further raising its energy level to the desired amount. Additional beam focusing is used before transport to the target.

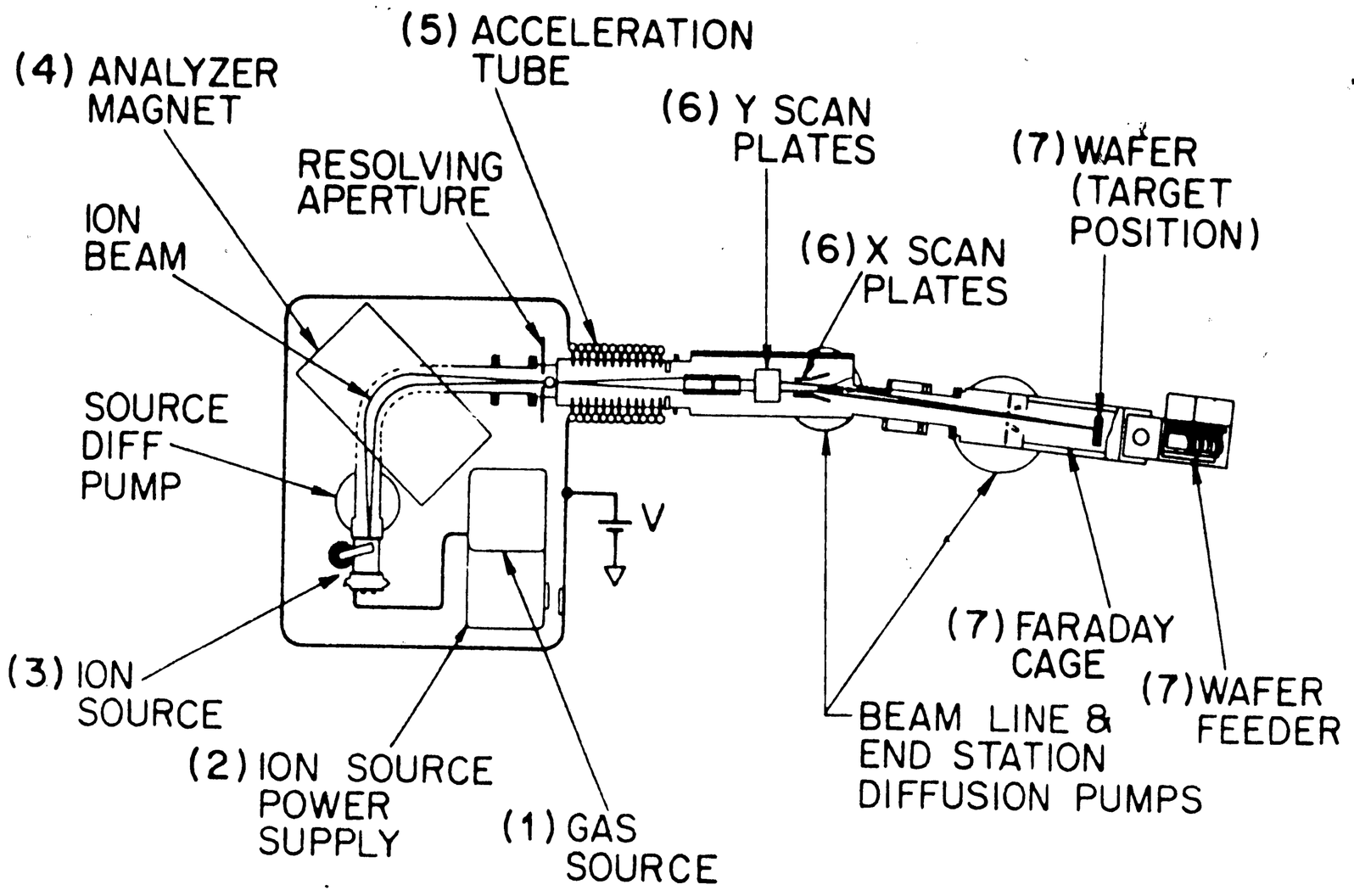


Figure 13. Commercial Ion Implanter System[29]

6. An electrical raster scan (sawtooth voltages applied to x and y deflection plates) provides ion beam uniformity throughout implantation. Two additional diffusion pumps (one beam line and one end station) produce a very high vacuum ($< 10^{-6}$ torr) in order to keep the beam free of residual gas atoms (neutrals).

7. A target chamber consisting of an area-defining aperture, Faraday cage and current integrator (for a direct measurement of the dosage), and wafer feeder mechanism. In general, a large negative bias is placed on the Faraday cage for

accurate dose calculation. Now that an overview of an ion implantation system in general has been presented, specifics regarding the Sherman Fairchild Laboratory's ion implanter used in this thesis work are now mentioned.

The Varian-Extrion 200-20A ion implanter is shown in block diagram form in Figure 14. The voltage range of this machine (extraction and accelerating) is from 25 keV to 200 keV allowing for a wide range of implantation energies. The 90° analyzing magnet is double-focused insuring high transmission of ion current coupled with high resolution of the desired ion species. The analyzer by design has a 1.5 inch gap between its magnets and its radius through the 90° turn is 9 inches which can minimize beam aberrations. Since mass analysis occurs prior to acceleration both the magnet current and the ion beam current remain constant while varying the beam energy over its entire range. The magnet operation is considered to be very stable, thus reducing drift and hysteresis effects during energy variation. The multi-section accelerator tube utilizes a resistor network for precision voltage gradient control in order to prevent high voltage arcing. Once accelerated, the beam is focused by an Einzel lens system and is then ready to be raster scanned for uniform implantation over the entire wafer. This explains, to some detail, the exact means by which an ion beam is made ready for implantation. As the ion beam reaches the wafer station, further system design allows for the removal of neutral particles, which can form during beam acceleration and cause excessive wafer heating. Thus the beam is deflected by 7° from the main beam line axis. The residual neutral beam, unaffected by the electrostatic deflection field, remains on its original path and is trapped on the electron suppressor, located behind the final defining aperture for the impinging

ion beam.

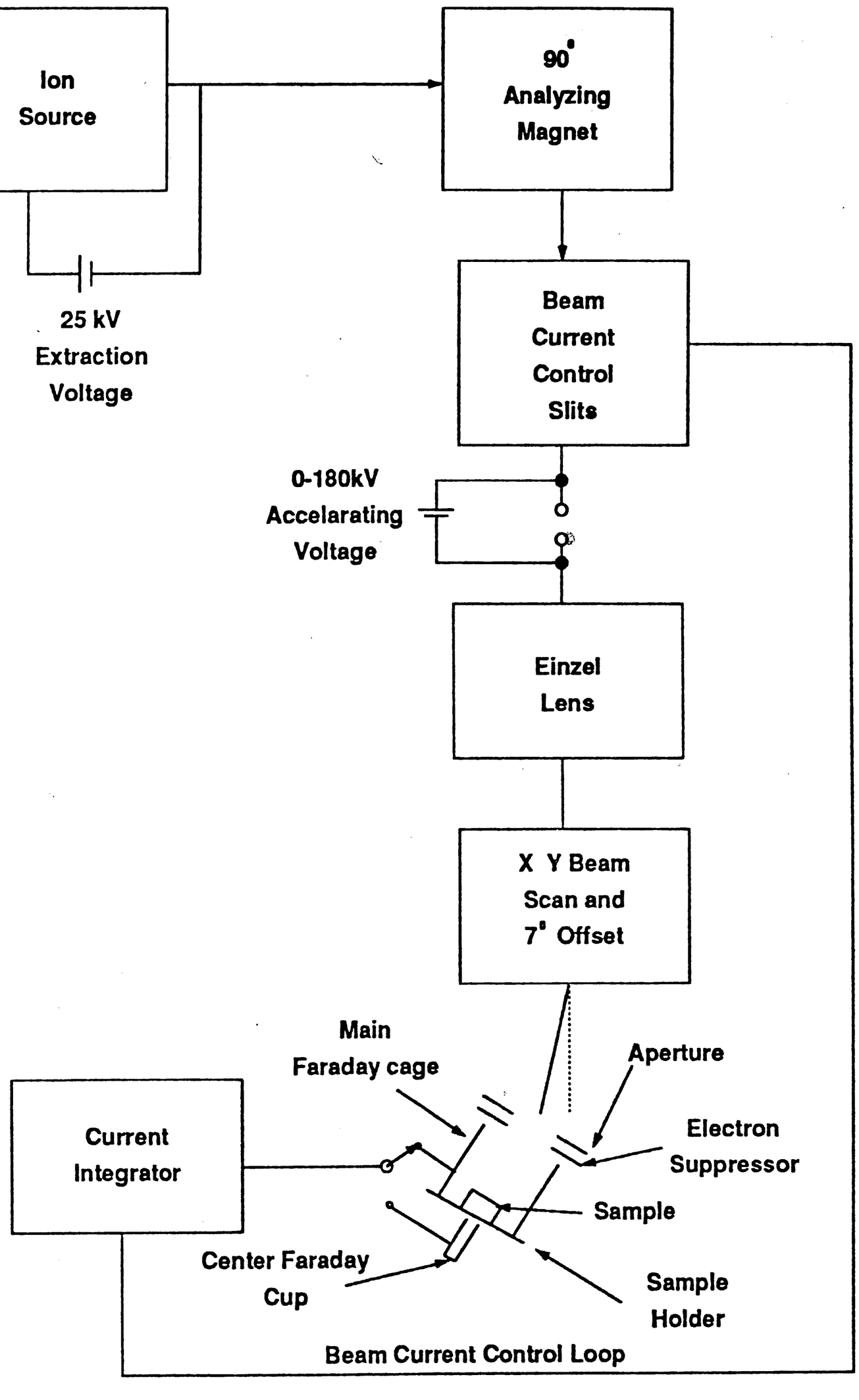


Figure 14. Block Diagram of a Varian-Extrion 200-20A Ion Implanter

It should be noted that the target wafer is rotated by 7° off the final beam

direction to minimize channeling effects. In addition, the current integrator unit measures the uniformity of dosage implanted and is connected to the beam current control slits by way of a feedback loop. If there are variations in the beam current as indicated by the current integrator, the beam current control slits will be adjusted to provide a constant beam current reflective of a uniform dosage. It should be clear that this system is very self-contained and, once prepared for implantation of a chosen ion impurity, could operate as an automated process.

All in all, the ion implanter is quite an intricate and delicate piece of equipment to maintain and operate. However, its ability to selectively control the amount of injected impurity into the target wafer proves without a doubt how unique and vital this system is to semiconductor research and development.

2.4 Fluorine

This section is strictly dedicated to the basic understanding of fluorine and how it became an interesting topic for study in MOS electronics research. The fundamental properties of fluorine in both its elemental and ionic states is discussed for background. The results of two papers from the 1970's are presented indicating that fluorine could have a pronounced effect within the Si/SiO_2 structure. Primary fluorine-implantation studies reveal its unique behavior in silicon and its effect on the oxide growth rate. Finally, the electrical character of implanted fluorine in MOS capacitors is discussed for the purpose of experimental guidelines and as an indication of the possible effects to be observed in the results of this thesis.

2.4.1 Elemental and Ionic Fluorine

As previously stated in Chapter 1, fluorine is a member of the Group VIIA elements, better known as halogens. It is classified as a nonmetal and has been considered as somewhat of an exception when compared to the other halogens. Fluorine possesses low values of electron affinity and bond energy associated with the diatomic molecule F_2. Its 2p orbitals are very small in size ($r_F = 0.64$ Å) resulting in large electron repulsions. Therefore, the existence of a weak bond within the F_2 structure is evident. The reference[30] to fluorine and its halogen counterparts provides a more detailed description with regard to both its elemental and ionic properties.

Because of its high reactivity, fluorine is not found as a free element in nature. It more readily exists as a halide ion (F^-), or commonly called an anion, due to its negatively charge state. Possessing a high electronegativity value (4.0), fluorine is very willing to form ionic bonds with metals and polar covalent bonds with semimetals (B, Si). The electrochemical nature and the bonding versatility of F^- ions between both metals and semimetals is discussed thoroughly in the next section pertaining to an experiment dealing with fluorine contamination of the Si/SiO_2 structure.

2.4.2 Early Fluorine Experiments

As mentioned in Chapter 1, experimentalists stumbled onto the use of fluorine in silicon and silicon-based structures when they wondered if fluorine was contaminating their samples during processing. Fluorine-based compounds such as HF and KF could very well dissociate leaving traces of fluorine on the surface

of the Si-substrate. If a significant amount is left behind, it could result in a pronounced effect on the oxidation growth rate, the character of the Si/SiO_2 interface, and possibly the quality of the produced devices.

This notion was considered by Croset and Dieumegard[7] who considered intentional fluorine contaminated of organic baths during anodic oxidation. The incorporated fluorine, introduced into the bath in a salt form (KF), was shown to have a square root dependence on oxide thickness and was found to be existing at both the Si/SiO_2 interface and within the oxide structure. This was explained by the relatively high chemical affinity F^- ions have for silicon and silicon-oxygen structures.

The electrical measurements, gathered from annealed MOS structure C-V testing, revealed a consistent interface charge density of $10^{11}/cm^2$. It was proposed that since this value was much lower than the surface concentration of the fluorine atoms at the interface ($10^{15} F^-$ atoms/cm^2), the fluorine was somehow linking itself to the Si atoms. Finally, a hysteresis in the C-V curves confirmed the existence of a disturbed interface whose compostion and structure differed from that in the bulk oxide.

About one year later, Williams and Woods[8] suggested the existence of mobile fluorine ions in SiO_2 as a way to trap and neutralize mobile positive ions such as Na^+ or Li^+ and thus provide stability to MOS devices. Their assumptions were based on the fact that ions of radii less than 1.69 Å (the Pauling radius of Cs^+, which was found not to be mobile in silicon) should be mobile. Since 1.36 Å is the radius of an F^- ion, an experiment was conducted to inject ionized fluorine into the oxide layer by negative corona discharge of the

fluoride salt coated surface. MOS capacitors were fabricated and subsequent C-V measurements were made.

The results show that with negative corona charging and air annealing a significant shift in the C-V curve to the right occurs which is characteristic of the presence of negative charge, most notably the fluorine anions. Furthermore, upon application of a bias-temperature stress (BTS) test (to be explicitly defined in Chapter 3) only one of the seven fluorine-treated MOS capacitors tested possessed a flat-band voltage due to positive charge. Although the flat-band voltage shift in the fluorinated samples was not as large as the shifts due to Na^+ contamination (untreated samples), they further concluded that around 1 X 10^{12} mobile Na^+ atoms/cm^2 were successfully neutralized by the F^- ions on a one positive charge to a one negative charge basis. On this premise, and with the expanding technology of semiconductor research throughout the remainder of the 1970's into the 1980's fluorine related experiments based on silicon would continue to provide unique information about this halide.

2.4.3 Fluorine Implantation Studies

With the advent of ion implantation systems as a means of introducing impurities into wafer substrates, F^- implantation was soon attempted. At first, as a means to dope silicon p-type, the ion species of BF_2^+ was implanted which then would dissociate into its component elements and with an anneal step, boron would become electrically active and thus dope the semiconductor. Questions concerning the activity of the fluorine molecule and its potential effects sparked an experiment concerning the migration and electrical character of fluorine after

implantation.

Tsai, et al.[5,6,31], after implanting with BF_2^+ into silicon and performing subsequent annealing treatments at various temperatures, began to take note of some of fluorine's unique properties. They found that fluorine migrates anomalously during annealing and produced a double peak distribution (one in the amorphous layer and one in the silicon layer), after the temperature was raised above 500° C. By the time the annealing was complete (1100° C) most of the fluorine had outdiffused and the peaks diminished. Their reasons for anomalous fluorine migration are associated with the apparent sweeping out of fluorine during recrystalization and its impurity-gettering effects. The results actually showed that the depth at which boron stopped being electrically active is at the exact point where the fluorine gettered peak exists. Thus fluorine can be used to decorate damaged regions in silicon.

By the 1980's, fluorine implantation became widely used in experimental semiconductor research and development. In particular with regard to oxidation growth and interfacial conditions in silicon and silicon dioxide. As Croset and Dieumegard found out almost a decade ago, fluorine seemed to aid the oxidation process as well as have a surface concentration present at the Si/SiO_2 interface. Similar interface conclusions were drawn by Williams and Woods.

Fluorine ions have been implanted into silica structures and oxides have been grown on top of the amorphous fluorinated layer. The fluorine seems to reduce a majority of the oxidation-induced atacking faults (OISF), a defect related to the oxide process resulting in nonuniform in SiO_2 layers. This was the work of both Isomae, et al.[9] and Van Hasselt, et al. [2] who also claimed the important

role fluorine plays at the Si/SiO_2. Kuper, et al.[11] studied the kinetics of dry oxidation of silicon after fluorine implantation. Their study proposed an enhanced Deal and Grove model to include the effects of fluorine implantation. They seemed to believe that the action of the F^- ions at the interface to alter the reaction rate constant and possibly form a silicon-fluoride complex. This type of evidence would suggest the study of fluorine implantation on a device level.

2.4.4 Fluorine Implantation in MOS Capacitors

As stated in the earlier portions of this manuscript, an MOS capacitor acts as a fundamental test structure for uncovering many of the electronic, interfacial, and material properties of silicon-based devices. It therefore seems obvious to study the effects of implanted fluorine in MOS capacitors since its structural changes can provide much information about fluorine behavior in semiconductor devices. This specific topic of research has been looked at by different groups in various ways and their experiments and results are presented here for the reader's information and as a guideline for this thesis.

Halogen implantation (Cl^- , F^-) into silicon for MOS capacitor testing was attempted by Greeuw and Verwey[1] in 1982. Their dosages were quite high (10^{14} and $10^{15}/cm^2$ of halide ions) in order to study the doping profile changes toward the Si-surface as the devices were tested. Specifically the C-V measurements with fluorine showed a decrease in the accumulation capacitance and noticeable changes in the shape (stretch-out effects) of the C-V curves. They did find a change in the average doping level ($\bar{N}_D$) whose origin was explained to be caused by a complex consisting of a halogen atom and an implantation induced

defect. The enhancement of the oxidation rate in silicon was also noted.

Others such as Wright, et al.[4] considered the effect of F^- implants on gate dielectric properties by implantation through the entire device (polysilicon/SiO_2/silicon). Their C-V studies found low levels of N_{it} and N_f approximately equal to 2 X $10^{10}/cm^2$ across all the samples which contained fluorine and higher implant doses ($10^{15}/cm^2$ of F^- ions) showed large flat-band shifts explained as a result of implantation damage. Still others like Zaima, et al.[5] explored the electrical characteristics of F^- implantation in MOS devices and proposed that a generation of deep acceptor levels due to the presence of fluorine. Device testing proved that a strong suppression of the device leakage was a diect result of fluorine implantation and did not degrade the MOS device characteristics.

By and large, fluorine implantation has and is producing a predominant effect on the world of semiconductor research and technology. Its unique elemental and ionic characteristics play a role in device modeling and theory of ion implanted MOS structures. The properties of fluorine in silicon are not completely understood, thus active experimentation in this particular area provided a challenging thesis problem.

Chapter 3
Experiment

This chapter is expressly concerned with the thesis experiment as a whole. A complete experimental overview is presented which includes both the purpose and goals associated with this problem. A detailed description of the wafer cleaning, processing and device fabrication is listed for the reader's knowledge. Two subsequent post-processing methods are applied to the implanted silicon structures in order to enhance characteristics. All of the various capacitance-voltage testing techniques used are briefly defined and explained with regards to what information may be obtained by their usage.

3.1 Experimental Overview

As stated in Section 1.4 of Chapter 1, this thesis project is designed to provide information by way of C-V device testing concerning fluorine implanted into an MOS capacitor. It had already been mentioned how current and important the topic of fluorine is in the realm of comtemporary semiconductor research. There is much to be learned about fluorine's behavior in silicon-based structures, and fluorine effects in silicon are of interest here at the Sherman Fairchild Laboratory. However, previous experiments have been concerned with the diffusion of fluorine and because ion implantation is a unique process in itself, it is a reasonable progression to attempt a fluorine ion implantation device study.

The specifics regarding the experimental design revolve around a few principles concerning ion implantation through an oxide and MOS capacitor theory. The use of oxides in implantation is a way to provide protection to the bare silicon surface during the process. Any region of the oxide affected by the implantation will develop charge states which would most likely change the material's electrical characteristics. At this point, MOS theory can be applied to explain the deviations from the ideal capacitor's response and provide insight into the effect the implanted species has on the metal-oxide-semiconductor system.

Furthermore, if the oxide thickness is relatively small, then it is very likely to have a low energy implanted impurity profile partially residing inside the silicon substrate and the remainder of it is in the silicon oxide film. This raises the question of placing a controlled amount of ion species at the Si/SiO_2 interface resulting in the formation of a sheet charge at the borderline of these two materials. Once again, a unique result produced by ion implantation is of interest to MOS device theory since interface charge density (Q_{it}, Q_f) will have a pronounced effect on a capacitor's electrical performance, comparable to a threshold implant widely used in MOS channel devices. It was on this premise that the thesis experiment was designed.

To begin with, Si-wafers are cleaned and prepared for dry O_2 oxidation and three relatively thin oxide thicknesses were chosen to be studied (600 Å, 800 Å; 1000 Å). After growing the oxides, the exact thickness of each wafer is determined by ellipsometry and an overall average oxide thickness is determined statistically. By knowing with some degree of accuracy the SiO_2 film thickness, the Projected Range Statistics tables by Gibbons, Johnson, and Mylroi[32], which

contain energy/range relationships for fluorine implanted in both silicon and silicon dioxide are employed. Using this and an iterative routine, an implantation energy to be used determined by using the average oxide film thickness as a guideline for placing the peak of the implanted fluorine profile at the Si/SiO_2 interface. This would hopefully guarantee a maximum amount of sheet interface charge and impose the greatest amount of change in the device's performance capabilities.

The F-ion implantation process itself could now be carried out at the estimated energies corresponding to the specific oxide thickness. Metallization of the circular gate using a shadow mask and the substrate contact by aluminum evaporation is carried out to complete the device as a test structure. The C-V measurements are made and as a means of comparison of the implanted set of MOS capacitors is compared to clearly note the effects due to fluorine implantation. The specifics of the entire experiment are now briefly presented in a step-by-step manner.

3.2 Sample Preparation and Device Fabrication

The step-by-step process of fabricating the MOS capcitors used in this thesis are explained with some detail. These are four phases involved in making the fluorine implanted MOS capacitors. They are wafer cleaning for oxidation, oxidation of the wafers, F-implantation, and metallization. All processes are the standard practices of the Sherman Fairchild Laboratory.

3.2.1 Wafer Cleaning Techniques

Beginning with wafers of low sensitivity, ρ = 6 - 7 Ω-cm (n substrate $\simeq$ 2 x 10^{15} atms/cm^3), with p-type substrates (B doped), and oriented in the <100> plane, the following cleaning procedure is adopted for funace oxidation:

1. 4 : 1

$H_2SO_4 : H_2O_2$

Immerse the wafers in this solution for 5-7 minutes at room temperature. Thoroughly rinse for 5 minutes with deionized (DI) water.

2. 50 : 1

DI-H_2O : HF

Immerse the wafers in this solution for 5-10 minutes at room temperature. Thoroughly rinse with DI water and check for a hydrophobic condition on the surface of the wafer.

3. 5 : 1 : 1

DI-H_2O : NH_4OH : H_2O_2

Place the wafers in solution on a hot plate and allow them to boil for 10-15 minutes. Allow wafers to cool on hot plate for another 5 minutes. Rinse the wafers thoroughly in DI water.

4. 5 : 1 : 1

DI-H_2O : HCl : H_2O_2

Place the wafers in solution on a hot plate and allow them to boil for 10-15 minutes. Allow wafers to cool on the hot plate for another 5 minutes. Rinse the

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4. 5 : 1 : 1

DI-H_2O : HCl : H_2O_2

Place the wafers in solution on a hot plate and allow them to boil for 10-15 minutes. Allow wafers to cool on the hot plate for another 5 minutes. Rinse the

wafers thoroughly in DI water. Once the wafers have been cleaned they are dried completely with compressed N_2 gas.

3.2.2 Oxidation Schedule

The wafers are then placed into grooves on a wafer boat and inserted into a Minibrute furnace for dry O_2 oxidation. The double-walled quartz furnace had a flat zone temperature of $T_{flat\ zone} = 1000^{\circ}$ C and three separate runs were performed to achieve three different oxide thicknesses. Table 1 summarizes the oxidation schedule and also lists the actual average mean values (statistically known as the "best" values) and the average standard deviation from the ellipsometer data. Their differences are tolerable and the oxidation process itself will be addressed again in the next chapter.

Table 1

Oxidation Step Results

Ideal Oxide Thickness (Å)	Average Mean Value $x_{"best"}$ (Å)	Average Standard Deviation σ (Å)	Oxidation Process Time t (min.)
600	593	± 22.6	70
800	755	± 30.6	100
1000	898	± 32.6	120

It should be noted that surface films were present on all wafers after cleaning and that high purity nitrogen (N_2) was pumped through the system as the wafers were loaded and unloaded from the furnace tube to deter any further oxidation after the wafer boat left the flat zone.

3.2.3 Implantation Preparation and Operation

As stated in section 3.1, once the average oxide thickness is known, energy/range statistics tables[32] can be employed to find the proper energy setting for the ion implanter. The results of the iterative process using the "best" values of each oxide thickness enable the energy, range and straggle estimations for fluorine implanted in silicon dioxide and is shown in Table 2. This method as explained is an attempt to place the F^- ions peak concentration at the Si/SiO_2 interface.

Table 2

Implantation Statistics

Estimated Implant Energy E (K eV)	Average Mean Value x " best " (Å)	Projected Range R_p (Å)	Projected Staggle ΔR_p (Å)	Transverse Straggle $\Delta R\perp$ (Å)
36	593	599	230	293
45	755	759	277	358
52.5	898	894	313	410

With the energy settings determined, the next task is to determine a source gas which, when analyzed, reveals a distinct $^{-}F^{19}$ peak. SiF_4 is chosen as the source gas and Figure 15 is the actual gas spectrum of the source which plots arbitrary analyzer magnet settings against the ionized element masses. All ionized masses are determined though a simple ratio of masses (M) to arbitrary magnetic settings (B)

$$\left(\frac{M}{m}\right)^{1/2} = K B \qquad (2-33)$$

where m is a number indicating the ionized charge state (for example, a singly ionized state would have m = 1), and K is a proportionality constant. All masses are essentially determined by first finding K for a given inert gas (Ar) which is mixed in with the source gas and is the predominant peak in the spectrum. For this SiF_4 gas source K = 0.016 and a magnetic setting of B = 271 produced a mass M = 19 corresponding to ionized fluorine. This peak is noted in the figure.

The implanter is now readied for the ion implantation process. A high dosage is chosen ($\phi = 3 \times 10^{14}$ F^- ions/ cm^2), to provide a distinguishable effect of fluorine in the MOS capacitors. As a note, for the implantation runs the beam current remained relatively constant at $I_{\text{beam line}} \simeq 0.5\ \mu A$ and yielded an average process time (dosage and current dependent) of $t_{\text{process}} \simeq 118$ min./ run.

9/28/87
SOURCE: $S_i F_4$
EXTRACT. V: 25 KeV
OPEN
PRESSURE: 1×10^{-6} Torr

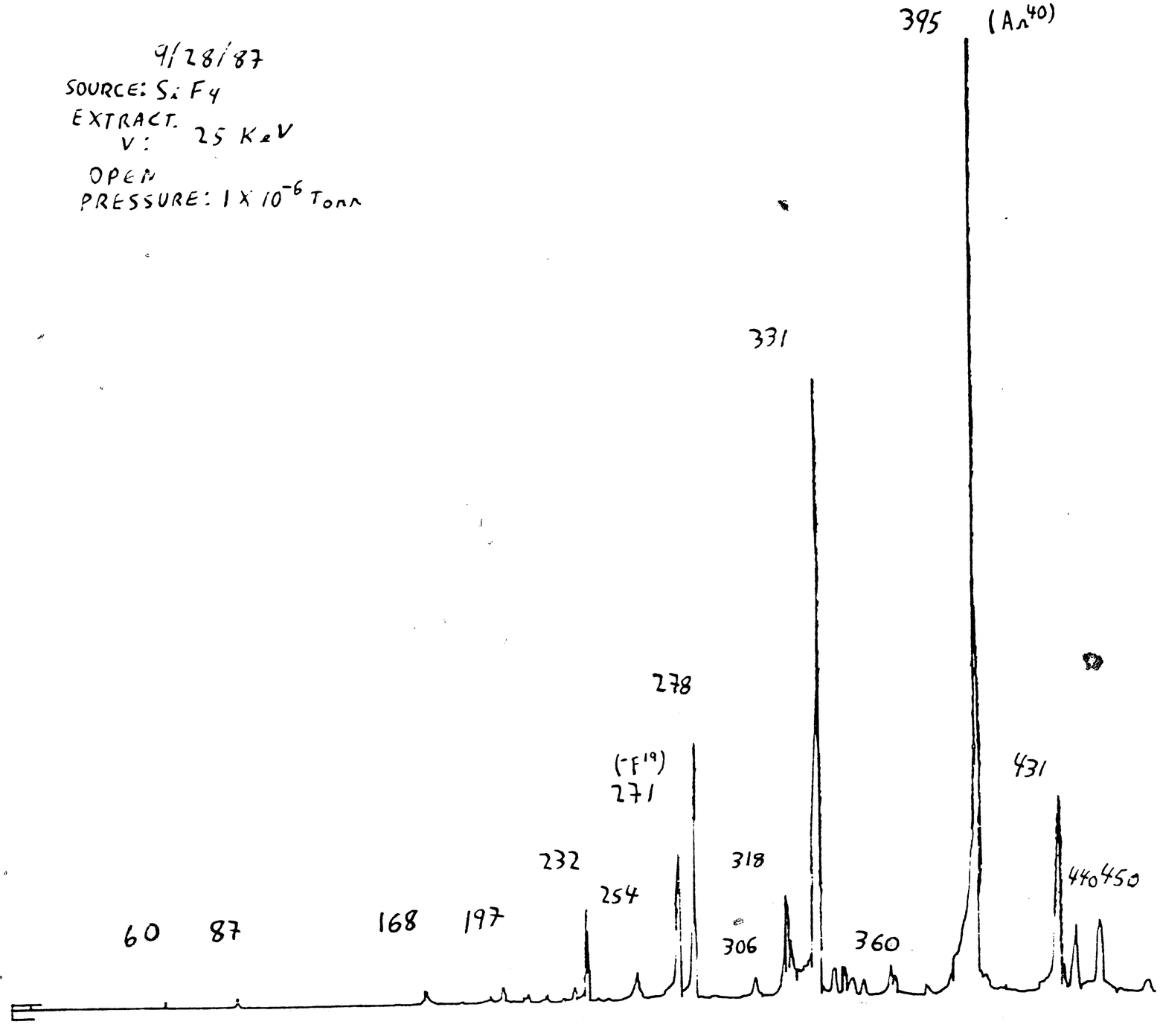

Figure 15. SiF_4 Gas Source Spectra

3.2.4 Gate and Substrate Metallization

In order to complete the MOS capacitor as a device, a metallization step must be performed on the front and backside of the wafers producing the MOS structure. This process is carried out with a vacuum bell jar evaporator which heats a tungsten filament and deposits vaporized aluminum onto the wafer surfaces. In order to form the circular gates on top of the oxide layer a metal contact mask is laid over the wafer prior to evaporation. The substrate side then has its oxide stripped off with a 10% HF solution which is confirmed when the surface of the substrate is hydrophobic. The wafer is blown dry with compressed N_2 and the substrate contact evaporation can occur.

There is one precaution which must be taken to ensure minimal Na^+ contamination during metallization. That is to clean the aluminum strips to be used evaporation along with their teflon handling tweezers as follows:

1. 5 : 1 : 1

$$DI\text{-}H_2O : H_2O_2 : NH_4OH$$

Allow this solution to boil for 5-10 minutes and thoroughly rinse in DI water.

2. 100 : 1

$$DI\text{-}H_2O : HCl$$

Heat this solution for 30 minutes, thoroughly rinse in DI water and blow dry all the pieces with compressed N_2. In addition, the contact mask is organically cleaned by boiling it in methylene chloride and by drying it with acetone and compressed N_2. Some of the effects of the metallization process are discussed with the results in Chapter 4.

3.3 Subsequent Testing and Experimentation

This section briefly describes two techniques applied- one after implantaiton and two after metallization as a means to procure more experimental information about the nature of fluorine in the Si/SiO_2 structure. Secondary Ion Mass Spectroscopy (SIMS), a way of determining the profile of the implanted species, is performed on the samples after F^- implantation. A postmetal furnace anneal is carried out on the completed devices in an attempt to reduce the implantation damage and possibly change the electrical character of the devices from the as-implanted MOS capacitors.

3.3.1 SIMS Analysis

Secondary Ion Mass Spectroscopy or SIMS[33], uses an energetic beam of focused ions directed towards a sample and impinges the surface. The momentum transferred from the incoming ions (primary beam) to the sample surface sputters off surface species (atoms and molecules) some of which possess positive or negative charges. These charged species are termed as secondary ions and are collected as they sputter off in a double focusing mass spectrometer for analyzation are measured on the basis of intensity versus depth. By applying SIMS to the samples in this thesis, the result is an implanted depth profile of the F^- ions.

For such an analysis to occur, implanted and unimplanted sample portions with an approximate surface area of 1 cm^2, are sent to Bell Labs of Allentown, Pennsylvania for SIMS testing. All of the profile data is collected from a Camera IMS-3F with an O_2+ primary beam and checked against a library F^- calibration

implant for quantitaion in Si. These compiled results are compared with computer profiles and are presented in the next chapter.

3.3.2 Furnace Annealing

As stated in the theory and background section of the previous chapter, annealing is the procedure by which implantation damage is removed and the electrical activation of implanted species onto substitutional sites takes place. Since the annealing step occurs after metallization, some considerations are addressed concerning the annealing procedure to be used. It is clear that the temperature of the furnace should be on the low end of the scale, in the range of 400-500° C which implies that very little recrystallization will occur and only a small fraction of the implanted species (20 - 30%) will become activated. At this low temperature, the risk of any aluminum-silicon complex froming is nearly nil, as well as diffusion effects in Si, thus preserving the as-implanted profile. The other concern stems from the furnace operating temperature and the risk of additional oxide growth and outside device contamination. Therefore a neutral ambient gas is flowed over the MOS capacitors during the annealing step minimizing the possibility of these problems arising.

For the postmetal anneal experiment, a furnace temperature of T = 400° C is chosen and an anneal time of 30 minutes. High purity nitrogen (N_2) is passed over the devices at a regulated rate of 1.5 liters per minute. This will provide some additional data and gives a third class of devices to be used for testing (as-grown oxides, F^- implanted; F^- implanted and annealed).

3.4 Device Characterization

Once all of the processing of the devices is completed, electrical characterization studies of the MOS capacitors can now take place. Four classifications of capacitance versus voltage (C-V) testing techniques are applied on the three different device types for obtaining information and for comparative analysis. These testing techniques are:

1) general high frequency C-V

2) Quasi-Static C-V

3) bias temperature stressing (BTS) and

4) Terman's analysis

Each of the above is now briefly defined with respect to their particular results. This provides the reader with the necessary background needed to understand what information is to be obtained during the testing phase.

3.4.1 High Frequency C-V

High frequency capacitance-voltage (HFCV) is an electrical characterization of an MOS capacitor at an AC frequency of 1 MHz. The device's response primarily provides information concerning the experimental C-V curve's deviation from the ideal. As one might recall, Figure 8 in Chapter 2 showed how nonuniformities (various types of oxide and interface charges) within the metal SiO_2/Si structure resulted in serious distortions of an ideal C-V curve. The flat-band voltage shift from the ideal is a very useful measurable quantity as well as the overall shape of the experimental C-V curves when compared to an ideally generated one. In addition, the deliberate alteration of the substrate by ion

implantation can cause a change in the doping density of the silicon near the surface and will in turn affect the measurement of the depletion capacitance. The introduction of impurities into the depletion layer is noted on a C-V curve whose C_{dep} does not match the C_{dep} of an unimplanted sample. All of these will be discussed as the data is presented in the next chapter.

3.4.2 Quasi-Static C-V

The Quasi-Static[34] C-V technique allows for the measurement of the low frequency C-V curve. Essentially a time varying gate bias is applied across an MOS capacitor by a voltage-ramp generator, and the resulting displacement current flowing through the capacitor is measured with an electrometer. This current is directly proportional to the differential capacitance and can be related to the capacitance using the known ramp rate.

The low frequency C-V curve yields the true value of C_{ox}, which by comparison to the C_{ox} measured at high frequency, can be used to determine the series resistance which affects the HFCV curve. The resistance value can then be used to correct the high frequency oxide capacitance.

3.4.3 Bias Temperature Stressing

Bias temperature stress[35] or BTS, is a testing mode which can be defined literally by its title. An MOS capacitor is first biased with a voltage to create a positive electric field of about 1 MV/cm while the wafer is heated to 200°C. The wafer is allowed to cool to room temperature and a C-V measurement is made. This process is reflected again for the same temperature but this time a bias is

applied which results in an electric field of equal magnitude but opposite orientation (-1 MV/cm).

The result is a C-V plot containing three curves: one at room temperature, one at 200° C with a positive 8-field applied, and one at 200° C with a negatively applied 8-field. Of interest is the shift of the C-V curve after positive bias temperature stressing in comparison to the room temperature curve. The shift is mainly the result of mobile ionic charge (Q_m) as defined in section 2.2. If the curve shifts to the left, there is a presence of positive mobile ions (Na^+), if the curve shifts to the right then negative mobile ions (F^-) are present. Observation of the negative BTS should find a C-V curve which nearly overlaps the room temperature curve since the opposite 8-field application should return the MOS capacitor's electrical characteristics back to its original condition. If this is not the case, then something else in the MOS structure has affected the mobile ionic charge as it moves between the interface of the metal gate and the silicon dioxide interface under both bias and temperature stress. Some of these effects are noted with the experimental results in Chapter 4.

3.4.4 Terman's Analysis

The Terman[36] method of analysis is an application of high frequency C-V curves which are used to generate interface state density ($D_{it}(E)$) profiles. These profiles come about from distortive and stretchout effects in HFCV curves that deviate from the ideal. In essence, the Terman technique involves first the calculation of the ideal high frequency C-V curve as a function of the gate voltage ($C_{HF}(V_G)$), which is to be compared with an experimental $C_{HF}(V_G)$ curve. Due

to the relationship between V_G and the silicon bond bending Ψ_S, every experimentally measured $C_{HF}(V_G)$ data point can be correlated to the single ideal $C_{HF}(\Psi_S)$.

V_G and Ψ_S values are then paired and can produce a Ψ_S versus V_G curve containing all the information about interface trap level density for HFCV measurements. A $D_{it}(E)$ versus Ψ_S (the energy above the valence bond E_V) characteristic curve is very easily constructed by taking the derivative of Ψ_S with respect to V_G ($d\Psi_S(V_G)/ dV_G$). Since stretchout is a common occurence with ion implanted MOS capacitors, the $D_{it}(E)$ versus Ψ_S data curves will prove to be of some importance when analyzing the fluorine implanted devices to those which are not.

This concludes the chapter concerning the experimental methods used to learn more about the nature of implanted F^- ions in metal/SiO_2/Si devices. As the results are presented in the next chapter, one will see how each particular mode of C-V testing contributed some useful information concerning fluorine in MOS capacitors. This element will prove to become an interesting aspect of semiconductor research.

Chapter 4
Experimental Analysis and Results

In this chapter the experimental results are presented an analyzed to determine the effect of fluorine implantation on MOS capacitors. First a computer generated fluorine concentration profile (an ideal implant) is compared to the SIMS data for accuracy of the energy/range predictions. Second, the high frequency C-V's of the three types of MOS capacitors are compared to ideal HFCV's for flat-band voltage shift data and general high frequency characteristics.

Third, the Quasi-Static curves are used to determine the true oxide capacitance and to study the low frequency behavior. Fourth, extensive BTS measurements are shown for all the device cases in order to provide an indication about the mobile fluoride ion concentration in these MOS structures. Fifth, $D_{it}(E)$ profiles offer some unique information linked to the F^- implants as all the device types are presented for comparison purposes. Last, a brief experimental summary is given concluding that some visible effects of the fluorine have been detected.

4.1 SIMS Data/Computer Profile Simulation

As a means of comparing the actual implanted fluorine profile to an ideally generated one, a software program entitled, "PROFILE"[34], from the company Implant Sciences Corporation is used because of their extensive elemental library

and multilayer calculation capabilities. The fluorine implants described in subsection 3.3.3 are computer-simulated and should be considered as ideal profiles. For each case, the computer generated profile is presented first followed by its accompanying SIMS profiles for fluorine implants into 800 A of oxide.

In both cases, it is clear that the peak F^- concentration appears in the silicon below the Si/SiO_2 boundary. This provides a certain amount of consistency between the actual profiles and the computer generated profiles. One will note from the SIMS plots (Figures 17 and 19) that a discontinuity exists within the F^- concentration profiles which is a marker for the Si/SiO_2 interface. This is explained by the obvious change in materials and from the SIMS analysis report, which states that the secondary ion yield enhancement for F^- in SiO_2 compared to Si is about a factor of 2. This is not present in the computer generated profiles (Figures 16 and 18) since the software is not available to produce the fluorine concentrations data in silicon dioxide.

It should be noted that some consideration should be given to the energy/range calculations for placing the peak closer to the interface even though for the present estimations the projected straggle (ΔR_p) does allow the projected range (R_p) of the peak to sit very close to the Si/SiO_2 boundary. It would be better now that the software is available, to perform a series of F^- implantation simulations to optimize the implant energy for the given oxide thickness. This energy value can be used for the ion implanter when the experiment is repeated to place the fluorine ion peak at the Si/SiO_2 boundary.

As an aside, Figure 20 is the computer simulated F^- ion concentration profile for 1000 A of oxide. Unfortunately, the sample sent to Bell Labs for SIMS testing showed no trace of fluorine unlike the other two.

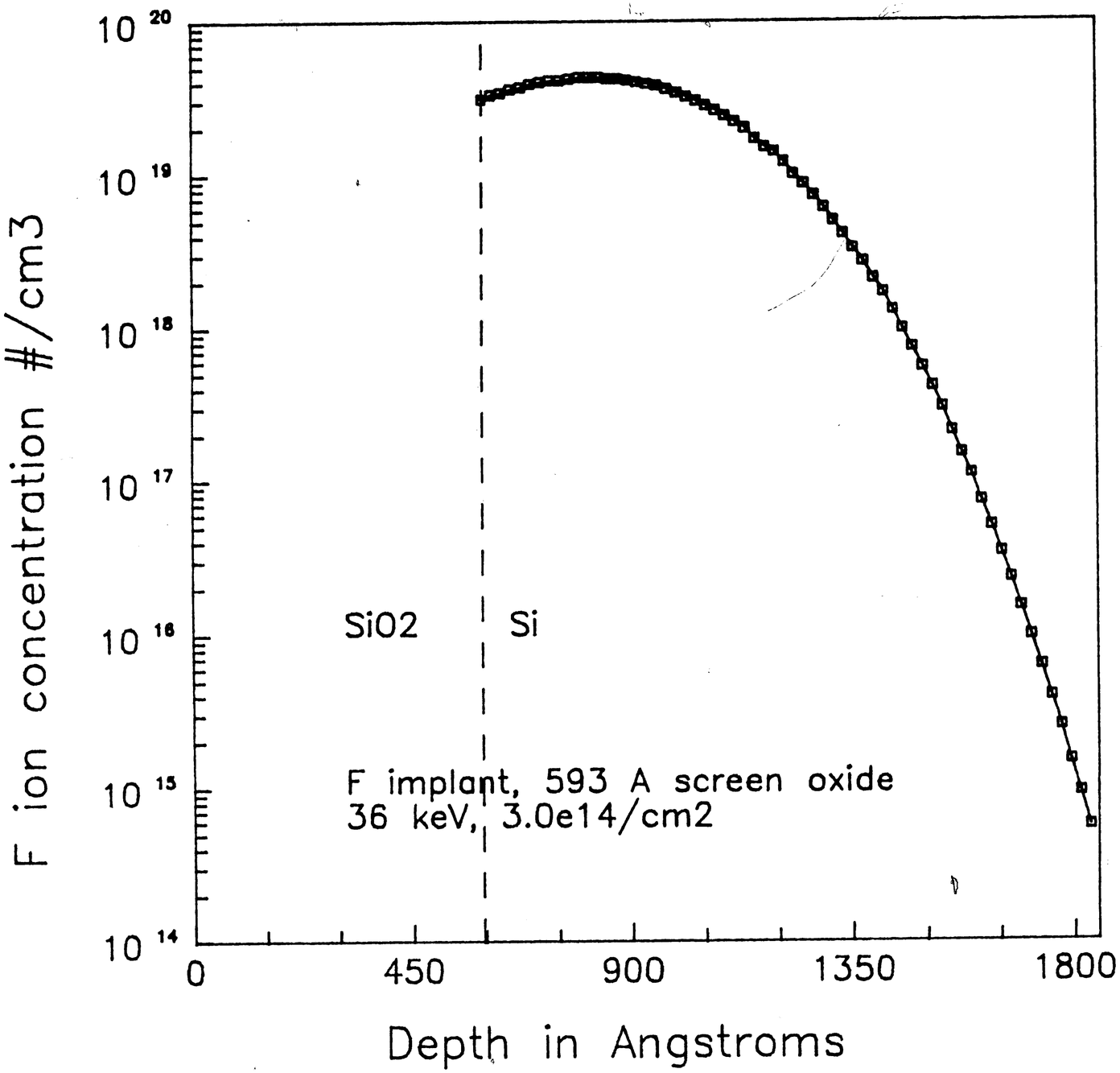

Figure 16. 600 A Computer Generated Fluorine Concentration Profile

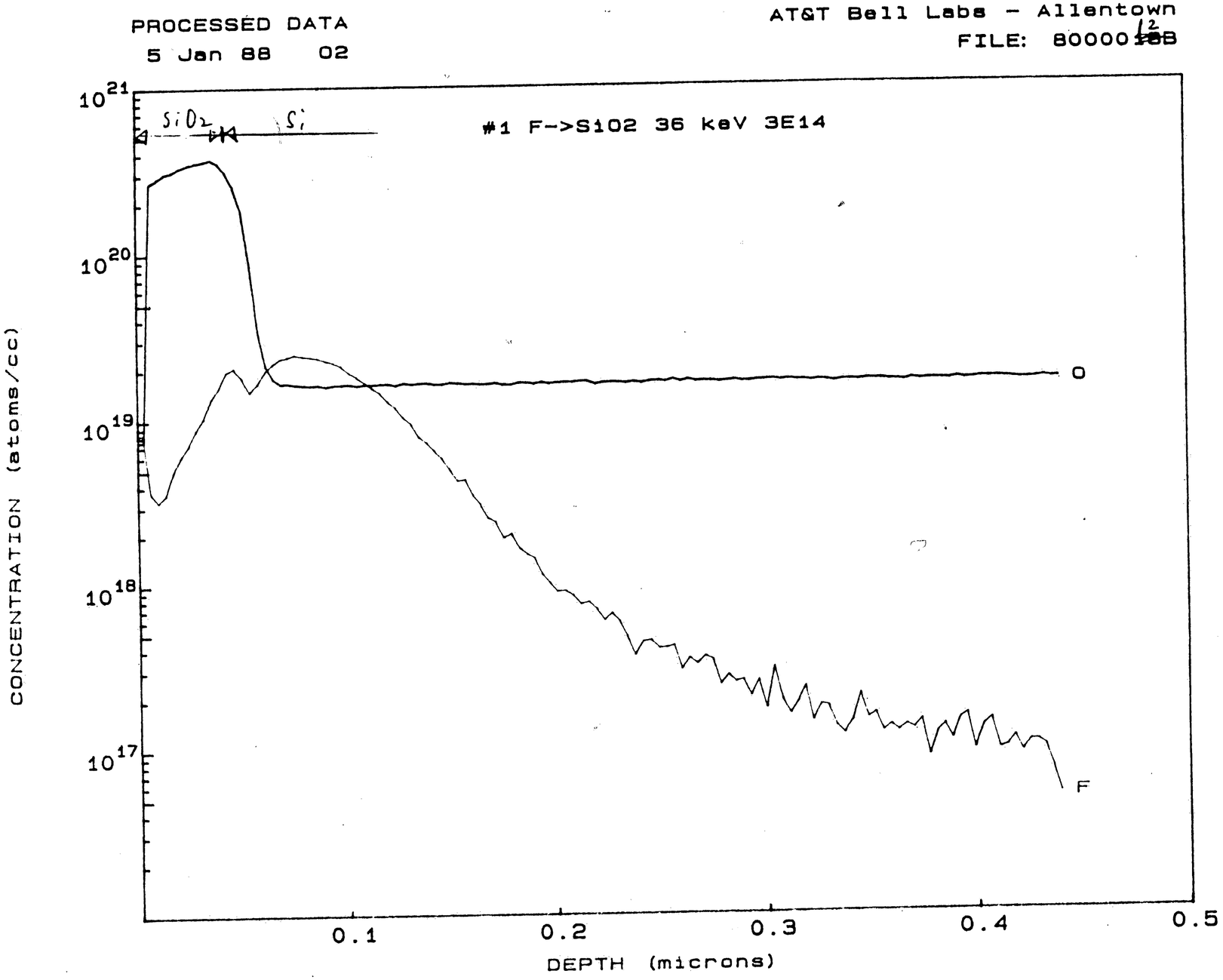

Figure 17. 600 A SIMS Fluorine Profile

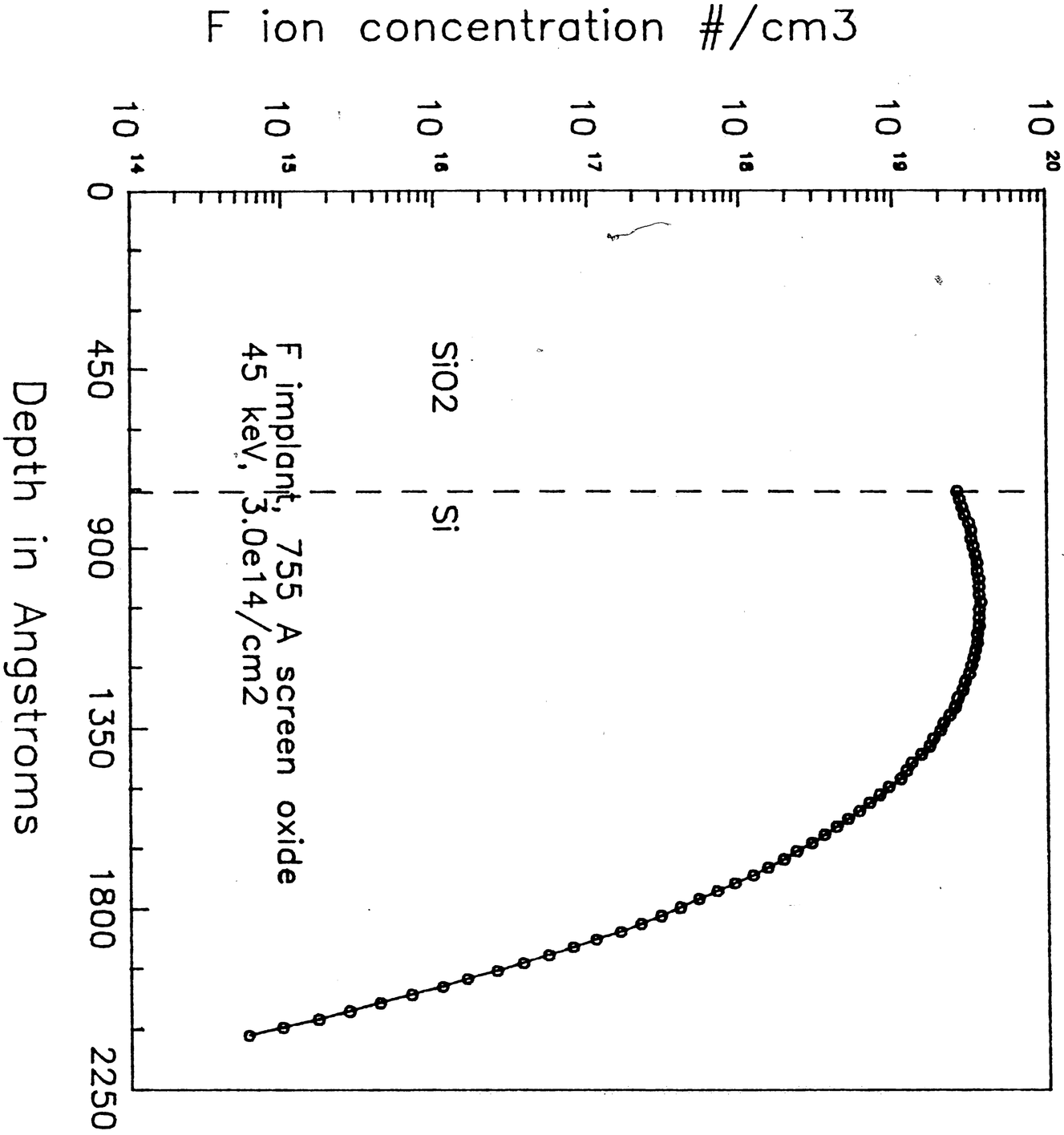

Figure 18. 800 A Computer Generated Fluorine Concentration Profile

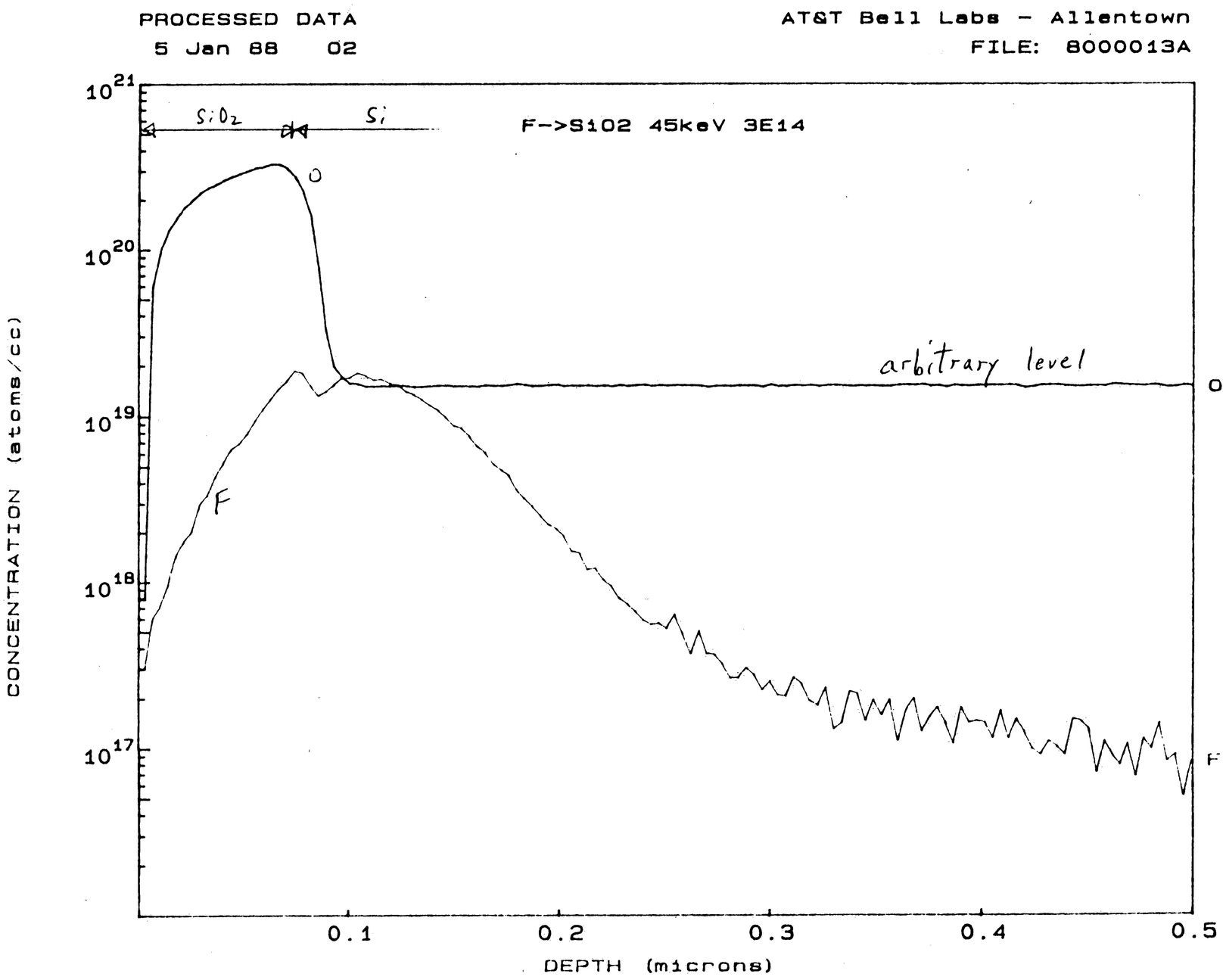

Figure 19. 800 A SIMS Fluorine Profile

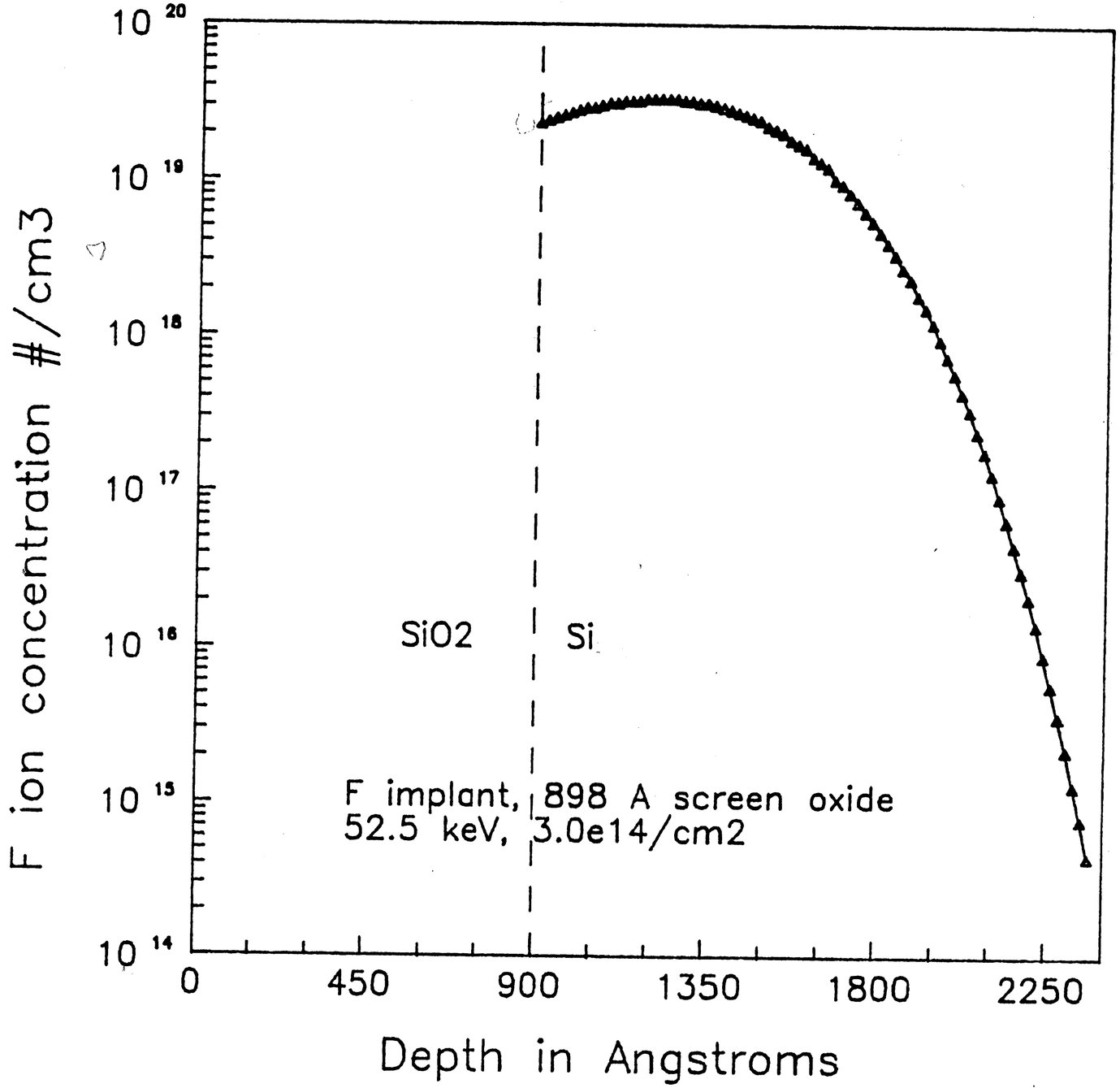

Figure 20. 1000 A Computer Generated Fluorine Concentration Profile

Although there is no direct way of comparing this generated plot with an actual one, one can see by observation that the result is the same, the fluorine peak lies within the silicon and optimization of the implant energy could enhance the experiment.

4.2 High Frequency Characterization

The as-grown oxide MOS capacitors for each thickness are first compared to their respective high frequency C-V curves and some comments regarding the control group are made. Then the HFCV's for the as-grown, as-implanted, and implanted and annealed samples are all plotted together according to oxide thickness, and general observations concerning changes in electrical characteristics are made. Tabulation of the flat-band voltage shifts and the total variation in trapped charge (ΔQ) for each case is presented for easy reference.

4.2.1 As-Grown Oxides To General Ideal Files

The initial observations of the as-grown oxide high frequency C-V curves plotted against the ideally generated HFCV curves (Figures 21, 22, and 23), suggest a strong deviation from the ideal. Visible stretchout is present in all these samples as well as a pronounced dip in the experimental C-V curve between the level of 0.5 and 0.6 of C/ C_{ox}. The dips are definite indicators of leaky oxides and at this point one could speculate upon whether it is the oxidation process or the substrate wafers themselves which have caused the nonuniformities present. Regardless of whatever defects are present, these curves are used as the standard curves for each oxide thickness and are now aligned on top of the as-implanted and implanted and annealed MOS capacitor samples.

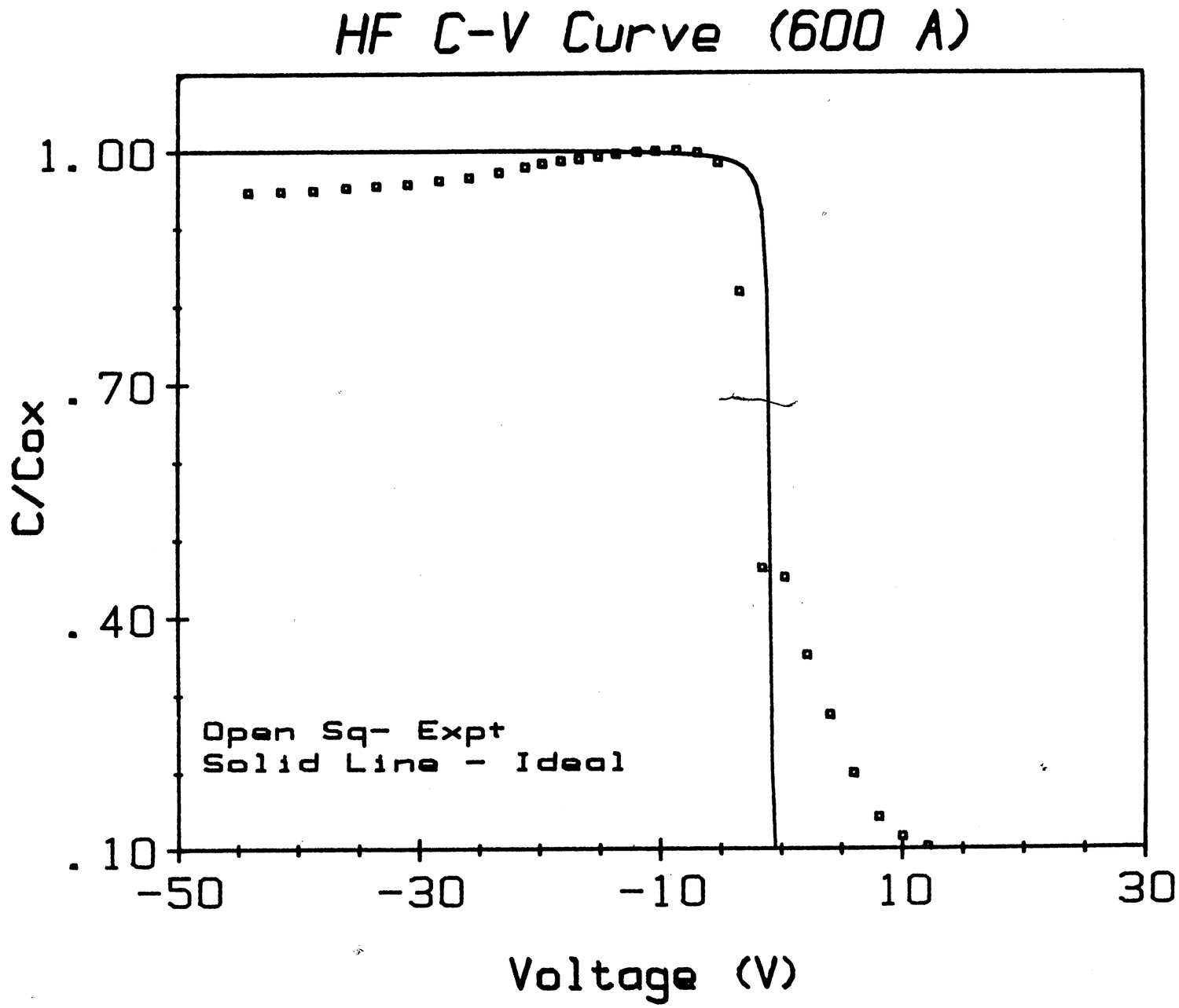

Figure 21. 600 A Experimental and Ideal High Frequency C-V Curves

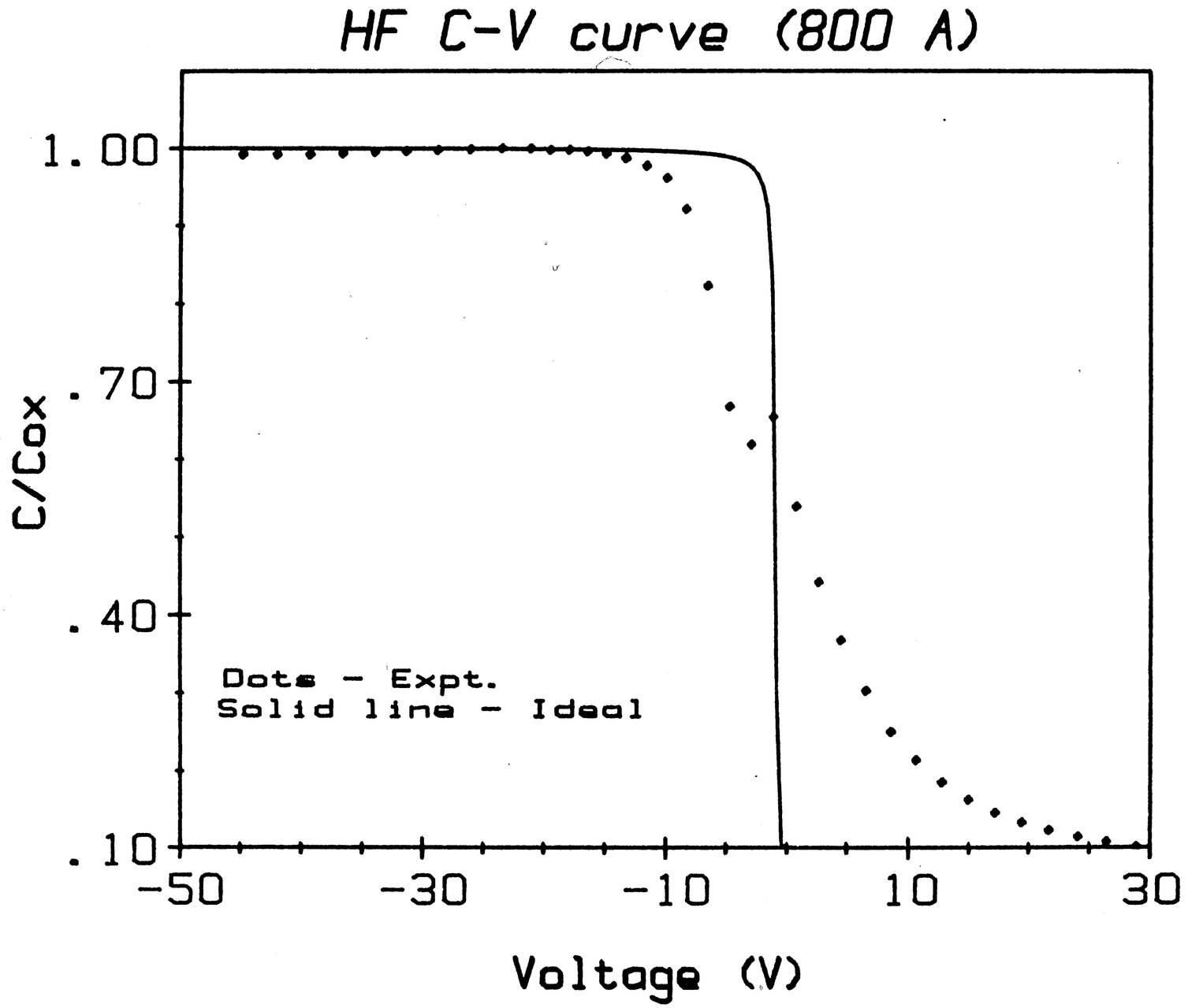

Figure 22. 800 A Experimental and Ideal High Frequency C-V Curves

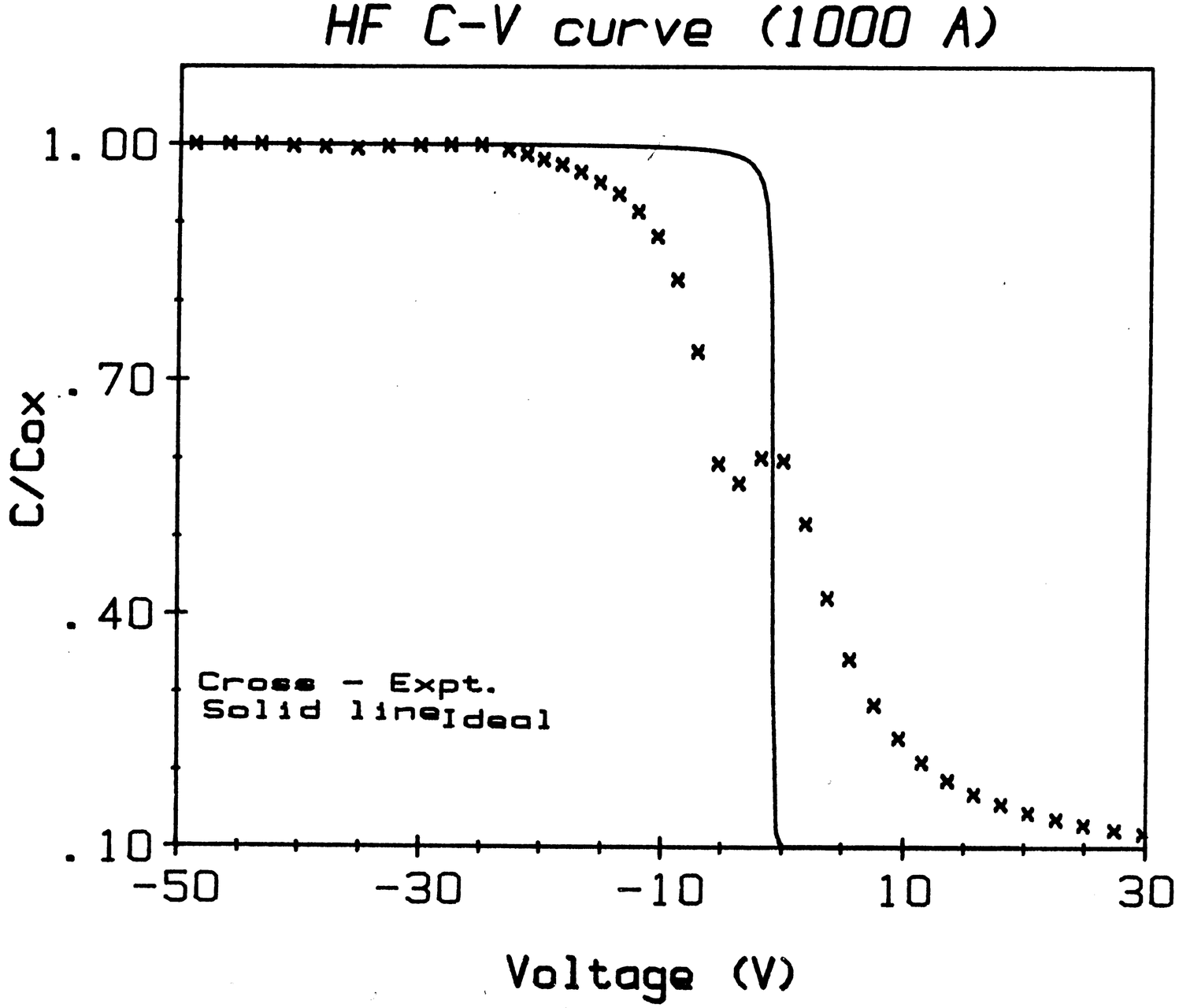

Figure 23. 1000 A Experimental and Ideal High Frequency C-V Curves

4.2.2 HFCV Flatband Shifts

As one would expect, the introduction of an ionic species by implantation should create a C-V stretchout effect, an obvious increase in the total amount of trapped charge present within the Si/SiO_2 structure. In addition, upon annealing the samples, a noticable reduction in the stretchout should be seen restoring the shape of the C-V curve to be similar to the as-grown oxide C-V curves, which were presented in the last subsection. This is partly the case with the 600 A and 800 A samples (Figures 24 and 25) which show a sizable reduction in stretchout after annealing (plotted as open squares) when compared to the as-implanted devices (plotted as diamonds). However, as one progessses with the experiment, an increase in C_{min} is also quite visible for these diagrams. This effect was noticed by Greeuw and Verwey[1] as they performed high dosage F^- implants and speculated on changes of average doping density near the surface of the silicon which would certainly affect the depletion region capacitance and C_{min}.

Note that this is not the condition with the 1000 A sample shown in Figure 26. Stretchout effects are not reduced upon annealing and C_{min} of the annealed sample is lower than the minimum capacitance of the as-implanted sample. The only speculation which can be proposed at this time is that the annealing process is not as effective as the oxide thickness increases and that after a certain thickness for a given dosage, annealing does not occur. Upon observing this series of plots, the flat-band shifts (ΔV_{FB}) for each oxide thickness can be estimated, and the room temperature number of fixed charge (ΔN_Q) calculated. Note that the 1000 A implanted and annealed sample was calculated as having its ΔN_Q increase after annealing as suggested above.

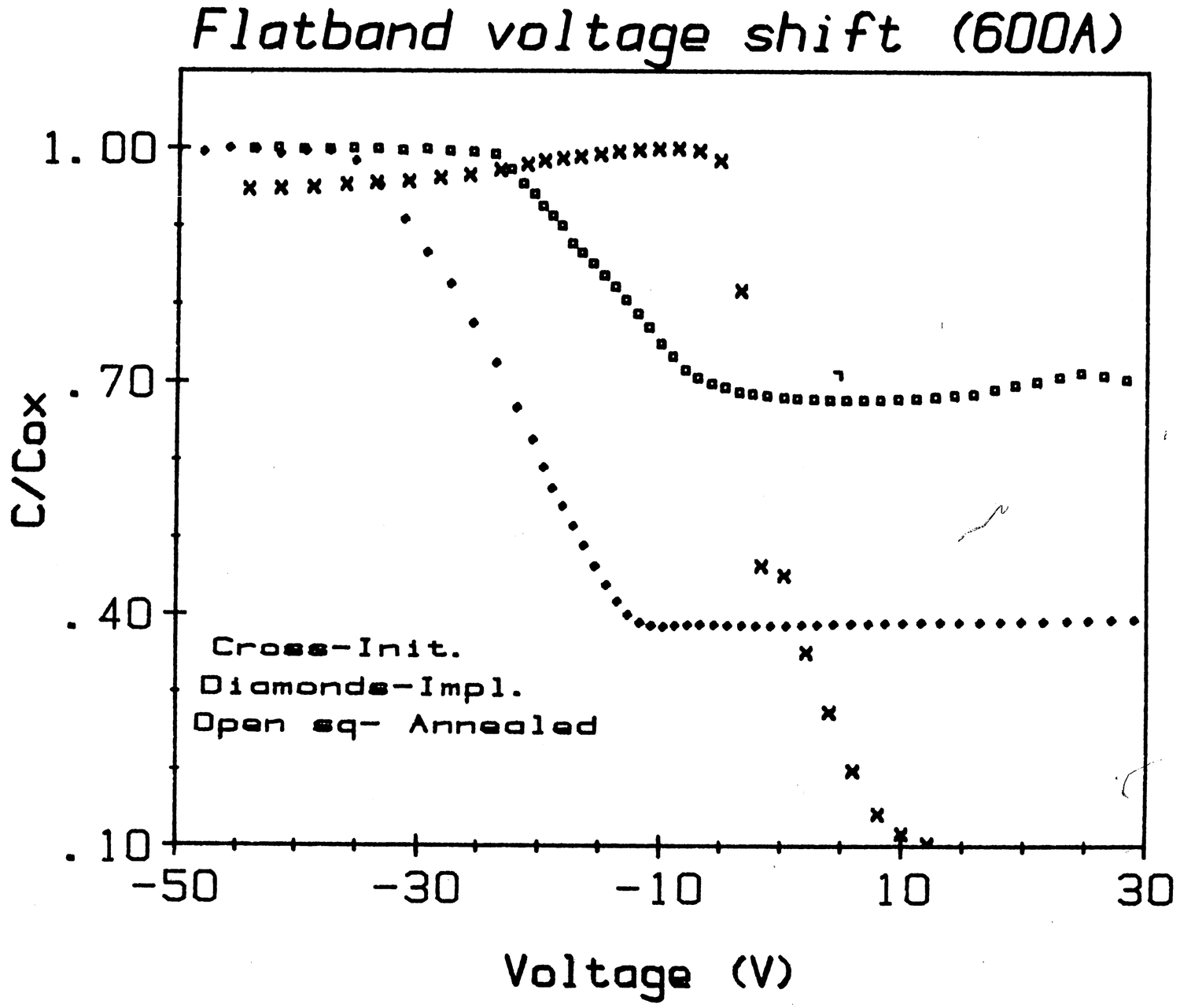

Figure 24. 600 A High Frequency Flat-Band Voltage Curves

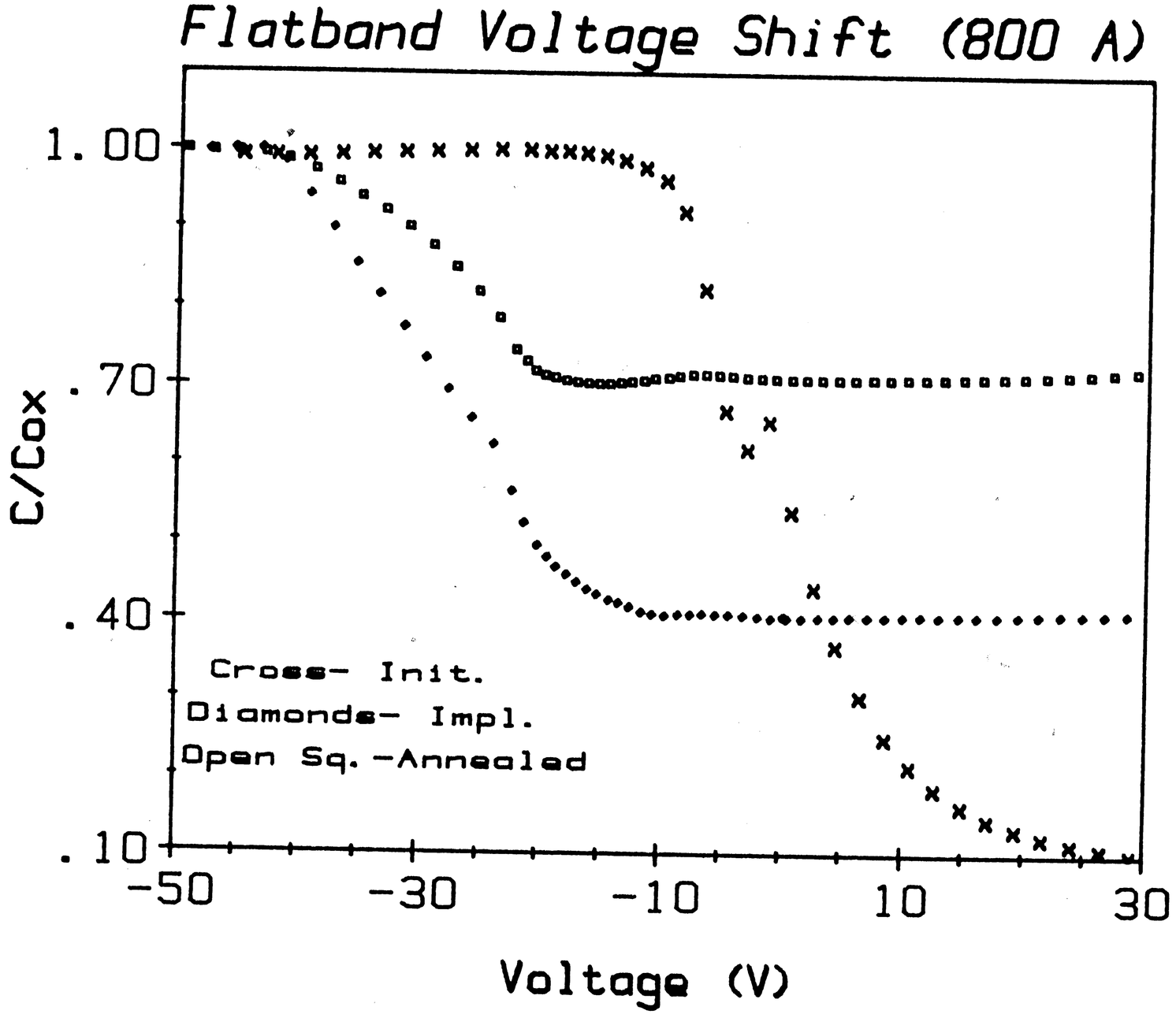

Figure 25. 800 A High Frequency Flat-Band Voltage Curves

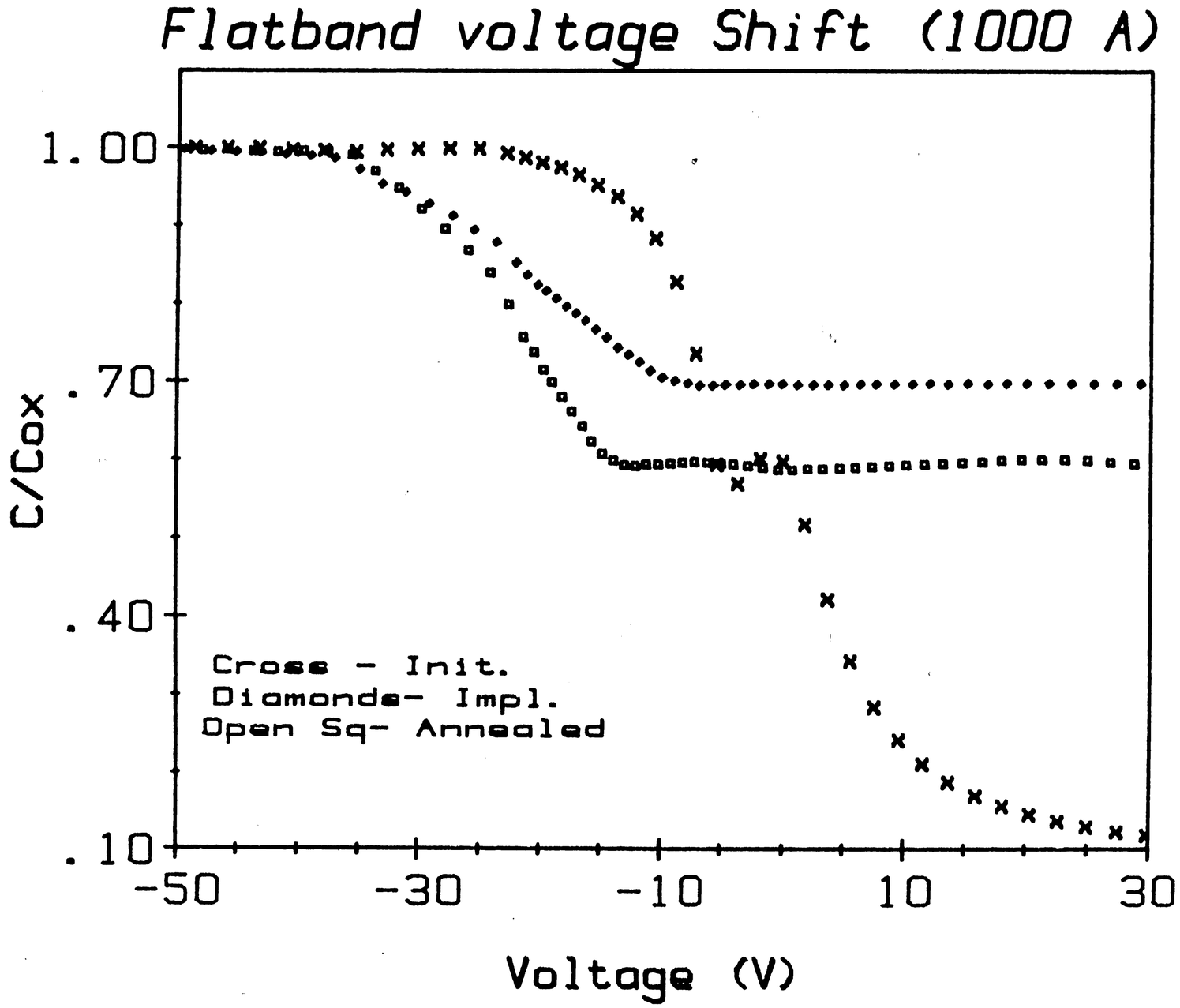

Figure 26. 1000 A High Frequency Flat-Band Voltage Curves

4.3 Quasi-State C-V Measurements

It has previously been mentioned that one of the important features of a Quasi-Static C-V measurement is to find out whether or not a true C_{ox} can be achieved at low frequencies. As an illustration, a 600 A as-grown oxide sample at low frequency is compared to an ideally generated low frequency C-V curve in Fugure 27. The oxide capacitive agreement is relatively good and the slight distortion and shift to the left of the ideal is consistent with the high frequency C-V results. The fall off of the experimental Quasi-Static C-V curve from the ideal at increasing positive voltages may be an indication of a leaky oxide problem. Nevertheless, by making the low freuency C-V measurements, it becomes apparent that a series resistance is present at high frequencies and should be calculated. It is noted that in performing 1 MHz conductance versus voltage (G-V) measurements and utilizing the series resistance method described by Nicollian and Brews[35], an average value of $R_{SERIES} = 220\ \Omega$ is calculated for the three different oxide thickness examples.

Other Quasi-Static figures include a plot of all three as-grown oxide MOS capacitors normalized (Figure 28) which shows good low frequency curves for each oxide thickness, and once again the increasing shift to the left as the oxide thickness increases is consistent with the HFCV curves. As an aside, one may have noticed a downward tilting of C_{ox} in Figures 24 and 25 as the gate voltage becomes increasingly more negative. It is assumed that this is a high E-field effect and this hunch is confirmed by some Quasi-Static measurements of similar nature. However, due to the noise and leakage surrounding these low frequency C-V measurements, none are presented at this time for review.

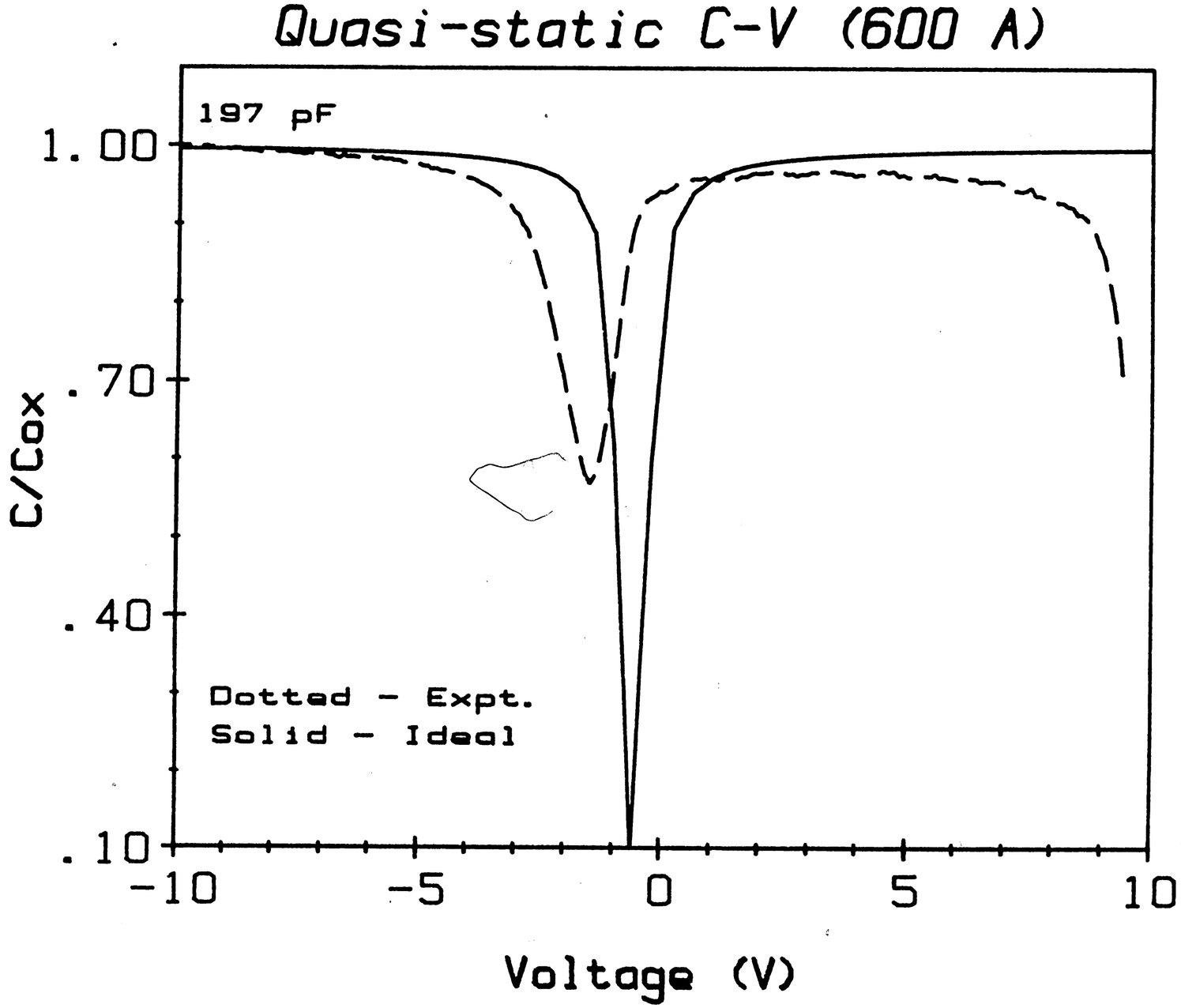

Figure 27. 600 A Experimental and Ideal Quasi-Static C-V Curves

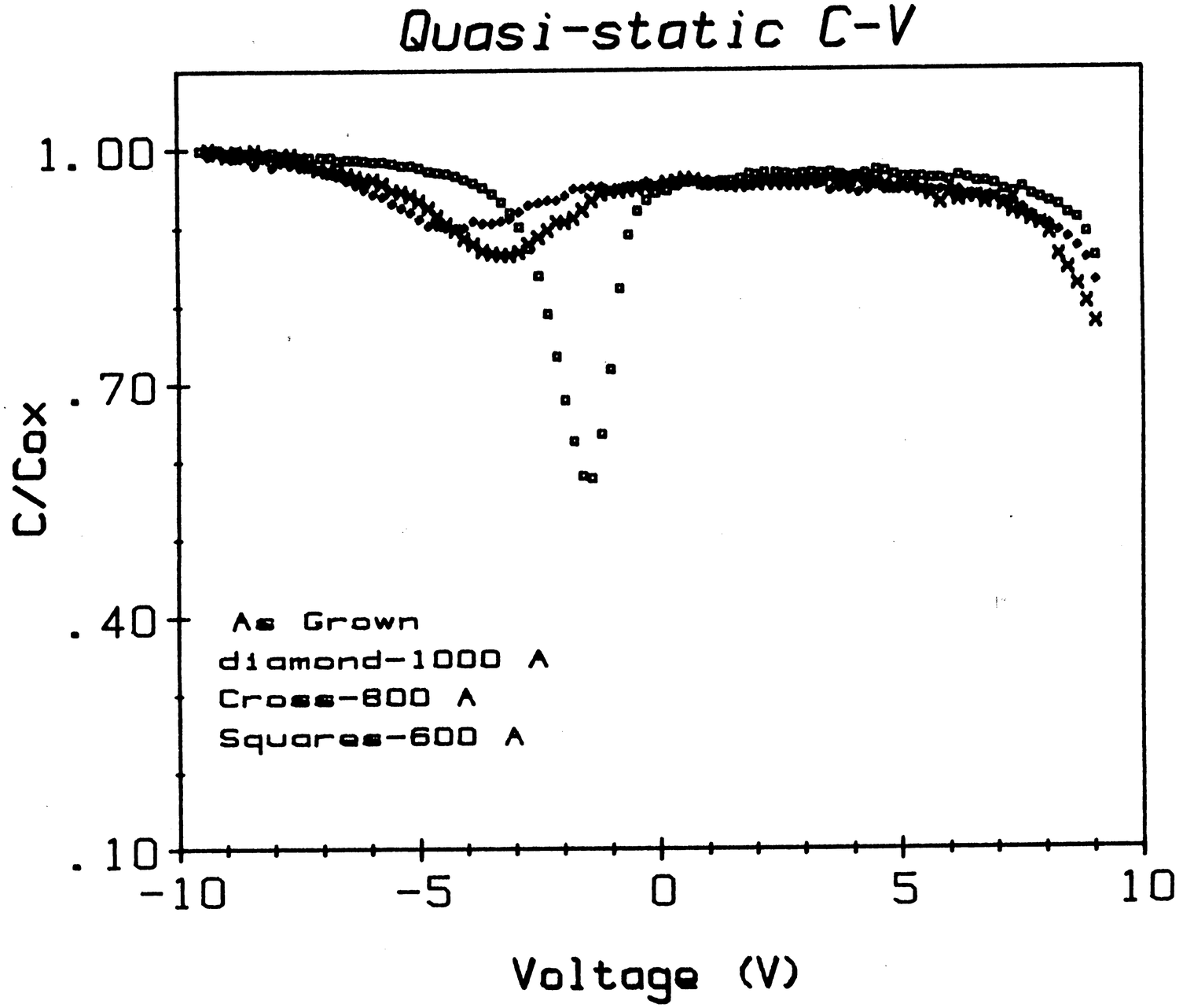

Figure 28. As-Grown Oxide Quasi-Static C-V Curves

4.4 Bias Temperature Stress Measurements

The bias temperature stress (BTS) experiment is performed for every type of sample (as-grown, F^- implanted, and F^- implanted and annealed) in the same manner with the hope of seeing some consistency. All MOS capacitors are heated to a temperature of T = 200° C and are then stressed with a positive and negative bias proportional to their oxide thickness in order to produce an electric field across the oxide on the order of ± 1 MV/cm. As had been mentioned before, if the fluorine is in a mobile state after implantation, the BTS high frequency curves should detect the presence of a negative mobile ion. Note that in the legend listed on Figure 30, solid line for initial or as-grown oxide, solid suare for positive bias at 200° C, and open square for negative bias at 200° C, is consistent for all BTS plots.

Figures 29, 30, and 31, the 600, 800, and 1000 A as-grown oxide BTS curves, respectively, show a relatively normal response to a bias temperature stress test. The high frequency curve's shift to the left under a positive &-field indicates the presence of a positive mobile ion, most likely Na^+ contamination from the metallization step. Under negative applied bias each of the C-V curves returns to a position very close to the original room temperature C-V curve, concluding that only mobile charge is present in these samples.

For the fluorine implanted samples of each oxide thickness, that is, Figures 32, 33, and 34, the BTS behavior is much different. Positive biasing depicts a shift to the right of the room temperature implanted curve, an indication of a negative mobile ion within the MOS capacitor. It is safe to conclude that this is fluorine and, although the shift is not as pronounced as with sodium, it is still visible and measurable in all these cases. One should note that under the negative

bias stress, the C-V shift continues to the right and is less noticable with an increase in thickness. A possible answer for this is that the mobile F^- ions become fixed within the damaged Si/SiO_2 layer and have changed the electrical character of the device. To prove if this is the case, a more in-depth experiment would have to be performed.

Finally, for the annealed MOS capacitors, Figures 35, 36, and 37, there are various effects present, but in all three samples there is a decrease in the shift of the C-V curve for both positive and negative bias temperature stressing. The biased curves tend to hover around the room temperature curve possibly indicating that fluorine as an ion has become less mobile after annealing. The variation of the C_{min} from sample to sample can only be explained by the unique way in which the device may have reacted under BTS testing. It may be stated that the annealing process did not completely remove the implantation damage or electrically activate the fluorine species.

From the figures listed, an estimated flat-band voltage shift (ΔV_{FB}), is used to calculate both the mobile positive ions (Na^+) and the mobile negative ions (F^-) for the conditions when they are applicable. The values calculated do possess a sizable negative surface concentration (N_Q-), corresponding to the implanted fluorine, which was expected. The information provided does give some initial proof of the mobility of a fluorine ion, but additional experiments need to be made.

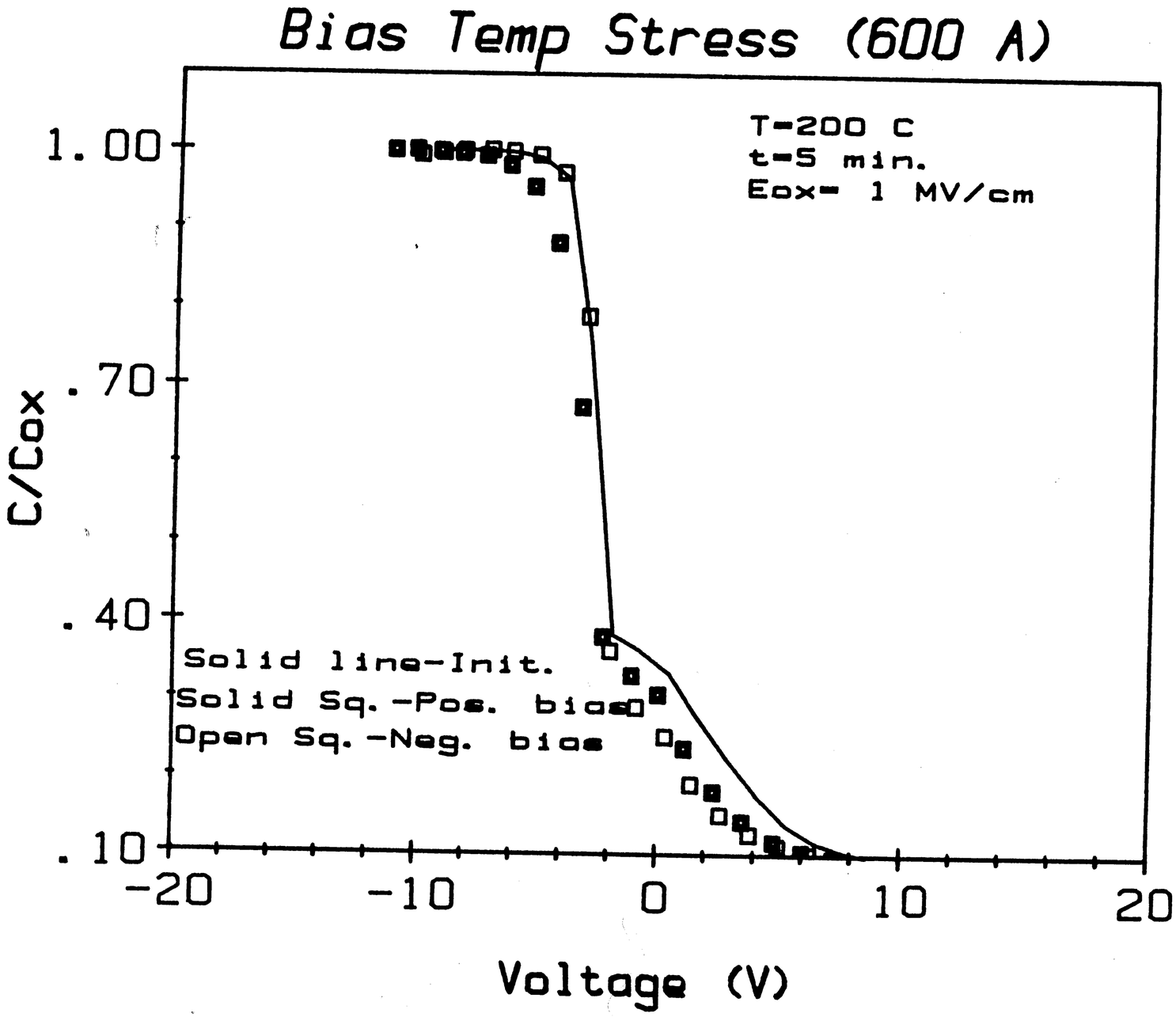

Figure 29. 600 A Bias Temperature Stress - Initial

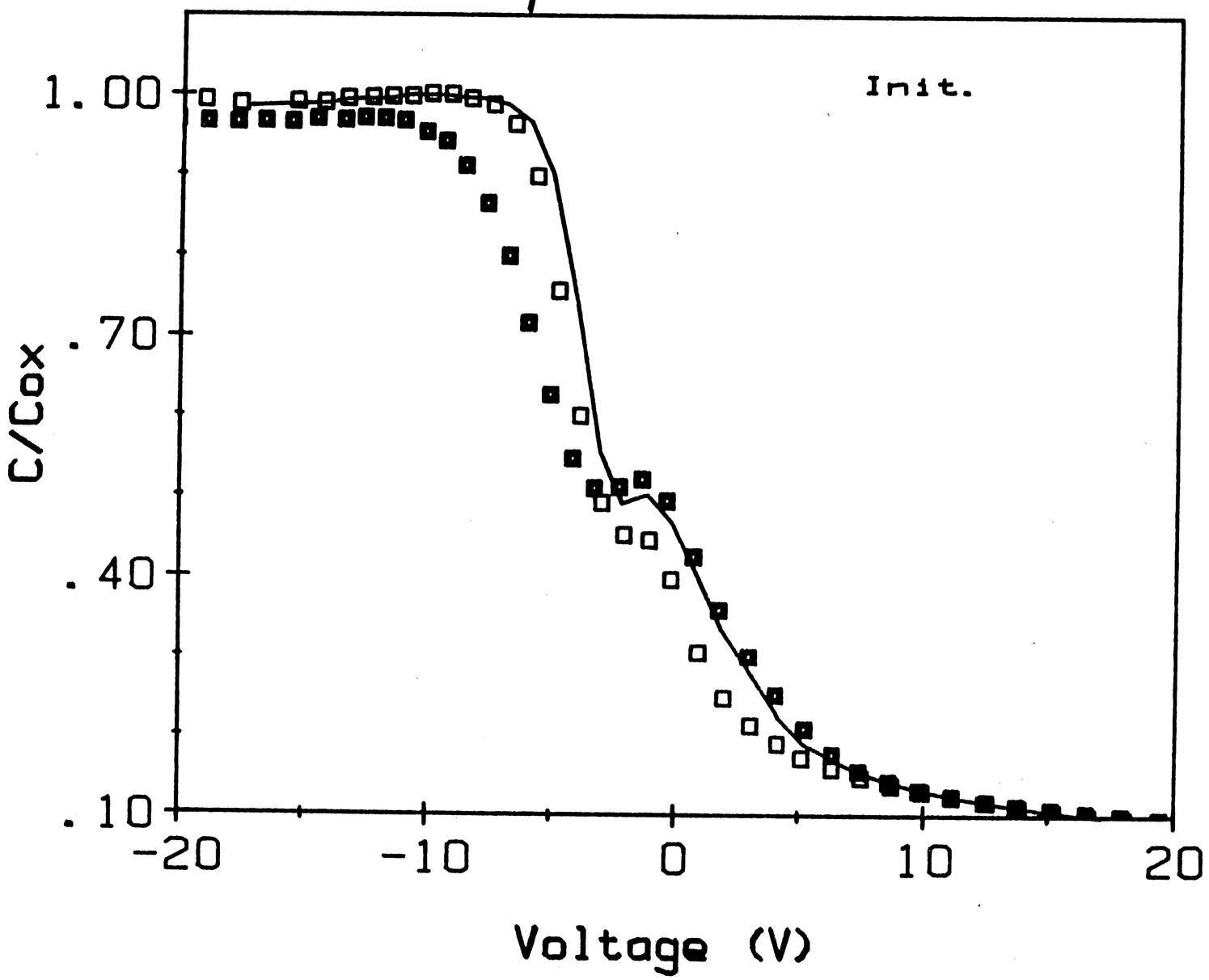

Figure 30. 800 A Bias Temperature Stress - Initial

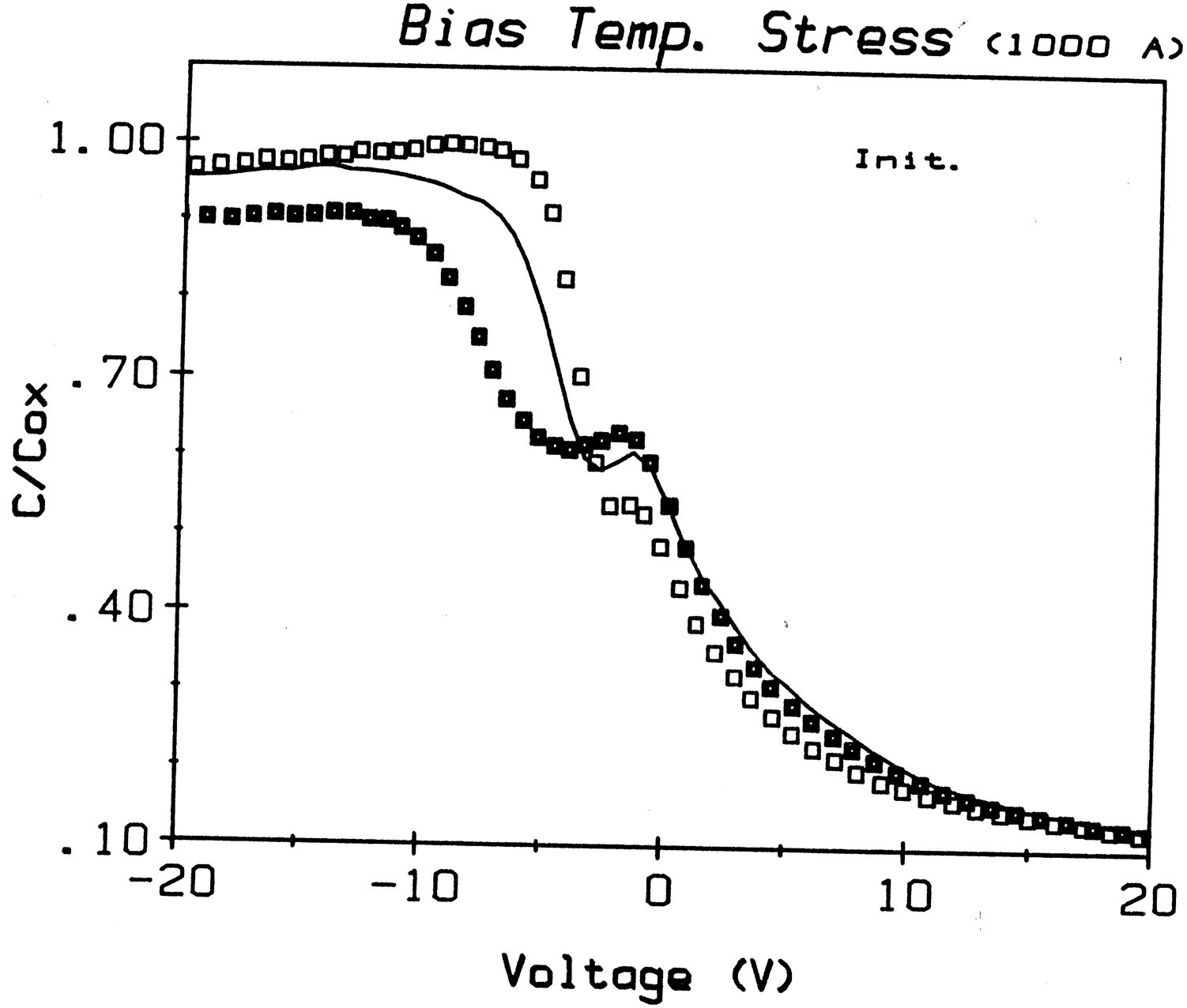

Figure 31. 1000 A Bias Temperature Stress - Initial

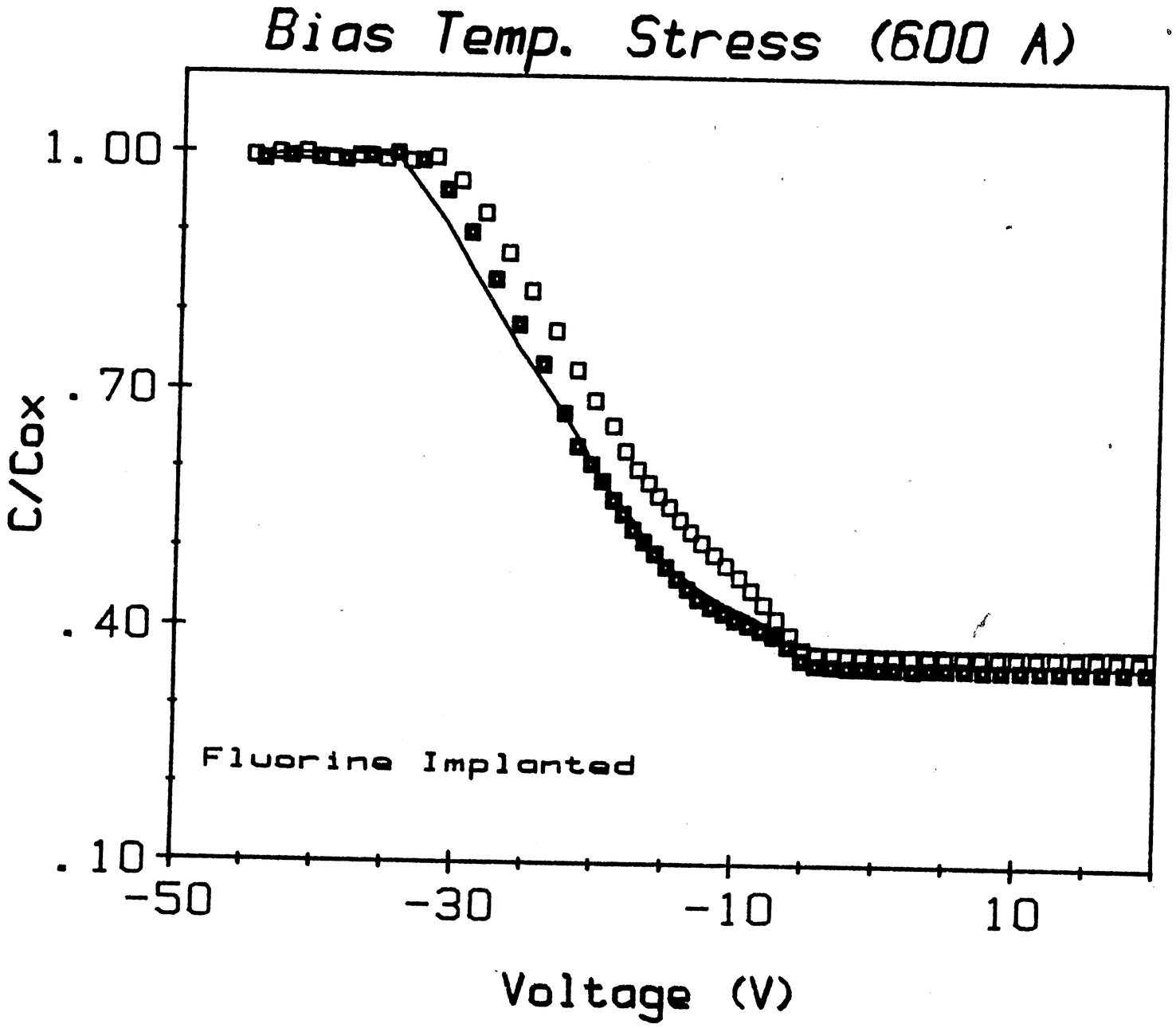

Figure 32. 600 A Bias Temperature Stress - Fluorine Implanted

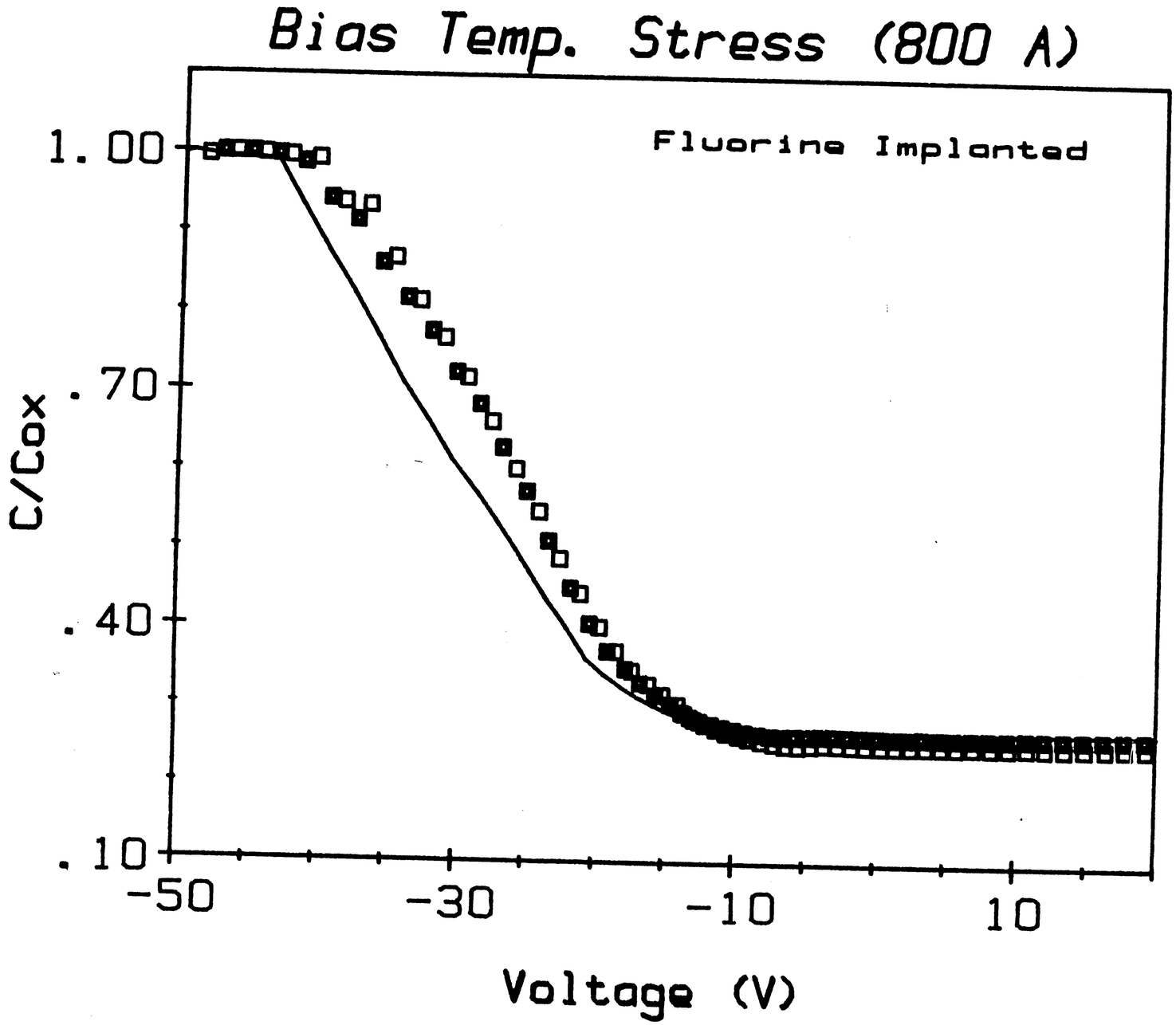

Figure 33. 800 A Bias Temperature Stress - Fluorine Implanted

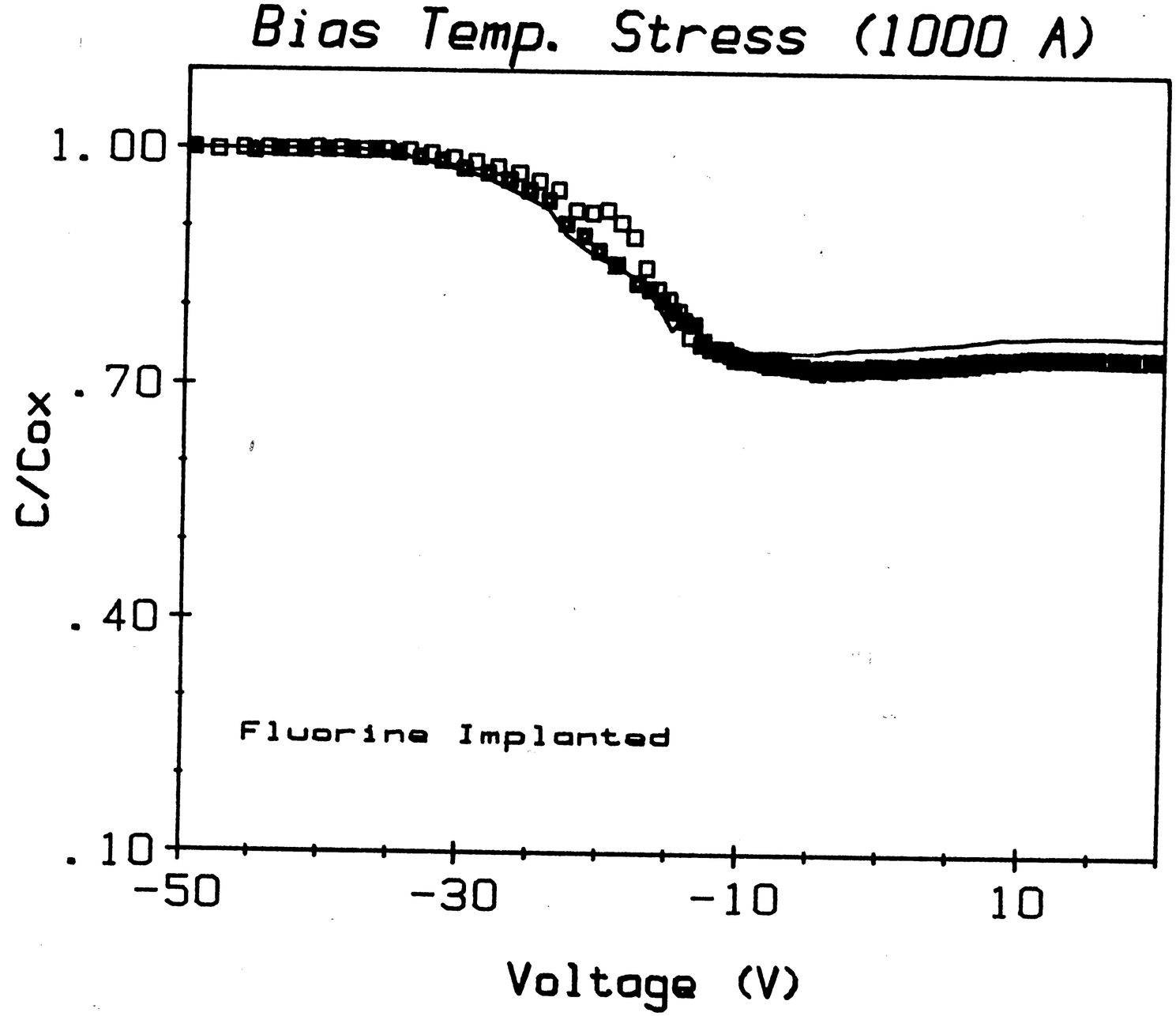

Figure 34. 1000 A Bias Temperature Stress - Fluorine Implanted

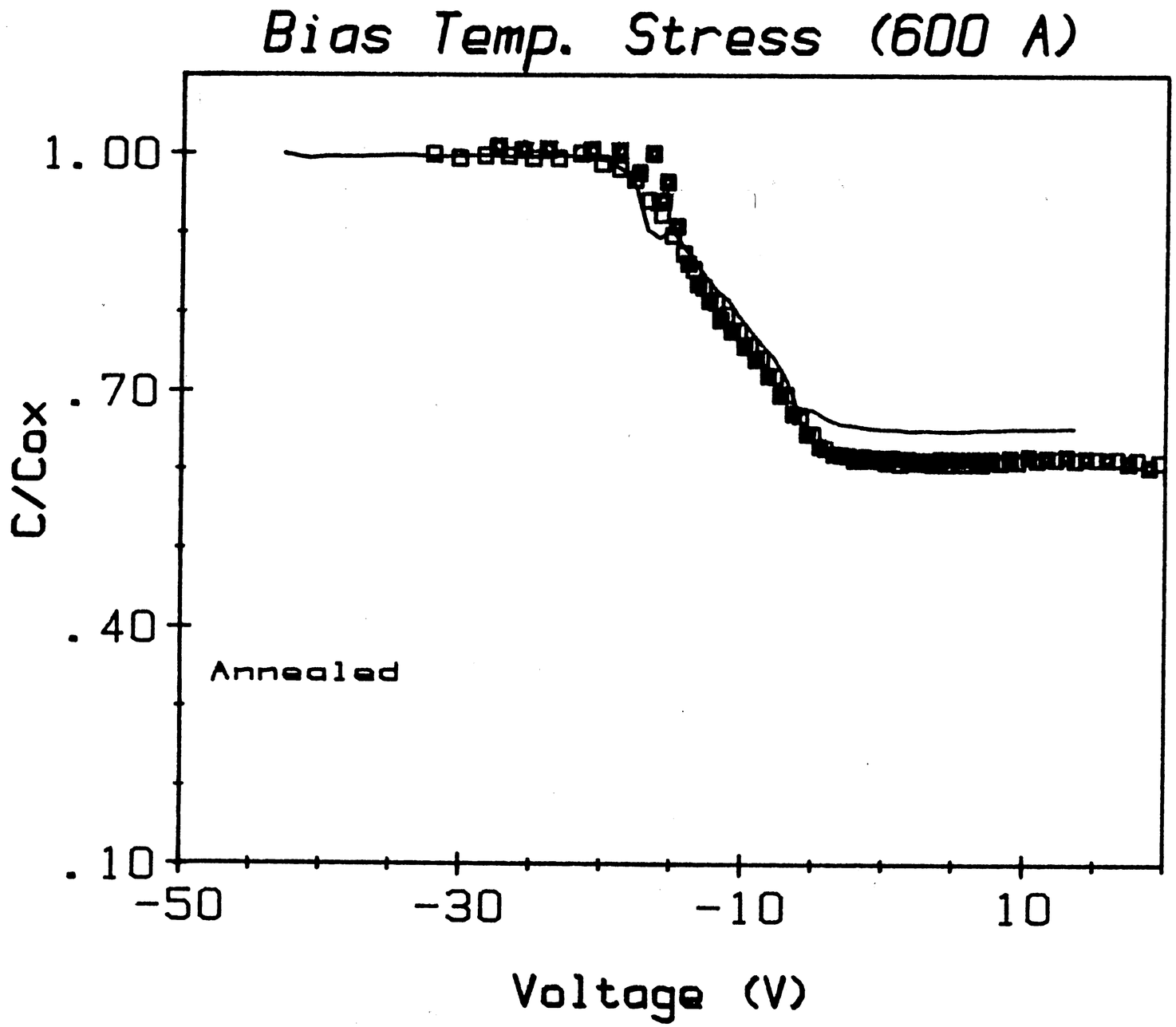

Figure 35. 600 A Bias Temperature Stress - Annealed

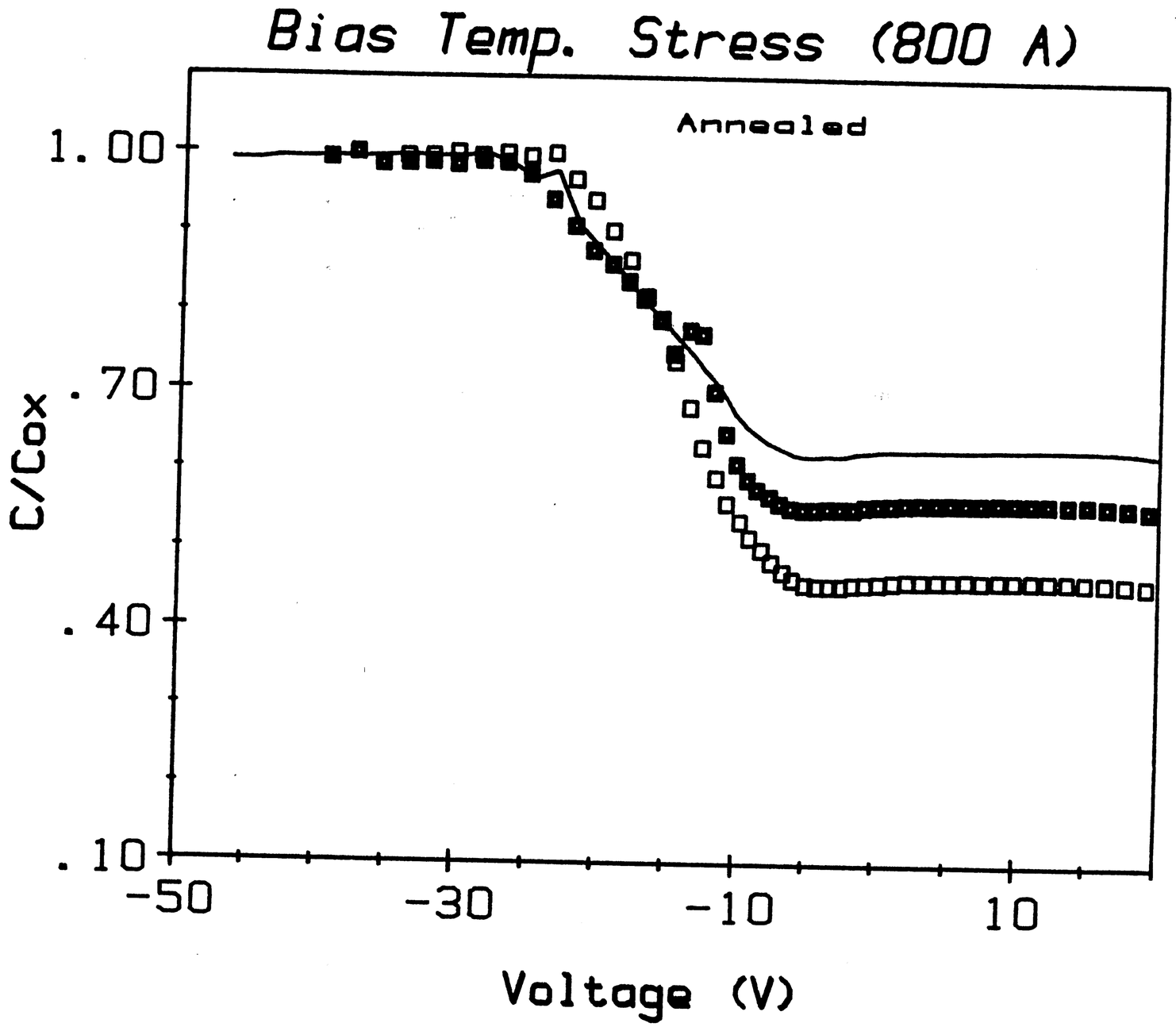

Figure 36. 800 A Bias Temperature Stress - Annealed

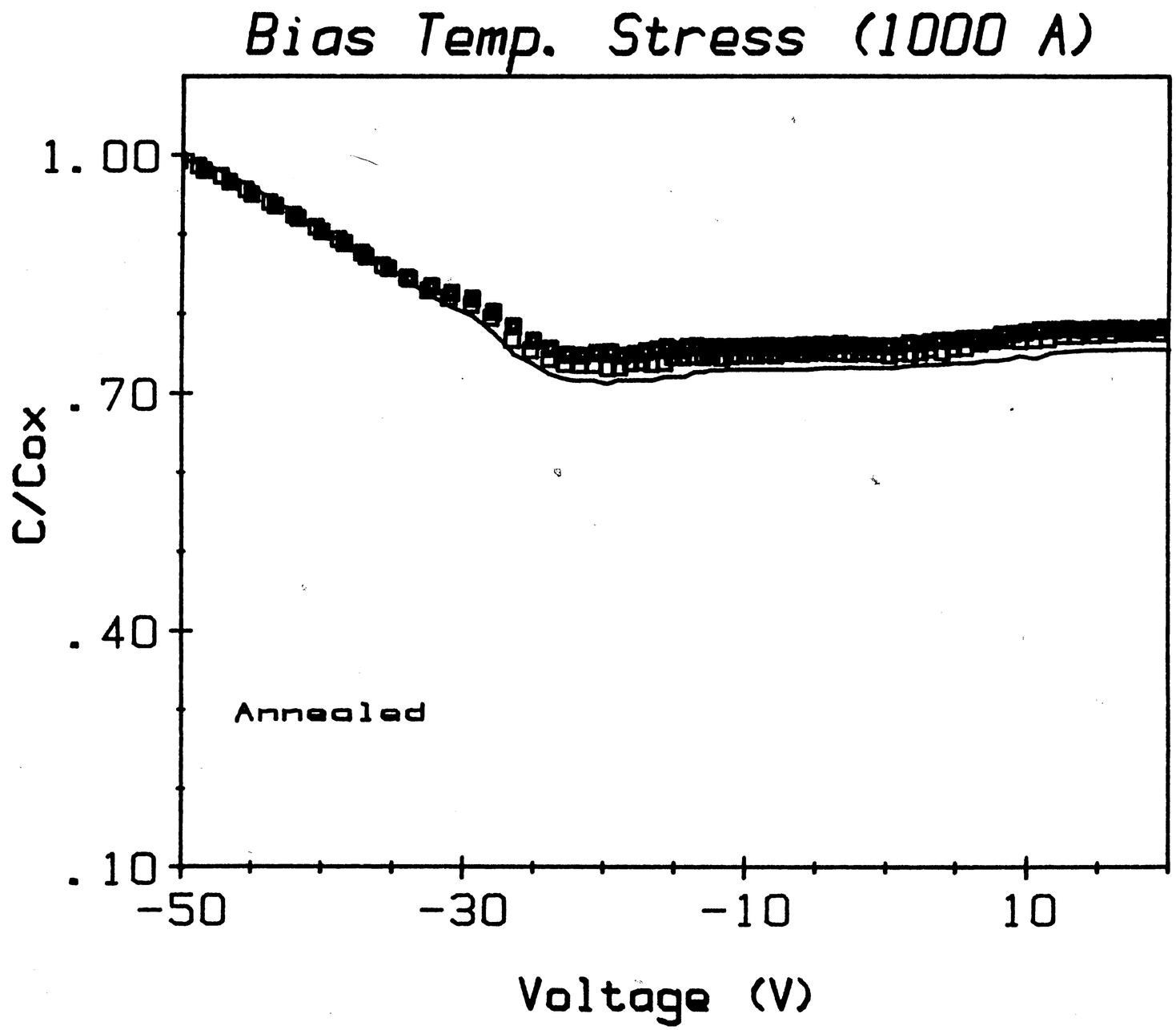

Figure 37. 1000 A Bias Temperature Stress - Annealed

4.5 Interface State Trap Density Measurements

The last measurements made are the high frequency ideal to experimental $D_{it}(E)$ profiles for each case of oxide thickness with all three types of MOS capacitors represented. The midgap $D_{it}(E)$ is initially 200 for each of the as-grown oxide samples (Figures 38, 39, and 40). After the samples are implanted and annealed, the midgap $D_{it}(E)$ is down by an order of magnitude (< 50). This must be an indicator of the effect the fluorine is having on the interface after it is both implanted and annealed. The implanted curves show that this results in most of the reduction of the interface state density, while the implanted and annealed curves are just a bit lower and tend to be flatter for a longer span of energy.

One should be made aware of the spike-type peaks visible in the 800 and 1000 A samples, Figures 40 and 41 respectively, that are at a level of energy 0.25 eV above the valence band E_v. In both situations, implantation and annealing greatly reduces this peak to a much more tolerable level. Figure 39 shows the implanted $D_{it}(E)$ curve with a spike at 0.2 eV which disapppears upon annealing. The position in energy suggests that it is an acceptor level which has been eradicated by the implantation of fluorine with annealing.

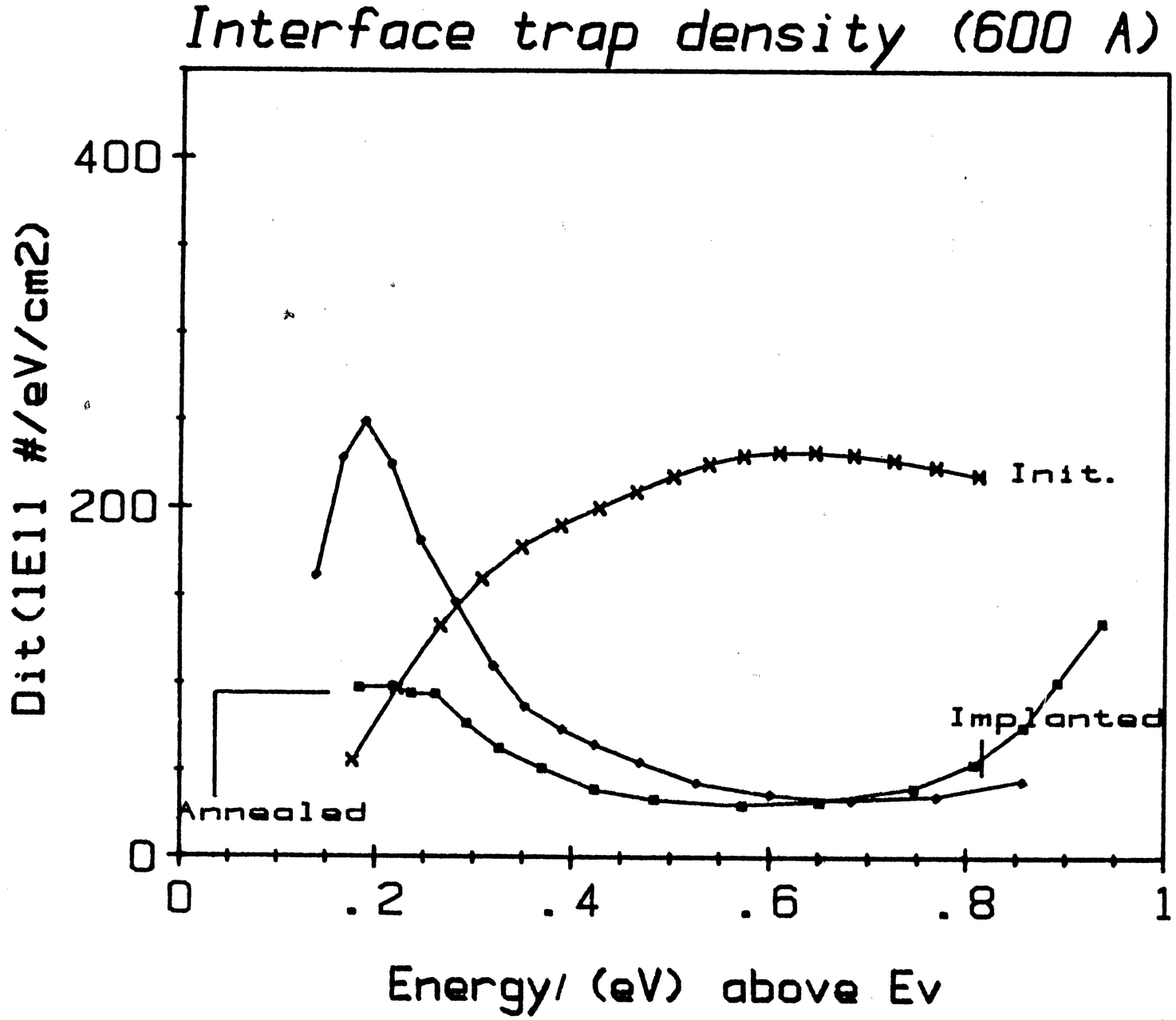

Figure 38. Interface Trap Density - 600 A

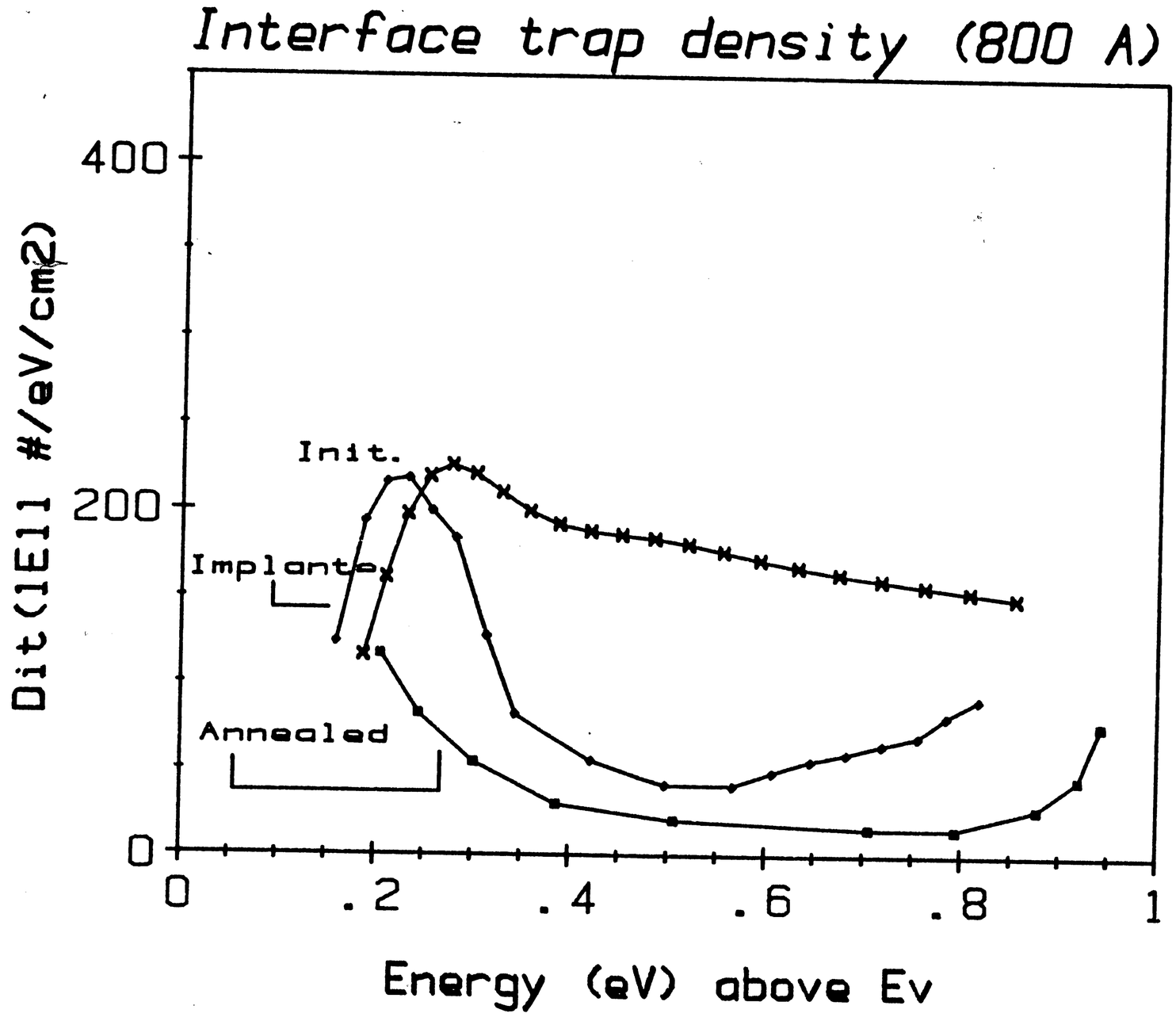

Figure 39. Interface Trap Density - 800 A

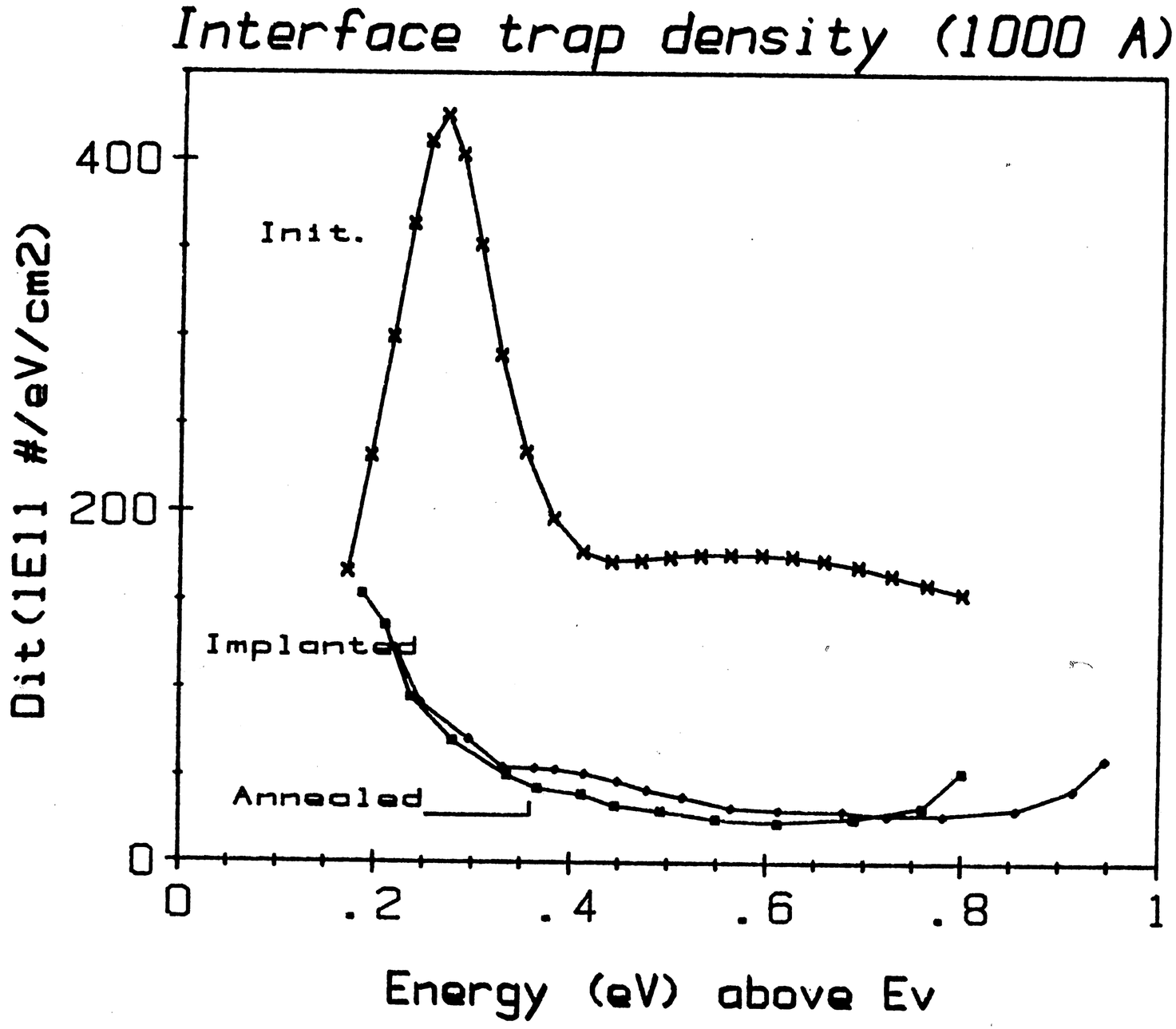

Figure 40. Interface Trap Density - 1000 A

4.6 Experimental Summary

Overall, this thesis experiment produced some rather unique results, which were to be expected from the literature readings concerning fluorine in MOS structures. Specifically, the results of a positive voltage shift from the BTS testing indicates a negative ion mobility, as was the case with Williams and Woods[8], and the changes in the HFCV curve after fluorine implantation with regard to stretchout. Changes in C_{min} were noted and this corresponds to some of the results of Greeuw and Verwey[1]. There is much to be learned about the properties of elemental and ionic fluorine in the MOS capacitive structure as well as its effects at the Si/SiO_2 interface which are very important with regard to discreet device research. This experiment shows much promise and with some proper planning and considering some of the suggestions recommended in the next chapter for experimental redesign, some of the speculations here could turn into positive conclusions.

Chapter 5
Conclusion

In the final chapter, some suggestions are made for future work. Guidelines are presented as a means to how the experiment may be improved upon, or how a wider testing base may be developed in order to draw more accurate conclusions from the analysis. Finally, some personal comments are addressed to the reader for his or her own personal information and understanding as the experiment reflects on the work accomplished.

5.1 Redesign of Experiment

If this experiment were to be redone or modified, I see five experimental parameters which, if performed more carefully, would vastly improve the outcome of the results. They are:

1) Quality oxide growth which will produce a control group of MOS capacitors with little deviance from the ideal;

2) Dosage varaition during the implantation runs (one high, one medium, and one low) certainly should vary the electrical behavior in the resulting devices;

3) Various annealing treatments before (such as RTA) and after metallization to optimize this process step and achieve better results; the postmetal anneal could have its temperature increased to T = 450° C, for example;

4) Ensuring a clean (or as clean as possible) metallization step in order to limit the sodium contamination;

5) Modeling of the MOS capacitors with the equivalent circuit model and attmepting some SPICE simulations as a comparison to experimental curves which are non-ideal.

These are obviously, as I had mentioned, only suggestions for improvement and will require a large investment of time in preparation for such an intricate experiment, but this must be done to have more significant results.

5.2 Final Comments

This is the first time such an experiment has been done at Lehigh University with the entire device processing sequence contained within the Sherman Fairchild Laboratory. It is obvious that very rough results have been obtained. However, detectable effects were observed, which indicate that improvement or refinement of the experiment should be made in the future. This is without a doubt a challenging and important problem because the results to be obtained are on the leading edge of implanted MOS device research and can enhance the knowledge of a very new field in silicon device technology.

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Vita

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