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Improved accuracy of propagation delay measurements of digital logic devices using automatic test equipment /

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Improved Accuracy of Propagation Delay Measurements of Digital Logic Devices Using Automatic Test Equipment

by

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ABSTRACT

Propagation delay inaccuracies can occur when testing digital logic devices on Automatic Test Equipment (ATE). Different measured values are obtained depending on the measurement system used. Correlation becomes a problem when attempting to compare measurements obtained from a bench test set-up and an ATE, or between two different ATEs. The difference can result in errors as large as 100%.

Background material is presented which describes the test methodology and the testing environment. This includes circuit descriptions of the bench test, ATE electronics and the Device Under Test (DUT). A simplified RC model is developed which represents the ATE/DUT interface. It uses measured characteristics of the DUT (i.e., dynamic output resistance) and develops a model of the ATE pin electronics.

A mathematical method is presented by which "correlation factors" can be calculated. These factors are applied to the measured propagation delay values to reduce the error between the bench and ATE data. The procedure was designed so that it can be incorporated into the ATE software.

Device measurements are taken and the correlation factors are applied to the data. The propagation delay value was improved from an error of 50% to less than 2%.

1. INTRODUCTION

Propagation delay measurement inaccuracies can occur when testing digital logic devices on Automatic Test Equipment (ATE). Although modern test equipment boasts of subnanosecond timing accuracies, measurements can have errors as large as 100 percent (2-5ns). These relative timing accuracies yield excellent measurement repeatability but absolute measurements remain in error. If a device were tested on three different ATE systems, the result would be three different values for the same propagation delay measurement. Often these differences are significant and are due to the characteristics of the ATE being used. With older technology devices these differences could be neglected, but with newer technologies these differences are approaching the total propagation delay of the device.

In general, the problem is most evident in SSI/MSI devices that have the fewest number of gate delays and therefore the shortest propagation delay. Testing devices that have propagation delays close to the specified limit may result in good devices being classified as failures. This leads to a correlation problem between the manufacturer and end user of the device. The problem is usually settled by a bench measurement where all test conditions are under tight control.

A. The Problem

The propagation delay is affected by many parameters such as input voltage levels, input rise and fall time, bias on unused input pins and the output load. The manufacturer's data sheet states what each of these parameters should be during the measurement. Modern ATE does an excellent job of controlling these parameters

except for one, the output load. This problem is not a fault of the ATE manufacturers because often the specified load is difficult to obtain even under laboratory conditions (bench test). Although the bench test can be used as a universal standard, it is both tedious and time consuming. A solution to this problem is needed for the following reasons: 1) bench testing each device code is impractical; 2) the ATE is designed to be universal and has inherent parasitic elements; and 3) the device manufacturer's test requirements are established with regard to bench, not ATE measurements.

One solution is to develop a method of translating the measurements obtained on the ATE to the equivalent values obtained under ideal laboratory conditions. In other words, there are two sets of data that are directly related (i.e., propagation delay of output pin number 1, 2, 3, . . etc.) but obtained using different methods (ATE vs Bench or ATE-A vs ATE-B). One way of equating them is by generating a set of numbers that can be added to or subtracted from one set of data to obtain the other. This set of numbers is defined as correlation factors. Two correlation methods presently being used are described below.

1. Direct Subtraction - In this method a sample of devices is measured on the bench and on the ATE. The differences between the two measurements are used by the ATE test program to add to or subtract from the actual measured value.
2. Golden Unit - In this method a sample of devices is measured on the bench, "Correlation Factors" are obtained and inserted into the ATE test program. Each time the test is run on the ATE, the golden devices are tested. These measurements are compared with the stored correlation factors and an algorithm gen-

erates numbers that are used by the ATE program to correct the measured value.

Both methods above are undesirable because they rely on bench measurements. They also do not account for parametric shifts from one device lot to another. Since the bench units do not change, the correlation factors have errors when testing a new lot of devices. The Direct Subtraction method is the most inaccurate because it does not account for any drift of the ATE measurement system. The Golden Unit method requires that the same Golden Units are measured before every testing session. This makes the test program difficult to transport and duplicate on another ATE, and a damaged Golden device would require additional bench testing. Therefore, these methods are inadequate.

B. Goals

Before developing a new approach, I first established several goals.

1. Avoid using bench measurements.
2. Do not use Golden Units.
3. The test program should be transportable.
4. The correlation factors should be based on measurements taken from each device or sample of devices from each lot.
5. Options:
    a. The test program and correlation factor generation would be totally self contained: No external (outside the ATE environment) software or hardware would be needed.

b. Approximations used to obtain correlation factors are kept to a minimum. This approach uses an external circuit simulation program with exact models of the device under test (DUT) and the pin electronics card (PEC) of the ATE. This would allow cause and effect analysis to be done quickly and easily.

C. Solution:

My proposal shows two possible methods of obtaining correlation factors to be used by the ATE program to improve propagation delay measurement accuracy. They both use circuit information about the input characteristics of the PEC and circuit diagrams of the DUT.

1. Network Analysis: Correlation factors can be calculated by first simplifying the network to obtain equivalent models of the DUT and PEC. Then using network analysis techniques, formulas are developed representing the circuit characteristics. Parametric data obtained from device measurements are used in the formula to obtain the correlation factors.

2. Computer Circuit Simulation (i.e., SPICE): Using computer simulation of the network (DUT and PEC), input and output characteristics can be generated that model the data obtained from ATE testing of the device. This requires an accurate circuit description of the DUT and the PEC. The correlation factors could then be obtained by changing the computer model to represent the ideal load conditions (manufacturer's specification).

As an alternative, a partial network description could be used. The minimum requirement would be an equivalent circuit model of the output of the DUT and the equivalent circuit model of the input of the PEC. A different set of correlation factors would be obtained from this computer simulation.

2. AC TESTING

A. General

For propagation delay measurements, the device manufacturer's data sheet specifies the load circuit (Figure 1) and characteristics of the input waveform applied to the DUT (Figure 2). This includes input low voltage (V_{IL}), input high voltage (V_{IH}), minimum pulse width (t_{pw}) and threshold voltage (V_{th}). The threshold voltage is the point on the input and output waveform at which the propagation delay is measured (Figure 2). Inaccurate timing measurements will result if any of these conditions are changed.

There is also another voltage I call the device threshold voltage (V_{thd}). It is the point at which the device senses a change on its input and begins to react. This threshold is usually different than V_{th} specified by the device manufacturer. V_{thd} may be above or below V_{th}, but for this example I chose V_{thd} to be less than V_{th}.

Figure 2(a) shows how the propagation delay is measured with an input having zero rise time. In reality, the input waveform has a finite rise time as shown in Figure 2(b). The effects of V_{thd} can now be seen. Since the device does not react until the input reaches V_{thd}, the output waveform is delayed by a certain amount, shown as (1) in

Figure 2(b). Although the input signal is now propagating through the device, the propagation delay measurement does not start until the input reaches V_{th}. The measured propagation delay (t_{pda}) is less than the original propagation delay (t_{pd}) by an amount shown as (2) in Figure 2(b) and:

$$t_{pd} = t_{pda} + (2)$$

In this example, I now apply a capacitive load to the output of the device. Figure 2(c) shows two things happening: first, the output is delayed further as the output driver of the device starts charging the load capacitor. This delay is shown as (3). The second delay is due to the effect of the load on the output rise time. The output takes longer to reach the threshold voltage and results in an additional delay shown as (4) in Figure 2(c). Therefore, to obtain the original propagation delay, the following equation applies.

$$t_{pd} = t_{pdc} + (2) - (3) - (4)$$

In general, the propagation delay specified by the device manufacturer is t_{pda} (bench test), not the t_{pd} shown in Figure 2; and t_{pdc} is the value obtained from the ATE. The value of V_{thd} varies from manufacturer to manufacturer and the effects of V_{thd} on propagation delay are small and can be ignored. However, the effects of device loading can be significant and are a major source of errors in device testing.

B. Bench Measurements

Figure 3 shows how the manufacturer's test conditions can be duplicated on a bench

fixture for an LSTTL device. High quality test equipment should be used including high impedance test probes. (For testing ECL devices these probes would be replaced by 50Ω coaxial cable). The printed circuit (PC) board must keep lines as short as possible to minimize stray capacitance. (For a 50Ω system, lines must be of equal length and the PC board must represent a 50Ω transmission line).

The propagation delay is then measured manually using an oscilloscope. Care must be taken to: 1) include the probe capacitance in the DUT load calculation and 2) measure the time between the input and output waveforms at the proper threshold voltage.

C. ATE Measurements

Modern ATE manufacturers attempt to emulate the I.C. manufacturers' data sheet specification for the DUT load circuit. But the load is different due to long wiring lengths, series resistance, open relays, printed circuit board stray capacitance and inductance. This results in a complex load impedance on the DUT output that is a major cause of measurement errors especially at high frequencies (> 1 MHz).

A diagram of a typical ATE/DUT interface (ATE test head) and its electrical equivalent is shown in Figure 4. The electrical model changes slightly as relays of the circuit are opened or closed, and the PEC is programmed by the ATE to be in the correct mode (Input, Output or Tri-state) for the test being performed.

The electrical equivalent of the ATE test head can be complex but many of the components are so small they can be neglected. In the past, the entire circuit was modeled as a single lumped capacitance. This model may be acceptable for older technology

devices, but with the new advanced devices (ALS, AS, HCT, etc.) a more accurate model may be needed.

The ATE uses 50Ω transmission lines for the signal path to and from the DUT. These transmission lines are transparent to the ATE and DUT if all the lines are terminated with 50Ω. This works well for the ECL family of devices, since the device provides the required 50Ω terminations on the input and output. But, other logic device families (i.e., TTL, FAST, HCT, etc.) have high input impedance and low output impedance (typically 30 to 120 ohms).

Signal integrity is maintained at the input of the DUT because of the high input impedance of the device. During the propagation delay test, the ATE attaches two lines to the input of the DUT (force and sense lines). The 50Ω force line sends the pulse to the DUT and it returns to the PEC through the 50Ω terminated sense line. The effect of the DUT on the pulse is negligible for two reasons: 1) the force line drivers are designed to drive transmission lines and can absorb reflections that take place and 2) the signal path remains matched because the force and sense lines are both terminated with 50Ω.

Signal integrity is not maintained at the output of the DUT if the output impedance does not match the ATE transmission line. In addition, when the ATE software configures a PEC as an output, parasitic elements are added to the DUT output (i.e., active load circuitry). The DUT output loading problem can be summarized by the following:

1. Typically, logic devices are not transmission line drivers. They were designed to drive short, high impedance lines.

2. Because of the impedance mismatch, the transmission line is no longer transparent and parasitic circuit elements are added to the output.

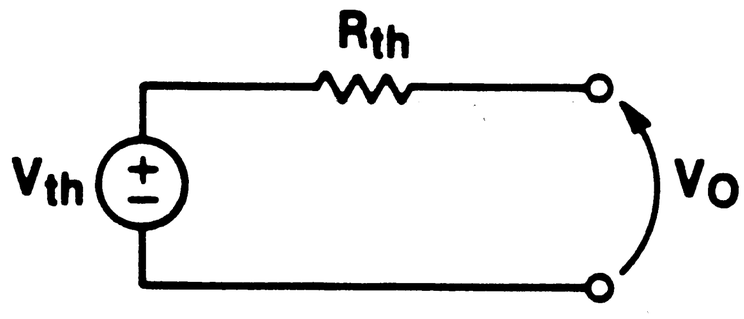
3. Active load circuits on the PEC, not present on the input pin, add significant loading on the DUT output.

The ATE model will be discussed later, but it is the interaction of this ATE load and the output impedance of the DUT that causes additional propagation delay errors. In order to analyze this problem, it is first necessary to determine the output impedance of the DUT.

3. DUT OUTPUT IMPEDANCE

In general, most logic circuits contain an output buffer/driver circuit that acts as isolation for the logic circuitry and increases the output drive capabilities. Typically, this circuit is configured in a "totem pole" style, where it has "pull-up" and "pull-down" circuitry. This switches the output between the high and low voltage state.

Through a detailed circuit analysis of the buffer/driver, it can be shown that the output can be represented by a Thevenin equivalent voltage and resistance. The figure below shows this simplified circuit.



Since the "pull-up" and "pull-down" circuitry are different, there would be two Theve-

nin circuits depending on the state of the output.

As an example of this, let's look at an equivalent circuit of a TTL output driver. Figure 5(a) shows the "totem pole" style output, where Q_1 is the "pull-up" transistor and Q_2 is the "pull-down" transistor.

During the pull-down state Q_1 is off and Q_2 is on (Figure 5(b)). Using the small signal equivalent model of the transistor, Figure 6(a) shows that $R_{th} = r_o$ and $V_{th} = r_o \times (I_L - g_m v_1)$. When the output is in the pull-up state, Q_1 is on and Q_2 is off (Figure 5(c)). The Thevenin equivalent model of the output is $R_{th} = (r_\pi + R_1) \,||\, (r_o + R_2)$ and $V_{th} = g_m v_1 r_o - I(r_o + R_2) + V_{cc}$, as shown in Figure 6(b).

It must be noted that the small signal equivalent circuit of the transistor is being used because during the transition (high-to-low, or low-to-high) the transistor is in the normal active mode. When the static DC measurements are made, the output transistors are in the saturated mode of operation and a different transistor model would be needed to represent this condition. Therefore, the output resistance is a dynamic one that is different than the static DC resistance (where $R_{OL} = V_{OL}/I_{OL}$ and $R_{OH} = V_{OH}/I_{OH}$). Throughout this paper I shall refer to the dynamic output resistance as r_o.

4. THE IDEAL DUT LOAD

The ideal DUT load is that specified by the device manufacturer's data sheet and is used when making bench measurements. By examining the load circuits of several different technologies (Figure 1), the DUT is generally loaded with a capacitor (C_L) and a resistor (R_L). The resistor is used to develop the proper DC amplitude level and has

negligible effect on the dynamic response. Therefore, it can be ignored for this analysis.

Many device manufactures show typical performance curves. One such curve is shown in Figure 7[1] which is the propagation delay (t_{pd}) vs load capacitance (C_L). It is assumed that these curves are straight lines and the formula shown below can be used to represent them.

$$t_{pd}\,(C_L) = \left(\frac{\Delta t_{pd}}{\Delta C_L}\right) C_L + t_{pd}(0)$$

Where,

$$t_{pd}(0) = \text{Logic delay} + \text{Buffer/Driver (unloaded)}$$

$$\Delta t_{pd}/\Delta C_L = \text{Slope of the line}$$

The slope of these curves ($\Delta t_{pd}/\Delta C_L$) has units of ohms. This resistance is proportional to the dynamic output resistance r_o. The equation used to find resistance has the form shown below. The proportionality constant (K_o) will be defined later.

$$r_o = K_o \left(\frac{\Delta t_{pd}}{\Delta C_L}\right) \tag{1}$$

The no load propagation delay ($t_{pd}(0)$) has two values because the high-to-low circuitry produces a different propagation delay than the low-to-high circuitry.

$$t_{pd}(0) = \text{Logic delay} + \text{Buffer/Driver (high-to-low)}$$

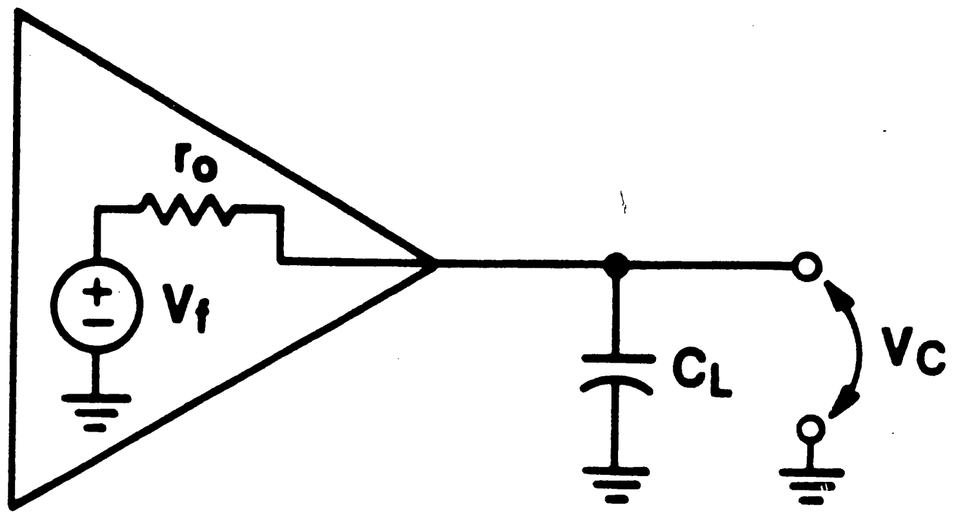
$$t'_{pd}(0) = (\text{Logic delay})' + \text{Buffer/Driver (low-to-high)}$$

Next, I will show that the propagation delay due to the capacitive load circuit can be represented by an RC low-pass filter where R is the dynamic resistance r_o. I will also

show that the slope of the t_{pd} vs C_L curve can be used to calculate r_o. The proportionality constant, K_o, will also be determined. This calculation is important in the determination of the correlation factors.

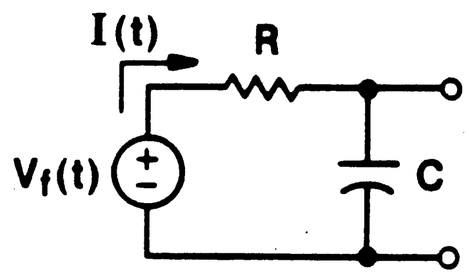
5. RC NETWORK

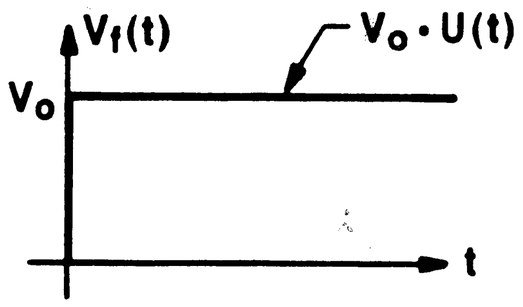
A simplified diagram of the DUT driver and load circuit is shown below.



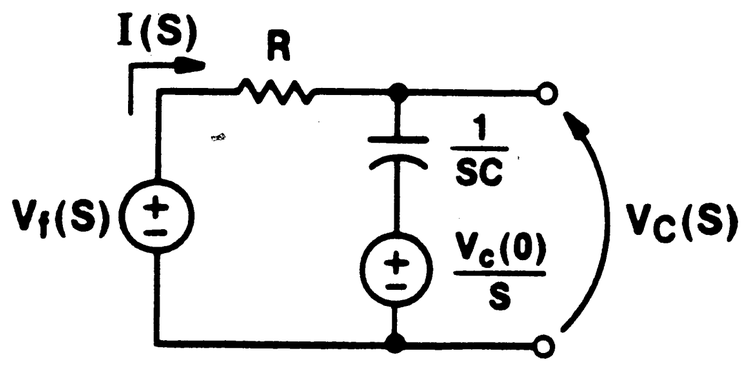
It is represented by a forcing voltage (V_f), a series resistor (r_o) and load capacitor (C_L). The overall output response (V_c) will be the sum of the forced response (V_f) and the natural response of the network. This series RC network can be analyzed using Laplace Transforms.

A. Unit Step Input





1. The input voltage (V_f) is a unit step input (U(t)). Transforming the circuit:



where, $V_c(0)$ = initial charge on the capacitor.

2. Using Kirchhoff's Current Law (KCL):

$$I_R(S) + I_c(S) = 0$$

$$\frac{V_c(S) - V_f(S)}{R} + SC\left[V_c(S) - \frac{V_c(0)}{S}\right] = 0$$

$$V_c(S)\left[\frac{1}{R} + SC\right] = \frac{V_f(S)}{R} + CV_c(0)$$

$$V_c(S) = \left[\frac{V_f(S)}{R} + CV_c(0)\right]\left[\frac{R}{1 + RCS}\right]$$

$$V_c(S) = \frac{V_f(S) + RCV_c(0)}{(1 + RCS)} \qquad (2)$$

3. Substituting the forcing function:

$$V_f(t) = V_o U(t)$$

And transforming it:

$$V_f(S) = \frac{V_o}{S}$$

$$V_c(S) = \frac{V_o/S + RC\,V_c(0)}{(1 + RCS)} = \frac{V_o + RCS\,V_c(0)}{S(1 + RCS)}$$

$$V_c(S) = \frac{V_o}{S(1 + RCS)} + \frac{RC\,V_c(0)}{1 + RCS} \qquad (3)$$

4. After some mathematics and taking the inverse transform we obtain:

$$V_c(t) = V_o(1 - e^{-t/RC})\,U(t) + V_c(0)\,e^{-t/RC}\,U(t) \qquad (4)$$

B. Proportionality Constant, K_o, of the Unit Step Input

The proportionality constant is defined as a ratio of the input to the output voltage. In other words, K_o proportions the RC time constant value to represent the time delay from a specified point on the output.

To show this, I will now define the propagation delay (t_{pd}) as the time it takes the output waveform to reach the midpoint (50%) of its final value from the midpoint of the input waveform. To simplify the calculation, all initial conditions are zero ($V_c(0) = 0$). Equation (4) now has the following form.

$$V_c(t) = V_o(1 - e^{-t/RC})$$

Solving for the propagation delay (t_{pd}) results in the following.

$$t_{pd} = -RC \ln(1 - V_c(t)/V_o)$$

$$\text{Where } \frac{1}{K_o} = -\ln(1 - V_c(t)/V_o)$$

Substituting the following into the propagation delay equation above,

$$V_c(t) = 0.5V_o,$$

then:

$$t_{pd} = 0.693\ RC$$

$$\text{and since } t_{pd} = RC/K_o$$

$$K_o = 1.443$$

The value of t_{pd} represents the time it takes for the output voltage to rise to 50% of its final value with an input step voltage.

If we assume that R remains constant, then for a change in capacitance (ΔC) there is a corresponding change in the propagation delay (Δt_{pd}). Solving for R, we obtain a solution very similar to equation (1), where $K_o = 1.443$.

$$R = 1.443 \frac{\Delta t_{pd}}{\Delta C}$$

This resistance is the dynamic output resistance (r_o) of the DUT which represents the slope of the t_{pd} vs C_L curve of the device.

$$r_o = 1.443 \frac{\Delta t_{pd}}{\Delta C_L}$$

The above formula has one flaw because it represents the response of the network to an input signal with zero rise time. In a real situation, an input waveform has a finite rise time as shown in Figure 2 and the above formula changes.

C. RAMP Input

1. The input voltage (V_f) is a Ramp function. The analysis is performed as before starting with equation (2).

$$V_c(S) = \frac{V_f(S) + RCV_c(0)}{(1 + RCS)} \qquad (2)$$

The Ramp forcing function is:

$$V_f(t) = \frac{V_o}{T_o} t\, U(t)$$

This transforms into:

$$V_f(S) = \frac{V_o}{T_o}\left(\frac{1}{S^2}\right)$$

2. Substituting $V_f(S)$ into equation (2):

$$V_c(S) = \frac{\frac{V_o}{T_o}\frac{1}{S^2} + RC\, V_c(0)}{(1 + RCS)}$$

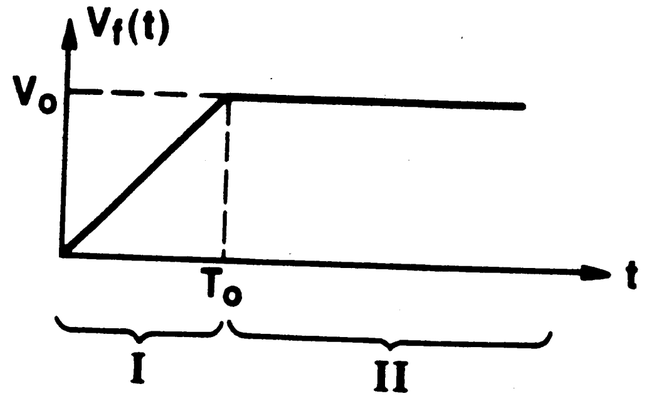
$$V_c(S) = \left(\frac{V_o}{T_o}\right)\left(\frac{1}{S^2(1 + RCS)}\right) + \frac{RC\, V_C(0)}{1 + RCS} \qquad (5)$$

3. Taking the inverse transform we obtain:

$$V_c(t) = \frac{V_o}{T_o} t\, U(t) + \frac{V_o}{T_o} RC\,(e^{-t/RC} - 1)\, U(t) + V_c(0)\, e^{-t/RC}\, U(t) \qquad (7)$$

This formula represents the output voltage response of the RC network to a Ramp input voltage.

D. Complete Response of the RC Network



The above waveform represents a more realistic input signal applied to a DUT. It is a low-to-high transition forcing function with a finite rise time and levels off at time T_o. To analyze the output response, the input must be divided into two parts.

1. For $0 < t < T_o$ (Region I) the response would be the ramp function and equation (7) applies.

$$V_c(t) = \frac{V_o}{T_o} t\, U(t) + \frac{V_o}{T_o} RC\,(e^{-t/RC} - 1)\, U(t) + V_c(0)\, e^{-t/RC}\, U(t) \qquad (7)$$

2. For $t > T_o$ (Region II) the response would be the unit step function, equation (4), with initial conditions ($V_c(0)$) being the value of equation (7) at $t = T_o$ (end of Region I).

$$V_c(t) = V_o\,(1 - e^{-t/RC})\, U(t) + V_c(0)\, e^{-t/RC}\, U(t) \qquad (4)$$

where,

$$V_c(0) = V_c(T_o) = \frac{V_o}{T_o}(T_o) + \frac{V_o}{T_o}(RC)\,(e^{-T_o/RC} - 1)$$

$$V_c(0) = V_o\left[1 + \frac{RC}{T_o}\,(e^{-T_o/RC} - 1)\right]$$

E. Proportionality Constant, K_o, of the Complete Response

Solving the above equations to find K_o, as we did with the unit step input, would be a non-trivial task. Let's examine the unit step input equation again. After making the assumptions about how the propagation delay is measured and normalizing the equation we obtained the following.

$$t_{pd} = 0.693RC$$

where

$$K_o = \frac{1}{0.693} = 1.443$$

The value of K_o remains constant regardless of R or C. Therefore, if we normalize further by letting R=1Ω and C=1F, then the proportionality constant is obtained directly.

$$K_o = \frac{RC}{t_{pd}} = \frac{1}{t_{pd}} \tag{8}$$

Where t_{pd} has units of seconds and K_o is dimensionless.

Making the same assumptions for the complete response as we did for the unit step response, the following equations are obtained (letting $t_{pd}=t$).

Region I: Ramp Input

$$V_c(t) = \left(\frac{t}{T_o} + \frac{1}{T_o}(e^{-t} - 1)\right) V_o$$

$$(0.5)\, T_o + 1 = t + e^{-t} \qquad 0<t<T_o \tag{9}$$

Region II: Unit Step Input

$$V_c(t) = 1 - e^{-t} + V_c(0)\, e^{-t}$$

where $V_c(0) = V_c$ of Region I, when $t = T_o$.

$$V_c(0) = \frac{T_o}{T_o} + \frac{1}{T_o}(e^{-T_o} - 1)$$

$$= 1 + \frac{1}{T_o}(e^{-T_o} - 1)$$

$$V_c(t) = 1 - e^{-t} + \left[1 + \frac{1}{T_o}(e^{-T_o} - 1\right] e^{-t}$$

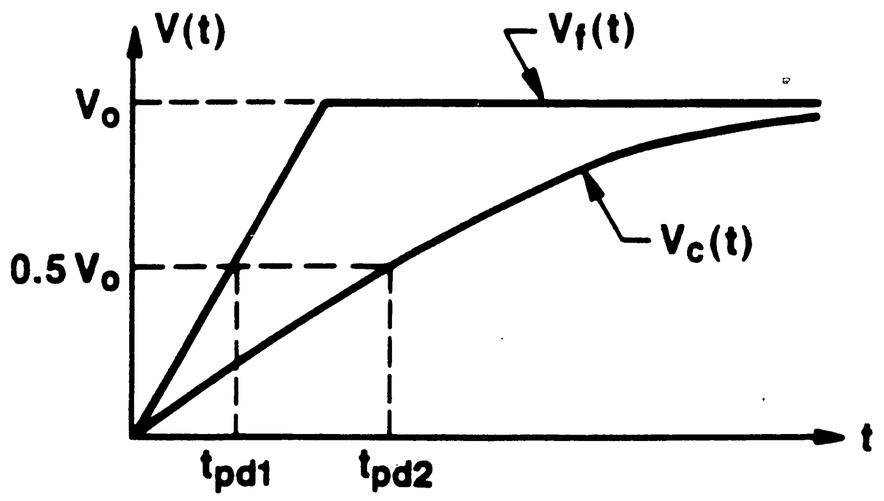
$$= 1 - e^{-t} + e^{-t} + \frac{1}{T_o}(e^{-T_o} - 1)\, e^{-t}$$

$$\frac{(0.5-1)T_o}{(e^{-T_o} - 1)} = e^{-t} \qquad t > T_o \qquad (10)$$

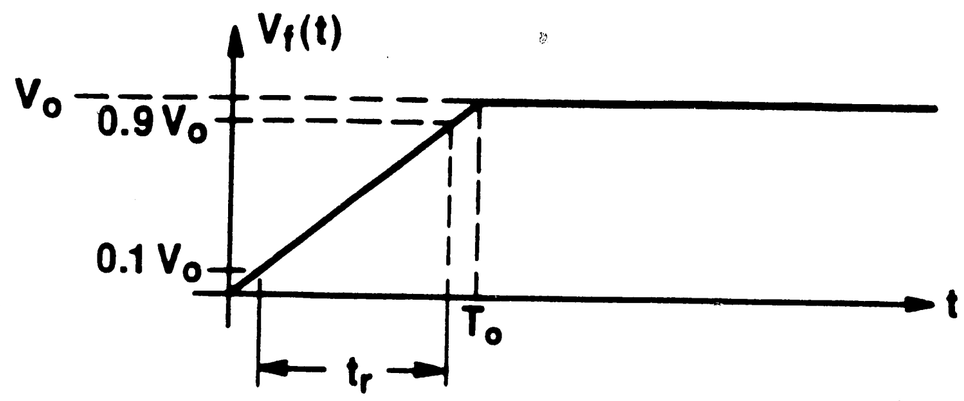
In order to find the propagation delay (t_{pd}), it must be determined at what time the output voltage reaches the threshold voltage of $0.5V_o$. If this point is less than T_o then equation (9) should be used, otherwise use equation (10). To solve equation (9) for t_{pd}, an iteration technique must be used (i.e., Newton-Raphson Algorithm).[2]

It must be noted at this point that the desired propagation delay is the difference between the forcing function (t_{pd1}) and the complete response (t_{pd2}) shown below, and the value K_o is found:

$$t_{pd} = t_{pd2} - t_{pd1} = \frac{1}{K_o}$$



The T_o value comes from the rise time of the forcing function. In real measurements the rise time is defined as the time between the 10% and 90% value of the waveform. The diagram below shows this definition graphically.



The equation of the ramp is:

$$V(t) = \frac{V_o}{T_o}\, t \tag{11}$$

In terms of the rise time (t_r):

$$\Delta V = \frac{V_o}{T_o}\, \Delta t$$

$$T_o = V_o \frac{\Delta t}{\Delta V} = V_o \frac{t_2 - t_1}{V_2 - V_1}$$

$$T_o = V_o \frac{t_r}{V_o(0.9 - 0.1)}$$

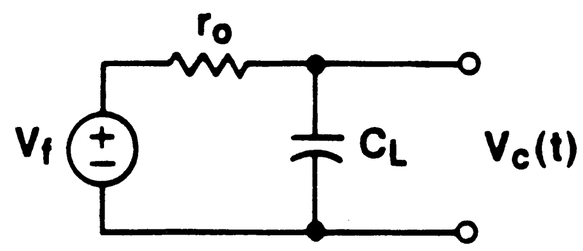
$$T_o = \frac{t_r}{0.8} \tag{12}$$

A short computer program was written to find the proportionality constant for various values of rise time using equations (8), (9), (10), (11) and (12). These values are shown in Table 1.

F. RC Network Summary

Several generalizations can be made about the preceding analysis.

1. The additional propagation delay due to the interaction of the DUT's output resistance and the ideal load can be modeled using a series RC circuit.



The equation for the output $V_c(t)$ depends on the forcing function $V_f(t)$.

2. This model requires an accurate value for the dynamic resistance (r_o). This resistance is obtained from two measurements of the DUT.

   a. The output rise time (t_r) of the unloaded DUT, used to find K_o.

   b. The change in propagation delay (Δt_{pd}) due to a change in load capacitance (ΔC_L), used to find r_o.

$$r_o = K_o \left(\frac{\Delta t_{pd}}{\Delta C_L} \right)$$

3. The calculation of K_o is difficult using the formulas obtained from the complete response to a ramp input. A method to implement this in a test program would be to create a table of K_o values for various t_r (similar to Table 1) and interpolate for values in-between.

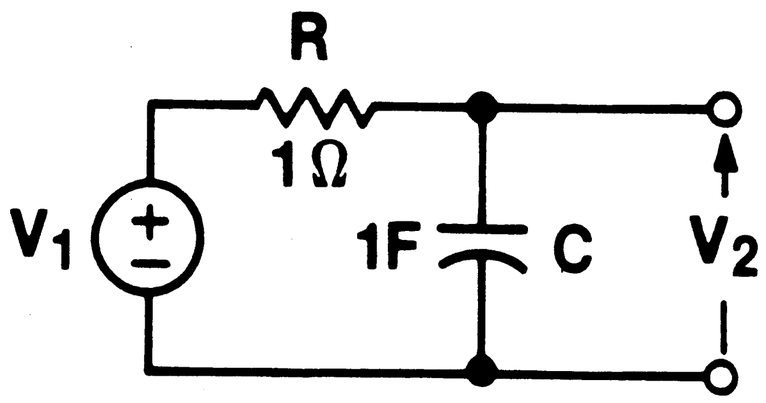
4. For long rise times of the DUT, the r_o formula simplifies to the following:

$$r_o = \frac{\Delta t_{pd}}{\Delta C_L}$$

Using the above equation for $t_r > 5$ RC would result in an error of less than 1%.

5. The desired propagation delay is the difference between the time delay of the input signal (t_{pd1}) and the output waveform (t_{pd2}) at the threshold voltage. To find this solution mathematically, one would have to find t_{pd1} using the ramp equation (11) and then solve equation (9) or (10) for the appropriate t_{pd2} value.

An alternate solution is to use a SPICE simulation. This was done to verify the equations and to examine the output waveforms. The RC circuit shown below was used for this simulation.

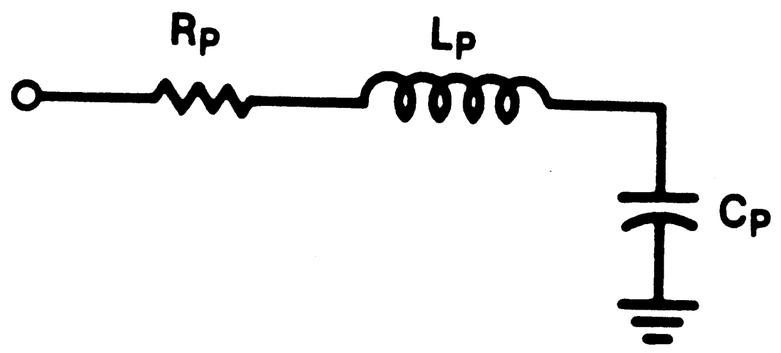


Figures 8 and 9 show the input and output response for input rise times of 0.1 and 15, respectively. Note that for long rise times (i.e., 15, shown in Figure 9) the output "follows" the input and the propagation delay is R x C = 1 second.

6. ATE LOADING

Figure 4 shows a complicated model of the ATE circuitry. It is desired to simplify this circuit, but a simplified model for the PEC of the ATE is difficult to obtain. Three possible methods are: 1) Obtain a high frequency model of the input characteristics of the PEC. High frequency test equipment could be used to obtain S-parameter data which would lead to an electrical equivalent circuit.[3] 2) The ATE manufacturers may be a source, since they may have performed detailed analysis of their own PEC.[4] 3) Empirical techniques may be used that model a close approximation of the PEC. This model could be modified after accumulation of test data and modeling on SPICE.

The sketch below shows a reasonable approximation for the PEC model.[3,4] The fundamental elements one would expect to find are: series resistance (i.e., contact resistance), wiring inductance and parasitic capacitance.



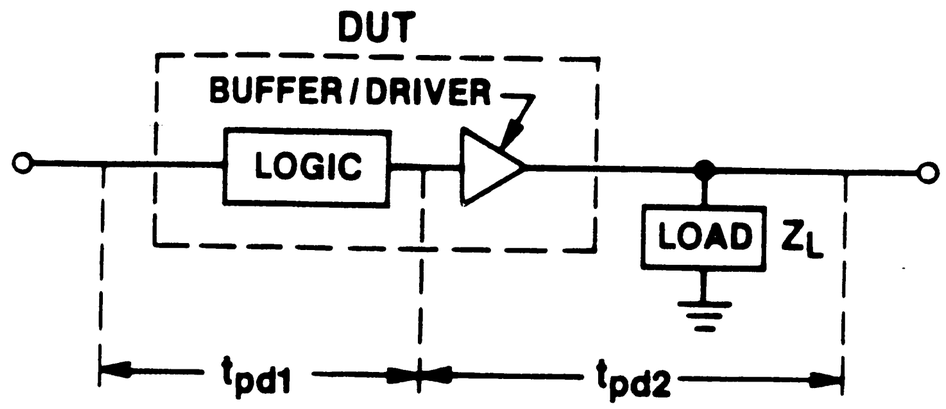
This will be my proposed equivalent circuit for the ATE PEC.

7. APPLYING CORRELATION FACTORS

The propagation delay measurement has been described and sources of errors have

been discussed in general terms. Now let's look at how a correlation factor may be applied to the actual measurements of the propagation delay.

Shown below is a block diagram of a typical logic device. It includes a logic block which represents the logic function of the gate and an output Buffer/Driver section.



The total propagation delay (t_{pd}) is the sum of a fixed delay due to the logic circuit (t_{pd1}) and the interaction of the Buffer/Driver output resistance (r_o) with the output load impedance (Z_L).

$$t_{pd} = t_{pd1} + t_{pd2}$$

The output propagation delay (t_{pd2}) can be further subdivided into the inherent delay of the Buffer/Driver circuit (t_{pd2a}), the effects of the data sheet load (t_{pd2b}) and the parasitic load (t_{pd2c}). Therefore,

$$t_{pd2} = t_{pd2a} + t_{pd2b} + t_{pd2c}$$

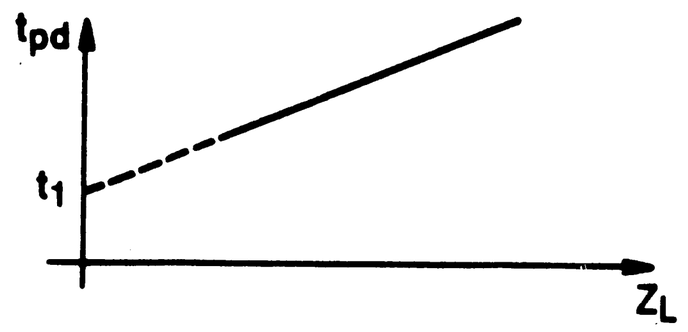
For a no load condition, only the Buffer/Driver circuit delay would be present.

$$t_{pd2} = t_{pd2a} \qquad \begin{matrix}\text{Limit } (t_{pd2}) \\ Z_L \rightarrow 0\end{matrix}$$

For the condition of large parasitic elements:

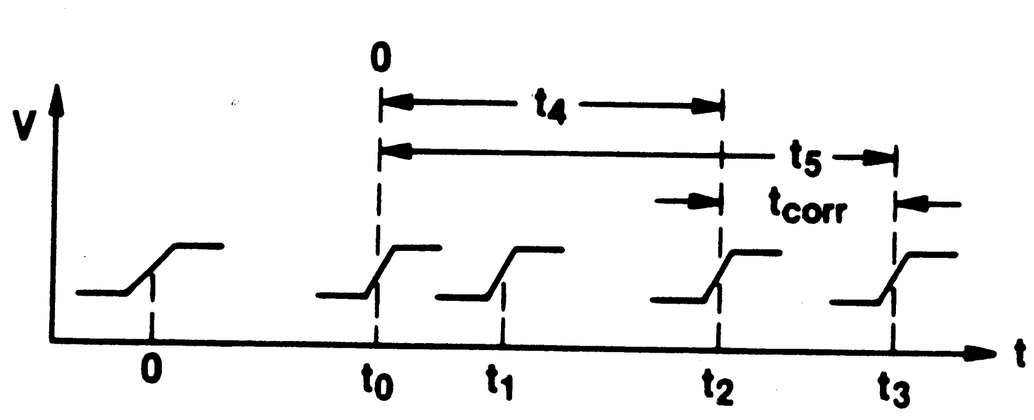
$$t_{pd2} \cong t_{pd2c} \qquad \begin{array}{l}\text{Limit } (t_{pd2}) \\ Z_L \rightarrow \text{ large}\end{array}$$

The figure below shows a graphical representation of this, where t_1 is the propagation delay of the logic gate and the unloaded output Buffer/Driver circuit.



Output Load (Z_L)

The effect can also be shown using a timing diagram.



Where,

0 = Signal applied to the DUT input
t_o = Logic delay time
t_1 = Logic delay + Buffer/Driver (unloaded)
t_2 = Logic delay + Buffer/Driver + Ideal load
t_3 = Logic delay + Buffer/Driver + Ideal load + Parasitic load

t_2 = Ideal propagation delay obtained from beach measurements
t_3 = Propagation delay obtained from the ATE measurements

The correlation factor (t_{corr}) is:

$$t_{corr} = t_3 - t_2$$

This is the correlation factor that could be obtained by modeling the entire DUT and PEC circuitry.

Another way to obtain the correlation factor is to model only the output Buffer/Driver circuit and the equivalent input impedance of the PEC. Time would start at the t_o point and the correlation factor is shown below.

$$t_{corr} = t_5 - t_4$$

The above correlation factor would be the simplest approach to use since it has the least amount of circuitry to model. Another advantage is that the equivalent circuit of the entire logic gate sometimes is not available, but the output circuitry and its characteristics usually are.

8. EXPERIMENTAL DATA

This section will present propagation delay measurements, which include bench and ATE measurements and a SPICE simulation. The purpose is to show the magnitude of

0 = Signal applied to the DUT input
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8. EXPERIMENTAL DATA

This section will present propagation delay measurements, which include bench and ATE measurements and a SPICE simulation. The purpose is to show the magnitude of

the problem and verify that the correct models are used for the DUT and PEC. The following steps were taken in the experiment.

1. Select a device.

2. Measure the device on the bench and two ATE systems.

3. Define the characteristics of each test method (i.e., input rise time, fall time, period, etc.).

4. Simulate, using Spice, the total DUT model with the ideal load and compare it with the bench measurements. This will verify that the correct DUT model is being used.

5. Simulate (SPICE) the simplified models with:

   a. Bench Model - RC circuit

   b. PEC Model - RLC circuit

   This will use the model of the DUT output circuit and require the measured value of the output resistance (r_o).

A. Device Selection

The 74LS27 was chosen for the experiment. This is a triple 3-input positive NOR gate. Figure 10 shows the device's pin configuration and logic diagram connections. It also shows the biasing that was applied during the bench and ATE measurements of the propagation delay. The equivalent circuit schematic of one gate is shown in Figure 11.[5] This circuit, with slight modifications, was used for SPICE simulations.

B. Bench and ATE Measurements

Propagation delay measurements of six 74LS27 devices were taken on a bench fixture and two ATEs (ATE-A, ATE-B). The results of the measurements are shown in Table 2. The propagation delay was then plotted for each device and is shown in Figure 12. It shows that for each test method, the data "tracks" the relative magnitude of the devices' propagation delay, but the absolute measurement remains in error. The propagation delay errors represent the percent difference between the bench measurement and the ATE raw data. They range from an error of 11% to 50% and are due to a combination of factors that will be discussed in the next section.

C. Test Characteristics

As mentioned in the introduction, the propagation delay is influenced by a number of factors (i.e., t_r, t_f, V_{IL}, V_{IH}, I_{OL}, etc.), most of which are controlled by the ATE. Table 3 shows the measured characteristics of each of the test methods used. Of all these factors, it was found through device measurements, that the most significant effects on propagation delay were due to the input rise and fall time and the DUT load circuit.

The simplified DUT load circuits are shown in Figure 13. The bench measurements used the load specified by the manufacturer (Figure 1: $R_L = 2k$, $C_L = 15$ pF). The ATE models are generally given as a lumped capacitance (C_P). The load of ATE-A consists of the diode network and the parasitic capacitance of the ATE. This capacitance was estimated to be 50 pF by test set engineers.[6] The DUT load circuit of ATE-B

consisted of the parasitic capacitance of the ATE and an active load (I_{OL} = 8 mA, I_{OH} = 0.4 mA). This capacitance was estimated to be in the range of 40 to 60 pF by the test set manufacturer.

D. SPICE Simulation

A circuit simulation was performed using the circuit of Figure 11 and the ideal (bench) load circuit (Figure 1(a)). Table 4 shows the results from SPICE and uses an average value of the six measured devices as comparison.

This method proved to be least desirable, since characteristics which are specific to each device are difficult to model and a different model would be needed for every device. Typical or average measurements were used for comparison purposes, because only a single value was obtained from the SPICE simulation.

Two other simulations of the DUT/PEC interface were done using the simplified RC model and the RLC circuit model (L = 15nH).[3] Using the characteristics of each test method (Table 3), no significant propagation delay differences were found between the two models. As a result, the RC model was used for correlation factor calculation.

E. Retest

The six devices were then retested varying the load capacitance. The bench test also varied the input rise time. The data for device #1 are shown on Tables 5, 6 and 7 for the bench, ATE-A and ATE-B respectively. A linear regression technique was used to obtain a slope and intercept of the data. The straight line correlation of the data was very good, with better than 99% correlation in all cases. This data was then plot-

ted for all the devices and, as an example, the data for device #1 is plotted in Figure 14. Each device plot showed several interesting characteristics:

1) The slope of the lines represents the value of r_o directly, since the unloaded output rise time (Table 5(b)) is greater than 15ns and therefore $K_o = 1$ (Table 1).

2) The slope of the ATE-A data is significantly different from that of the bench or ATE-B. This was unexpected, since r_o is a characteristic of the device and should be constant.

3) Three distinctly different intercept points were obtained for each device tested. The intercept point (t_1) was discussed in Section 5 and is the propagation delay with no external capacitance (C_L=0). It represents the inherent propagation delay of the logic gate and should be constant for each device under these test conditions.

9. DISCUSSION

The results show that each test method yields different slopes and intercept points. Under ideal conditions the ATE data would overlay the bench data. I propose that a reason for these differences is because the ATE data has undergone two shifts: one, due to series resistance and another due to parallel capacitance.

Figure 15(a) shows the circuit model of the PEC. The ATE has introduced two additional components to the simple RC circuit model: a series resistance (R_s) and a parallel capacitance (C_p).

The effects of these two components are shown separately in Figures 15(b) and 15(c).

The slope of the line increases as R_s increases, and as C_p increases the line is shifted up but remains parallel with the original line.

A. ATE-A

Figure 16 shows the explanation of the data obtained from ATE-A with both R_s and C_p present. First, the slope is increased by R_s then the entire line is moved up by C_p. The point t_3 represents the ATE propagation delay obtained under normal conditions (no external capacitance added, $C_L + 0$). The point t_1' represents the point where C_p is zero (the inherent propagation delay of the DUT). Working backwards, the value of C_p can be determined from the straight line equation of the ATE-A data and the intersection of t_1 (obtained from the bench test). The value of R_s can be obtained by subtracting the slopes of the ATE-A data and bench data.

The correlation factor is obtained by subtracting t_2 from t_3. The point t_2 is the propagation delay with the value of capacitance specified by the data sheet (C(spec.)). Since it is undesirable to measure all the devices on the bench, t_2 is unknown. But this point can be calculated once C_p and R_s are determined using the following equations.

$$
\begin{aligned}
t_{corr} &= t_3 - t_2 \\
t_3 &= R_{out} \times C_{out} = (R_A) \times (Cp) \\
t_2 &= R_{out} \times C(spec) = r_o \times C(spec) \\
&= (R_A - R_S) \times C(Spec) \\
t_{corr} &= R_A \times C_p - (R_A - R_S) \times C(spec)
\end{aligned}
$$

B. Sample Calculation

The following procedure was used to find the correlation factor for device #1, which was tested on ATE-A.

Given:	C (spec)	=	15pF
	t_r (input)	=	5ns (Table 3)
	t_r (output, unloaded)	=	21.8ns (Table 5)
Therefore:	K_o	=	1.0 (Table 1)
Measurements:	C_p	=	11.97pF (Table 6)
	R_A	=	133.4 Ω (Table 6)
	r_o	=	62 Ω (Table 5)
	R_s	=	71.4 Ω
Formula:	t_{corr}	=	$R_A \times C_p - (R_A - R_s) \times C(spec)$
		=	$133.4 \times 11.97pF - (133.4 - 71.4) \times 15pF$
	t_{corr}	=	0.667ns

The corrected propagation delay (t'_{PLH}) is the ATE measured value minus t_{corr}.

$$t'_{PLH} = t_{PLH}(ATE) - t_{corr}$$

$$t'_{PLH} = 9.38ns - 0.667ns = 8.71ns$$

This value has an error of only -0.50% from the bench data.

10. CORRELATION FACTORS APPLIED

The above calculation was performed on the rest of the devices for both ATE-A and ATE-B. Table 8 shows the correlation factors for each device and the percent error of the uncorrected and corrected data. The error has decreased from a maximum of 50.3% to 1.78%.

A. Final Note

It was found that the first calculation of the correlation data was much worse than the results shown on Table 8. This was due to the results of the linear regression technique used on the test data (Tables 5, 6 and 7). Correlation factors were significantly improved if only data points near C(spec) and the origin were used. This was done for several reasons:

1. The bench data showed that $t_{PLH}(C_L)$ decreased with decreasing C_L, where $t_{PLH}(8pF)$ was the last measured point. It was expected that the $t_{PLH}(0)$ point would be less than the $t_{PLH}(8pF)$ point, but the straight line equation (using all the data points) predicted $t_{PLH}(0)$ was greater than $t_{PLH}(8pF)$.

2. The r_o values were inconsistent with the test data. The propagation delay of device #3 increased above the other devices (Figure 12). This suggests that r_o for device #3 should be greater than the rest, but the result was lower when all the data points were used.

3. There were inconsistent values for Cp. This value varied widely using all the data points, while it was expected to be constant (a characteristic of the test set).

4. SPICE simulation did not agree with the data points.

As a result, fewer points were used in the linear regression calculation. It was kept to 3 or 4 points near the origin and the data sheet load of 15pF. This error can be corrected in future measurements by using small values of capacitance.

11. CONCLUSIONS

This report presents a method which results in improved propagation delay accuracy. It uses a simple RC network representation of the test environment, it is based on device characteristics, and can be implemented using ATE software.

As the project progressed, less emphasis was placed on the computer aided design (SPICE). Although it provided a helpful guide and verification tool in the circuit analysis, it proved to be less desirable in obtaining correlation factors for several reasons;

1. It is external to the ATE environment.
2. Detailed device parameters would have to be obtained for more accurate results.
3. Complete circuit diagrams of the DUT are usually not available.

There is definitely a need for additional study in this area. This report only discussed the t_{PLH} measurement, but the theory can easily be applied to all timing measurements. It can also be used for other device technologies (i.e., CMOS, HCT, ALS, etc.) having the totem pole output structure.

This correlation method has not yet been implemented using ATE software, but a program has been written to calculate correlation factors. It uses BASIC programming language and takes input data from device measurements (t_r, V_{OH}, V_{OL}, V_{th}, etc.) and calculates K_o, r_o and t_{corr}.

A model of the DUT output is obtained from these measurements and calculations. Using this model and applying the manufacturer's specified load (or simplified equivalent) the first time delay is obtained (t_4, Section 7). The ATE model is applied to the DUT model and another time delay is obtained (t_5, Section 7). The difference between these two times is the correlation factor (t_{corr}) and when applied to the actual ATE measurement, the measurement error is improved from 50% to less than 2%.

Figure 17 shows an equivalent circuit model that is used to represent the ATE load. The values shown are an average of the six devices. The models could be improved even further by measuring a larger sample of devices. The "negative resistance" of the ATE-B model is due to test set resolution and accuracy. It would probably reduce to zero by testing a larger sample size.

The following are comments which are a result of this experiment.

1. Modeling of complex circuitry is not necessary to obtain good correlation factors.

2. Test set and DUT boards vary, therefore a good model of the PEC for each test set is essential.

3. To obtain good correlation factors the test system must have good measurement repeatability.

4. A good test set calibration is important. A software calibration is better than a hardware one.

5. A test system that averages many measurements is better than a single measurement.

6. Golden Units may be used to monitor shifts in the test set measurement system, but a set of Golden Units for each device function and package type is not required.

7. Active loads of the ATE have a significant effect on propagation delay.

8. The values of R_A and C_p are significantly effected by test set resolution. For example: ATE-B has a resolution of 0.5ns. A change of 0.5ns in the first data point resulted in a change of R_A by 7 Ω and C_p by 33pF, which may have caused the negative resistance mentioned above.

Proportionality Constant, K_o, for Values of DUT Output Rise Time

Rise Time, t_r (Sec)	T_o (Sec)	K_o (---)
0.0	0.0	1.4427
0.1	0.125	1.4413
0.2	0.25	1.4373
0.3	0.375	1.4306
0.4	0.5	1.4214
0.5	0.625	1.4097
0.6	0.75	1.3957
0.7	0.875	1.3796
0.8	1	1.3615
0.9	1.125	1.3417
1	1.25	1.3203
2	2.5	1.1348
3	3.75	1.0638
4	5	1.0323
5	6.25	1.0167
6	7.5	1.0089
7	8.75	1.0047
8	10	1.0025
9	11.25	1.0014
10	12.5	1.0008
20	25	1.0000

Table 1

Propagation Delay Errors

(a) t_{PLH} (ns) (Pin 13 to 12)

Device #	Bench	ATE-A	ATE-B	Error (%) ATE-A	Error (%) ATE-B
1	9.38	11.25	14.0	19.9	49.3
2	8.98	10.47	13.0	16.6	44.8
3	10.74	12.81	16.0	19.3	49.0
4	8.98	10.00	13.5	11.4	50.3
5	8.98	10.31	13.5	14.8	50.3
6	8.98	10.15	13.5	13.0	50.3

(b) t_{PHL} (ns) (Pin 13 to 12)

Device #	Bench	ATE-A	ATE-B	Error (%) ATE-A	Error (%) ATE-B
1	7.13	9.06	9.0	27.1	26.2
2	6.48	8.44	8.5	30.3	31.2
3	7.47	9.84	9.5	31.7	27.2
4	6.25	7.97	8.5	27.5	36.0
5	6.25	7.97	8.5	27.5	36.0
6	6.25	7.97	8.5	27.5	36.0

Table 2

Test Method Characteristics

Input Characteristics

	Bench	ATE−A	ATE−B
Period	1 μs	2 μs	1 ms
Pulse Width	500ns	1 μs	1.84 μs
Rise time	6ns	5ns	8.2ns
Fall time	6ns	5ns	10ns
V_{IL}	0.8 V	0 V	0 V
V_{IH}	3 V	3 V	3 V
V_{th}	1.3 V	1.3 V	1.3 V

Other Characteristics

	Bench	ATE−A	ATE−B
I_{OH}	-	-	0.4 mA
I_{OL}	-	-	8 mA
R_L	2 kΩ	2 kΩ	-
C_L	15 pF	50 pF*	40 - 60 pF*

* See Text

Table 3

SPICE Simulation Results

Parameter	Average DUT Measurements	SPICE	Error
t_{PLH}	9.34ns	10.0	7%
t_{PHL}	6.64ns	7.0	5.4%
t_r	23.3ns	22.2	---
t_f	4.4ns	7.0	---

Table 4

Bench Test Data for Device #1

(a) Effects of Load Capacitance on Propagation Delay

C_L (pF)	t_{PLH} (ns)	t_{PHL} (ns)	t_r (ns)	t_f (ns)
8	8.98	5.78	22.85	3.60
15	9.38	7.13	23.12	4.65
65	12.50	13.28	18.79	11.04
115	14.45	19.14	24.82	17.59
165	16.80	22.85	27.84	21.94
215	18.17	27.15	35.00	26.93

(b) Effects of Rise and Fall Time on Propagation Delay

C_L (pF)	$t_r = t_f$ (Input, ns)	t_{PLH} (ns)	t_{PHL} (ns)	t_r (Output, ns)	t_f (Output, ns)
8	1	8.50	6.09	20.38	3.74
8	15	11.13	5.37	23.05	4.01

(c) Linear Regression of t_{PLH} Data: (Improved)*

Data Correlation	:	99.28%	(99.99%)
Slope (r_o)	:	45.30 Ω	(61.99 Ω)
Intercept (t_1)	:	8.98ns	(8.47ns)
C (0)	:	-198.18 pF	(-136.6 pF)
C (t_1)	:	0 pF	(0 pF)

* See Text.

Table 4

ATE-A Test Data for Device #1

(a) Test Data:

C_L (pF)	t_{PLH} (ns)
0.0	10.00
15.26	12.19
57.1	17.66
99.6	23.28
154.0	29.37
222.0	38.28

(b) Linear Regression of t_{PLH} Data: (Improved)*

Data Correlation	:	99.96%	(99.98%)
Slope (r_o)	:	126.22 Ω	(133.43 Ω)
Intercept (t_1)	:	10.27ns	(10.07ns)
C (0)	:	-81.37 pF	(-75.44 pF)
C (t_1, bench)	:	-10.24 pF	(-11.97 pF)

* See Text.

Table 6

ATE-B Test Data for Device #1

(a) Test Data:

C_L (pF)	t_{PLH} (ns)
0.0	14.0
15.26	14.5
57.1	16.0
99.6	18.0
154	21.0
222	22.5

(b) Linear Regression of t_{PLH} Data: (Improved)*

Data Correlation	:	99.23%	(99.70%)
Slope (r_o)	:	40.58 Ω	(39.99 Ω)
Intercept (t_1)	:	13.96ns	(13.91ns)
C (0)	:	-343.98 pF	(-347.7 pF)
C (t_1, bench)	:	-122.76 pF	(-135.96 pF)

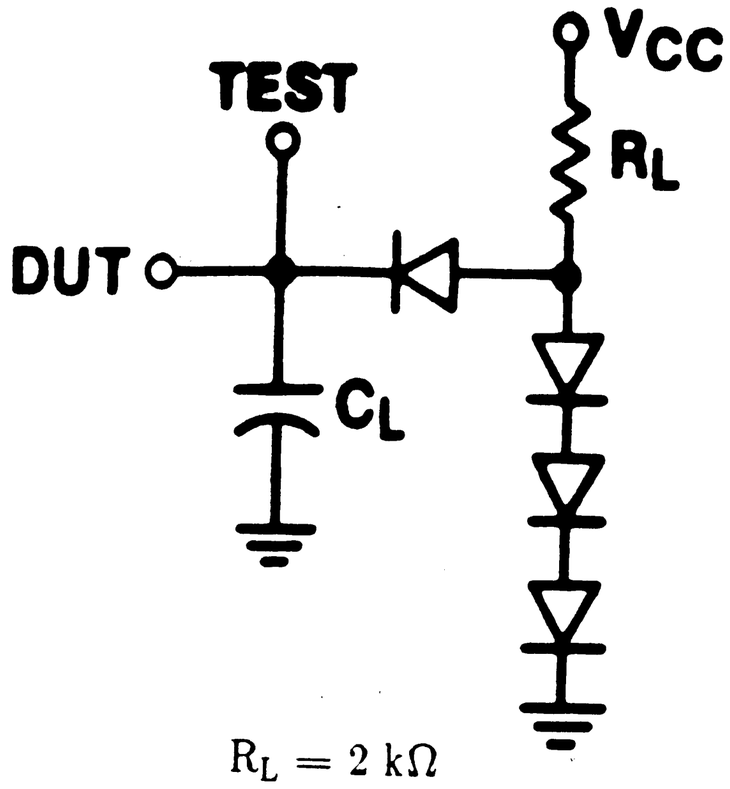
* See Text.

Table 7

Propagation Delay Errors With and Without Correlation Factors

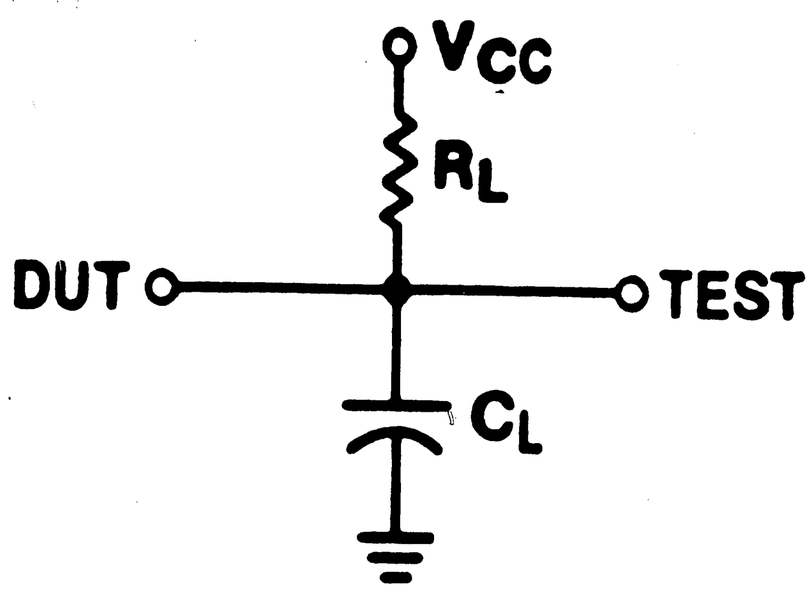
Device #	% Error Uncorrected ATE-A	% Error Uncorrected ATE-B	t_{corr} (ns) ATE-A	t_{corr} (ns) ATE-B	% Error Corrected ATE-A	% Error Corrected ATE-B
1	19.9	49.3	0.667	4.51	-0.50	1.17
2	16.6	44.8	0.327	4.58	-0.97	-0.67
3	19.3	49.0	0.825	5.31	1.44	-0.47
4	11.4	50.3	0.240	4.18	1.67	-1.78
5	14.8	50.3	0.397	4.46	1.70	0.67
6	13.0	50.3	0.289	4.51	1.12	0.11

Table 8



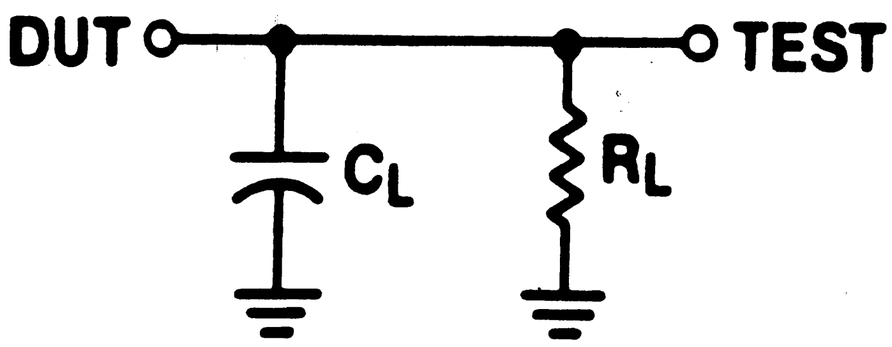
$R_L = 2\ k\Omega$
$C_L = 15\ pF$

(a) Standard LSTTL Load



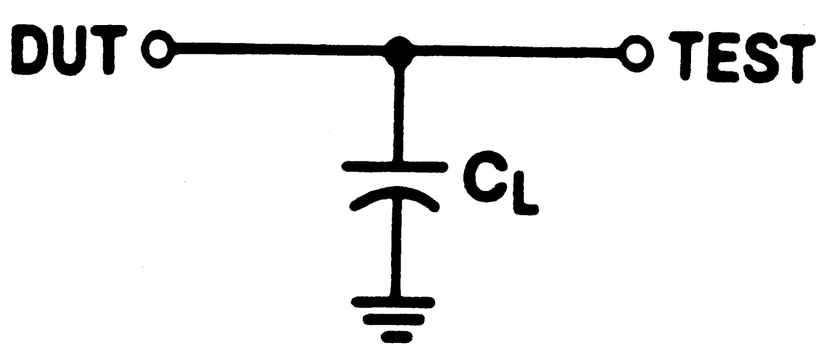
$R_L = 2\ k\Omega$
$C_L = 15\ pF$

(b) Optional LSTTL Load



$R_L = 500\Omega$
$C_L = 50\ pF$

(c) Standard ASTTL Load

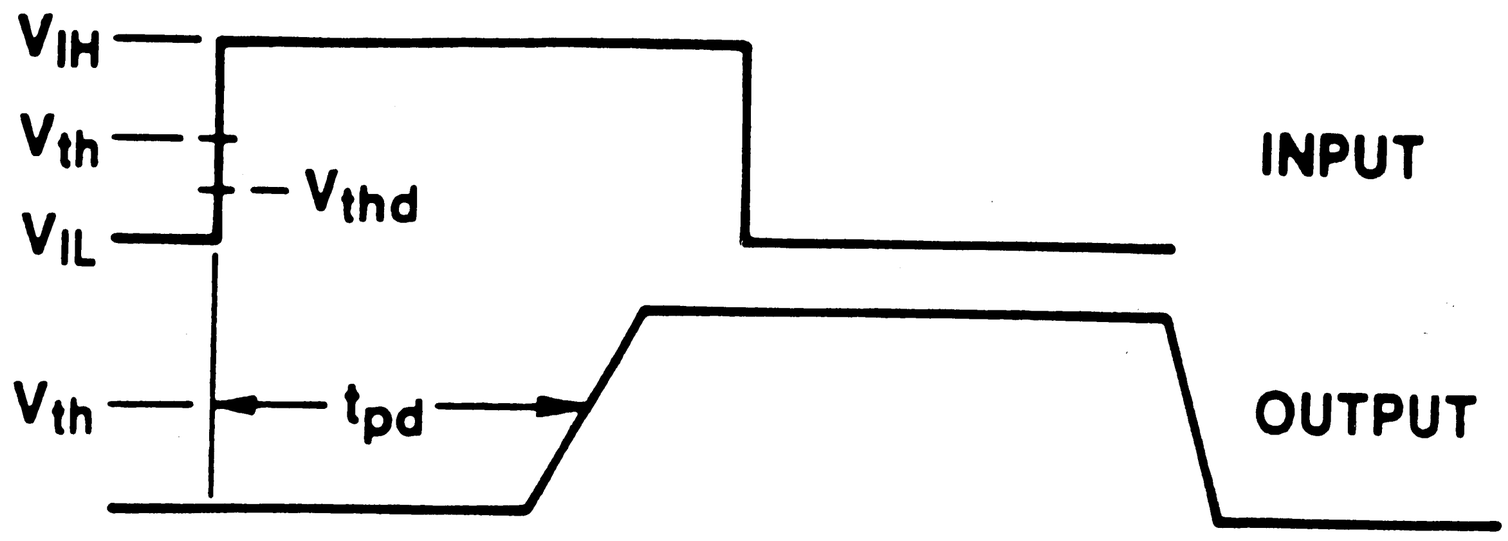


$C_L = 50\ pF$

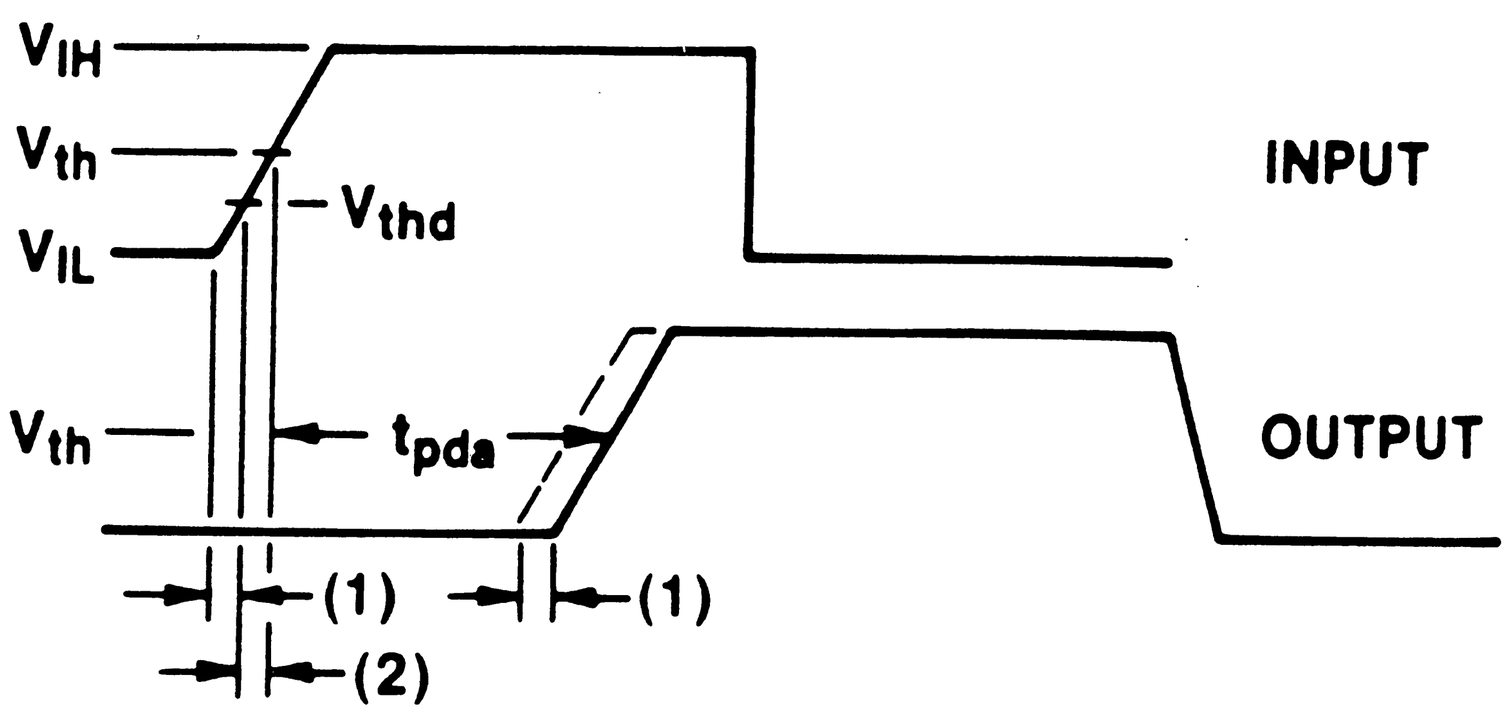
(d) Standard HC and HCT Load

Manufacturer's Specified Loading for Propagation Delay Measurements

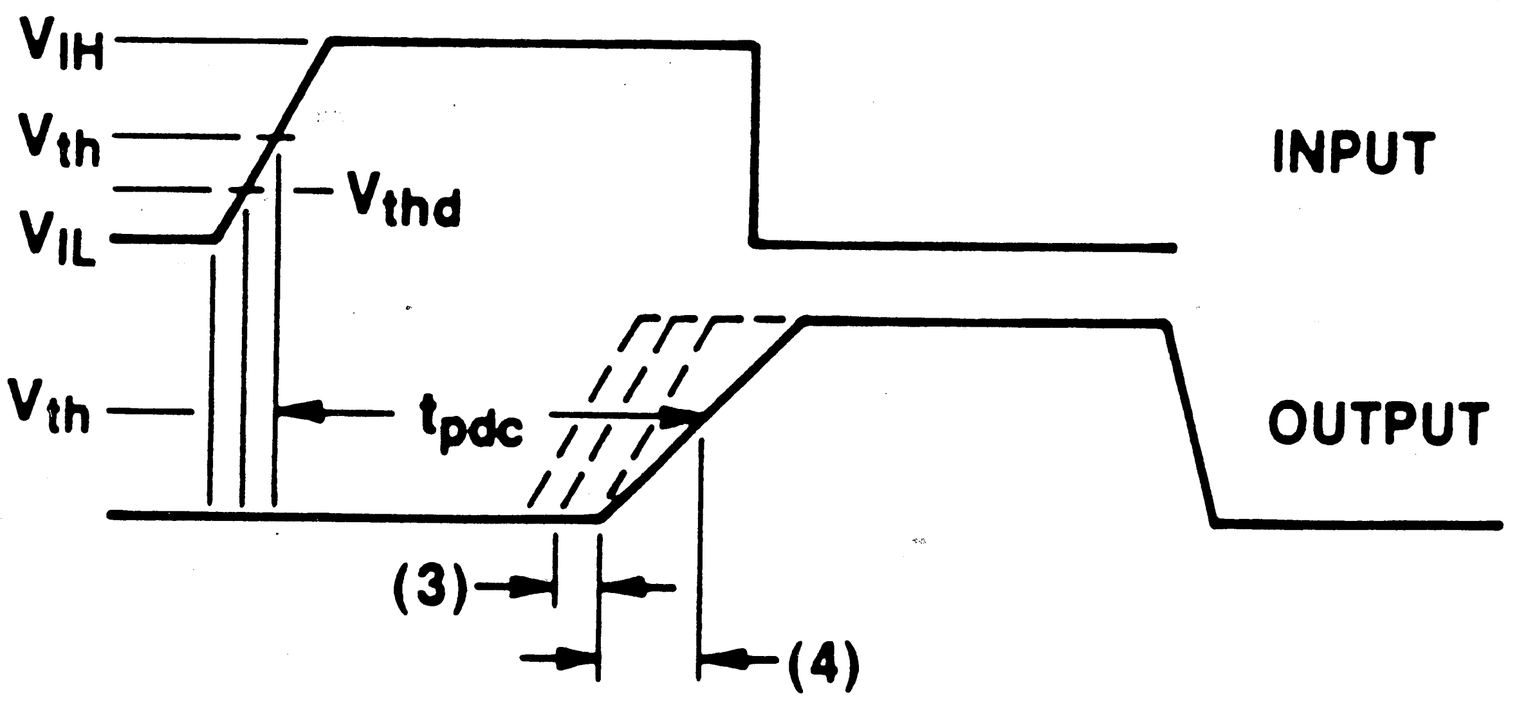
Figure 1



(a)



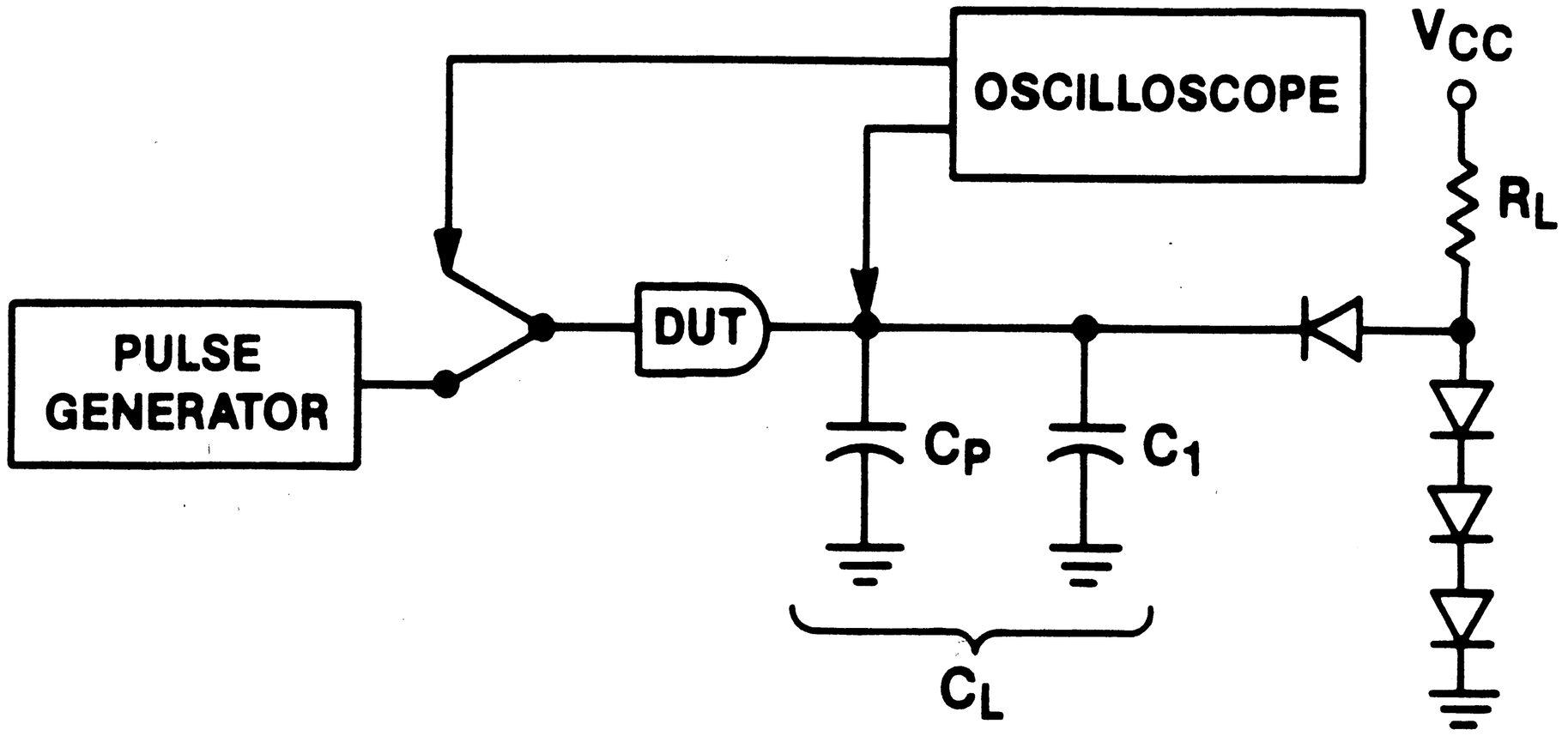
(b)



(c)

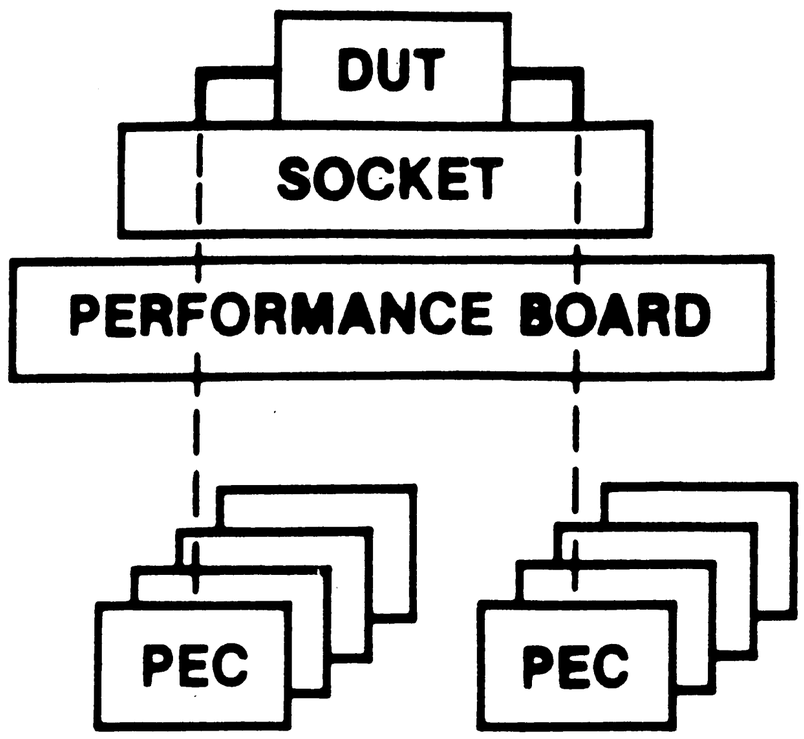
Propagation Delay Measurements

Figure 2



Bench Fixture for Testing LSTTL Devices

Figure 3

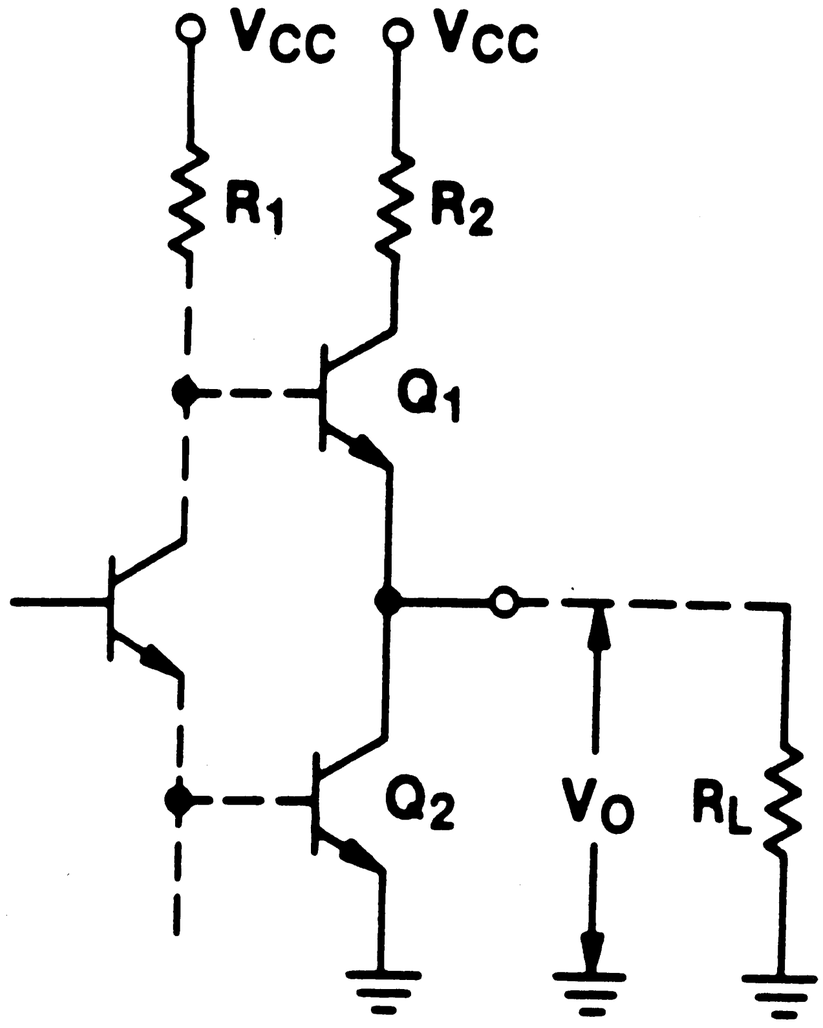


(a) Block Diagram of
ATE Test Head

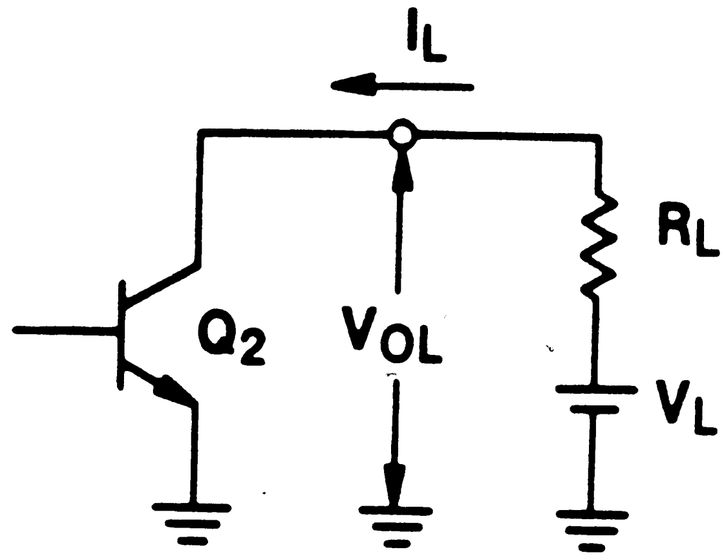
(b) Electrical Model of
ATE Test Head

Block Diagram and
Electrical Model of the ATE

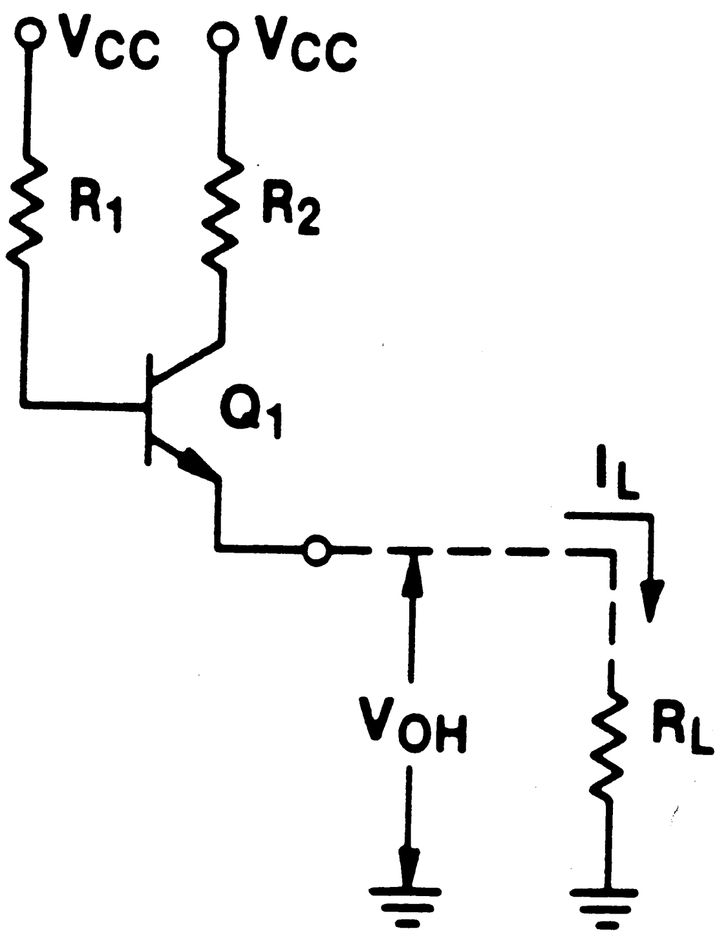
Figure 4



(a) Totem Pole Output



(b) Output Low-State

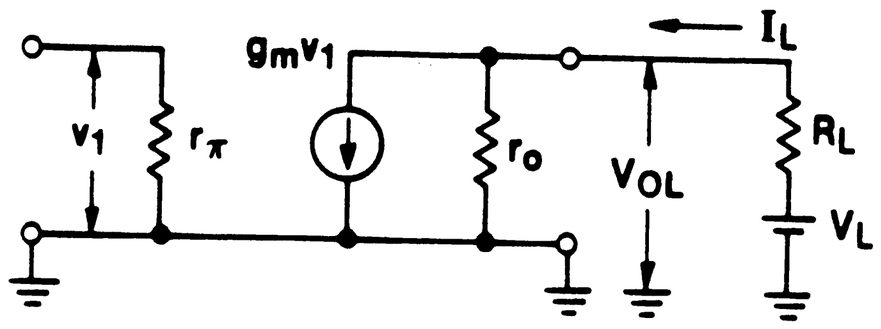


(c) Output High-State

TTL Output Buffer/Driver Circuit

Figure 5

(a) Output Low State (V_{OL} = Output Voltage Low-State)

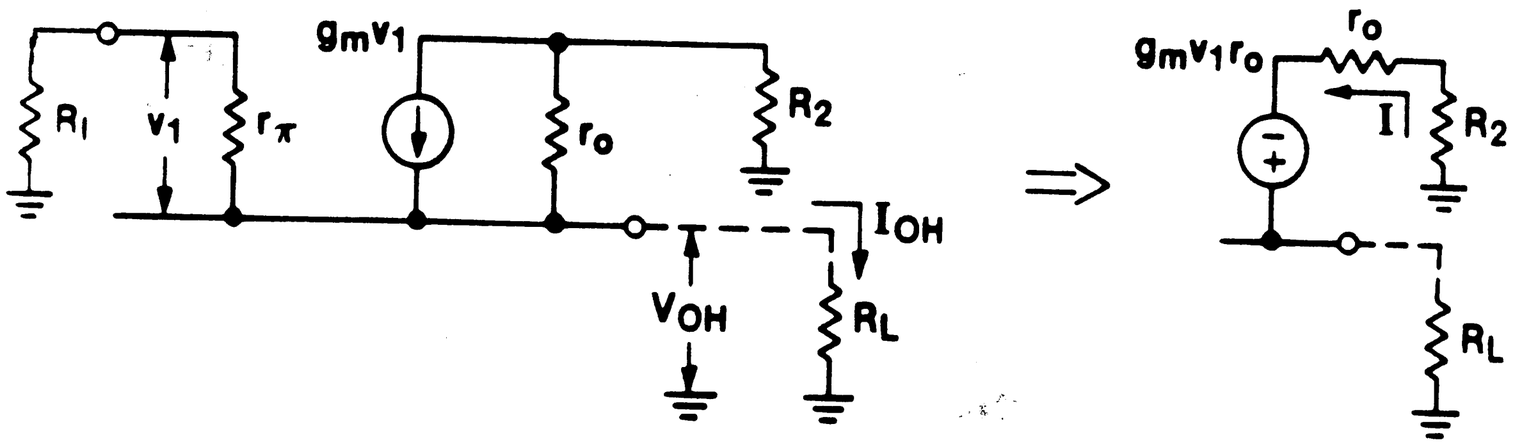


$$R_{th} = r_o$$

$$V_{th} = r_o I_L - r_o g_m v_1$$

$$V_{th} = V_{OL} = r_o (I_L - g_m v_1)$$

(b) Output High State (V_{OH} = Output Voltage High-State)

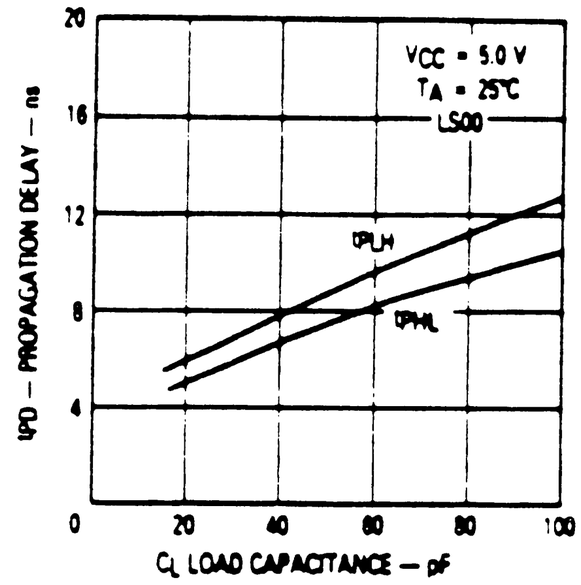


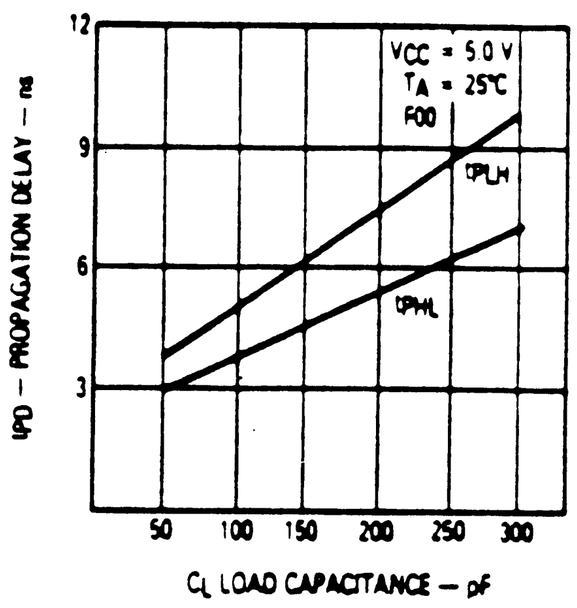
$$R_{th} = (r_\pi + R_1) \,||\, (r_o + R_2)$$

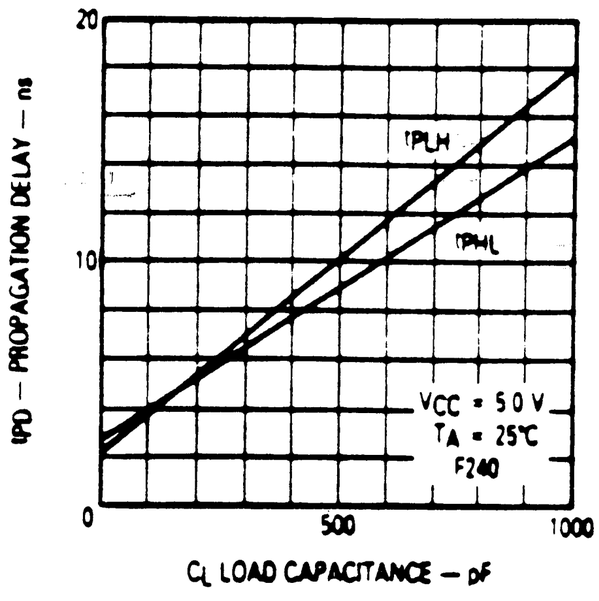
$$V_{th} = g_m v_i r_o - (r_o + R_2)I + V_{CC}$$

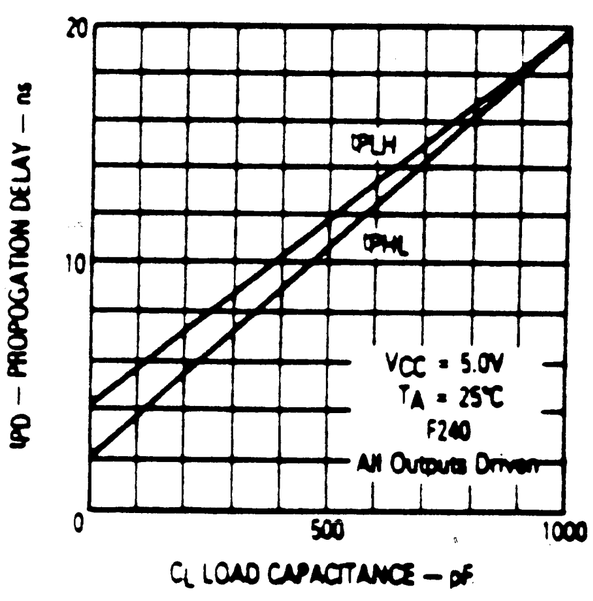
Equivalent Output Models

Figure 6



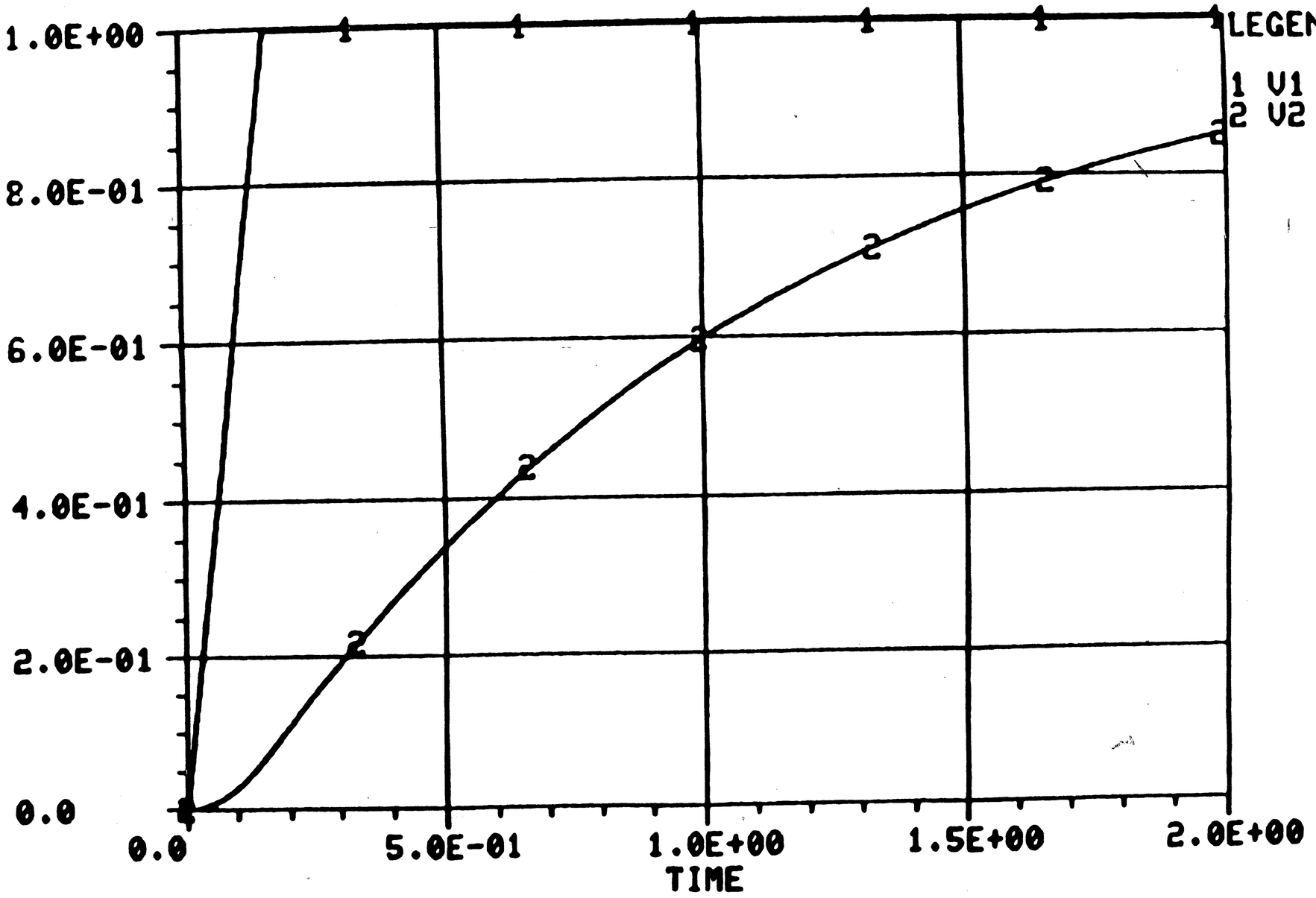






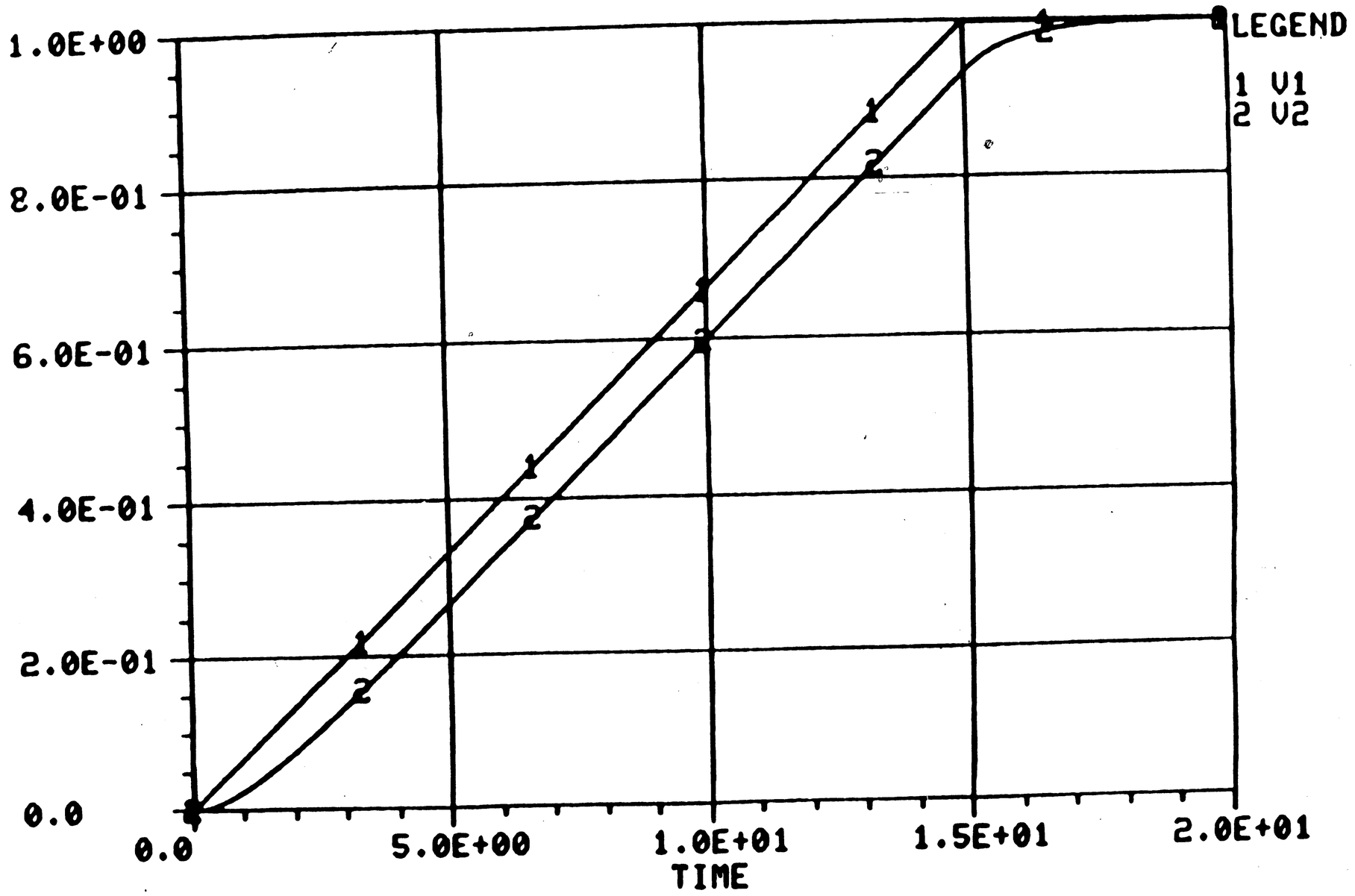
Typical Propagation Delay vs Load Capacitance.

Figure 7



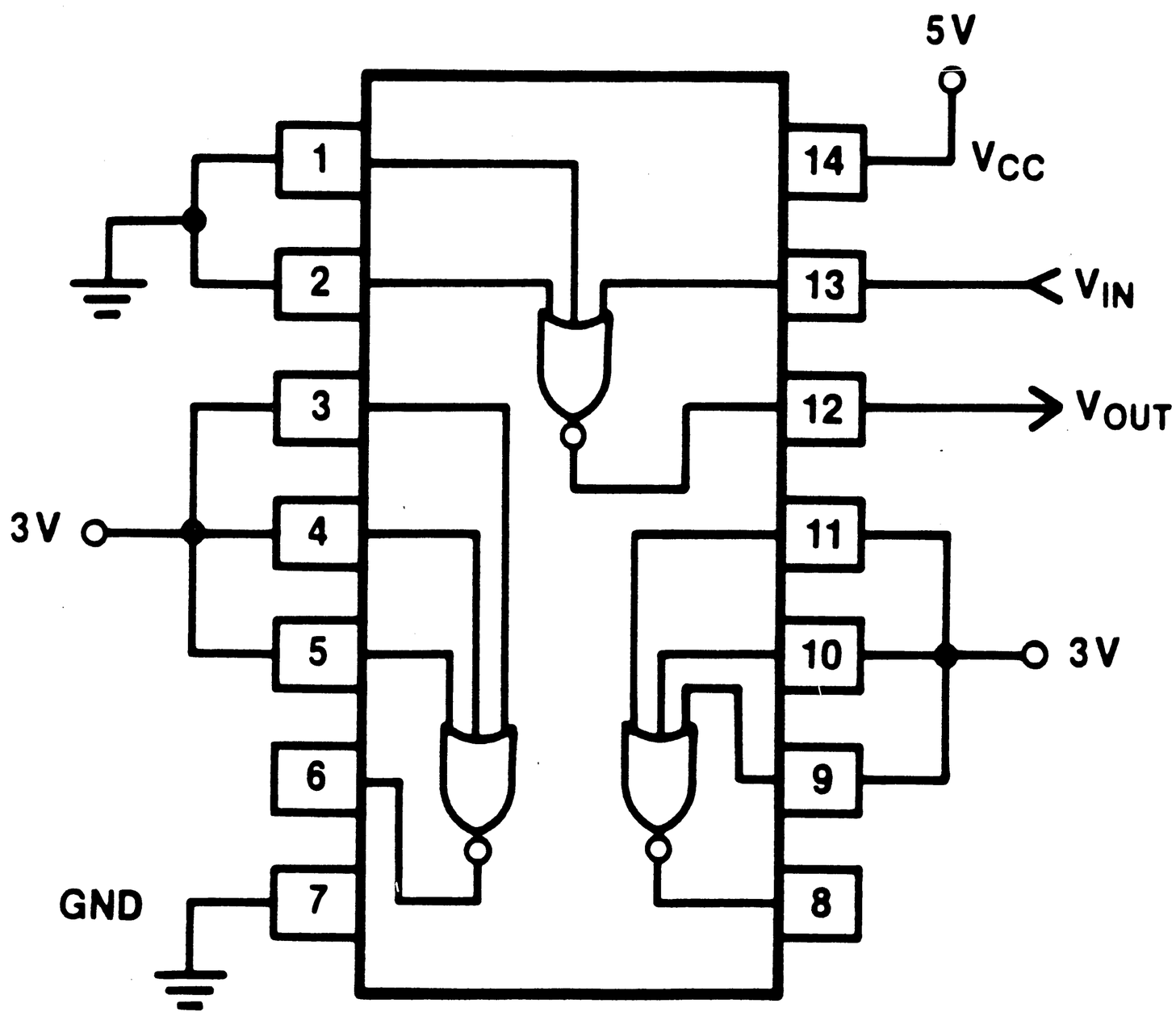
Output Response for Fast Rise Times

Figure 8



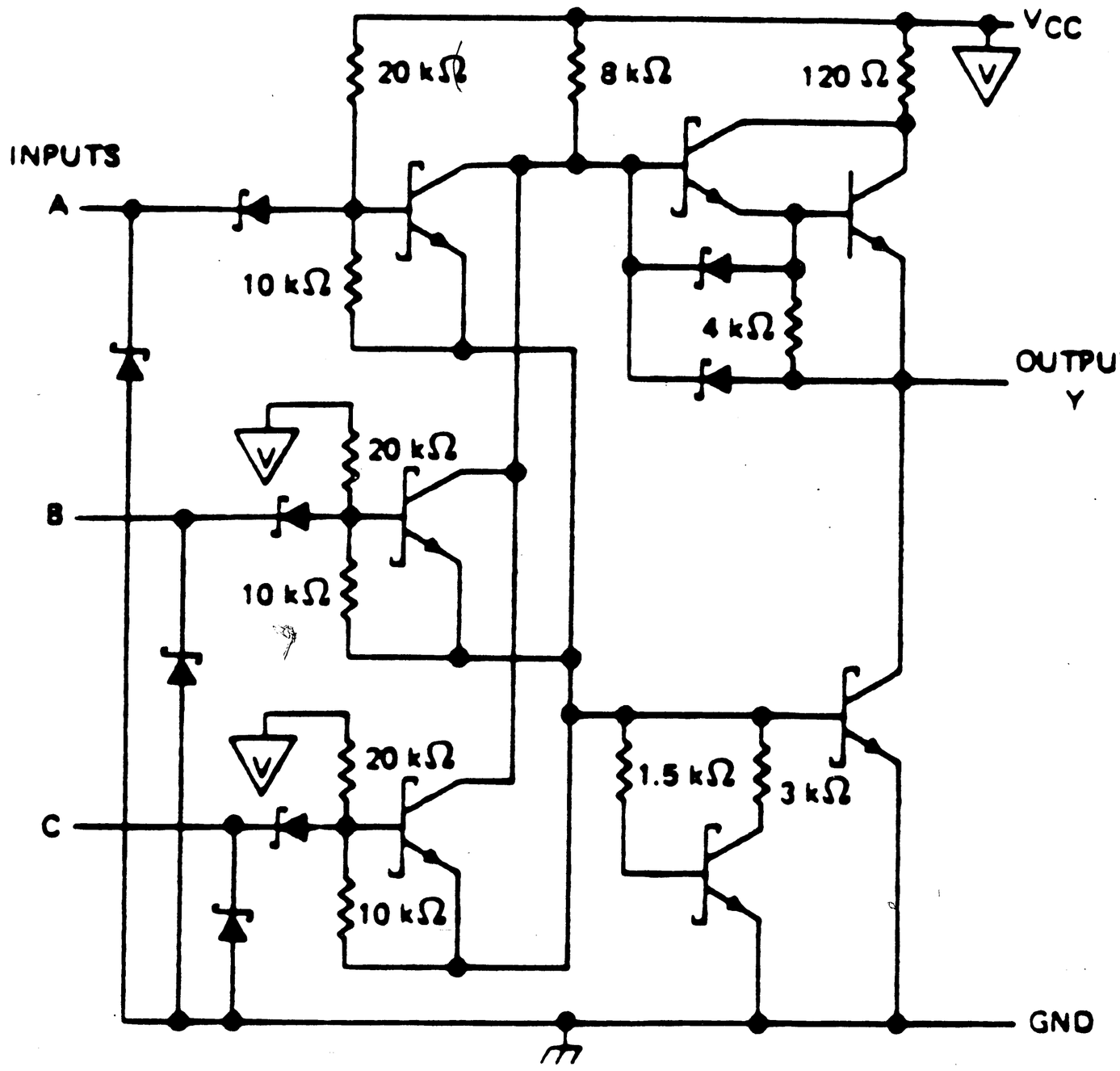
Output Response for Slow Rise Times

Figure 9



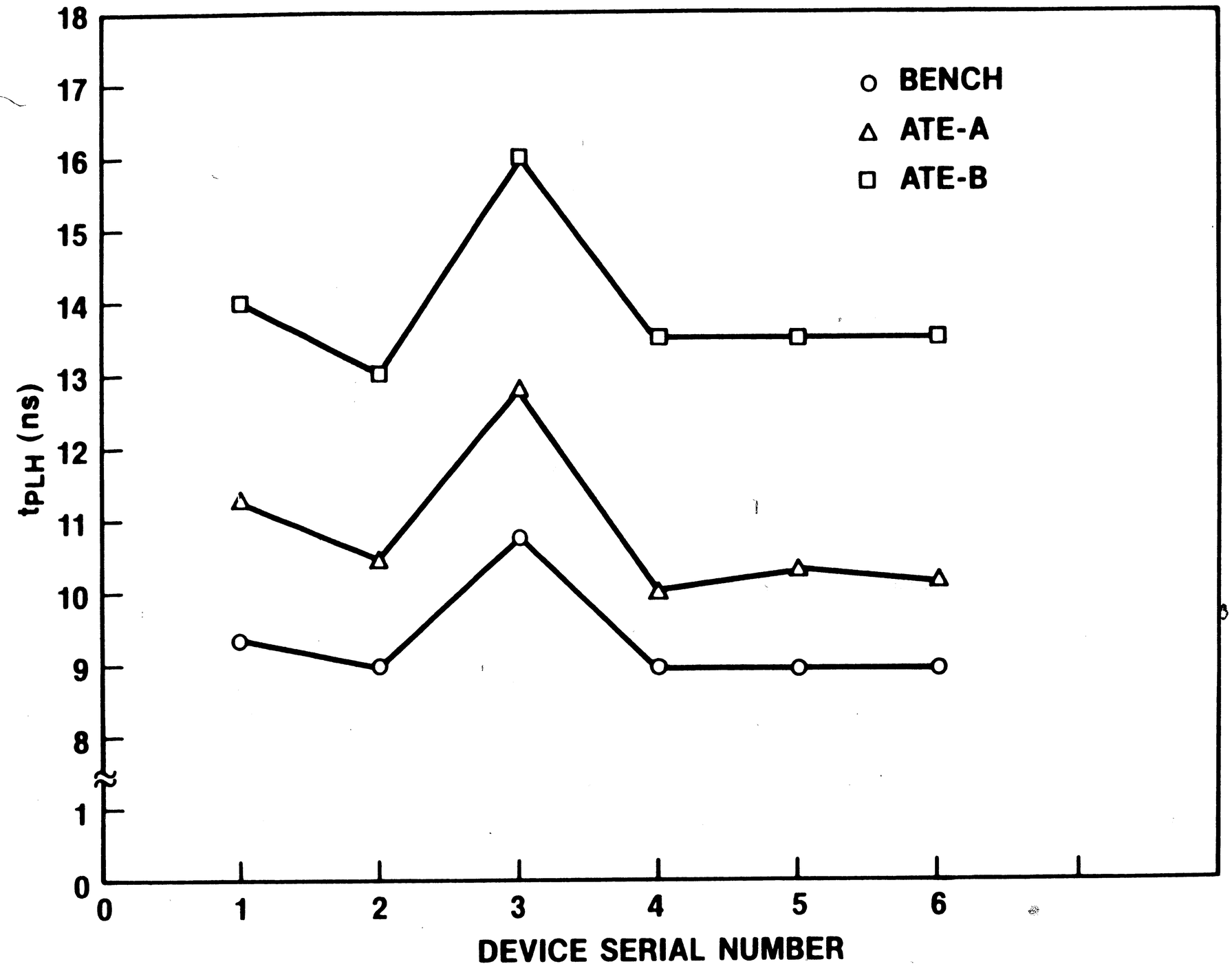
LOGIC DIAGRAM AND CONNECTIONS FOR THE t_{pd} TESTS

FIGURE 10



One Gate Equivalent Circuit of the 74LS27

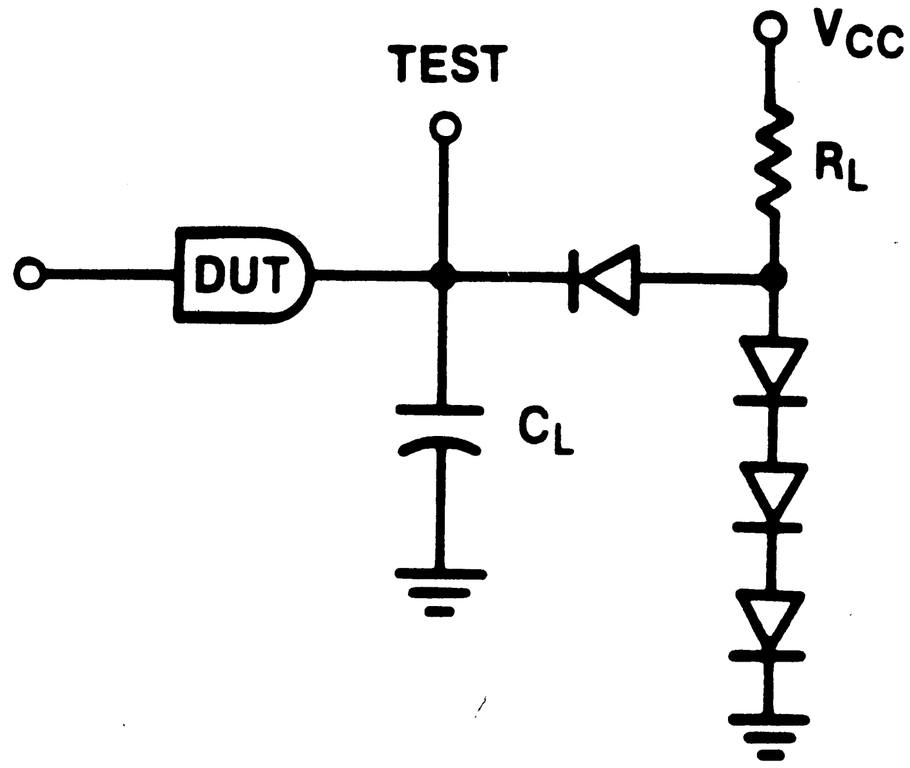
Figure 11



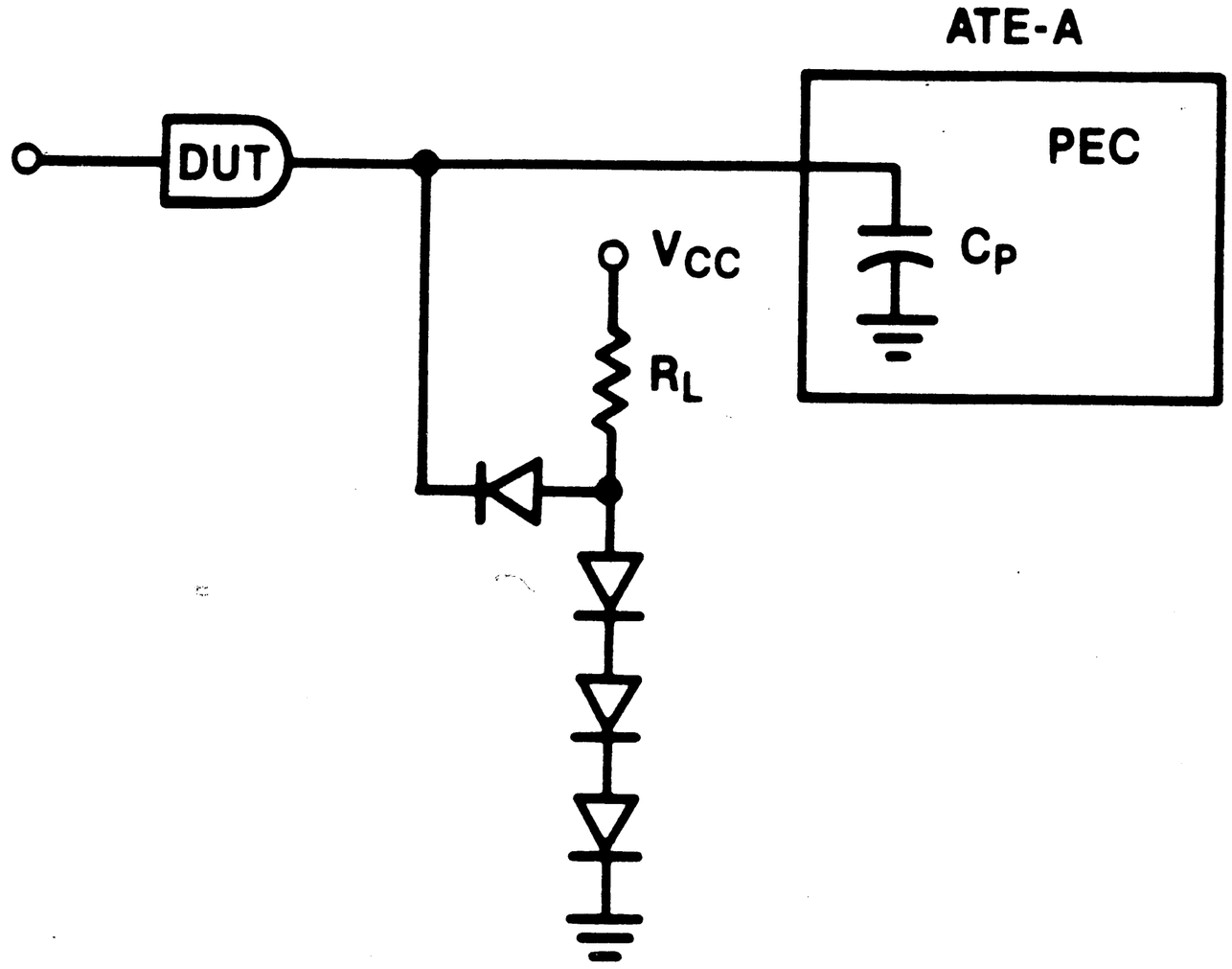
PROPAGATION DELAY (t_{PLH}) VS DEVICE NUMBER

FIGURE 12

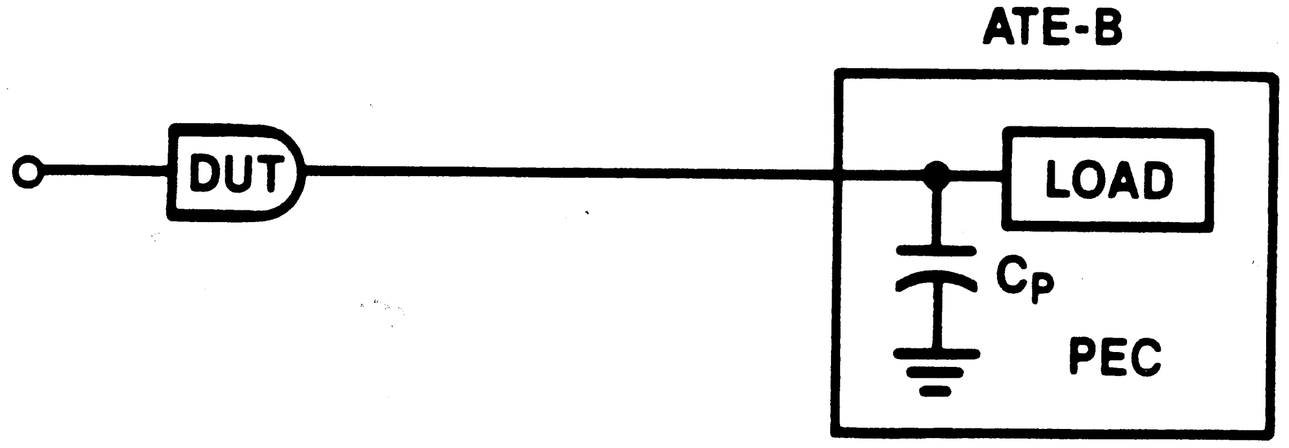
BENCH:



ATE-A:

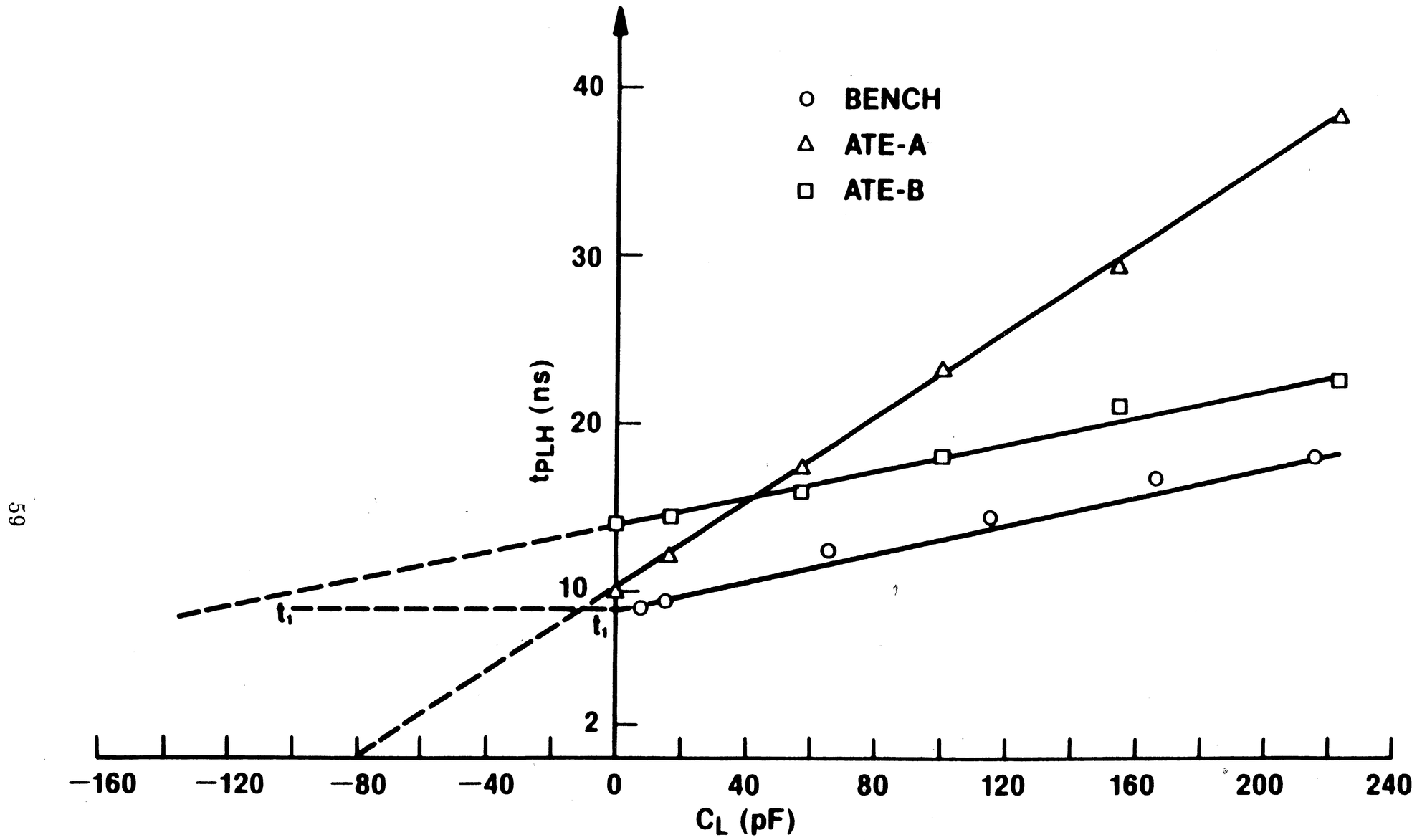


ATE-B:



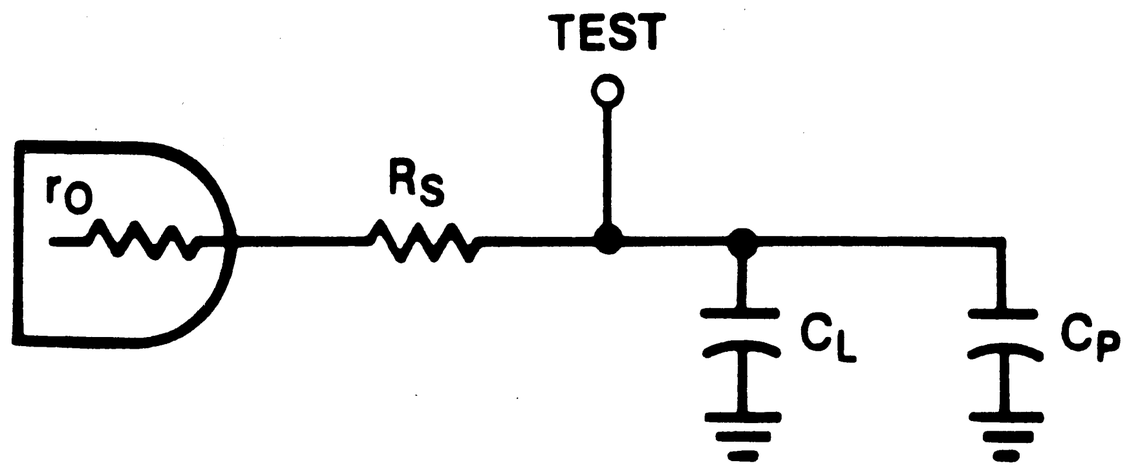
DUT LOAD CONNECTIONS

FIGURE 13

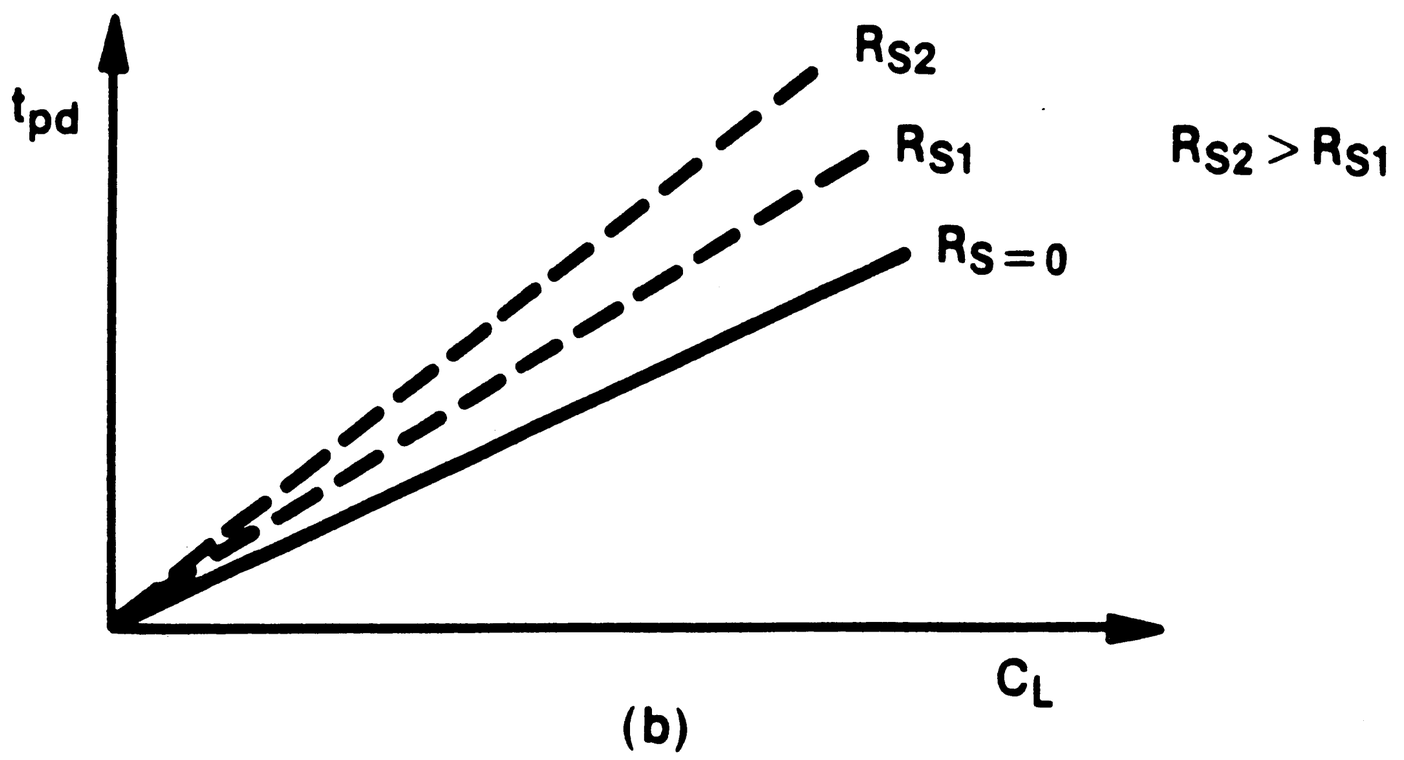


t_{PLH} VS C_L DATA FOR DEVICE #1

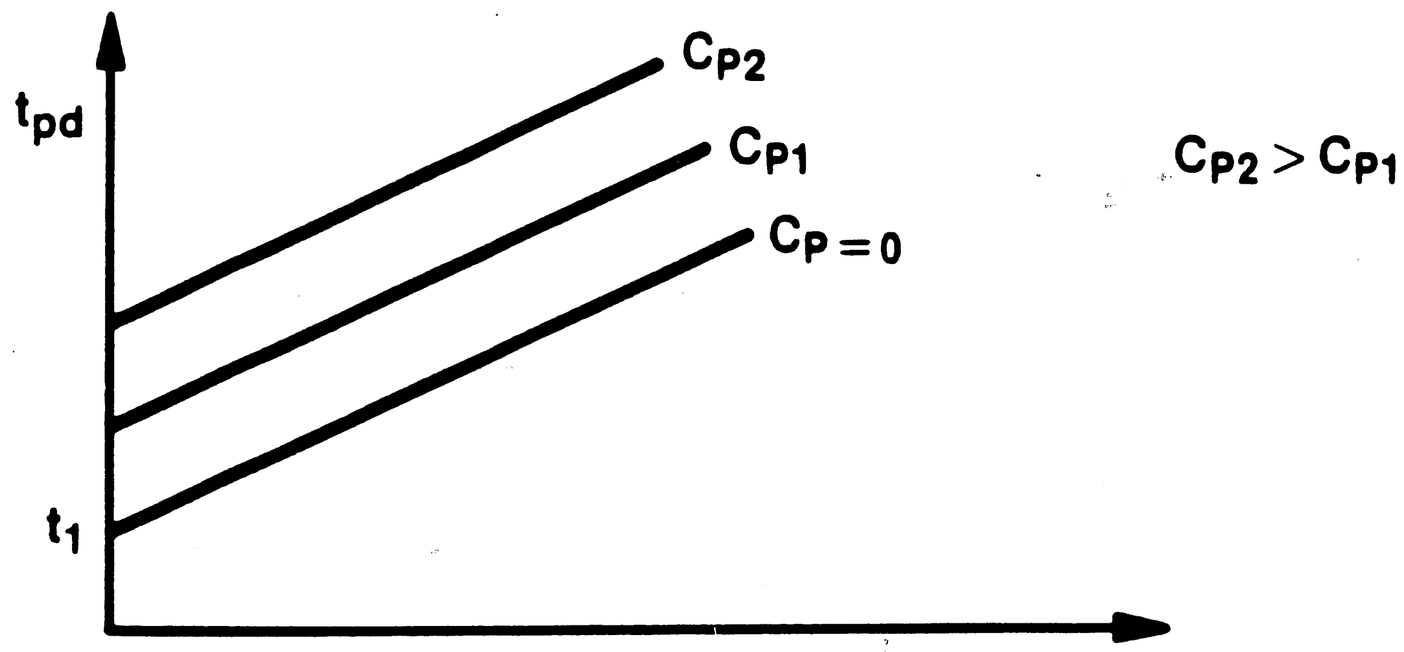
FIGURE 14



(a)



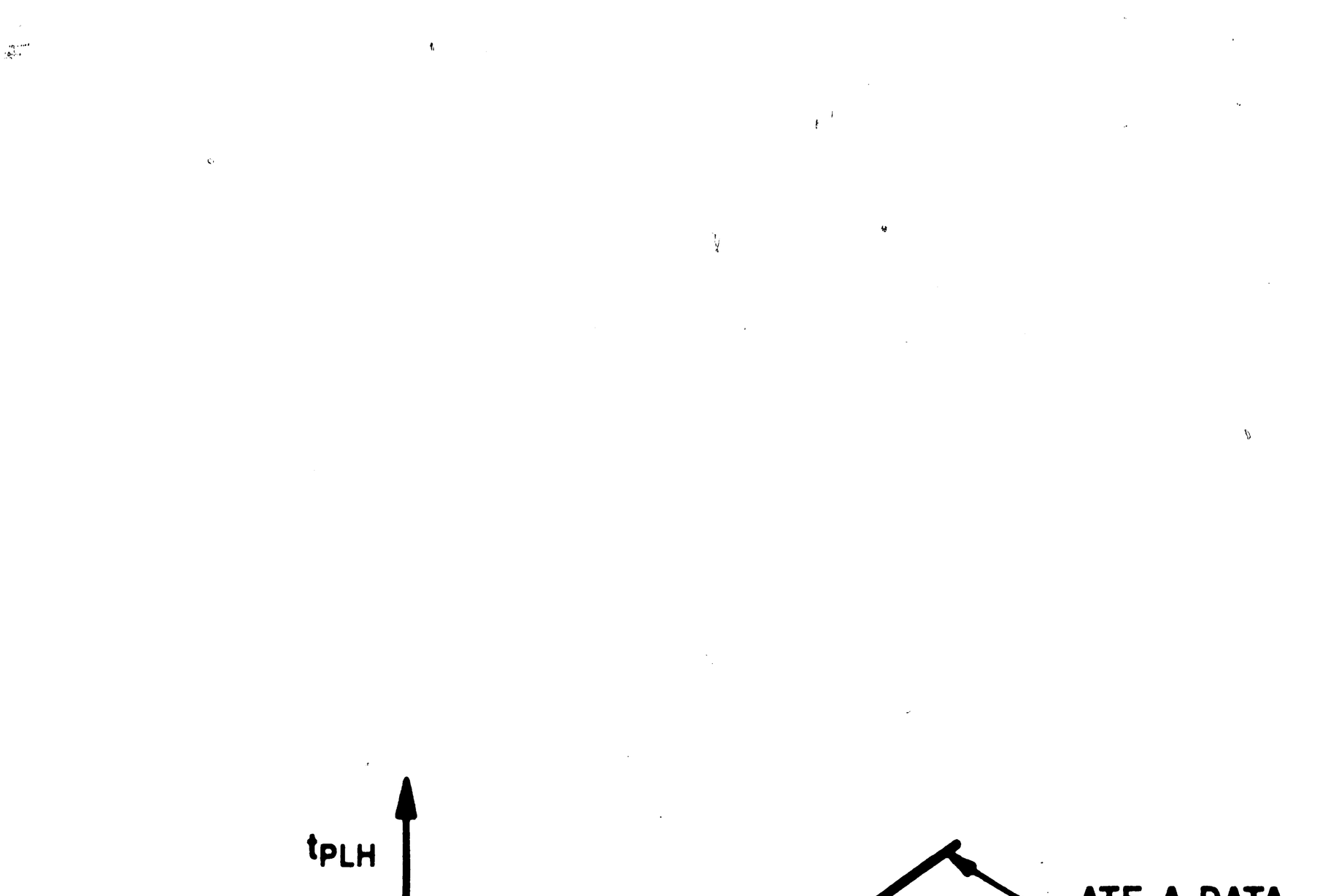
(b)



(c)

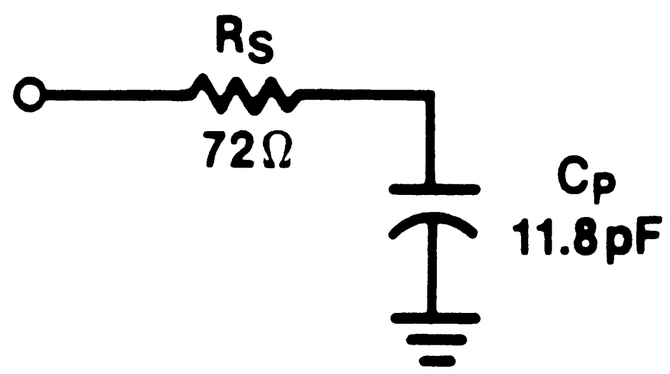
EFFECTS OF R_S AND C_P ON THE RC MODEL

FIGURE 15

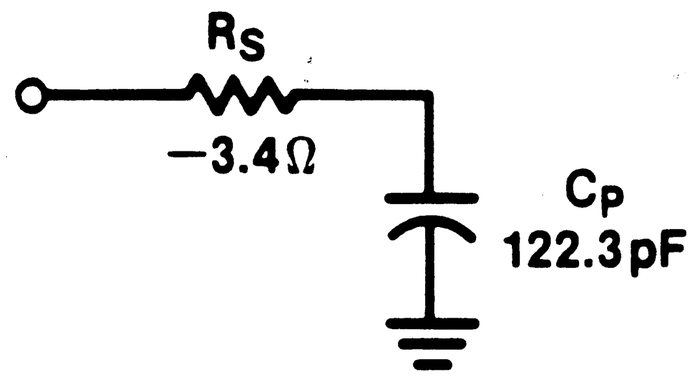


ATE-A TEST DATA SHIFT

FIGURE 16



(a) ATE-A



(b) ATE-B

SIMPLIFIED ATE EQUIVALENT MODEL
FIGURE 17

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[1] Fast and LSTTL Data Book, (Motorola Semiconductor Inc., 1986), p. 2-6.

[2] Omac Wing, Circuit Theory with Computer Methods, (McGraw-Hill Book Co. Inc., New York, 1978), p. 126-135.

[3] Dennis Petrich, "Achieving Accurate Timing Measurement on TTL/CMOS Devices", (IEEE Design and Test of Computers, 1986), p. 33-42.

[4] Private Communication with the Engineering Department of the ATE-A manufacturer, May 8, 1987.

[5] The TTL Data Book, Vol. 2, (Texas Instruments, 1985), p. 3-131.

[6] D. E. Diehl and R. T. Lane, "Test Programs for AT&T LS Device Evaluation", Internal Memorandum, 52221-861015-01IM, AT&T Bell Laboratories, Allentown, Pa., October 16, 1986.

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VITA

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In June of 1978 he joined AT&T Bell Laboratories and began an evening study program at Lafayette College, Easton, Pennsylvania. He graduated from the program in May, 1984 with a degree of Bachelor of Science in Electrical Engineering and is now concluding work on his Master of Science degree in Electrical Engineering at Lehigh University, Bethlehem, Pennsylvania.