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Table of Contents

List of Figures

List of Tables

Abstract

An existing application at *AT&T* involves the design of an *IC* using *CMOS* devices. In addition, the application requires that the inputs to this *IC* be *ECL*(Emitter-Coupled-Logic) compatible. It is well known that interfacing between *CMOS* and *ECL* is a tedious task.

This paper descibes a system that meets the interface requirements as well as other necessary specifications involving stability, power supply rejection and buffering. A description of the system is presented as well as the simulated results. The system is found to exhibit propagation delays as small as *1.2ns*, and rise and fall times as low as *0.2ns* which is expected for *ECL* compatible circuits. The system performance is guaranteed over a power supply range of $5.2 \pm 5\%$ and a temperature range of *0 to 75° C.*

Chapter 1
INTRODUCTION

Generally a digital system is constructed using only a single logic family, such as *CMOS, ECL, TTL,* or *NMOS.* However, sometimes this is impossible or not advantageous. Sometimes the desired components such as gates, registers, memories, and microprocessors are not available in a single logic family. Also, it may be only the "front-end" logic that requires the high speed of *ECL* ; for the slower logic the lower power *TTL*, or even *CMOS*, may be adequate. Then it becomes necessary to interconnect components from different logic families. Accomplishing this requires that the input characteristics of the interface be similar to those of the driving gate, while the output characteristics of the interface match the input characteristics of the receiver gate. Then it will appear as if the driving gate is driving a gate of the same logic family as the driver, and the reciever gate is being driven from a gate of the same logic family as the receiver.

In the past, most of the interfacing circuits that exist were between the *TTl* and *CMOS* logic families. This is because the input/output levels of *CMOS* and *TTL* gates are compatible with each other. However, we are faced with a problem when an application requires the high speed of *ECL* gates and the low power consumption of *CMOS* gates because the input/output levels of a typical *ECL* gate is not compatible with *CMOS* levels. This mandates the modification of our application slightly by using *TTL* gates to obtain the high speed requirements.

Internally, there are a few *ECL* to *CMOS* interfacing circuit available, but their performance characteristics are not what you would normally expect from

ECL compatible circuitry. However, at the present this problem is slowly being resolved due to the newest development in the *BiCMOS* technology. Although, the *BiCMOS* technology costs about 10% more to manufacture, it has a definite advantage over the now used *CMOS* technology in that it is *ECL* compatible. Thus, by using this technology a suitable *ECL* to *CMOS* interface is obtainable.

At present(1987) *CMOS* is still the most widely used form of digital *IC* , especially in the area of *LSI* and *VLSI*. Hence, in this paper, we will primarly be concerned with interfacing between the *ECL* and the *CMOS* logic family constructed in the *CMOS* process.

The components of the system that illustrates the interfacing between the two logic families are shown in Figure 1. The interfacing between each component is as follows:

First, the start-up circuit interfaces with the internally generated reference bias network to insure that the reference circuit starts up and operates in its proper bias state. An additional requirement is that the circuitry added to do this must not interfere with the normal operation of the reference once the circut has reached the desired operating point. Furthermore, this circuit serves as a biasing network to the current sources used in the op-amp circuit shown in Figure 11.

Next, the interfacing of the reference voltage is shown in block 2. The reference voltage is provided by an internal temperature and voltage-compensated bias driver. The bias driver is capable of generating any dc voltage level within a given range. However, our application requires that the bias driver sets the reference voltage, V_{ref} at the midpoint of the ECL input logic swing logic swing relatively independent of the temperature as illustrated in

Figure 2. This is done to minimize the switching time skews that would normally accur if the reference were not centered. With the V_{DD} supply set at $-5.2V$, the reference voltage turns out to be approximately $-1.3V$ at room temperature when referenced from V_{DD}. This is an additional requirement of the reference voltage namely to insure that this voltage is *ECL* compatible. The use of a negative supply for V_{DD} with V_{SS} at ground potential reduces the effects of noise voltages which may be coupled in to the power supply connections.

The third component used in interfacing *ECL* and *CMOS* levels is the unity-gain op-amp employed as a voltage follower. The op-amp serves as a buffer between the reference and the voltage comparator circuit. The buffering of the reference is needed to reduce the impedance mismatch problem between the reference circuit output and the comparator input, and to insure optimum drive to the comparator circuit. In addition, the op-amp is used also to enhance the reference current.

The comparator makes up the last block of the *ECL-To-CMOS* interface. The inputs are two *ECL* voltages V_{in} and V_{ref}. V_{ref} is internally generated and the other *ECL* input V_{in} is externally applied with a switching voltage range of $0.8V$. The comparator converts a single-ended *ECL* input signal to *CMOS* output levels. The desired level-shifting and amplifying take place in two different stages to insure optimum drive to a *CMOS* load.

Since the comparator output voltages are intended for *CMOS* inputs, the recieving logic gate is a *CMOS* inverter. The inverter is designed in such a way to insure optimum drive to a standard *CMOS* load with a fan-out of three.

The content of this paper will be discussed as follows: First, a brief in-

troduction to the overall system is discussed, followed in Chapter 2 with an introduction to several reference circuts examined for possible consideration as the stable reference voltage within the ECL-To-CMOS translator. Chapter 3 deal with the actual CMOS voltage reference circuit chosen for the system application. In addition, the performance characteristics of the circuit examined under worst case is presented. Chapter 4 discusses several discrete components of the system which include the design and analysis of the following circuits; a start-up circuit, a unity-gain CMOS op-amp, a voltage comparator and the CMOS gain-stage output load. This is followed in Chapter 5 with performance characteristics of the overall system simulated under all possible conditions which included process, temperature and power supply variations. Also, the sensitivity of each parameter to the final output node is discussed. Finally, a summary and conclusion of the system is presented

Chapter 2
INTRODUCTION TO REFERENCED-CIRCUITS

2.1 Introduction

During the last few years, there has been an increasing trend to realize analog and digital circuits on the same chip. Bipolar technologies are more appropriate to implement analog functions, but *CMOS* technologies are more interesting if large digital parts have to be realized. The implementation of analog and digital circuits on the same chip would require some type of reference voltage which determines the full-scale analog input or output level.

Voltage references are a key element of analog and digital circuits. In the past, several *CMOS* compatible voltage reference [14, 10, 11, 13, 15] have already been proposed but none of them achieves the presicion of purely bipolar bandgap references. The circuits suffer from the weakness of *CMOS* technologies (large amplifier offset, poor matching of transistors, etc.) or are quite complex and do not deliver a continuous reference voltage [13]. The reference voltage must be stable with variation in temperature and must be precisely controlled in spite of process and power supply variations.

As shown in Figure 2, our application requires the reference voltage generator providing a temperature and power supply tracking reference potential that is somewhere midway between a V_{IL} (maximum available gate voltage for a logic 1) and V_{IH} (minimum gate voltage for a logic 0) signal input level and is to be set by the transistor whose gate is connected to the reference voltage supply, V_{BB}. Furthermore, a centered V_{BB} minimizes switching time skews that

would occur if the reference supply were not centered. This is done to optimize noise immunity so that a gate can reliably detect the difference between a logic 1 high state(≈-0.7v) and a logic 0 low state(≈-1.9v). An additional requirement is that the voltages V_{IL} , V_{IH} and V_{BB} be referenced from the nominal supply voltage rail, V_{DD} which will range from a *-4.94V to -5.46V.*

The first approach in generating an internal reference supply voltage uses the difference between the threshold voltages of enhancement and depletion mode devices. Although this approach realizes a voltage which exhibits low thermal drift, the value of the output voltage is poorly controlled because it depends on the accuracy of depletion and enhancement implants. In addition the threshold differencing scheme requires an extra depletion implant, not normally needed in the *CMOS* process. A complete analysis of the theory will be presented, followed by the complete circuit realization.

The second approach used in generating a reference voltage utilizes the bandgap principle. Two reference diodes are forward biased by ratioed currents, and the positive temperature coefficient of the voltage difference is offset by the negative temperature coefficient of the single diode. This approach is used mostly in bipolar *IC*'s, where both reference devices and precision resistors are available. The basic principle of the reference is studied in detail, followed by a brief example of how to vary the circuit or the device parameter to yield a desirable output voltage.

In the next section, the design of a simple bandgap circuit that can be conveniently implemented in *CMOS* technology is presented. The unique approach is to use p^+-diffusion temperature dependent resistors to provide bias currents to the reference diodes, which are the emitter-base junctions of the

bipolar transistors formed by the p^+ diffusion inside the n-well on a p-substrate.

Finally, enhancements to the *CMOS* reference circuit will be presented. Simulation results of the circuit performance under worst case conditon will be illustrated.

2.2 The Threshold-Referenced Voltage Source

2.2.1 The Basic Reference

The first step in realizing a complete voltage reference is to find a stable unit of voltage, such as the Zener or bandgap voltage used in bipolar reference circuits [17]. Individual terms that make up the threshold voltage (given as (2.1) for an enhancement device) include components that are both highly temperature sensitive and process dependent.

$$V_{TE} = V_{FB} - \frac{Q_{SS}}{C_{OX}} + V_S + 2|\phi_P| + \frac{|Q_d|}{C_{OX}} \tag{2.1}$$

In Eq. (2.1) V_{FB} is the flat-band voltage, Q_{SS} is the surface charge per unit area, C_{OX} is the gate oxide capacitance per unit area, V_S is the source voltage, $2|\phi_P|$ is the voltage required for strong inversion, and Q_d is the charge per unit area in the inversion layer. Both V_{FB} and ϕ_P vary with temperature, and all terms (except V_S) are process dependent.

If an implant is added to the process to yield depletion devices, the depletion threshold is given by:

$$V_{TD} = V_{FB} - \frac{Q_{SS}}{C_{OX}} + V_S + \phi_{bi} + \frac{|Q_d|}{C_{OX}} + \frac{|Q_i|}{C} \tag{2.2}$$

where Q_i is the implanted charge per unit area, ϕ_{bi} is the built-in potential between the channel and the substrate, and C consists of the series connection of C_{OX} and a capacitance defined by the depth of the implanted channel [8]. The

depletion-threshold equation contains many of the same temperature and process-dependent terms as the enhancement equation, and therefore, neither threshold voltage alone is suitable for use as a reference.

Substracting Eq. (2.2) from Eq. (2.1) yields

$$V_{TE} - V_{TD} = 2|\phi_P| - \phi_{bi} + \frac{|Q_i|}{C} + |Q_d|\left(\frac{1}{C_{OX}} - \frac{1}{C}\right) \tag{2.3}$$

Many of the temperature-sensitive terms have been cancelled, and since $2|\phi_P|$ is approximately equal to ϕ_{bi} and C_{OX} is about equal to C [8], the difference between the enhancement and depletion thresholds is mainly fixed by the magitude of the implant charge Q_i. This quanity depends on an easily controllable and reproducible process step, and to a first order is independent of temperature. A stable voltage reference can thus be obtained by realizing a circuit that generates a voltage proportional to the difference between the enhancement- and depletion-threshold voltages.

Analogous to bipolar references [17] in which the base-emitter voltage is used to sense the magnitude of the silicon bandgap, the gate/source voltage of a *MOS* device can be used to sense the threshold voltage.

A circuit that produces a reference voltage sensitive to the V_{GS} differences is shown in Figure 3. In the figure, transistors M_1 and M_2 are the enhancement/depletion reference pair and the output voltage is seen to be the difference between V_{GSE} and V_{GSD}. By using an operational amplifier in a negative feedback configuration, the output voltage is forced to a level that causes the reference devices to operate at equal V_{DS} and I_{DS} values.

To analyze the temperature sensitivity of V_{ref}, we make use of the equation for a saturated MOS transistor to derive

$$V_{GS} = \sqrt{\frac{I_{DS}}{\beta}} + V_T \tag{2.4}$$

where I_{DS} is the drain-to-source current, V_T is the threshold voltage, and $\beta = \mu k C_{OX} W/L$ is the gain factor for the device.

Considering all possible variations in Eq. (2.4), we can derive

$$\frac{dV_{ref}}{dT} = \frac{d}{dT}\left(V_{GSE} - V_{GSD}\right)$$

$$= \frac{d}{dT}\left(V_{TE} - V_{TD}\right)$$

$$+ \frac{1}{2\sqrt{I_{DS}}}\left(\frac{1}{\sqrt{\beta_E}} - \frac{1}{\sqrt{\beta_D}}\right)\frac{dI}{dT}$$

$$+ \frac{\sqrt{I_{DS}}}{2}\left[\frac{1}{\sqrt{\beta_D}}\frac{1}{\mu_D}\frac{d\mu_D}{dT} - \frac{1}{\sqrt{\beta_E}}\frac{1}{\mu_E}\frac{d\mu_E}{dT}\right] \tag{2.5}$$

where the subscripts E and D refer to the enhancement and depletion devices. The three factors in Eq. (2.5) that show appreciable temperature sensitivity are the threshold voltages, the device drain currents (assumed equal for both devices), and the channel mobilities. Overall reference performance can be predicted by separately considering the effects of each of these terms.

2.2.2 Threshold-Voltage Consideration

The foregoing discussion of the basic reference has emphasized it dependence on the threshold voltages of the enhancement and depletion *MOS* transistors. The basic equation that have been given for the threshold voltages [Eqs. (2.1) and (2.2)] were derived for *MOS* transistors having constant doping near the surface under idealized conditions, and should be regarded as first-order theory.

Lee [9] has considered the threshold voltage of *MOS* transistors in

elaborate detail. His analysis shows that the threshold voltage depends on geometry and drain and substrate bias as well as on the specific dopant density near the surface. The dependence of V_T on drain bias makes it imperative to use a consistent bias scheme when specifing the threshold voltage. In particular, V_T as determined from channel conductance at zero bias is different from V_T as determined from the square root of I_D in the saturation region.

2.2.3 Bias-Current Consideration

The second term in Eq. (2.5) shows that the reference voltage can be made insensitive to drain current variations by equating β_E and β_D . This can be done by mismatching the aspect ratios of the enhancement and depletion devices so that

$$\mu_E \frac{W}{L_E} = \mu_D \frac{W}{L_D} \tag{2.6}$$

absolute bias current also appears as a coefficient of the mobility variation term in Eq. (2.5), and since that term does not cancel by equating the device gain factors, correct choice of operating current is necessary for optimum reference performance.

The drain current in a *MOS* transistor tends to increase with temperature because of its dependence on the threshold voltage, and to decrease with temperaure because of the temperature sensitivity of the mobility. These tendencies are nearly in balance at a bias level that is itself only slightly variable with temperature. If the reference *MOS* transistors are biased at this current level, the individual variations in V_{GS} will be reduced. Although the voltage reference is sensitive to the difference between V_{GS} in the depletion and enhancement MOS transistors, simulations show that the temperature sensitivity of the refer-

ence is also improved by using bias currents that desensitixe the individual V_{GS} values. To obtain an equation for the optimal bias current in the reference, we assume that mobility varies roughly as $T^{-3/2}$ [7]; that is

$$\mu = (\mu_0 T_0^{3/2}) T^{-3/2} \tag{2.7}$$

where μ_0 and T_0 are convenient reference mobility and temperature values. Since the threshold voltage can be characterized by $V_T \approx V_{T0} - \alpha T$ over the useful range of temperatures, we can express the derivative of V_{GS} with respect to temperature by using these expressions in Eq. (2.4).

$$\frac{dV_{GS}}{dT} = -\alpha + \sqrt{\frac{L}{kWC_{OX}dT}} \sqrt{\frac{I_{DS}}{\mu_0}\left(\frac{T}{T_0}\right)^{3/2}} \tag{2.8}$$

If Eq. (2.8) is set to zero, we can derive

$$\begin{aligned} I_{DS} &= \alpha^2 \mu_0 T_0^{3/2} k C_{ox} \sqrt{T} \frac{W}{L} \\ &= \mu C_{OX} \frac{W}{L} k (\alpha T)^2 \end{aligned} \tag{2.9}$$

When the *MOS* transistor is biased with the current given in Eq. (2.9), its gate voltage will be constant at V_{T0}. It is neither practical nor necessary to cause the bias current to have the exact variation with temperature that is predicted by Eq. (2.9), because the reference is sensitive to the differences in V_{GSE} and V_{GSD}, not to their individual values. The design value for the bias current in therefore 9μA, which corresponds roughly to Eq. (2.9) evaluated in the middle of the temperature range.

2.2.4 Mobility Versus Temperature

The initial consideration of the basic reference neglected sensitivity of V_{ref} to the variation of mobility with temperature based upon an assumption that mobilities vary as $T^{-3/2}$ both for the depletion and enhancement devices. This assumption is only approximately true. Scattering by impurity centers plays a more dominant role in the depletion *MOS* transistor than it does in the enhancement devices. This is true because the total impurity density in the channel region is greater in the depletion *MOS* transistor than in the enhancement *MOS* transistor. As a result, the ratio μ_D/μ_E increases with temperature in the low-temperature range [1]. The ratio becomes more nearly constant in the mid- and high-temperature range where lattice scattering dominates in determining the mobility value.

Mobility variations introduces a positive derivative to dV_{ref}/dT that tends to cancel the negative temperature gradient from the threshold-voltage variations. True variations in mobility produces variations in V_{ref} that are of the order of the variation in V_{TE}-V_{TD} and of opposite sign. Simulations have shown that for different temperatures, the mobility variation term dominates at low temperatures, and the threshold-variation term dominates at high temperatures [1]. This leads to a voltage drift versus temperature curve similar to that of bipolar bandgap reference in that the temperature coefficient is positive for low temperatures, flattens to zero near room temperature, and then becomes negative for high temperatures.

2.2.5 Reference Circuit

The considerations of the previous sections have shown that a stable *NMOS* reference can be made by taking the difference between the gate/source voltages of enhancement and depletion *NMOS* devices operating at appropriate current levels near threshold.

Figure 3 shows the full schematic of a low TC *NMOS* voltage reference based on this principle. Transistors M_1 and M_2 are the differential enhancement/depletion pair, loaded by depletion-current sources M_3 and M_4. The matching of these loads is important, since mismatch in the reference-pair drain currents degrades the output-voltage temperature coefficient. The geometry used has a 7-μm channel width and a 40-μm gate length, which yields high output resistance, and, therefore, high gain when used as a load. While the individual values of channel width and gate length were chosen to insure proper matching, the device aspect ratio was chosen to supply the reference pair with the drain current in the low dV_{GS}/dT range, as previously described. Since the threshold voltages of M_3 and M_4 must match to provide equal bias currents, it is necessary to maintain equal voltages at their respectives drain. This is achieved by adding a second differential gain stage (M_5 - M_8) in the main feedback loop. Balance of this stage is improved by use of M_7 which also provides balance- to single-ended conversion. If equal currents flow through matched depletion transistors M_7 and M_8, then V_{GS7} must equal zero, since the gate and drain of M_8 are shorted. Thus, M_5 and M_6 always operate with equal V_{DS}, regardless of the absolute voltage swing caused by output load current variations changing V_{GS} in the output buffer M_9. To obtain equal currents in M_7 and M_8, it is necessary to make M_{11} with the same geometry as M_8, and make the aspect ratio of M_{14}

twice that of M_{19}. All geometries must be designed to nominally equate the voltages at the drains of M_{11} and M_8, so that matching is preserved for variations in threshold voltage caused by negative supply voltage changes.

Loop gain of the two-stage unity-gain feedback amplifier is 40dB, which is large enough to yield proper load regulation, but low enough to allow frequency compensation with a small capacitor placed between the sources of M_1 and M_2. Common-mode bias loops consisting of transistors M_{11} - M_{15} provide feedback to insure that all depletion-current sources operate in their saturated regions. More than *50dB* of supply rejection is achieved, since all voltages and currents depend on individual device geometries.

Using the correct geometries from the final reference design (including the optimizing mismatch of the aspect ratios of the enhancement/ depletion reference pair, which compensates for the mobility differences), *ADVICE* predicts a *TC* greater than 500ppm/° C which is not compable to the *TC* obtained in bipolar reference circuits. The choice of the optimum reference-pair bias current was verified, as the substrate voltages of M_3 and M_4 (Figure 3) were varied to produce reference-pair currents of 6 and 9μA.

2.3 Bipolar Referenced-Circuit

The drawbacks of the threshold-referenced circuit using the difference between threshold voltage of enhancement and depletion devices [3] are as follow: Although this approach realizes voltages which exhibits low thermal drift, the value of the output is poorly controlled because it depends on the accuracy of the depletion and enhancement implants. The accuracy of the implants influences the accuracy of the threshold voltage which is sensitive to process variations. Threshold voltages are adjusted with a single implant that causes

an equal but opposite change in both the enhancement and depletion threshold voltage. For example, if the implant is adjusted (say 10%) is such a way that the threshold voltage of the enhancement device increases (say 209mV), this will cause the depletion-threshold to decrease by the same amount. These values are based on a combination of process data and simulation for the *MOS* process at *AT&T*. Thus we are led to examine other possibilities for the realization of a biasing circuit with a low temperature coefficient.

The second appraoch used in precision bipolar analog circuit utilizes the bandgap principle. We assume for simplicity that the objective is a voltage source of a low but controllable temperature coefficient. The first step in obtaining a voltage reference is to generate a relatively temperature independent current reference. Figure 4 shows the classical Widlar Bipolar *PTAT* (Proportional- To-Absolute-Temperature) current reference upon which the *CMOS* reference circuit discussed later is based. The circuit application is as follow; the current mirror consisting of Q_1, Q_2 combined with reference resistor R_{ref} satifies the relationship

$$I_2 R_{ref} = V_T \ln \left[\frac{I_1 I_{S2}}{I_2 I_{S1}}\right] \tag{2.10}$$

where I_{S1}, I_{S2} are the saturation currents of Q_1, Q_2 respectively and $V_T = \frac{kT}{q}$. The feedback loop consisting of transistors Q_1-Q_4 force the bias current

$$I_1 = I_2 \tag{2.11}$$

Solving Eq. (2.10) and Eq. (2.11) yields

$$I_{PTAT} = I_1 = I_2 = \frac{V_T \ln (n)}{R_{ref}} \tag{2.12}$$

where $n = \frac{I_{S2}}{I_{S1}}$ is the area factor that differ Q_3 to Q_4. As can be seen from Eq.

(2.12), the current produced is proportional to absolute temperature ($PTAT$). The magnitude of this current is physically controlled by proper sizing of R_{ref} and n. The possibility exists for referencing the output current, I_{PTAT} to a composite voltage that is a weighted sum of $V_{BE(on)}$ and V_T By mirroring this $PTAT$ current into a series combination of a resistor and a diode. a temperature stable voltage can be obtained. The positive temperature coefficient of the voltage across the resistor is cancelled by the inherent negative temperature coefficient of the diode. By proper sizing of devices Q_5, R_1, and D_1, the point in temperature at which this cancellation occurs can be controlled. In order to determine the required value for Q_5, R_1, and D_1, we must determine the temperature coefficient of the output voltage V_{BB} more precisely.

From Figure 4, the output voltage can be expressed as

$$V_{BB} = V_{BE1(on)} + I_{out}R_1 \tag{2.13}$$

where $I_{out} = mI_{PTAT}$ and $m = \beta_{M_{p5}}/\beta_{M_{p3}}$. The $V_{BE(on)}$ can be written, neglecting base current,

$$V_{BE(on)} = V_T \ln \frac{I_{out}}{I_{S5}} \tag{2.14}$$

The saturation current, I_{S5}, can be related to device structure by [5]

$$\begin{aligned} I_{S5} &= \frac{qA_{E5}n_i^2\overline{D}_P}{Q_B} \\ &= B\overline{D}_P n_i^2 \\ &= \overline{B}n_i^2 T\overline{\mu_P} \end{aligned} \tag{2.15}$$

where n_i is the intrinsic minority-carrier concentration, Q_B is the total base doping per unit area, $\overline{\mu_P}$ is the average hole mobility in the base, A_{E5} is the

emitter-base junction area, and T is the temperature in degrees kelvin. The Einstein relation $\overline{\mu_P} = \frac{\overline{D}_P}{V_T}$ was used to write I_S in terms of $\overline{\mu}_P$ and n_i^2. The quantities in Eq. (2.15), that are temperature dependent are given by

$$\overline{\mu_P} = CT^{-\overline{n}} \tag{2.16}$$

$$n_i^2 = DT^3 \exp(\frac{-V_{G0}}{V_T}) \tag{2.17}$$

where V_{G0} is the bandgap voltage of silicon extrapolated to zero degrees kelvin. Combining Eqs. (2.15), (2.16) and (2.17)

$$\begin{aligned} I_{S5} &= ET^{\delta} \exp(-V_{G0}/V_T) \\ &= N(1.964E{-}16) \end{aligned} \tag{2.18}$$

where

$$E = \overline{B}CD \tag{2.19}$$

and

$$\delta = 4 - \overline{n} \tag{2.20}$$

and N is the number of diodes connected in parallel to produce $V_{BE(on)}$. The value *1.964E-16A* is the saturation current needed for a one unit diode. This value was extracted from the *BIMOS* process at *AT&T*. Combining Eq (2.12) and Eq. (2.13)

$$I_{out} = \frac{mV_T \ln(n)}{R_{ref}} \tag{2.21}$$

Substituting Eq. (2.14), Eq. (2.18), and Eq. (2.21) into Eq. (2.13) and rearranging, it follows that

$$V_{BB} = V_T \ln\left[AmV_T \ln(n) m \frac{T^{-\delta}}{R_{ref}} \exp(\frac{V_{G0}}{V_T})\right] + \frac{mV_T \ln(n) R_1}{R_{ref}} \tag{2.22}$$

where $A = 1/E$ is a temperature independent quanity. Simplying Eq. (2.22) yields

$$V_{BB} = V_T Q(T) + V_{G0} \tag{2.23}$$

where

$$Q(T) = m\ln(n)x + \ln\left[\frac{mk_B \ln(n) AT^{(1-\delta)}}{qR_{ref}}\right] \tag{2.24}$$

and

$$x = \frac{R_1}{R_{ref}} \tag{2.25}$$

This expression gives the output voltage as a function of temperature in term of circuit parameters, x and δ and the device parameters m and n. Our primary objective is to be able to have complete control of dV_{BB}/dT and to this end we take the derivative of V_{BB} with respect to temperature. Differentiating Eq. (2.23),

$$\pm\overline{m_1} = \frac{dV_{BB}}{dT}$$

$$= \frac{V_T}{T}\left[xm\ln(n) + \ln\frac{mk_B \ln(n) AT^{(1-\delta)}}{qR_{ref}} + (1-\delta) - T(TCFR_{ref})\right]_{T=T_r} \tag{2.26}$$

where

$$TCFR_{ref} = \frac{1}{R_{ref}}\frac{dR_{REF}}{dT} \tag{2.27}$$

and T_r is the reference temperature at which the parameters in Eq. (2.26) is evaluated. Shown in Figure 2, the V_{BB} is specified to lie between V_{IL} and V_{IH}. It also shows that V_{BB} should have a slope approximately equal to the slope of V_{IH}. By knowing the slope of V_{BB} and the current level at which the reference should operate, we can rearrange Eq. (2.26) to find the value for x. Once the value of x is known, this value is placed into Eq. (2.24) then into Eq. (2.23) to

give the desired value of V_{BB} that corresponds to the desired slope. An eample is given below to illustrates how we can achieve the value for the expression $V_{BB}/dT \approx dV_{IH}/dT$ at 25 ° C.

Suppose that an application requires that the magnitude of the reference voltage V_{BB} be centered in order to minimizes switching time skews. Extracting the necessary data from Figure 2 the magnitude

$$|V_{BB}| = \frac{V_{IHmin} + V_{ILmax}}{2} \tag{2.28}$$

is approximately equal to $1.3V$. In addition, the slope should be chosen such that

$$m_1 = \frac{dV_{BB}}{dT} \approx \pm \frac{dV_{IN}}{dT} \tag{2.29}$$

The extracted value of the slope is approximately equal to $1.33mV/°\ C$ and should maintain this regulation over a temperature range of 0 to 75 ° C and a power supply range of 4.94 to $5.46V$.

Assume that the reference current is not to exceed a value of 10μA, the feedback loop of Q_1 - Q_4 is ideal, and that area factor n equals 5.

The reference resistor is given by Eq. (2.15) as

$$R_{ref} = \frac{V_T \ln(n)}{I_{PTAT}} \tag{2.30}$$

$$R_{ref} = \frac{25.73m\ x\ \ln(5)}{10\mu} = 4.14k\Omega \tag{2.31}$$

Using the data summarized in Table 4, the value of E needed to produce $V_{BE(on)}$ is given by Eq. (2.18). Assume $N = (5\ x\ n)$, we get:

$$E = (5\ x\ n)\ x\ 1.964\ x\ 10^{-16} T^{-\delta} \exp(\frac{V_{G0}}{V_T}) = 44.997\ ° K \tag{2.32}$$

and

$$A = \frac{1}{E} = 22.22\ x\ 10^{-3}/^{\circ}K \tag{2.33}$$

The desired slope m_1 can be calculated by rearranging Eq. (2.26) and is given by

$$x = \frac{R_1}{R_{ref}} = \frac{T}{m\ln(n)}\left[\frac{\pm m_1}{V_T} + \frac{(\delta-1)}{T} + TCF(R_{ref}) - \frac{1}{T}\ln\left(\frac{mk_B \ln(n) A T^{1-\delta}}{qR_{ref}}\right)\right] \tag{2.34}$$

Figure 2 shows that the reference voltage slope m_1 should be chosen such that its value is closer to V_{ILmax}. Thus, the desired slope is to be less than zero. Again, using the data in Table 4, the ratio resistor is calculated to be

$$x = \frac{R_1}{R_{ref}} = 6.840 \tag{2.35}$$

Thus, the output resistor, R_1 is designed to equal

$$R_1 = 6.840\ x\ R_{ref} = 28.32k\Omega \tag{2.36}$$

Neglecting base currents, $V_{BE(on)}$ can be calculated by using Eq. (2.14) and is given as

$$V_{BE(on)} = V_T \ln \frac{I_{out}}{I_{S5}} \tag{2.37}$$

Given that the saturation current is

$$I_{S5} = (5\ x\ n)\ x\ 1.964\ x\ 10^{-16}A = 49.10\ x\ 10^{-16}A, \tag{2.38}$$

A comparable value for the base-emitter voltage is calculated

$$V_{BE(on)} = 25.73m\ln\left[\frac{10\mu}{49.10\ x\ 10^{-16}}\right] = 0.552V \tag{2.39}$$

This value is exactly as *ADVICE* predicts.

The resulting output voltage is given from Eq. (2.13) as

$$V_{BB} = V_{BE2(on)} + xmV_T \ln(n) = 0.835V \tag{2.40}$$

2.4 CMOS Referenced Circuit

Figure 5 shows the simplest implementation of the reference in *CMOS*. An improved Wilson current source is used to insure the drain voltage of transistors M_1 and M_2 are equal. The feedback loop formed by M_1, M_2, M_3, and M_4 forces the current in transistor Q_1 to be the same as in R_{ref} The bottom mirror utilizes substrate pnp devices Q_1 and Q_5 connected as diodes. Transistors Q_1 and Q_5 have areas that differ by a factor of n and the feedback loop forces them to operate at the same bias current. Assuming the devices M_1 and M_2 that forms the current mirror is ideal, these devices force the voltage at nodes A and B to be equal causing the same logarithmic relationship betweeen I_1 and I_2 as seen in the bipolar circuit. That is, if

$$V_A = V_B \tag{2.41}$$

then

$$I_{PTAT} = I_1 = I_2 \tag{2.42}$$

Equation (2.12) can be written in term of the differences in the base-to- emitter voltages of Q_1 and Q_2 and is given by

$$I_{PTAT} = \frac{V_{BE1} - V_{BE5}}{R_{ref}} = \frac{\Delta V_{BE}}{R_{ref}} \tag{2.43}$$

As a result, Eq. (2.43) shows that the difference between the two V_{BE}'s appear across the reference resistor, R_{ref} Also, this expression can be written in term of the diode area parameter, n and as a function of temperature which is given in Eq. (2.12) for the bipolar circuit. Once a suitable reference current is obtained, device M_5 mirrors the reference current, I_{PTAT} through R_1 and Q_2 as in the bipolar circuit. The expression that shows the mirroring of the I_{PTAT} current into the output is shown in Eq. (2.21).

The primary advantage of this circuit is that the thermal voltage V_T has a positive temperature coefficient, and this, in combination with the positive temperature coefficient of the resistor gives a relatively temperatue-independent output current. This can be shown more clearly by taking the derivative of the expression given for the thermal voltage, V_T. This is

$$V_T = \frac{k_B T}{q} \tag{2.44}$$

where k_B is the Boltzman constant ($1.379 \text{x} 10^{-23} \text{J}/^\circ$ K), T is the absolute temperature in degree kelvin, and q is the electron charge ($1.6\ x10^{-19}$ coulomb). Differeniating the above expression gives

$$\frac{dV_T}{dT} = \frac{V_T}{T} \tag{2.45}$$

Using the expression in Eq. (2.27) for defining the temperature coefficient, it follows that the temperature coefficient of the thermal voltage is

$$TCF(V_T) = \frac{1}{V_T}\frac{dV_T}{dT} = \frac{1}{T} \tag{2.46}$$

This expression shows that the temperature coefficient of V_T is positive and vary indirectly with temperature. Nature insures us of alway having a positive temperature coefficient for the p^+-diffusion resistor, R_{ref}. With the results of Eq. (2.46), we can show I_{PTAT} as being relatively temperature independent and to this end we take the derivative of I_{PTAT} with respect to temperature. Differeniating Eq. (2.12),

$$\frac{dI_{PTAT}}{dT} = \frac{k_B \ln(n)}{q}\left[\frac{1}{R_{ref}(T)} - T\,\frac{dR_{ref}(T)}{dT}\,\frac{1}{R_{ref}{}^2(T)}\right] \tag{2.47}$$

Equation (2.47) can be written in term of I_{PTAT} to give

$$\frac{dI_{PTAT}}{dT} = I_{PTAT}\left[\frac{1}{T} - \frac{1}{R_{ref}}\,\frac{dR_{ref}(T)}{dT}\right] \tag{2.48}$$

Again, using the expression in Eq. (2.27) for defining the temperature coefficient, it follows that the the temperature coefficient of I_{PTAT} is

$$TCF(I_{PTAT}) = \frac{1}{T} - TCF(R_{ref}) \tag{2.49}$$

Combining Eq. (2.46) with Eq. (2.48) yield

$$TCF(I_{PTAT}) = TCF(V_T) - TCF(R_{ref}) \tag{2.50}$$

where

$$TCF(V_T) > TCF(R_{ref}) \tag{2.51}$$

This equation shows that if the condition given in Eq. (2.51) holds, the temperature coefficient of I_{PTAT} is alway positive and the output current can be made relatively temperature independent.

Although the circuit of Figure 5 will function, several non-idealities exist which mandate a more complex design. The first problem with the circuit is due to small differences in the gate-to-sorce voltage of M_1 and M_2. This can be best explained by examining the drain-to-source current of each device. The enhancement-mode MOS transistors, M_1 and M_2 are in the saturation mode of operation since their gates are shorted to their drain and their gate-to-source voltages exceed their threshold voltage, V_{TH}. We can express the drain currents of the two devices as

$$I_{DS1} = \frac{\beta_{n1}}{2}\left[(V_{GS1} - V_{Tn1})^2(1 + \lambda V_{DS2})\right], \tag{2.52}$$

$$I_{DS2} = \frac{\beta_{n2}}{2}\left[(V_{GS2} - V_{Tn2})^2(1 + \lambda V_{DS2})\right], \tag{2.53}$$

where I_{DS} is the drain-to-source current, V_{GS} is the gate-to-source voltage, V_T is the device threshold voltage, V_{DS} is the drain-to-source voltage, λ is an empirical channel length modulation factor having a value of (100) for the 1.75μm

twin-tub process, and β is the MOS transistor gain factor. β is dependent on both the process parameters and the device geometry, and is given by

$$\beta = \frac{\mu\epsilon}{t_{ox}}\left(\frac{W}{L}\right) \tag{2.54}$$

where μ is the effective surface mobility of the electrons in the channel, ϵ is the permittivity of the gate insulator, t_{ox} is the thickness of the gate insulator, W is the width of the channel and L is the length of the channel. Assuming that the devices are identical and neglecting body effect, Eq. (2.52) and Eq. (2.53) show that any small differences in the gate-to-source voltage of M_1 and M_2 will result in large variation in the output current. Furthermore, Eq. (2.43) can be revised to shows the effects of small differences in the gate-to-source voltage on the output current and is given by

$$I_{PTAT} = \frac{\Delta V_{BE} + \Delta V_{GS}}{R_{ref}} \tag{2.55}$$

where

$$\Delta V_{GS} = V_A - V_B \tag{2.56}$$

$$\Delta V_{BE} = V_{BE1} - V_{BE5} \tag{2.57}$$

Equation (2.55) shows that for large variations in output current, the voltage drop across R_{ref} is only on the order of 100mV. These voltages can result from device mismatches or from channel-length modulation in M_1 and M_2. Since the pairs of device M_3 - M_4 and M_1 - M_2 have different drain-to-source voltages, significant error currents are present. The second problem is due to *MOS* threshold voltage dependence on drain-to-source voltage. This can be shown theoretically for each device by rearranging Eq. (2.52) and Eq. (2.53) in term of V_T. Rearranging

$$V_{T1(V_{DS1})} = V_{GS1} - \sqrt{\frac{2I_{DS1}}{\beta_{n1}(1+\lambda V_{DS1})}} \tag{2.58}$$

$$V_{T2(V_{DS2})} = V_{GS2} - \sqrt{\frac{2I_{DS2}}{\beta_{n2}(1+\lambda V_{DS2})}} \tag{2.59}$$

The gate-to-source and drain-to-source voltage of each device shown in Figure 5 is given by

$$V_{GS1} = V_G - V_B \tag{2.60}$$

$$V_{GS2} = V_G - V_A \tag{2.61}$$

$$V_{DS1} = V_{D1} - V_B \tag{2.62}$$

$$V_{DS2} = V_{D2} - V_A \tag{2.63}$$

and

$$V_G = V_{G1} = V_{G2} \tag{2.64}$$

Combining Eqs. (2.60) - (2.64) with Eq. (2.58) and Eq. (2.59), we find

$$V_{T1(V_{D1},V_B)} = (V_G - V_B) - \sqrt{\frac{2I_{DS1}}{\beta_{n1}(1+\lambda(V_{D1} - V_B)}} \tag{2.65}$$

$$V_{T2(V_{D2},V_A)} = (V_G - V_A) - \sqrt{\frac{2I_{DS2}}{\beta_{n2}(1+\lambda(V_{D2} - V_A))}} \tag{2.66}$$

These equations show that the voltage at node A and B are equal only if the threshold voltage of M_1 and M_2 are equal. Figure 5 illustrates that the drains and sources of transistors M_1 and M_2 are not equal. Since their V_{DS} term are different, this results in an error term ΔV_{DS} being applied across resistor R_{ref}. Equation (2.43) can be rewritten to show the error term, ΔV_{TH} and is given as

$$I_{PTAT} = \frac{\Delta V_{BE} + \Delta V_{TH}(V_{DS}) + \Delta V_{GS}}{R_{ref}} \tag{2.67}$$

where

$$\Delta V_{TH} = V_{Tn1} - V_{Tn2} \tag{2.68}$$

$$\approx V_A - V_B \tag{2.69}$$

This error can be as large as ± 10%.

The third problem is that the reference voltage generated has to be referenced from the most negative supply rail, V_{DD}. This is necessary because all voltages obtained must be referenced to the same supply rail that the *ECL* signals are referenced from. However, Figure 5 shows the reference voltage as being taken from the V_{SS} rail. An obvious solution is to rotate the circuit 180° in such a way that the substrate of the vertical *pnp* transistor is tied to V_{DD}. Simulation confirmed the fact that the circuit is capable of operating nicely. However, the 1.75μm twin-tub process at *AT&T* requires that the collector of the the *pnp* transistor that is the paristic devices inherent in *p*-substrate *CMOS* technology be connected to the most negative supply available. Also, in this *CMOS* technology the vertical *pnp* bipolar devices are not readily available. These devices have not been widely explored because of lack of means of providing temperature controlled currents. However, in the 1.75μm *CMOS* technology the lateral *pnp* bipolar devices are available with the *p*-substrate collector tied to V_{SS}, *n*-tub base and p^+ emitter.

The final problem with the circuit of Figure 5 is inherent to most power supply independent biasing schemes. That is, the circuit has two operating points. One is at the desired current value and the other is a zero current state. This mandates a start-up circuit be included in order to insure proper operation.

Chapter 3
THE CMOS REFERENCED-VOLTAGE GENERATOR

3.1 CMOS Referenced-Voltage Generator

Figure 6 shows the development of a more practical implementation of the reference circuit. This circuit utilizes large geometry devices for M_1-M_{10} so as to minimize offsets in the drain voltage and cascode current sources in order to minimize channel-length modulation effects. The first items of interest are the current mirrors. The simple *PMOS* and *NMOS* current mirrors of Figure 4 (M_1, M_2 and M_3, M_4) have been replaced with cascode current mirrors. Devices M_3, M_4, M_6, and M_7 form the *PMOS* cascode current mirror and devices M_1, M_2, $M_9$and M_{10} form the *NMOS* cascode current mirror. Due to the cascode configurations, the output conductance mismatch problem describe above is significantly reduced. The primary reason in using cascode current source is to allow more voltage gain to be achieved in amplifier stages by increasing the load resistance. In this circuit, transistor M_2 shields transistor M_{10} and transistor M_7 shields transistor M_4 from the variations in voltage that occur at the output terminals. The small-signal output resistance that results have been increased by a factor $(1 + g_m r_o)$. It is interesting to note that the effect of the body effect in M_7 and M_{10} is to increase the output resistance slightly [5]. This cascode configuration also serve to improve the power supply rejection of the overall circuit.

In addition, the drain-to-source voltages of M_1 and M_2 are now forced to be equal, eliminating the errors associated with threshold dependence upon

drain-to-source voltage. As mentioned, all cascode devices used have longer than minimum channel lengths which results in lower output conductance and therefore better supply rejection.

The *PMOS* cascode current mirrors are biased by the bias node of *BIAS1* and *BIAS2* as shown in Figure 6. The *NMOS* mirrors are similarly biased by the same biasing point. This technique insures that devices M_1, M_4, M_7 and M_9 all remain in the saturated region of operation and yet have the minimum drain-to-source voltages possible.

3.1.1 p^+ Diffused Resistor

The next item of interest in the reference circuit is the resistors, R_{ref}, R_1, R_3, and R_4. Simulations have shown that the proper operation of reference devices requires small biasing current in the microampere range. To provide these small currents, resistance values of the order of 10^5 ohms or higher are needed. The only on-chip conductor available in *CMOS* technology that has sufficiently high sheet resistance to render these resistors practical is the p^+ diffusion. The model for the p^+- diffusion resistor used in the analysis and simulation is shown in Figure 7. The sheet resistance of the p^+ diffusion in the 1.75μ twin tub *CMOS* technology is $200\pm50\Omega/\ $. Thus resistor values up to $0.5M\Omega$ can be readily realized. The resistor temperature coefficients have been extracted for the 1.75μ process, where the fit is of the form:

$$R(T) = R(t_0)\left[1 + \frac{TC_1(t-t_0)}{1E6} + \frac{TC_2(t-t_0)^2}{1E6}\right] \tag{3.1}$$

The extracted first-order temperarure coefficient, TC_1 for the p^+ diffusion is $880ppm/^\circ$ C and the second order temperature coefficient, TC_2 was found to be $1ppm/^\circ$ C.

3.1.2 The Reference Diode

The last item of interest in the reference circuit is the reference diode. It is well known that nearly ideal diode characteristics can be obtained from the base-emitter voltage V_{BE} of a bipolar transistor. In *CMOS* technology the lateral *p-n-p* bipolar devices are readily available with p-substrate collector, n-tub base and p^+ emitter.

In the design of the bipolar devices to be used as a reference diode, 5 unit transistors are connected in parallel to make one reference diode (25 unit diodes in total). Using this approach the reference device can operate at large biasing current, and in addition better matching of references can be achieved.

These devices, designed in the 1.75μ linear *CMOS* process, were characterized to obtain the value of parameters n and δ necessary to predict the voltage drop across the reference devices as given in Eq. (2.15).

3.1.3 The Mirroring of the Referenced-Voltage

Other considerations must be analyzed once a suitable reference voltage has been obtained. That is, our application requires the *ECL* input reference voltage V_{BB} be referenced from the same supply rail $(V_{(DD)})$ as the external *ECL* input signals. However, Figure 6 shows this voltage as being referenced from V_{SS}. This leads to the development of a circuit that will allow us to mirror the *DC* voltage V_{BB} referenced from V_{SS} to a voltage referenced from V_{DD}. The circuit is given as part of Figure 6. It consists of two mirror resistors R_3 and R_4, and a current mirror M_{11} and M_{12}.

Assuming that node V_{out} is insulated to prevent DC current leakage and that M_{11} and M_{12} are well matched, the reference current, I_{out} is mirrored to the output through the current mirror M_{11} and M_{12}. In addition, the diode-

connected transistor, M_{11} is used to set the gate-source voltage of the constant-current output device, M_{12}. Resulting in the ideal (first order) equations to be true.

$$V_{BB} = V_7 \tag{3.2}$$

and

$$I_{R3} = I_{R4} = \alpha I_{out} \tag{3.3}$$

where

$$\alpha = \frac{(W/L)_{12}}{(W/L)_{11}} \tag{3.4}$$

The reference current is given as in Eq. (2.15) as

$$I_{out} = \frac{mV_T \ln(n)}{R_{ref}}$$

The voltage across R_4 can be written as

$$V_{R4} = I_{R4} R_4 \tag{3.5}$$

Combining Eqs. (3.3), (3.5), and (2.15), the voltage across R_4 can be written in terms of the device parameters, α, m, and n as

$$V_{R4} = \frac{\bar{k} T R_4}{R_{ref}} \tag{3.6}$$

where

$$\bar{k} = \frac{\alpha m k_B \ln(n)}{q} \tag{3.7}$$

Similarily, the voltage across R_9 can be written as

$$V_{R3} = V_{ref} = V_{DD} - V_{out} = I_{R3} R_3 \tag{3.8}$$

Combining Eqs. (3.3), (3.8), and (2.15) the voltage drop across the resistor R_9 is now

$$V_{ref} = \frac{\bar{k}TR_3}{R_{ref}} \tag{3.9}$$

Taking the ratio of expression given in Eq. (3.6) and Eq. (3.9)

$$\frac{V_{ref}}{V_{R4}} = \frac{R_3}{R_4} \tag{3.10}$$

Using the condition in Eq. (2.40), Eq. (3.10) becomes

$$\frac{V_{ref}}{V_{BB}} = \frac{R_3}{R_4} \tag{3.11}$$

This expression indicates that the reference voltage V_{BB} mirrored from V_{SS} can be mirrored from V_{DD} to obtain V_{ref} by proper sizing of R_3 and R_4. If the ratio R_3:R_4 is unity, ideally V_{BB} is properly mirrored to obtain V_{ref}. However, if the ratio R_3:R_4 is not unity, then V_{BB} is not ideally mirrored and the following conditions must occur. That is

1. R_3:$R_4 > 1$: The magnitude of the output voltage V_{ref} is shifted upward from V_{BB}.
2. R_3:$R_4 < 1$: The magnitude of the output V_{ref} is shifted downward from V_{BB}.

3.1.4 Temperature Coefficient of V_{ref}

Not only is it necessary to mirror the reference current and the magnitude of the reference voltage to the output, but the associated temperature coefficient of V_{BB} also must be mirrored. This leads to the development of an expression for the temperature coefficient of V_{ref}

The TC of V_{ref} is derived by differenating Eq. (3.9). That is

$$m_2 = \frac{\bar{k}R_3}{R_{ref}} \tag{3.12}$$

where

$$m_2 = \frac{dV_{ref}}{dT} \tag{3.13}$$

For a fixed value of m_1, Eq. (3.12) shows that the slope m_2 can be adjusted by:

1. Varying the magnitude of the reference resistor R_{ref}. This is not feasible since R_{ref} is inversely proportional to the reference current I_{out} and directly proportional to the slope m_1.

2. Varying the magnitude of the mirror resistor R_s. However, this does not gaurantee that the slope m_1 is ideally mirrored.

3. Varying the device parameters(α, m_1, and n). Again this is not feasible since the device parameters are directly related to I_{out} and m_1.

However, an expression for the slope of the mirrored reference voltage V_{ref} can be obtained in terms of the slope of V_{BB} by taking the derivative of Eq. (3.10). This is given as

$$m_2 = m_1 \frac{R_3}{R_4} \tag{3.14}$$

where

$$m_1 = \frac{dV_{BB}}{dT} \tag{3.15}$$

Equation (3.14) shows that for a fixed m_1, the output slope m_2 may be influenced by ratio R_3:R_4 in the following manner. If

1. $R_3:R_4 = 1$: The slope m_1 is ideally mirrored to the output. That is $m_1 = m_2$.

2. $R_3:R_4 > 1$: The slope m_1 is mirrored downward from the output slope. That is $m_1 < m_2$.

3. $R_3:R_4 < 1$: The slope m_1 is mirrored upward from the output slope, m_2. That is $m_1 > m_2$.

3.1.5 Simulated Results

The performance characteristics of the *CMOS* reference circuit with cascode current mirrors are summarized in Table 2. The results were obtained through simulation on *ADVICE* [4] using the 1.75μ *CMOS* process. The circuit was simulated over temperature, process and power supply induced variations. The device parameters used in the simulation are listed in Table 6.

The value of NM_L and NM_H shown in Table 2 are calculated using the following definitions:

$$NM_L = V_{ILmax} - V_{OLmax} \tag{3.16}$$

$$NM_H = V_{OHmin} - V_{IHmin} \tag{3.17}$$

where V_{ILmax} and V_{IHmin} values are taken from the Motorola *ECL* catalog for an *ECL* translator. The values for V_{OLmax} and V_{OHmin} are the minimum and maximum output reference voltage generated by the reference circuit. Figure 8 shows that the reference voltage can indeed be centered between V_{ILmax} and V_{IHmin} as illustrated in Figure 2. Since the noise margin low(NH_l is less than the noise margin high(NM_H as given in Table 2, this guarantees that no additional dc gain in the design of the reference circuit is obtainable.

Furthermore, Figure 9 shows that a reference voltage with a very low temperature coefficient is obtainable when the device parameters in Table 6 are slightly modified.

Chapter 4
THE CMOS SWITCH-LEVEL CIRCUIT

4.1 Start-Up Circuit

As mentioned above, unless precautious are taken, the reference circuit may operate in the zero-current state. The zero-current state can be avoided by insuring that some current always flows in the transistors in the circuit so that their current gain does not fall to a low value. An additional requirement is that the circuitry added to do this must not interfere with the normal operation of the reference once the circuit has reached the desired operating point. The additional devices , M_{13}-M_{18} form the start-up circuit for the reference as illustrated in Figure 10. The operation is as follows:

At power up no current is flowing in any of the legs of the circuit. Therefore node 15 gets charged to the value of the power supply by devic M_{14} which is in the triode region of operation. M_{17} and M_{18} then conduct current to flow in device M_{13}. This current is mirrored to M_{16} and pulls charge out of mode 15 turning off M_{17} and M_{18} which disconnects the start-up circuit from the reference.

As shown in Figure 10, the voltage at nodes *BIAS1* and *BIAS2* are used to bias the *PMOS* and *NMOS* cascode current mirrors in the voltage reference circuit given in Figure 6. Also, the voltage at node 16 is used to bias the current sources of the unity gain *CMOS* operational amplifier discussed later and is shown in Figure 12.

4.2 Unity-Gain CMOS Operational Amplifier

The desired *ECL* input reference voltage V_{ref} has been obtained. However, this dc voltage with design variations must be buffered to insure optimum drive to the *CMOS* load of the comparator. Obviously, this buffering is needed to offset the impedance mismatch problem observed between the output of the reference circuit and the input of the voltage comparator circuit. Furthermore, simulation shows that since the reference voltage is measured from the V_{DD} power supply rail which is very sensitive to temperature and process variation, this causes large variations in the reference current which results in insufficient biasing to the comparator. Therefore, in addition the driving capability of the reference current needs to be enhanced. Thus, a unity-gain *CMOS* operational amplifier is implemented. The op-amp must be designed to operate near V_{DD} to guarantee *ECL* compatible logic levels at its output.

Figure 11 shows a two stage noninverting op-amp. The op-amp used as a voltage follower can be designed to insure that the impedance mismatch problem is reduce to yield proper drive capability to the input of the comparator, and that the refernce current is enhanced enough to provide adequate biasing. The first stage of the op-amp is the basic CMOS gain stage with M_{pP3} and M_{p4} as saturated loads, M_{n6} as a constant current source, and M_{n3} and M_{n4} as the differential inputs. If the inputs of M_{n3} and M_{n4} are grounded, then the quiescent output voltage at the drain of M_{p3} is equal to the voltage at the drain of M_{p4} (M_{p3} and M_{p4} have the same drain current and gate-source voltage and hence must have the same drain-source voltage). However, the value of the gate voltage of M_{p5} that is required to force the amplifier output voltage to zero may be different from the quiescent output voltage of the first stage. For a first stage

gain of *50*, for example, each *50mV* difference in these voltages results in *1mV* of input-referred systematic output. Thus the β of M_{p3} , M_{p4} and M_{p5} must be chosen so that the current density in these devices are equal. For the first stage shown in Figure 11, this constraint would take the form [5].

$$\frac{\beta_{p3}}{\beta_{p5}} = \frac{\beta_{p4}}{\beta_{p5}} \tag{4.1}$$

In order that this ratio be maintain over process-induced variations in channel length, the channel lengths of M_{p3}, M_{p4}, M_{p5} were chosen to be the same, and the ratios were provided by properly chosing the channel widths.

A second gain stage source-follower or common-drain configuration is added to insure that the op-amp operates near V_{DD} and provides proper impedance matching between the reference voltage circuit and the op-amp. As shown in Figure 12, the transistor pairs of M_{n1}-M_{n5} and M_{n2}-M_{n7} serves as the source-follower. This circuit is used primarily for the purpose of lowering the impedance level in the signal path, since its low-frequency input impedance is very high and its low-frequency output impedance is approximately equal to the inverse of the device transconductance. In contract to the bipolar case, however, it can be applied to the *ECL* reference dc voltage, V_{BB}, since the dc voltage drop between the gate and source can be made large, and can be controlled by the β of the device and the bias current.

Further insight about the voltage gain of the op-amp can be obtained by analyzing the voltage gain of the source follower. This can be done by using the small-signal equivalent circuit given by [6]. If no body effect were present, and if the load resistance of M_{n5} and M_{n7} were infinite, voltage gain from input to output would be unity. However, the presence of body effect causes the threshold to vary with output voltage in such a way as to make the gain less

than unity. The smaller the body effect is, the closer the voltage gain will be to unity. In the 1.75μm *CMOS* technology, the n-channel device is formed in a p-well on a p-substrate. Hence, if the device is used as a source-follower and the p-well is tied to the source, the body effect is eliminated and the unloaded voltage gain is unity.

The open loop-gain is set by the β of the output stage, M_{p5}. The gain increase as β_{p5} increases and falls off as β_{p5} decreases . In addition, the β of transistor M_5 was made large to insure proper drive capability to the CMOS load and to minimize impedance mismatch as shown in Figure 11. The current sources of the op-amp M_{n5}, M_{n6}, and M_{n7} are biased by node 16 as given in Figure 10.

The performance characteristic of the unity-gain op-amp is shown in Table 1. The results were obtained through simulation on *ADVICE* using the 1.75μm *CMOS* process.

4.3 The Comparator Circuit

Figure 12 shows an unique schematic of a single-ended input, single-ended output inverting mode of a differential amplifier used as a very-high-speed voltage comparator. The output swing and dc levels are adjusted to be compatible with conventional *CMOS* logic circuits.

The functions of the voltage comparator is to compare the instataneous value of a signal voltage at one input with a reference voltage on the other input and produce a digital 1 or 0 level at the output when one input is higher than the other.

Since the comparator output is switched between two output states, the voltage gain is necessary only to reduce the differential input level charge

needed to make the output swing from one extreme level to another. To interface with digital *CMOS* circuits, the required peak-to-peak output swing levels are in the range of *3-5V*. Therefore, a voltage gain of ≥ 100 is usually sufficient to bring the input signal amplitude needed for full output swing to a level comparable with the input stage offset. Therefore, very high values of voltage gain are not required.

The speed of response is a critical parameter for this comparator. It is required to switch between two output states in a minimum amount of time, subsequent to an appropriate input level change, and it should exhibit fast rise and fall times as its output.

The operation of the comparator circuit can be briefly described as follows. The comparator has two gain-stage and two stages of level- shifting. The first-gain stage comprised of transistors M_{p1} and M_{p2} forms a single-ended input gain stage with balanced current mirror loads M_{n1} and M_{n2}. The output of the first-gain stage may be viewed as a source-follower, withM_{p2} as the p-channel gain stage and M_{n2} as the n-channel current mirror load. Also, this configuration can be employed as a DC level shifter, since the dc voltage drop between the gate and source can be made large and can be controlled by the device geometry and bias current. The level shifting capabilities of the source follower shifts the source voltage of M_{p2} negatively if large output signal swings are to be obtained. The source-follower is used primarily for the purpose of lowering the impedance level in the signal path, since its low-frequency input impedance is very high and its low-frquency output impedance is approximately equal to the inverse of the device transconductance.

The second-gain stage is connected as a common-source amplifier comprised

of the n-channel gain stage, M_{n4} and the current-mirror load M_{p4} and M_{p5}. The current sources M_{n5} is biased by the diode connected transistor M_{p5a} and M_{n5a}. In addition, the circuit serves as a dc level-shifter. The required shift between the gate of the gain stage and the drain voltage of M_{n4} is provided by the gate-to-source voltage of M_{n4}. The output of the second stage is the desired *CMOS* output levels.

4.3.1 DC Level-Shift Stages

Since large-value coupling capacitors are not available in monolithic circuits, all high gain stages need to be dc coupled. This means that the output dc level of a gain stage should be compatible with the dc level at the input of the next stage. In a source follower gain stage, the output dc level is always higher than the dc level of the input. Therefore, if a number of such gain stages are cascaded, the output dc level rapidly builds up toward the positive supply voltage. This in turn limits the amplitude and the linearity of the available output swing. Ideally, such a dc level buildup can be avoided by using complementary (n-channel and p-channel) gain stages. The comparator circuit given in Figure 12 employs this concept. The output of the first gain stage V_B, is at a more positive voltage level than the input signal. Thus, after one or two stages of gain, the output dc level has to be level shifted toward the negative supply with minimum attenuation of the ac signal. Since there are no practical resistor values available in *CMOS* analog design, this level shifting must be accomplished solely with active devices.

One simple and often used level-shift device is the grounded-gate gain stage shown in Figure 12, which provides a dc level shift, in addition to serving as an unilateral buffer. Therefore, it is required to have a high input im-

pedance and a relatively low output impedance to prevent interstage loading.

We can determine the amount of shifting needed to level-shift the dc source voltage, V_{in} to a more negative dc level, V_D by analyzing the dc shifting capability of each stage individually.

If we operate the devices in the subthreshold region where an acceptable amount of gain is obtainable; set $V_{ref}=V_{in}$, and observe that the diode connected n-channel load M_{n1} forces the gate-to-source voltage equal to the drain-to-source voltage of M_{n1}. Thus, the current through the p-channel gain stage and the n-channel current mirror load can be expressed as

$$I_{DSp2}=\frac{\beta_{p2}}{2}[-V_{in}-V_{tP2}]^2 \tag{4.2}$$

and

$$I_{DSn2}=\frac{\beta_{n2}}{2}[V_B-V_{tn2}]^2 \tag{4.3}$$

where I_{ds} is the drain-source current, V_{gs} is the gate-to-source voltage, V_t is the device threshold, and β is the MOS transistor gain factor.

Since both devices are operating in the saturation region, M_{p2} and M_{n2} act as two current source in series. Therefore,

$$I_{out}=I_{DSp2}=I_{DSn2} \tag{4.4}$$

Combining Eqs. (4.2), (4.3), and (4.4), the first-stage output voltage may be expressed as

$$V_{in}=|V_{tdp2}|+\sqrt{\frac{\beta_{n2}}{\beta_{p2}}}(V_{tn2}-V_B) \tag{4.5}$$

$$V_B=V_{tn2}+\sqrt{\frac{\beta_{p2}}{\beta_{n2}}}(|V_{in}|+|V_{tp2}|) \tag{4.6}$$

Similarly, the output of the second-stage of gain can be found by observing that

the diode p-channel load forces

$$V_C = V_D \tag{4.7}$$

The current through the n-channel gain stage and the p-channel load is given as

$$I_{DSp4} = \frac{\beta_{p4}}{2}(V_D - V_{DD} - V_{tp4})^2 \tag{4.8}$$

$$I_{DSn4} = \frac{\beta_{n4}}{2}(V_B - V_{tn4})^2 \tag{4.9}$$

By setting

$$I_{DS} = |I_{DSp4}| = I_{DSn4} \tag{4.10}$$

We can obtain an expression for the output stage voltage by combining Eqs. (4.8), (4.9) and (4.10). This results in

$$V_D = \sqrt{\frac{\beta_{n4}}{\beta_{p4}}}(V_B - V_{tn4}) + (V_{DD} - |V_{tp4}|) \tag{4.11}$$

Substracting Eq. (4.5) from Eq. (4.11), we can find the overall net level shift, V_{in}-V_D. That is, the amount in which the output gain stage have been shifted from input voltage level.

The overall net level shift becomes

$$V_{in} - V_D$$

$$= \left[|V_{tp2}| + |V_{tp4}| - V_{DD}\right] + \left[\sqrt{\frac{\beta_{n2}}{\beta_{p2}}}(V_{tn2} - V_B) + \sqrt{\frac{\beta_{n4}}{\beta_{p4}}}(V_{tn4} - V_B)\right] \tag{4.12}$$

If we set the gain factor of the first-stage and second-stage equal, that is

$$\beta_{n2} = \beta_{p2} \tag{4.13}$$

and

$$\beta_{n4} = \beta_{p4} \tag{4.14}$$

Then, Eq. (4.12) becomes

$$V_{in} - V_D = [|V_{tp2}| + |V_{tp4}| - V_{DD}] + [V_{tn2} + V_{tn4} - 2V_B] \tag{4.15}$$

The possible values of V_{in}- V_D in the saturation region can be deduced as follows:

1. $V_{in}-V_D=0$: No dc level shift.
2. $V_{in}-V_D<0$: Negative dc level shift.
3. $V_{in}-V_D>0$: Positive dc level shift.

If properly designed, the two dc level-shifting circuits employed in Figure 12 can provide substanial voltage gain, high input impedance, low output impedance, and an output swing nearly equal to the supply voltage, in addition to the desired shift in dc level.

4.3.2 Voltage Gain Considerations

The overall voltage gain of the comparator can be found by considering the two stage separately, since no loading of the first-stage by the second occurs because of the essentially infinite input resistance of the *MOS* devices.

Figure 12 shows the first-stage of the *CMOS* single-ended high-gain amplifier stage can be briefly explained as follows. The p-channel device, and M_{p2} operates as a grounded-gate gain stage, and drives the opposing n-channel current mirror load made up of the pair M_{n1} and M_{n2}. The current mirror output current is determined by the bias current source, I_{out} when M_{n2} and M_{p2} are in the saturation region. If the gate-to-source voltage of M_{p2}, V_{in} is increased beyound V_{ref}, M_{p2} begins to conduct; however M_{n2} stays in the triode region until the current through M_{p2} is approximately equal to I_{out}. At this point, both transistors, M_{N2} and M_{P2} are in the saturation region and operates as two current sources in series. If the inputs of the first-stage are grounded and

$V_{ref}=V_{in}$, then the quiescent output voltage at the drain on M_{N2} is equal to the voltage at the drain of M_{N1} (M_{N1} and M_{N2} have the same drain current and gate-source voltage and hence just have the same drain-source voltage).

For our application, the amplifier stage is biased in the region where both devices are active and the circuit has a high small-signal gain.

Setting the small-signal input shunt resistance, r_π to infinity, the available voltage gain of the first-stage can be given as [6]

$$A_{V1} = \frac{g_{m(Mp2)}}{g_{0(Mp2)} + g_{0(Mn2)}} \tag{4.16}$$

where $g_{m(Mp2)}$ is the transconductance of the input transistor and $g_{0(Mp2)}$ and $g_{0(Mn2)}$ are the small-signal device output conductance of M_{p2} and M_{n2}.

The small-signal device output conductance can be approximated as

$$g_{0(Mp2)} = \frac{I_{out}}{V_{A1(Mp2)}} \tag{4.17}$$

and

$$g_{0(Mn2)} = \frac{I_{out}}{V_{A2(Mn2)}} \tag{4.18}$$

where $V_{A1(Mp2)}$ and $V_{A2(Mn2)}$ are the intercept voltages for M_{p2} and M_{n2}. The intercept voltages depend on the channel length of the respective devices and can be increased by making the channel length larger, that is, by using so-called long-channel devices.

The transconductance $g_{m(Mp2)}$ is given as

$$g_{m(Mp2)} = \sqrt{2 I_{out} \mu_p C_{ox} (W/L)_{Mp2}} \tag{4.19}$$

where W is the channel width, L is the effective channel length, C_{ox} is oxide capacitance, and μ_P is the hole mobility.

Assuming no loading effects on the output of the first-stage and since both

M_{n2} and M_{p2} are in series as shown in Figure 13, $I_{out}=I_{D(Mn2)}=I_{D(Mp2)}$, and the first-stage gain can be written from Eq. (4.17) and Eq. (4.19) as

$$A_{V1} = \frac{1}{\sqrt{I_{out}}} \frac{|V_{A,Mn2}||V_{A,Mp2}|}{|V_{A,Mn2}| + |V_{A,Mp2}|} \sqrt{2\mu_p C_{ox}(W/L)_{Mp2}} \tag{4.20}$$

Simulation shows that by using a grounded-gate gain stage, the small-signal voltage gain is maximized. With practical bias levels and device geometries, typical voltage gains obtainable from such gain stages are in the range of 100-1000. The available values of gain can be increased to the range of 1000-10,000 by using a more complex current source(such as the Wilson current mirror) for M_{n1} and M_{n2}. Yet, it should be noted that the total available gain is still approximately an order of magnitude lower than that of a bipolar stage because of the lower values of transconductance, g_m.

Similary, the small-signal voltage gain of the second-stage amplifier can be analyzed. The most commonly used *CMOS* gain stage is the basic *CMOS* inverter, where one device serves as a common-source amplifier and the other device acts as an active load. Figure 12 shows the circuit configuration for such a stage For illustrative purposes, an n-channel device is used as the gain stage, with a p-channel current mirror as its active load.

The operation of the circuit can be briefly explained as follows. M_{p3} and M_{p4} form a current mirror whose output current is determined by the bias current source of M_{n3}, I_C when M_{p4} is in its saturation region. If the input voltage V_B is less than the threshold voltage $V_{T(Mn4)}$ of the n-channel device, then M_{n4} is nonconducting and M_{p4} is in its triode region with virtually a zero voltage drop across it. If V_B is increased beyond $V_{T(Mn4)}$, M_{n4} begins to conduct; however M_{p4} stays in its triode region until the current through M_{n4} is approximately equal to I_C. At this point, M_{p4} leaves the triode region and enters

its saturation region. This corresponds to a region where both M_{n4} and M_{p4} are in their saturation regions and operate as two current sources in series. If the input voltage is increased further, M_{p4} stays in its saturation region and M_{n4} is pushed into its triode region with a very low voltage drop across its source-drain terminals. This corresponds to a region where any further increase in V_B will result in a negligible change of output voltage.

For our applications, the inverter stage is biased in the saturation region where both devices are active and the circuit has a high incremental (i.e., small-signal) gain.

The incremental voltage gain for the circuit, for its operation in the saturation region, can be calculated from the small-signal model of the *MOS* transistor [6] as

$$A_{V2} = \frac{-g_{m(Mn4)}}{g_{0(Mn4)} + g_{0(Mp4)}} \tag{4.21}$$

where $g_{0(Mn4)}$ and $g_{0(Mp4)}$ are the output conductances of M_{p4} and M_{n4}, and are due to the channel length modulation effects. As indicated by Eq. (8.82), they can be approximated as

$$g_{0(Mn4)} = \frac{|V_{A1(Mn4)}|}{I_{D(Mn4)}} \tag{4.22}$$

and

$$g_{0(Mp4)} = \frac{|V_{A(Mp4)}|}{I_{D1(Mp4)}} \tag{4.23}$$

where $V_{A(Mn4)}$ and $V_{A(Mp4)}$ are the intercept voltages for M_{p4} and M_{n4}.

The transconductance $g_{m(Mn4)}$ is given from Eq. (4.19) as

$$g_{m(Mn4)} = \sqrt{2\mu_n C_{ox}(W/L) I_{DS}} \tag{4.24}$$

Since both transistor M_{n4} and M_{p4} can be assumed to be in series in Figure 12,

$I_D = I_{D(Mn4)} = I_{D(Mp5)}$, and the incremental gain can be written from Eq. (4.22) and Eq. (4.24) as

$$A_{V2} = \frac{1}{\sqrt{I_D}} \frac{|V_{A(Mn4)}||V_{A(Mp4)}|}{|V_{A(Mn4)}| + |V_{A(Mp4)}|} \sqrt{2\mu_n C_{ox}(W/L)_{Mn4}} \tag{4.25}$$

Neglecting the interstage loading effects, the overall voltage gain of the comparator is given by combining Eqs. (4.25) and (4.20)

$$\begin{aligned} A_V &= A_{V1} \, x \, A_{V2} \\ &= \frac{2C_{ox}}{\sqrt{I_C}} \frac{|V_{A,G}|}{|V_{A,L}|} \sqrt{\mu_C (W/L)_g} \end{aligned} \tag{4.26}$$

where

$$I_C = I_D I_{out} \tag{4.27}$$

$$V_{A,G} = |V_{A(Mp2}|) \, x \, |V_{A(Mn4)}| \, x \, |V_{A(Mn2)}| \, x \, |V_{A(Mp4)}| \tag{4.28}$$

$$V_{A,L} = |V_{A(Mn2)}| + |V_{A(Mn4)}| + |V_{A(Mn4)}| + |V_{A(Mp2)}| \tag{4.29}$$

$$\mu_C = \mu_n \mu_p \tag{4.30}$$

and

$$(W/L)_g = (W/L)_{MN4} \, x \, (W/L)_{Mp2} \tag{4.31}$$

From Eq. (4.26) one can draw the following conclusions.

1. The available overall incremental gain varies inversely with the square root of the drain currents. This is because the transconductance decreases with the square root of I_C, whereas the output resistance r_0 is inversely proportional to I_C. Therefore, the product shows an inverse square-root dependence of I_C and thus, higher gain can be achieved by operating the stages at lower bias currents. However, if the drain current is reduced to extremely low levels (i.e., $I_0 \leq 0.1$ μA), then both M_{n4} and M_{p2} are very nearly cutoff. In this very low current range of operation, where the conductive channel is barely at the verge of exiting, the basic transconductance [Eq. (4.24)] is no longer valid. Instead, g_m exhibits a linar dependence on I_C in a manner similar to the case is reduced low enough to bring the devic to its subthreshold region, the gain levels off and becomes relatively constant with current.

2. At any given current level, one can increase the available voltage gain by increasing the channel lengths of M_{n4} and M_{p2}, which causes V_A of each of the devices to increae. However, increasing L_{Mn4} also has a detrimental effect since it trends to reduce $g_{m(Mn4)}$, unless the W/L ratio of M_{n4} is maintained constant. In terms of frequency response characteristics, using long channel devices is not desirable since this increases the gate-channel capacitance of both M_{n4} and M_{p2}.

For the comparator applications, the overall voltage gain that is required is on the order of several hundred, implying a gain in each stage on the order of *50*. In order to achieve this level of gain per stage, one usually chooses transistors bias currents and channel lengths and witdhs such that the value of the transistor $(V_{GS}\text{-}V_T)$ is several hundred millivolts, and the drain depletion region is on the order of one-fifth or less of the effective channel length att he typical drain bias of several volts. This gives a gain on the order of *50*.

Simulation shows that the comparator provides a nominal voltage gain of approximately 100 with a bandwidth of approximately *88MHz*. Its response time was found to be less than *5ns* with *4-mV* overdrive.

4.3.3 Switching Capabilities

A basic *ECL* switch is shown in Figure 12. While this circuit is the basic building block for the *ECL-To-CMOS* translator system, it is also the basic comparator configuration used widely in modern linear integrated circuit. In this section, we will discuss the parameters that will effect the switching capabilities of the comparator circuit shown in Figure 12.

Generally, the switching speed of a circuit is the time it takes for a circuit to go from one extreme level to another, and the level are set by the output swing of the power supply. Thus, the switching speed of the camparator circuit is expected to be very fast since the output swing of the *ECL* input signal is

small, *0.8V*. Before preceeding, let us define the logic levels for an *ECL* system. First, a logic 1 is defined as the most positive voltage level of the input signal and a logic 0 as the most negative. The opposite convention(most positive=logic 0 and most negative=logic 1) could also be used. Practice, however, has favored the positive notation, which will be used in our analysis.

With the logic swing given at *0.8V*, the input/output levels were given to be ≈*-0.7V* and ≈*-1.9V* with respect to ground at room temperature, for both compensated and uncompensated products.

The two primary factors that determine the switching performance of the voltage comparator is the individual *IC* delays and the associated wiring delays. The individual *IC* delays of the comparator can be altered in several different ways. First, by increasing the supply voltage, we may increase the speed. In a like manner increasing the load capacitance decreases the comparator speed. The speed of the comparator also may be increased by increasing the size of the comparator structure. As *W/L* increases, the speed also increases. A limiting speed is eventually reached; that is, where increasing this ratio will not contribute to an additional increase in speed.

Care was taken to insure the signal wiring capacitance was held to a minimum. This was done by using metal wire as interconnection between each gain stage. The sheet resistance of metal is given in Table 10 and is very low compare to that of polysilicon. The problem of capacitance loading is another contributing factor to wiring delays. For every wire used as interconnection, there exists an associated capacitance. Simulation shows that the most contributing capacitance that degrades the speed of the comparator was the capacitance at node B. As mentioned, one way of overcoming this problem is by

increasing the W/L ratio of the individual device. However, clever layout techniques can also be employed. One technique used is the diffusion sharing method. This is used when a very large device is needed. The devices are stacked in parallel to decrease the area of the drain diffusion. The area of the source is also reduced, but if the source of the device is tied to the power supply, no switching occurs at the node because no capacitance exists. By using this technique, *ADVICE* shows that the speed of the comparator was slightly improved.

The number of *IC* loads driven by the output of the comparator(fanout) can also add to the fundamental delays of the circuit. Figure 12 shows that the comparator has a fanout of only one and is designed to properly drive this standard *CMOS* inverter.

The performance characteristics of the comparator is illustrated in Figure 13. The rise and fall times were defined as the time required for V_D to rise from 20 to 80% of V_{DD}, and the fall time is defined as the time required for V_D to fall from 80 to 20% of V_{DD}. One should note that these measurements are different from the conventional measurements of 10 and 90%. For a balanced comparator, the output rise and fall time is approximately equal.

The other parameter is the propagation delay time from input(V_{in}) to output(V_D). Propagation delays time is inherent in logic gates of all types and is measured between the 50% points of the input and output waveforms.

In conclusion, a comparator used as an *ECL* switch has been designed. The comparator is capable of driving like stages over a wide range of temperature-0 to 75° C(commerical grade)- with power supply voltage ranges of typically ± 5% about the *5.2V* nominal supply rail. The circuit was found to

exhibit performance characteristics similar to that of an *ECL* circuit.

4.3.4 Output Load

The load which the comparator has to drive is a basic *CMOS* inverter stage. The inverter is given as part of Figure 12. In this configuration, the p-channel device source is connected to V_{DD} and the n-channel device source to V_{SS}. Their gates are tied together to form the inverter input, and the drains form the common output. In addition, both devices are isolated from each other by being placed in two different tubs. Another way to insure isolation between the two device is to bias the p-substrate to V_{SS}, commonmly grounded and the n-tub to V_{DD}. This provides a reverse-biased *pn* junction between devices.

The threshold voltage for the p-channel transistor(V_{tp}) and for the n-channel transistor(V_{tn}) are not equal and is given in Table 10 for the $1.75\mu m$ process.

The circuit operation is as follows. M_{p5} acts as the active load of the inverter and M_{n5} serves as the gain stage. For small values of V_D and less than V_{tp}, M_{n5} is completely off and no current flows through it. Output voltage, V_{out} equals V_{DD} under this condition, because M_{ps} is fully turned on and is in its linear region of operation. As V_D increases above V_{tn}, both devices enter their saturation regions. As V_D is further increased, V_{out} drops to V_{SS} and M_{n5} becomes fully on, conducting in its linear region;M_{p5} is completely off.

In the design of the *CMOS* inverter, the W/L ratio of the p-channel transistor is sized to be 2 time greater than that of the n-channel transistor. The mobility of electrons is typically greater than the mobility of holes, the effective carrier in the p-channel device, by this amount. This is done to achieve a

more balanced switching speed by making the inverter's output rise and fall times essentially the same. One should note that it is the W/L of the p-chanel device that governs the pull-up capability and the W/L of the n-channel device that controls the pull-down capability of the output node, V_{out}

The performance characteristics at the inverter output is shown in Figure 14, and is found to be favorable to *ECL* compatible systems.

Chapter 5
Circuit Performance

5.1 Output Voltage Sensitivity

Before presenting the simulated results of the translator, a brief discussion of the sensitivity of the translator output due to variants in processing, temperature and power supply will be presented.

The main processing parameters which affect the output of the translator system are: p^+-diffusion doping, resistor mismatch in the voltage mirroring circuit, reference diode mismatch, and the threshold mismatch of the reference current mirrors, the op-amp and the voltage comparator input devices. The threshold mismatch, which results in the current mirrors, the op-amp and the voltage comparator offset error, mainly affects the magnitude of the output voltage if the offset itself is not a function of temperature. All other processing variations affect magnitude, as well as the temperature compensation of the output.

The doping of the p^+-diffusion affects the resistance of the biasing resistors and the V_{be} drop across the reference diodes. Both the value of the biasing resistor, and the B_{be} drop across the reference devices affect the reference voltage, V_{ref} of the reference circuit.

The mismatch of the resistor ratio R_3 and R_4 affect the accuracy of the reference voltage mirror. The mismatch of the ratio R_{ref} and R_1 influence the current ratio supplied to the reference, and thus the different between V_{BB} and V_{ref}

In a similar manner, the main temperature and power supply parameters

which affect the output of the translator system are: the effective mobility, p^+-diffusion doping and the threshold mismatch problem.

The variations in the effective mobility is due to changes in temperature. This variation causes error in the drain-to-source conductance which results in an additional error term in the reference current definition.

The affect of temperature on the p^+-diffusion resistor is the same as that described for process induced variations.

Since the threshold voltage is directly proportional to variations in temperature, any changes in temperature will result in error terms in the reference current equation and the associated reference voltage expression. Furthermore, a change in threshold voltage will cause an offset error to occur in both the op-amp and the voltage comparator circuit. Most importantly, changes in threshold due to temperature variations has a detrimental affect on the switching performance of the voltage comparator.

In addition, the threshold voltage is also affected by power supply variations. This is so because the threshold voltage is proportional to the source-to-body voltage of a *CMOS* device. If the source-to-body voltage is not shorted together, and the source of the device is tied to the power supply, any variations in the power supply voltage will result in changes to the threshold voltage which as explained, have a remote affect on many of the device and circuit parameters.

The p^+-diffusion resistors used in the reference circuit are formed inside a n-well. Normally, the n-well is tied to V_{DD}. Thus any variations in the power supply voltage will result in the biasing point of the well to be biased at different potentials.

All of the parameters discussed above have an affect on the translator output. However, the *1.75μm* twin-tub process at *AT&T* is well controlled and can guarantee a reasonable margin of error in the inaccuracy of each parameter. The regulations of each parameter is given in Table 10.

5.2 Simulated Results

The system as shown in Figure 1 has been extensively simulated using *ADVICE* [4]. These results are now presented.

First on interest is the temperature performance of the reference at a nominal power supply voltage of *5.2* volts. The results of such a simulation are shown in Figure 8. An examination of the data points allows the circuit performance to be given in Table 2 . Table 6 gives a listing of the device parameters used in the simulation of this circuit. Furthermore, Figure 9 shows that a reference voltage can be obtained with nearly a zero temperature coefficient if so desired. The device parameters of this circuit is given in Table 6.

Next the voltage performance of the reference was evaluated. A dc sweep of the power supply and the resultant effect upon V_{ref} is also found in Figure 8. As is seen in Figure 2 the reference maintains regulation down to power supply values as low as 4.0 volts. At values below 3.5 volts, convergence problems were encountered. This often indicates instability, especially in high gain feedback circuit of this type. By examining the data points of Figure 8, it was seen that that for 4.5 volts of power supply variation the output changed less than *14mV*. Thus, for a *90%* variation in power supply, the output changed about *1.5%*. This corresponds to a dc power supply rejection of *-41.86dB*.

Last to be evaluated was the switching characteristics of the translator at power supply voltage of *5.2± 5%*, temperature variations of *0 - 75° C* and

process induced variations. The simulation for a worst-case analysis is shown in Figure 14. The switching characteristics(rise time, fall time, and propagation delays) of the system is given in Table 3 for worst-case. After analyzing all the data points, the worst-case was observed to be at high-voltage($5.46V$), high-gain(V_{tp}=$1.3V$ *and* V_{tn}=$0.9V$), and high-temperature(75° C). Based upon the results in Table 3 it seem that the translator should perform extremely well when interfaced with a *CMOS* integrated circuit.

Chapter 6
CONCLUSIONS

The design of a simple and practical precision *ECL-To-CMOS* input buffer has been quantitatively analyzed. A description of the system and some of the design considerations involved in its development has been presented. The magnitude and temperature stability of the *CMOS* output levels is shown to be tolerant to the most common variations of the *CMOS* process. Designed in the standard digital *1.75 μm CMOS* technology, the performance of the system is found to exhibit propagation delays as small as *1.2ns*, and rise and fall times as low as *0.2ns* which is conceivable for *ECL* compatible circuits. This data maintains regulation over a power supply range of *5.2 $\pm$ 5%* and a temperature range of *0 to 75 $^{\circ}$ C.*

This translator should prove useful in interface with *CMOS* designed circuits. The dramatic improvement in the performance can be achieved if the now being developed *BIMOS* process were available.

Table 6-1: Performance Characteristics of the Unity-Gain Op-Amp

Parameter	Unit	Performance
Power Supply Variation	V	4.94 - 5.46
DC Gain	dB	≥ 1
Temperature Range	$^{\circ}C$	0 - 75
Input Offset Voltage	mV	25
PSRR	dB	-42.88 - -36.59
Unity-Gain Bandwidth	MHz	17 - 55
Phase Margin	$Degree$	39.01 - 88.13

Table 6-2: Performance Characteristics of the CMOS Reference Circuit

Parameter	Unit	Performance
Power Supply Variation	V	*4.94 - 5.46*
Temperature Range	$^{\circ}C$	*0 - 75*
Process Variation	mV	*0.5 - 27.4*
PSRR	dB	*-41.86 - -29.60*
Reference voltage dc range	V	*-1.3507 - -1.2184*
Temperature Variation	$mV/^{\circ}C$	*0 - 1.2733*
NM_L	mV	*129.3*
NM_H	mV	*148.4*
$V_{ref}(25^{\circ}C)$	V	*1.3047*

Table 6-3: Performance Characteristics of the ECL-To-CMOS Translator

Parameter	Unit	Performance
Power Supply Variation	*V*	*4.94 - 5.46*
Temperature Range	$^{\circ}C$	*0 - 75*
Reference Current, I_{PTAT}	μA	*9*
Nominal Voltage Gain	V/mV	< 1700
Propagation delay, t_{pd}	*ns*	*1.938 - 4.55*
Rise time, t_r	*ns*	*0.3816 - 0.5194*
Fall time, t_f	*ns*	*0.5324 - 0.8249*
Small-Signal Bandwidth	*MHz*	*83.5 - 100*
Pulse-Width Distortion	*ns*	*0.026 - 0.732*
Input Offset Voltage, V_{os}	*mV*	*-8.65 - 0.35*
ECL Input Logic Swing Level	*V*	*0.8*

Table 6-4: Summary of Circuit, Device and Physical Parameters

Parameter	Unit	Result
Temperature Range	$^{\circ}C$	*0 - 75*
Current β ratio,m		*1*
Area factor,n		*5*
Bandgap Voltage,V_{G0}	*V*	*1.20595*
Reference Current,I_{PTAT}	μA	*10*
Mobility exp,δ		*1.775*
Resistor TCF,$TCF(R_{ref})$	$1/^{\circ}$ *K*	$880x10^{-6}$
Thermal Voltage,V_T	*mV*	*25.73*

Table 6-5: Device Paramaters for the CMOS Referenced Biasing Circuit

Parameter	Unit	Value
Current β ratio, m		*1*
Area factor, n		*5*
Reference Resistor, R_{ref}	kΩ	6
Slope Resistor, R_1	kΩ	36.421
$(W/L)_{M1}$	$\mu m/\mu m$	96/12
$(W/L)_{M2}$	$\mu m/\mu m$	96/12
$(W/L)_{M3}$	$\mu m/\mu m$	20/4
$(W/L)_{M4}$	$\mu m/\mu m$	20/4

Table 6-6: Device Paramaters for the CMOS Referenced Biasing Circuit using current mirrors.

Parameter	Unit	Value
Current β ratio, m		*1*
Area factor, n		*5*
Reference Resistor, R_{ref}	kΩ	6
Slope Resistor, R_1	kΩ	36.421
Mirror Resistor, R_3	kΩ	309.24
Mirror Resistor, R_4	kΩ	200
$(W/L)_{M1}$	$\mu m/\mu m$	96/12
$(W/L)_{M2}$	$\mu m/\mu m$	96/12
$(W/L)_{M9}$	$\mu m/\mu m$	96/12
$(W/L)_{M10}$	$\mu m/\mu m$	96/12
$(W/L)_{M11}$	$\mu m/\mu m$	96/12
$(W/L)_{M12}$	$\mu m/\mu m$	120/12
$(W/L)_{M3}$	$\mu m/\mu m$	20/4
$(W/L)_{M4}$	$\mu m/\mu m$	20/4
$(W/L)_{M5}$	$\mu m/\mu m$	20/4
$(W/L)_{M6}$	$\mu m/\mu m$	20/4
$(W/L)_{M7}$	$\mu m/\mu m$	20/4
$(W/L)_{M8}$	$\mu m/\mu m$	20/4

Table 6-7: Device Paramaters for the Start-Up Circuit

Paramete	Unit	Value
$(W/L)_{M13}$	$\mu m/\mu m$	20/4
$(W/L)_{M14}$	$\mu m/\mu m$	1.5/41
$(W/L)_{M15}$	$\mu m/\mu m$	20/4
$(W/L)_{M16}$	$\mu m/\mu m$	20/4
$(W/L)_{M17}$	$\mu m/\mu m$	400/2
$(W/L)_{M18}$	$\mu m/\mu m$	400/2

Table 6-8: Device Paramaters for the Unity-Gain CMOS Op-amp

Paramete	Unit	Value
$(W/L)_{Mn1}$	$\mu m/\mu m$	18.48/2.25
$(W/L)_{Mn2}$	$\mu m/\mu m$	18.48/2.25
$(W/L)_{Mn3}$	$\mu m/\mu m$	20/2.25
$(W/L)_{Mn4}$	$\mu m/\mu m$	20/2.25
$(W/L)_{Mn5}$	$\mu m/\mu m$	18.48/2.25
$(W/L)_{Mn6}$	$\mu m/\mu m$	20/2.25
$(W/L)_{Mn7}$	$\mu m/\mu m$	18.48/2.25
$(W/L)_{Mp3}$	$\mu m/\mu m$	20/2.25
$(W/L)_{Mp4}$	$\mu m/\mu m$	20/2.25
$(W/L)_{Mp5}$	$\mu m/\mu m$	60/2.25

Table 6-9: Device Paramaters for the voltage-comparator circuit

Paramete	Unit	Value
$(W/L)_{Mp1}$	$\mu m/\mu m$	5/2.25
$(W/L)_{Mp2}$	$\mu m/\mu m$	5/2.25
$(W/L)_{Mp3}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mp3a}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mp4}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mp5}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn1}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn2}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn3}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn3a}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn4}$	$\mu m/\mu m$	10/2.25
$(W/L)_{Mn5}$	$\mu m/\mu m$	10/2.25

Table 6-10: 1.75μm Process Specification

Parameter	Unit	value
p^+ sheet resistance	$\Omega/$	200± 50
n^+ sheet resistance	$\Omega/$	25± 5
Alum sheet resistance	$\Omega/$	.04± .01
Poly sheet resistance	$\Omega/$	3.0± 1
p-chan. threshold,V_{tn}	V	0.7± 0.2
n-chan. threshold,V_{tp}	V	1.1± 0.2
Channel length,L_{effp}	μm	1.3± 0.3
Channel length,L_{effn}	μm	1.3± 0.3
Resistor TCF	$ppm/^\circ C$	880
Oxide thickness,t_{ox}	A	250± 25
p-well dose,N_B	$/cm^2$	4E12
n-well dose,N_P	$/cm^2$	5-6E12

Figure 1 *A Block Diagram of the ECL-To-CMOS Translator*

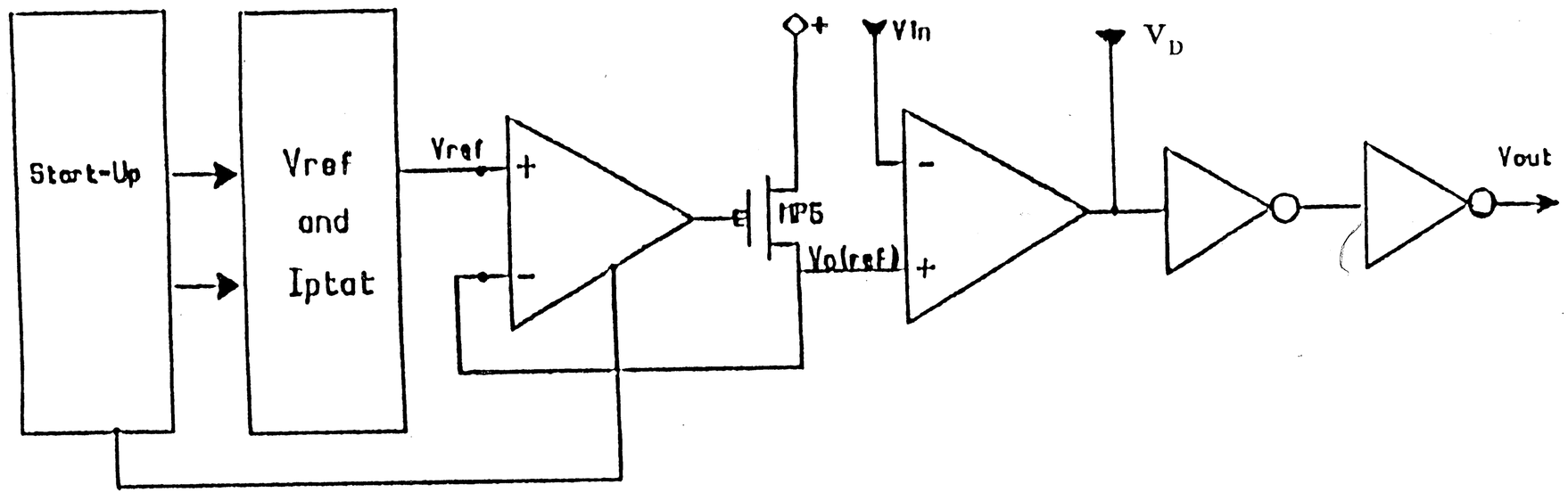


Figure 2 *The Required ECL Input Specifications*

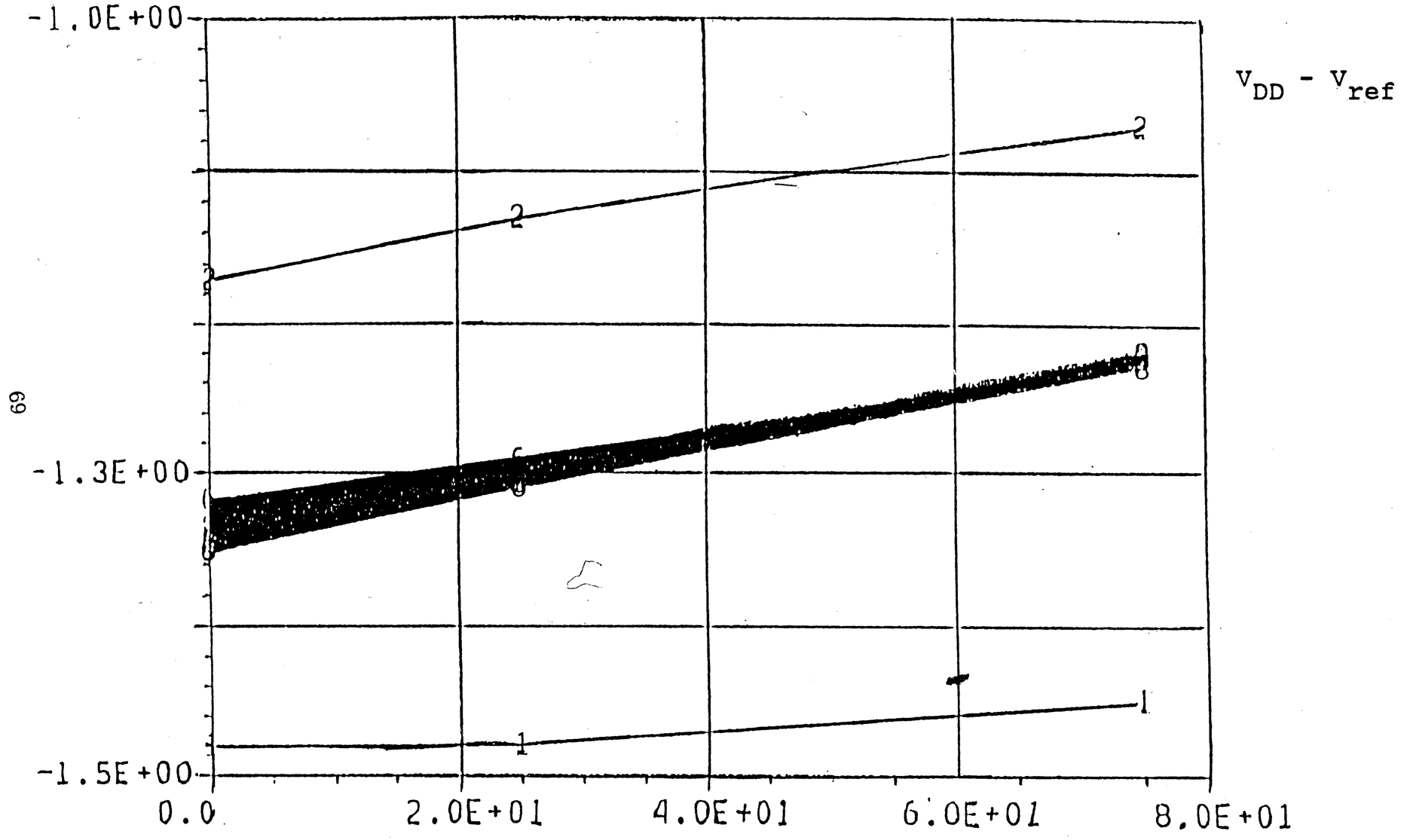


Figure 3 *The Threshold-Referenced Circuit*

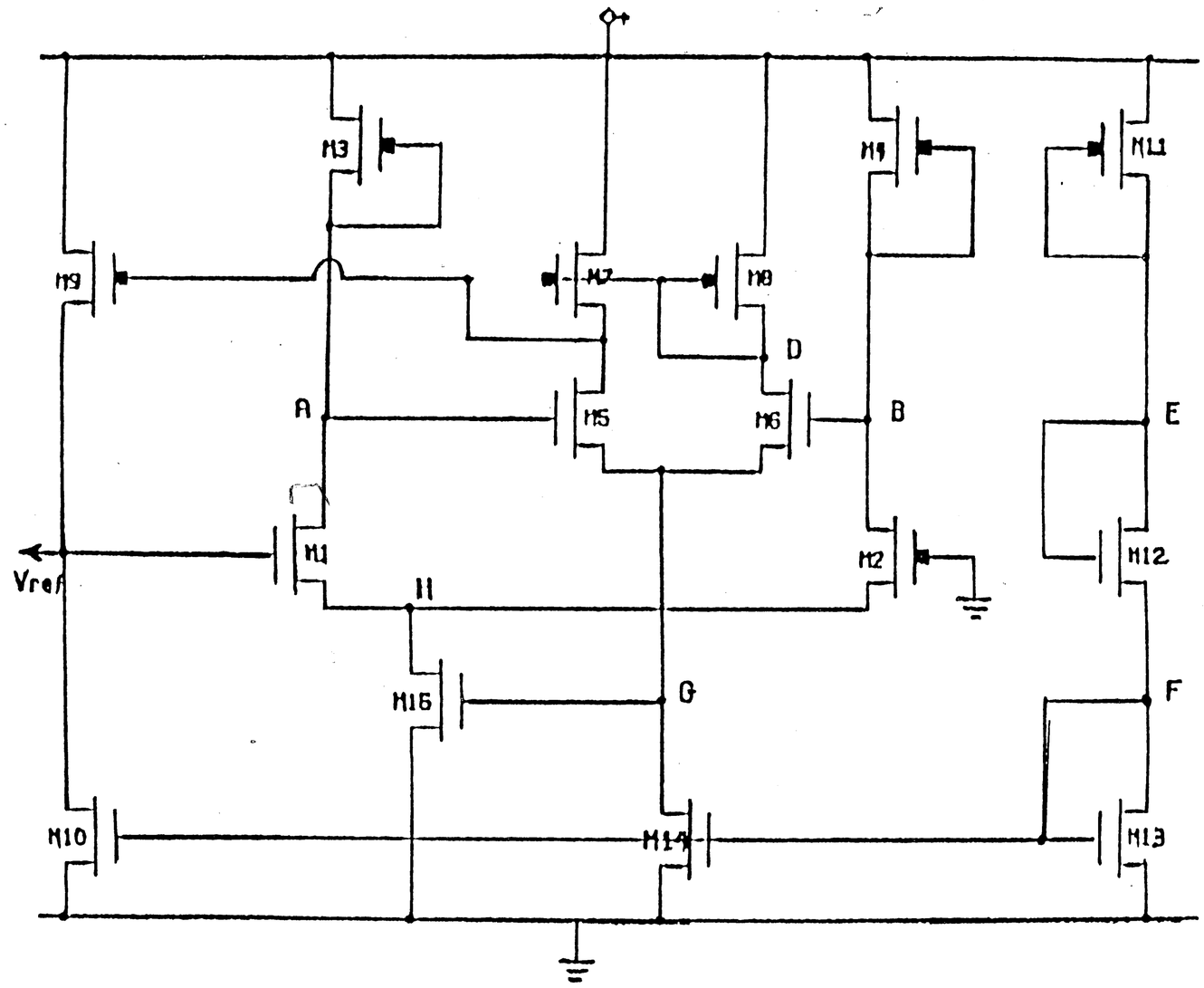


Figure 4 *The Widlar Bipolar Reference Circuit*

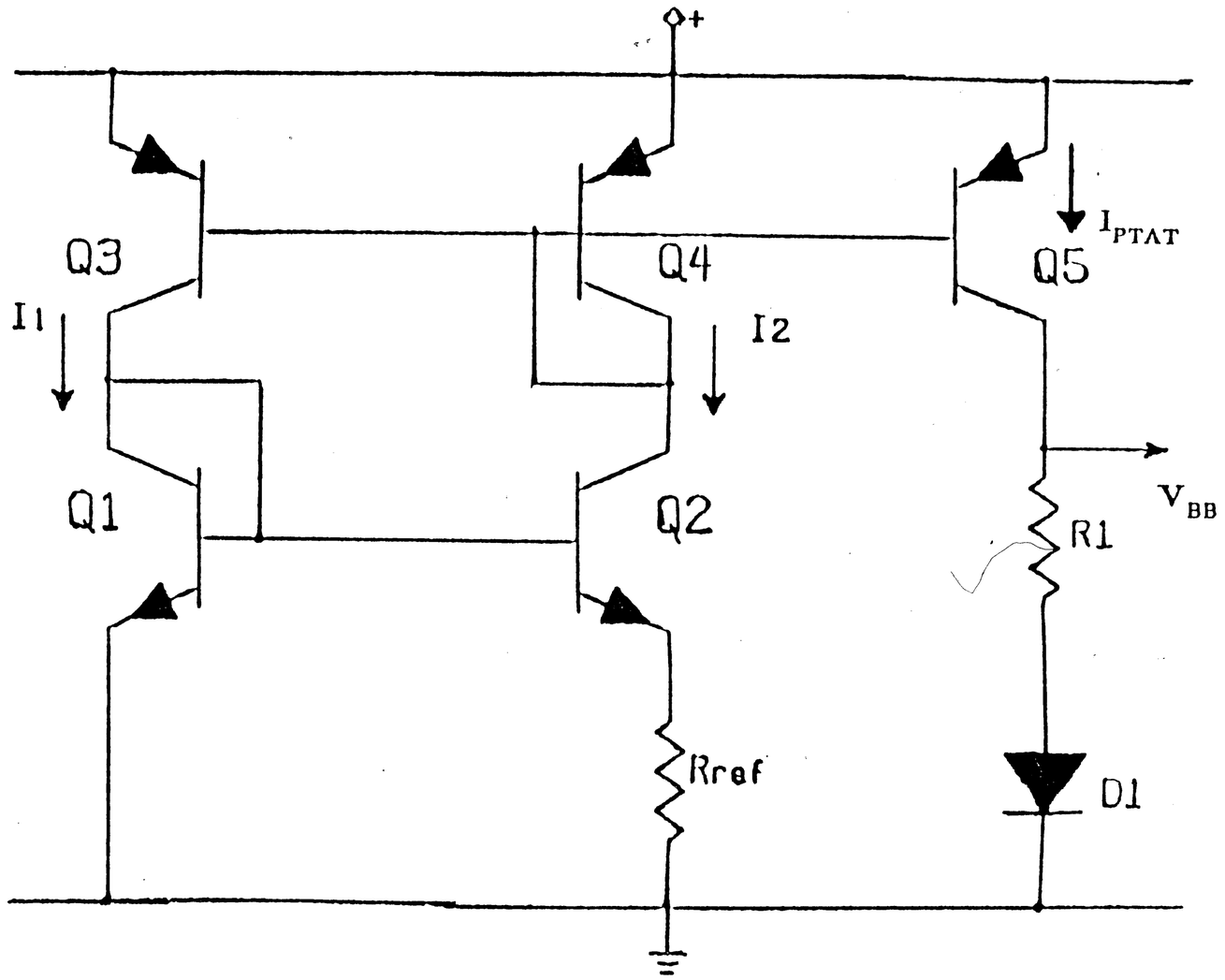


Figure 5 *A CMOS Bandgap Reference Circuit*

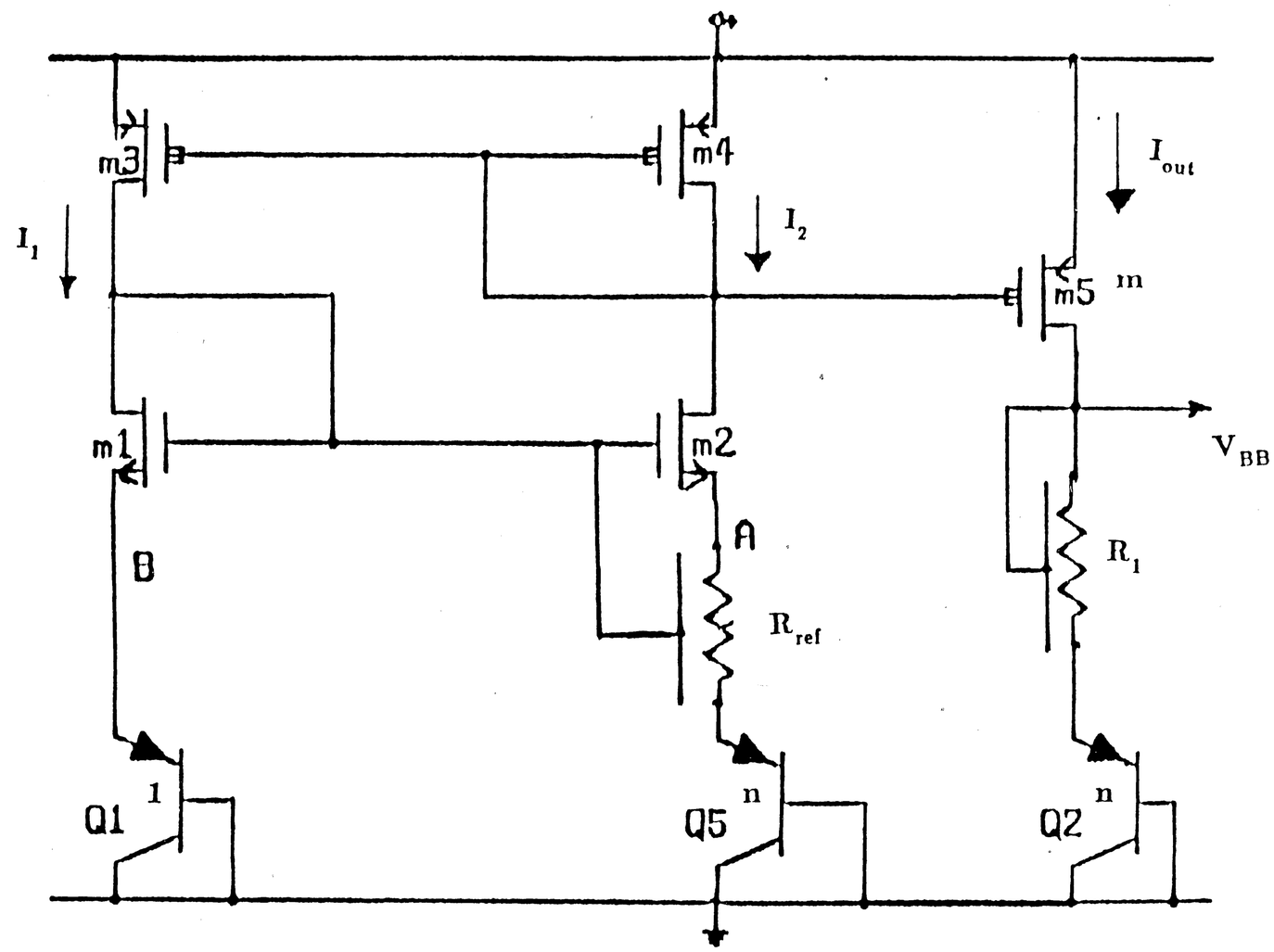


Figure 6 *An Enhancement to the CMOS Bandgap Reference Circuit*

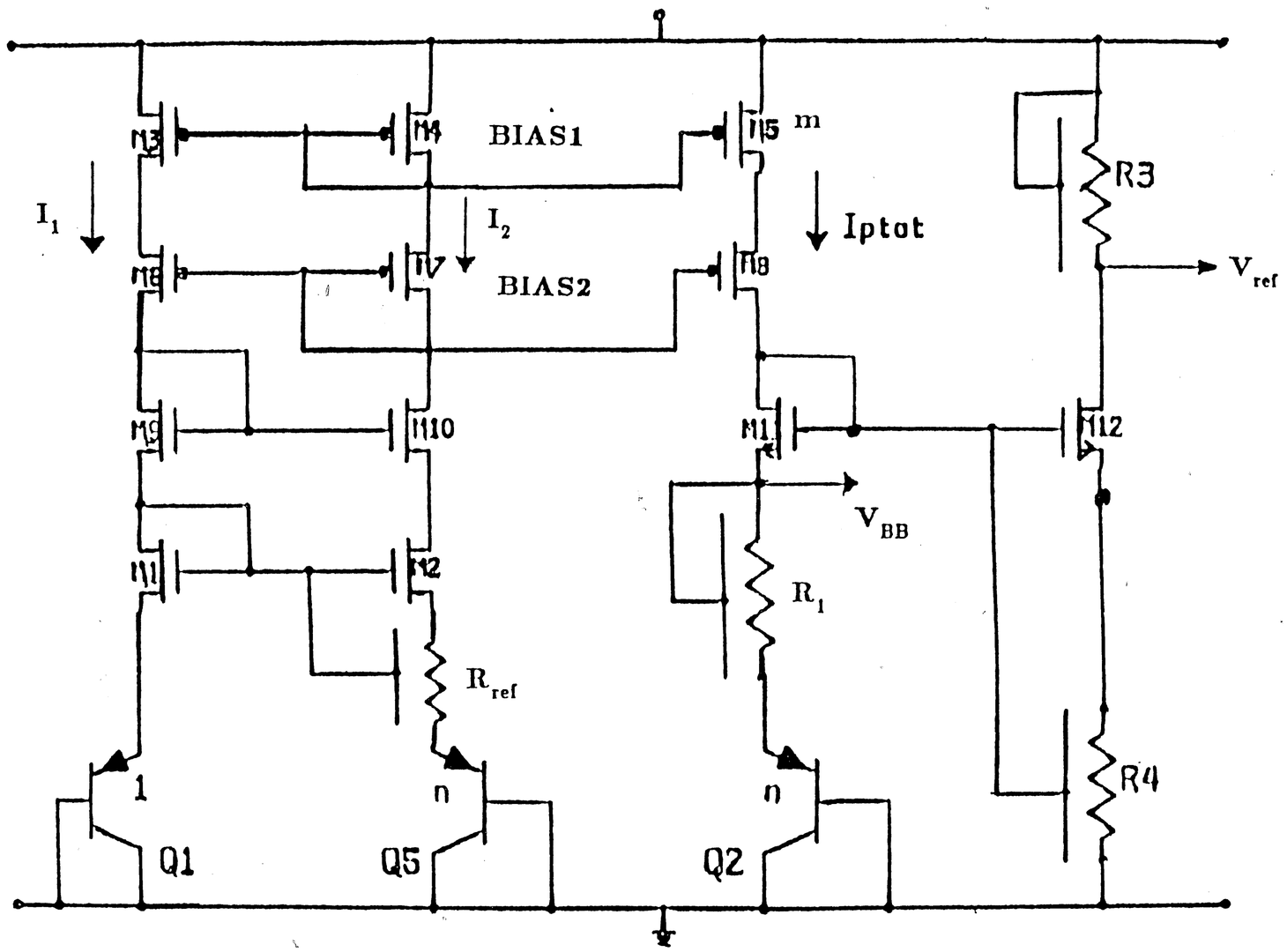


Figure 7 *The p+-diffusion resistor model*

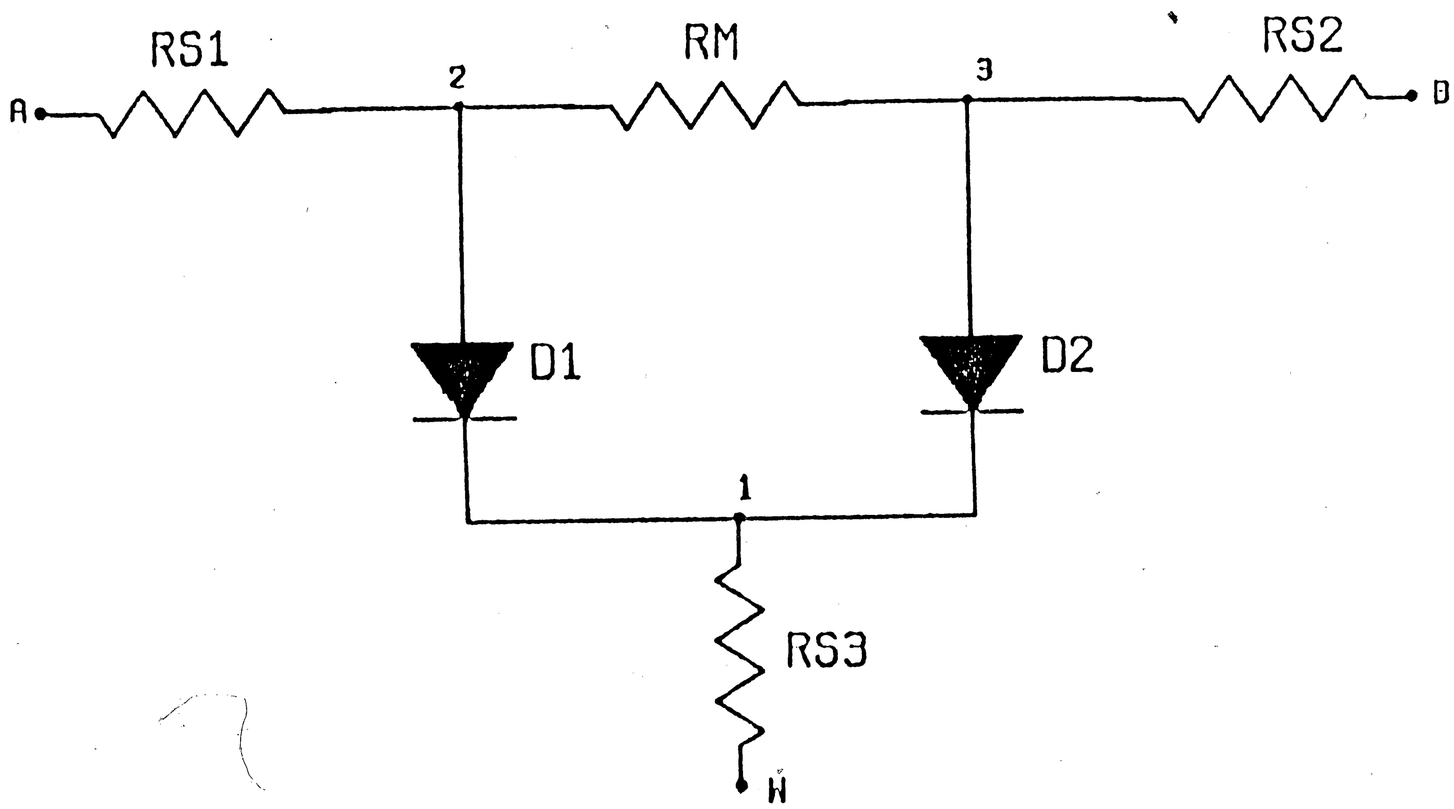


Figure 8 *The Actual ECl Input Specifications for the ECL-To-CMOS translator.*

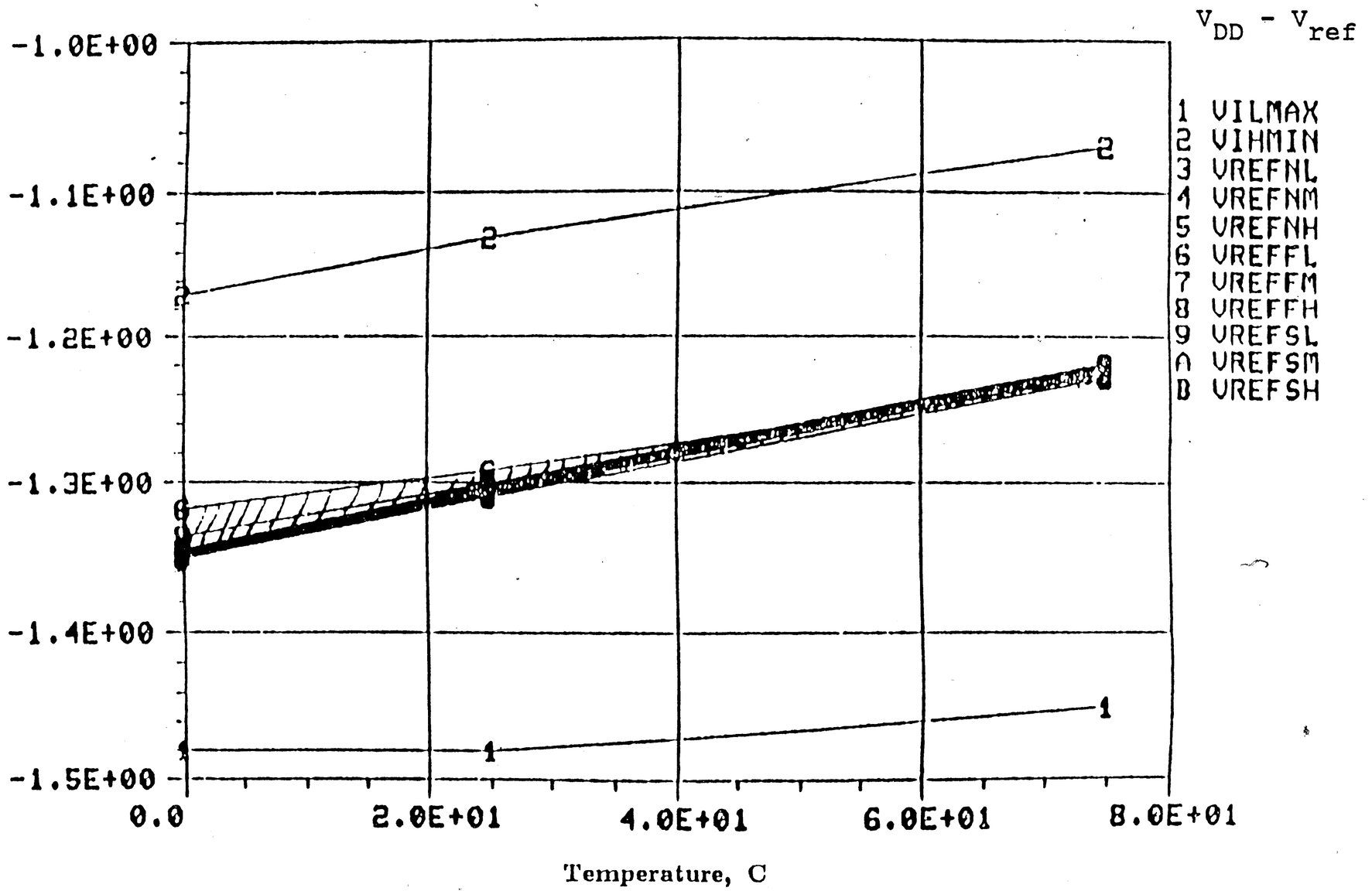


Figure 9 *The Performance Characteristics of the CMOS Reference with a low temperature coefficient*

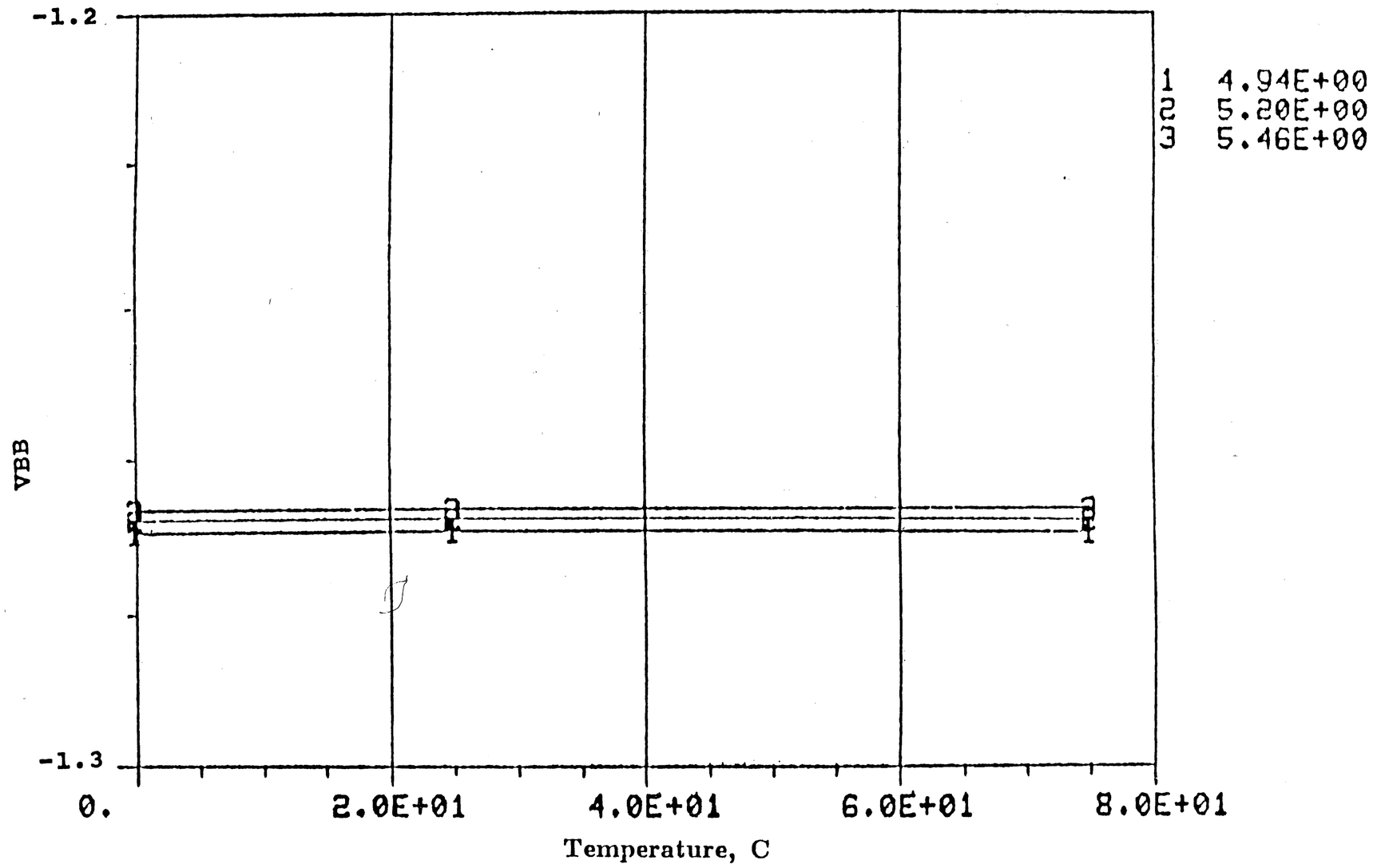


Figure 10 *The Start-Up Circuit*

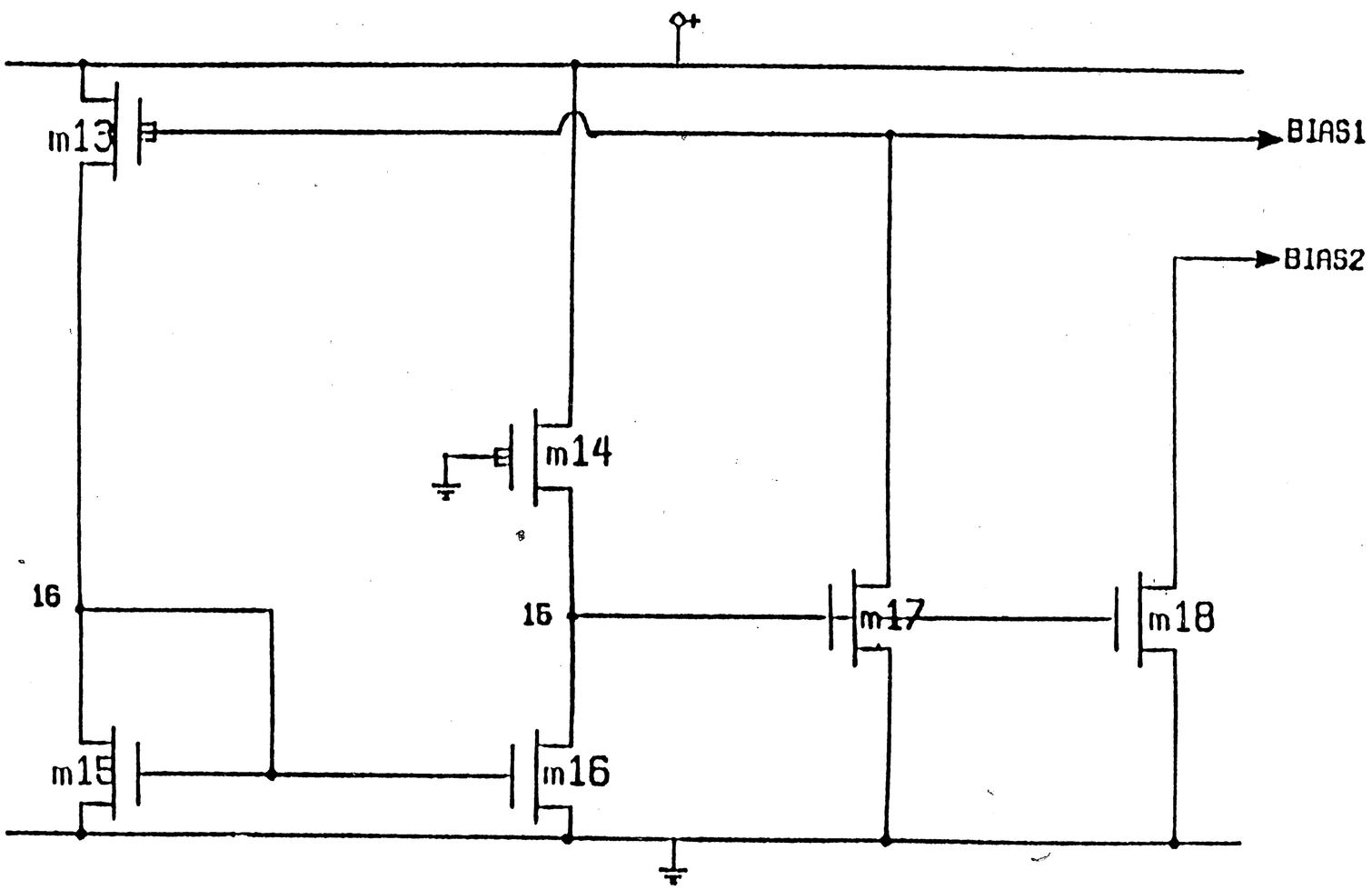


Figure 11 *The Unity-Gain Op-amp configuration*

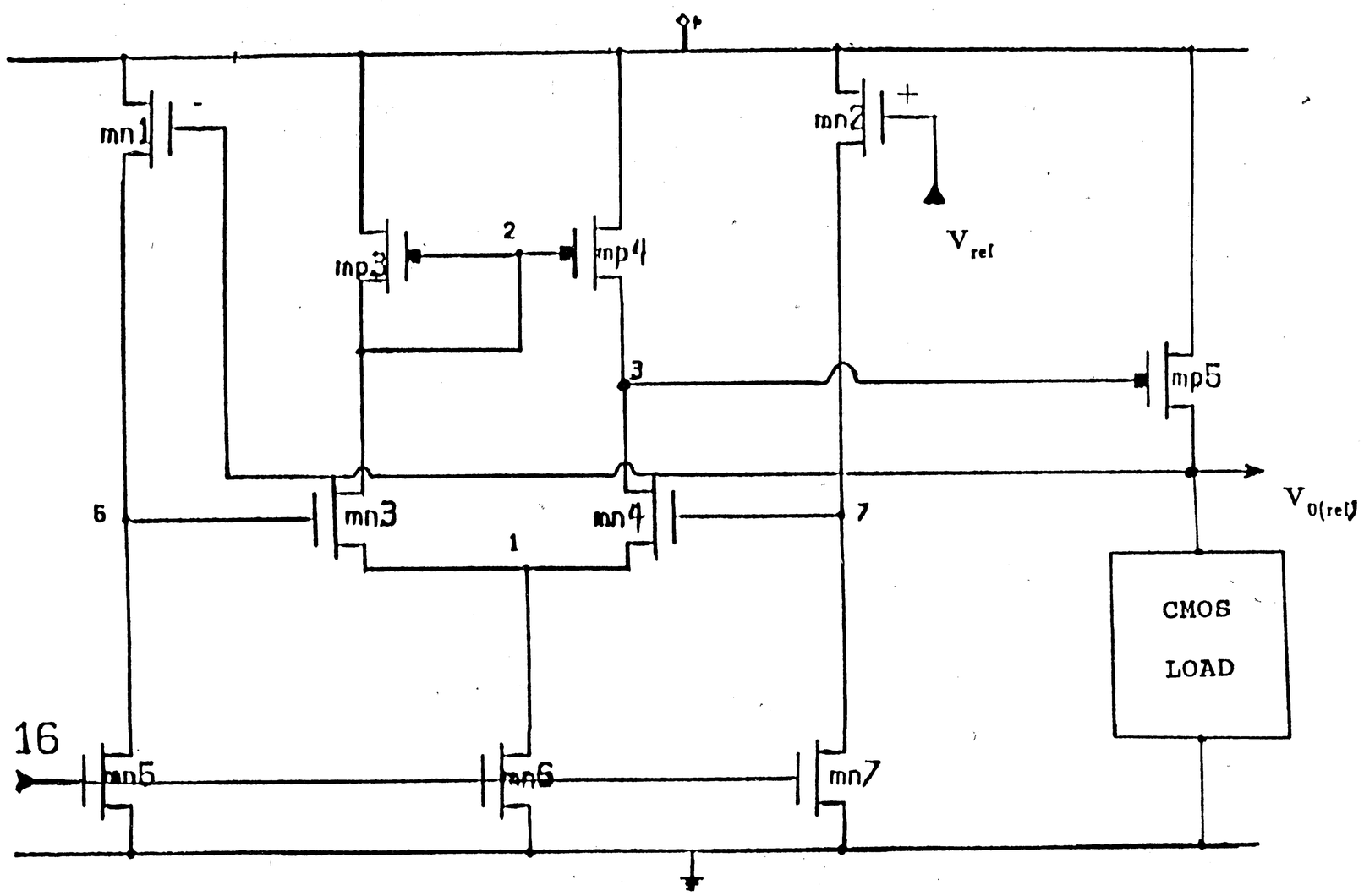


Figure 12 *The Voltage Comparator Circuit*

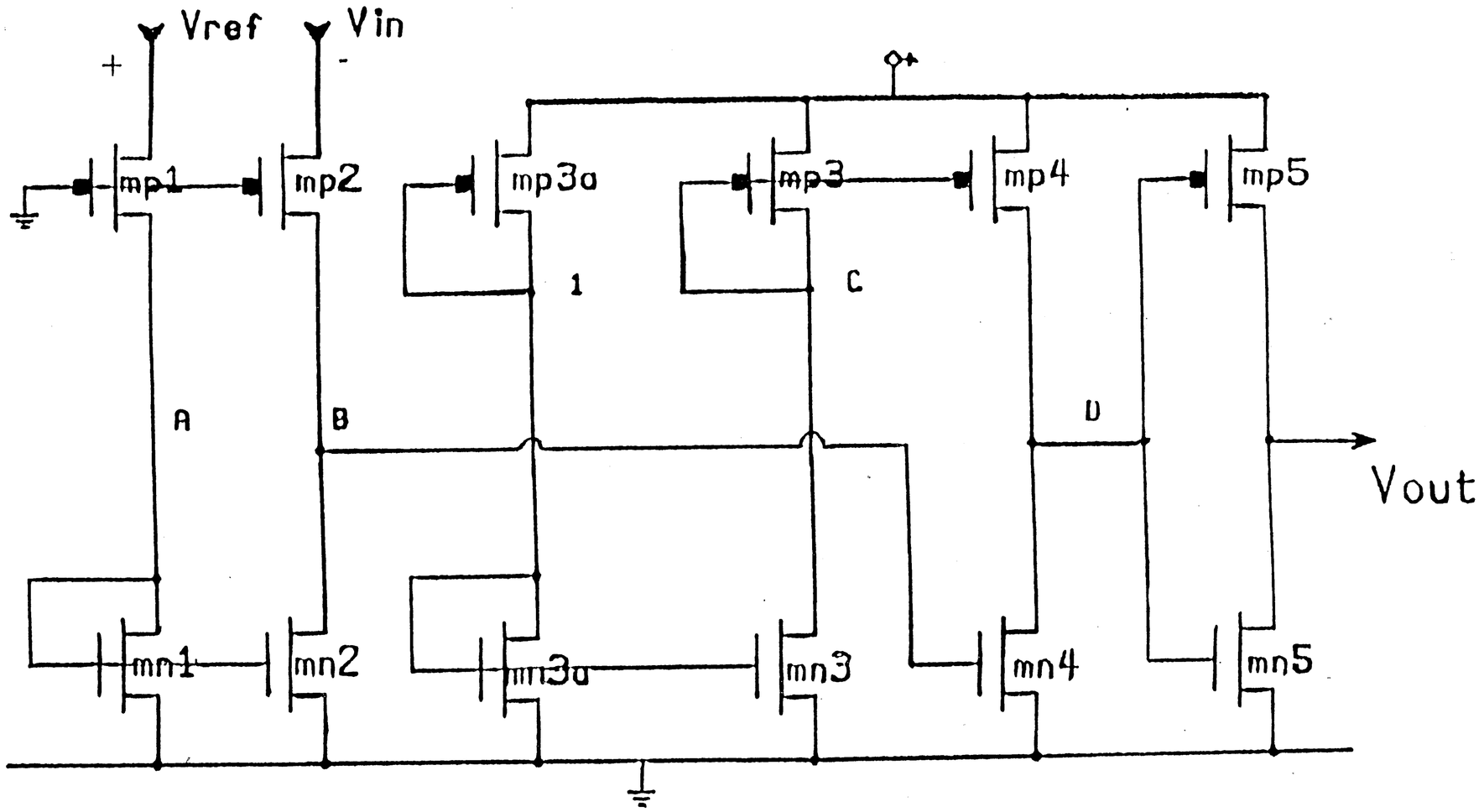


Figure 13 *The Performance Characteristic at the comparator output with VDD=4.94V T=75 C and fast process*

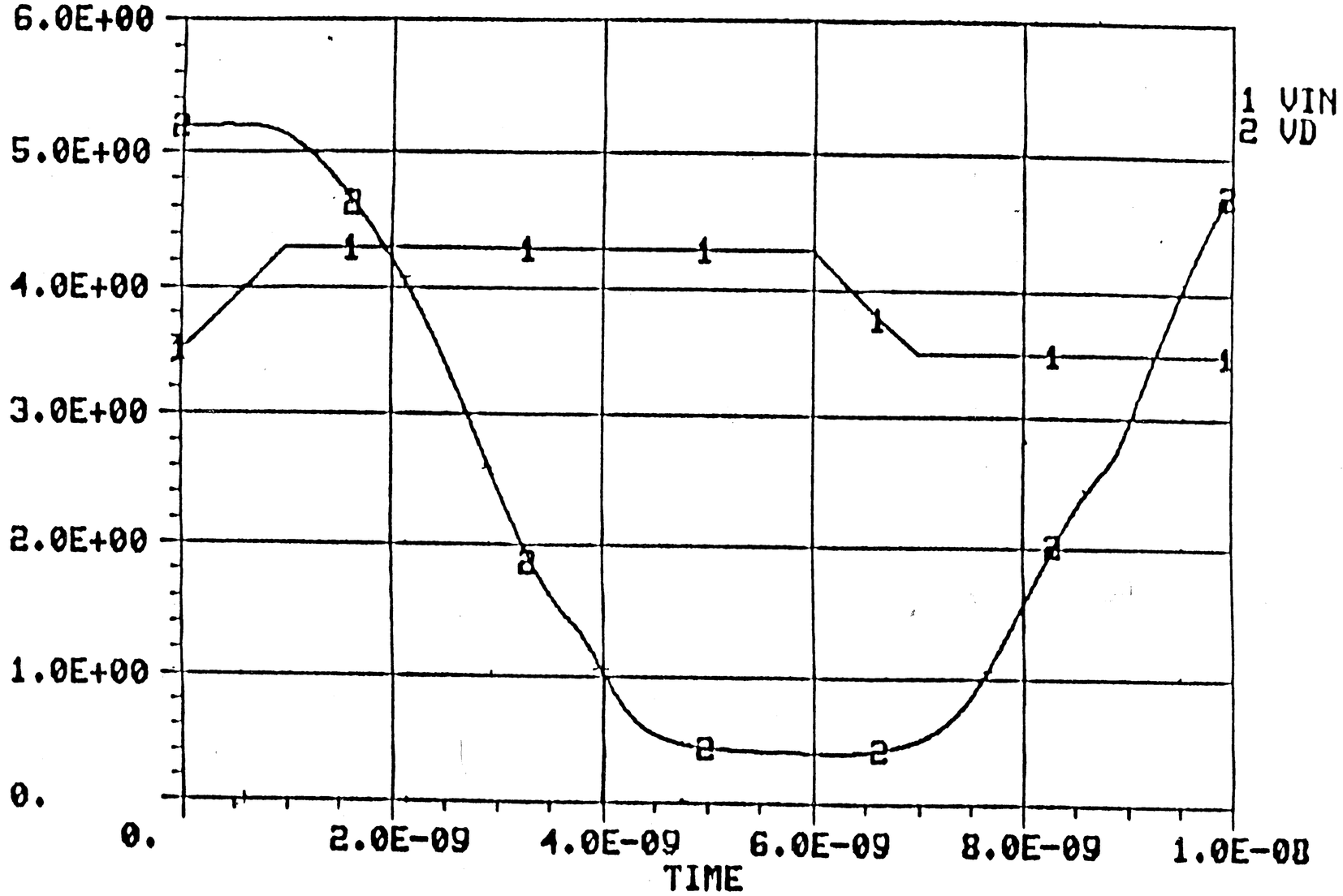
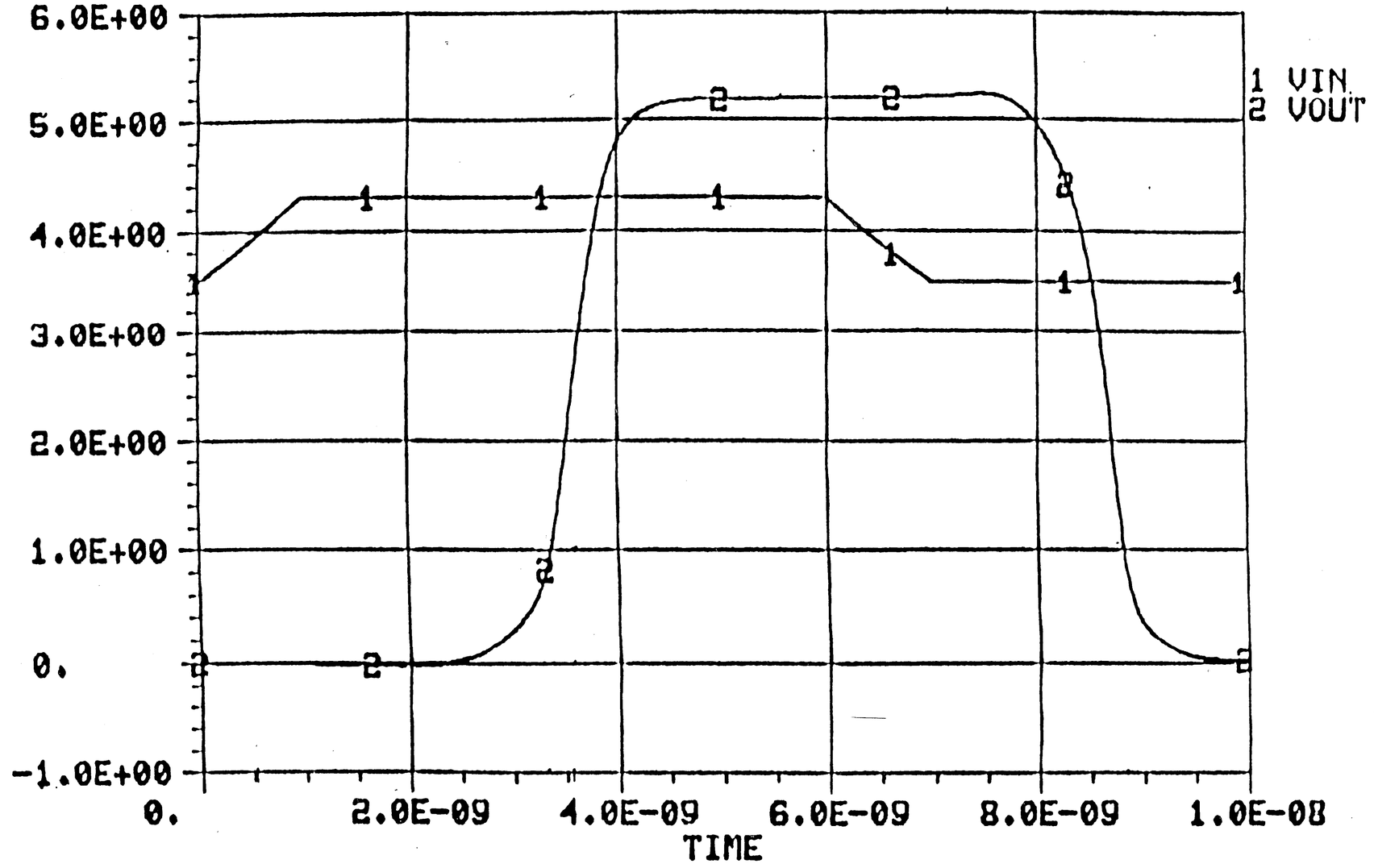


Figure 14 *The Performance Characteristic at the inverter output with VDD=4.94 T=75 C and fast process*



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Vita

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