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RETENTION ENDURANCE AND INTERFACE TRAPS IN MONOS MEMORY TRANSISTORS

by

Anirban Roy

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University
1985

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

Sept. 17th, 1985

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Professor in Charge

Chairman of Department

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ABSTRACT

A computer-aided dynamic characterization system for scaled MONOS (metal oxide nitride oxide semiconductor) transistors has been designed and tested. It offers speed and accuracy of data acquisition. Retention measurements from a few microseconds to a few days are possible, with more than 12 decades in time. Two newly designed instruments, an 8 channel versatile digital stimuli generator and a "Write-Erase & Read Circuit" are described which have rendered this possible.

Sample measurements on 85A nitride scaled MONOS complementary transistors are presented for the first time, with an enhanced detection scheme.

Extraction of the interface trap density at the Si-SiO_2 interface with subthreshold conduction in the MONOS transistor has been demonstrated with the HP4145 Semiconductor Parameter Analyzer.

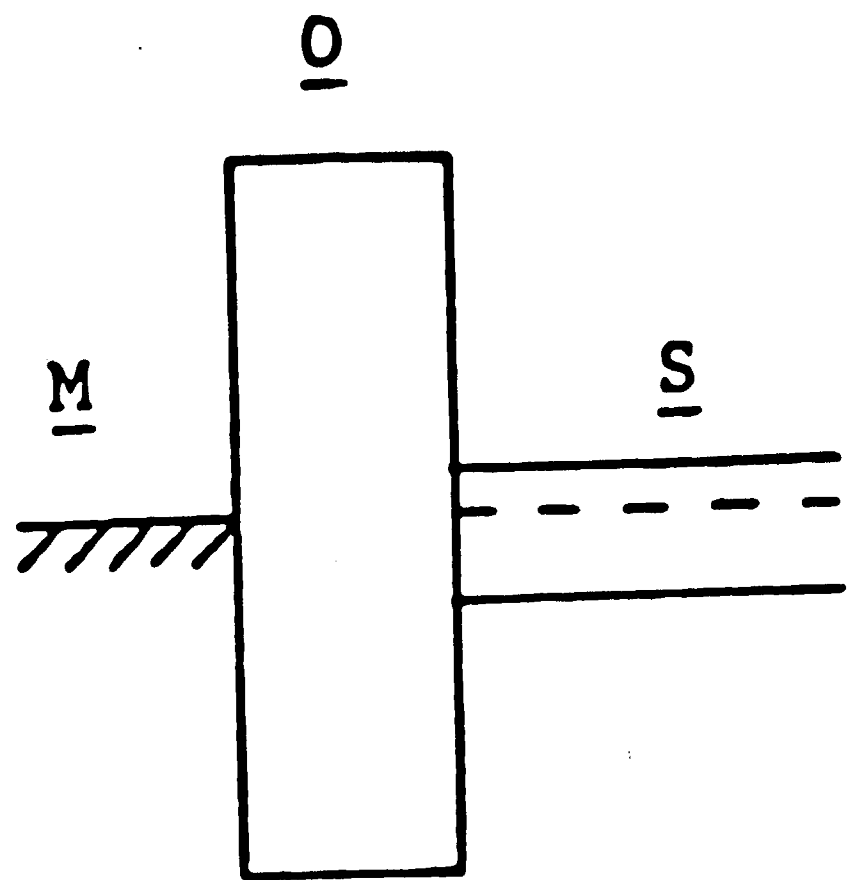
Chapter 1
INTRODUCTION

1.1 Background

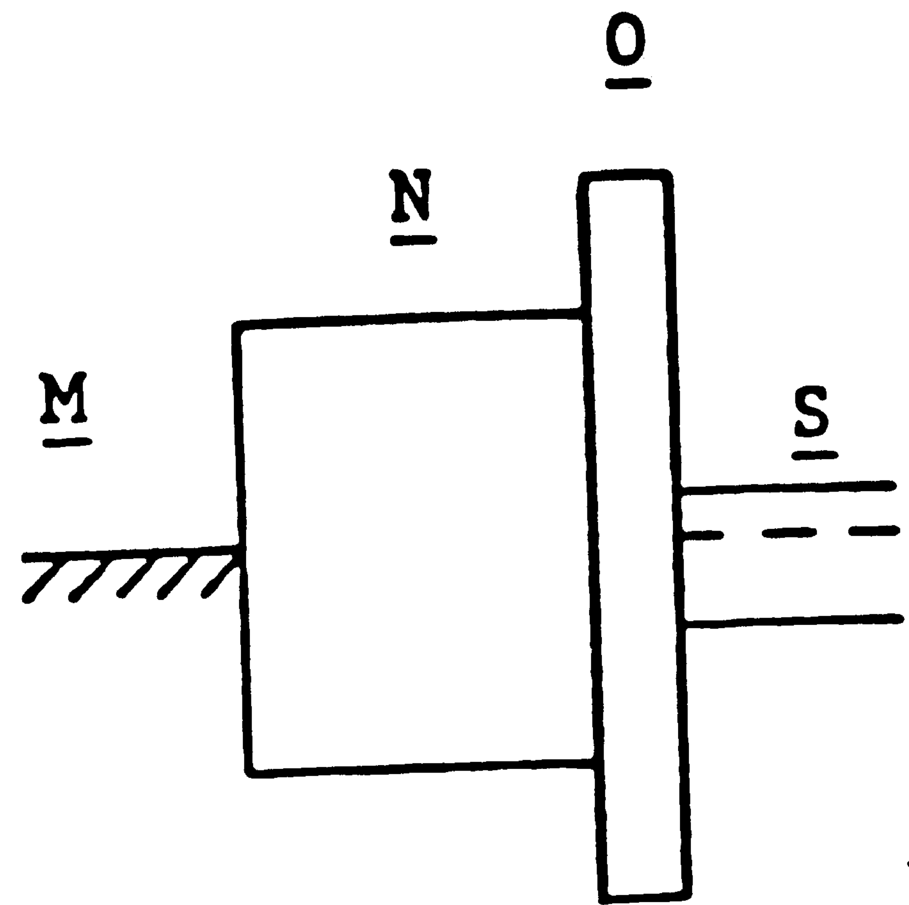
MOS (metal oxide semiconductor) transistor, MNOS (metal nitride oxide semiconductor) transistor, MONOS (metal oxide nitride oxide semiconductor) transistor and floating gate (metal oxide poly oxide semiconductor) transistor are from the same family; the MIS (metal insulator semiconductor) structures. Fig.1-1 shows the band diagram of the four above-mentioned structures. The MONOS transistor is a modified form of the MNOS transistor and so in this section only MNOS structure will be referred to since both these share the same terminology.

MNOS and MOS transistors have the same basic electrical characteristics. They differ only in one respect. For the MOS transistor, the threshold voltage remains fixed at a constant value. In contrast, the MNOS transistor provides the capability that the threshold voltage can be set and reset electrically to high and low (digital nomenclature) values. Once set, a specific threshold voltage will remain near its value for an extended and predictable length of time even after any source of power to the device has been removed (a non-volatile memory transistor).

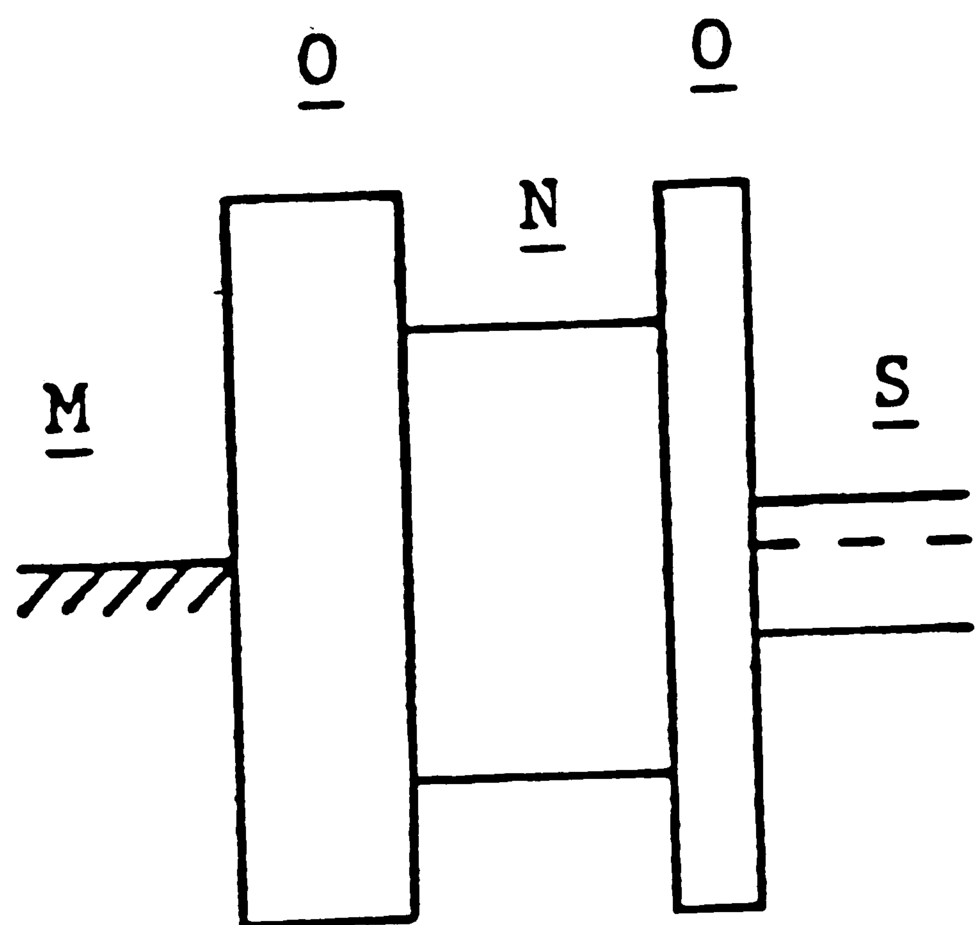
The change in threshold voltage in MNOS transistors is manifested because of exchange of charge between the nitride layer and the thin tunneling oxide layer between it and the silicon. The scaled down MONOS structure and its



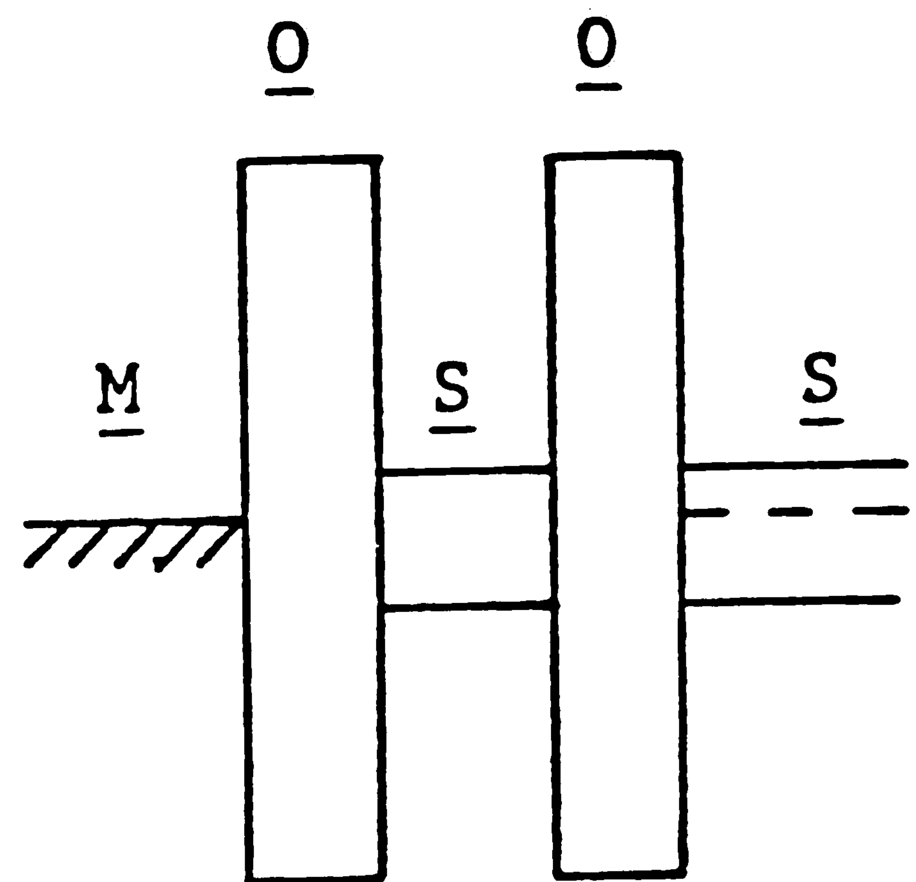
MOS Structure



MNOS Structure



MONOS Structure



Floating Gate E^2PROM Structure

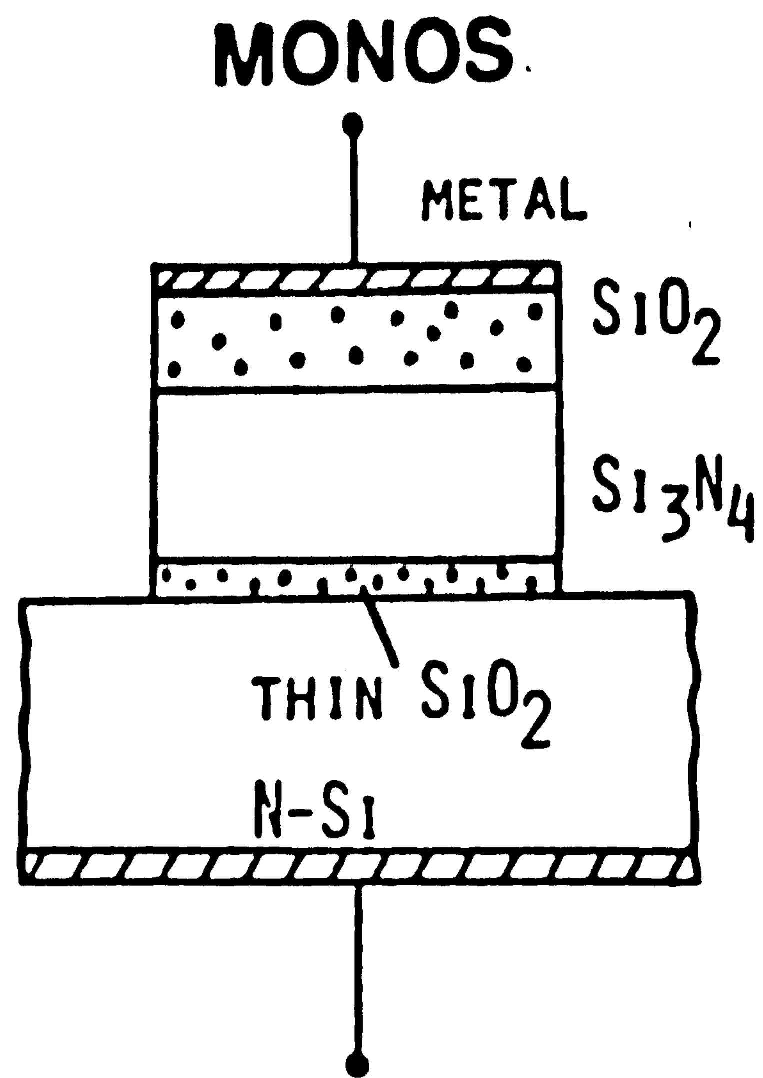
Figure 1-1: Various MIS structures

detailed energy band diagram is shown in fig.1-2, and the various current components in the MONOS structure under positive and negative gate bias (relative to the bulk) are indicated in fig.1-3. **Writing** an MNOS transistor results in putting the transistor into a low conduction (LC) state. This means the transistor will be normally off. This pertains to accumulation of carriers in the nitride, from the inversion layer at the silicon. **Erasing** results in putting the transistor into a high conduction (HC) state. This means the transistor is normally on. This pertains to accumulation of carriers in the nitride, from the silicon surface accumulation layer.

Retention is the time period defined by the time elapsed between the instant of writing/erasing an MNOS transistor and the instant when either state becomes indistinguishable from the other. Therefore, the end of retention depends very much on the method of interrogation and on the sense amplifier, since they decide distinctness. The time period t_{rd} between the end of writing/erasing pulse and the start of read condition is referred as **read delay**. There are three ways of defining and measuring retention.

1. CONSTANT CURRENT RETENTION : Retention inherent in the MNOS transistor when gate and drain are biased to result in a constant drain current during information storage.

2. CONSTANT VOLTAGE RETENTION : Retention inherent in the MNOS transistor when source, drain and substrate are grounded, and a fixed bias is maintained at the gate.



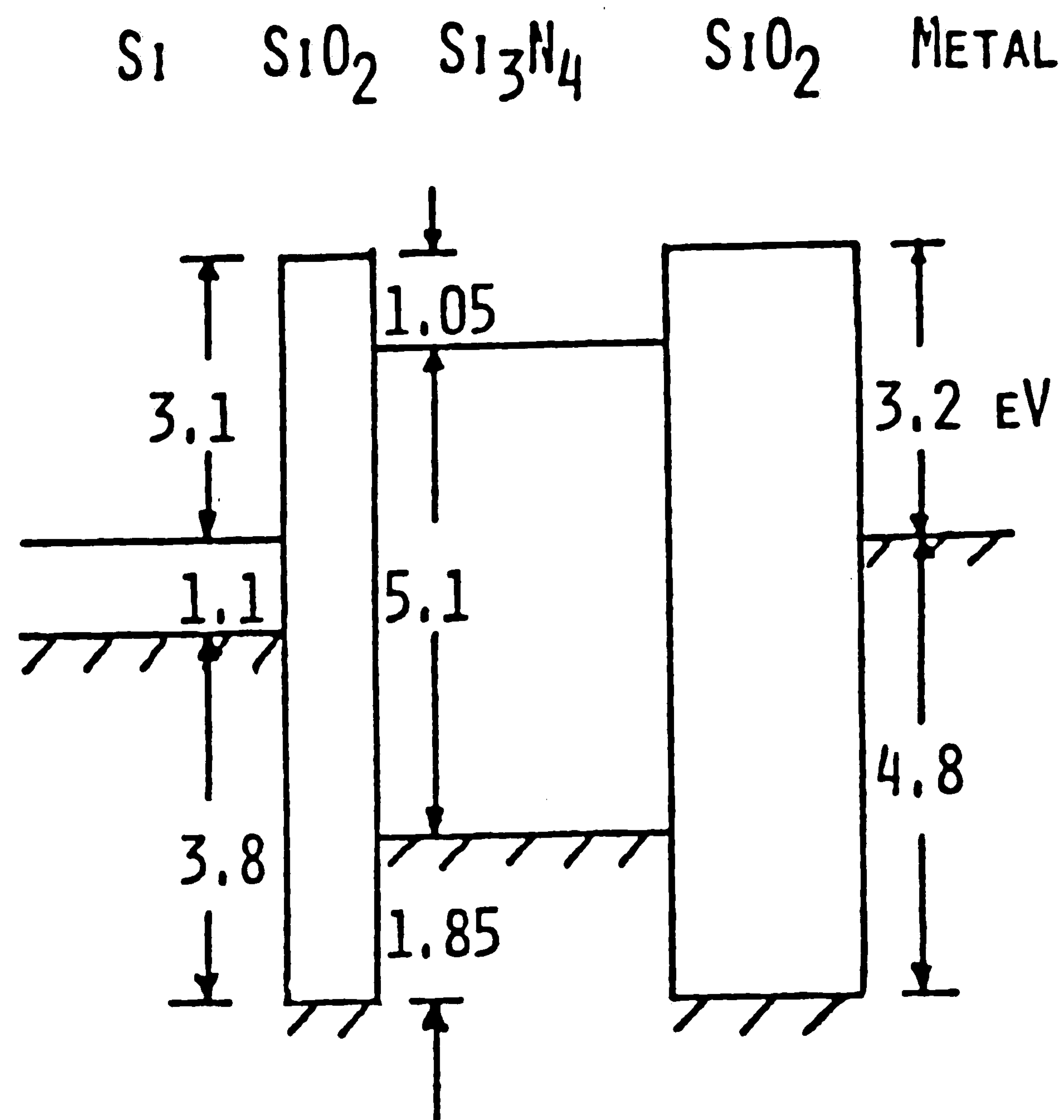
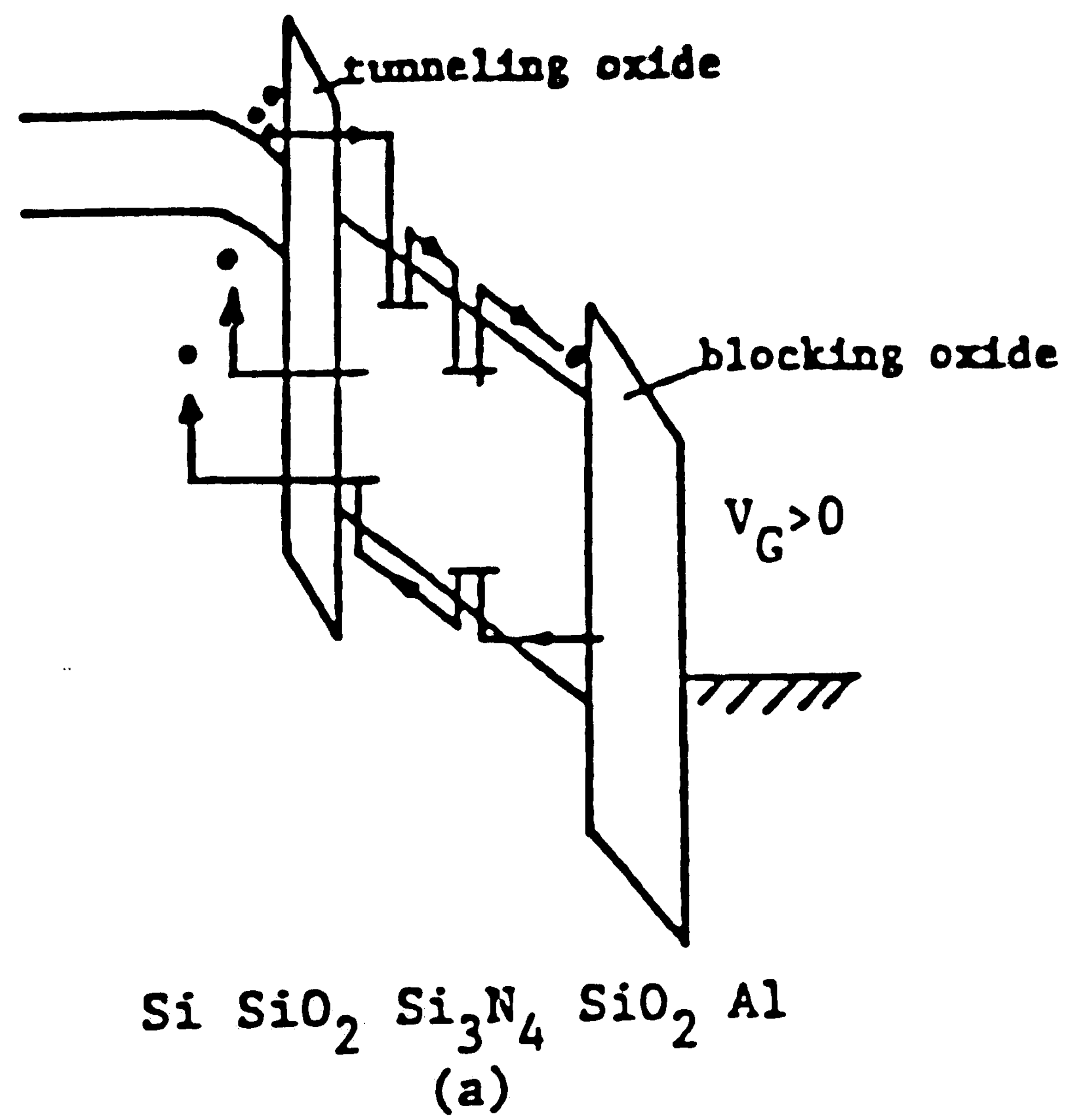
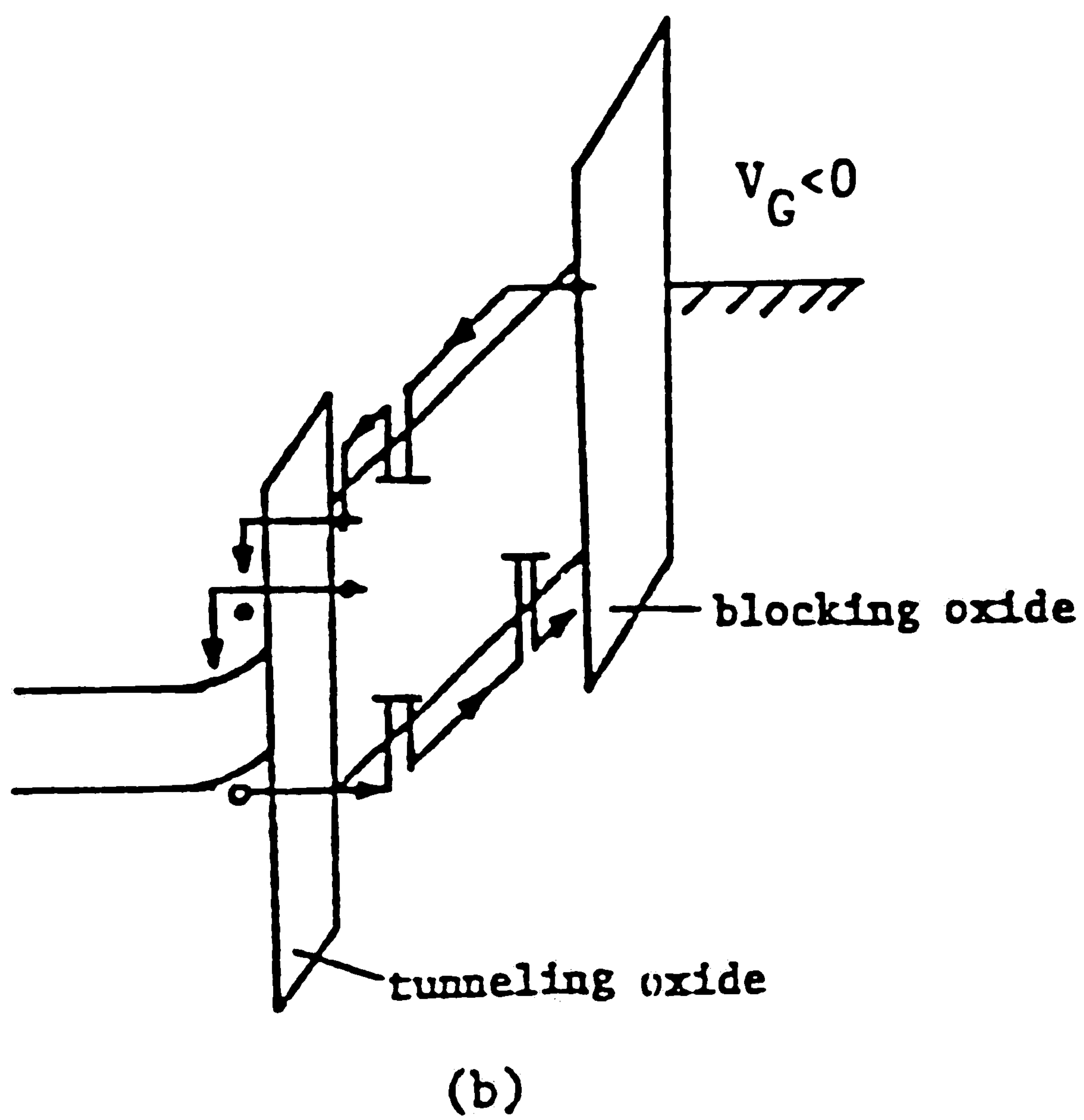


Figure 1-2: (a) The scaled MONOS structure and (b) its ideal energy band diagram



(a)



(b)

Figure 1-3: Various tunneling current components in the MONOS sandwich under: (a) positive gate bias and (b) negative gate bias

3. ZERO BIAS (OR RELAXATION TIME) RETENTION : Retention inherent in the MNOS transistor when all terminals are grounded during information storage.

Endurance of an MNOS transistor is the number of write-erase cycles accumulated before any defined unacceptable change in device properties occur. The limit of endurance varies some-what with the details of the stress condition and it manifests itself in diverse ways. The most important effect observed is a reduction in retention.

Compared to floating gate devices the MNOS transistors exhibit smaller retention but faster programming times and a higher endurance. Transverse conductivity of the floating gate allows discharge of the stored charge thru defects in the thin insulator. On the other hand MNOS devices are relatively free from total charge loss at pinholes because the charge is stored in traps within the Si_3N_4 insulator. In addition, the MNOS process can be so realized that it's largely compatible with VLSI Si-gate technology for logic circuits.

1.2 Historical Review of Retention

Voluminous literature exists on studies regarding dependence of retention on device structure, fabrication processing and operating variables.

- Structure Variations

1. Tunnel Oxide Thickness : The various figures of merit impose conflicting constraints on the device parameters. For instance short write times require thin SiO_2 layers, but such thin layers

also decrease the retention time. However, thin oxides have a higher endurance to prolonged cycling as compared to thicker oxides, ie., >30A

2. <u>Drain Source Protected Devices</u> : In thin-oxide MNOS devices, with symmetric positive and negative voltage pulses applied, the flat band voltage shifts in the positive and negative directions respectively. In some memory designs, this is undesirable. One way of eliminating this problem is to use the so called "tri-gate" structure or "drain source protected" structure. Endurance data obtained by Cricchi et.al. [8] using this structure were several orders of magnitude better than those reported by others.

3. <u>Vertical Scaling</u> : To realize a low voltage EEPROM with an MNOS structure, the thickness of the gate insulators must be scaled down. The thickness of the tunnel oxide cannot be scaled because tunneling probability is exponentially related to thickness, but the nitride thickness can be scaled. An approximate scaling limit is defined by a nitride thickness which is twice the charge centroid. Suzuki et.al. [24] worked on the scaled down MONOS devices, introduced by Chen [7] in 1977, and reported ±6V programming voltages with retention decay rate of 0.11V/decade for +7V writing for n-channel and 0.094V/decade for p-channel devices.

- Process Variations

1. Tunnel Oxide Growth : Endurance depends critically on the thickness and process used to grow the thin tunneling oxide. The most prevalent technology for tunnel oxides is dry thermal oxidation. Neugebauer et.al. [18] had grown tunneling oxide by boiling concentrated nitric acid, but obtained less endurance.

2. Nitride Growth : Both APCVD (atmospheric pressure chemical vapor deposition) and LPCVD (low pressure chemical vapor deposition) nitrides have been investigated. The gases used are either NH_3 and SiH_4, or NH_3 and $SiCl_2H_2$. Different gases ratios give different stoichiometry of the nitride, either silicon rich or nitrogen rich, thus changing trapping density and conductivity in the nitride.

3. Annealing : A hydrogen annealing study of SNOS non-volatile memory devices showed that the important parameter in determining the optimum annealing temperature for maximum charge retention is the previous thermal history of the memory devices.

   W.D. Brown [5] reported that HCl annealing of memory oxides does not have a significant effect on either endurance or retention. But White et.al. [29] reported that non-HCl oxides

maintain better window definition than HCl oxides with extended cycling.

- Operating Variations

1. Elevated Temperature Discharge : Jones and Brown [14] studied endurance and retention over the temperature range from -50°C to 125°C and concluded that retention is a more sensitive function of endurance cycling than elevated temperature. Increased nitride conductivity, thermal excitation tunneling and increased interface trap density were attributed to degradation at elevated temperatures.

2. Write-Erase Time and Voltage Levels : Write-erase voltages of the order of 20-25V have been used for thick nitride (>450A) MNOS devices. Depending on the tunneling oxide the writing speed varies from author to author, ranging from few microseconds to few tens of milliseconds.

3. Read Disturbance : "Read Disturb" is the instantaneous change in threshold voltage of an MNOS transistor due to the very act of measuring it, and does not occur until the MNOS transistor begins conduction. In order to minimize read disturb, the threshold of the memory device must be sensed as soon as possible.

The introduction of the Metal Oxide Nitride Oxide Semiconductor (MONOS) memories offers a new dimension to the scaling of non-volatile memories. The scaling of these devices leads to the following salient features of this new structure over the conventional thick nitride Metal Nitride Oxide Semiconductor (MNOS) structures:

- The nitride thickness can be scaled down below 195A , the limit considered for MNOS structures [11].

- This device structure utilizes a so-called "blocking oxide" to effectively inhibit the movement of the charge centroid and gate electrode injection.

- Low programming voltages (5-10V)

1.3 Recent Results On Scaled Devices

In this section, dynamic characterization results on scaled nitride MNOS/MONOS devices reported in the literature in the past few years to reflect on the state of the art in device technology, characterization instrumentation capabilities and device performance. A comparitive study is detailed below, in a chronological order:

1. Chen,1977 [7].

    - DEVICE STRUCTURE: n-channel SONOS capacitors and transistors with tunnel oxide thickness of 30A, nitride thickness of 400A and oxy-nitride thickness of 150A.

- ERASE WRITE: Erase voltage= – (36V to 42V) ; Write voltage= 30V to 36V ; Erase-write time=20 to 100ms.

- RETENTION: SONOS capacitor at 70°C with grounded terminals during storage. Threshold change monitored with HF C-V shifts. Retention monitored from 10s to 2×10^5s. Logarithmic decay observed with decay for the write state: 0.4V/decade and for the erase state: 0.15V/decade.

- OTHER COMMENTS: First author to introduce blocking layer over the nitride and announce the MONOS structure.

2. Jacobs et.al.,1981 [7]

   - DEVICE STRUCTURE: n-channel SONOS transistor. Tunneling oxide thickness of 20A , nitride thickness of 240A and blocking oxide thickness of 100-150A.

   - ERASE-WRITE: Erase voltage= – 25V ; Write voltage=25V ; Erase time=100ms ; Write time=10ms.

   - RETENTION: Static I-V shifts for threshold change monitoring. Retention monitored from 1min. to 10^5min. Logarithmic decay behaviour observed with write state decay rate=0.65V/decade.

   - OTHER COMMENTS: Restriction of the test setup is the

generation of single W/E pulse-width of 100μs.

3. Yatsuda et.al.,1982 [13]

   - DEVICE STRUCTURE: n-channel MNOS and MONOS transistors. For the MNOS structure the tunnel oxide thickness is 21A, the nitride thickness is 195A. For the MONOS structure the tunnel oxide thckness is 21A, the nitride thickness of 150A and blocking oxide thickness of 25A.

   - ERASE-WRITE: Erase voltage= $-$ 10V ; Write voltage=10V ; Zero programming window obtained at 100μs.

   - RETENTION: Room temperature retention. Retention data reported from 1s to 10^6s. Logarithmic decay behaviour for both states. Write decay rate=0.3V/decade ; Erase decay rate=0.1V/decade.

   - OTHER COMMENTS: Write time independent of tunnel oxide thickness. Better endurance of MONOS structures over MNOS.

4. Suzuki et.al.,1983 [10]

   - DEVICE STRUCTURE: n-channel MONOS capacitor. Tunnel oxide thickness of 23A ; nitride thickness of 63A to 94A ; and blocking oxide thickness of 0 to 50A.

- ERASE-WRITE: Erase voltage=−7V ; Write voltage=7V ; Write-erase time=1s.

- RETENTION: Threshold changes monitored from the HF C-V shifts. Retention monitored from 10ms to 10^4s. Logarithmic decay behaviour observed for both states. Write decay rate=0.11V/decade ; Erase decay rate=0.094V/decade. Initial window=2.5V.

- OTHER COMMENTS: Low voltage EEPROM operation was demonstrated.

5. Haken et.al.,1983 [10]

    - DEVICE STRUCTURE: p-channel SONOS transistors in an array. Tunnel oxide thickness of 20A ; nitride thickness of 100A and blocking oxide thickness of 40A.

    - ERASE-WRITE: Erase voltage=13V ; Write voltage=−13V ; Speed of programming(zero window)=5μs.

    - RETENTION: 3 to 10 days of retention claimed.

    - OTHER COMMENTS: Application for NVRAM. Endurance greater than 10^{11} cycles claimed.

6. Topich,1984 [26]

- DEVICE STRUCTURE: n-channel SNOS transistor. Tunnel oxide thickness of 20A ; nitride thickness of 390A.

- ERASE-WRITE: Erase voltage= – 25V ; Write voltage=25V ;Erase time≃100ms.; Write time=10ms.

- RETENTION: Temperature used 100°C. Grounded terminals of the device for long term retention. Retention monitored from 1s to 1year. Initial decay logarithmic. Write decay rate=900mV/decade ; Erase decay rate=950mV/decade. Decay rates decrease after 10^4s to 10^5s for write and after 10^5s to 10^6s for erase states of an uncycled device.

- OTHER COMMENTS: Decreasing decay rates reported for the first time. Different long term retention characteristics than of thick nitride devices.

A comparison of the retention results of the above authors is attempted in fig.1-4.

Some other authors have been working on scaling aspects of MNOS and MONOS devices [6].

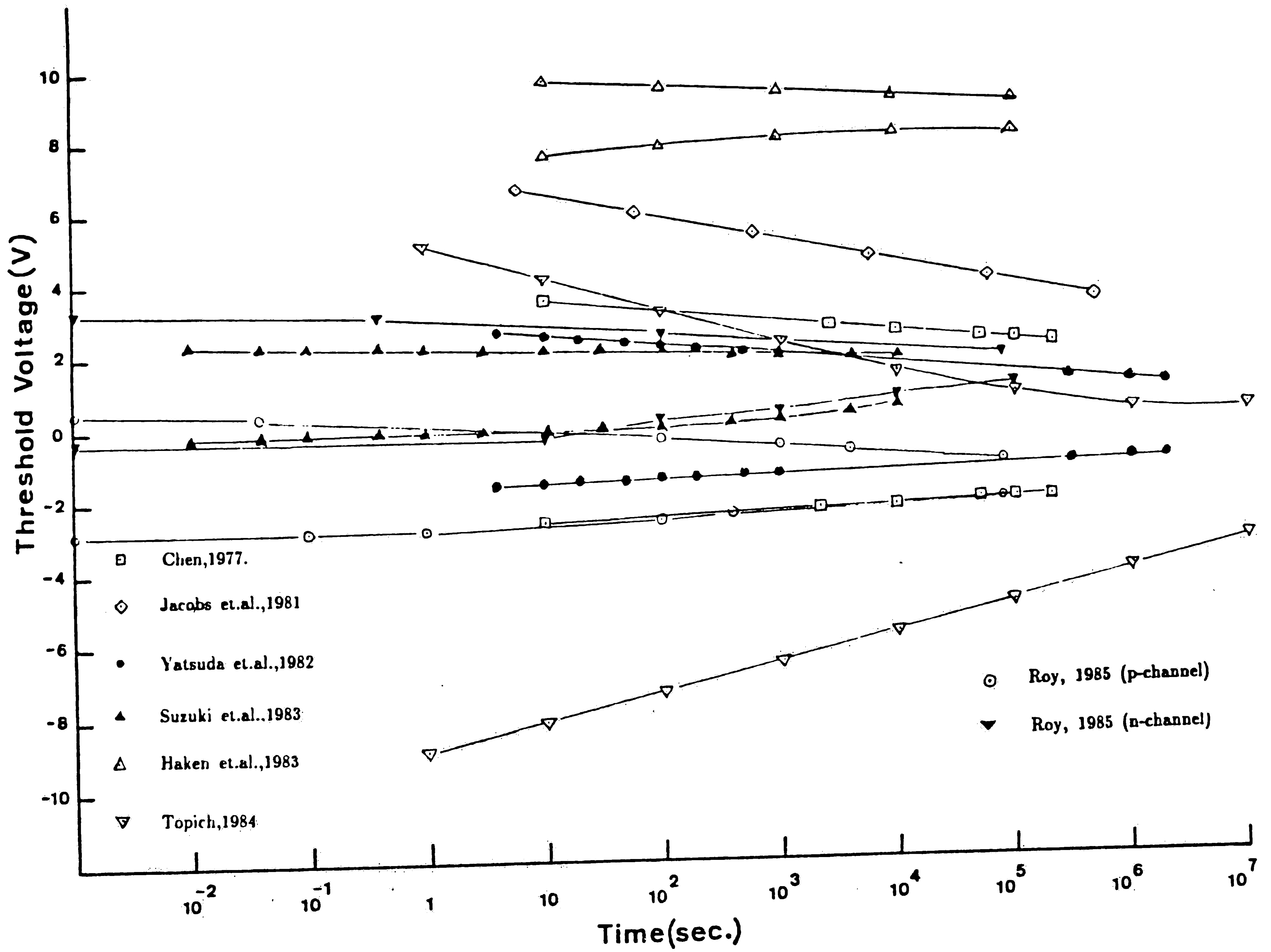


Figure 1-4: Comparison of retention data of scaled MNOS/MONOS devices

1.4 Purpose Of The Work

Available literature on the dynamic characterization of scaled MONOS devices is not conclusive. In order to understand the physics behind the device operation and the advantages or disadvantages that the device structure offers, transient response of the device is the most important attribute, because it reflects the operation of the device as a memory element.

The work presented in the thesis has been a solution to the dynamic characterization. It has been my attempt to obtain an accurate, computer automated test vehicle for exercising memory devices. The work concentrates on the single transistor structures but can be extended to an array organization of devices.

The Si-SiO_2 interface is one of the most elaborately studied areas in device physics, but the extraction of interface trap density of MONOS devices with the conventional C-V techniques is really inappropriate; since the device undergoes stress, and exchange of charge from the nitride and the semiconductor is present. This work includes examination of the subthreshold conduction of the MONOS transistor in order to extract interface trap density near midgap in the semiconductor.

Chapter 2
THEORIES ON RETENTION

2.1 Early Models

MNOS switching models were suggested within a few years of the reporting of the MNOS device by Wegener et.al. [27]. Models by Ross and Wallmark [23] and Dorda and Pulver [9] did not treat the storage characteristics of the memory device. It was White and Cricchi [28] who modeled both the erase/write and storage characteristics with WKB approximation to obtain the tunneling current through the oxide.

WHITE-CRICCHI MODEL : This work, which treats the case of discharging, including the changing rate of charge transfer, essentially assumes that:

1. Charge loss occurs by direct tunneling from the nitride traps to interface traps at the same energy level, lying within the silicon band gap and at the interface between silicon and silicon dioxide.

2. Nitride traps are at a single level and spatially localized, i.e.,

   $$N_t(x,E,0)=N_o\delta(x)\delta(E-E_o)$$

   The interface trap distribution can be written as:

   $$D_{it}(t)=D_{it}(E_o)exp(\frac{V_{ox}(t)}{V_s})$$

   , where V_s is a characteristic potential reflecting the slope of the $Si\text{-}SiO_2$ interface trap distribution.

3. The oxide current J_{OD} in the barrier region is evaluated using WKB approximation and the Fermi's Golden Rule.

Fig. 2-1 illustrates the exchange of charge between the nitride trapped charge and the Si-SiO_2 interface traps. The expression for the change in threshold voltage is:

$$\Delta V_{TH} = -\frac{V_T^-}{1+\frac{V_T^-}{V_s}}\left(1+\frac{C_{ox}}{C_N}\right)ln\left(1+\frac{t}{\tau_D}\right)$$

where

$$\tau_D = \frac{C_{ox}C_N V_T^-}{\left(1+\frac{V_T^-}{V_s}\right)J_{OD}(t=0)}$$

$$V_T^- = \frac{1}{X_{ot}}\left(\frac{2\hbar^2\phi^-}{qm_B^*}\right)^{\frac{1}{2}}$$

ϕ_B^- is the barrier height for electrons.

2.2 Later Models

The early model was proposed in 1972. The experiments on retention in the subsequent years were suggesting that direct tunneling is not totally appropriate for modeling retention. This is because the logarithmic dependence of decay when extrapolated for long times did not predict the observed retention curves and the charge centroids in the nitride was more than the maximum tunneling distance calculated by Ferris-Prabhu [22]. The threshold voltage ΔV_{TH} is related to the charge Q_N trapped in the nitride and the charge centroid x_N by:

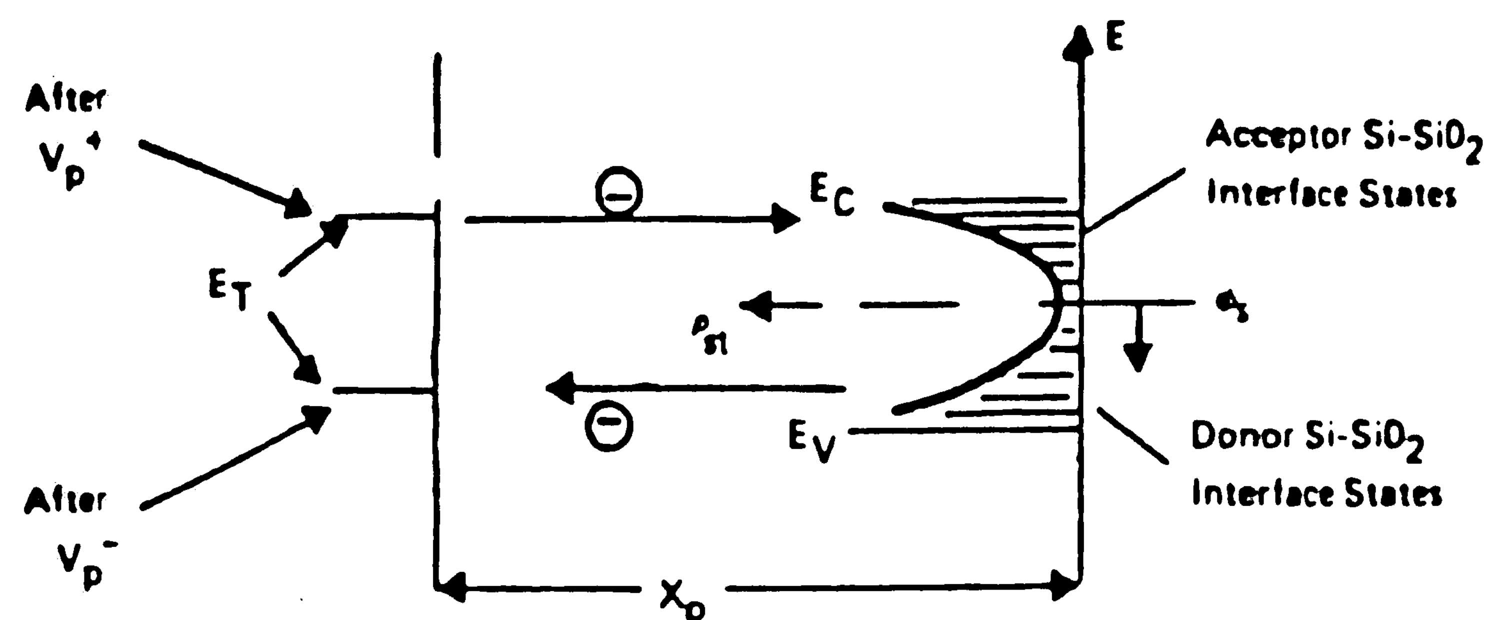


Fig. 4. Tunneling from deep traps to Si–SiO2 interface states.

Figure 2-1: Tunneling from deep traps to Si-SiO_2 interface traps.

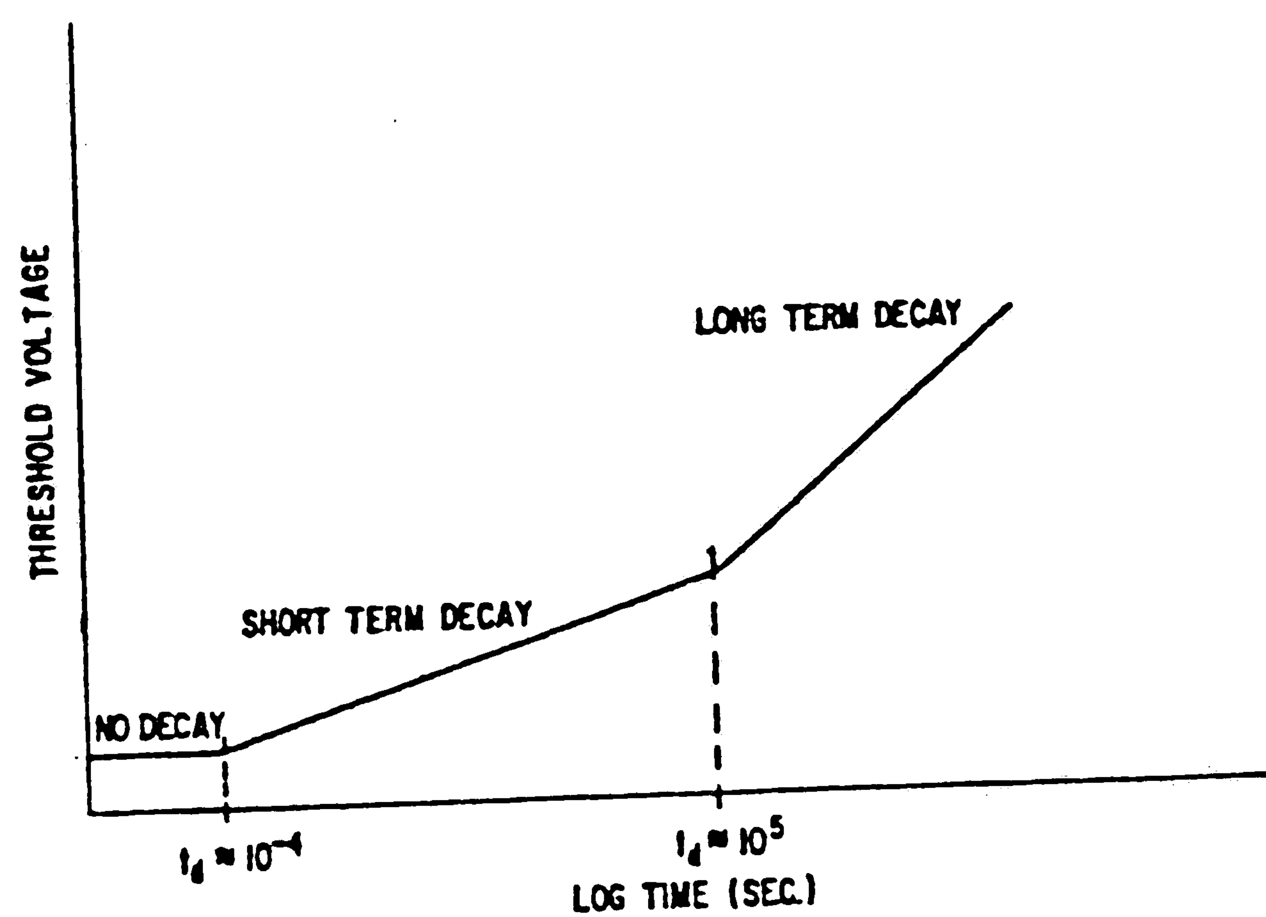


Figure 2-2: Three regimes in a retention plot.

$$\Delta V_{TH} = \frac{Q_N}{\epsilon_N}(x_N - \bar{x}_N)$$

This suggests that the loss in memory can be accounted with loss of charge , increase in charge centroid or both. Neugebauer and Burgess [18] discussed the retention characteristics in terms of three time regimes. For times of the order of few microseconds no decay was reported. Till around 10^5 seconds the decay was classified as **short term** and the dominant decay process was identified as "back-tunneling" of charge from the nitride. Beyond the short term decay regime the decay rate increased and the decay was termed as **long term** and the dominant process was attributed to rearrangement of stored charge in the nitride; see fig. 2-2.

In the remaining section three models will be discussed which attempted to resolve the issue of long term decay. All these models tacitly agree that short term decay is back tunneling of charge from the nitride traps to the silicon. The models predict enhanced decay for long term retention by considering different thermal and electric field effects on nitride conductivity. A comparison of the three models is in table 2-1. The details of the models is being summarised below:

- LUNDQUIST's MODEL [17] : The nitride trap distribution is assumed to be continuously distributed in energy from depth ϕ_{min} to depth ϕ_{max} (below the nitride conduction band). Direct tunneling and thermal excitation processes have been treated as independent. In the model: t_d marks the beginning of the decay; λ is the mean path for trapping; α_N is the tunneling damping factor and τ_o is the inverse

Author	Processes Included	Expression
Lundquist 1976	(1) Direct tunneling discharge (2) Thermal excitation discharge	$V_{FB}=V_{FB}(0)(1-r_r log\frac{t}{t_d})M(\frac{kT}{q}ln\frac{t}{\tau_o})$
White 1977	(1) Direct tunneling discharge (2) Cycling enhanced J_N and J_O	$\frac{\partial V_{TH}}{\partial t}= - C_N^{-1}(J_N+J_O)$
Lehovec 1978	Frenkel Poole discharge	$V_T(t)-V_T(\infty)\approx x_N\beta^{-2}ln^2[\nu t exp(-\phi)]$ for i[t]$\gg$ 1 sec.

Table 2-1: Comparison of the retention models incorporating long term decay

of the attempt to escape frequency. Further more:

$$r_r = \frac{2.3}{\lambda \alpha_N}$$

and

$$M(\phi) = \frac{1}{N_t} \int_{\phi}^{\phi_{max}} d\phi \frac{\partial N_t}{\partial \phi}$$

- WHITE's MODEL [29] : This model assumed that there is charge trapped near the nitride-oxide interface. The back-tunneling is from the nitride traps to the Si-SiO_2 interface traps like in the early model. The effect of cycling is to increase the Si-SiO_2 interface trap density and thus increase decay rate but the threshold voltage decreases because the nitride conductivity is increased by cycling and the charge moves into the nitride. The oxide tunneling current can be expressed as:

$$J_O = a Q_I D_{it} e^{-\beta x_{ot}} = \frac{Q_I}{\tau}$$

where, J_O is the oxide tunneling current, Q_I is the stored charge in the nitride, a and β are constants, D_{it} is the Si-SiO_2 interface trap density and x_{ot} an effective tunneling distance for the centroid of the stored charge. Thus, to first order, the short term decay rate is proportional to the initial stored charge, the Si-SiO_2 interface trap density and the negative exponent of the effective tunneling distance. The long term charge retention characteristics are influenced by the nitride current density J_N and its variation under prolonged cycling.

- LEHOVEC's MODEL [15] : This model assumes mono-energetic traps. The emission of trapped electrons by Frenkel Poole mechanism is considered, where, the escape rate of traps is:

$$\frac{\partial n_t}{\partial t} = -n_t \nu \, exp[-\phi + \beta(E)^{\frac{1}{2}}]$$

and ϕ is the trap depth (normalized to kT/q); n_t is the trapped charge; E is the electric field; ν is the escape attempt frequency of nitride traps. The movement of the charge centroid is neglected. The expression for retention is valid for zero bias retention.

Chapter 3
DYNAMIC CHARACTERIZATION

3.1 Introduction

Dynamic characterization in our context would include:

- erase-write, which is a measure of voltage and speed of programming of the memory device.
- retention, which is a measure of memory after programming.
- endurance, which is a measure of repetitive cycling effects on the device.

From the stand-point of experimentation all the above three characteristics require the following capabilities:

1. Application of voltage pulses of variable magnitude and time duration on the gate of the device with respect to the substrate, source and drain.
2. Detection of the threshold voltage (or flat band) with a variable time-delay after step 1 and is referred to as read delay.
3. Maintenance of all device terminals at a single potential for time excluding steps 2 and 3 in-order to realistically model a powered-down state.

Different combinations of the steps 1, 2 and 3 are required for the three different characterization and each contributes to the complexity of instrumentational realizability. Another important factor for instrumentation is that it should be computer-aided and automated for data acquisition with minimal experimentor intervention.

3.2 Test Vehicles In Literature

Dynamic characterization of MNOS devices in literature can be classified in terms of the technique used for threshold detection. In the case of capacitive test structures the following methods have been used:

1. Observing shifts in the high frequency C-V traces as a function of time; see fig. 3-1. This is one of the easiest methods requiring no specialized instrumentation. Many investigators have used this method; more recently used by Şuzuki et.al. [24].

   One of the disadvantages of this method is that it's very slow (read delay >100ms) and does not reflect the actual transient situation.

2. In order to study back-tunneling effects in MNOS capacitors B.H.Yun [31] introduced a feedback operated flatband and charge release monitoring scheme as shown in fig. 3-2.

   This method offers decreased minimum read delay capabilities (limited by 1ms settling of the phase locking amplifier). Secondly it provides data regarding charge transport and discharge of MNOS

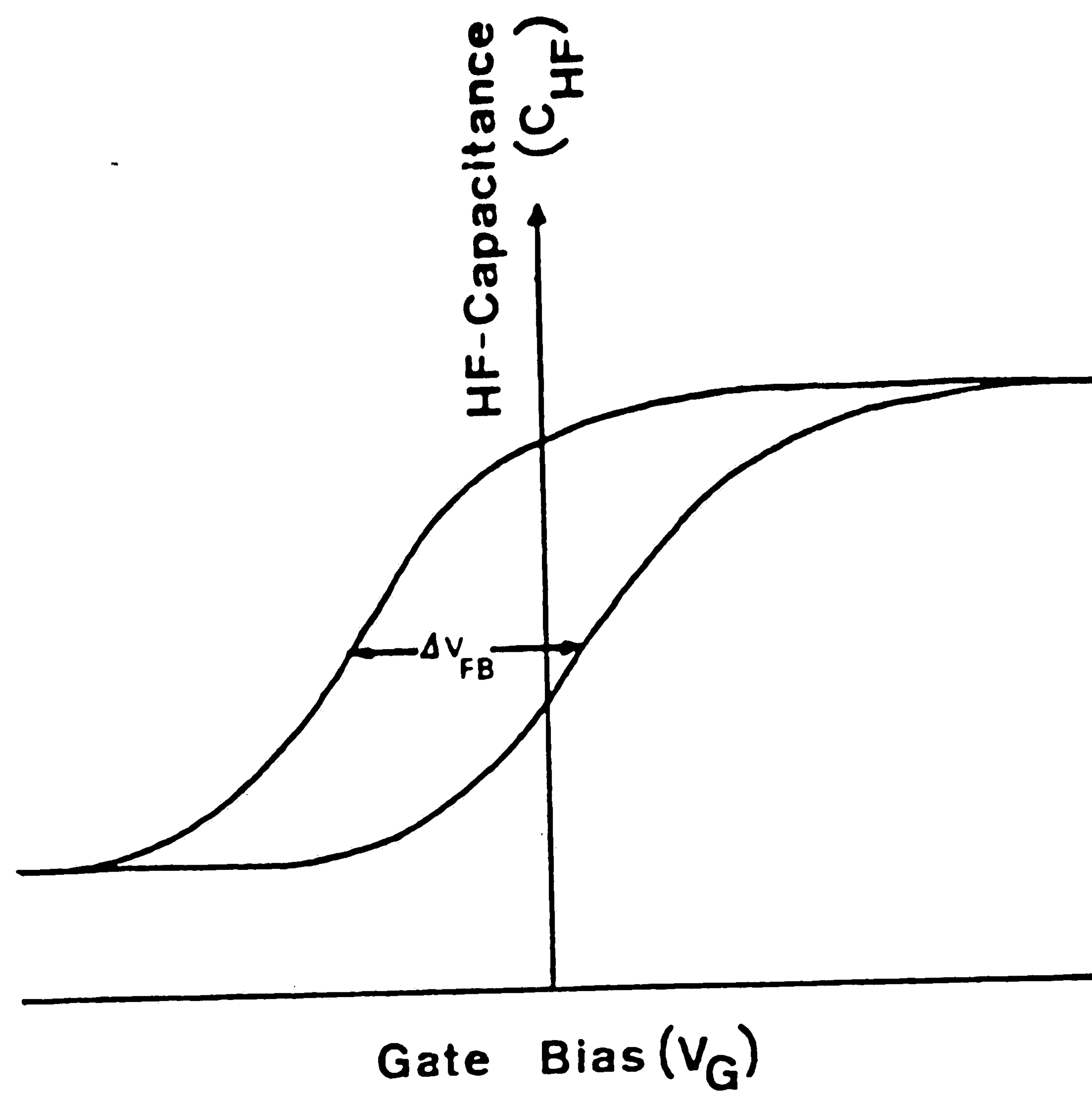


Figure 3-1: Flat band shifts in HF-CV plots

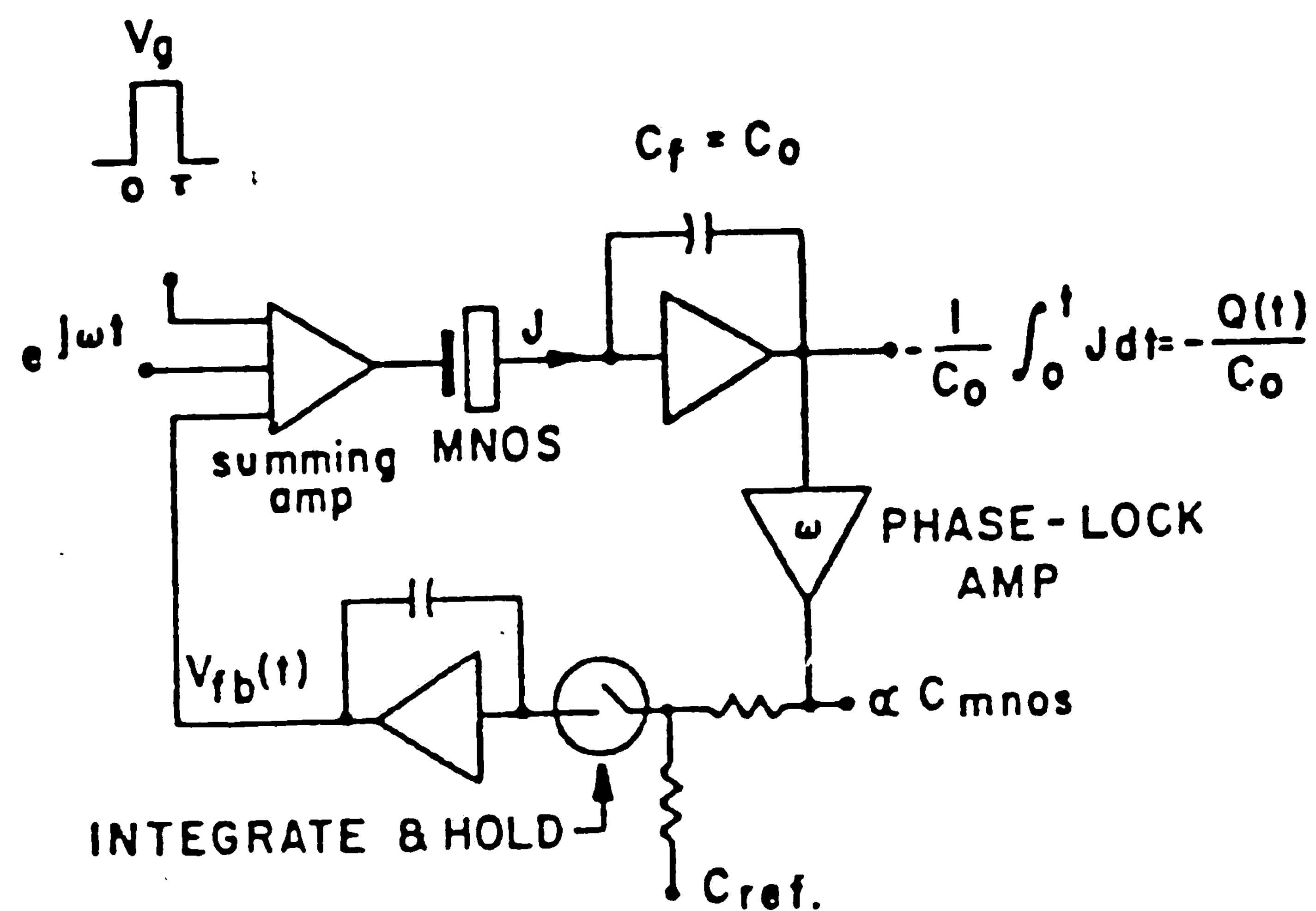


Figure 3-2: Flat band circuit "holds" during the pulse and searches for the new V_{FB} at $t > t'\{t'-\tau \approx 20ms.\}$.

devices. It also provides a step towards automation of data acquisition.

One of the problems inherent with a capacitive structure is the write state, because minority carriers have to be supplied by artificial means like optical excitation.

With transistor test structures the following techniques have been used for monitoring threshold voltage with write/erase capabilities:

1. This method uses static I-V characteristics and employs the shift of the threshold voltage(see fig. 3-3).

   It's inherently slow as it's capacitance counterpart technique 1 discussed above, short term retention measurements are impossible.

2. This method uses realistic conditions of erase-write and read operations and was used by White et.al. [28], refer fig. 3-4 for the schematic of the test station.

   The threshold detection scheme is referred as "source follower-constant current method of threshold detection" [12]. With this test station fast measurements were achieved. The threshold voltage was measured as the gate to source voltage for a given read voltage, but did not take into account the following:

   - The sense-current for threshold depends on the threshold voltage

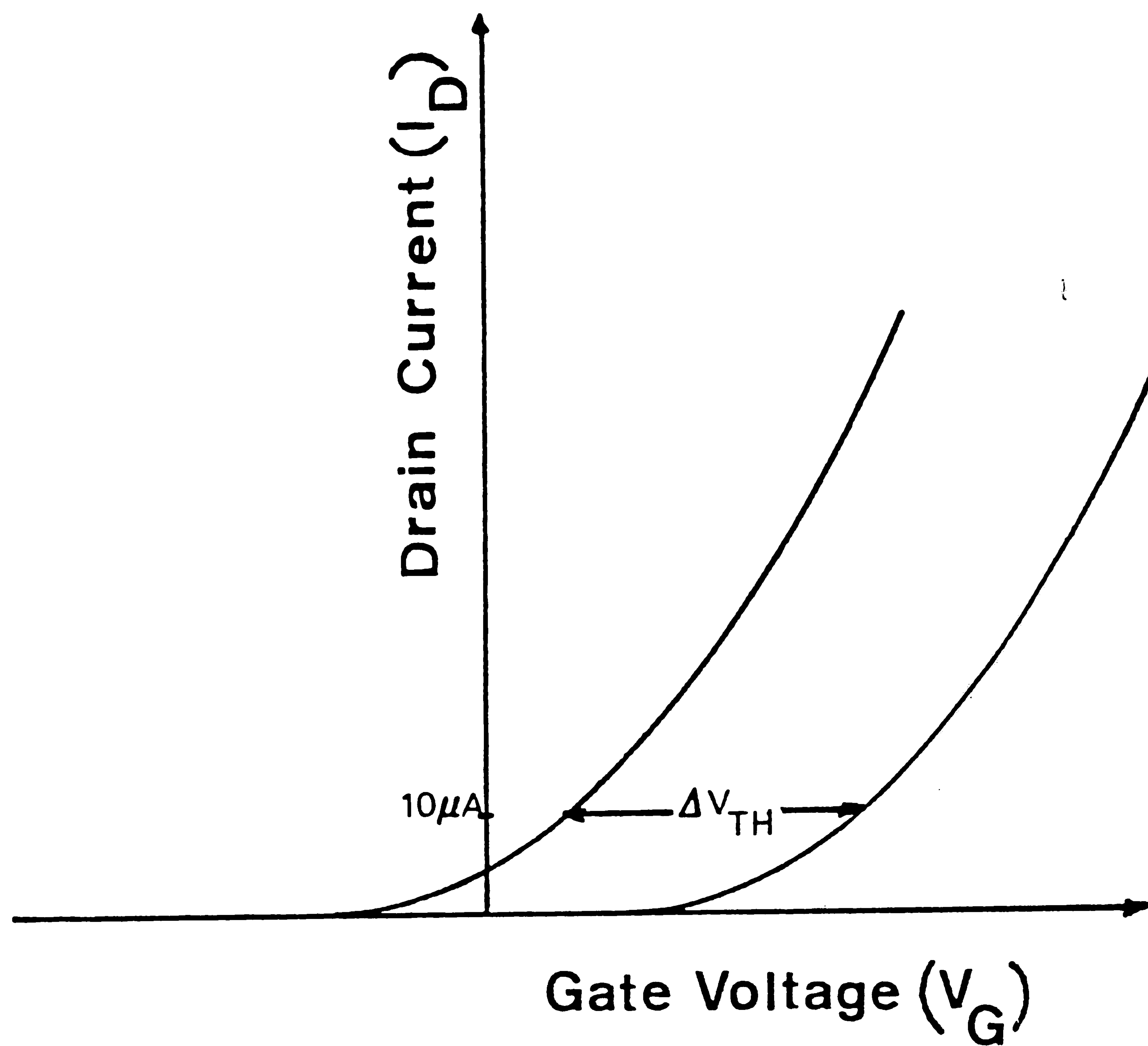


Figure 3-3: Threshold detection with static I-V characteristics

itself.

- There is a substrate to source potential, so there is a varying contribution of substrate bias to the threshold.

Another problem with this setup is that it uses 3 pulse generators and so data acquisition is very operator intensive and very expensive to automate using programmable pulse generators.

3. Another method of threshold detection is referred as "saturated drain-constant current method" [12]. Fig. 3-5 shows the circuit configuration. In this scheme the read pulse produces a constant current for the transistor, and the gate voltage through the opamp. feedback settles at the threshold voltage. An improved threshold detection scheme has been used by F.R.Libsch [16]. The problems involved are that the sense-current value limits the charging of stray capacitance at various nodes of the DUT. Secondly, to accomodate the write-erase capability to this threshold detection scheme there are possibilities of the opamp going into saturation, and also the opamp races to saturation during the initiation of the read, since the feedback depends on the transistor being turned-on.

With this overview of the test vehicles used by different investigators I will present my test-station design and implementation and how it tries to attend to the various challenges discussed in this section.

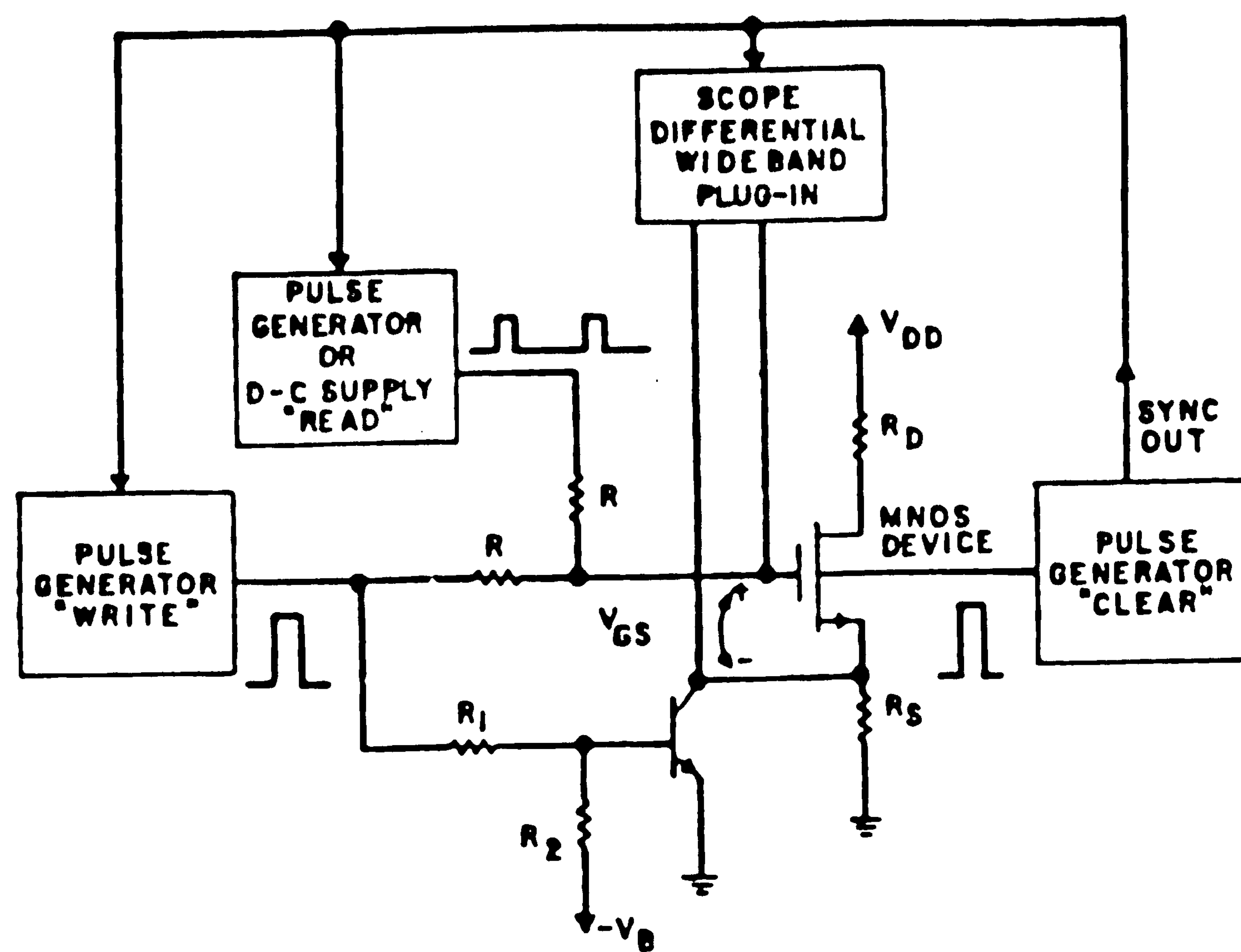


Figure 3-4: Test station using source follower threshold detection.

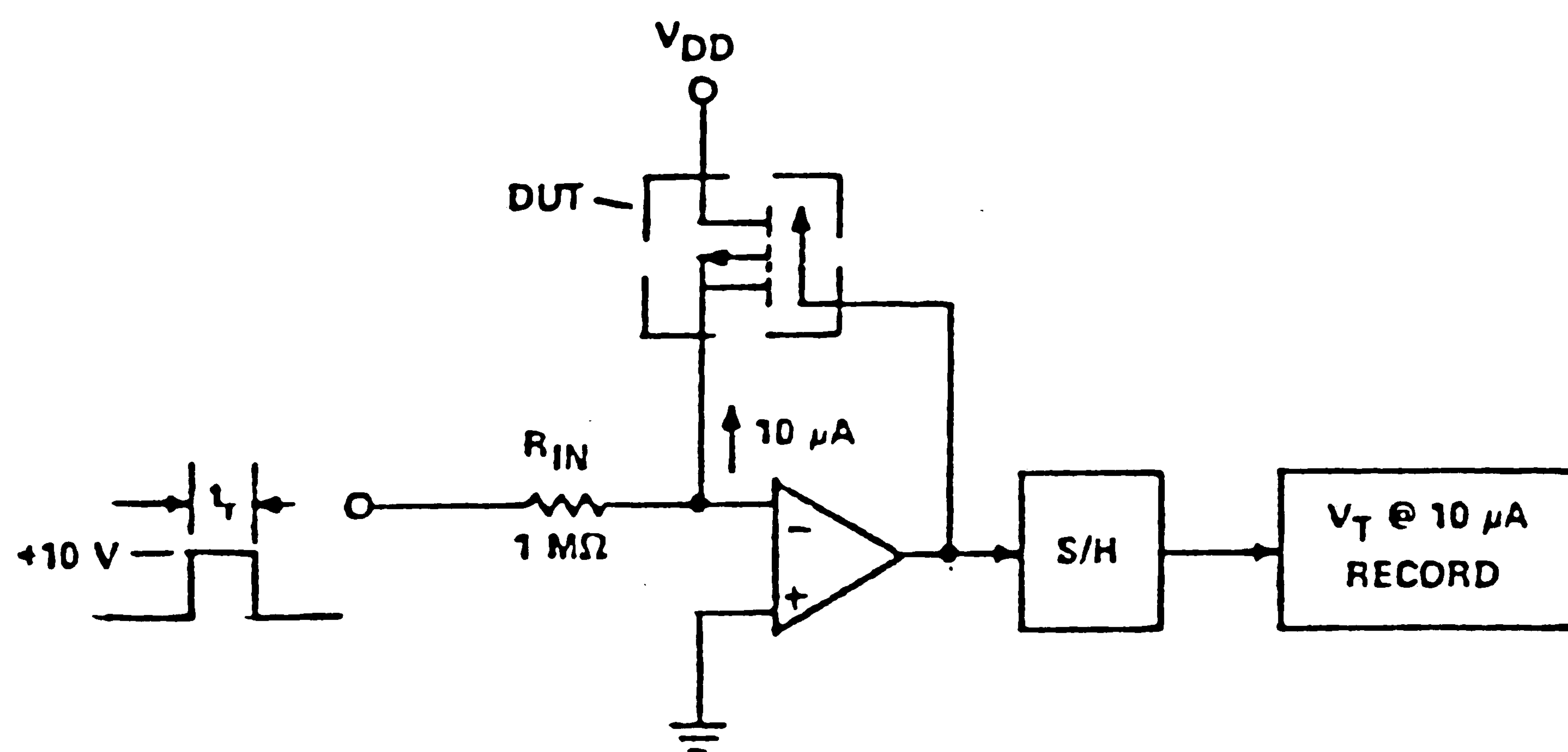


Figure 3-5: Circuit schematic for saturated drain constant current method.

3.3 My Test Vehicle

In order to address the requirements of fast erase-write and read together with the flexibility for both n-channel and p-channel device characterization, an analog W/E and READ circuit was designed with digital controls. The automation for data acquisition was taken with the design of a digital pattern generator for providing digital controls to the W/E and read circuit.

Before the test station is described the design and features of the two new instruments will be detailed in the next subsections.

3.3.1 W/E & Read Circuit

The schematic circuit diagram is shown in fig. 3-6. The operational amplifiers 3 and 4 form a current source as well as provide a unity gain buffer for the source of the DUT. Opamp 1 and 2 constitute a current sense amplifier and are used as a proportional feedback element for the current source voltage reference, during the read mode. The current source senses the threshold at a current level of $10\mu A$. The value of the current source is related to V_{REF} by $I = V_{REF}/50k\Omega$. The feedback increases the current source output current, for zero drain voltage, by a factor of 10; in order to facilitate the charging of stray capacitances at the source and drain. All opamps operate in the linear region and so the unnecessary saturation delays and unwarranted stressing of the DUT (because of opamp saturation) are avoided. The switches SW1-SW3 are fast settling MOS analog switches. The digital (TTL compatible) controls for these switches are utilized to obtain various modes of operation for the DUT viz., erase-mode, write-mode, read-mode, and idle-mode. The schematic representations are shown in fig. 3-7.

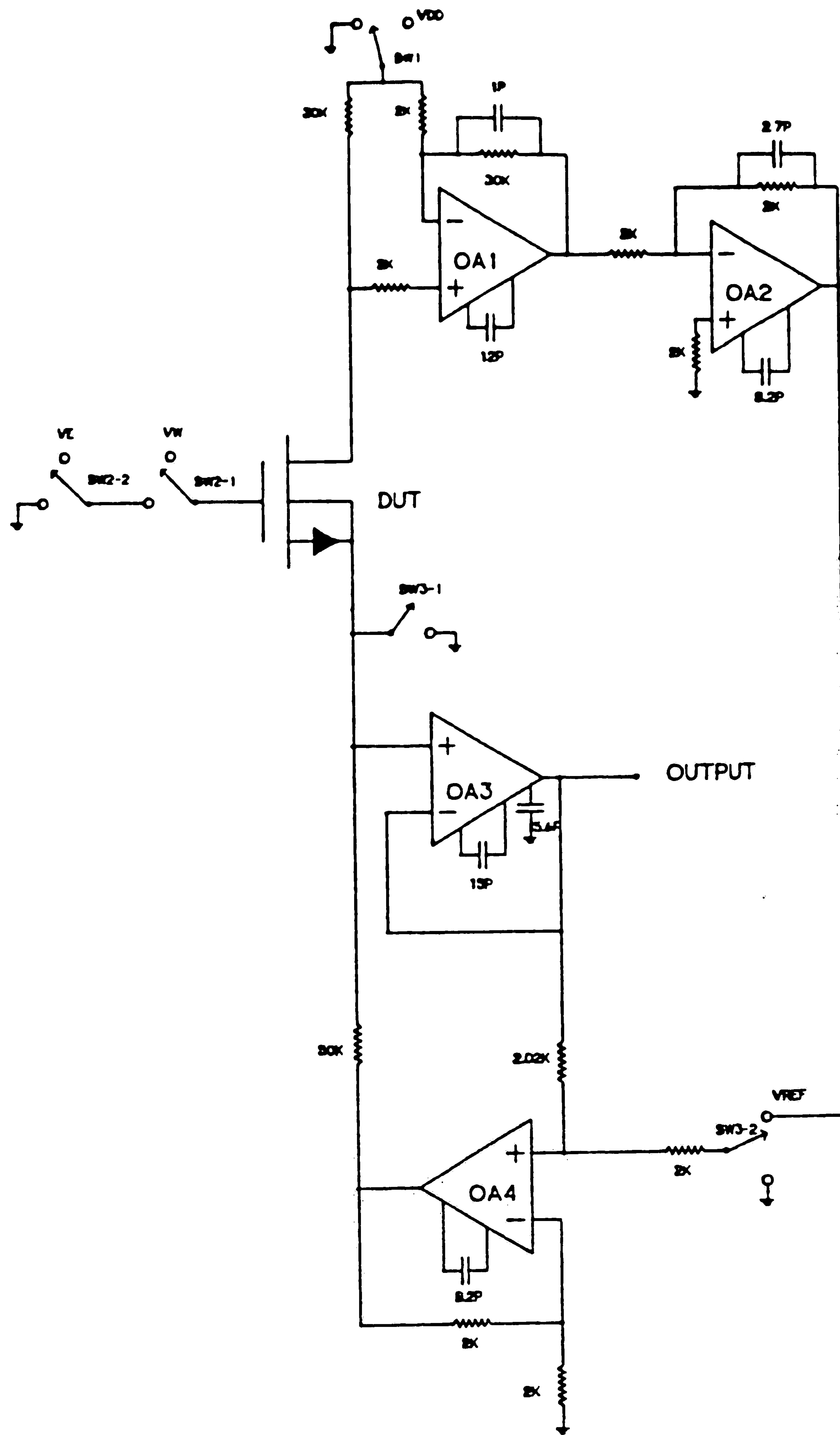


Figure 3-6: Schematic circuit diagram of the W/E & Read Circuit.

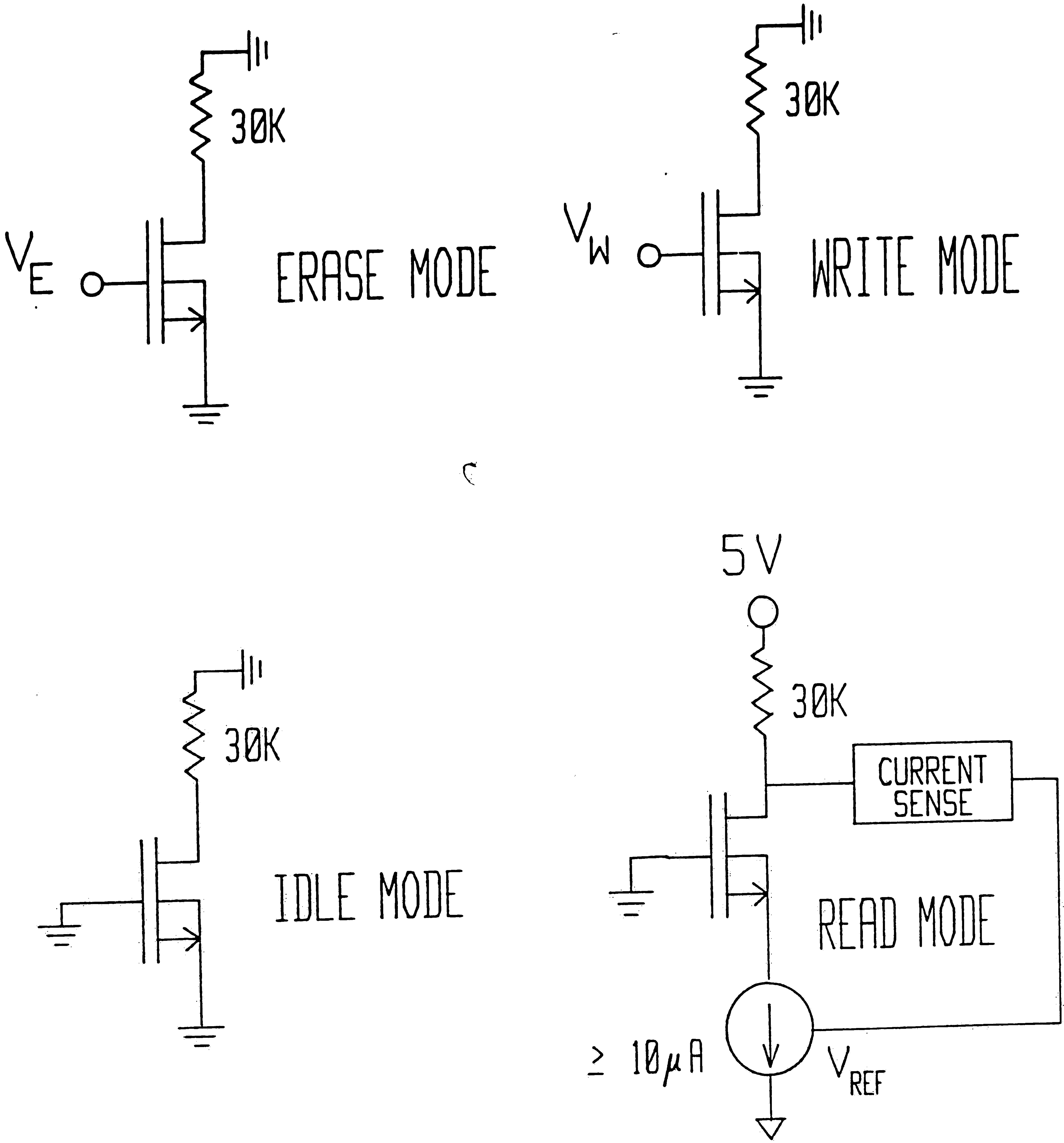


Figure 3-7: Simplified representation of the W/E & Read Circuit for different modes of the DUT during characterization.

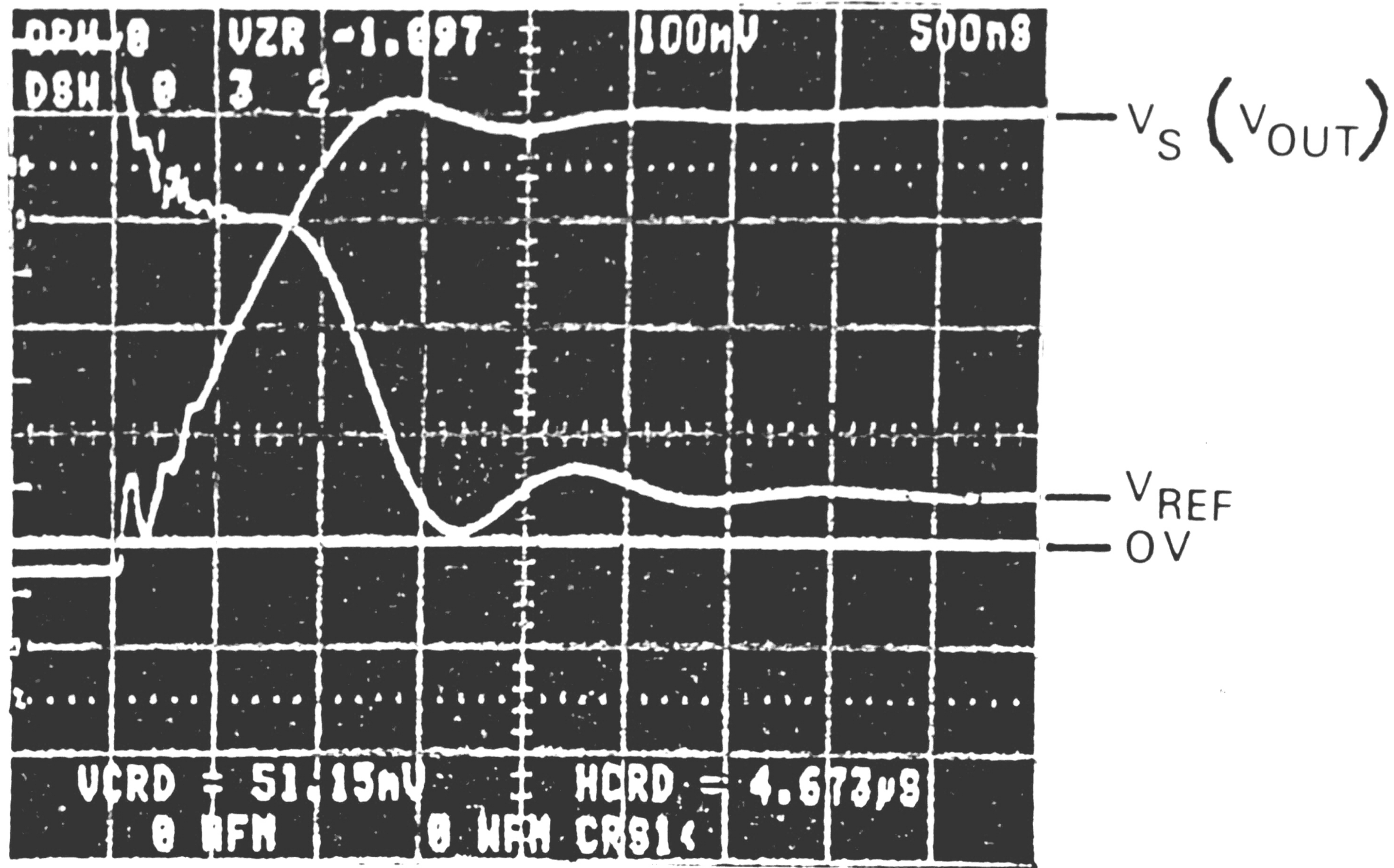
In the read mode as the gate is grounded, the source voltage adjusts to a value so that V_{GS} supports a current of 10μA. So the "threshold voltage" is negative of the source voltage. The current source has been designed and implemented to provide high output impedance and bidirectional current , under bipolar output voltage.

The threshold can be sensed after a few microsecond delay after a write/erase operation. The feedback settling time, the charging of parasitic capacitances and switching of analog switches account for the delay. Fig. 3-8, shows a photograph of the sampled threshold voltage after a write operation, together with the reference voltage to the current source. It illustrates the current pumping action of the current sense feedback. The transient analysis of the circuit during threshold detection is in appendix

3.3.2 Pattern Generator

The Pattern Generator is a 8 channel synchronous, 10MHz, single board digital stimuli generator. It has a parallel interface to be programmed with a given "sequence" from any computer, but has been implemented using the AIM 65 microcomputer. A "sequence" relates to the assignment of a string of logic states to each channel for a given time, referred to as "pattern" and "delay" later in the description.

The AIM 65 microcomputer runs an interactive software package programmed in-house in its EPROM memory space for user specification of the sequence. The software is structured under a main driver routine, as shown in fig. 3-9.



P-MONOS , 10X PROBE

Figure 3-8: Photograph of the source voltage and V_{REF} during in the initial stages of threshold detection.

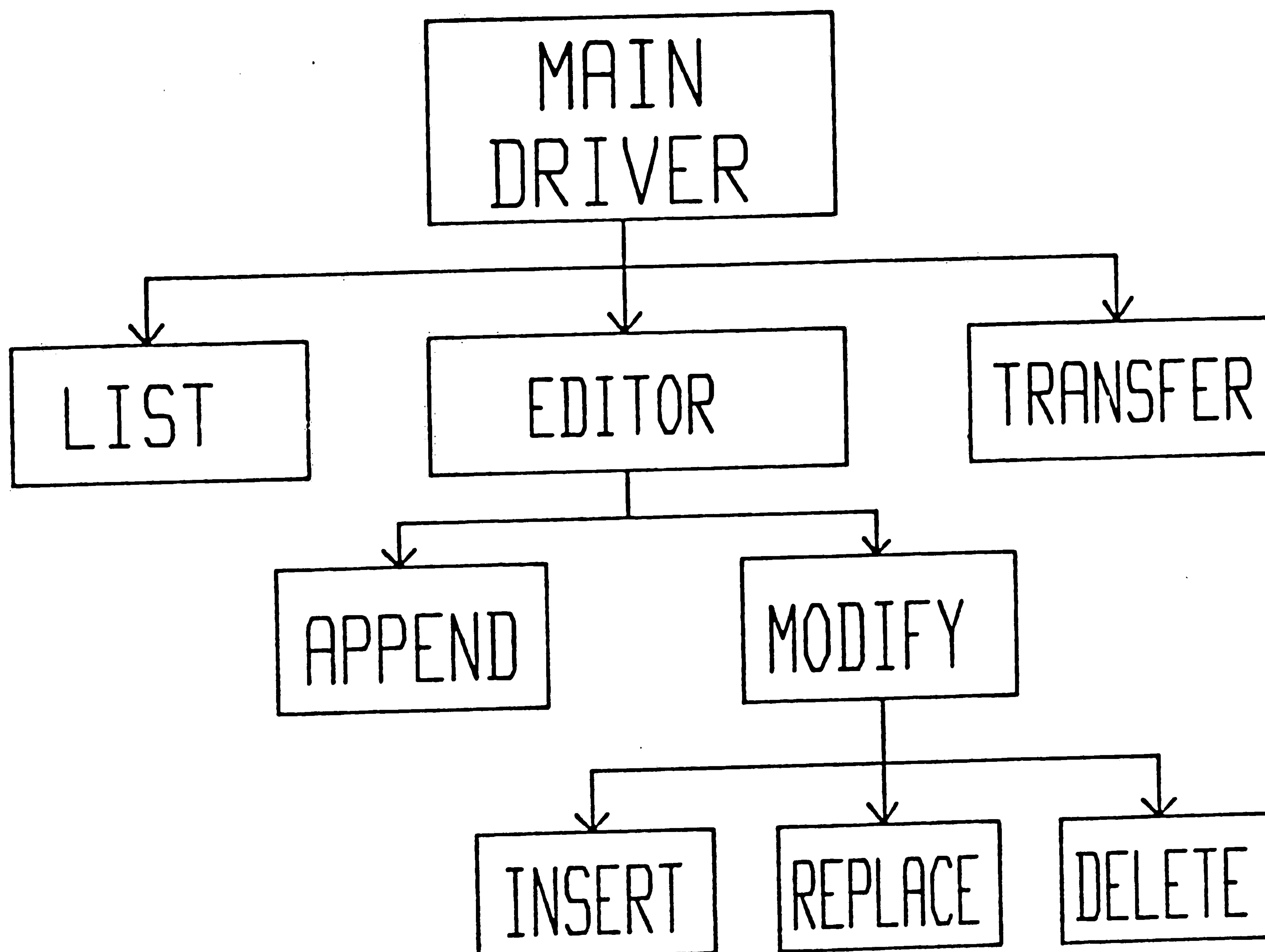


Figure 3-9: Software structure on the AIM 65 for pattern generation

A sample of the editing session is included in the appendix E. After the sequence has been edited it's transferred to the pattern generator, which must be in the "reset" mode. In the "reset" mode the outputs are cleared and the internal clock is disabled. The design of the pattern generator is insensitive to the speed of data transfer from the AIM 65. The circuit diagram and corresponding block diagram of the generator is shown in figs. 3-10 and 3-11.

The pattern is transferred in the PATTERN RAM and the dclay in the DELAY RAM. The RAM's are addressed with the SEQUENCER. The RAM's are in the write mode only during transfer from the microcomputer. The DATA BUS BUFFER only transmit durng the above mode.

When a sequence of pattern and delay is to be executed the generator is started and the 10MHz clock drives the count down of the delay loaded from the DELAY RAM into a 12 decade ripple DELAY COUNTER. The SEQUENCER senses the ripple out of the DELAY COUNTER and advances to the next item in the sequence. The pattern from the PATTERN RAM gets reflected at the output of the OUTPUT LATCH. The sequence repeats itself after the expiration of the last delay. This provides use for repetitive sampling and W/E cycling of the memory devices.

A sample of the pattern generator output is illustrated in the snap-shot in fig. 3-12.

The present implementation handles a maximum sequence length of 100

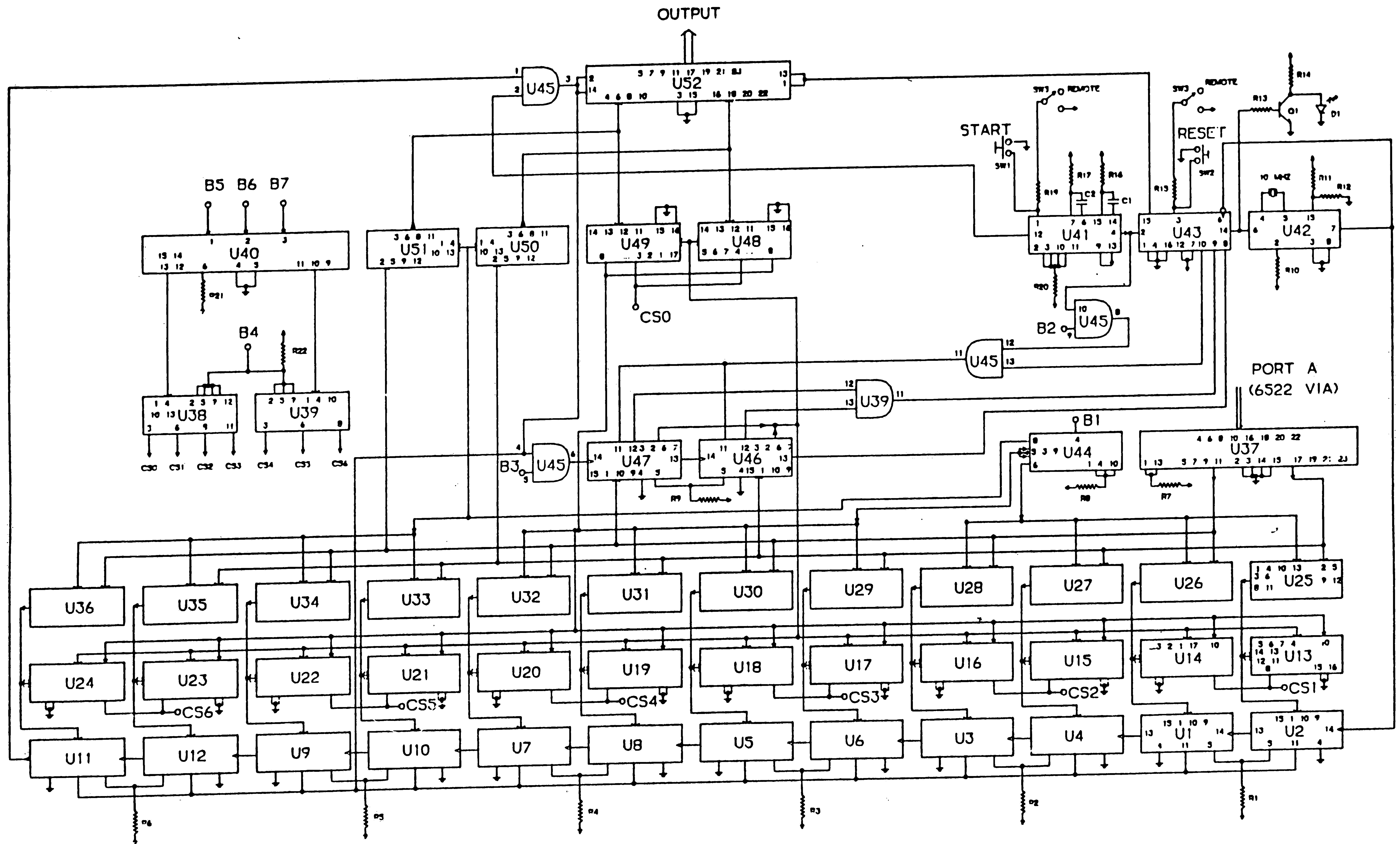


Figure 3-10: Pattern generator board circuit diagram

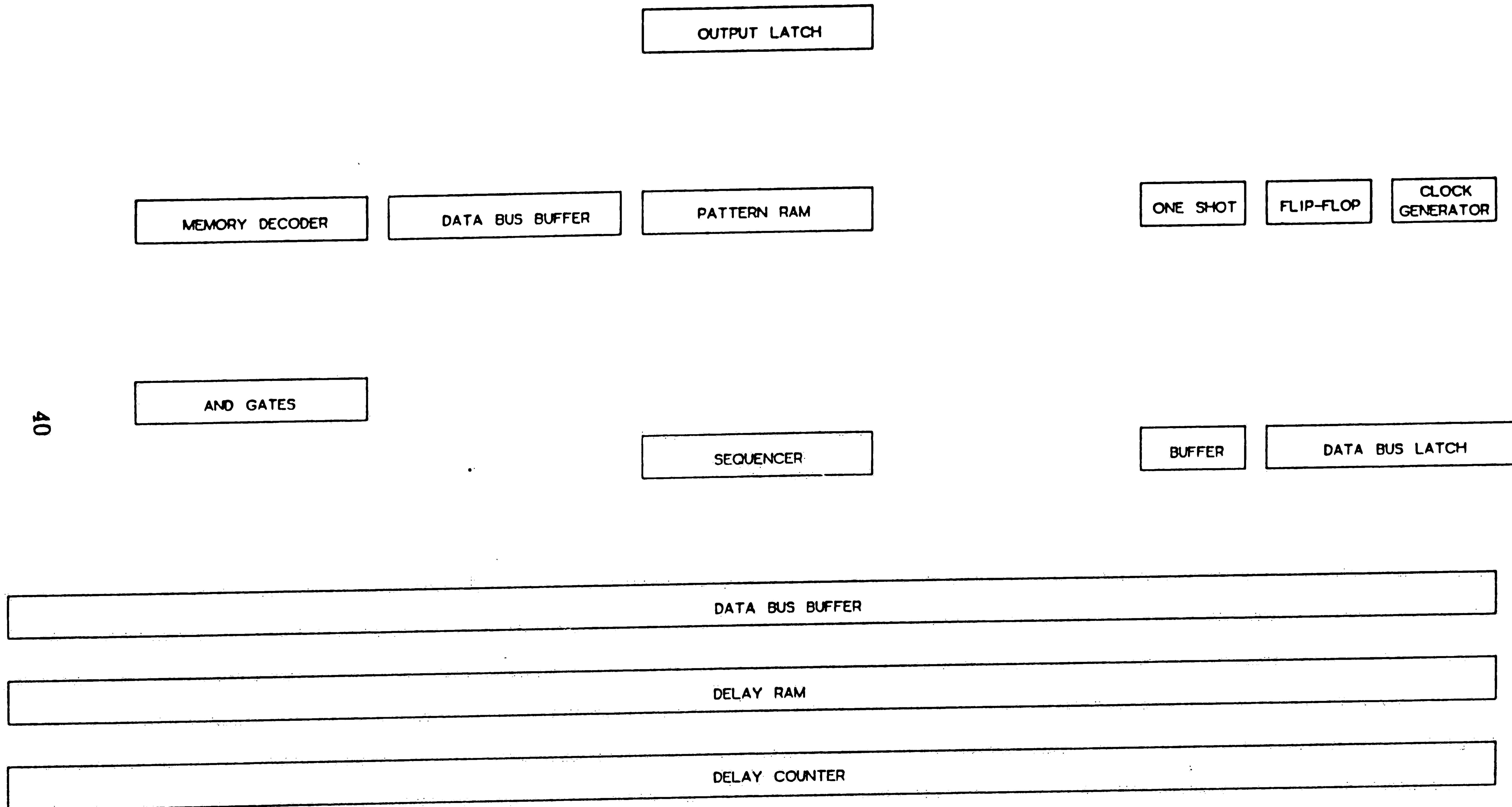


Figure 3-11: Pattern generator board block diagram

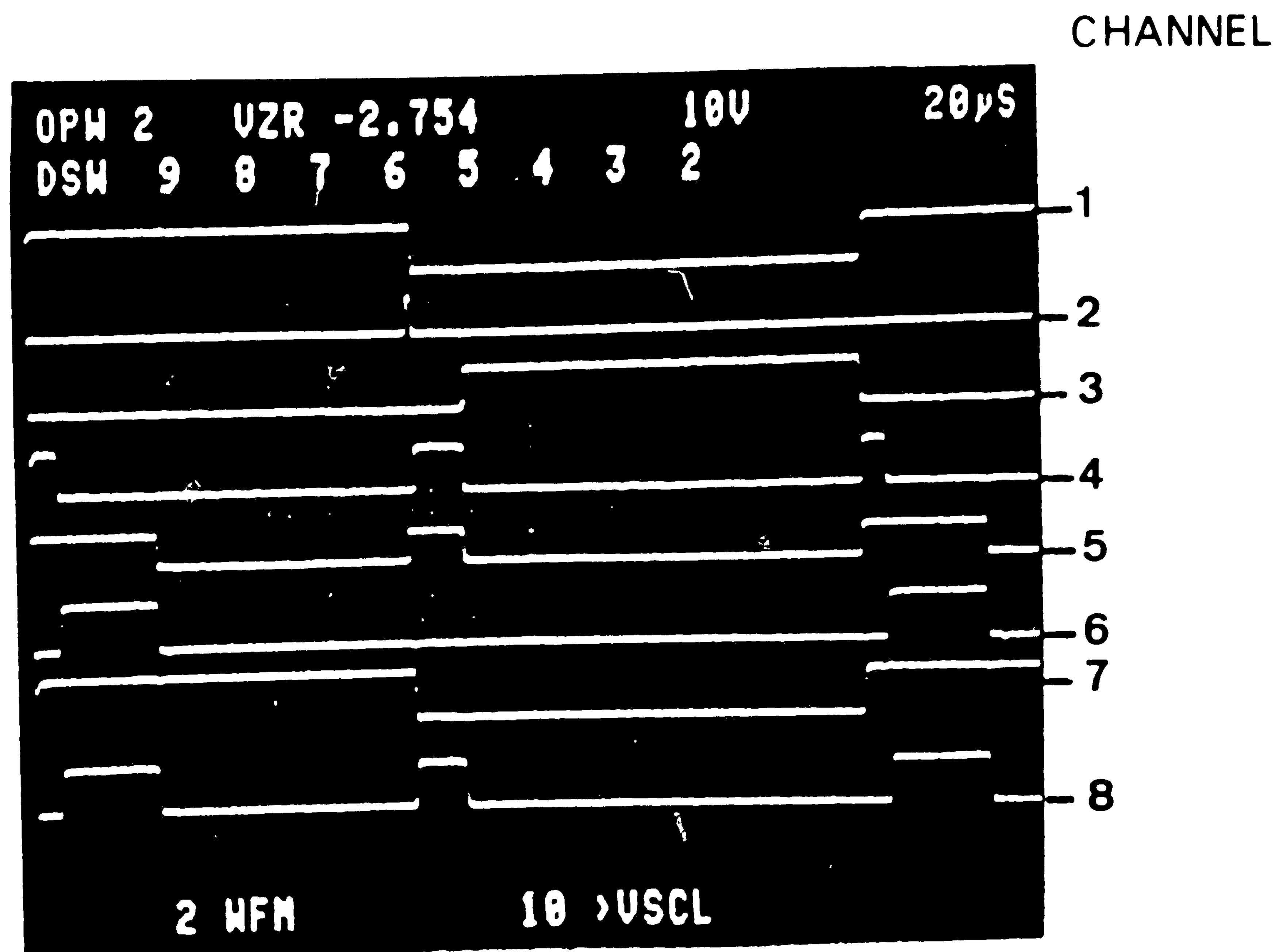


Figure 3-12: 8 synchronous channels of the pattern generator

with single delay specification ranging from 100ns to 99,000s. This is particularly attractive for memory dynamic characterization because between two adjacent patterns the time delay varies by several orders of magnitude. Most word generators available use read-out from RAM with a constant frequency clock and so the size of the memory necessary to obtain hours of operation with a 10MHz clock is enormous, and impractical. The generator also offers both remote and local modes of operation which is utilized for automatic data acquisition.

3.3.3 Test Station

The test station can be operated both in the local mode and remote mode using the versatility of the pattern generator and the IEEE interface of the TEK 7854 scope. The configurations are shown in figs. 3-13 and 3-14. The TEK 7854 scope is trigerred with the read logic controlling the W/E and Read circuit. Output of the Read Circuit is sampled. There is flexibility of single shot sampling with approximately 4μs resolution and 128 number of sample points; or one may do repetitive acquisition for increased bandwidth of sampling or signal averaging for noise reduction.

Multiple waveforms can be stored within the scope memory, or transferred for permanent storage on the disk in the remote configuration. This is useful for sequential reads after a write and/or erase operation.

A photograph of the test-station in the characterization laboratory is shown in fig. 3-15.

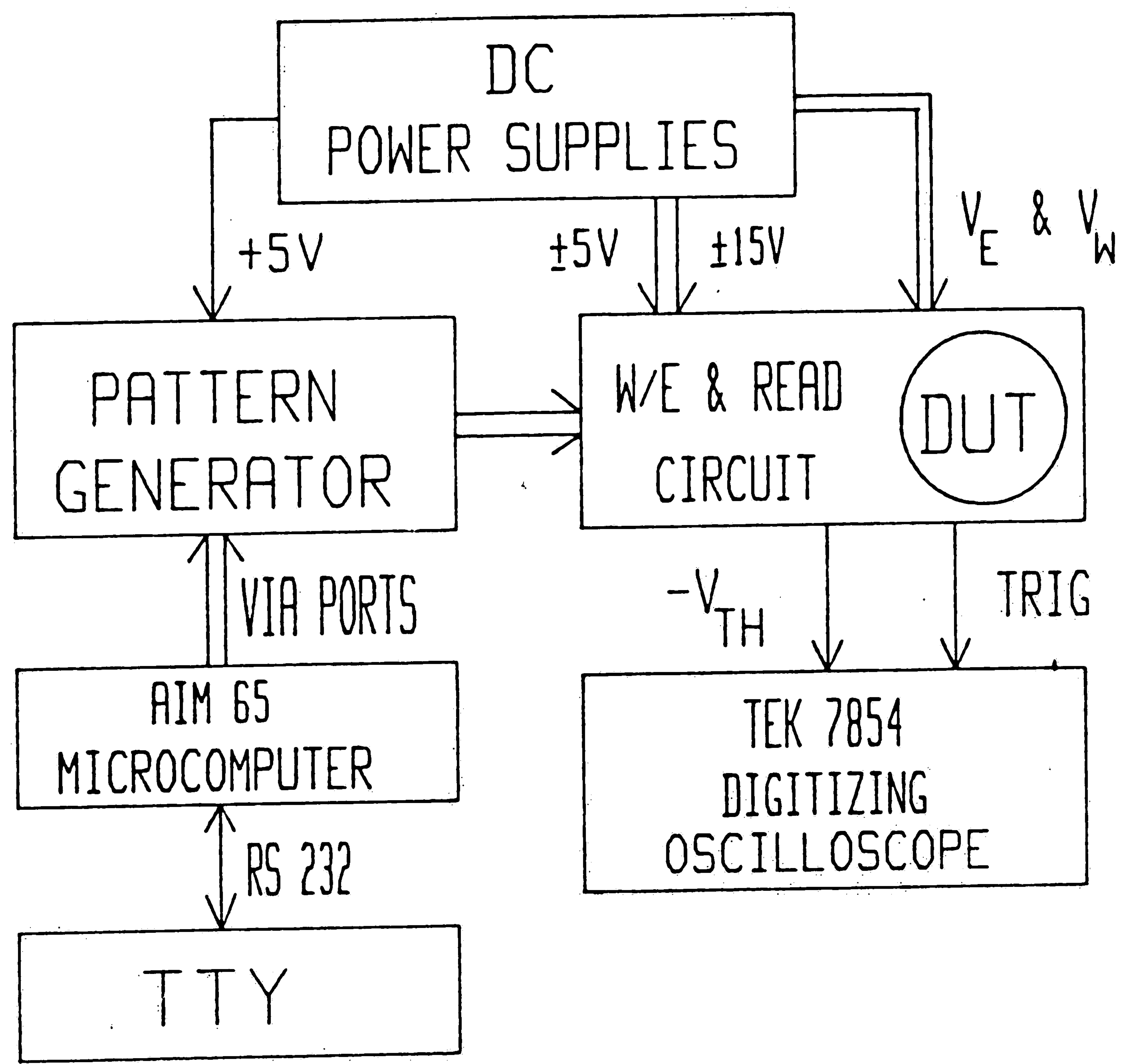


Figure 3-13: Test station configuration under local mode.

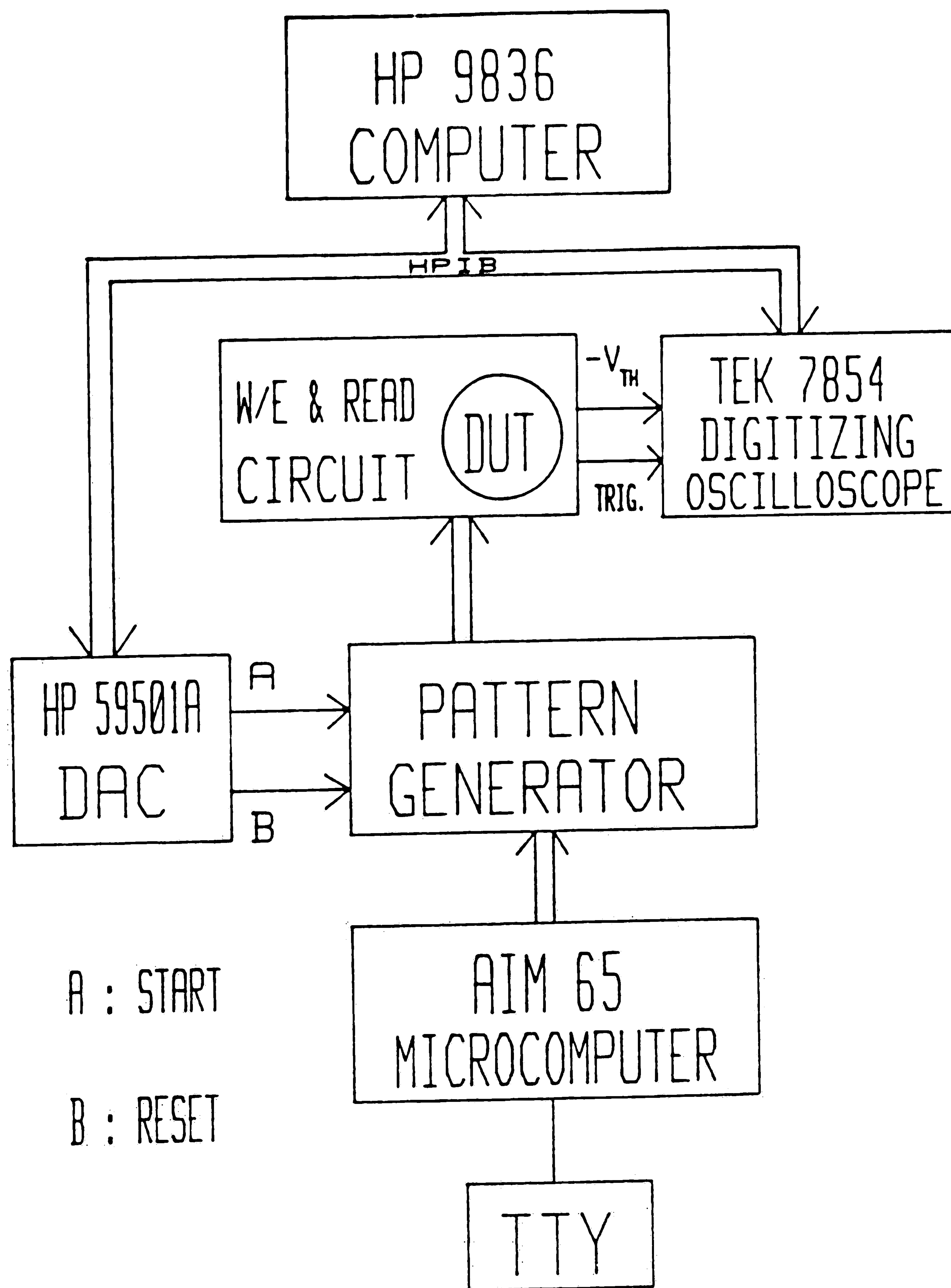


Figure 3-14: Test station configuration under remote mode.

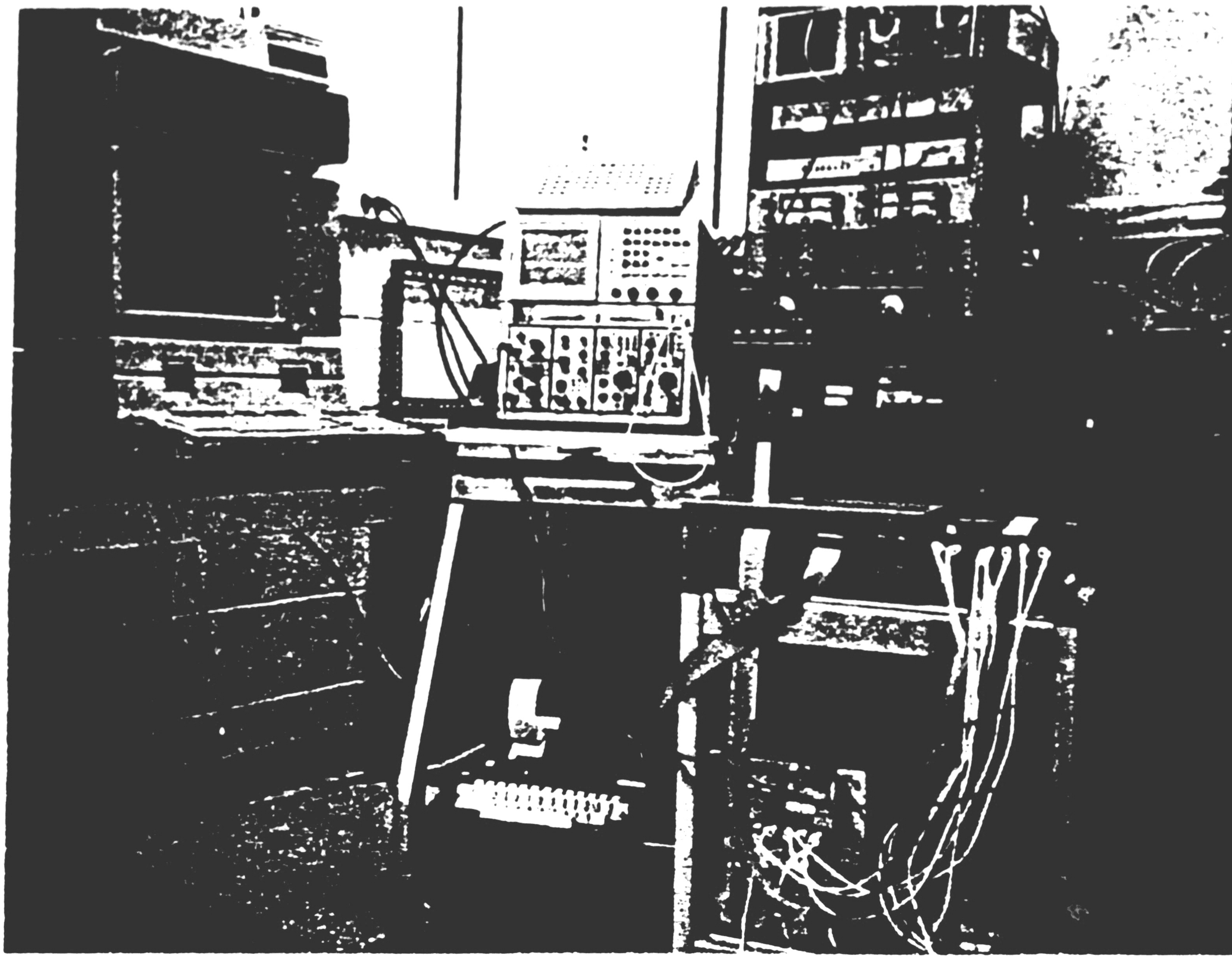


Figure 3-15: Test station with the HP-9836 computer controlled instrument panel in the background

Chapter 4
EXPERIMENTS

In this chapter experiments conducted using the test station detailed in chapter 3 will be discussed. Samples were complementary MONOS transistors fabricated in-house using the technology detailed in appendix D. The tunnel oxide thickness is 20A , nitride thickness is 85A and blocking oxide is of 51A thickness.

4.1 Erase-Write Characteristics

Erase-write characteristics uses ±10V programming voltages. In this measurement at first the device is written/erased for 10seconds and the change from that state is observed using a variable pulse width erase/write voltage; pictorially illustrated in fig. 4-1 for a p-channel transistor. The SEQUENCE used for the measurement is in appendix E.

In order to reduce noise the signal (threshold voltage) was averaged 5 times, on the TEK scope. The pattern generator was continually programmed for different erase/write and data obtained. Erase-write characteristics of p-channel and n-channel transistors are shown in figs. 4-2 and 4-3 respectively.

4.2 Retention Characteristics

Zero-bias retention characterization (for definition see chapter 1) has been done on the MONOS transistors. Retention characteristics were taken at ±10V programming level. For the erased state, the device is first written for 10sec., then erased for 100ms and read after variable read delay ranging from 100ns to 10^5s.

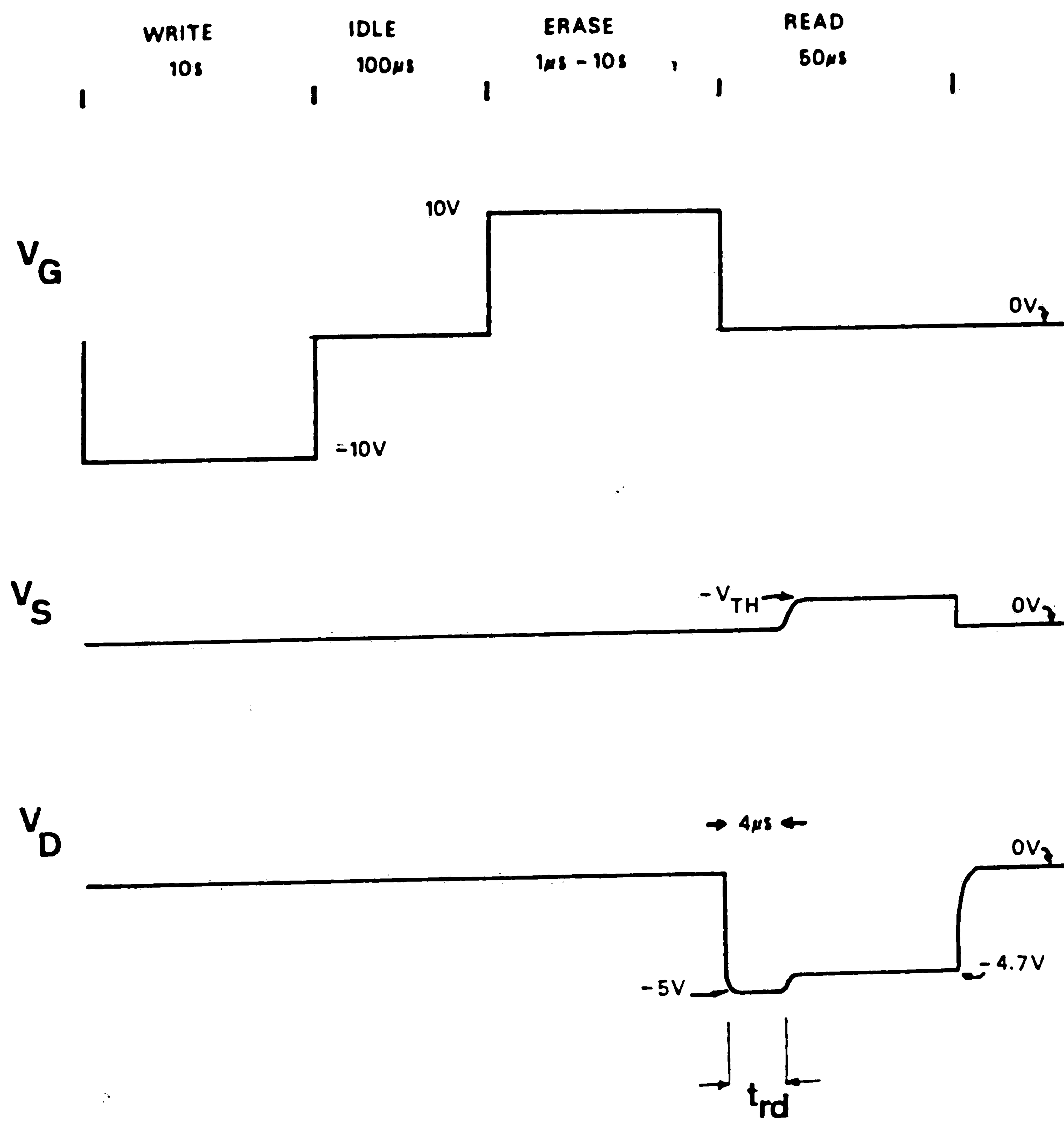


Figure 4-1: Erase-write pulsing sequence

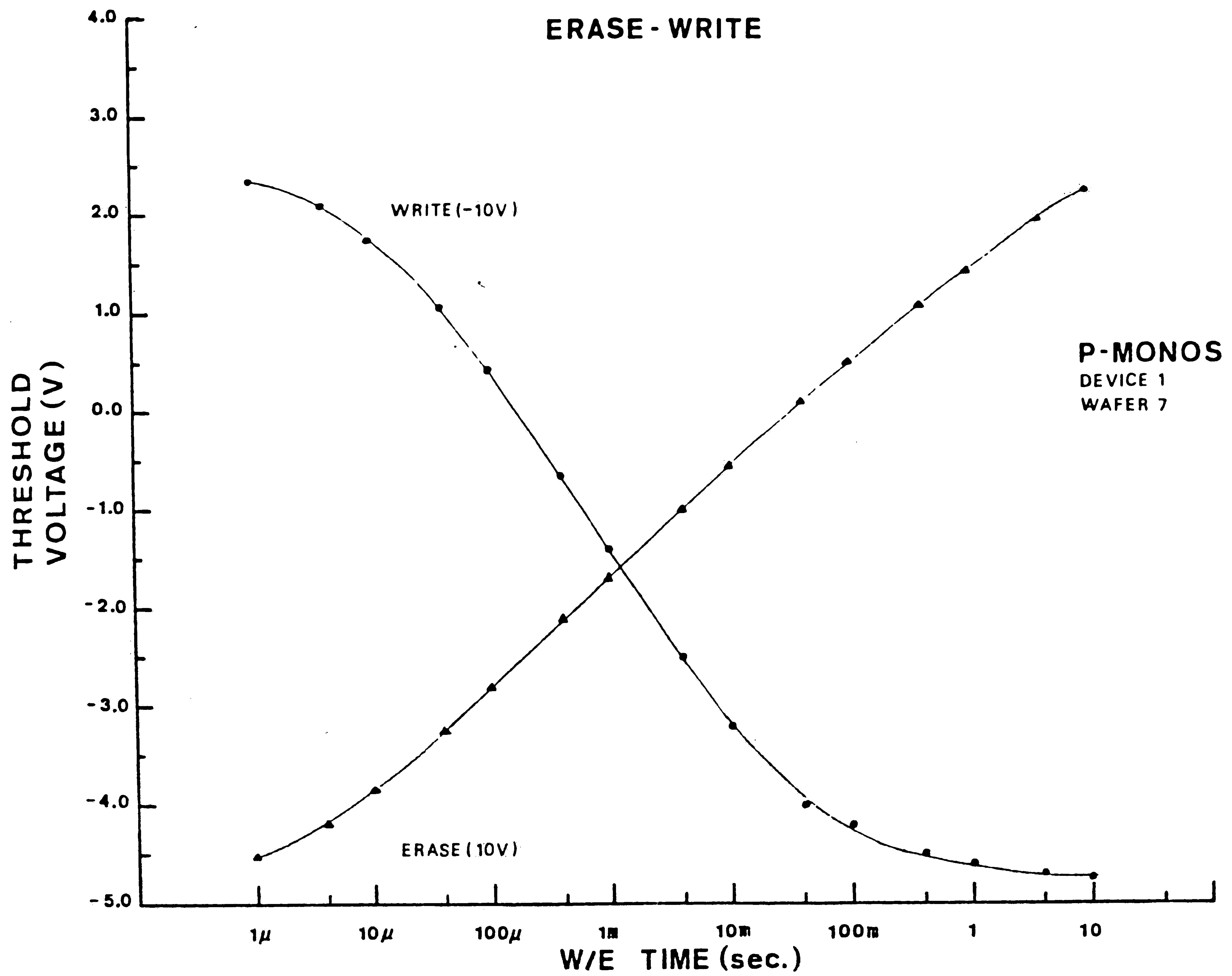


Figure 4-2: Erase-write characteristics of a p-channel MONOS transistor with x_{ot}=20A, x_N=85A and x_{oB}=51A

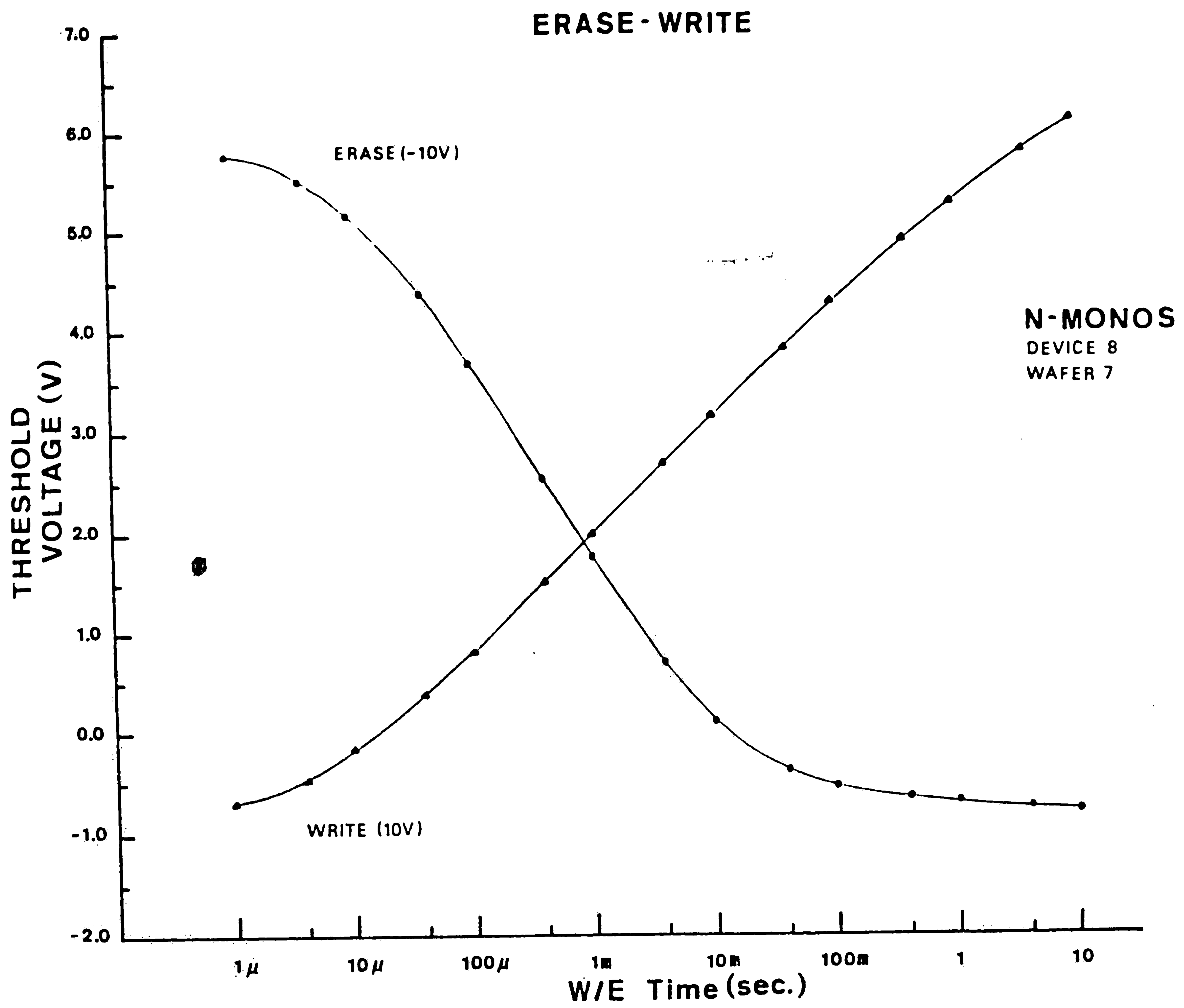


Figure 4-3: Erase-write characteristics of a n-channel MONOS transistor with x_{ot}=20A, x_N=85A and x_{oB}=51A

Retention measurements are partitioned into short-term and long-term retention data acquisition. The short-term period is taken from read delay of 100ns to 100sec., and 5 times signal averaging is done, refer fig. 4-4.

The long-term retention is monitored by 5 times programming (to provide continuity with the short-term results) and a sequence of read operations with read delay of 56μs., and then starting at 100μs. and then upto 10^5s., refer to fig. 4-5.

For the write state, the device is first erased for 10sec. and then written for 10ms. and the rest of the procedure is the same as for the erased state.

The retention characteristics of the p-channel and n-channel transistor is shown respectively in figs. 4-6 and 4-7.

4.3 Endurance Characteristics

Endurance has been studied on the n-channel transistor. The transistor is cycled with 100μs. write (-10V) and 100μs. erase (10V). The fig. 4-8 illustrates the stressing cycle. After a certain number of cycles retention characteristics are obtained for the both states to identify any effect of cycling on the window or the decay characteristics.

The endurance characteristics of the n-channel transistor is shown in fig. 4-9.

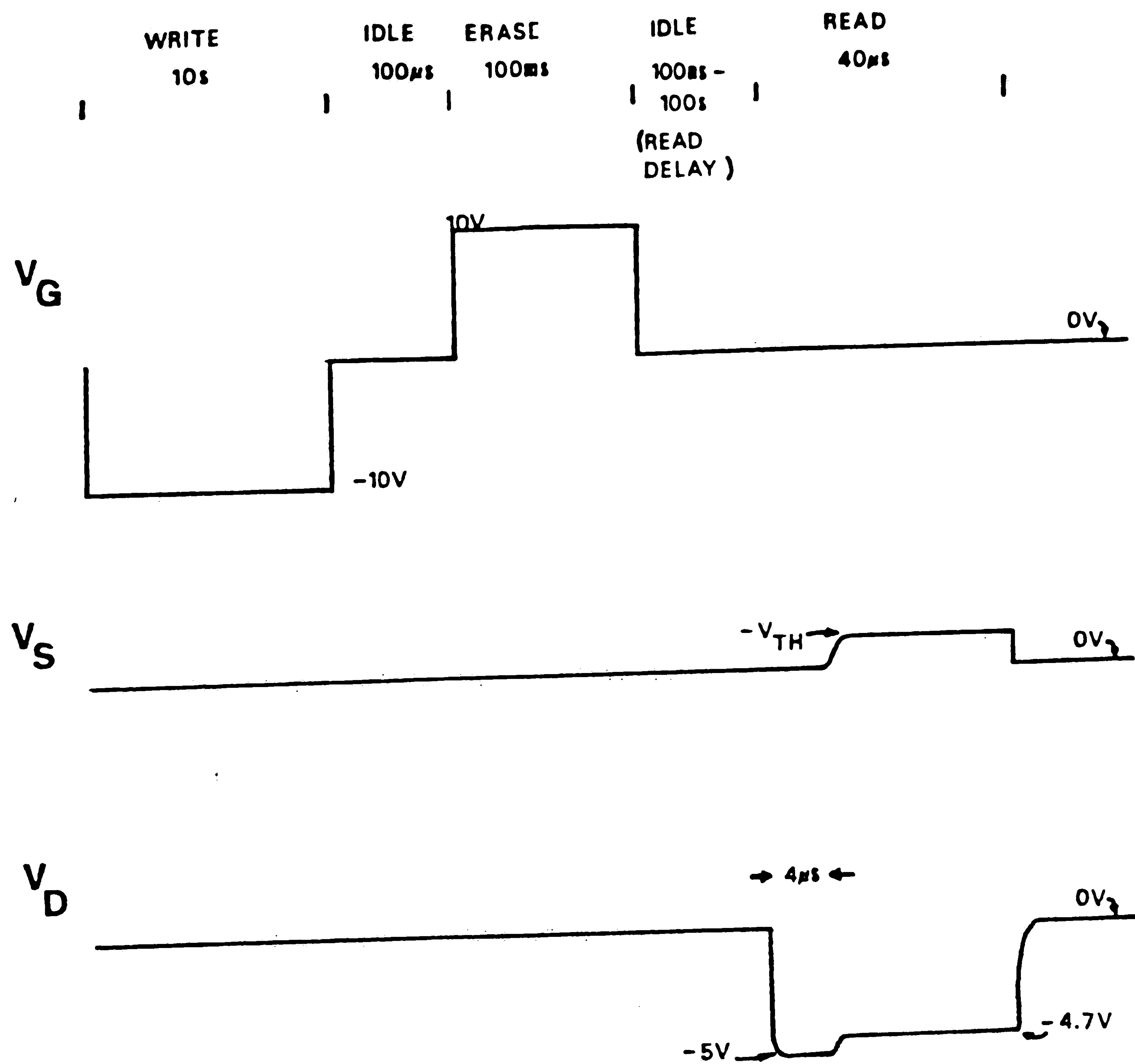


Figure 4-4: Pulse sequence for short term retention measurement

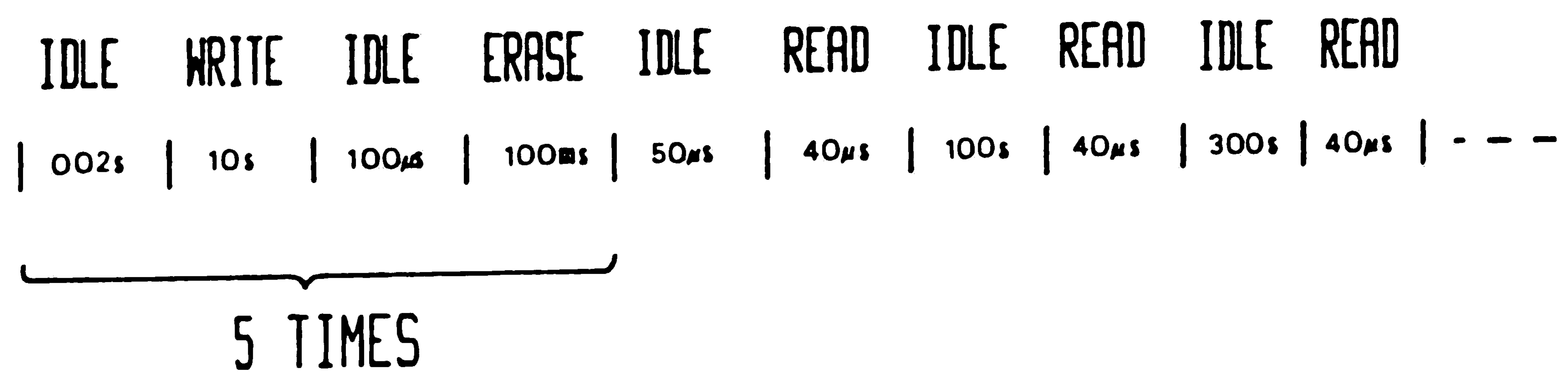


Figure 4-5: Pulse sequence for long term retention measurement

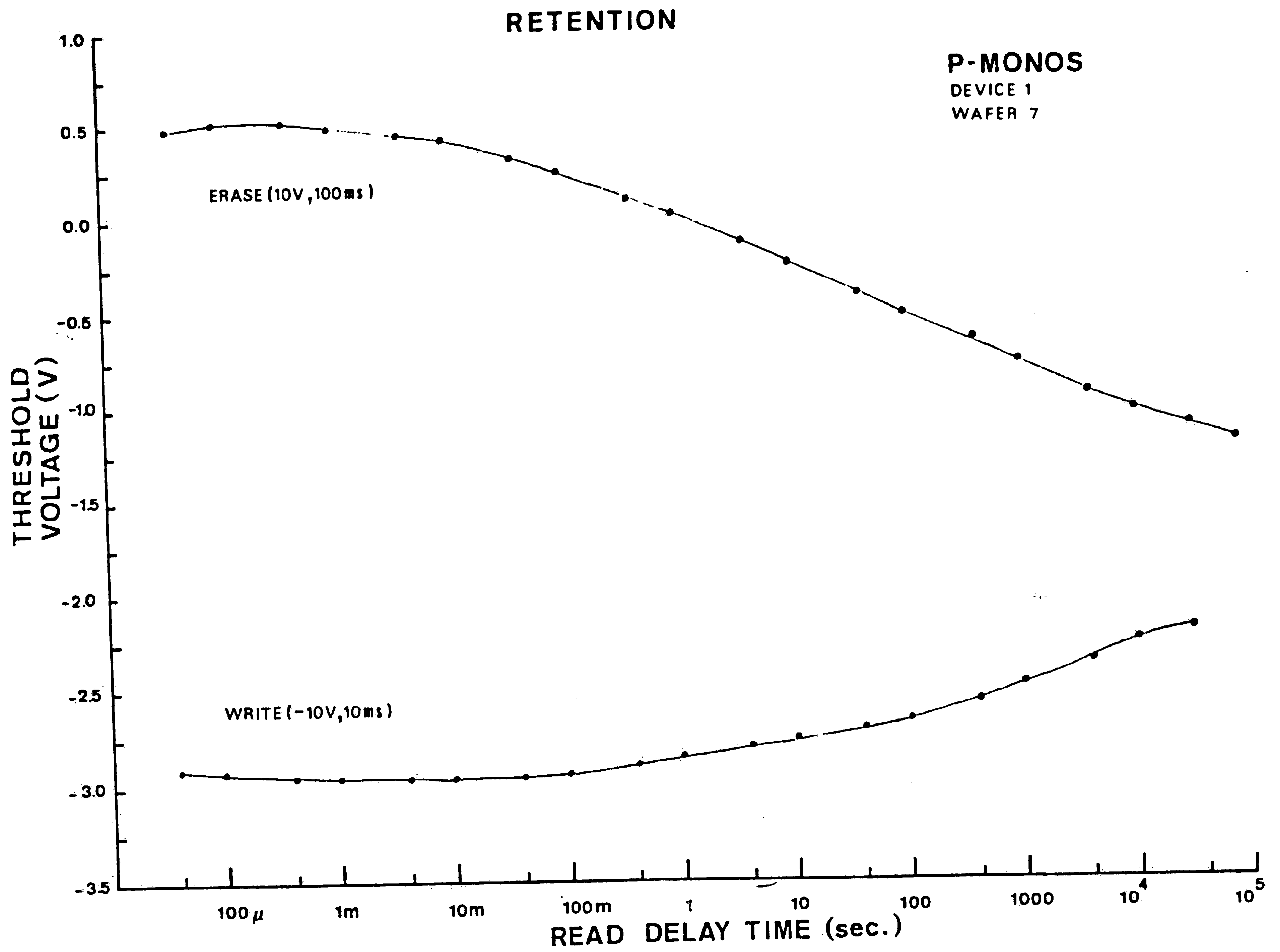


Figure 4-6: Zero-bias Retention plot for a p-channel MONOS transistor with x_{ot}=20A, x_N=85A and x_{oB}=51A

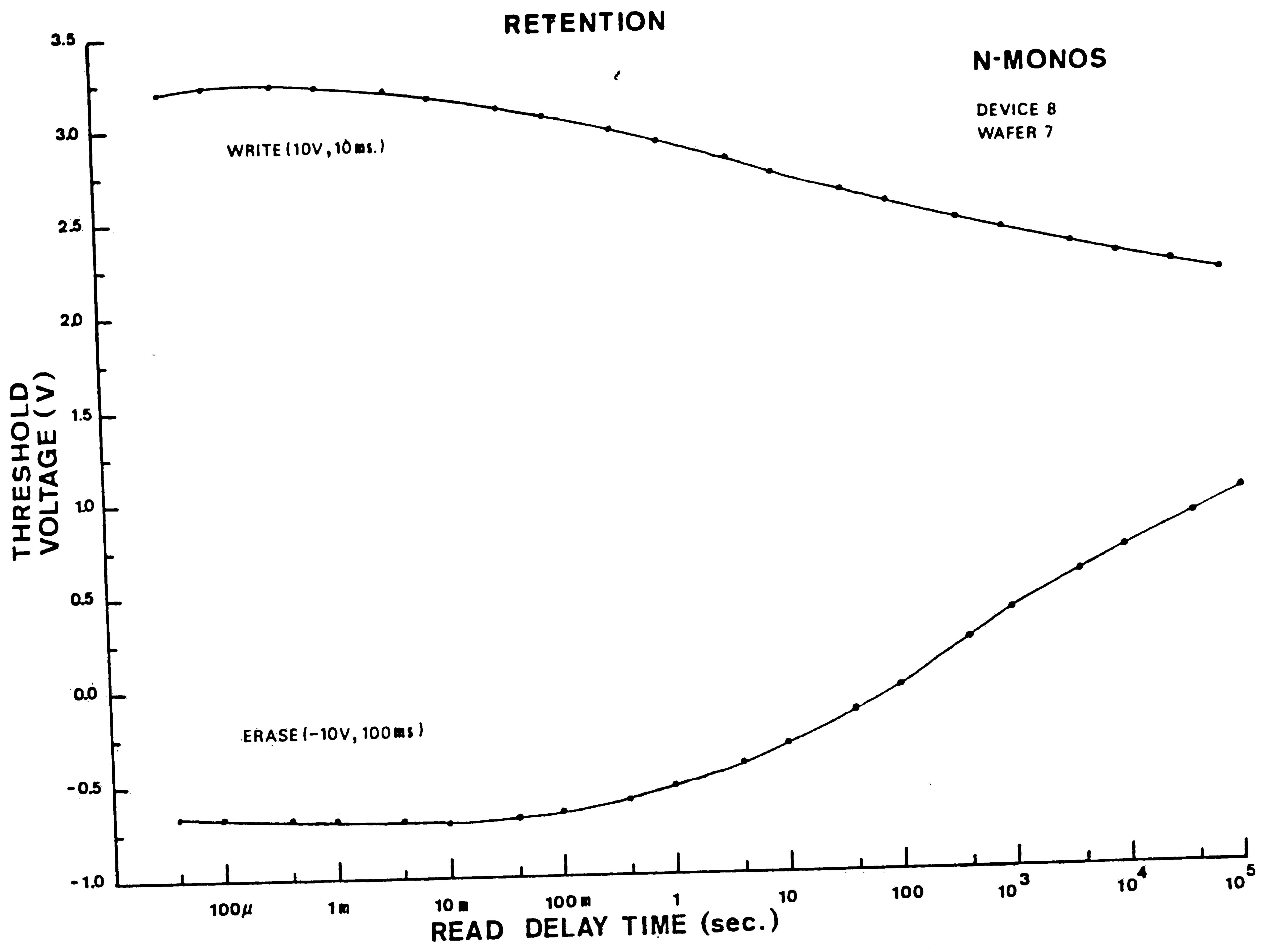


Figure 4-7: Zero-bias Retention plot for a n-channel MONOS transistor with x_{ot}=20A, x_N=85A and x_{oB}=51A

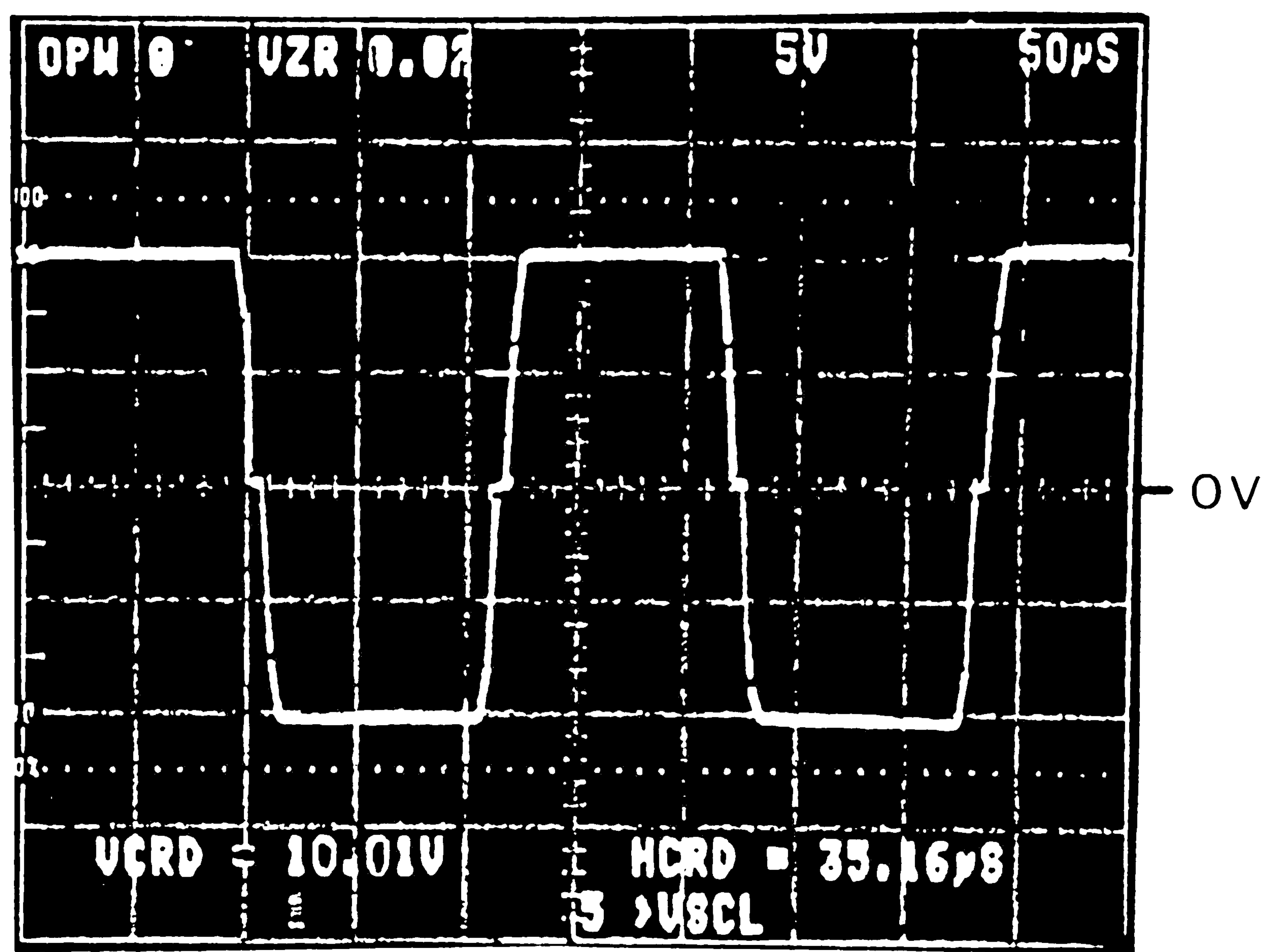


Figure 4-8: Photograph of the pulse sequence on the gate of the transistor with source, substrate and drain grounded for a n-channel MONOS transistor

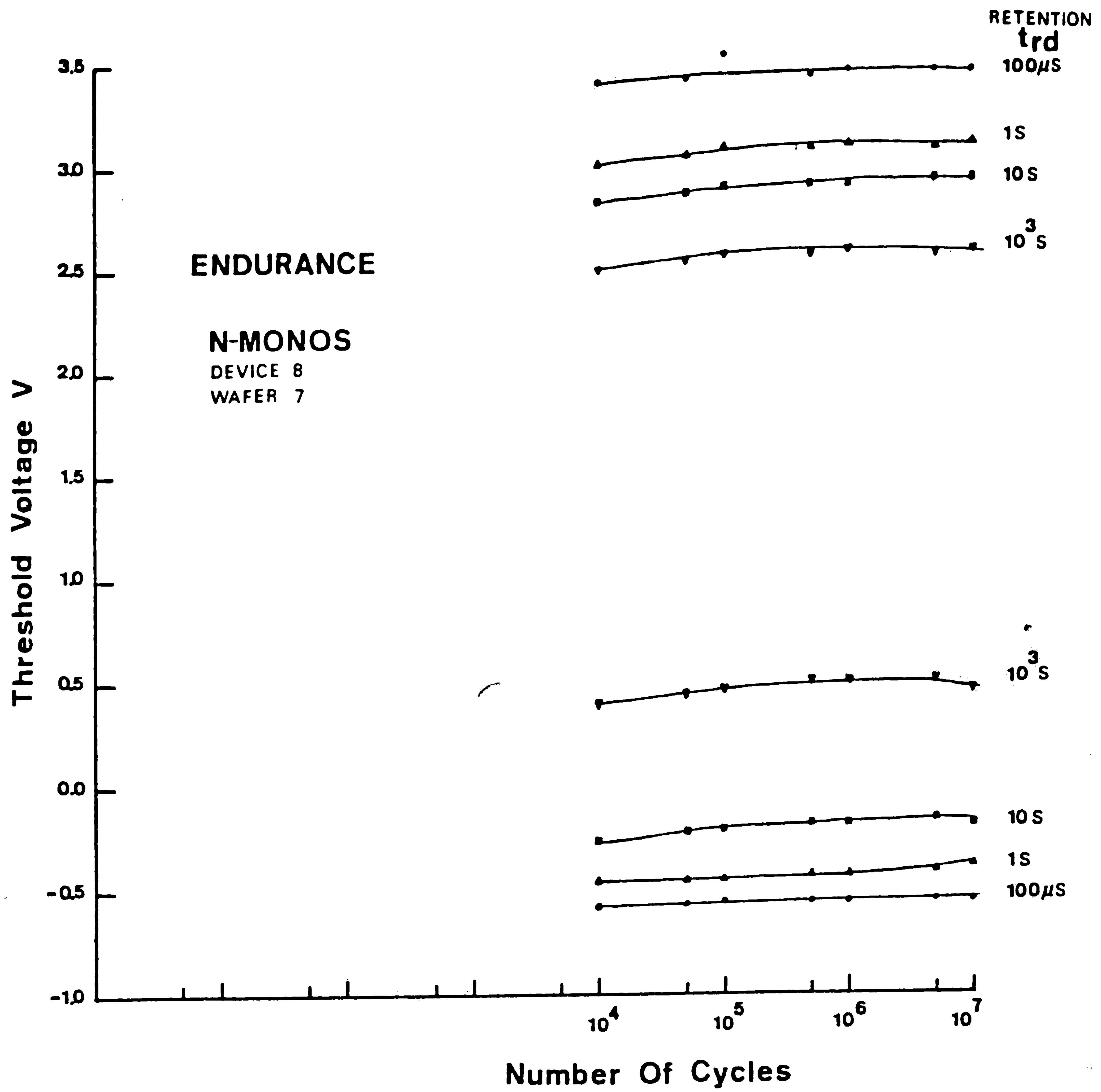


Figure 4-9: Endurance plot for a n-channel MONOS transistor with x_{ot}=20A, x_N=85A and x_{oB}=51A

Chapter 5
Conclusions

5.1 Discussion Of Results

5.1.1 Erase-Write Characteristics

The erase-write characteristics of complementary MONOS transistors are in figs. 4-2 and 4-3. The centre of the programming window for $\pm 10V$ programming is significantly different, $\sim -1.25V$ for the p-channel and $\sim 2.5V$ for the n-channel device. For both the devices the window is nearly equal to 7V, the curves almost superimpose on each other with the erase-write crossover point around 1ms.

The difference in the centre of the window for the two devices can be accounted only partially by the difference in the fermi-levels of the two devices and the fact that the threshold voltage at $10\mu A$ drain current is more positive than the classical threshold voltage for the n-channel device and more negative for the p-channel device.

The fact that the erase characteristics of the p-channel device have the same shape as the write characteristics of the n-channel device and vice-versa, indicates that the injection is independent of the injecting source type. Furthermore it can be concluded that electrons are injected into the nitride for 10V and holes are injected into the nitride for $-10V$ programming. This is in agreement with the findings of Agarwal et.al. [1], using the linear ramp technique.

The erase-write characteristics reported by Yatsuda et.al. [30] on n-channel MNOS and MONOS devices have the same basic trend as in the present work. The erase curve shows saturation but the saturation of the write curve is not there, for the n-MONOS transistor. After comparing MNOS with MONOS transistors Yatsuda concluded that the blocking oxide is a barrier only for electron and not for hole transport in the gate dielectrics.

5.1.2 Retention Characteristics

The zero bias retention plots for p and n-channel devices is in fig. 4-6 and 4-7 respectively. The devices were written for 10ms. for the written state and erased for 100ms. for the erased state retention data. This may be one of the factors responsible for the fact that the dacay of the erased state for both devices was greater than the corresponding written state.

The beginning of decay for electrons (i.e. 10V programming) for both the devices is around 400μs. of read delay, while for holes (i.e. -10V programming) is around 40ms. This indicates a smaller effective barrier for electron back-tunneling as compared to hole back-tunneling into the silicon from the nitride.

The retention characteristics for either state can be divided into three regimes:

1. no decay

2. short term decay

3. slowing down of decay

The latter two regimes were also observed by Topich [26] on MNOS transistors with thicker nitride thickness and zero bias retention measurements. Even though zero bias retention is claimed to account for the worst case [12], the retention of the device is better than predicted by the extrapolation of the short term decay curve. This is in contrast to the massive evidence in the literature with MNOS devices, where the long term decay is more than the short term decay or only single logarithmic decay has been reported.

In a memory array organization, during a read delay the memory transistor is established in a state called an "inhibit state", where the gate is grounded but the source is "floated". The difference in the decay characteristics between zero bias retention and retention with inhibit state read delay can be seen in fig. 5-1 for a p-channel MONOS transistor. The difference is very small but the zero bias curve exhibits slightly higher decay rate.

5.1.3 Endurance Characteristics

The endurance plot for the n-channel MONOS transistor is shown in fig. 4-9. No degradation in retention, under a 5MV/cm average nitride field, was observed for 10^7 W/E cycles. The gate dielectric dc leakage current did not increase. The Si-SiO_2 interface trap density measured by the subthreshold method [refer appendix A for details on this technique] for the uncycled and 5.2×10^6 cycles were found to be 3.8×10^{11}/eV-cm^2 and 5.3×10^{11}/eV-cm^2 respectively.

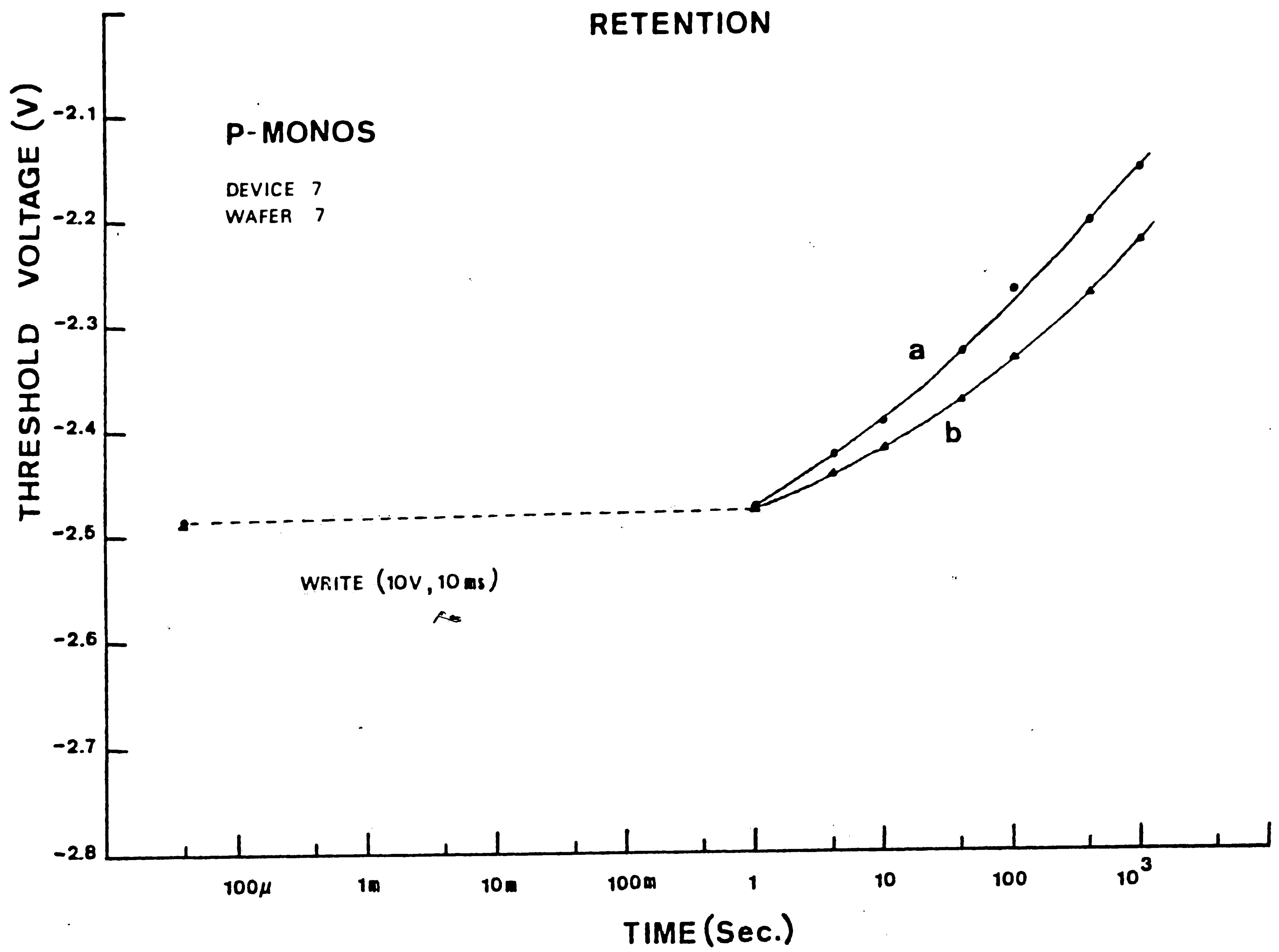


Figure 5-1: Comparison of short term decay characteristics of an n-channel MONOS transistor with (a) source grounded and (b) source floating.

5.2 Recommendations

During the course of this study most of the effort has been towards building a versatile, fast, accurate and computer aided test station. The flexibility of the test station especially in terms of the pattern generator and the W/E & Read circuit allows investigation of retention, erase-write and endurance characteristics of MONOS transistors with different control sequences for the analog switches. This will permit a more extensive comparison of constant voltage retention, constant drain current retention and zero bias retention for the scaled devices. Also the influence of read disturb on retention can be studied. The modular design of the pattern generator renders its use for other experiments requiring many sychronous control signals.

The new technique of extracting the interface trap density at the Si-SiO_2 interface for MONOS transistors can be used to study the correlation of cycling of devices, degradation of retention, and the interface trap density. The simplicity of the technique is attractive from the standpoint that extraction of the density of interface traps has to be done a number of times.

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Appendix A
Subthreshold Conduction

The theory of subthreshold conduction in MOSFETs has been developed by [25], [2], [20], [21], [3]. The expression for the channel current in weak inversion can be written as:

$$I_{DS}=\mu C_D \frac{W}{L}\frac{n}{m}\left(\frac{kT}{q}\right)^2 exp\left(\frac{V_{GS}-V_{TH}}{nV_t}\right)\left(1-exp\left(\frac{mV_{DS}}{nV_t}\right)\right)$$

, where $n=1+\frac{C_{it}+C_D}{C_{ox}}$, $m=1+\frac{C_D}{C_{ox}}$ and $V_t=\frac{kT}{q}$, also μ is the channel mobility in weak inversion, C_D is the depletion capacitance, W and L are the width and length of the channel, C_{it} is the Si-SiO_2 interface trap density under weak inversion conditions.

Information about the interface trap density around weak inversion condition, i.e., mid gap density of states can be extracted from the subthreshold conduction measurements of the transistor. Overstraeten et.al. [21] emphasizing that surface potential fluctuations render the I_D-V_G characteristics in the subthreshold regime useless in terms of interface trap density extraction and they presented that the I_D-V_D characteristics together with the calculated depletion capacitance can be used for interface trap density extraction and compared values obtained from conductance measurements.

Using the above expression for the channel current a method utilizing the capabilities of the HP4145 Semiconductor Parameter Analyzer has been devised to obtain the interface trap density at the Si-SiO_2 interface for the MONOS memory transistors. The method is attractive from the point of view that

conventional C-V measurements involve injection into the nitride and cause distortion and shifts in the C-V plots (particularly for the scaled down devices). In the case of the subthreshold conduction all information can be extracted with gate bias variation of a volt or two and drain bias of half a volt. Secondly, the interface trap density for thin oxide structures are high enough to be insensitive to the effects of surface potential fluctuations [20]. Over the weak inversion range the density value varied from 8.9×10^{11} /eV-cm^2 to 9.2×10^{11} /eV-cm^2 for the p-channel transistor (see example at the end of this appendix).

Experimentally the channel current must be monitored at the source (with source and substrate grounded and drain voltage applied). This is because as the drain bias increases the drain substrate depletion layer generation currents manifest; it's more dominant in the I_D-V_D characteristics and the saturation of the characteristics as predicted by theory is not obtained. Fig. A-1 illustrates the effect with both the source and drain currents on the same plot.

The I_S-V_G characteristics for a p-channel MONOS transistor for small drain voltage is shown in fig. A-2. The weak inversion can be identified by the exponential dependence of I_S on V_G. The slope of this $\log I_S$-V_G characteristics is $\gamma_1 = (nV_t \ln 10)^{-1}$

The I_S-V_D characteristics for the same p-channel transistor biased at a gate voltage in the weak inversion regime is shown in fig. A-3. The saturated value of the current β can be extracted, such that the expression for the current can be written as:

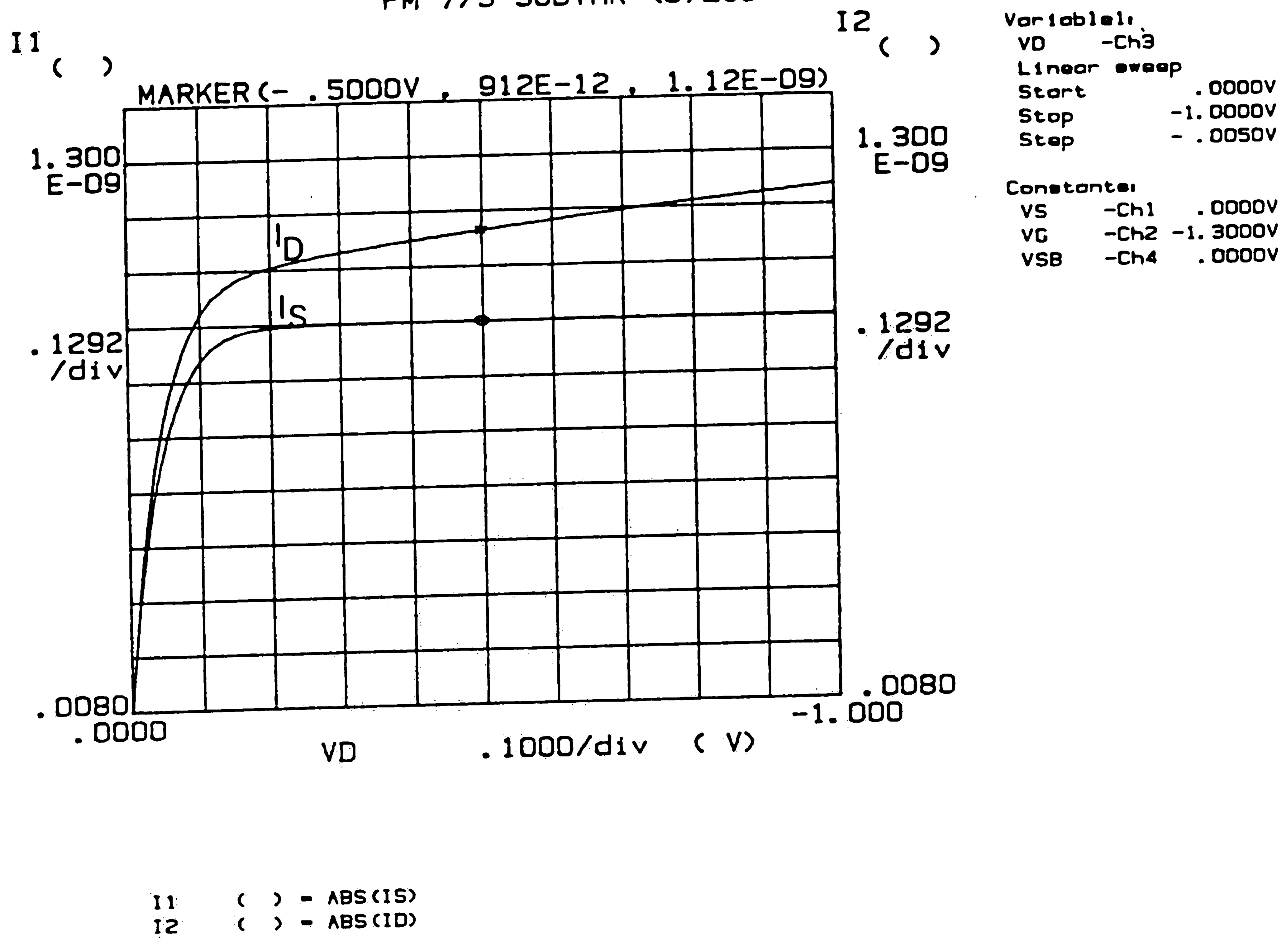
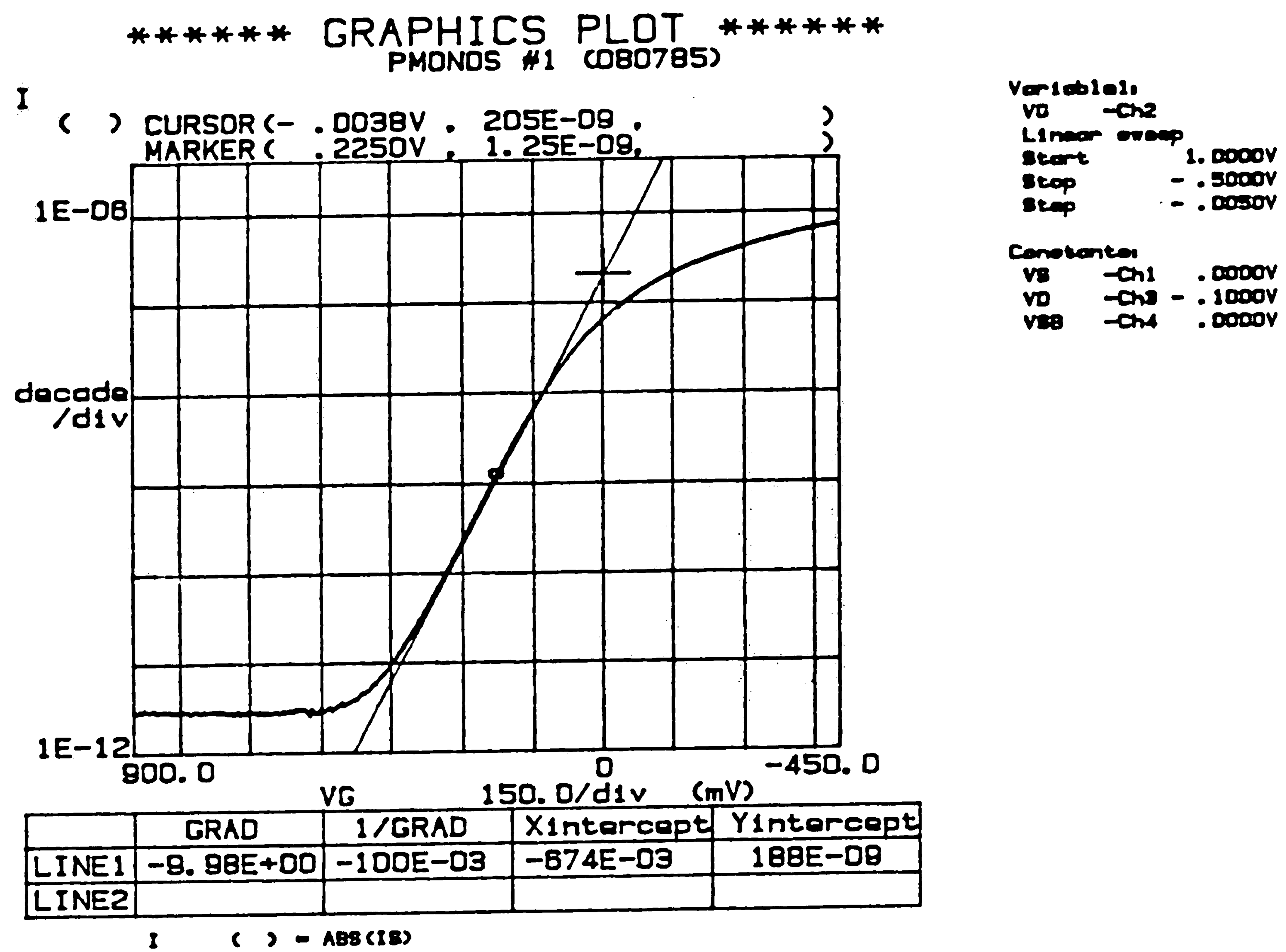


Figure A-1: Difference between source and drain currents in weak inversion as a function of drain voltage



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-9.98E+00	-100E-03	-674E-03	188E-09
LINE2				

Figure A-2: I_S-V_G characteristics of a p-channel MONOS transistor in the subthreshold conduction regime

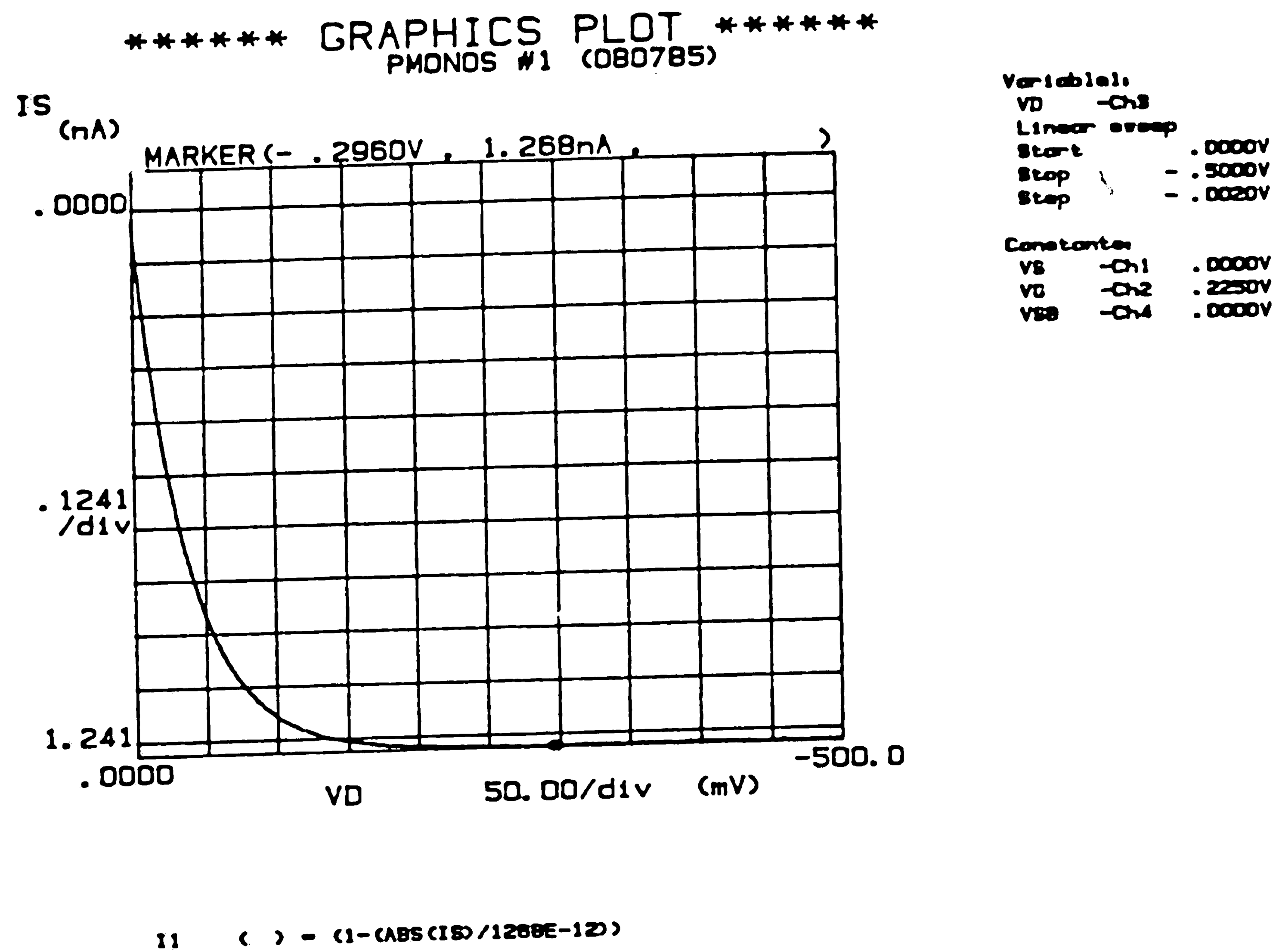


Figure A-3: I_S-V_D characteristics for the p-channel transistor (same as in fig. A-2) biased in the subthreshold conduction regime with V_G=0.225V

$$I_S = \beta\left[1 - exp\left(\frac{mV_{DS}}{nV_t}\right)\right]$$

Define $I_1 = (1 - \frac{I_S}{\beta}) = exp(\frac{mV_{DS}}{nV_t})$. The slope of the $log I_1$-V_{DS} characteristics is a straight-line with slope $\gamma_2 = (\frac{nV_t ln10}{m})^{-1}$.

From γ_1 the parameter n can be calculated. From γ_2 and the value of n, the parameter m can be calculated. The interface state density in the weak inversion region is given by:

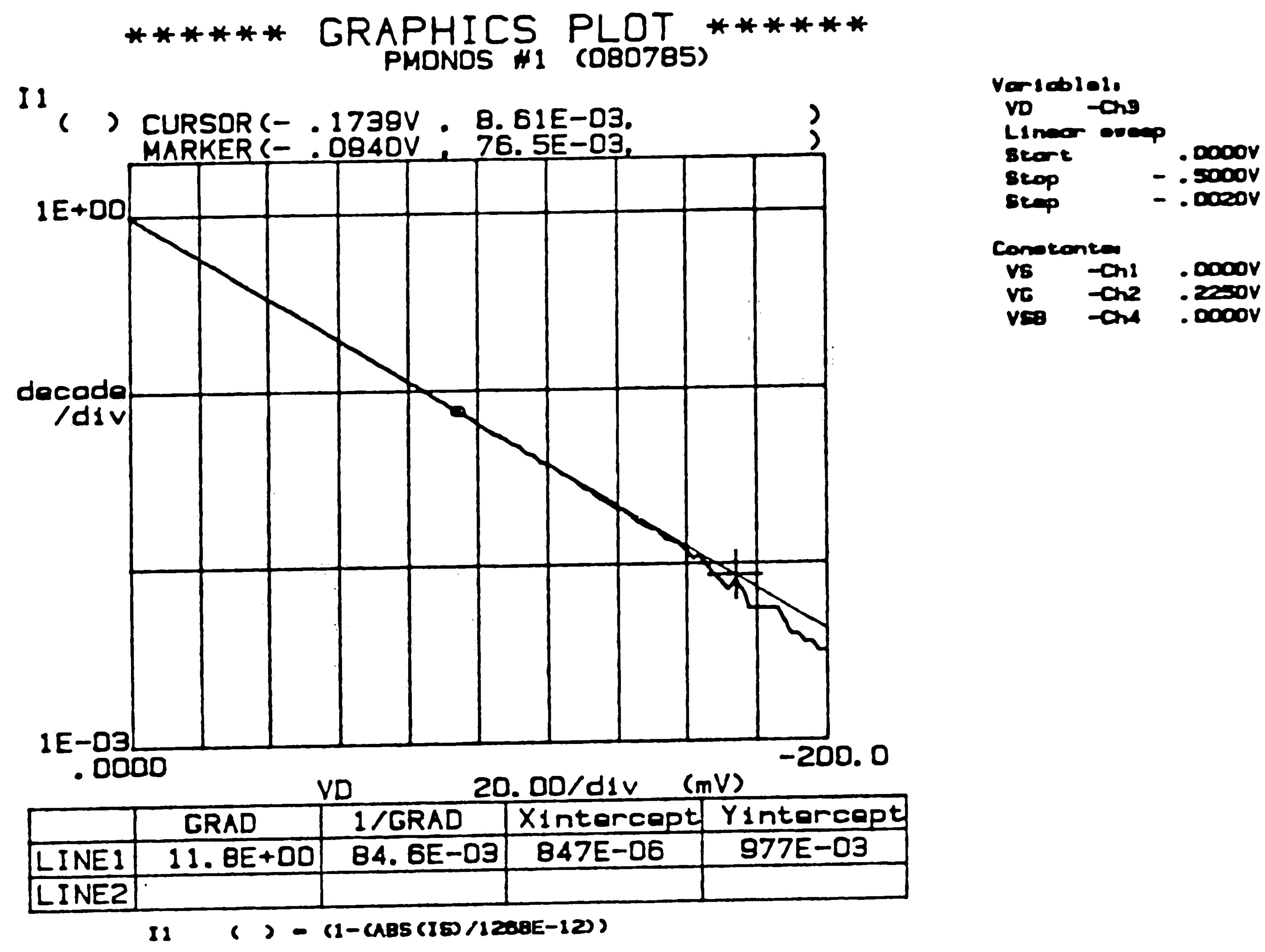
$$\overline{D}_{it} = \frac{C_{it}}{q} = \frac{(n-m)C_{eff}}{q}$$

, where C_{eff} is the capacitance of the dielectric layers under the gate.

Example:

In this example the extraction of interface trap density at the Si-SiO_2 interface will be illustrated for the p-channel MONOS transistor characterised by retention and erase-write experiments in chapter 4. From the fig. A-2 the subtreshold conduction regime slope $\gamma_1 = (100mV)^{-1}$. This leads to a value for n=1.683. From fig. A-3 the saturated value of the source current for gate bias of 0.225V is 1.268nA. The corresponding $log I_1$-V_{DS} plot is shown in fig. A-4, with slope γ_2 of $(84.6mV)^{-1}$. This yields a value for $\frac{n}{m}$=1.424, leading to a value of **m**=1.182. From quasi-static measurements on the transistor the effective capacitance of the gate is 0.283μF/cm^2. This leads to the interface trap density, for the gate bias of 0.225V, equal to $\mathbf{8.85\times10^{11}/eV\text{-}cm^2}$.

By picking up another gate bias within the subthreshold conduction regime



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.8E+00	84.6E-03	847E-06	977E-03
LINE2				

Figure A-4: Plot of I_1-V_D for gate bias of 0.255V.

the density of interface traps has been evaluated. Fig. A-5 is the $log I_S$-V_G characteristics with slope $\gamma_1 = (101mV)^{-1}$, leading to **n**=1.699. With gate bias of 0.4V the $log I_S$-V_D shows saturation at 24.1pA (see fig. A-6). The $log I_1$-V_D plot in fig. A-7 gives a value for $\frac{n}{m}$=1.441. The value for **m**=1.179. The interface trap density comes out to be $\mathbf{9.18 \times 10^{11}/eV\text{-}cm^2}$. It's an expected result because subthreshold conduction corresponds to scanning the middle of the Si band gap, where the density of interface traps is relatively constant.

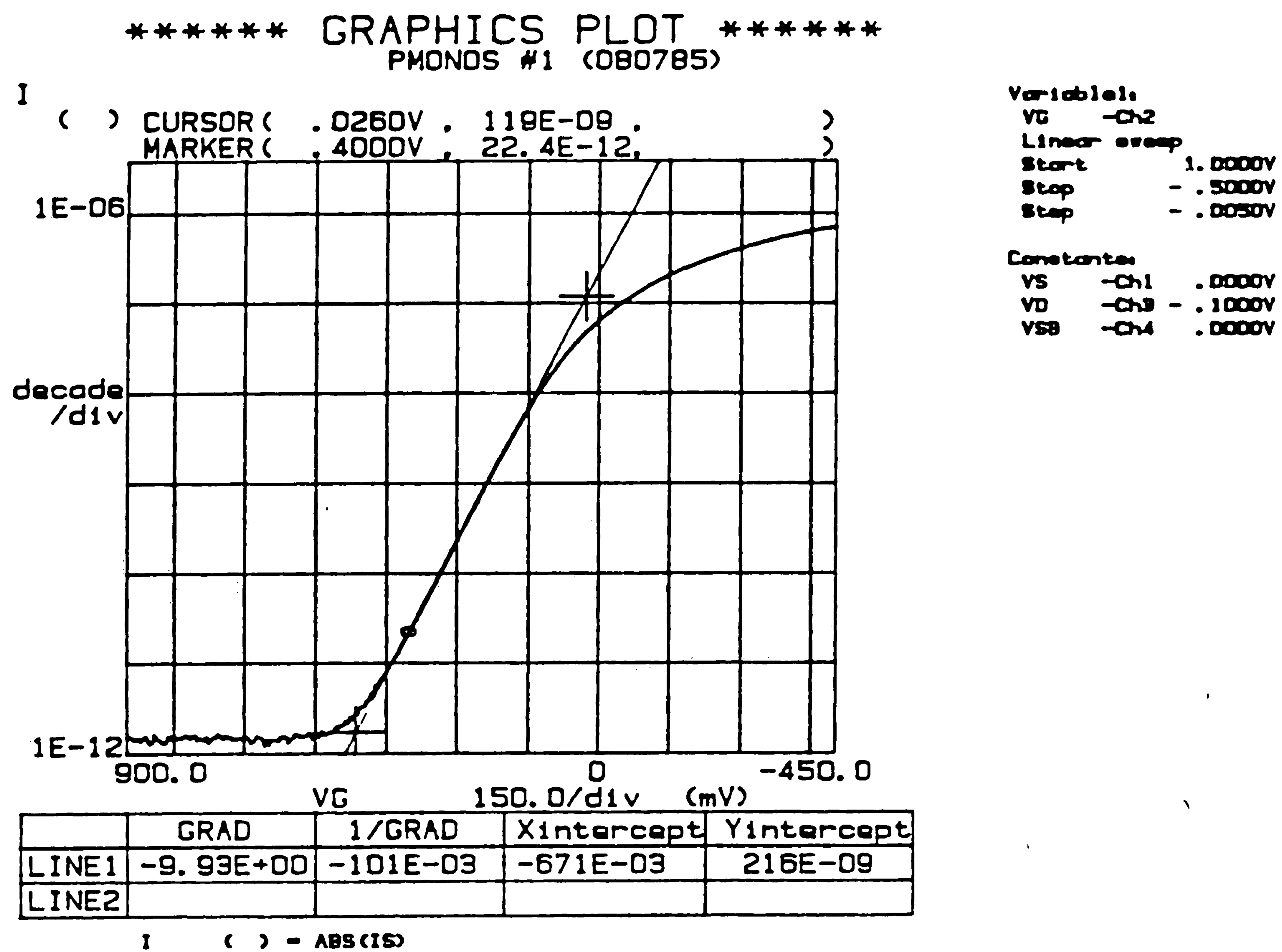


Figure A-5: I_S-V_G characteristics of the PMONOS transistor, same as in fig. A-2

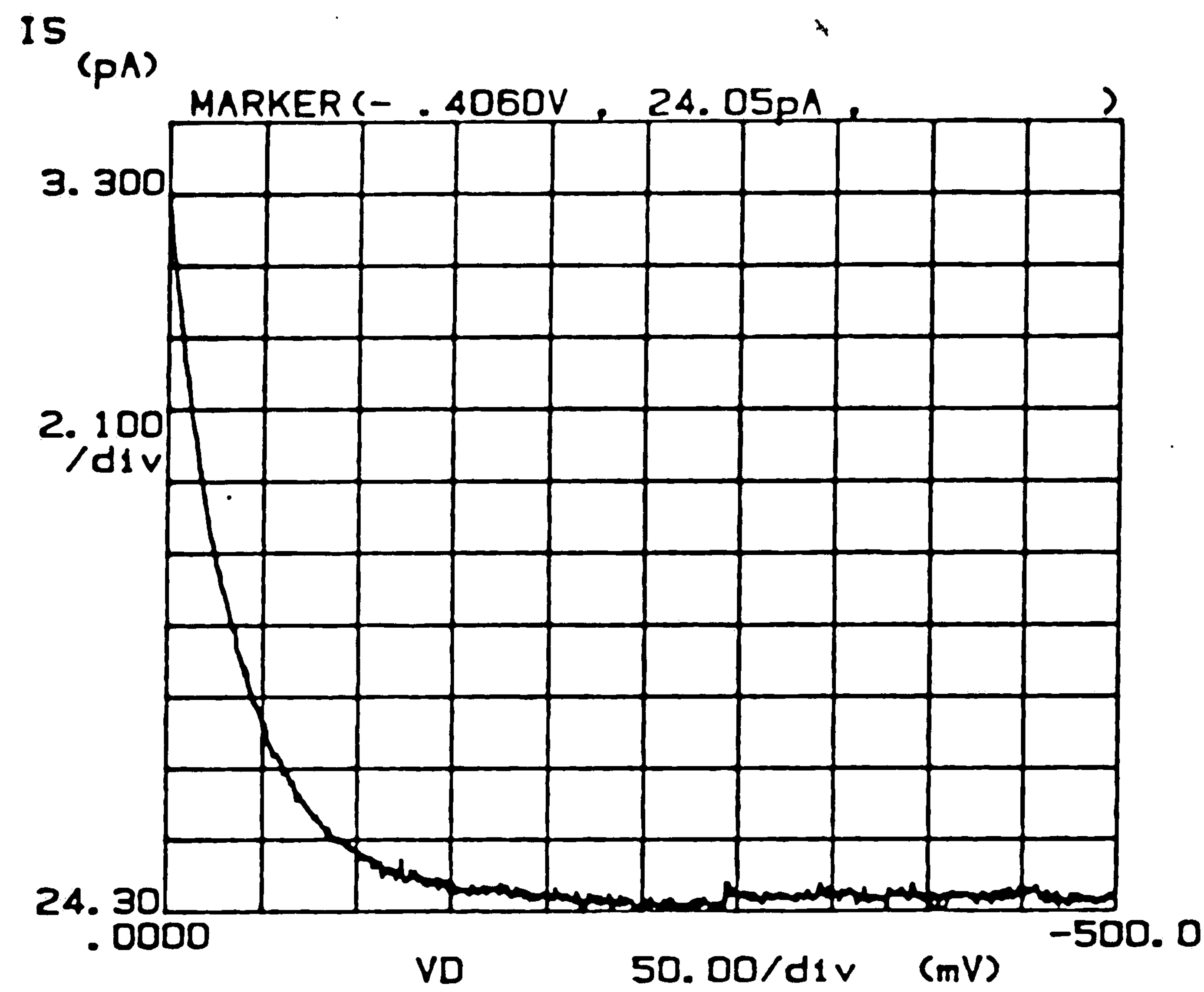


Figure A-6: I_S-V_D characteristics for V_G=0.400V.

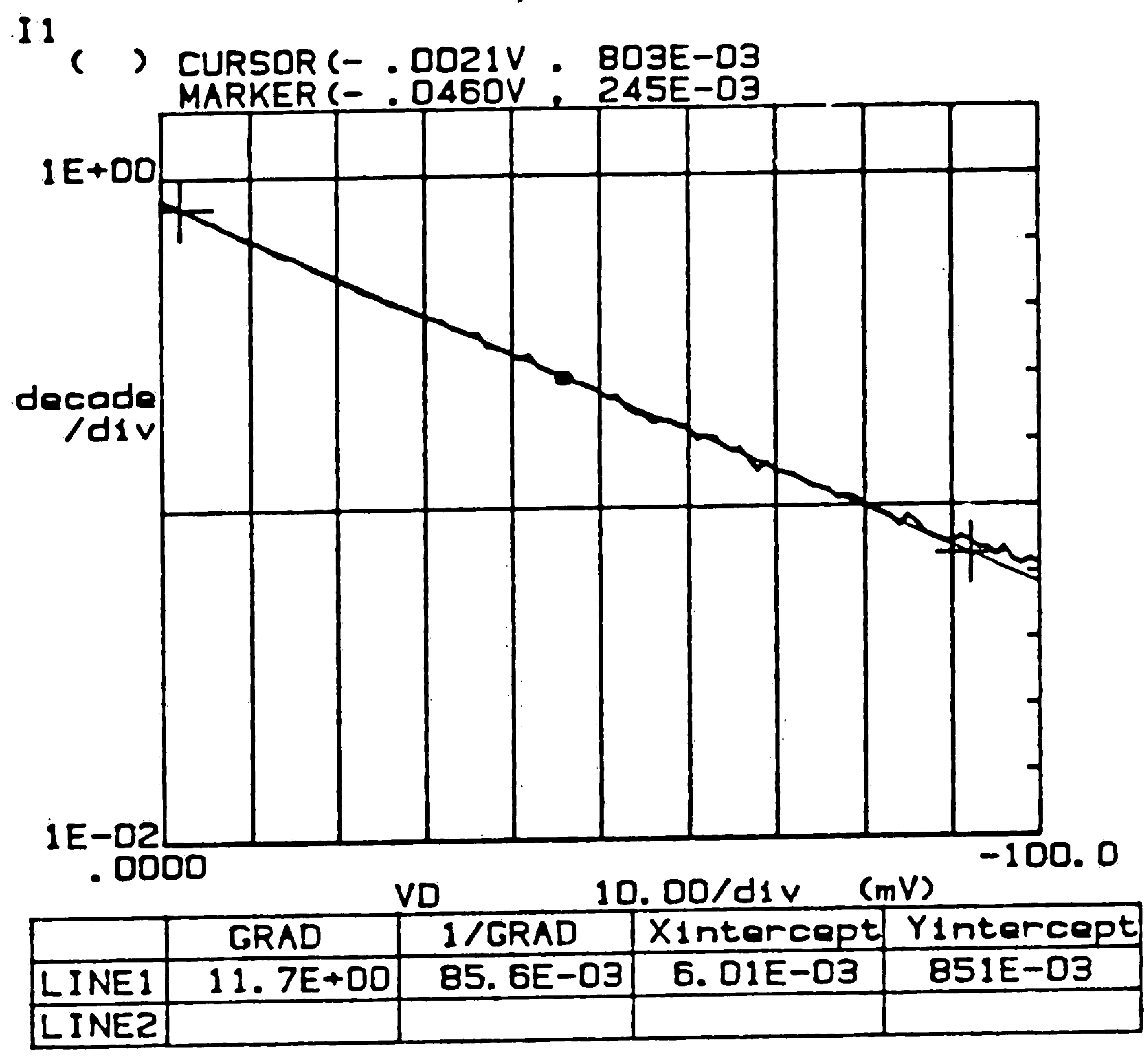


Figure A-7: I_1-V_G plot for V_G=0.400V.

Appendix B
Pattern Generator

B.1 Generator Board

The components on the circuit schematic of the pattern generator board in fig. 3-10, chapter 3 are listed below:

U1-U12,U46,U47	74LS190;SYNCHRONOUS UP/DOWN BCD COUNTER
U13-U24,U48,U49	2114-20;1K×4 200NS MOS STATIC RAM
U25-U36,U50,U51	74125; BUFFER GATES WITH 3 STATE OUTPUTS
U37,U52	74116; DUAL 4 BIT LATCHES
U38,U39,U45	7408; QUAD 2 INPUT AND GATES
U40	74LS138;3 TO 8 LINE DECODER
U41	74LS221;DUAL MONOSTABLE MULTIVIBRATOR
U42	74S124; DUAL VCO
U43	7476; DUAL J-K FLIP-FLOP
U44	74126; BUFFER GATE WITH 3 STATE OUTPUTS

Q1	2N3904;	NPN TRANSISITOR
D1		RED LED
SW1,SW2		PUSH BUTTON SWITCH
SW3		SPDT SWITCH
B1-B7		ROCKWELL VIA PORT B
R1-R10,R13,		
R17,R19,R21	5.6KΩ	
R11	200Ω;	METAL FILM RESISTOR
R12	300Ω;	METAL FILM RESISTOR
R14,R15	100Ω	
R16	4.7KΩ	
R20	1KΩ	
R22	12KΩ	
C1	0.02MF	
C2	0.47MF	
REMOTE		BNC INPUTS FOR CONTROLLING THE START AND RESET ;PULSED LOW.

The organization of the components on the generator board is shown in fig. B-1. The components are wire-wrapped on the 8800V series microprocessor board to obtain efficient packing. The board requires a single 5V power supply and draws approximately 2 amperes of current. The power pin to each IC chip is decoupled using 0.01μf ceramic capacitors.

FOR 8800V SERIES MICROPROCESSOR BOARD

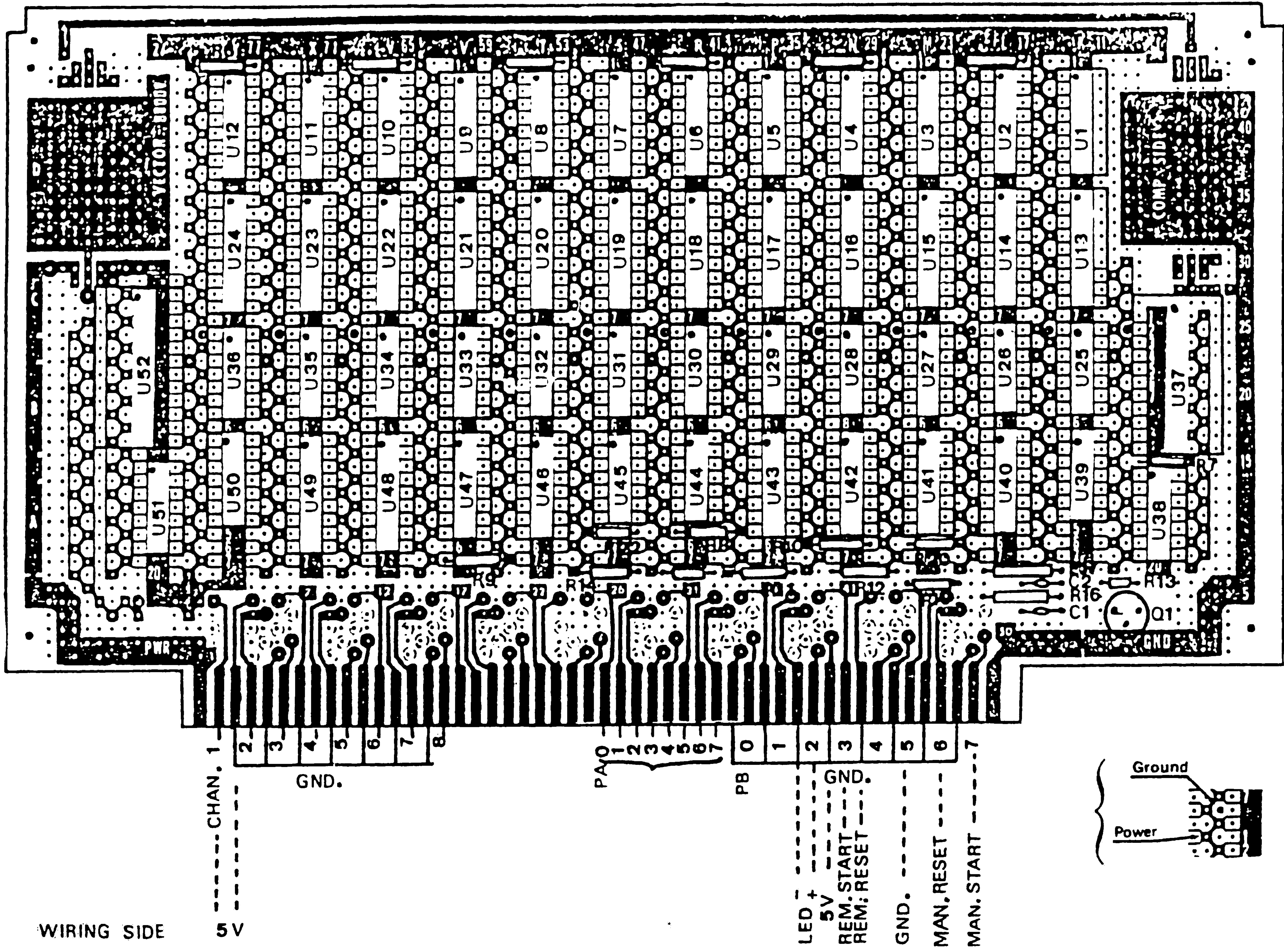


Figure B-1: Component layout on the pattern generator board

B.2 Rockwell AIM 65 Interface and Software

The Rockwell AIM 65 hardware system organization block diagram is shown in fig. B-2. The video terminal is attached to the teletype interface, programs are stored/read from audio casette interface. The PROM with the main driver object code starts at memory location $C000. The 8 line parallel ports A and B of the user dedicated R6522 VIA are programmed as outputs and are interfaced directly to the generator board.

The software was developed on the same system, using the 6502 assembly language. The program listing is included at the end of this appendix.

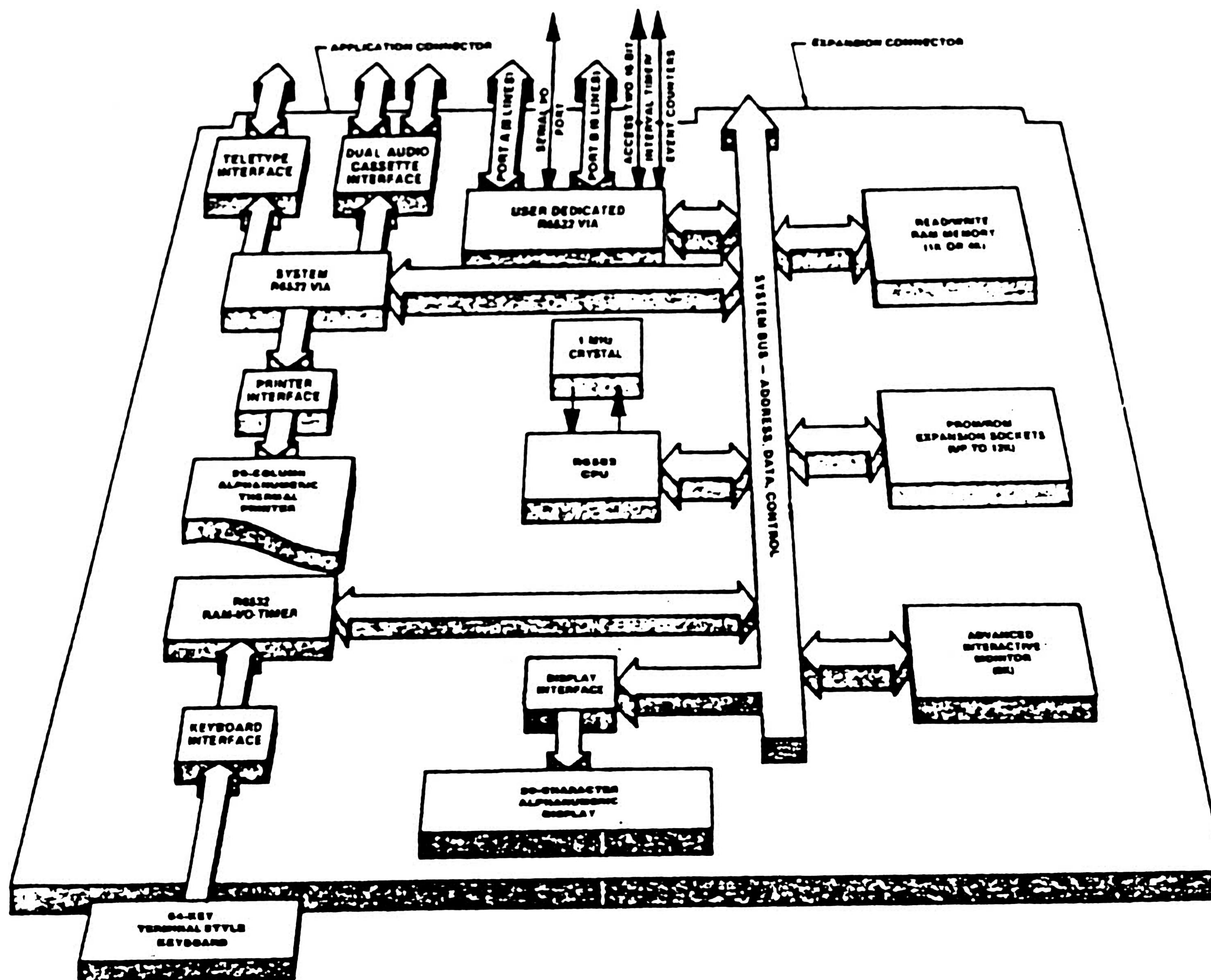


Figure B-2: Hardware system organization of the Rockwell AIM 65

```
-----------------------------------------------------
THIS IS THE DRIVER PROGRAM FOR THE PATTERN GENERATOR
-----------------------------------------------------
.PAGE 'MAIN PROGRAM'
;PROGRAM CONSTANTS
.SKI
CRLF=$E9F0
HEX=$EA7D
LL=$E8FE
OUTALL=$E9BC
REDOUT=$E973
NUMA=$EA46
BLANK2=$E838
PHXY=$EB9E
PLXY=$EBAC
UDDRA=$A003
UDDRB=$A002
UDRA=$A00F
UDRB=$A000
.SKI
;PAGE 0 VARIABLES
*=$00
MAINCR *=*+1
CNRFLG *=*+1
ERRNUM *=*+1
COUNTR *=*+1
CONTR1 *=*+1
CONTR2 *=*+1
CONTR3 *=*+1
CONTR5 *=*+1
CHRPTR *=*+1
CHRBUF *=*+10
MSGPTR *=*+2
DUMPTR *=*+1
DUMBUF *=*+10
ERRFLG *=*+1
ADDPTR *=*+2
LODPTR *=*+2
.SKI
;MESSAGES
;-------------------------------------
*=$CE00
MSG0 .BYT 'PATTERN =;'
MSG1 .BYT 'DELAY =;'
MSG2 .BYT 'FORMAT ERROR #;'
MSG3 .BYT 'N=NEXT OR Q=QUIT',$0D,$0A,'+;'
MSG4 .BYT 'G=CONTINUE '
.BYT 'OR Q=QUIT',$0D,$0A,'^;'
MSG5 .BYT 'UTILITIES: '
.BYT 'E=EDITOR , '
.BYT 'L=LIST , '
.BYT 'T=TRANSFER;'
MSG6 .BYT 'WELCOME TO THE'
.BYT ' DRIVER ROUTINE;'
MSG7 .BYT 'T=TYPE ,'
.BYT 'D=DELETE LAST '
.BYT 'LINE ,'
.BYT 'K=ERASE ALL ,'
```

```
.BYT 'Q=QUIT;'
MSG8 .BYT $OD,$OA,'^;'
MSG9 .BYT 'NO PATTERN'
.BYT ' LEFT;'
MSG10 .BYT '     PATTERN'
.BYT '     DELAY;'
MSG11 .BYT 'NUMBER OF '
.BYT 'SEQUENCES=;'
MSG12 .BYT 'A=APPEND ,'
.BYT 'M=MODIFY ,'
.BYT 'Q=QUIT',$OD,$OA,'%;'
MSG13 .BYT 'BUFFER FULL'
.BYT $OD,$OA,';'
MSG14 .BYT 'R=REPLACE ,'
.BYT 'D=DELETE ,'
.BYT 'I=INSERT ,'
.BYT 'Q=QUIT;'
MSG15 .BYT $OD,$OA,'$;'
MSG16 .BYT 'LINE NUMBER=;'
.SKIP
;MESSAGE ADDRESSES
;-----------------------------------
MSGADD .WOR MSGO,MSG1,MSG2
.WOR MSG3,MSG4,MSG5
.WOR MSG6,MSG7,MSG8
.WOR MSG9,MSG10,MSG11
.WOR MSG12,MSG13,MSG14
.WOR MSG15,MSG16
.SKIP
;MAIN PROGRAM DRIVER
*=$COOO
JSR LL
ALPHA LDA #$OB
JSR PROMPT
ALP1 JSR REDOUT
CMP #$OD
BEQ ALP2
JSR HEX
BCS ALP3
TAY
JSR REDOUT
JSR HEX
BCS ALP3
STA CONTR5
TYA
LDY CONTR5
JSR BINDEC
PHA
JSR CRLF
PLA
JMP ALP4
ALP3 LDA #$41
STA ERRNUM
JSR CRLF
JSR ERROR
JMP ALPHA
ALP2 JSR CRLF
LDA #OO
```

```
ALP4 STA MAINCR
LDA #$06
JSR PROMPT
JSR CRLF
FLOOP   LDA #05
JSR PROMPT
JSR CRLF
WAITER  LDA #'*'
JSR OUTALL
JSR REDOUT
PHA
JSR CRLF
PLA
CMP #'E'
BNE A1PONT
JSR EDITOR
JMP WAITER
A1PONT  CMP #'L'
BNE A2PONT
JSR LIST
JMP WAITER
A2PONT  CMP #'T'
BNE A3PONT
JSR TRXFER
JMP WAITER
A3PONT  JMP FLOOP
LDA #00
STA ADDPTR
STA LODPTR
LDA #$20
STA ADDPTR+1
LDA #$28
STA LODPTR+1
;SUBROUTINE PROMPT
;-----------------------------------------
PROMPT;PRINT MESSAGES
ASL A
TAX
LDA MSGADD,X
STA MSGPTR
INX
LDA MSGADD,X
STA MSGPTR+1
LDY #0
PLOOP   LDA (MSGPTR),Y
CMP #';'
BEQ PRTURN
JSR OUTALL
INY
JMP PLOOP
PRTURN  RTS
;-----------------------------
;UTILITY EDITOR,ENTER AND MODIFY PATTERN AND DELAY
;---------------------------------
EDITOR
LDA #00
STA COUNTR
STA ADDPTR
```

```
STA LODPTR
LDA #$20
STA ADDPTR+1
LDA #$28
STA LODPTR+1
DELTA LDA #$0C
JSR PROMPT
JSR REDOUT
PHA
JSR CRLF
PLA
CMP #'A'
BNE DELTA1
JMP APPEND
DELTA1 CMP #'M'
BNE DELTA2
JMP BETA
DELTA2 CMP #'Q'
BNE EDITOR
JSR CRLF
RTS
APPEND LDA COUNTR
CMP MAINCR
BEQ DELTA3
JSR SEQINC
INC COUNTR
JMP APPEND
DELTA3 JSR MLOOP
LDA #00
CMP DUMPTR
BNE EDITOR
JSR QLOOP
INC COUNTR
LDA COUNTR
CMP #$63
BNE DELTA4
LDA #$0D
JSR PROMPT
JMP EDITOR
DELTA4 INC MAINCR
JMP DELTA3
BETA LDA #00
STA COUNTR
STA ADDPTR
STA LODPTR
LDA #$20
STA ADDPTR+1
LDA #$28
STA LODPTR+1
LDA #$0E
JSR PROMPT
BETA1 LDA #$0F
JSR PROMPT
JSR REDOUT
PHA
JSR CRLF
PLA
CMP #'R'
```

```
BNE BETA2
JMP REPLAC
BETA2 CMP #'D'
BNE BETA3
JMP DILETE
BETA3 CMP #'I'
BNE BETA4
JMP INSERT
BETA4 CMP #'Q'
BNE BETA5
JMP DELTA
BETA5 LDA #$42
STA ERRNUM
JSR ERROR
JMP BETA
;--------------------------------
;SUBROUTINE BETA6,FOR READING
;LINE NUMBER
BETA6 LDA #$10
JSR PROMPT
BETA7 JSR REDOUT
JSR HEX
BCS BETA8
TAY
JSR REDOUT
JSR HEX
BCS BETA8
STA CONTR5
TYA
LDY CONTR5
JSR BINDEC
PHA
JSR CRLF
PLA
JMP BETA9
BETA8 LDA #$42
STA ERRNUM
JSR CRLF
JSR ERROR
JMP BETA6
BETA9 PHA
JSR CRLF
PLA
RTS
;------------------------
REPLAC JSR BETA6
CMP MAINCR
BMI BETA20
BEQ BETA20
JMP BETA10
BETA20 TAY
DEY
BEQ BETJ
BETA11 JSR SEQINC
DEY
BNE BETA11
BETJ JSR MLOOP
LDA #00
```

```
CMP DUMPTR
BNE BETI
JSR QLOOP
BETI JMP BETA
BETA10 LDA #$43
STA ERRNUM
JSR ERROR
JMP BETA
DILETE JSR BETA6
CMP MAINCR
BMI BETA21
BEQ BETK
JMP BETA10
BETA21 TAY
STA COUNTR
DEY
BEQ D1LETE
BETA12 JSR SEQINC
DEY
BNE BETA12
D1LETE
LDX COUNTR
BETA13 JSR SEQREC
JSR SEQINC
INX
CPX MAINCR
BCC BETA13
BETK DEC MAINCR
JMP BETA
INSERT LDA #$62
CMP MAINCR
BPL BETA23
LDA #$0D
JSR PROMPT
JMP BETA
BETA23 JSR BETA6
CMP MAINCR
BMI BETA22
BEQ BETA22
JMP BETA10
BETA22 STA COUNTR
LDY MAINCR
DEY
BEQ BETL
BETA14 JSR SEQINC
DEY
BNE BETA14
BETL LDX MAINCR
BETA15 JSR SEQADV
JSR SEQDEC
DEX
CPX COUNTR
BCS BETA15
INC MAINCR
JSR SEQINC
JSR MLOOP
LDA #00
CMP DUMPTR
```

```
BEQ BETA30
LDA COUNTR
JMP D1LETE
BETA30 JSR QLOOP
JMP BETA
;---------------------
;SUBROUTINE MLOOP, FOR PATTERN
;ACQUISITION
MLOOP   LDA #00
STA DUMPTR
JSR PROMPT
LDX #00
NLOOP   JSR REDOUT
CMP #$0D
BEQ NRTURN
CMP #'Q'
BNE CONT1
INC DUMPTR
JSR CRLF
RTS
CONT1 STA CHRBUF,X
INX
JMP NLOOP
NRTURN PHA
JSR CRLF
PLA
CPX #00
BEQ APOINT
CPX #08
BEQ BPOINT
LDA #$31
STA ERRNUM
JSR ERROR
JMP MLOOP
BPOINT  LDX #07
EPOINT  LDA CHRBUF,X
JSR ASCHEK
CPOINT  LDA ERRFLG
CMP #00
BEQ DPOINT
CZPONT
LDA #$32
STA ERRNUM
JSR ERROR
JMP MLOOP
DPOINT  LDA DUMBUF,X
CMP #02
BCS CZPONT
DEX
BMI FPOINT
JMP EPOINT
FPOINT  LDX #00
F2PONT
LDA CHRBUF,X
LDY #00
STA (ADDPTR),Y
STY CNRFLG
JSR INCPTR
```

```
INX
CPX #08
BNE F2PONT
LDX #07
LDY #00
LDA DUMBUF,X
STA DUMBUF+9
ALOOP   DEX
INY
LDA DUMBUF,X
STY CONTR1
GPOINT  ASL A
DEC CONTR1
BNE GPOINT
CLC
ADC DUMBUF+9
STA DUMBUF+9
CPX #00
BNE ALOOP
LDY #00
STA (LODPTR),Y
INY
STY CNRFLG
JSR INCPTR
RTS
APOINT  LDA #00
STA CNRFLG
LDX #08
BLOOP   JSR INCPTR
DEX
BNE BLOOP
INC CNRFLG
JSR INCPTR
RTS
;------------------------------
;SUBROUTINE QLOOP, FOR DELAY ACQUISITION
QLOOP   LDA #01
JSR PROMPT
LDX #00
RLOOP   JSR REDOUT
CMP #$0D
BEQ RRTURN
STA CHRBUF,X
INX
JMP RLOOP
RRTURN PHA
JSR CRLF
PLA
CPX #00
BEQ HPOINT
CPX #04
BEQ IPOINT
LDA #$33
STA ERRNUM
JSR ERROR
JMP QLOOP
HPOINT  JMP QQTURN
IPOINT  LDX #02
```

```
JPOINT  LDA CHRBUF,X
JSR ASCHEK
KPOINT  LDA ERRFLG
CMP #00
BEQ LPOINT
LDA #$34
STA ERRNUM
JSR ERROR
JMP QLOOP
LPOINT  DEX
BMI MPOINT
JMP JPOINT
MPOINT  LDX #00
M2PONT
LDA CHRBUF,X
LDY #00
STA (ADDPTR),Y
STY CNRFLG
JSR INCPTR
INX
CPX #04
BNE M2PONT
LDA CHRBUF+3
CMP #'K'
BEQ NKPONT
CMP #'S'
BEQ NSPONT
CMP #'M'
BNE NM1ONT
JMP NMPONT
NM1ONT
CMP #'U'
BNE NEXT1
JMP NUPONT
NEXT1  CMP #'N'
BNE NEXT2
JMP NNPONT
NEXT2 LDA #$35
STA ERRNUM
JSR ERROR
JSR DECPTR
JSR DECPTR
JSR DECPTR
JSR DECPTR
JMP QLOOP
NKPONT  LDA #00
STA CNRFLG
JSR DECPTR
JSR DECPTR
JSR DECPTR
JSR DECPTR
LDA #$30
LDY #00
STA (ADDPTR),Y
JSR INCPTR
JSR INCPTR
JSR INCPTR
JSR INCPTR
```

```
INC CNRFLG
LDA #00
LDX #05
LDY #00
JSR LODBYT
LDA DUMBUF+1
LDY DUMBUF+2
JSR BINDEC
LDY #00
STA (LODPTR),Y
JSR INCPTR
JMP BBPONT
NSPONT  LDA #01
STA CNRFLG
LDA #00
LDX #03
LDY #00
JSR LODBYT
LDA DUMBUF+2
LDY #01
JSR BINDEC
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA DUMBUF
LDY DUMBUF+1
JSR BINDEC
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA #00
STA (LODPTR),Y
JSR INCPTR
JMP BBPONT
NMPONT  LDA #01
STA CNRFLG
LDA #00
LDX #02
LDY #00
JSR LODBYT
LDA DUMBUF+1
LDY DUMBUF+2
JSR BINDEC
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA #00
LDY DUMBUF
CMP DUMBUF
BMI ZETA1
JMP ZETA2
ZETA1 CPY #09
BNE ZETA3
LDA #01
LDY #00
JMP ZETA2
ZETA3 INY
ZETA2 JSR BINDEC
```

```
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA #00
LDX #02
JSR LODBYT
JMP BBPONT
NUPONT  LDA #01
STA CNRFLG
LDA DUMBUF+2
LDY #00
JSR BINDEC
LDX #01
JSR LODBYT
LDA DUMBUF
LDY DUMBUF+1
JSR BINDEC
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA #00
LDY #00
LDX #04
JSR LODBYT
JMP BBPONT
NNPONT
LDA #00
STA CNRFLG
JSR DECPTR
JSR DECPTR
JSR DECPTR
LDA #$30
LDY #00
STA (ADDPTR),Y
JSR INCPTR
STA (ADDPTR),Y
JSR INCPTR
JSR INCPTR
INC CNRFLG
LDA #00
LDY DUMBUF
JSR BINDEC
CMP #00
BNE AAPONT
LDA #01
AAPONT
LDY #00
STA (LODPTR),Y
JSR INCPTR
LDA #00
LDX #05
JSR LODBYT
JMP BBPONT
QQTURN
LDX #04
LDA #00
STA CNRFLG
QQLOOP  JSR INCPTR
```

```
DEX
BNE QQLOOP
LDA #01
STA CNRFLG
LDX #06
PPLOOP  JSR INCPTR
DEX
BNE PPLOOP
BBPONT  INC COUNTR
RTS
;---------------------------
AATURN  RTS
;----------------------------------
;UTILITY LIST FOR DISPLAY AND DELETION
LIST    LDA #07
JSR PROMPT
BWAIT   LDA #08
JSR PROMPT
JSR REDOUT
PHA
JSR CRLF
PLA
CMP #'T'
BNE B2PONT
JMP TYPE
B2PONT  CMP #'D'
BNE B3PONT
JMP DELETE
B3PONT  CMP #'K'
BEQ ERASE
CMP #'Q'
BNE B1PONT
RTS
B1PONT LDA #$36
STA ERRNUM
JSR ERROR
JMP LIST
ERASE   LDA #00
STA MAINCR
LDA #09
JSR PROMPT
JSR CRLF
RTS
DELETE LDA MAINCR
CMP #00
BEQ ERASE
DEC MAINCR
BEQ B4PONT
JMP BWAIT
B4PONT  LDA #09
JSR PROMPT
JSR CRLF
RTS
TYPE    LDA MAINCR
CMP #00
BEQ B4PONT
STA COUNTR
LDA #00
```

```
STA ADDPTR
STA CNRFLG
LDA #01
STA CONTR1
STA CONTR2
LDA #$20
STA ADDPTR+1
LDA #$0A
JSR PROMPT
JSR CRLF
B5PONT  LDA COUNTR
CMP #00
BNE B6PONT
JMP BWAIT
B6PONT  LDA CONTR1
JSR NUMA
JSR BLANK2
LDX #08
LDY #00
B7PONT  LDA (ADDPTR),Y
JSR OUTALL
JSR INCPTR
DEX
BNE B7PONT
JSR BLANK2
JSR BLANK2
LDX #04
LDY #00
B8PONT  LDA (ADDPTR),Y
JSR OUTALL
JSR INCPTR
DEX
BNE B8PONT
JSR CRLF
DEC COUNTR
INC CONTR1
INC CONTR2
LDA CONTR2
CMP #21
BEQ B9PONT
JMP B5PONT
B9PONT  LDA #04
JSR PROMPT
JSR REDOUT
PHA
JSR CRLF
PLA
CMP #'G'
BEQ C1PONT
CMP #'Q'
BEQ C2PONT
JMP B9PONT
C2PONT  JMP BWAIT
C1PONT  LDA #01
STA CONTR2
JMP B5PONT
;------------------------------------
;SUBROUTINE INCPTR ,FOR DOUBLE BYTE POINTER INCREMENT
```

```
.SKIP
INCPTR  PHA
LDA CNRFLG
CMP #01
BEQ D1PONT
INC ADDPTR
BNE D2PONT
INC ADDPTR+1
D2PONT  PLA
RTS
D1PONT  INC LODPTR
BNE D3PONT
INC LODPTR+1
D3PONT  PLA
RTS
;--------------------------------
;SUBROUTINE ASCHEK,FOR CHECKING VALID ASCII (0-9) IN
;CHRBUF,X
; RETURNS THE BINARY EQUIVALENT FOR VALID
; ASCII IN DUMBUF,X.
;SETS ERRFLG FOR INVALID ASCII
.SKIP
ASCHEK  LDA #00
STA ERRFLG
LDA CHRBUF,X
CMP #$30
BCC E1PONT
CMP #$3A
BCS E1PONT
AND #$0F
STA DUMBUF,X
RTS
E1PONT  INC ERRFLG
RTS
;-------------------------------
;SUBROUTINE ERROR
.SKIP
ERROR   LDA #02
JSR PROMPT
LDA ERRNUM
JSR OUTALL
JSR CRLF
RTS
;---------------------------------
;SUBROUTINE LODBYT
.SKIP
LODBYT  STA (LODPTR),Y
JSR INCPTR
DEX
BNE LODBYT
RTS
;---------------------------------
;SUBROUTINE BINDEC,FOR CONVERTING TWO BYTES INTO
;TWO HEXADECIMAL DIGITS
.SKIP
BINDEC  LDX #04
CLOOP   ASL A
DEX
```

```
BNE CLOOP
STY CONTR5
CLC
ADC CONTR5
RTS
;-------------------------------
;UTILITY TRXFER,FOR LOADING THE GENERATOR BOARD
;-------------------------------
TRXFER  LDA #01
STA CNRFLG
LDA MAINCR
STA COUNTR
LDA #00
STA LODPTR
LDA #$28
STA LODPTR+1
LDA #$FF
STA UDDRA
STA UDDRB
LDA COUNTR
JSR HEXDEC
STA UDRA
LDA #$F8
STA UDRB
LDA #$FC
STA UDRB
CTLOOP  LDA COUNTR
CMP #00
BEQ CTTURN
LDY #00
LDA #$1C
STA CONTR1
LDA #$1E
STA CONTR2
LDA #00
STA CONTR3
LDX #07
LDA (LODPTR),Y
STA UDRA
LDA CONTR2
STA UDRB
LDA CONTR1
STA UDRB
LDA CONTR2
STA UDRB
JSR INCPTR
CULOOP  DEX
BNE T1PONT
JMP T2PONT
T1PONT  LDA (LODPTR),Y
STA UDRA
INC CONTR3
LDA CONTR3
STA CONTR5
ASL CONTR5
ASL CONTR5
ASL CONTR5
ASL CONTR5
```

```
ASL CONTR5
LDA CONTR2
ORA CONTR5
STA UDRB
LDA CONTR1
ORA CONTR5
STA UDRB
LDA CONTR2
ORA CONTR5
STA UDRB
JSR INCPTR
JMP CULOOP
T2PONT
LDA #$F6
STA UDRB
LDA #$FE
STA UDRB
DEC COUNTR
JMP CTLOOP
CTTURN  LDA MAINCR
JSR HEXDEC
STA UDRA
LDA #$FA
STA UDRB
LDA #$EE
STA UDRB
RTS
;-------------------------------
;SUBROUTINE DECPTR
.SKIP
DECPTR
LDA CNRFLG
CMP #01
BEQ U1PONT
SEC
LDA ADDPTR
SBC #01
STA ADDPTR
BCC U2PONT
RTS
U2PONT SEC
LDA ADDPTR+1
SBC #01
STA ADDPTR+1
RTS
U1PONT SEC
LDA LODPTR
SBC #01
STA LODPTR
BCC U3PONT
RTS
U3PONT
SEC
LDA LODPTR+1
SBC #01
STA LODPTR+1
RTS
;---------------------------------
```

```
;SUBROUTINE HEXDEC CONVERTS 8 BIT BINARY INTO
;TWO BCD DIGITS
HEXDEC SEC
PHA
LDA #00
STA CONTR5
PLA
CMP #$0A
BCC V2PONT
V1PONT SBC #$0A
INC CONTR5
CMP #$0A
BCC V2PONT
JMP V1PONT
V2PONT TAY
LDA CONTR5
JSR BINDEC
RTS
;----------------------------------------
;SUBROUTINE SEQINC,FOR INCREMENTING
;(ADDPTR) AND (LODPTR)
SEQINC TXA
PHA
LDX #$0C
LDA #00
STA CNRFLG
GAMMA1 JSR INCPTR
DEX
BNE GAMMA1
INC CNRFLG
LDX #07
GAMMA2 JSR INCPTR
DEX
BNE GAMMA2
PLA
TAX
RTS
;----------------------------------------
;SUBROUTINE SEQADV,FOR SHIFTING
;PATTERN DOWN
SEQADV LDA #$0C
STA CONTR5
LDY #$0B
EK01 TYA
PHA
LDA (ADDPTR),Y
PHA
TYA
CLC
ADC CONTR5
TAY
PLA
STA (ADDPTR),Y
PLA
TAY
DEY
BMI EK02
JMP EK01
```

```
EK02 LDA #07
STA CONTR5
LDY #$06
EK03 TYA
PHA
LDA (LODPTR),Y
PHA
TYA
CLC
ADC CONTR5
TAY
PLA
STA (LODPTR),Y
PLA
TAY
DEY
BMI EK04
JMP EK03
EK04 RTS
;------------------------------
;SUBROUTINE SEQREC,FOR SQUEEZING THE PATTERN
SEQREC LDA #$0C
STA CONTR5
LDY #$17
FOX1 TYA
PHA
LDA (ADDPTR),Y
PHA
SEC
TYA
SBC CONTR5
TAY
PLA
STA (ADDPTR),Y
PLA
TAY
DEY
CPY CONTR5
BCC FOX2
JMP FOX1
FOX2 LDA #$07
STA CONTR5
LDY #$0D
FOX3 TYA
PHA
LDA (LODPTR),Y
PHA
SEC
TYA
SBC CONTR5
TAY
PLA
STA (LODPTR),Y
PLA
TAY
DEY
CPY CONTR5
BCC FOX4
```

```
JMP FOX3
FOX4 RTS
;-------------------------------
;SUBROUTINE SEQDEC
SEQDEC TXA
PHA
LDY #$0C
LDA #00
STA CNRFLG
PHI1 JSR DECPTR
DEX
BNE PHI1
INC CNRFLG
LDX #07
PHI2 JSR DECPTR
DEX
BNE PHI2
PLA
TAX
RTS
;--------------------------------

END
```

Appendix C
W/E & Read Circuit

C.1 Circuit Board

The W/E & Read circuit shown in fig. 3-6, chapter 3 has been implemented on an in-house prepared PCB. The details of the components are detailed below:

OA1-OA4	ADLH0032G;HIGH SLEW RATE (500V/μs) AND WIDE 70MHZ BANDWIDTH
SW1-SW3	DG303; CMOS ANALOG SWITCHES WITH 200NS SWITCHING 20Ω ON RESISTANCE

The opamps and the analog switches are both operated at supply voltages of ±15V. The circuit can handle around ±14V programming level. The V_{DD} level is +5V for n channel and −5V for p channel transistor, selected by manual toggle switch.

All resistors are metal film resistors (1% tolerance). The PCB layout is shown in fig. C-1. The DUT should be bonded on 8-pin (TO-8) headers. The pin configuration can be mapped to the gate, source, substrate and drain connections using jumpers. This allows flexibility to accomodate two devices on

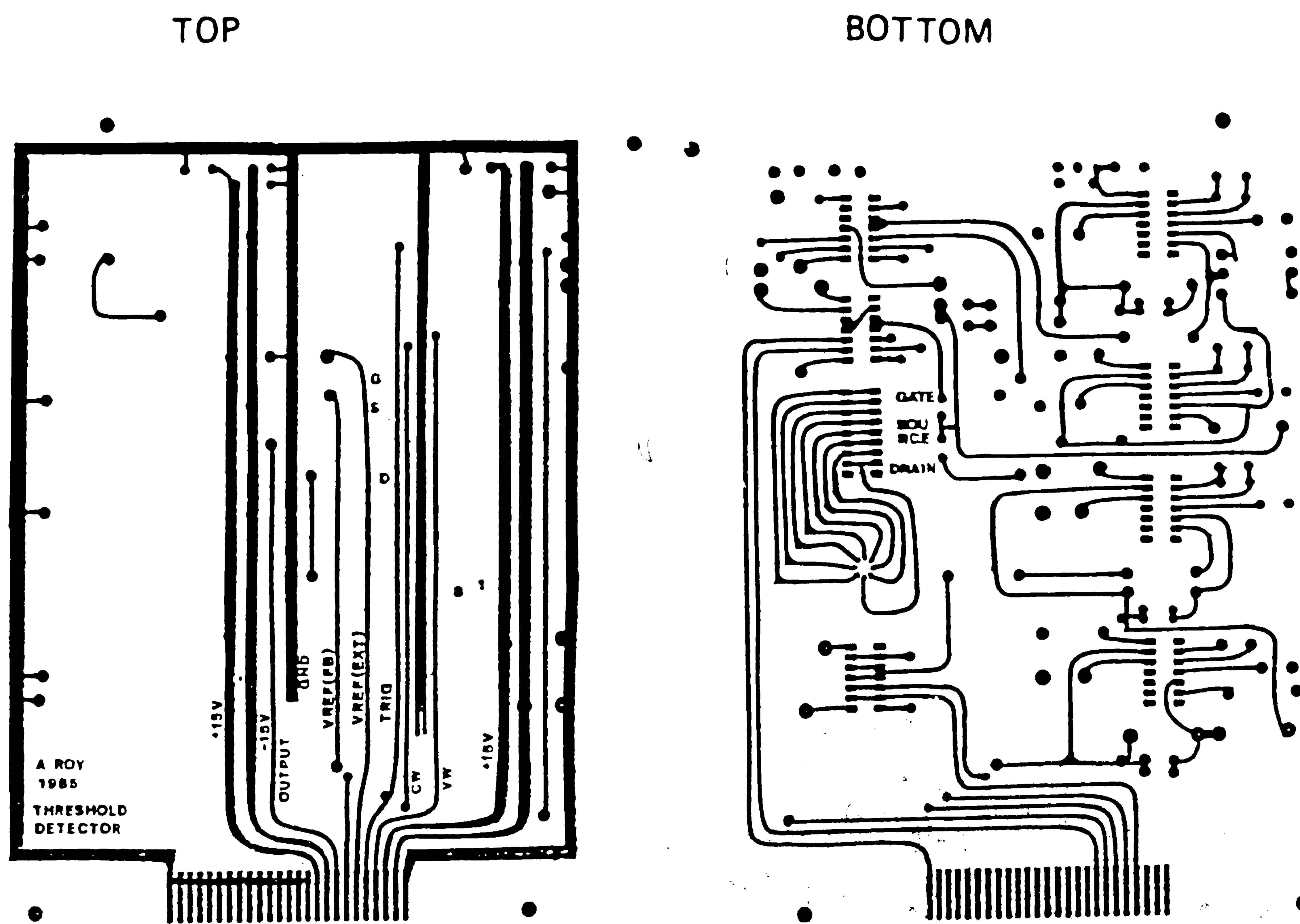


Figure C-1: PCB layout of the W/E & Read circuit

a single header.

C.2 Transient Analysis

The dynamics of threshold detection is one of the essential attributes of the W/E & Read circuit. In this section a first order analysis of the transient response of the circuit, during the initiation of the "read" operation, will be presented.

The circuit diagram in the "read" configuration is shown in fig. C-2 using variables for the resistors and capacitors. C_S is the parasitic capacitance at the source node, contributed by the transistor gate to bulk capacitance, the analog switch and other stray sources.

The analysis presumes an p-channel transistor and that the gate to source voltage V'_T (which supports a 10μA of drain current) is more negative than the classical threshold V_T, as illustrated in fig. C-3. A negative V_T is being considered. The time constants corresponding to the compensating capacitors on the various opamps have been neglected.

For the current source the following current-voltage relations can be written:

$$V_{REF} = -V_{DD} - I_D R_D (1 + \frac{R_F}{R_1})$$

$$I_{REF} = \frac{V_{REF}}{R_S}$$

$$I_{REF} = -\frac{1}{R_S}[V_{DD} + I_D R_D (1 + \frac{R_F}{R_1})] \qquad (C.1)$$

Figure C-2: Circuit diagram during threshold detection

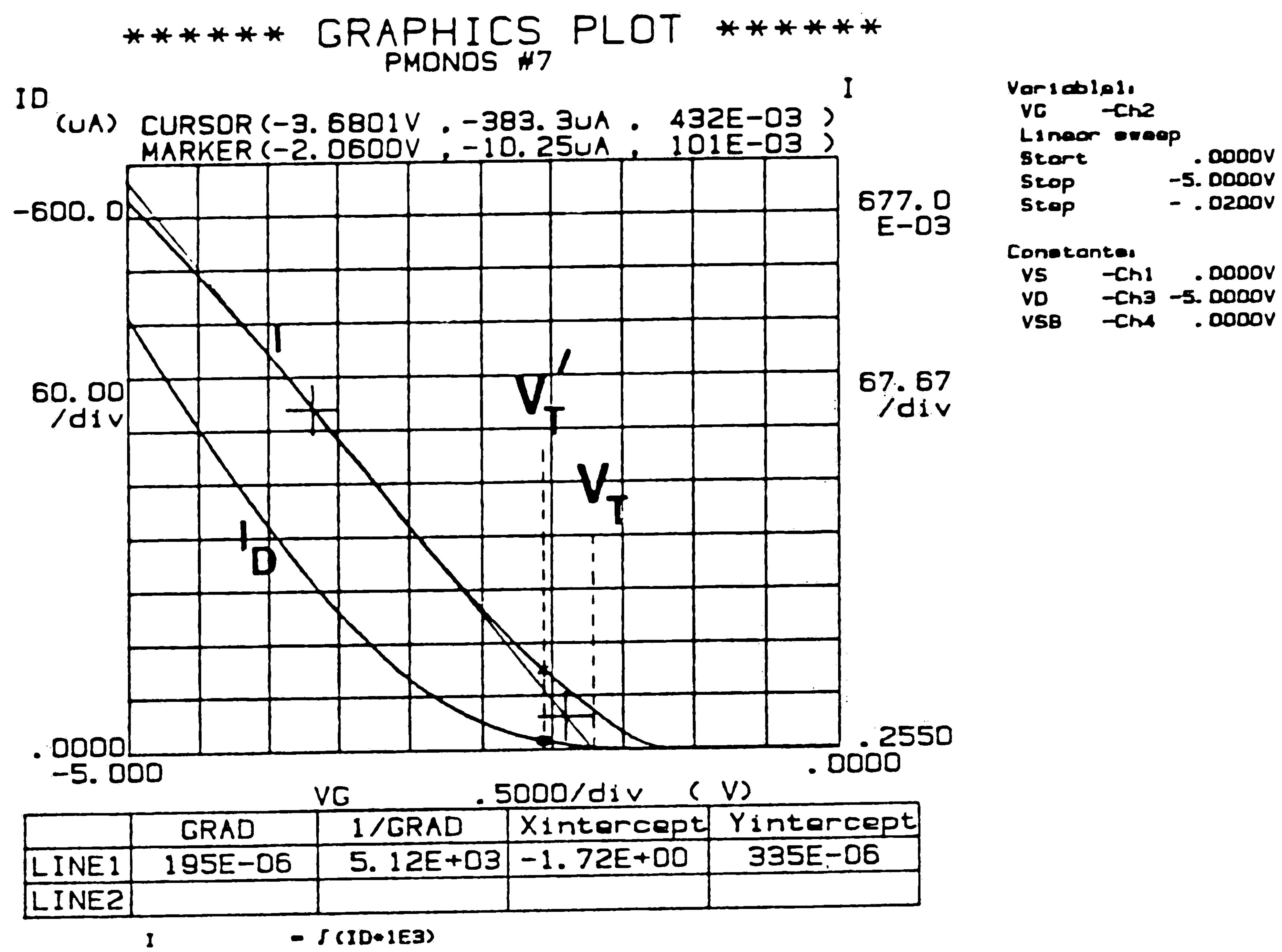


Figure C-3: Difference between classical threshold V_T and V_T'

The charging equation is:

$$C_S\frac{dV_{out}}{dt} = I_{REF} - I_D \tag{C.2}$$

Consider an initial condition of $V_{out}=0$; then for $V_{out} < |V_T|$ we have $I_D \ll I_{REF}$. This leads to the relation :

$$V_{out} = -\frac{V_{DD}t}{R_S C_S} \tag{C.3}$$

Consider $V_{out} > |V_T|$. Assume that the transistor is operating in the saturated state (classically), i.e.,

$$I_D \approx \frac{\beta}{2}(V_{out}+V_T)^2 \tag{C.4}$$

The equations (C.2), (C.1) and (C.4) can be simplified to give:

$$\frac{dV_{out}}{dt} = -[\frac{V_{DD}}{R_S C_S} + \frac{\beta}{2C_S}(V_{out}+V_T)^2\{\frac{R_D}{R_S}(1+\frac{R_F}{R_1}) + 1\}]$$

Substitute $V'_{out} = V_{out}+V_T$, $\gamma=\frac{V_{DD}}{R_S C_S}$ and $\alpha=\frac{\beta}{2C_S}\{\frac{R_D}{R_S}(1+\frac{R_F}{R_1}) + 1\}$ and obtain:

$$\frac{dV'_{out}}{-V'^{2}_{out}+\frac{\gamma}{\alpha}} = \alpha dt$$

Use the initial condition that $V'_{out}=0$ at $t=t_0$, where t_0 is given by $t_0=\frac{V_T R_S C_S}{V_{DD}}$.

The solution for $\mathbf{t} > \mathbf{t}_0$ is:

$$V_{out} = -V_T + \sqrt{\frac{\gamma}{\alpha}}[1 - \frac{2}{exp\{2\sqrt{\alpha\gamma}(t-\frac{V_T}{\gamma})\}+1}] \tag{C.5}$$

The solution for $\mathbf{t} < \mathbf{t}_0$ is given by equation (C.3). The solution for V_{out} is sketched in fig. C-4. It can be compared to the photograph for V_{out} in fig. 3-8 in chapter 3. The ringing in the waveforms can be explained by the delay in the feedback of the circuit which we have neglected in the analysis.

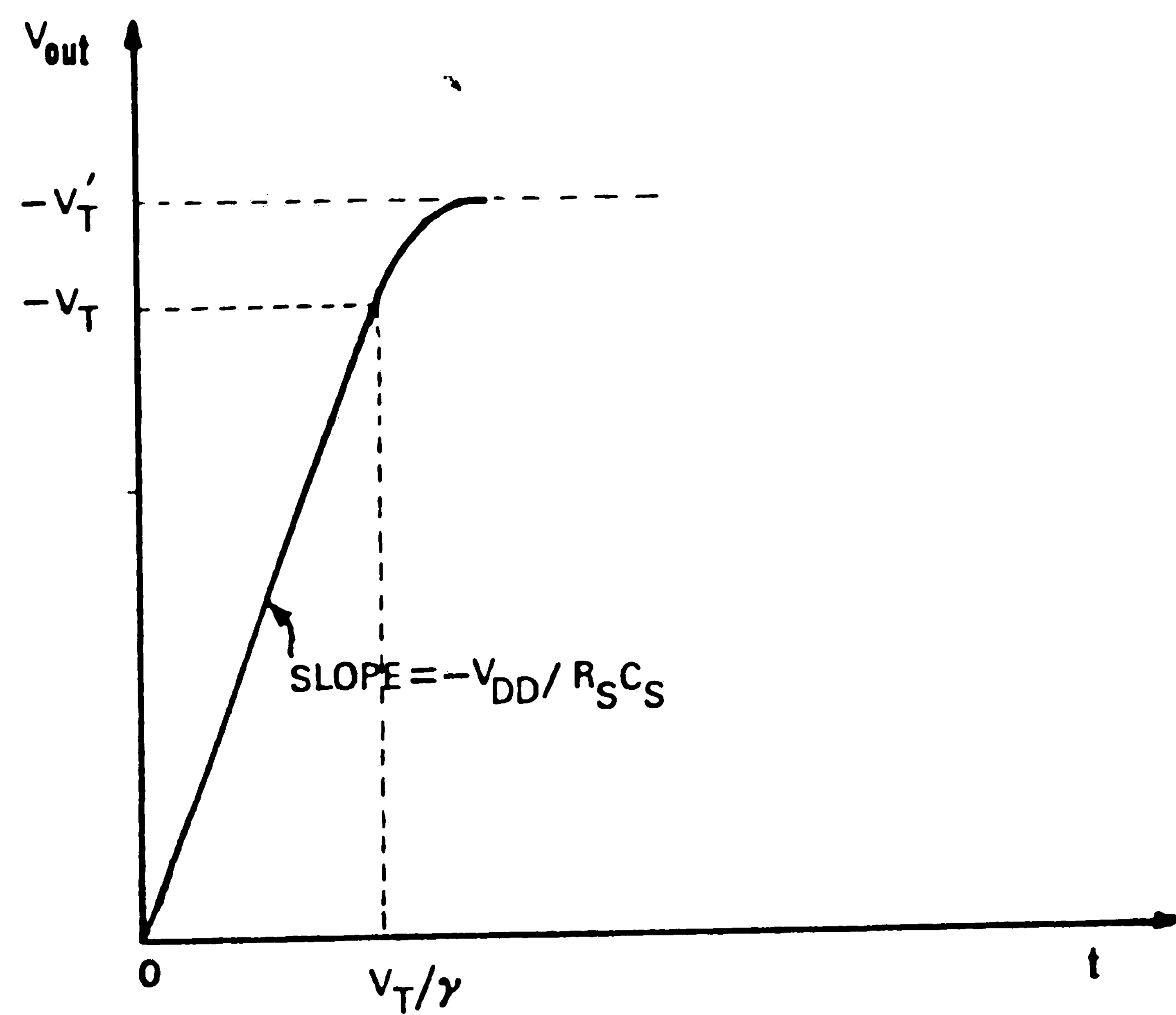


Figure C-4: Transient response of the circuit during threshold acquisition.

Appendix D
FABRICATION TECHNOLOGY

The Microelectronics Laboratory, a part of the Sherman Fairchild Center at Lehigh University, has a unique "in-house" capability to vary the device technology parameters, and study their influence on the physical electronics of the MONOS memory microstructure. The device cross-section of complementary MONOS transistors is shown in fig. D-1.

The design of microstructures was done with the Applicon 860 VLSI Interactive Graphics System, followed by E-Beam generation of photomasks at the local AT&T Bell Lab. facilities. The test pattern TP100 is a multi-project effort and the transistor structures on this have been characterized for the present study. Fig. D-2 shows the test pattern designed for CMOS-MONOS microstructures and 5μm design rules.

The starting material is <100> oriented n-type Si sustrate. The process sequence used only diffusion for incorporation of impurities in the silicon. The bottom two layers of dielectric viz., the tunnel oxide and the nitride were grown in the LPCVD deposition system. The blocking oxide is formed by steam oxidation of the nitride. Aluminium is vapour deposited as the gate metal and source, drain and bulk contact metal.

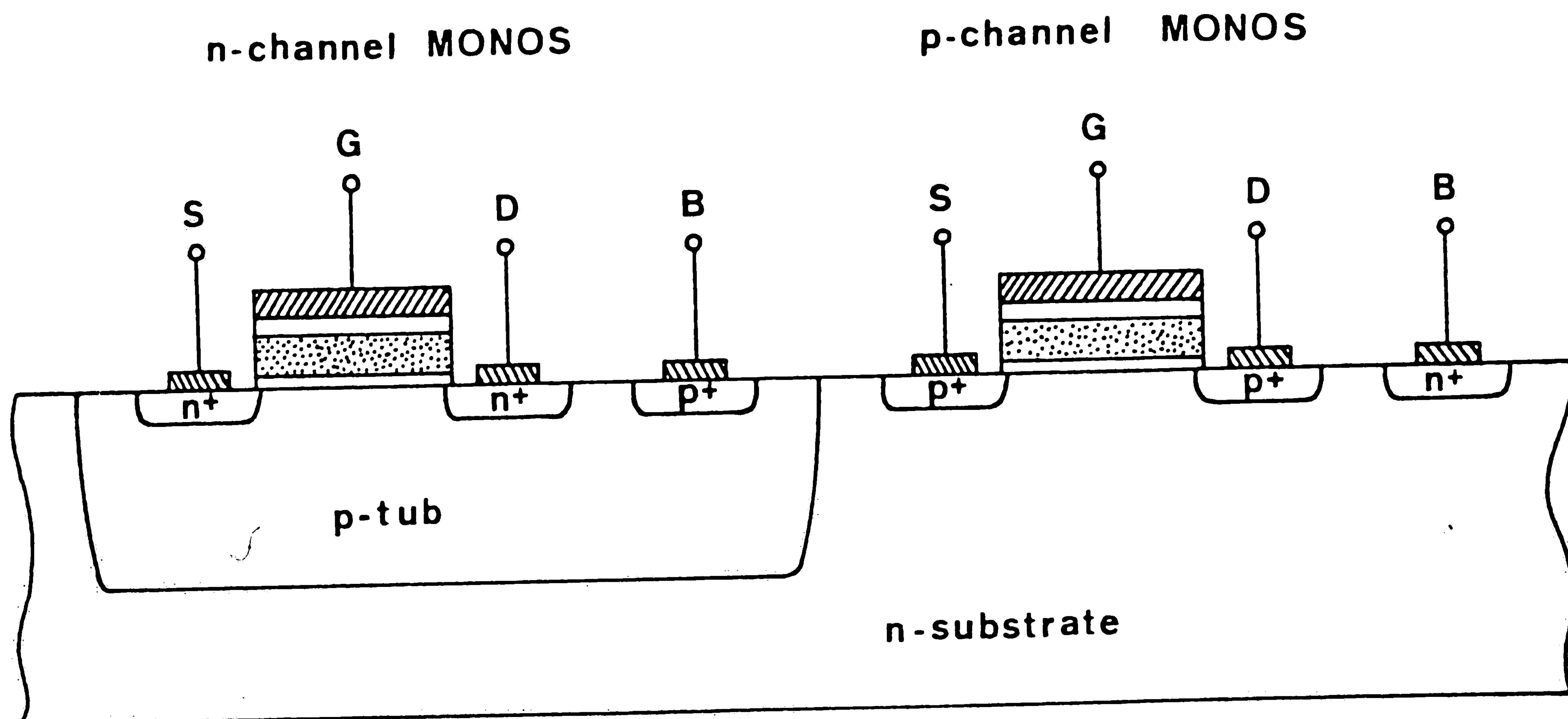


Figure D-1: Cross-section of complementary MONOS transistors

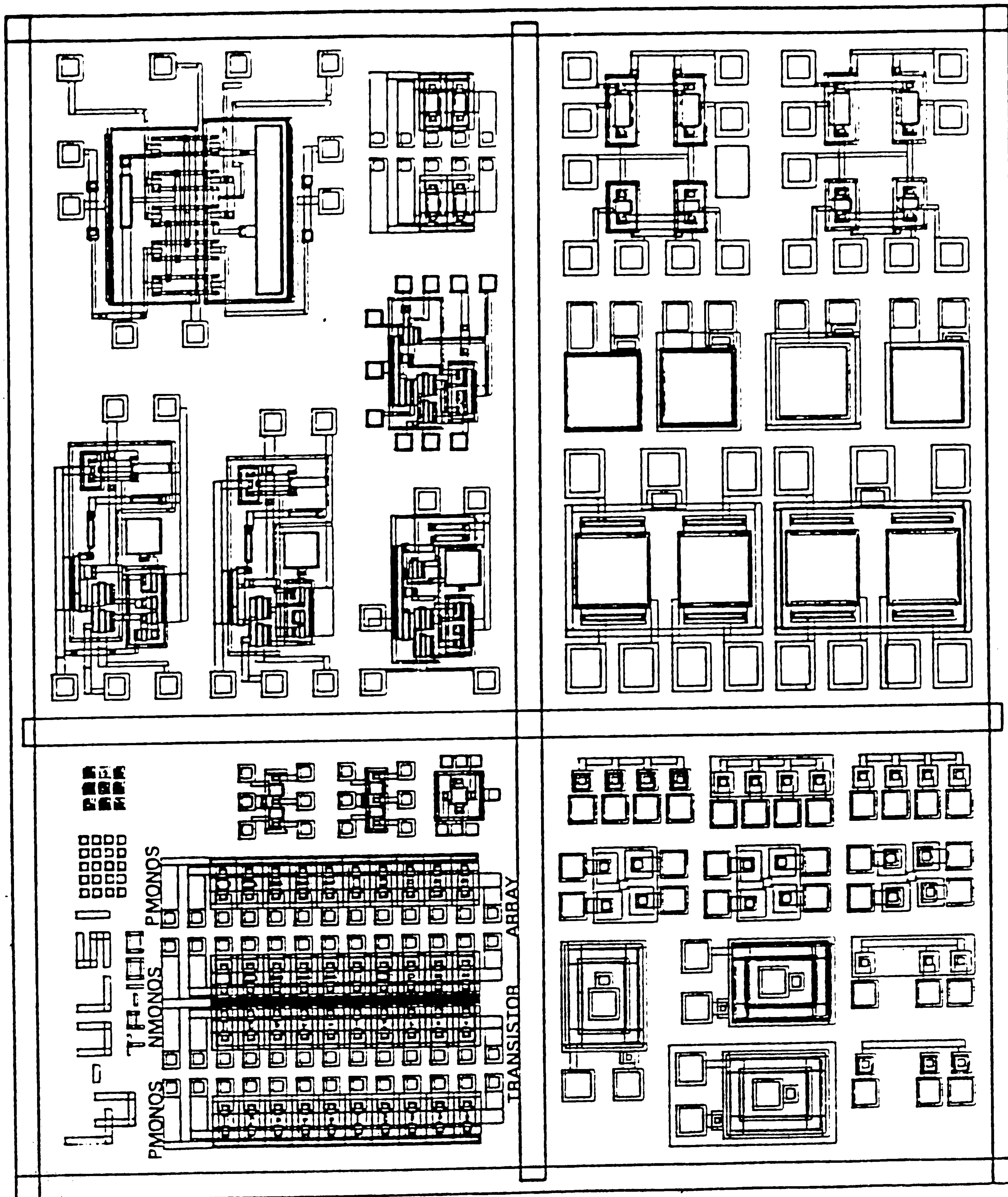


Figure D-2: Test pattern TP100, a multi-project chip

D.1 Process Sequence

The process sequence is detailed below:

STARTING MATERIAL: n <100> , 5-10Ω-cm Si wafers.

1. Intrinsic Getter

   a. Clean and HF etch.

   b. Wet oxidation for field oxide 5kA (1100°C , 40 min.)

   c. Anneal (N_2 , 700°C , 16 hrs.)

2. P-Tub Formation

   a. Photolithography (Mask 1)

   b. Etch oxide and clean

   c. Diffusion (predeposition) of B (900°C , 15 min.)

   d. Etch borosilicate glass.

   e. Wet oxidation for 5A field oxide (1100°C , 40 min.)

   f. Drive-in-diffusion (1150°C , 24 hrs. ,N_2)

for tub depth of 10μm.

3. P+ Source and Drain

a. Photolithography (Mask 2)

b. Etch oxide and clean.

c. Diffusion (Predeposition) of Boron (900°C , 30 min.).

d. Drive-in (N_2 , 1100°C , 1 hr.).

e. Etch glass.

f. Wet oxidation 3kA (1100°C , 20 min.).

4. N+ Source and Drain

a. Photolithography (Mask 3)

b. Etch oxide and clean

c. Diffusion (Predeposition) of Phosphorus (900°C , 30 min.).

d. Wet oxidation (1100°C , 40 min.).

e. Drive-in (N_2 , 1100°C , 30 min.).

5. Gate Dielectrics

a. Photolithography (Mask 4)

b. Etch oxide and clean

c. Grow tunnel oxide 20A (dry O_2 , 730°C , 14 min.).

d. LPCVD Si_3N_4 deposition 116A (730°C , NH_3:$SiCl_2H_2$=100:30 , 0.3 torr , deposition rate=15A/min).

e. Wet oxidation for blocking oxide (1000°C , 50 min.).

f. Anneal (N_2 , 1000°C , 15 min.).

6. Contact Window

a. Photolithography (Mask 5)

b. Etch oxide (buffered HF)

c. Etch nitride (plasma etching , 96% CF_4 , 4% O_2).

d. Etch oxide (buffered HF)

e. Clean

f. Anneal (forming gas , 600°C , 1.5 hrs.).

g. Etch oxide (10% HF)

7. Metallization

a. Vapor deposition of Aluminum 10kA.

b. Photolithography (Mask 6)

c. PAN etch for Aluminum.

d. Sinter (450°C , 30 min. , N_2)

Appendix E
Operational Details

E.1 Test Station Operation Under Local Mode

The test station should be operated by the following power up starting procedure:

- POWER ON the Rockwell computer and the terminal.
- POWER ON the TEK 7854 scope.
- POWER ON the pattern generator (5V); and place it in RESET mode.
- EDIT the SEQUENCE on the Rockwell terminal.
- TRANSFER the SEQUENCE to the pattern generator.
- SELECT the device type ("n" or "p") with the manual switches on the W/E & Read circuit module front panel.
- POWER ON the ±15V supplies to the W/E & Read circuit.
- POWER ON the ±5V supplies to the W/E & Read circuit.
- POWER ON the programming voltage power supplies to the W/E &

Read Circuit.

- MAP the connections for gate, source, bulk and drain with the jumpers on the W/E & Read circuit board.

- PLACE a resistor (say 1kΩ) across the source and drain connections on the socket (DIP) on the W/E & Read circuit board.

- PLACE the DUT on the TO-socket.

- REMOVE the resistor from the socket.

- START the pattern generator for the exercising the DUT.

The power down procedure is almost the reverse of the power up procedure. The procedure is detailed for user convenience:

- RESET the pattern generator.

- REPLACE the resistor between the source and drain connections on the socket.

- REMOVE the DUT.

- POWER DOWN the programming voltage power supplies.

- POWER DOWN the ±5V supplies to the W/E & Read circuit.

- POWER DOWN the ±15V supplies.

- POWER DOWN the 5V supply to the pattern generator.

- POWER DOWN the rest of the equipment.

E.2 Test Station Operation Under Remote Mode

The power on procedure is the same as in the previous section only the HPIB interface from the scope to the HP9836 computer must be established. The remote control lines for the pattern generator from the programming power supplies should be tested for a maximum voltage swing of 0-5V (since there is no overvoltage protection on-board). The start and reset lines are to be pulsed low, and should be normally high. After the remote lines are connected switch manually to remote mode. The software to be run on the HP computer is only a variation of the program detailed in the thesis by F.R. Libsch [16].

E.3 Editing Session For Pattern Generation

An example of the editing session using the software on the AIM 65 computer is given below:

```
<*>=COOO

<G>/
NUMBER OF SEQUENCES=OO
WELCOME TO THE DRIVER ROUTINE
UTILITIES: E=EDITOR , L=LIST , T=TRANSFER
*E
A=APPEND ,M=MODIFY ,Q=QUIT
%A
PATTERN =10000000
DELAY =100N
PATTERN =10101010
DELAY =002U
```

```
PATTERN =000011001
FORMAT ERROR #1
PATTERN =00000111
DELAY =967M
PATTERN =00110011
DELAY =675S
PATTERN =09
FORMAT ERROR #1
PATTERN =01011100
DELAY =989M
PATTERN =Q
A=APPEND ,M=MODIFY ,Q=QUIT
%Q
```

<*>=*C000* initializes the program counter (of the AIM 65) at the beginning of the software. The utility EDITOR is the most intense part of the software. APPEND is useful for adding a string of PATTERN and DELAY with minimal protocol. For PATTERN specification start from left to right (channels 1-8) with a string of 1's and 0's for each channel. For DELAY specification four characters are required (first three are numbers between 0 and 9 and the last character is the unit of time). The abbreviations for the time character is as follows:

N-----------nanoseconds(only in hundreds of ns.)
U-----------microseconds.
M-----------milliseconds.
S-----------seconds.
K-----------thousand of seconds.

To exit from APPEND type "Q" as the PATTERN.

```
*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
      PATTERN    DELAY
01   10000000    100N
02   10101010    002U
03   00000111    967M
04   00110011    675S
05   01011100    989M
```

```
^Q
*E
A=APPEND ,M=MODIFY ,Q=QUIT
%M
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$R
LINE NUMBER=03

PATTERN =01000110
DELAY =56[illegible]U
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$Q
A=APPEND ,M=MODIFY ,Q=QUIT
%Q

*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
     PATTERN     DELAY
01   10000000    100N
02   10101010    002U
03   01000110    567U
04   00110011    675S
05   01011100    989M

^Q
*E
A=APPEND ,M=MODIFY ,Q=QUIT
%M
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$I
LINE NUMBER=04

PATTERN =00000000
DELAY =598N
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$Q
A=APPEND ,M=MODIFY ,Q=QUIT
%Q

*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
     PATTERN     DELAY
01   10000000    100N
02   10101010    002U
03   01000110    567U
04   00000000    500N
05   00110011    675S
06   01011100    989M

^Q
*E
A=APPEND ,M=MODIFY ,Q=QUIT
%M
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$D
LINE NUMBER=04
```

```
R=REPLACE ,D=DELETE ,I=INSERT ,Q=QUIT
$Q
A=APPEND ,M=MODIFY ,Q=QUIT
%Q

*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
     PATTERN     DELAY
01  10000000    100N
02  10101010    002U
03  01000110    567U
04  00110011    675S
05  01011100    989M

^D

^T
     PATTERN     DELAY
01  10000000    100N
02  10101010    002U
03  01000110    567U
04  00110011    675S

^K
NO PATTERN LEFT
*
```

At this point the "SEQUENCE length" is 0, but 5 SEQUENCES were edited at one stage. They are not lost!! So to retrieve the SEQUENCES go into monitor mode and execute the program once again but respond with "05" for NUMBER OF SEQUENCES.

```
<*>=C000

<G>/
NUMBER OF SEQUENCES=05
WELCOME TO THE DRIVER ROUTINE
UTILITIES: E=EDITOR , L=LIST , T=TRANSFER
*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
     PATTERN     DELAY
```

```
01  10000000    100N
02  10101010    002U
03  01000110    567U
04  00110011    675S
05  01011100    989M

^Q
*E
A=APPEND ,M=MODIFY ,Q=QUIT
%A
PATTERN =00000000
DELAY =234U
PATTERN =11111111
DELAY =090K
PATTERN =Q
A=APPEND ,M=MODIFY ,Q=QUIT
%Q

*L
T=TYPE ,D=DELETE LAST LINE ,K=ERASE ALL ,Q=QUIT
^T
     PATTERN    DELAY
01  10000000    100N
02  10101010    002U
03  01000110    567U
04  00110011    675S
05  01011100    989M
06  00000000    234U
07  11111111    090K

^Q
*T
```

E.4 Sequence For Erase-Write Measurements

The SEQUENCE used for erase-write measurements (as described in chapter4) is shown below with comments.

	PATTERN	DELAY	Comments
01	00000010	002S	Idle mode for 2s.
02	00000011	010S	Erase mode for 10s.
03	00000010	100U	Idle mode for 100μs.
04	00000110	001U	Write mode for 1μs.
05	00000010	100N	Idle mode for 100ns.
06	00010010	004U	Read delay for 4μs.
07	00011000	050U	Read mode for 50μs.

Repeats after this!! useful
for repetitive sampling.

VITA

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