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Garrett James Derbyshire
Lehigh University

DESIGN OF A MICROPROCESSOR BASED SYSTEM FOR PROVIDING BEAM FOCUSING AND STEERING SUPPORT IN A PHASED ARRAY ULTRASOUND SYSTEM

by

Garrett James Derbyshire

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

3/1/85
(date)

Douglas King
Professor in Charge

Eric P. Thompson
Chairman of Department

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Abstract

Ultrasound is a safe, non-invasive real-time imaging technique that is employed in obstetrics, cardiology and radiology.[3,5,6,8] In order to create a cross-sectional scan through soft tissues, phased array ultrasound sweeps a narrow sound beam across a 90° sector plane utilizing electronic beam focusing and steering. Beam control is accomplished using a linear piezoelectric transducer array with rapidly adjustable phase and time delays.[1,7,12] Digitally controlled multi-tapped L-C delay lines produce variable time delays and the variable phase delays are controlled through local oscillator phase. The delay subsystem must determine the delays required for proper beam control and convert the delays into "coefficients" which select the proper LO phases and L-C taps. Previous system designs have stored delay coefficients in ROM which leads to system inflexibility.

In this paper, an ultrasonic imaging system design is presented with various aspects of the design being discussed in some detail. Special emphasis is placed on methods for increasing image resolution by custom calculating the delay coefficients.

Image resolution is difficult to improve with ROM based systems; therefore, a microprocessor/RAM based coefficient generating system was developed with the

capacity to custom calculate the coefficients in a nominal amount of time. This hardware implementation utilizes a recursive approach to calculating the required delay coefficients. Because real time imaging requires fast RAM access, a hardware RAM sequencer and a dynamic RAM controller were developed which would support high RAM access speed and provide automatic RAM refresh.

The resultant design is capable of generating delay coefficients for high resolution imaging while minimizing power and space requirements. Recursion decreased the calculating time to an acceptable time period and the increased system flexibility can provide for an almost unlimited number of transducer frequencies. All together, the new design has the potential for providing image resolution and system flexibility unmatched by previous designs.

Introduction

The primary goal of medical imaging is to non-invasively view internal structures of the human body. The imaging process consists of two parts. First, the object to be imaged must be radiated with energy. The irradiated object then reflects, absorbs or scatters the incident radiation. The second step is to reconstruct the image of the object using the received energy. Forms of radiation such as X-rays and ultrasound readily interact with tissue based on various tissue properties.

Ultrasonic imaging systems present the mechanical properties of tissue (i.e. parameters such as elasticity and density) in the form of an image. In the image, organ boundries and fluid-tissue interfaces are easily identified. Information provided by ultrasound is complementary to other medical imaging modalities such as X-ray in which the image is based upon the nuclear density of the irradiated tissue.

A particular advantage of ultrasonic imaging is that it can be done in "real time". This allows rapidly moving structures such as the heart to be imaged without distortion. Also, it enables the operator to manipulate the ultrasonic transducer over the body surface to obtain an optimum image in an interactive way.

Ultrasound appears to be one of the safest medical

imaging modalities currently available. The non-invasiveness and use of non-ionizing radiation make ultrasound the preferred method for fetal and obstetrical imaging. Various studies have been done on the possible side effects of ultrasound and so far none has demonstrated any harmful effects during clinical examinations.

Ultrasound cannot be used to image all parts of the body. Bone is highly attenuative and air interfaces are excellent reflectors of ultrasound, hence making it difficult to image through bony structures such as the skull or air filled structures such as the lungs. Areas of the body where ultrasound is particularly useful include cardiac structures, abdominal organs such as the liver, kidneys and gall bladder, and the fetus and uterus.

In addition to imaging body structures, ultrasound can also be used to determine blood velocity[6]. This is done by detecting the Doppler shift in the returning echoes which is caused by the moving fluid. This property of ultrasound can be extremely useful in diagnosing various hemodynamic disorders such as valvular regurgitation and thrombotic turbulence. Doppler can also be used to non-invasively determine cardiac output.

The principle problem at hand is to develop a

versatile imaging system which will be capable of not only generating high resolution 2-dimensional images but which will also be capable of detecting Doppler shifts. More specifically, this paper will approach some of the problems involved in the design of a phased array ultrasound system utilizing electronic beam focusing and beam steering. The heart of the ultrasonic beam control, a powerful 16-bit microprocessor based delay coefficient system, will be investigated in significant depth. Specific reasoning behind the design approach taken will be discussed in greater detail later.

Physical Principles of Ultrasound

Ultrasound refers to sound that has a frequency (f) beyond the range of human hearing. The sound waves consist of periodic regions of local compression and rarefaction which propagate through a medium at some velocity (v) with a wavelength determined as follows[5]:

$$\text{wavelength} = v / f$$

where: v = velocity (meters/sec)
f = frequency (hertz)

Acoustic imaging is often done at 3.5 MHz and since the velocity of sound in soft tissue is approximately 1540 m/s, the wavelength is 0.44 mm. Since it is not possible to resolve objects smaller than a wavelength, it is desirable to image at the highest possible frequency (smallest wavelength) to get the best resolution[9].

The ultrasonic wave is transmitted and received with a piezoelectric transducer. This is a crystalline ceramic which converts an electrical signal into acoustic energy and vice versa. The transducer's physical construction will be discussed in more detail later. For imaging, the transducer is placed directly on the skin surface.

As the sound wave propagates through the body, the acoustic intensity is attenuated exponentially with the propagation distance. The acoustic attenuation also

increases exponentially with frequency. A typical attenuation coefficient for soft tissue is 1 dB/cm/MHz. For example, when imaging a structure that is 10 cm deep in the body at 3.5 MHz, the round trip attenuation would be 70 dB. At 10 MHz the round trip attenuation would be 200 dB. This demonstrates a basic and important trade-off in ultrasonic imaging: As the frequency is increased in order to achieve finer resolution, the penetration depth is decreased[7]. This makes it desirable to provide a wide selection of transducer frequencies, thus allowing the user to best optimize the resolution/penetration depth trade-off for each application.

The most common mode of acoustic imaging is the pulse echo mode which is analogous to radar. A short burst of acoustic energy is directed into the body and the reflected energy is received at a later time. Different tissues reflect energy depending on their characteristic acoustic impedance. The impedance is defined by:

$$Z = p \times v$$

where: Z = Impedance (Rayls)
p = Density (Kg/m**3)
v = Velocity (meter/sec)

As the sound passes between tissues of different acoustic impedances, a portion of the sound wave is reflected back. For example, when sound crosses the

boundry between muscle (Z = 1.7 x 10**6 Rayls) and blood (Z = 1.6 x 10**6 Rayls), about 3.0% of the incident sound energy is reflected back. This echo is the signal that is used to create the image of the blood-muscle interface. The rest of the sound is transmitted across the interface and continues into the body to image deeper structures.

Other tissue structures can also interact with sound giving that tissue a unique textural appearance. Objects which are much smaller than a wavelength of the sound wave tend to cause a diffuse omnidirectional scattering, creating a smooth, filled in appearance. If the object is much larger than the sound wavelength, it will act much like a mirror and thus create a distinct tissue boundry.

Ultrasonic Imaging Systems

The most common type of acoustic imaging generates a cross-sectional "slice" through an object by sweeping a narrow beam of sound through a sector in the scan plane. The pulse rate is selected such that the transmitted sound wave has time to travel to the deepest target and back again before the next sound pulse is launched. The sound wave is assumed to travel in a straight line with a constant velocity. As the sound propagates through the body along any scan line, echoes are generated from tissue interfaces which travel back to the receiver. The data is presented on a cathode ray tube (CRT) display in which the image brightness is a function of the received echo strength. An image can be formed in real time since it takes only 260 us for sound to travel 20 cm into the body and back. For example, if the display frame rate is 30 frames per second, there can optimally be 125 scan lines in the sector image.

In practice, the transmit and receive functions are separate but reciprocal processes. Consider the events necessary to generate one line of an image. First a set of transmit pulses are launched so as to provide a coherent wavefront along a given line. This transmit beam is fixed-focused at mid range. As the transmitted wavefront propagates through the body, it is reflected

off tissue boundries along the scan line and echoes start returning to the transducer array. After transmitting the ultrasonic beam, the system switches to the receive mode. In the receive mode, the array progressively changes its receiver focal depth to successively deeper regions at the same time that the echoes are being received from the deeper regions, thus tracking the sound wave through the tissue. This process greatly enhances the image quality and is called dynamic focusing.

The phased array approach to the sector scan uses a linear, stationary array of many small transducers which are electronically controlled to steer and focus the beam. In effect, the system acts like an acoustic lens with an electronically variable focal length and angle[12]. This concept is shown in figures 1 and 2.

Assume that a region of tissue at some location P has reflected a short pulse of sound. The returning echo will reach each transducer element E(n) along the array at a different time, depending on the position of P. Variable time delay elements T(n) in series with each transducer element are rapidly varied under computer control to bring the electrical pulses generated by the transducer elements into coincidence at the summing junction. For instance, if the object is on axis but far away from the array, the returning wavefronts are

essentially planar and the time delays are set equal. If the object is off-axis, at some angle in the far field, the time delays must be varied linearly across the array aperture for coherent summation. Deflecting the sound beam in this manner is called beam steering. When the object is close to the array, the approaching wavefront is curved and the delay distribution across the array is nearly parabolic. Changing the delays to accommodate the curvature of the wavefront is called beam focusing and is necessary to achieve optimal resolution in the near field.

Resolution is a measure of the system's ability to visually separate small objects in the scan plane[9]. It has three components: Range resolution (along the scan line), azimuthal resolution (perpendicular to the scan line), and elevation resolution (the thickness of the sector scan slice). The range resolution is determined by the acoustic pulse length: A short pulse gives high range resolution. The pulse length is primarily determined by the system bandwidth and the transducer design. The resolution in the azimuthal direction depends on the transducer array aperture and the acoustic wavelength. High azimuthal resolution is achieved with a large aperture and a short wavelength. Dynamic focusing optimizes the azimuthal resolution of the imaging system.

The elevation resolution is determined by the silicon rubber acoustic lens placed on the transducer.

A simplified block diagram for an ultrasonic imaging system is shown in figure 3. The system consists of five functional blocks: Transducer, transmitter, receiver, display and control. The transmitter excites the transducer elements with short electrical pulses so that the sound wave is generated. The returning echoes are first applied to a variable gain stage called a time gain compensation (TGC) amplifier. This amplifier increases its gain with time as echoes come from deeper regions of the body, thus compensating for the tissue attenuation. In a phased array system each element of the transducer has its own TGC amplifier. The function of the beam former is to combine the outputs of the individual receiver channels. The beam former uses variable time delay and phase adjustments to bring the received signals into coincidence and hence to bring an object into focus. The signal is then analog to digital converted so that an entire image frame can be stored in the digital memory of the digital scan converter (DSC). The digital scan converter changes the scan format from sector to conventional T.V. raster scan. These activities are coordinated under processor control.

Phased Array Transducer

The transducer utilized in the phased array ultrasound system consists of 64 evenly spaced PZT-5H (Lead Zirconate Titanate) ceramic piezoelectric crystals. The crystals are driven in the transmit mode by a 400 volt p-p square wave pulse which cause the crystals to resonate for up to 3 cycles at the resonant frequency.

Figure 4 shows the steps required to produce the transducer array. The base of the transducer stack consists of a backing material which is acoustically lossy (dampening) and is impedance matched to the rest of the stack. A thin metallic foil layer is attached to the backing in order to provide an electrical contact with the PZT ceramic layer. The 64 long, narrow transducer elements are formed by sawing through the PZT and foil layers with a fine diamond saw. The resulting elements are 14 mm long by 0.48 mm thick and are 0.25 mm wide with an element spacing of 1/2 the sound wavelength. Because of the frequency dependence of the element spacing, a different transducer is required for each transducer frequency. A layer of thin brass foil is then attached to the crystal array to provide the common electrical contact with the PZT. Finally, a convex, cylindrical acoustic lens made of silicon rubber is attached to the foil to provide the fixed focusing in the

elevation plane.

The resultant transducer produced by this technology meets the following transducer requirements: Minimal element-to-element spacing to eliminate side lobes, minimal element-to-element coupling, wide bandwidth to provide short acoustic pulses, adequate sensitivity and minimal element gain variation[7,12].

Signal Delay Theory

The phased array sound beam can be steered up to 45 degrees off the center axis and can be focused at depths ranging from 2 cm to 24 cm by using a combination of digitally controlled time delays and phase adjustments. A multi-tapped delay line provides the course time delay while a vernier phase adjustment provides a fine delay control.

Each of the receiver channels is heterodyned with a local oscillator (LO) to create an IF frequency of 1.7 MHz. The phase of the local oscillator is digitally adjustable. Such phase variations are imposed on the signals by the mixers to allow for the coherent, in phase addition of the received signals. The course time delay adjustment is provided by a multi-tapped L-C delay line and a digitally controlled tap selector switch. The tap selector switch allows the receiver channels to be switched into any tap providing a programmable time delay. The outputs of the delay lines are summed, IF filtered and then envelope detected before going to the analog to digital converter. Appendix A demonstrates the mathematical approach to the phased/delay line concept.

The beamformer described has already been developed[7], the current design problem is to develop a subsystem capable of providing the delay "coefficients".

The delay coefficients are used to control the phase of the local oscillator and the tap selector such that coherent beam focusing and steering are performed.

RAM vs ROM

The current ultrasound system retrieves the required time delay coefficients from ROM. The system has only 61 different scan lines* with 12 receiver focal zones used during dynamic focusing. Two transducer frequencies, 2.5 MHz and 3.5 MHz, are currently used, each of which requires a unique set of delay coefficients due to the frequency dependence of the delay calculation.

The new ultrasound system will have 121 different scan lines* with 21 receiver focal zones in order to provide improved image resolution. This increase in focal points requires greater than a 3 fold increase in coefficient storage space and due to critical power supply and PC board space limitations, this increase would be difficult to achieve using a ROM based delay coefficient system.

In addition to providing an increased number of scan lines and focal zones, the image resolution can also be improved in specific regions of tissue by generating a custom set of transmitter coefficients focused at the specific depth of interest. Resolution in the region of interest can also be improved by selecting the receiver coefficients such that they are focused in the compressed region of interest rather than being evenly spaced over the entire scan line. Custom coefficient tailoring such

as this could provide image resolution unmatched by any ROM based coefficient system.

The new system will also use a greater variety of transducer frequencies, thereby allowing the user to better optimize the resolution/penetration depth trade-off discussed earlier. Because a complete set of delay coefficients are required for each transducer frequency, the addition of 5.0 MHz and 7.5 MHZ transducers would double the already increased coefficient storage requirement, making a ROM based coefficient system totally unfeasible.

Doppler shift detection will also be incorporated into the new ultrasound system to allow the user to monitor the patients blood flow[6]. In Doppler mode, the system will transmit a sound pulse which is focused at the point of interest. The system will then detect the resulting frequency shift of the echo returning from the specified point. The Doppler subsystem therefore requires that a customized set of transmit and receive coefficients be generated in order to optimize the resolution at the gate location.

The new features led to the design of a micro-processor/RAM based coefficient generating system that is capable of custom calculating the delay coefficients and is able to do so in an acceptable amount of time.

* Note- In practice, the coefficients required for scan lines at negative angles are identical to the coefficients required for scan lines at positive angles if the transducer leads are reversed. Therefore, a system with coefficients for either 61 or 121 different scan lines can actually image with either 121 or 241 scan lines (respectively) if during negative scan angles, the transducer leads are effectively reversed.

Delay Coefficient Calculation

A dedicated microprocessor (MC68000L8) is used to calculate the delay coefficients required to focus and steer the ultrasound beam. After being calculated, the delay coefficients are stored in RAM from which they will be transferred to the local oscillator phase control registers and the tapped delay selector registers by the data sequencer.

Maximally, there are 121 different scan lines (high resolution mode) in the 90 degree sector image. Each scan line has 1 transmit focal zone and 21 receiver focal zones used during the dynamic focusing. Since there are 64 transducer delay elements, the total number of delay times to be determined are:

121 lines * 22 focal zones * 64 elements = 170368

The calculation required to determine the delay times is derived in appendix B. The delay coefficients are calculated each time the ultrasound scanner is powered-up. The coefficients are also recalculated whenever the transducer frequency is changed while optimizing the trade-off between the system resolution and penetration depth. Because of the calculation complexity and the large number of delay coefficients needed, a relatively long period of time is required to complete the calculations as shown in appendix C. This

calculation time is unacceptable, therefore an alternate approach utilizing recursion (see appendix D) had to be developed which required less calculation time as shown in appendix E. A flowchart for the recursive algorithm is given in appendix F.

Once the required time delays are determined by the recursive algorithm, the delays are then converted into the proper tap and phase settings which will yield the desired delays.

Microprocessor Overview

The Motorola MC68000 microprocessor was employed to calculate the delay coefficients because of its high execution speeds and powerful instruction set. The MC68000L8 is a 16-bit microprocessor which uses an 8 MHz single phase clock and resides in a 64 pin DIP. The processor has 14 addressing modes and its internal 32-bit register structure includes 8 data, 7 address and 2 stack registers. Data operations may be performed in byte (8-bit), word (16-bit), or long word (32-bit) modes. Variations in the 56 instruction types can provide over 1000 useful instructions. Included in table 1 are several sample execution times which demonstrate the 68000's high speed[11].

Table 1- Sample MC68000L8 Execution Times

Operation		Execution Time
16-bit addition	(reg-to-reg)	0.5 us
16-bit memory access	(mem-to-reg)	1.0 us
program control jump		1.0 us
16-bit x 16-bit multiplication		8.8 us
32-bit / 16-bit division		19.8 us

Coefficient Card Description

A detailed block diagram of the MC68000 microprocessor circuit is provided in figure 4. The microprocessor is a slave to the ultrasound system's central processor (CPU). On receiving a prioritized interrupt from the main CPU, the 68000 will load the appropriate command information from the CPU controlled data latch. The 68000 can also send information back to the CPU via another data latch which is read by the CPU. The CPU indirectly controls various system status and control lines by directing the 68000 to output the proper signals to the control line data latch. The 68000 microprocessor is running at maximum speed since the data control lines are fed through a timer back to the data acknowledge (DTACK) pin.

Lines from the CPU control the delay coefficient outflow via the data strobe and the coefficient sequencer. The data strobe is a timer which notifies the receiving registers when valid coefficients are on the coefficient data bus. The sequencer causes the coefficients to be outputted from the dynamic RAM at the proper time and in the correct sequence. The sequencer also controls which phase and delay tap registers will be receiving the outgoing delay coefficients.

The dynamic RAM controller is a relatively complex

timing and switching circuit. The controller allows the microprocessor to read and write to the dynamic RAM. It also allows the coefficient sequencer to read the coefficients from RAM at a high rate of speed when the 68000 isn't accessing the RAM. It also refreshes the dynamic RAM when neither the 68000 nor the sequencer are accessing the RAM.

During the digital signature analysis (DSA) test*, the data buffers are disabled, only ROM can be selected by the address decoder and a valid "dummy" instruction is asserted onto the data bus. The microprocessor will continuously fetch the dummy instruction and hence will cycle through all addresses, causing unique signals to appear on various lines when the processor is functioning properly.

* Note: The DSA test is a simple test that can be performed by field service technicians. The DSA test puts the system into a repetitive cycle, thus generating known, repeating signal patterns. A system fault may be detected by checking various nodes for known signal patterns. Unexpected signal patterns can be traced back to the source, thereby identifying the fault.

Microprocessor Core Description

The microprocessor core circuit diagram is shown in figure 5. The 68000 data bus is buffered by 74LS245's (U52,75) and A1-A16 of the address bus are buffered by 74LS244's (U98,101). Address lines A17-A21 are used by the 74LS138's (U77,100) for address block decoding.

The 2764 ROMs (U102,103) and the 6116 RAMs (U104-107) are configured in a standard 16-bit memory configuration. The Write Upper (NWU) and Write Lower (NWL) signals are generated by ORing (U50b,d) the Upper Data Strobe (UDS) and the Lower Data Strobe (LDS) with the Write Enable (NWE). These signals allow either the upper data byte, the lower data byte or both upper and lower data bytes to be written to by the microprocessor. The Output Enable (OE) signal for the memory is generated by ANDing (U55a) the Address Strobe (AS) with the Write Enable (NWE) and then delaying the signal one clock period with a 74LS175 (U78) to insure that the Chip Enable (NCE) and Output Enable (NOE) pins are not simultaneously applied to the memory chips to guarantee stability.

The DSA test is performed when the DSA switch (S1) is closed. Closing the switch causes the DSATEST signal to go high which disables the data buffers (U52,75) and disables one of the address decoders (U77). It also

pulls UDO, UD8 and UD15 to ground through diodes D1, D2 and D3 while the other data lines are pulled to logical ones by resistor blocks R12 and R13. This in effect puts the machine code for the Move Quick (MOVEQ) instruction on the data bus which allows the DSA test to be performed as previously described.

The asynchronous bus cycle is terminated when the Data Acknowledge (DTACK) signal is asserted. This signal is asserted automatically after two clock periods by the 74LS175 (U78) and allows the 68000 to run at its maximum speed. The bus cycle can be slowed down by one clock period to allow for slow memory devices by moving the jumper from W2 to W1.

The prioritized interrupt from the main CPU is clocked into the 74LS175 (U79) when the CPU Read (MR/NW) and the Register 4 Enable (REG4) signals are asserted by the main CPU. The interrupt is then synchronized with the 68000's Master Clock (MC) by the 74S175 (U74) before being applied to the microprocessor. After recognizing the interrupt, the 68000 asserts the Interrupt Acknowledge code (111) on FC0-FC2. These signals are NANDed (U59a) to form the Interrupt Acknowledge (NIA) signal. The Interrupt Acknowledge is then ORed (U50c) with the Address Strobe (NAS) and applied to the VPA pin which forces the 68000 into the auto-vector interrupt

mode. After servicing the interrupt, the 68000 can clear the interrupt register (U79) by asserting the Interrupt Clear signal (NCE15).

The 68000 microprocessor may be reset by one of three methods. A reset is performed when both the HALT and the RESET pins are pulled low for greater than 100 ms. A reset is done on power-up by D1, C1 and R6 and can also be done by manually closing the RESET switch. The main CPU may also reset the 68000 by asserting the NRESET COEFF signal.

The main CPU can transfer data to the 68000 by writing to the 74LS374's (U57,76). After the main CPU puts valid data on DO-D15, it then asserts the CPU Write (MR/NW) and the Register 5 Enable (REG5) signals which clock the data into the register. Writing to the register also clocks the flag register (U80b) which sets the NDATA REC signal high and notifies the 68000 that new data is present in the register. After the 68000 reads the data register by asserting the Chip Enable (NCE6) signal, the NDATA REC flag is cleared.

Similar to how the 68000 receives information from the main CPU, the 68000 may also send data back to the main CPU by writing to another 74LS374 register (U54). Data is clocked into the register when the Chip Enable (NCE6) is asserted during the write cycle. In addition

to reading from the data register, the main CPU may also read various status lines through the 74LS244 (U53) by asserting the Register 4 Enable (REG4) signal during the read cycle. Likewise, the 68000 may read various status lines through U53 by asserting the Chip Enable (NCE7) signal during the read cycle.

Coefficient Sequencer

The circuit diagram for the coefficient sequencer is given in figure 6. The sequencer is controlled by the LOAD SCAN (LDSC') and LOAD FOCUS (LDF') signals from the main CPU. The LOAD SCAN pulse causes the sequencer to send out the transmitter delay coefficients for the current scan line. The initial pulse on the LOAD FOCUS line causes the tapped delay line coefficients and the first set of phase delay coefficients to be sent out to the receivers. Each successive LOAD FOCUS pulse causes a new set of phase delay coefficients to be sent to the receivers which update the focal point to progressively deeper locations, hence tracking the sound wave and supporting the dynamic focusing (see figure 7).

The LOAD SCAN pulse sets the Transmit flag (NXMIT) and the Sequencer Enable flag (SEQ EN) by clearing the respective 74LS74's (U85a,60a). In addition, the LOAD SCAN pulse also clears the sequence counters (U40,64,65) and the Burst Clock (BCLK) registers (U84a,b). Likewise, a LOAD FOCUS pulse also sets the Sequencer Enable flag (SEQ EN) in addition to clearing the Transmit (NXMIT) flag.

When the Sequencer Enable (SEQ EN) flag is set, the sequence counters, the Burst Clock and the Address Decoder ROM (U16) are enabled. Each successive pulse on

the MC/2 line causes a BCLK signal to be sent after a one clock period delay (U84a,b). Each MC/2 pulse will also advance the sequence counter. The sequence counters are connected in series (utilizing look-ahead carry) in order to provide a 10-bit synchronous count (MA15=Low order bit). The sequence counter output is decoded by the TBP28L22 (U16) high speed ROM and the 74LS86 XOR gates (U66a,b,c) into the appropriate coefficient register address. The register address is latched and delayed for one clock period by the 74LS174's (U19,43,61,62) before being transferred to the register address bus (SEQ4-SEQ15). The delay in the Burst Clock and the sequencer address output is necessary in order to synchronize the Burst Clock and Coefficient Address with the Coefficient Data being outputted by the dynamic RAM because the dynamic RAM read cycle requires two full clock periods to be completed.

Once the SEQ EN flag is set, the sequencer will continually send out coefficients until the ROM decodes the address of the last coefficient to be sent. The high order (D7) bit of the ROM output is then used to clear the SEQ EN flag, thereby halting the sequencer. Proper timing in the sequencer circuit is maintained by U1 and U15a which generate the SYNC1 and SYNC2 signals that control the gating of U59b, U60 and U83b.

If the 68000 microprocessor wishes to access the dynamic RAM. it can disable the coefficient sequencer by writing a zero (BDO=0) to the Memory Enable (MEM ENB) flag (U60b) using NCE8. The 68000 can re-enable the sequencer by resetting (BDO=1) the MEM ENB flag. The MEM ENB line is used to gate U59b and U83b which control the counter clock and RAM Access (ACCESS) signals respectively.

Dynamic RAM

The dynamic RAM controller posed the most difficult design problem of the coefficient subsystem. Dynamic RAM was choosen over static RAM because of the lower cost, higher density and lower power requirement. The major disadvantages of dynamic RAM are its slow speed, complex timing signals and the need for refresh.

The RAM design had to insure that adequate RAM refreshing would be performed. When the 68000 is controlling the RAM, the system must provide software refreshing to prevent data loss. In the normal imaging mode, RAM locations are sequentially read out by the sequencer, and hence, refresh is guaranteed; however, in the "Doppler Only" mode of operation, the same Doppler line is repeatedly fired which increases the Doppler bandwidth[6]. It is during this mode, when no imaging is being done, that data can be lost, hence the design had to include hardware that would refresh the dynamic RAM during "free" access cycles.

Another major design consideration was the need for a fast RAM access cycle. During the dynamic focusing operation, the focal zones progressively "jump" from one depth to the next. Focal zone updating during these jumps must be done as rapidly as possible because the beam is out of focus until all coefficients are accepted

by the receiver registers. Therefore it is important to optimize the RAM access time in order to minimize the focal zone update time.

The dynamic RAM circuit diagram is shown in figure 8. The 4864A-12 RAMs (U108-115,117-124) are high speed, 64k x 1-bit dynamic RAM chips. The 74S151's (U89-96) select the proper address to be asserted on the RAM address bus. U89-96 choose between the refresh counter address, the sequencer address or the 68000 address buses and also select either the row address or the column address of the appropriate bus. Critical timing is maintained by a multi-tapped delay line (U28) which has ten outputs in 20 ns increments. The RAM controller can undergo any one of three cycles: A 68000 read/write, a coefficient sequencer read or an automatic refresh.

U74 of figure 6 is used to divide the Master Clock (MC) frequency by two in order to generate MC/2. MC/2 is then delayed 40 ns by U24b to generate MC/2' which is further delayed another 40 ns by U24a to generate MC/2''. The delayed signals insure that proper set-up times are met on U26b and U25a before being clocked.

Dynamic RAM access and refresh cycles are initiated when the START signal goes high. Referring to the timing diagrams in figures 9 and 10, the following is a description of the sequence of events which occur after

the START signal goes high:

1) START clocks U26a causing START' to go high.

2) START' begins propagating through the tapped delay line (U28).

3) After 40 ns, NRAS is clocked low by U29a. NRAS is the Row Address Select signal for the RAM.

4) After 60 ns, NCOL SEL is clocked low by U29b. NCOL SEL switches the output of U89-96 from row address to column address.

5) After 80 ns, NCAS' is clocked low by U30a which in turn clocks NCAS low if it has not been disabled by DIS CAS. NCAS is the Column Address signal for the RAM.

6) After 100 ns, the START' signal is reset low when U26a is cleared.

7) After 160 ns, NCOL SEL is switched from column back to row address when U29b is cleared.

8) After 180 ns, NRAS and NCAS' are reset high when U29a and U30a are cleared, thus terminating the RAM cycle. The RAM's output data is latched by U87 and U88 when CAS (U66a) goes low (i.e. NCAS' goes high).

The outputs of U87 and U88 are then asserted onto the coefficient data bus or may be read back onto the 68000 data bus through U86 and U116.

The RAM controller is under 68000 control when the 68000 sets both the NDISREFR (U81a) flag and the 68ACCESS (U25b) signal low. The RAM controller is under coefficient sequencer control when both the NDISREFR flag and the ACCESS (U83b) signal are set high. When the NDISREFR flag is set high and the ACCESS signal remains low, then an auto-refresh will be performed.

Dynamic RAM: Auto-Refresh

When neither the 68000 uP nor the coefficient sequencer are accessing the dynamic RAM (i.e. NDISREFR=high and ACCESS=low), automatic refreshing is performed to prevent data loss. Referring to the timing diagram in figure 9 and the circuit diagram in figure 8, the following events occur during the RAM refresh:

1) NDISREFR must be set high by the 68000 (U81a), otherwise the NREFR CLR signal generated by U55b will keep REFR (U26b) low, thus preventing a refresh from occurring. This provides a means for the 68000 to prevent the refresh when it wishes to access the RAM. If the refresh is disabled, the 68000 must provide software refreshing to avoid losing RAM data.

2) ACCESS is synchronized with MC/2 by the sequencer circuit. The 40 ns delay in MC/2' provides the sequencer with enough set-up time so that ACCESS can be set high and clocked into U25a if a RAM access is needed. If ACCESS remains low (i.e. the sequencer does not need a RAM access), then SEQ ACCESS will be clocked low by MC/2' which enables a refresh to be performed.

3) REFR is set high if MC/2'' clocks START through U26b while START is low. START will only be low if both SEQ ACCESS and 68ACCESS are low, which occurs when neither the sequencer nor the 68000 are accessing the RAM. REFR is reset low by NREFR CLR (U55b) during the second half of the refresh cycle when MC/2' goes low.

4) The low-to-high transition of REFR sets DIS CAS (U30b) high. When DIS CAS is high, both CAS and NCAS are disabled which is necessary for a RAM refresh. DIS CAS also propagate through U27d and U32a which causes U89-96 to select the refresh counter (C0-C7) as the RAM address (S0=high and S1=high). DIS CAS remains high until either SEQ ACCESS or 68ACCESS goes high which clears U30b via U39d.

5) The low-to-high transition of REFR also causes START to go high via U27b. The low-to-high transition of START initiates the memory cycle as previously described.

6) When REFR is reset low by NREFR CLR, the refresh counter (U56) is incremented to the next RAM location.

Therefore, the overall strategy of the auto-refresh circuit is to refresh consecutive RAM locations each time that a "free" MC/2 cycle occurs. If the refresh circuit is disabled, then either the 68000 must provide software refreshing or the sequencer must access consecutive RAM locations to insure complete refresh.

Dynamic RAM: Sequencer Access

The 68000 can enable or disable the coefficient sequencer by setting or clearing the MEM ENB (U60b) flag. With the sequencer enabled, the coefficient read cycle is started by setting ACCESS high after the coefficient address is asserted. A timing diagram for the sequencer access is given in figure 10.

ACCESS is gated through U55c along with NXMIT. If the coefficients are transmitter coefficients (i.e. NXMIT=low), then the output of U55c will be low which causes U89-96 to select the transmitter coefficient address (S0=low and S1=low). If NXMIT is high, then the output of U55c will also be high which will select the

receiver coefficient address (SO=high and S1=low).

ACCESS is clocked through U25a by MC/2' which will set SEQ ACCESS high. SEQ ACCESS then propagates through U27a and U27b causing START to go high, thereby initiating the RAM access cycle as previously discussed.

START will reach the input of U26b before MC/2'' goes high because of the 40 ns delay (U24a). This keeps REFR from being clocked high, thus preventing a refresh cycle from occurring.

Dynamic RAM: 68000 Access

When the 68000 wants to access the dynamic RAM, it must first disable the refresh circuit by setting NDISREFR (U81a) low and disable the sequencer by setting MEM ENB (U60b) low. The 68000 then sets 68ACCESS (U25b) high by pulling the Chip Enable (NCE3) low.

68ACCESS propagates through U27d causing the 68000 address bus (BA1-BA16) to be selected (SO=low and S1=high) by U89-96. 68ACCESS also propagates through U27a and U27b causing START to go high which initiates the RAM access cycle as previously described. As with the sequencer RAM access, START will also prevent a refresh from occurring. The RAM output data is asserted onto the 68000 data bus during memory read cycles by U86 and U116.

Afterthought

The dynamic RAM controller posed several difficult design problems. Dynamic RAM was used instead of static RAM because of the large data storage requirement and limited space availability, however dynamic RAM is inherently tricky to use because of stringent timing requirements. Unique system requirements such as high speed RAM access, automatic hardware refresh and multiple RAM users made the design problem even more difficult.

The use of the multi-tapped delay line (U28) introduced stability problems into the design because the device characteristics can change as parameters such as temperature vary. This problem is compounded by the narrow window of timing tolerance given by the RAM.

Reflecting back on the RAM controller design, a simpler design with better stability could have been employed. As shown in figure 11, a stable high frequency crystal oscillator could be used to provide an accurate timing reference. The oscillator in turn would then clock a high speed counter. The counter output could be decoded by a programmable logic array (PLA) which would generate the desired timing signals. This type of arrangement would generate the complex dynamic RAM control signals with a high degree of stability and accuracy while requiring a minimal amount of hardware.

Results

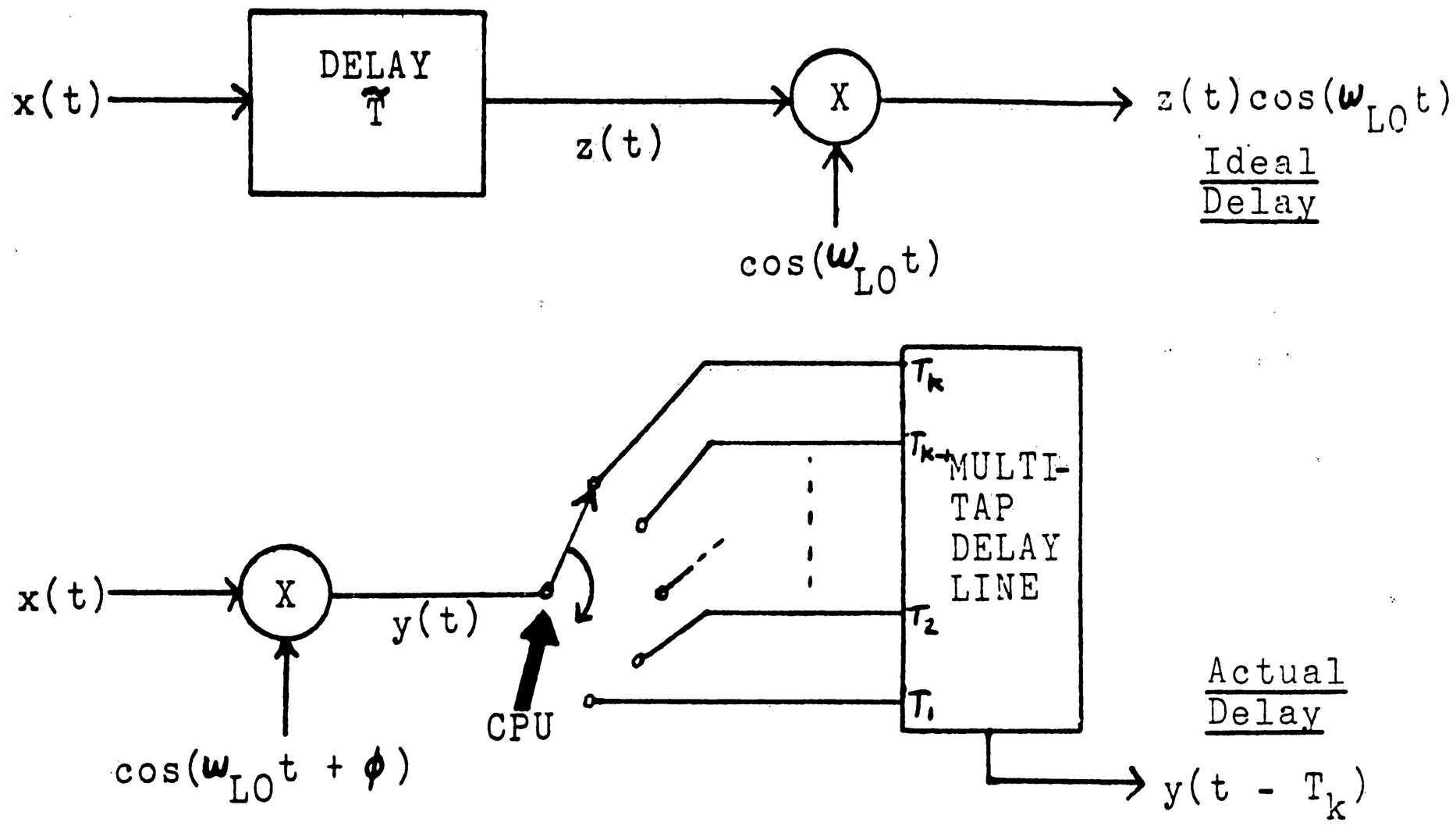
The design problem that was presented was to create a microprocessor system capable of generating the delay coefficients necessary to focus and steer the ultrasound beam electronically. High image resolution, low power availability and limited PC board space demanded a dense RAM configuration utilizing 64k dynamic RAM chips. The large number of focal points and the delay calculation complexity required the use of the fast and powerful MC68000L8 microprocessor in order to perform the calculations in an acceptable amount of time. The microprocessor based coefficient system also provided the flexibility required to custom tailor the delay coefficients to accommodate the Doppler subsystem and allow the use of a greater variety of transducer frequencies.

This paper has mostly analyzed the receiver operation in the phased array ultrasound. This is because the theory of the transmit function is really just the reciprocal of the receive function. Both beam focusing and steering of the transmit pulses are accomplished using the same type of phase delays as in the receive mode. In practice however, the transmitter delays are much easier to obtain than the receiver delays. Transmitter delays are accomplished by first

presetting a counter with the desired delay and then at time t=0, the counter is clocked down by a crystal oscillator. When a count of zero is reached, the transducer element on that particular channel is pulsed. This produces an accurate digital time delay while minimizing the amount of required hardware.

The MC68000L8 microprocessor based delay coefficient board was constructed on a six layer, 8"x14" printed circuit board. The microprocessor board requires less than 3.5 amperes of power supply current and the total parts cost is approximately $400.00. The microprocessor requires only 8 seconds to calculate the delay coefficients for 61 different scan lines and 16 seconds for 121 different scan lines (high resolution mode). The image consists of a 24 cm deep, 90 degree sector scan with a frame rate of 30 per second (15 per second in high resolution mode). The image quality is excellent with no observable image degradation over the previous ROM based imaging system.

Appendix A- Idealized Time Delay



In order to cause the actual delay line to function the same as the idealized delay line, the outputs of the systems above must be made equivalent. This is done as follows:

If $x(t) = \cos(w_{rf} * t)$

then $z(t) = \cos(w_{rf} * (t - \tilde{T}))$

$y(t) = \cos(w_{rf} * t) * \cos((w_{lo} * t) + \phi)$

therefore

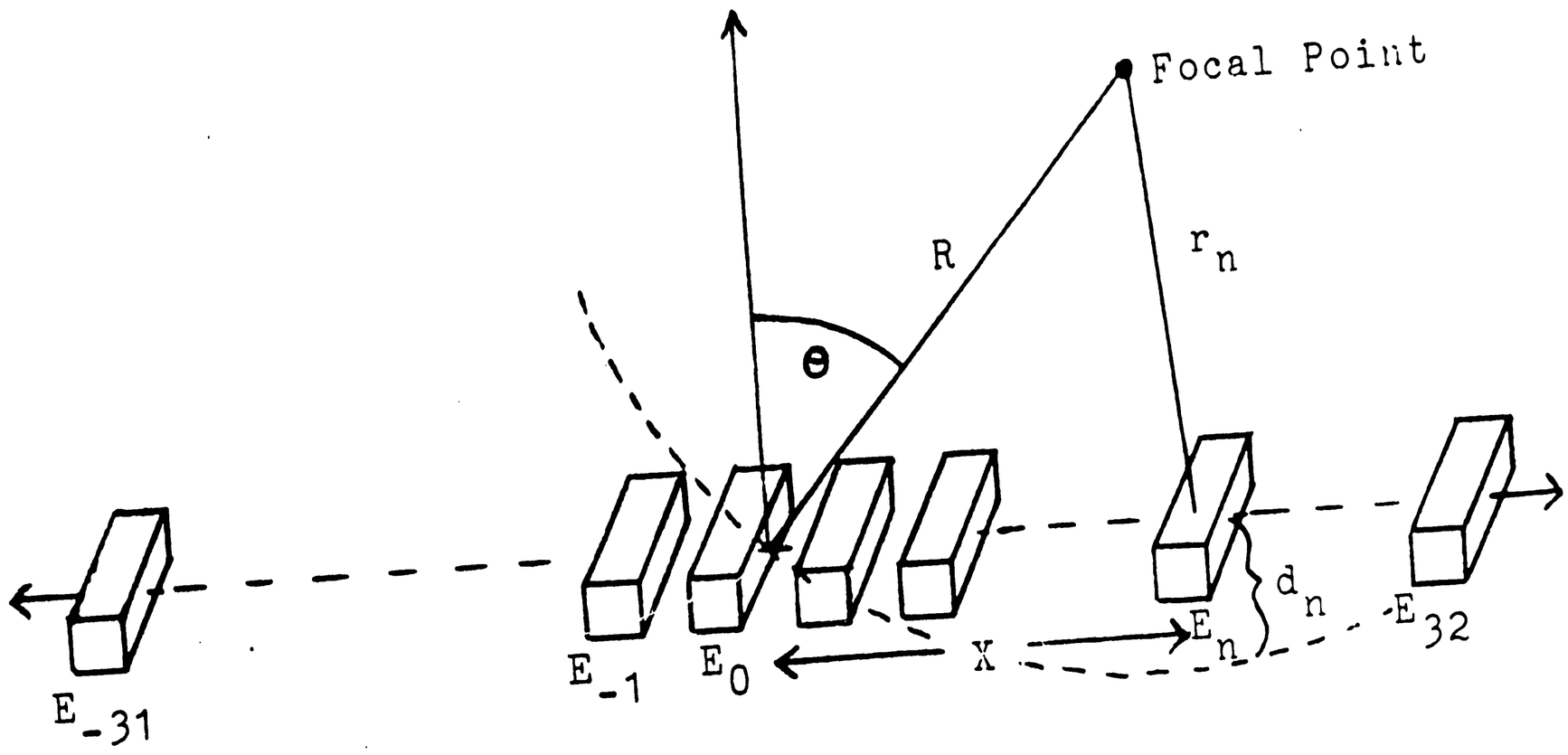
$z(t) * \cos(w_{lo} * t) = \cos(w_{lo} * t) * \cos(w_{rf} * (t - \tilde{T}))$

$y(t - T_k) = \cos(w_{rf} * (t - T_k)) * \cos(w_{lo} * (t - T_k) + \phi)$

Forcing these equations to be equivalent yields:

$$\phi = w_{rf} * (\tilde{T} - T_k) + w_{lo} * T_k$$

Appendix B- Time Delay Calculation



From the law of cosines:

$$r_n = \sqrt{R^2 + X^2 - (2 * R * X * \sin\theta)}$$

therefore the relative time delay is:

$$d_n = (R - r_n) / v \qquad \text{where: } v = \text{velocity of sound}$$

$$d_n = (R / v) * \left(1 - \sqrt{1 + (X^2 / R^2) - (2 * X / R * \sin\theta)}\right)$$

Using the 2nd order Taylor series approximation*:

$$\sqrt{1 + P} \approx 1 + (1/2 * P) - (1/8 * P^2) \qquad \text{(for small P)}$$

Let $P = (X^2 / R^2) - (2 * X / R * \sin\theta)$:

$$d_n \approx R/v * [1 - (1 + X^2/(2R^2) - X/R * \sin\theta - X^2/(2R^2) * \sin^2\theta + X^3/(2R^3) * \sin\theta - X^4/(8R^4))]$$

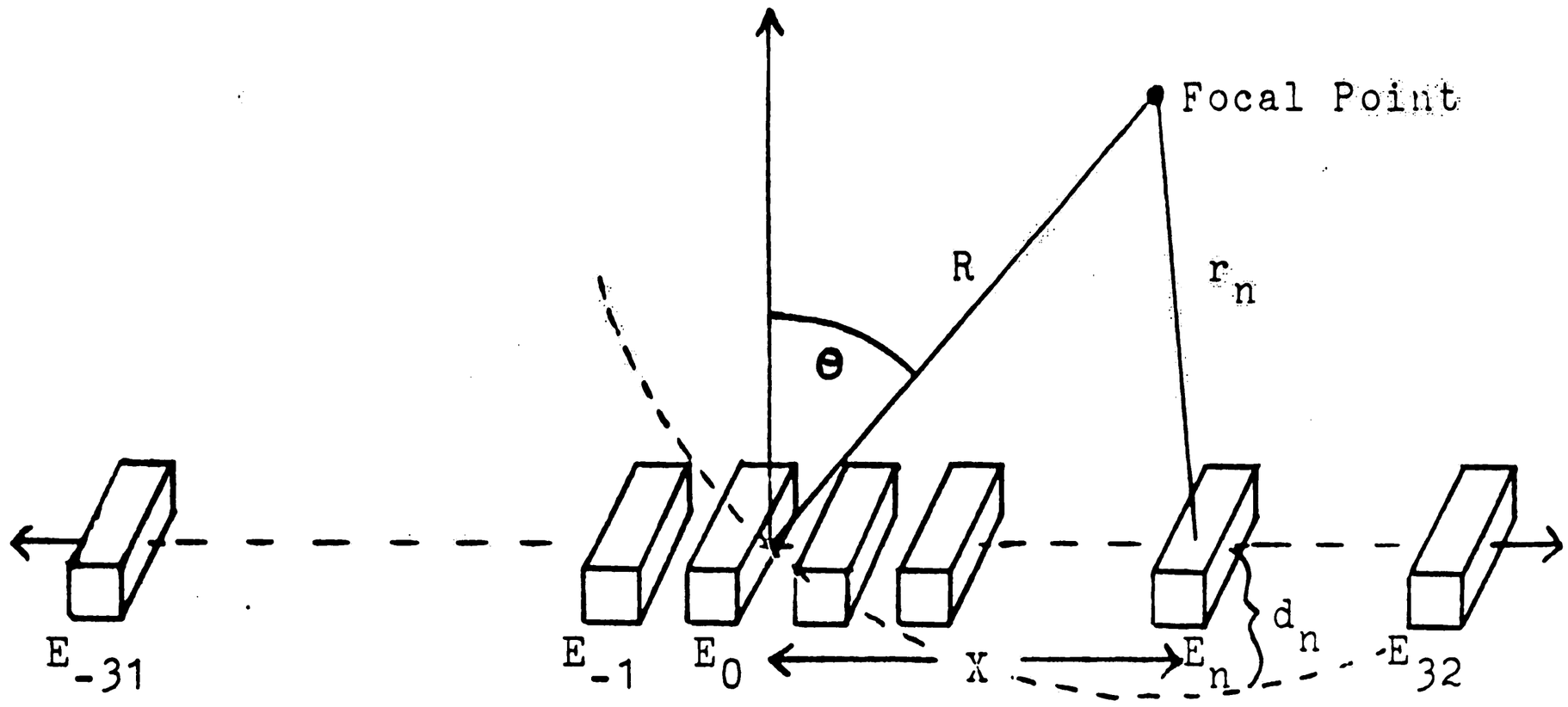
$$\boxed{\text{Delay}_n \approx X/v * \sin\theta - X^2/(2Rv) * \cos^2\theta - X^3/(2R^2v) * \sin\theta + X^4/(8R^3v)}$$

* Note: The 2nd order approximation has a substantial error associated with it, however due to computation time limitations, it is impractical to even consider the 3rd order approximation.

RETAKE

The Operator has Determined that the Previous Frame is Unacceptable and Has Refilmed the Page in the Next Frame.

Appendix B- Time Delay Calculation



From the law of cosines:

$$r_n = \sqrt{R^2 + X^2 - (2 * R * X * \text{Sin } \theta)}$$

therefore the relative time delay is:

$$d_n = (R - r_n) / v \qquad \text{where: } v = \text{velocity of sound}$$

$$d_n = (R / v) * (1 - \sqrt{1 + (X^2 / R^2) - (2 * X / R * \text{Sin } \theta)})$$

Using the 2nd order Taylor series approximation*:

$$\sqrt{1 + P} \approx 1 + (1/2 * P) - (1/8 * P^2) \qquad \text{(for small P)}$$

Let $P = (X^2 / R^2) - (2 * X / R * \text{Sin } \theta)$:

$$d_n \approx R/v*[1-(1+X^2/(2R^2)-X/R*\text{Sin}\theta-X^2/(2R^2)*\text{Sin}^2\theta+X^3/(2R^3)*\text{Sin}\theta-X^4/(8R^4))]$$

$$\boxed{\text{Delay}_n \approx X/v*\text{Sin}\theta-X^2/(2Rv)*\text{Cos}^2\theta-X^3/(2R^2v)*\text{Sin}\theta+X^4/(8R^3v)}$$

* Note: The 2nd order approximation has a substantial error associated with it, however due to computation time limitations, it is impractical to even consider the 3rd order approximation.

Appendix C- Computation Time

Time delay derived in appendix B:

$$d_n \approx X/v*\sin\theta - X^2/(2Rv)*\cos^2\theta - X^3/(2R^2v)*\sin\theta + X^4/(8R^3v)$$

In order to decrease the computation time, the following values can be tabulated in ROM:

$A_\theta = \sin\theta$		(121 values)
$B_\theta = \cos^2\theta$		(121 values)
$C = 1 / v$		(1 value)*
$D_R = 1 / (2*R*v)$		(22 values)
$E_R = 1 / (2*R^2*v)$		(22 values)
$F_R = 1 / (8*R^3*v)$		(22 values)

Therefore:

$$d_n \approx X*C*A_\theta - X^2*D_R*B_\theta - X^3*E_R*A + X^4*F_R$$

This calculation requires:

13 multilications @ 20 us** / multiply = 260 us

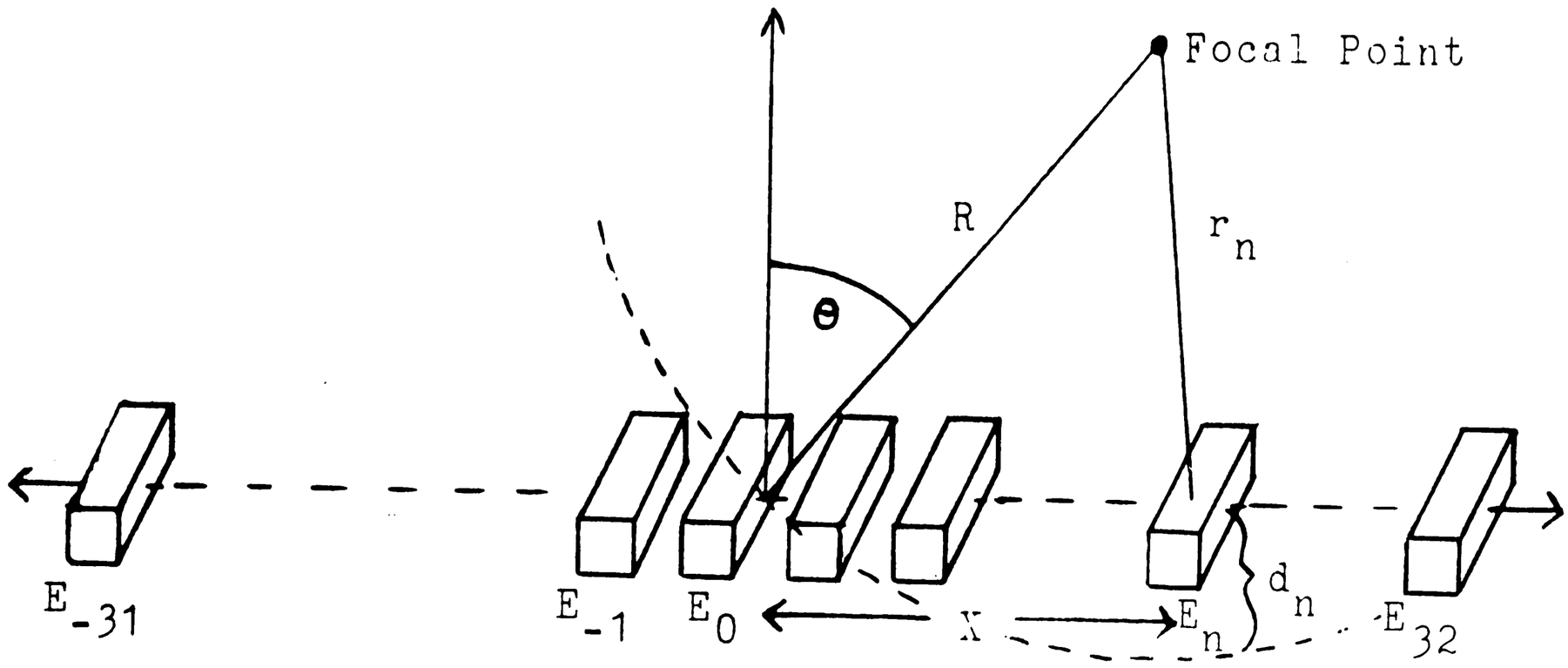
The total calculation time would then be:

170000 x 260 us ≈ 44 seconds

* Note- The sound velocity (v) is actually tissue dependent, however the variations from tissue to tissue are small, therefore it can be assumed to be constant. (1540 M/s)

** Approximation for MC68000L8 floating point multiply

Appendix D- Recursive Approximation



From the law of cosines:

$$r_n = \sqrt{R^2 + X^2 - (2 * R * X * \text{Sin } \theta)}$$

$$y(X) = r_n / v = 1/v * \sqrt{R^2 + X^2 - (2 * R * X * \text{Sin } \theta)}$$

= time from the n^{th} element to the focal point

The time from adjacent elements to the focal point is:

$$Y(X \pm \Delta X) = Y(X) \pm \frac{dY}{dX}\Delta X$$

$$= 1/v * \sqrt{R^2 + X^2 - (2*R*X*\text{Sin } \theta)} \pm \frac{1/v^2*(X-R*\text{Sin } \theta)}{1/v*\sqrt{R^2 + X^2 - (2*R*X*\text{Sin } \theta)}} \Delta X$$

$$= Y(X) \pm 1/Y(X) * (X/v^2 - R/v^2 * \text{Sin } \theta)\Delta X$$

If $X = (n - 1/2)\Delta X$, then:

$$Y(n \pm 1) = Y(n) \pm 1/Y(n) * [(n-1/2)\Delta X^2/v^2 - R\Delta X/v^2*\text{Sin } \theta]$$

Therefore the relative delay is:

$$d_{n\pm1} = R/v - Y(n \pm 1)$$

$$\boxed{d_{n\pm1} = R/v - Y(n) \pm 1/Y(n) * [(1/2-n)*\Delta X^2/v^2 + R*\Delta X/v^2*\text{Sin}\theta]}$$

for $-31 \leq n \leq 32$

Note- Use of the recursive approximation causes errors to accumulate for larger values of n, however a "fudge" factor was empirically determined which reduced the accumulated error to an acceptable value.

Appendix E- Recursive Computation Time

Time delay as derived in appendix D:

$$d_{n\pm1} = R/v - Y(n) \pm 1/Y(n) * [(1/2-n)*\Delta X^2/v^2 + R*\Delta X/v^2*\sin\theta]$$

In order to decrease the computation time, the following values can be tabulated in ROM:

$A_\theta = 1/v^2 * \sin\theta$ (121 values)

$B_R = R / v$ (22 values)

$C = \Delta X^2 / v^2$ (1 value/transducer frequency)*

$D_R = R * \Delta X$ (22 values/transducer frequency)*

Therefore:

$$d_{n\pm1} = B_R - Y(n) \mp 1/Y(n) * [(n-1/2)*C - D_R*A_\theta]$$

This calculation requires:

2 multiplications @ 20 us**/multiply

1 division @ 30 us**/division

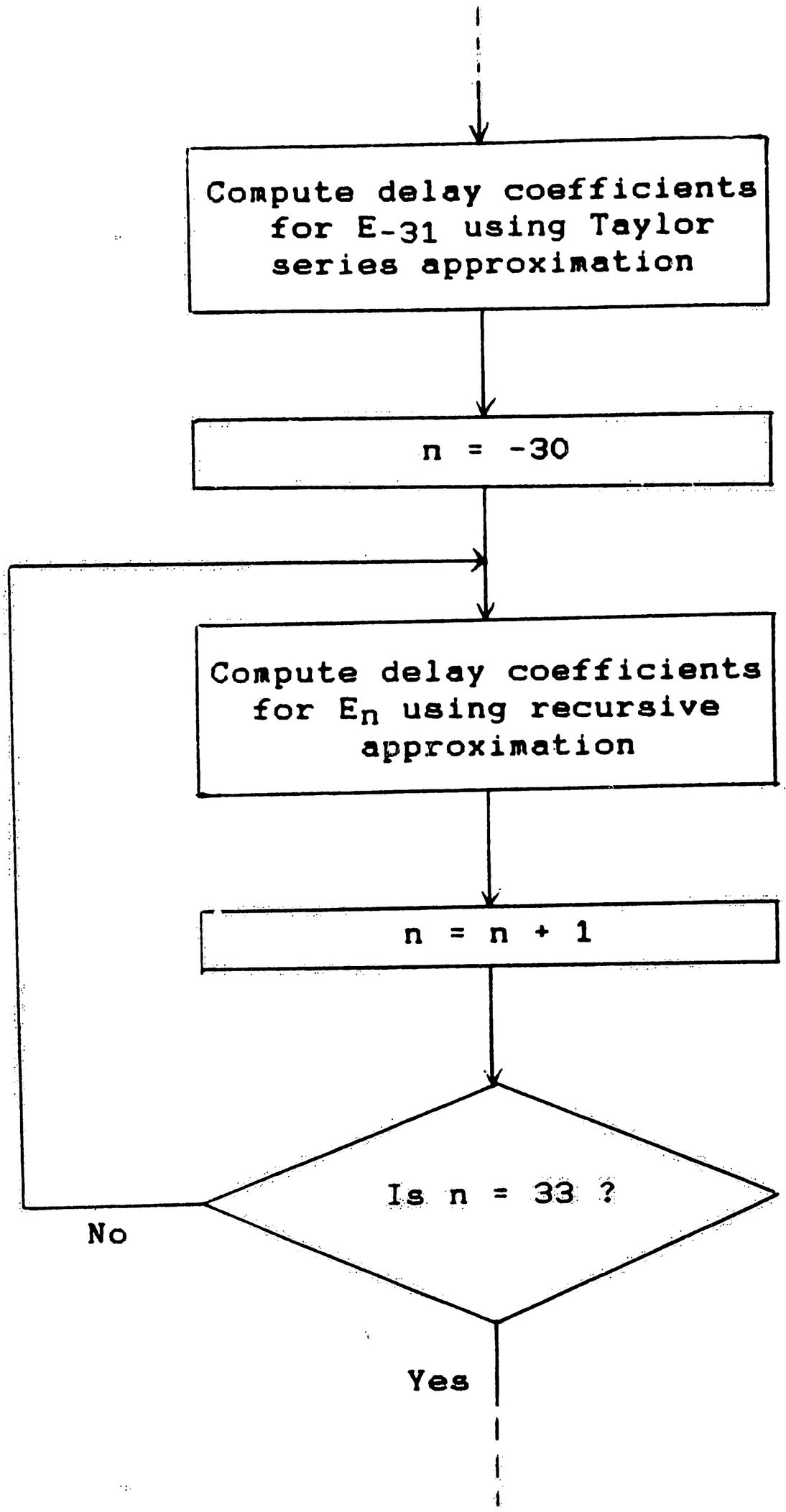
The total calculation time would be:

170000 x (40 + 30) us 12 seconds

* ΔX is dependent on the transducer frequency ($\Delta X = 1/2\lambda$)

** Approximation for MC68000L8 floating point arithmetic

Appendix F- Recursive Algorithm



The routine is repeated for each focal depth and angle.

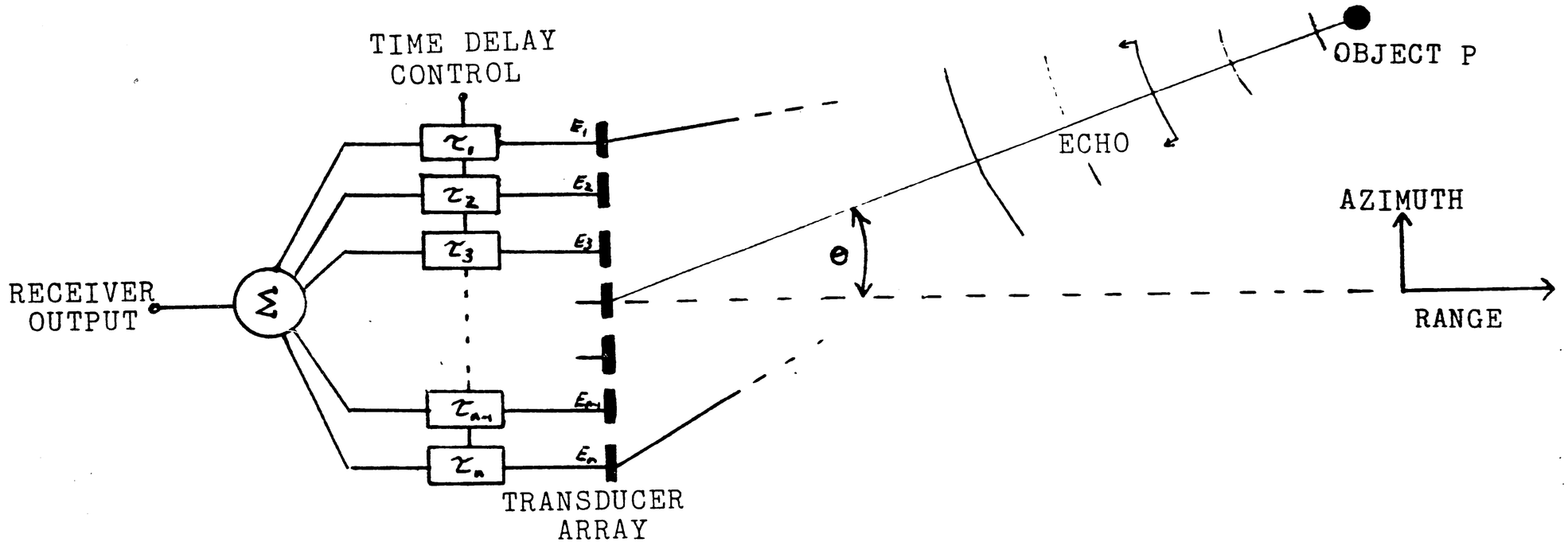


Figure 1: Phased Array Operation

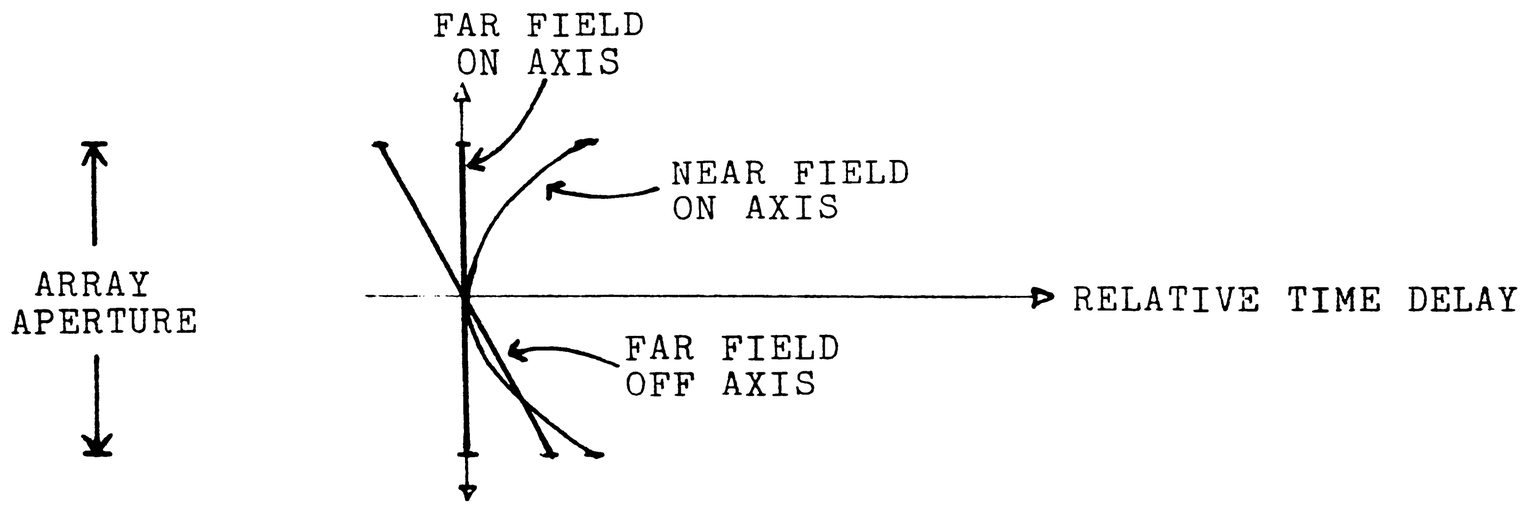


Figure 2: Phased Array Focusing and Steering

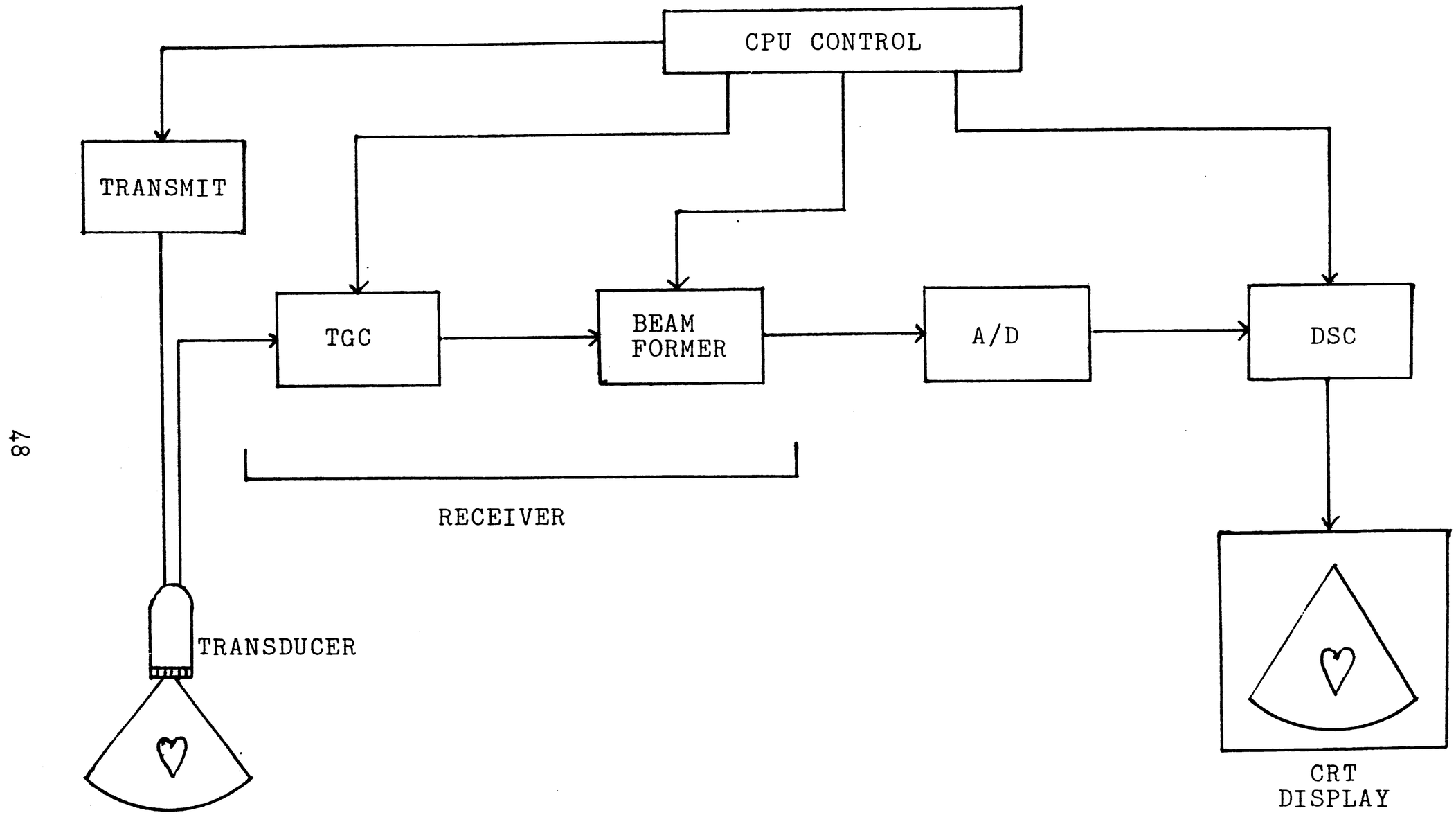


Figure 3: Ultrasound Imaging System Block Diagram

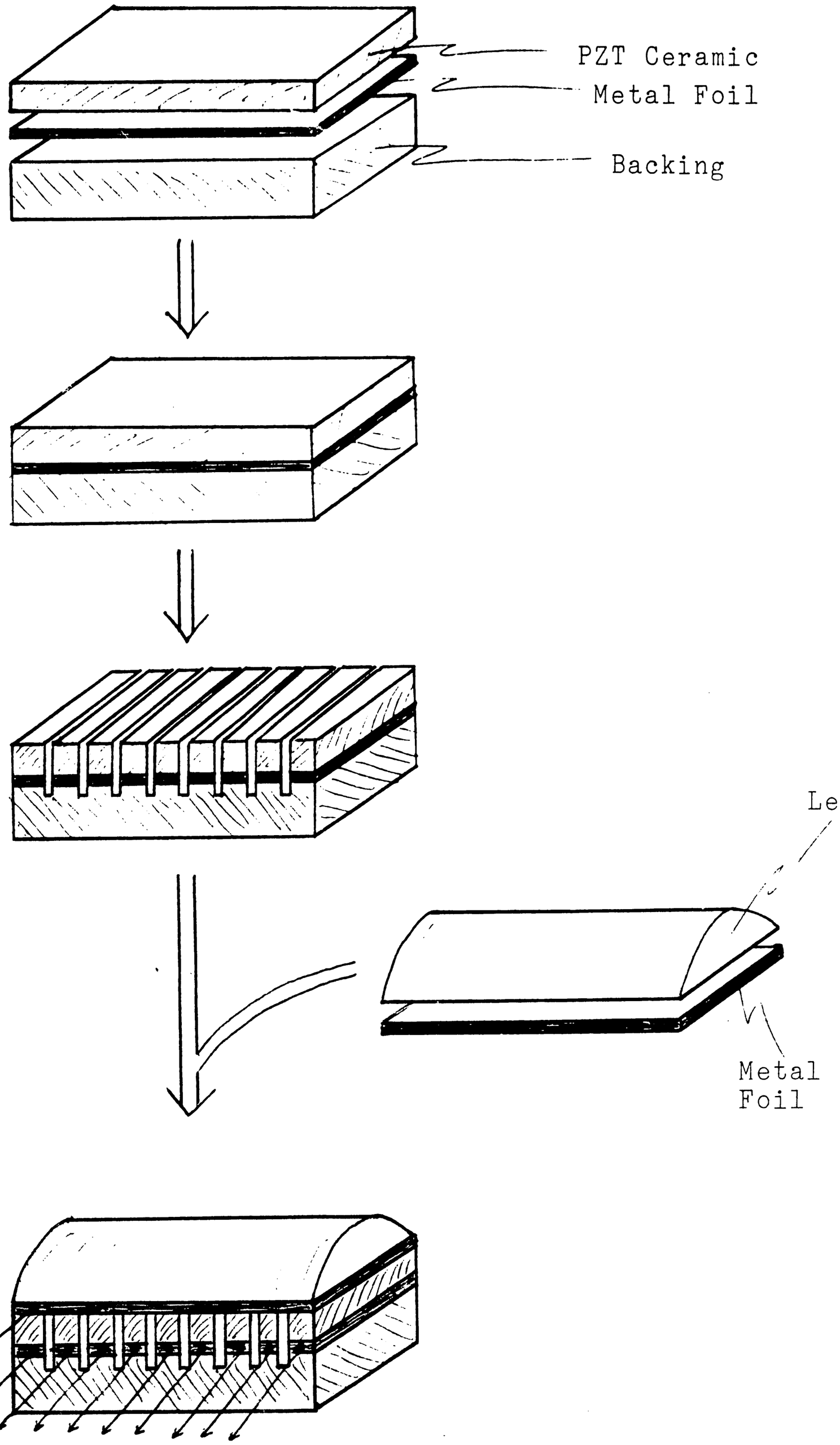


Figure 4: Transducer Design

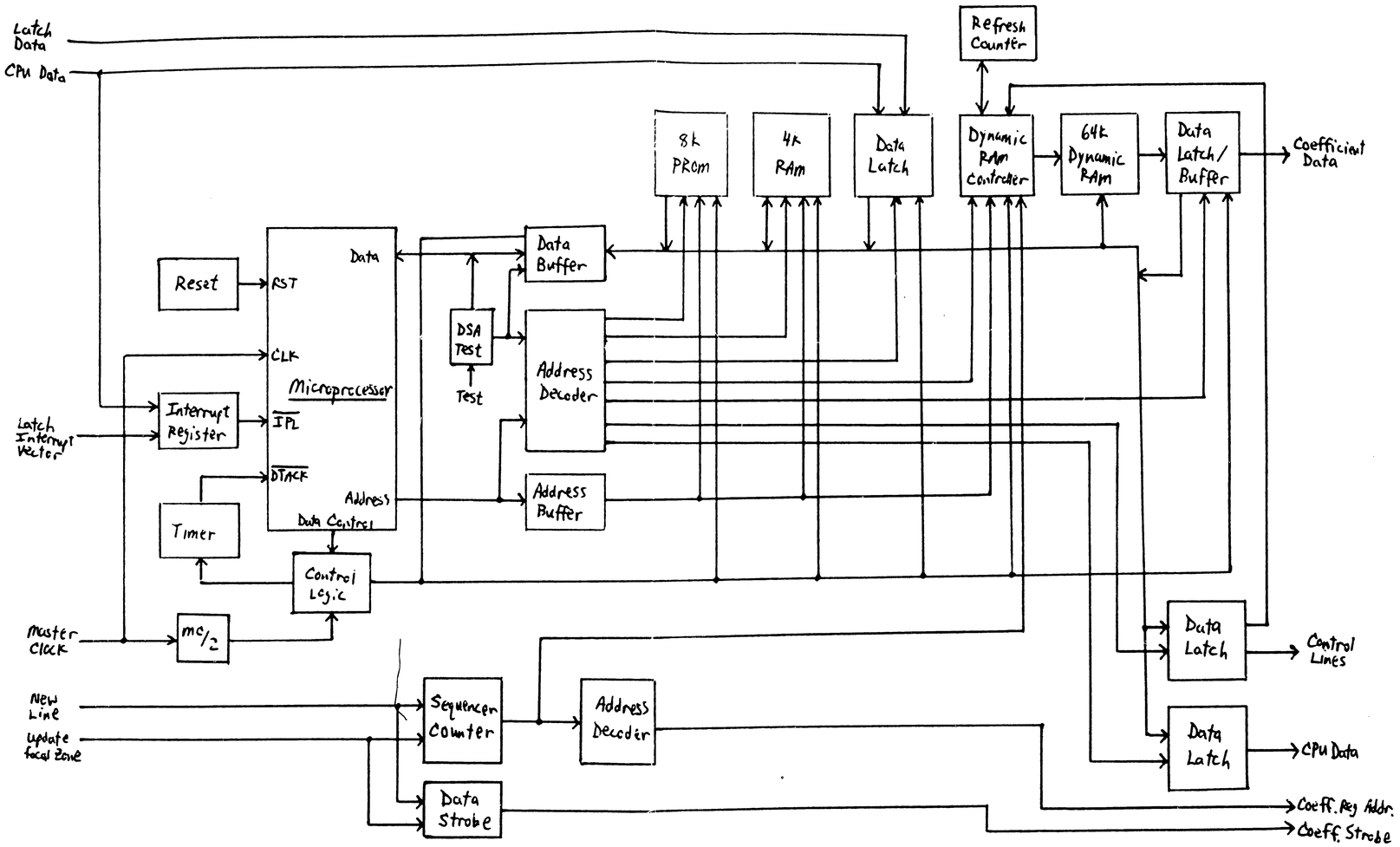


Figure 5: Coefficient Card Block Diagram

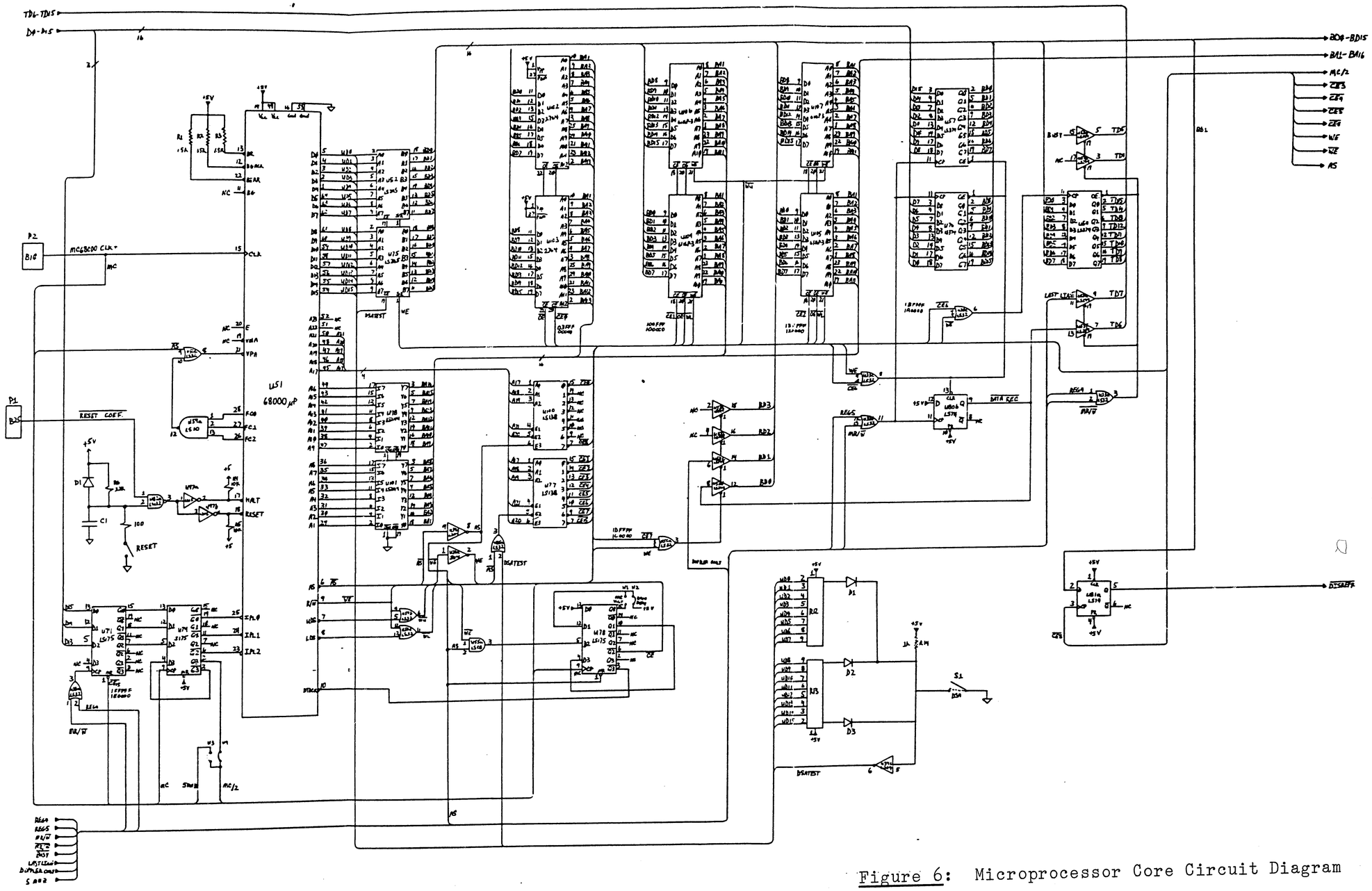


Figure 6: Microprocessor Core Circuit Diagram

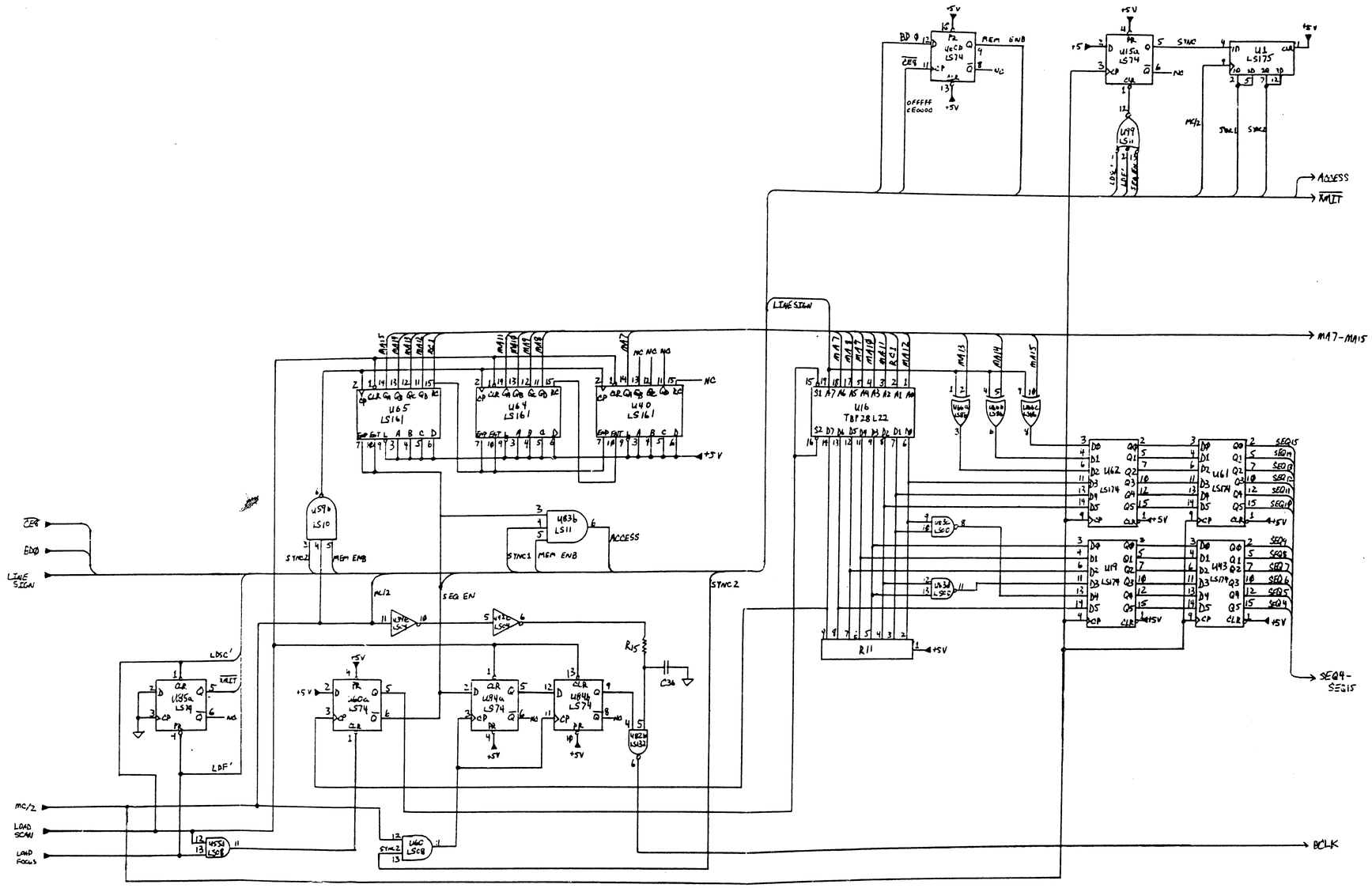


Figure 7: Coefficient Sequencer Circuit Diagram

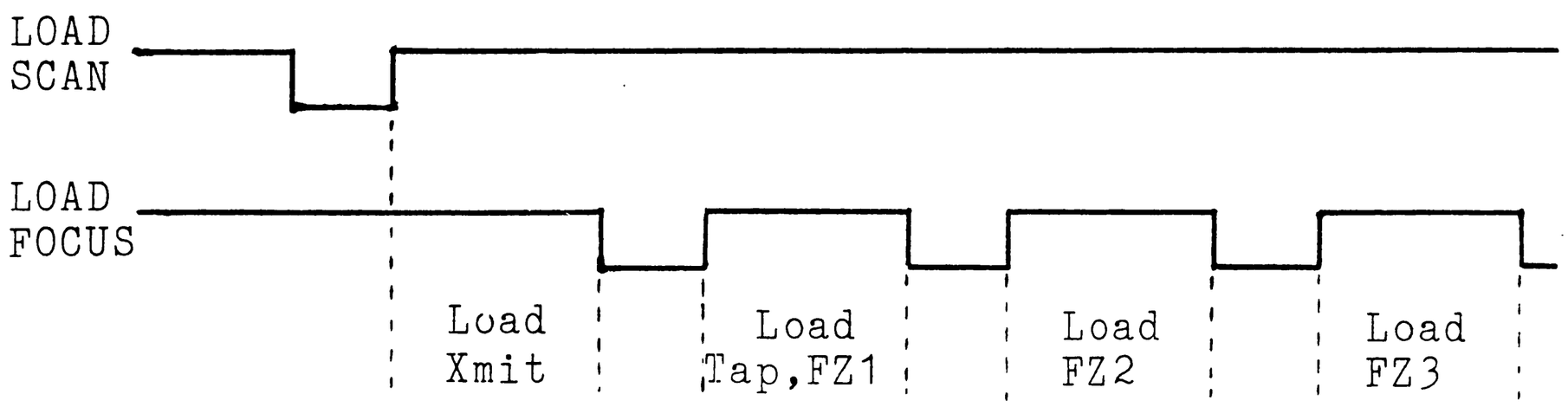


Figure 8: Sequencer Control Timing

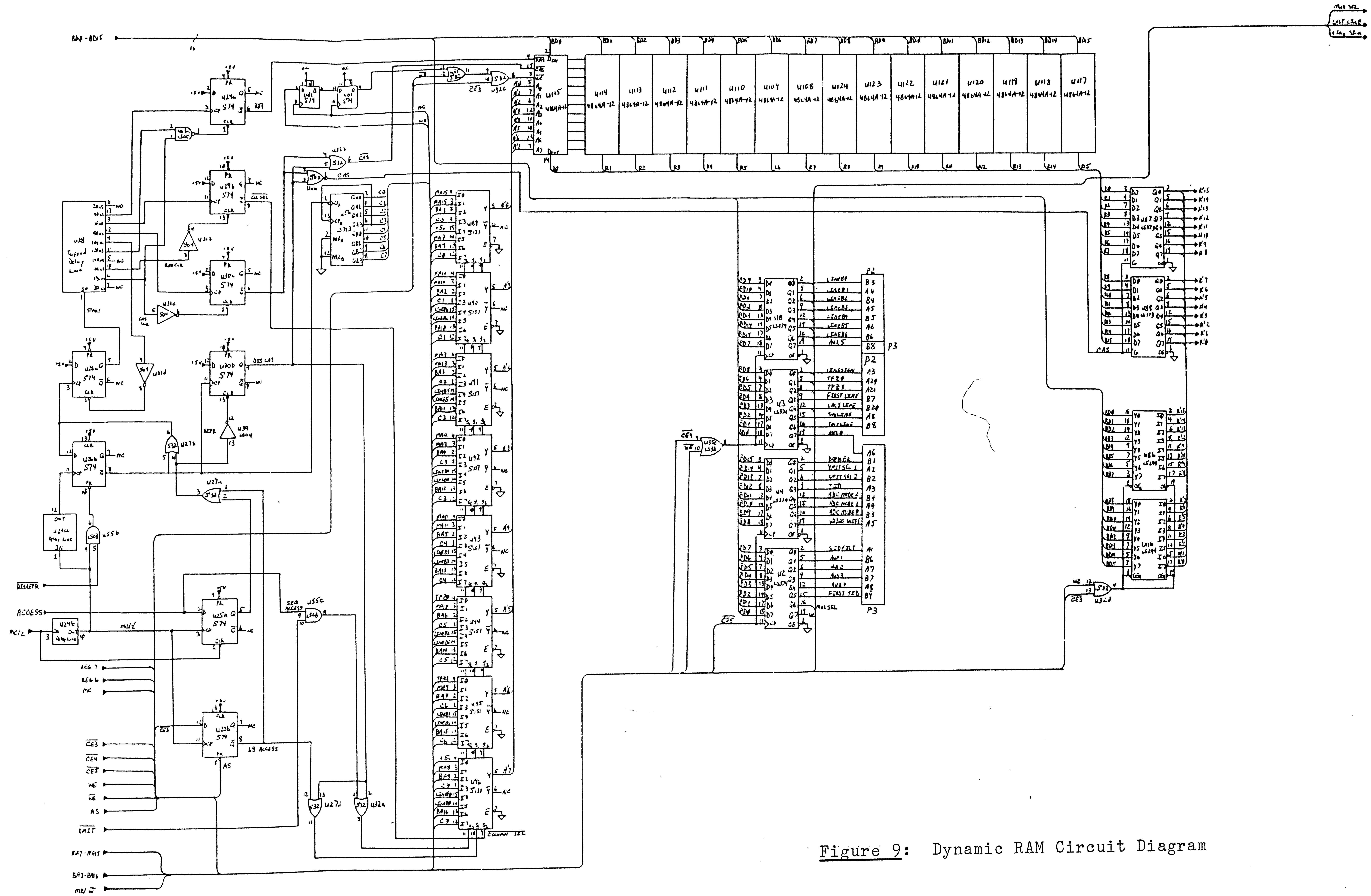


Figure 9: Dynamic RAM Circuit Diagram

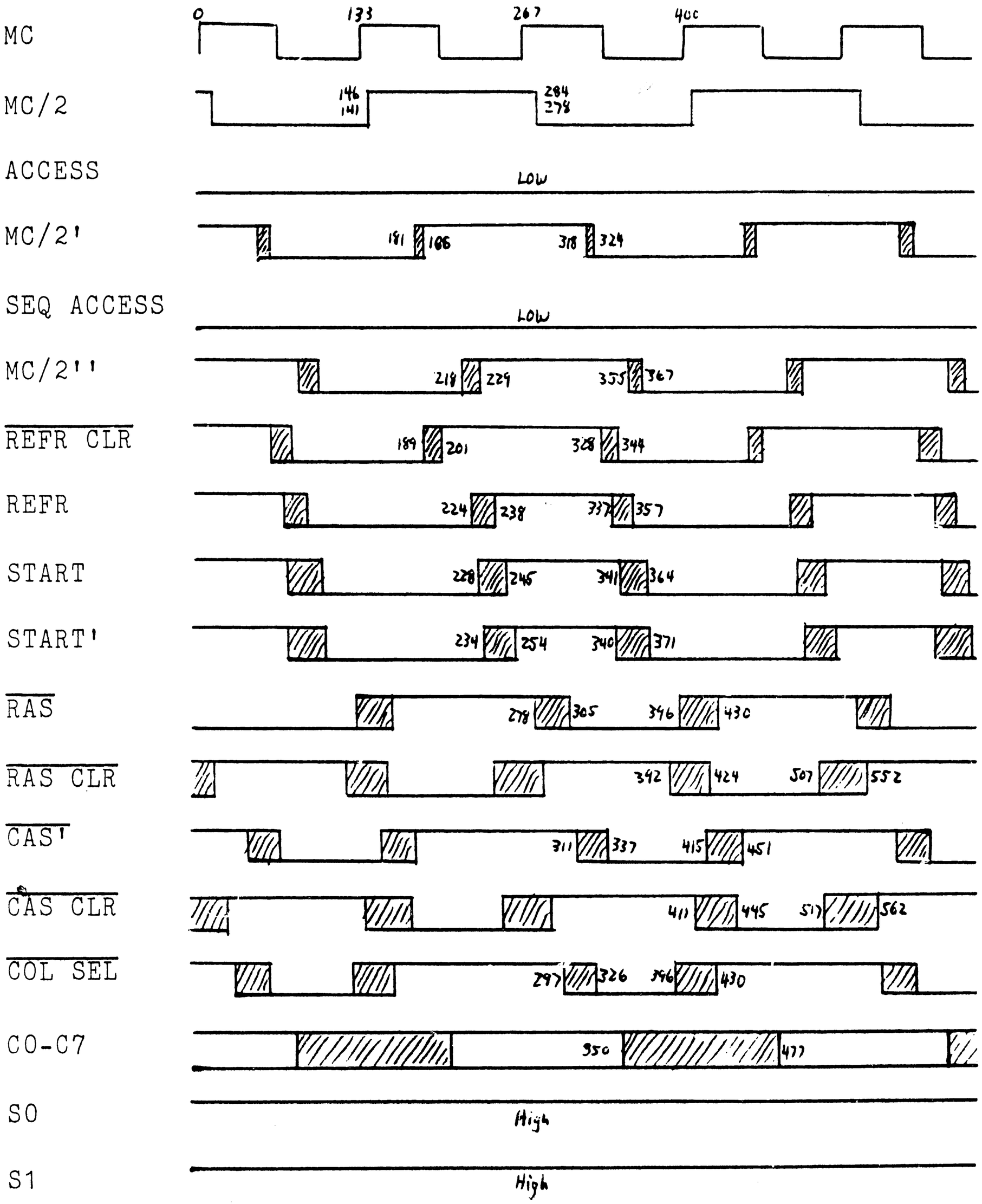


Figure 10: Timing Diagram for Dynamic RAM Refresh

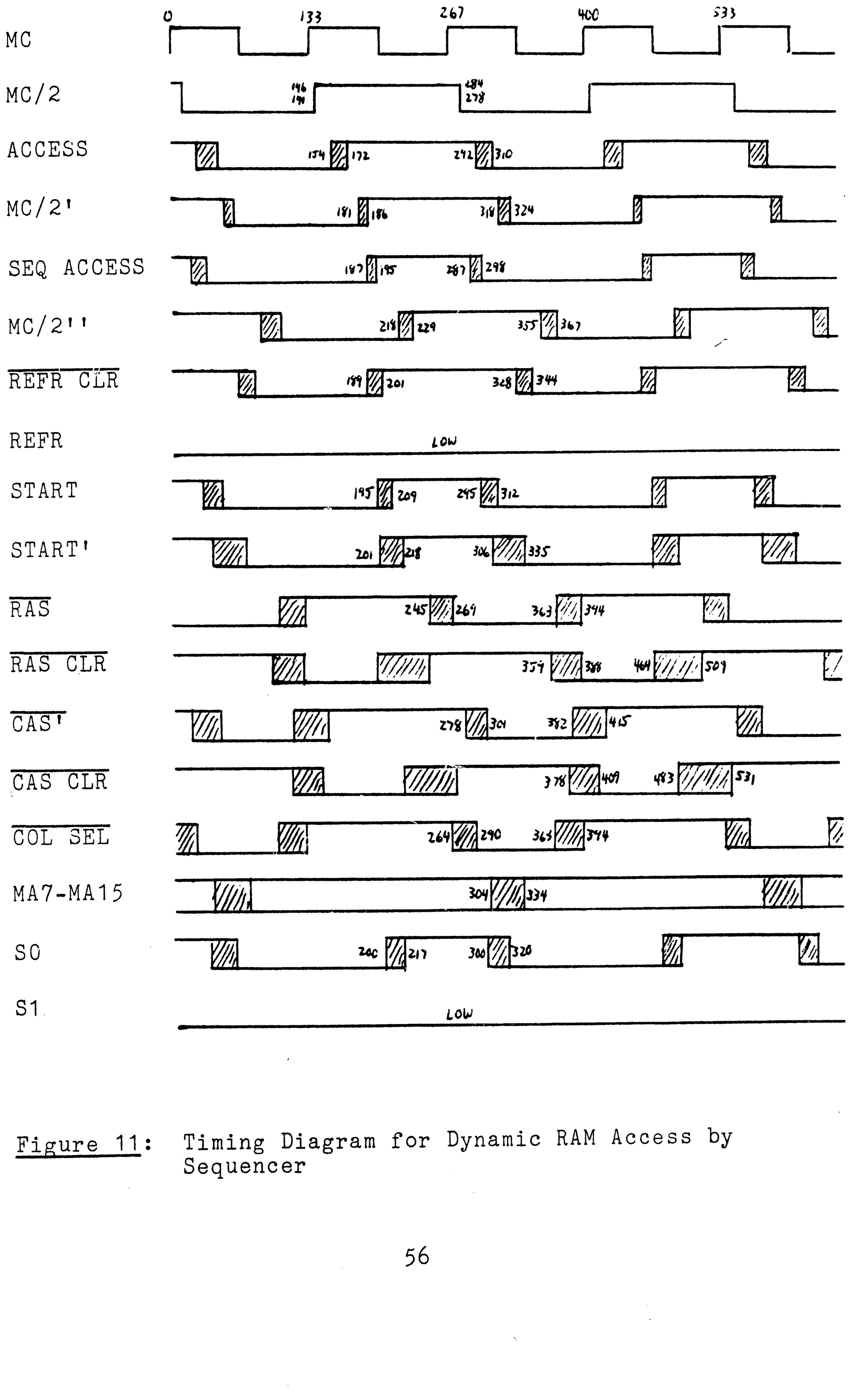


Figure 11: Timing Diagram for Dynamic RAM Access by Sequencer

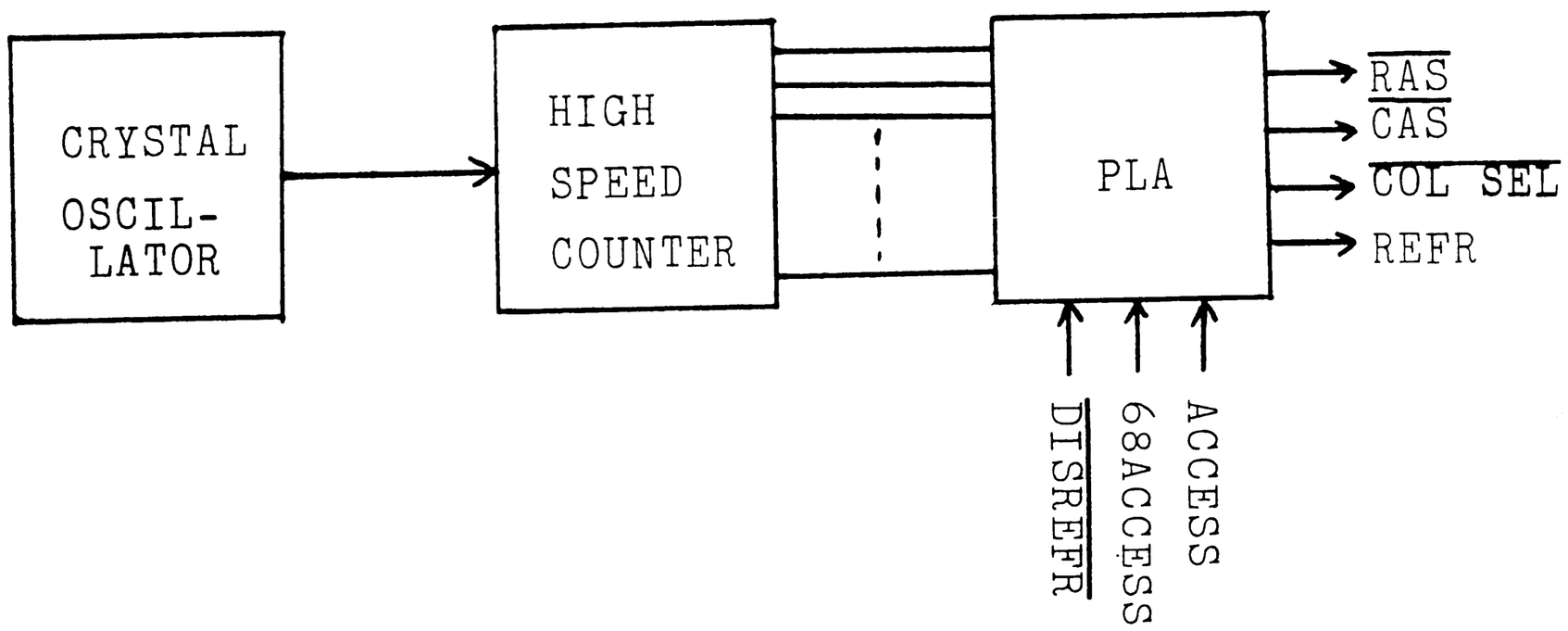


Figure 12: RAM Controller with Improved Stability

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Vita

Garrett J. Derbyshire was born in Philadelphia, PA, to Mr. and Mrs. Roger S. Derbyshire on June 4, 1957. He received the B.S. degree in Electrical Engineering with Highest Honors from Lehigh University in 1981. While pursuing the M.S. degree in Electrical Engineering, he was employed as a Development Engineer with the Hewlett Packard Biomedical Products group. He is currently a combined degree candidate, pursuing both the M.D. degree and the Ph.D. degree in Bioengineering, at the University of Pennsylvania on a fellowship from the National Institute of Health.