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# EVALUATION OF SILICON CARBIDE AS A FURNACE MATERIAL FOR USE IN MOS DEVICE FABRICATION

by

Robert W. Schanzer

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1984

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Certificate of Approval

This thesis is accepted in partial fulfillment of the requirements for the degree of Master of Science.

12/13/84
(Date)

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Thesis Advisor

Chairman of Department

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## ABSTRACT

The fabrication of an MOS memory device requires approximately twenty-five different furnace operations. This thesis demonstrates the feasibility of substituting high purity silicon carbide process tubes and paddles for the widely used quartz tubes and paddles and mullite liners now generally in use. The important physical properties of silicon carbide components which determine the applicability of this material to furnace processing were considered. These properties include thermal conductivity, purity and mechanical strength. In addition, results are presented to show that the memory devices (DRAM) could be successfully processed using silicon carbide process tubes. These devices have passed reliability testing.

# I. INTRODUCTION

## Background

An initial interest in silicon carbide (SiC) process tubes developed in 1980 when a new A T & T facility in the Orlando area was being considered. It was shown that power in that area, particularly in the summer months was subject to frequent power line disturbances (1). These disturbances could potentially affect any microprocessor controlled facility. Specifically, the loss of power to a furnace facility could result in large quantities of cracked furnace liners and/or fused quartz tubes, not to mention the loss of the production time involved. If these conventional process tubes and liners were replaced with tubes made of a material that was less susceptible to thermal shock, and was suitable in terms of purity and thermal properties, then the risk from power failures would be minimized. Additionally, silicon carbide process tubes can be used for higher temperature processing. Certain device codes require furnace temperatures in excess of 1200oC. Quartz tubes and paddles can not withstand such temperatures for long periods of time. Eventually, these quartz components deform and must be replaced. Because of the superior high temperature behavior of silicon carbide, mechanical deformation (see Table 1) such as sagging due to creep is prevented and long service life is practical. Furthermore, current A T & T practice is to periodically replace quartz tubes, paddles and mullite liners even when the temperatures involved are less than 1200oC due to the devitrification of quartz and the lower thermal skock resistance of mullite. Thus, the use of SiC for tubes and paddles would represent a permanent replacement and also offer significant cost savings.

TABLE 1

COMPARATIVE PHYSICAL PROPERTY DATA

| Properties | Typical Values | | |
|---|---|---|---|
| | Crystar-XP[1] | Polysilicon | Quartz |
| Density $g/cm^3$ | 3.0 | 2.3 | 2.2 |
| Coefficient of Thermal Expansion (RT to 1000°C) $\times 10^{-6}/°C$ | 4.8 | 3.8 | 0.5 |
| Thermal Conductivity (1000°K) W/(m.°K) | 38.0 | 33.0 | 4.0 |
| Thermal Capacity (1000°K) J/kg.°K) | 1130.0 | 920.0 | 1210.0 |
| Cross Bending Strength (1200°C) MPa | 172.0 | * | 107.0 |
| Young's Modulus of Elasticity GPa | 280.0 | 110.0 | 70.0 |
| Electrical Resistivity ohm-cm RT | 0.1 | * | $1 \times 10^{17}$ |
| 600°C | - | * | $5 \times 10^{6}$ |
| Emissivity (1000°K) | 0.8 | 0.7 | 0.6 |
| Apparent Porosity | <1% | <1% | <1% |

1 Trademark, Norton Co., Worcester, MA

* Not Available

Another important feature of SiC is its high thermal conductivity. The thermal conductivity of SiC is over nine times the thermal conductivity of quartz and six times the thermal conductivity of mullite. In addition, the emissivity is higher than fused quartz (see Table 1). Because of these properties the transient temperature response of a furnace during wafer insertion is improved. High thermal conductivity promotes uniform heating of wafers by redistributing the thermal energy thus normalizing hot spots within the flat zone. This effect should also improve process uniformity (i.e. oxide thickness).

Finally, the high purity of silicon carbide diffusion components gives the potential for providing low contamination. It has been shown that SiC acts as an effective diffusion barrier for metallic impurities and sodium (2). Such species now diffuse through the fused quartz tube, their source being the mullite liner. These impurities readily contaminate wafers inside the process tube (3).

This thesis will show that since SiC process tubes appear to have both the requisite purity and mechanical strength, there is no longer a need for using liners. Therefore, larger diameter process tubes that would allow processing of larger diameter wafers would be possible in existing furnace facilities.

## Economic Analysis

Table 2 lists current prices of mullite and quartz furnace components and their replacement frequency. This table shows that quartz tubes and paddles used at temperatures below 1000°C have a replacement frequency of twice a year while tubes and paddles used at higher temperatures have a replacement frequency of seven times per year. Table 3 lists the cost of a silicon carbide tube, paddle and rack.

Although the average lifetime of a SiC process tube has not been determined, we can assume that it will last at least as long as a polysilicon tube, which has demonstrated lifetimes of approximately five years (4). As an example for the economic analysis, assume there is a cleanroom which has a diffusion facility consisting of one hundred tubes. Assume that the process tubes and paddles being used are fused quartz and each tube is enclosed by a mullite liner. Also assume that fifteen percent of these tubes will be used at temperatures exceeding 1000°C. Then if the existing quartz/mullite liner system used in this clean room were replaced with SiC components a total savings of $505,500 per year would result. The actual breakdown of these prices is listed in Tables 4 and 5. And since the SiC tubes are expected to last up to ten years the savings could be even greater.

TABLE 2

BREAKDOWN OF QUARTZ AND MULLITE COSTS (per year per tube)

| ITEM | REPLACEMENT FREQUENCY | PRICE | TOTAL |
|---|---|---|---|
| QUARTZ PROCESS TUBE (TEMP ≤ 1000°C)* | (2.0/yr) | $700 | $1400 |
| QUARTZ PADDLE (TEMP ≤ 1000°C)* | (2.0/yr) | $400 | $800 |
| QUARTZ PROCESS TUBE (TEMP > 1000°C)** | (7.0/yr) | $700 | $4900 |
| QUARTZ PADDLE (TEMP > 1000°C)** | (7.0/yr) | $400 | $2800 |
| MULLITE LINER | (1.0/yr) | $1250 | $1250 |
| QUARTZ BOATS (USED FOR HIGH TEMP > 1000°C ) | (26.0/yr) | $100 | $2600 |

* Temp ≤ 1000°C is defined as process tube and paddle used at 1000°C or less.

** Temp > 1000°C is defined as the same process tube and paddle as above but used at a greater temperature, thereby requiring a greater replacement rate.

TABLE 3

COST OF SILICON CARBIDE COMPONENTS

| ITEM | PRICE |
|---|---|
| COST OF SILICON CARBIDE PROCESS TUBE | $10,400.00 |
| COST OF SILICON CARBIDE PADDLE | $ 2,200.00 |
| COST OF SILICON CARBIDE RACKS | $ 848.00 |
| TOTAL COST OF SiC TUBES, PADDLES & RACKS | $13,448.00 |

TABLE 4

SUMMARY OF SUPPLY SAVINGS VS. SILICON CARBIDE INITIAL COST

| | |
|---|---|
| TOTAL NUMBER OF PROCESS TUBES IN THE CLEAN ROOM | 100 |
| COST OF QUARTZ TUBES | |
| A. TUBES AT TEMP $\leq$ 1000°C (85 TUBES) | $119,000 |
| B. TUBES AT TEMP > 1000°C (15 TUBES) | $ 73,500 |
| COST OF QUARTZ PADDLES | |
| A. PADDLES AT TEMP $\leq$ 1000°C (85 PDLS) | $68,000 |
| B. PADDLES AT TEMP > 1000°C (15 PDLS) | $42,000 |
| COST OF QUARTZ RACKS (BOATS) | |
| A. QUARTZ RACKS (AT TEMP > 1000°C) (15 X 2 RACKS/TUBE = 30) | $ 78,000 |
| COST OF MULLITE LINERS | $125,000 |
| TOTAL QUARTZ/MULLITE COSTS = TOTAL SAVINGS/yr = | $505,500/yr |

TABLE 5

INITIAL SILICON CARBIDE COST

| | |
|---|---|
| TOTAL COST OF 100 SILICON CARBIDE PROCESS TUBES AND PADDLES | $1,260,000 |
| SILICON CARBIDE RACKS (MINIMUM QUANTITY-30) | 25,440 |
| BULK DISCOUNT AT 10% | $128,544 |
| TOTAL COST OF SiC PROCESS TUBE, PADDLE, RACK | $1,156,896 |

Statement of the Thesis

This thesis presents the results of a study that demonstrates the feasibility of substituting the conventional quartz paddle, quartz tube and mullite liner with a SiC paddle and a single silicon carbide tube in a standard furnace facility. Such a substitution will provide process tubes with an extended lifetime and will in the long run reduce manufacturing costs. It will also allow for the production of larger diameter wafers or the use of cantilever loading in already existing furnace facilities.

# II. LITERATURE REVIEW

## History of Silicon Carbide Components

Silicon carbide has been manufactured since 1892. At that time loose grains of SiC were primarily used as a lapping and polishing compound. Because of properties such as high temperature stability, corrosion resistance, good thermal conductivity and thermal shock resistance, silicon carbide components were used as refractory materials. Some refractory uses included shapes for kiln furniture, muffles and hearths for furnaces, and retorts and condensors for zinc distillation (5).

Through the use of new bonding techniques with silicon nitride or silicon carbide itself, other applications were found. The silicon nitride bonded material made the production of rocket nozzles and combustion chambers possible. The self-bonded recrystallized SiC, which consisted of SiC with less than 5% of any other material was used for heating elements, heat exchangers and thermocouple protection tubes (6).

As the application for SiC components increased a need for a purer material also developed. When silicon carbide diffusion components were introduced to the area of device fabrication purity was a problem. Certain parameters in semiconductor devices are greatly effected by impurities. One parameter in particular is the minority carrier lifetime (7). Carrier lifetimes are reduced by small quantities of certain metallic impurities (8). The presence of impurity precipitates in devices are also detrimental (9).

Impurity Analysis on the Material

In the past few years much work has been done in the field of contamination detection in silicon device manufacturing. In a recent paper, Schmidt (10) compared the impurity concentrations in different types of process tube liners using Neutron Activation Analysis (NAA). The liners compared were: 1) standard mullite; 2) high purity mullite; and 3) high purity alumina. In the same paper, Schmidt reported NAA results for high purity silicon carbide liners and compared them with standard silicon carbide liners of previous years. The results of these analyses are listed in Table 6 and Table 7. The results show that the purity of the silicon carbide liners has improved greatly since 1968 and that their purity appears superior to any of the other liners analyzed (Table 6).

Since the NAA results of silicon carbide liners show low impurity content, the question arises, can silicon carbide process tubes exhibit the same high purity and can these tubes replace the standard quartz and mullite combination?

Silicon Wafer Impurity Analysis

Pearce and Schmidt (11) have examined silicon wafers oxidized in a quartz process tube enclosed by a mullite liner (Table 8). The average impurity concentrations reported were obtained from furnace control wafers processed in two clean rooms. The analysis of the impurity concentrations listed in columns one and two is from the 1974-75 time period while the analysis listed in column three represents 1977. These values form a basis to which the present study can be compared.

TABLE 6

Impurities in Standard Mullite,
High Purity Mullite
and High Purity Alumina ($Al_2O_3$) Furnace Liners*

All Concentrations in ppm

| Element | Standard Mullite | High Purity Mullite | High Purity $Al_2O_3$ |
|---|---|---|---|
| Cu | 282.0 | 487 | trace |
| Mn | 50.5 | 36.5 | n.d. |
| Cr | 62.9 | 4.1 | 7.1 |
| Fe | 8185 | 545 | 512 |
| Co | 5.7 | 0.36 | 0.27 |
| Ni | 9.4 | 1.4 | 9.4 |
| Zr | 210 | 30.3 | 1000 |
| Hf | 6.2 | 1.4 | 1.7 |
| Ta | 3.6 | 0.07 | n.d. |
| Mo | n.d. | n.d. | n.d. |
| W | 8.2 | n.d. | 1.6 |
| Th | 2.2 | 0.32 | n.d. |
| U | 0.12 | 0.16 | n.d. |
| Na | 980 | 342 | 350 |
| K | 7570 | 41.5 | 143 |

n.d. - defined as not detected

* Analysis performed by Schmidt, reference (2).

TABLE 7

Impurities in Standard Silicon Carbide Furnace Liners
As A Function of Approximate Manufacturing Date*

All Concentrations in ppm

| Element | 1968 | 1973 | 1978 | 1982 |
|---|---|---|---|---|
| Cu | 380 | 24.2 | 2.2 | 0.17 |
| Mn | 103 | 35.2 | Trace | 0.24 |
| Cr | 75.1 | 43.1 | 0.39 | 0.37 |
| Fe | 19350 | 2883 | 122 | 24.7 |
| Co | 51.1 | 2.3 | 0.20 | 0.17 |
| Ni | 195 | 43.3 | 10.6 | 12.3 |
| Zr | 9325 | 19.6 | 4.9 | 18.4 |
| Hf | 3.5 | 0.61 | 0.12 | 0.31 |
| Ta | - | 0.11 | 0.001 | 0.003 |
| Mo | - | 3.2 | 0.61 | 2.4 |
| W | 0.42 | 0.59 | 0.03 | - |
| Th | - | 0.49 | 0.10 | 0.74 |
| U | - | 0.20 | 0.13 | 0.88 |
| Na | 19900 | 2.10 | 2.00 | 85.1 |
| K | 1860 | - | - | 32.9 |

(-) defined as not detected

* Analysis performed by Schmidt, reference (2)

TABLE 8

Average concentration per cc detected on furnace controls from the DCL and MOS clean rooms 1974-75 and on processed wafers in the DCL in 1977*.

| | Standard Quartz Tube/Mullite Liner | | |
|---|---|---|---|
| Element | DCL | MOSIC | DCL 1977 |
| Cu | 2.0E14 | 3.0E14 | 7.8E13 |
| Ni | 2.0E14 | 8.6E14 | 1.26E14 |
| Fe | 1.08E15 | 1.46E15 | 2.2E14 |
| Cr | 3.20E14 | 4.0E14 | 1.7E13 |
| Co | 3.4E12 | 4.8E13 | 4.6E12 |
| Au | 3.8E12 | 1.2E13 | 1.8E13 |
| Na | 1.66E14 | 4.8E14 | Not recorded |

* Analysis performed by Pearce and Schmidt, reference (11)

Table 9 shows the concentration (per cc) of wafers oxidized in a silicon carbide process tube in another cleanroom at the Allentown plant in 1982. Note that in Table 9 half the samples were oxidized in a 98% $O_2$ and a 2% HCL ambient, while the other half were oxidized in a 100% $O_2$ ambient. This table shows that the average concentration of impurities on wafers oxidized in the $O_2$-HCL ambient is essentially equivalent to wafers oxidized in an $O_2$ ambient. Also, note that in Table 9 iron and chromium were analyzed for and not detected. This is not surprising since the iron and chromium concentrations in the original silicon carbide material are very low, Table 7. It is interesting to note that if the impurity concentrations for each wafer in Table 9 were averaged, the results would be very similar to those results listed in Table 8.

In another paper by B. D. Foster and R. F. Tressler (12) trace amounts of impurities on wafers processed in three different process tubes were analyzed by Atomic Absorption Spectroscopy and compared. The three types of process tubes used were a Norton Crystar silicon carbide tube, a polysilicon tube, and a fused silica or quartz tube. Prior to any oxidations each of the tubes was purged with 5% HCL for approximately eight hours after which the tubes were then purged with nitrogen for one day. Wafers, prior to oxidation, were cleaned with a standard clean (13) and then inserted into the furnace in a pure $O_2$ ambient. After oxidizing at 1100oC for three hours, the wafers were annealed with nitrogen for ten minutes.

TABLE 9

Impurity concentration per cc detected on furnace controls processed in a silicon carbide tube in MOS IVB in 1982*.

| Wfr ID | HCL-1 | | HCL-2 | | NO HCL-1 | | NO HCL-2 | |
|---|---|---|---|---|---|---|---|---|
| | 24 | 25 | 19 | 20 | 21 | 22 | 17 | 18 |
| Element | | | | | | | | |
| Cu | 2.78E15 | 6.3E14 | - | 5.3E14 | 1.48E15 | 6.4E14 | - | - |
| Ni | - | 4.34E14 | 3.10E14 | 2.47E14 | 3.73E14 | 3.68E14 | 2.64E14 | - |
| Fe | - | - | - | - | - | - | - | - |
| Cr | - | - | - | - | - | - | - | - |
| Co | 8.63E12 | 9.83E12 | 7.53E12 | - | 1.13E13 | 1.43E13 | 5.07E12 | 5.9E12 |
| Au | 2.77E12 | 1.23E12 | 8.47E11 | 7.07E11 | 1.44E12 | 1.24E12 | 1.11E12 | 1.07E12 |
| Na | 2.69E15 | 8.46E15 | 8.66E15 | 6.64E15 | 2.21E15 | 4.22E15 | 1.19E15 | 5.55E15 |
| W | 4.83E12 | - | - | - | - | - | - | - |
| Hf | 1.31E12 | - | - | 5.8E11 | 1.41E12 | 5.81E12 | 1.8E12 | 2.31E12 |
| Sc | - | 5.13E11 | 5.23E11 | 3.64E11 | 2.33E11 | 2.13E11 | 2.84E11 | - |
| Zr | - | - | - | - | 2.39E14 | 2.24E14 | - | - |
| Zn | - | - | - | - | 4.99E13 | 5.02E13 | - | - |

(-) denoted as not detected

* Analysis performed by Schmidt

The top 10 microns of two wafers from each run were then etched in a solution of nitric and hydrofluoric acid. After additional steps which included evaporation and further acid cleans, the etchant from each sample was analyzed using the atomic absorption technique. The results of this analysis (Table 10) showed that the wafers processed in the silicon carbide process tube were much purer than wafers processed in either the polysilicon or quartz tubes.

In general the impurity levels detected by Foster and Tressler were higher than those quoted by Pearce and Schmidt (11). This is because the impurity concentrations were determined for the surface layers and not for the entire wafer. Other work has shown that the impurity concentrations at the surface are approximately 50 to 100 times greater than the impurity concentrations in the bulk of the wafer (14). The conversion of these concentrations to concentrations averaging over the bulk of the wafer (as done for NAA results in this study) is shown in column 5 of Table 10 (divide values in column 4 by 50). These results now agree with the results presented in Tables 8 and 9.

TABLE 10

Impurity Analysis of Oxidized Silicon Wafers
Atomic Absorption Spectroscopy of the Top 10 Micron Layer*

Average Concentration Per $Cm^3$

| | Process Tubes | | | |
|---|---|---|---|---|
| | | | SiC | |
| Element | Fused Silica | Polysilicon | Top 10[1] Micron | Total[2] Volume |
| Cu | 7.0E15 | 3.3E15 | 2.0E15 | 4E13 |
| Ni | 1.57E17 | 3.0E16 | 3.0E16 | 6E14 |
| Fe | 2.0E17 | 1.4E16 | 1.1E16 | 2.2E14 |
| Cr | 2.5E16 | 2.5E15 | 1.0E15 | 2E13 |
| Co | 2.8E16 | 7.4E15 | 4.8E15 | 9.6E13 |
| Au | 6.0E14 | 6.0E14 | 6E14 | 1.2E13 |
| Mn | 7.8E15 | 8.5E14 | 9.0E14 | 1.8E13 |

* Results by B. D. Foster and R. E. Tressler, reference (12)

[1] See text for method of analysis

[2] Total volume as explained in text

## III. Materials

### High Purity Crystar XP Silicon Carbide Tube

The high purity "Crystar" silicon carbide process tubes used in these experiments were purchased from Norton Industries. The overall tube length was 188 cm (74 inches) with a minimum inner diameter of 16.51 cm (6.5 inches) and maximum outer diameter of 17.78 cm (7.0 inches). The tube was fabricated from silicon carbide grain and slip cast into its final shape. It was then fired to a temperature above 2100oC under controlled atmospheric conditons in order to achieve a continuous SiC matrix. The tube contains 10 to 15% of unreacted silicon and a small percentage of voids or pores. The composition is the same as that of liners presented previously in column 4 of Table 7.

### T07 Fused Quartz Tube

The T07 clear fused quartz tubes were purchased from Heraeus-Amersil Inc.. The overall length of the quartz tube was also 188 cm (74 inches) with a minimum ID of 15.24 cm (6.0 inches) and a maximum outer diameter of 16.15 cm (6.357 inches). The actual composition of this tube is listed in Table 11.

### MV-30 Mullite Liner

The MV-30 Mullite liner was supplied by McDanel Refractory Porcelain Company. The overall tube length was 172.72 cm (68 inches) with a minimum 17.3 cm (6 13/16 inch) ID by a maximum 19.5 cm (7 11/16 inch) OD. Physical properties of this material is listed in Table 12.

TABLE 11

Clear Fused Quartz Impurity Analysis*

| Element | ppm by weight |
|---|---|
| Al | 10.0 to 50.0 |
| Sb | 0.15 |
| As | 0.08 |
| B | 0 to 0.1 |
| Cd | 0 to 0.1 |
| Ca | 0.8 to 3.0 |
| Cr | 1.0 to 2.0 |
| Cu | .07 |
| Ga | 0 to .008 |
| Au | 0.0003 |
| Fe | 0.8 |
| Li | 0 to 2.0 |
| Mg | 0.2 |
| Mn | 0.01 |
| P | 0.1 |
| K | 0.8 |
| Ag | n.d. |
| Na | 1.0 |
| Ti | 0.8 |
| U | .0003 |
| Zr | 0 to 0.1 |

* Analysis performed by Heraeus-Amersil, Inc.

TABLE 12

Typical Physical Properties of the MV-30 Mullite Liner*

| Property | Value |
|---|---|
| Constitution | 86% Mullite<br>15% Glass |
| Bulk Specific Gravity | 2.8 |
| Impenetrability | Gas Tight |
| Flexural Strength (psi) | 27,000 |
| Compressive Strength (psi) | >190,000 |
| Tensile Strength (psi) | 18,000 |
| Hardness (mohs) | 7.5 |
| Maximum Working Temp. | 1750°C |
| Maximum Temp. Supported Tube | 1700°C |
| Likely Sag Temp. Unsupported Tube | 1600°C |
| Thermal Conductivity 24°C<br>(BTU/ft$^2$/hr./°F/in) 800°C | 40<br>25 |
| Dielectric Strength 24°C V/mil | 250 |
| Thermal Expansion (per °C x $10^{-6}$)<br>(24°C - 1000°C) | 5.0 |

* From McDanel 1981 Catalog.

## IV. EXPERIMENTAL PROCEDURE AND RESULTS

### Process Development

#### Equipment

##### Diffusion Furnaces

A comparison was made between wafers processed through a high purity silicon carbide tube versus the standard quartz tube and mullite liner configuration. Both types of tubes were evaluated using a Bruce BD-F 8-stack furnace manufactured by BTU Engineering Corporation. Each individual tube is microprocessor controlled using a DDC 7351 microcontroller. This controller includes direct digital temperature control, automatic time sequencing, automatic temperature profiling and programmed boat travel. Other features include setpoint outputs for mass flow controllers and process monitoring with alarms. Temperature uniformity in the 75 cm flat zone of each tube is $\pm$ 0.5°C in the temperature range 800°C - 1250°C with a maximum gas flow of five liters per minute. A photograph of this furnace is presented in Figure 1.

##### Film Thickness Measuring Instruments

1. The instrument used for measuring oxide thicknesses above 400 A was a Nanospect/AFT system, manufactured by Nanometrics Inc..
2. An Auto EL III ellipsometer manufactured by Rudolph Research was also used for measuring oxide thicknesses below 400 A.
3. A Perkin-Elmer spectrophotometer, model 553, was used for measuring oxide thicknesses over a doped polysilicon layer.

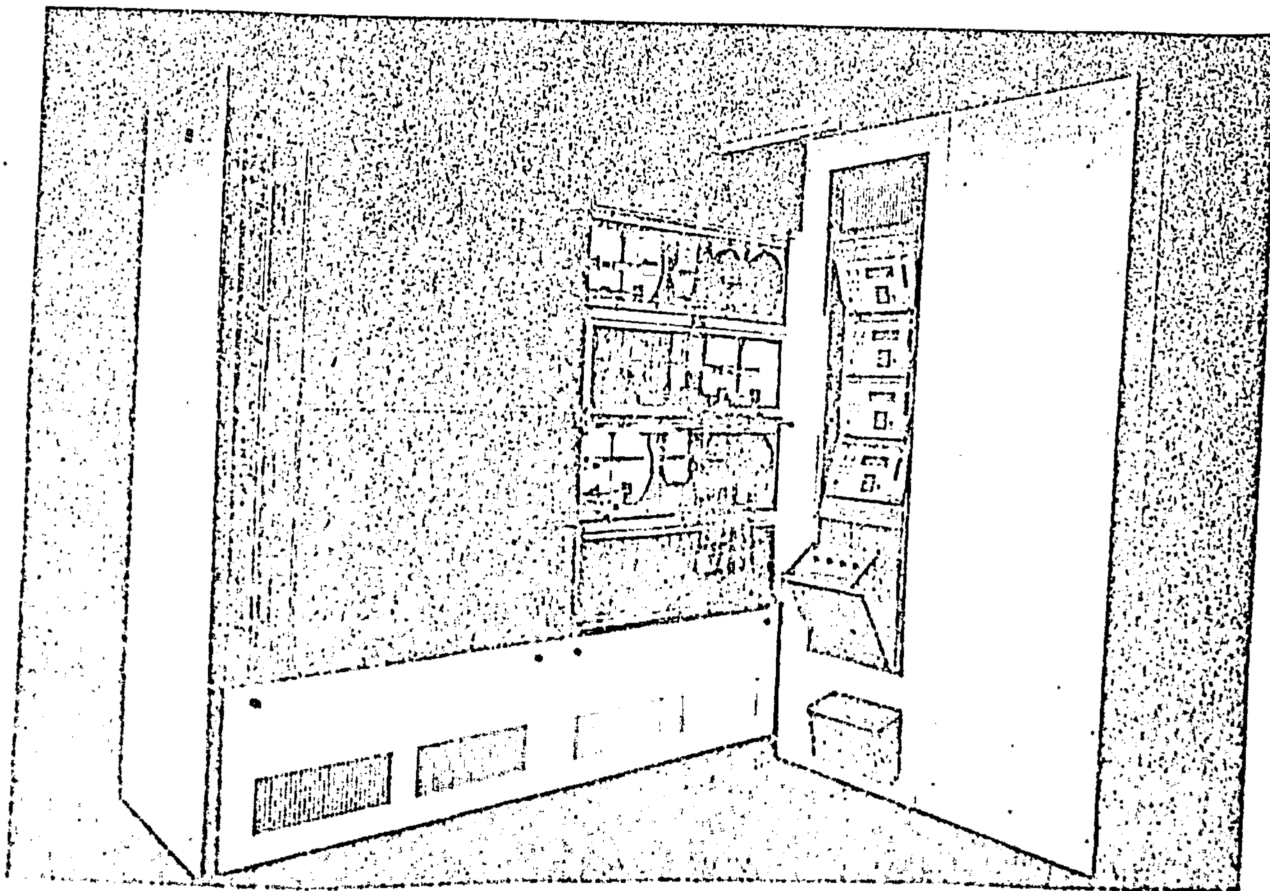


Figure 1. Bruce Diffusion Furnace

## Installation

A single gas inlet, high purity Crystar XP silicon carbide process tube and paddle were cleaned in a 10% HF solution for one hour, rinsed in deionized water, dryed in air and installed in the furnace described earlier. The tube and paddle were then heated to 1000oC for three hours after which a 5% HCL, 95% $O_2$ flow was passed through the tube for twelve hours.

Subsequently two additional high purity Crystar XP silicon carbide tubes and paddles were purchased and installed in the same furnace facility. These newer tubes were double inlet tubes. One inlet is used for gas flow into the tube the other for inserting profile thermocouples, enclosed in quartz sheaths, inside the tube. Prior to the installation these tubes were cleaned according to the procedure discussed above. A diagram of the double inlet tube and paddle is shown in Figures 2A and 2B.

## Establishing Furnace Parameters

Initial experiments using the single inlet high purity silicon carbide tube involved the fabrication of a 64K Dynamic RAM devices. Four specific oxidation processes were developed. These processes included oxidations consisting of $O_2$ and HCL mixtures. Temperatures, gas flows and wafer insertion speeds for each individual process were determined. A method was also developed for automatic profiling of the four different process temperatues, namely 850oC, 900oC, 950oC, and 1000oC. Experiments were made using 100mm wafers to demonstrate that oxide thicknesses would be within specifications.

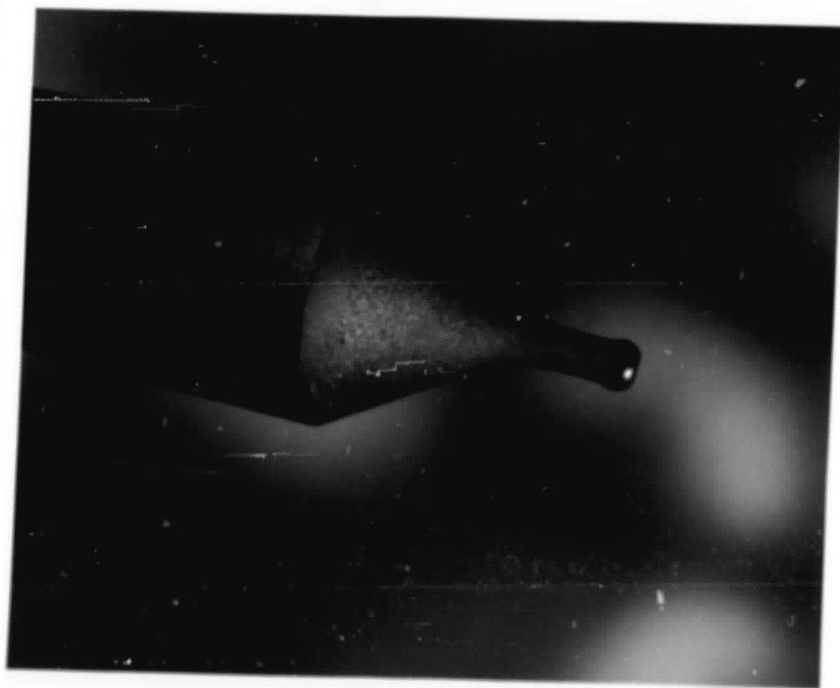


Figure 2A. Photographs of Double and Single Inlet SiC Process Tubes. Courtesy of Norton Industrial Ceramics, Worcester, Mass.

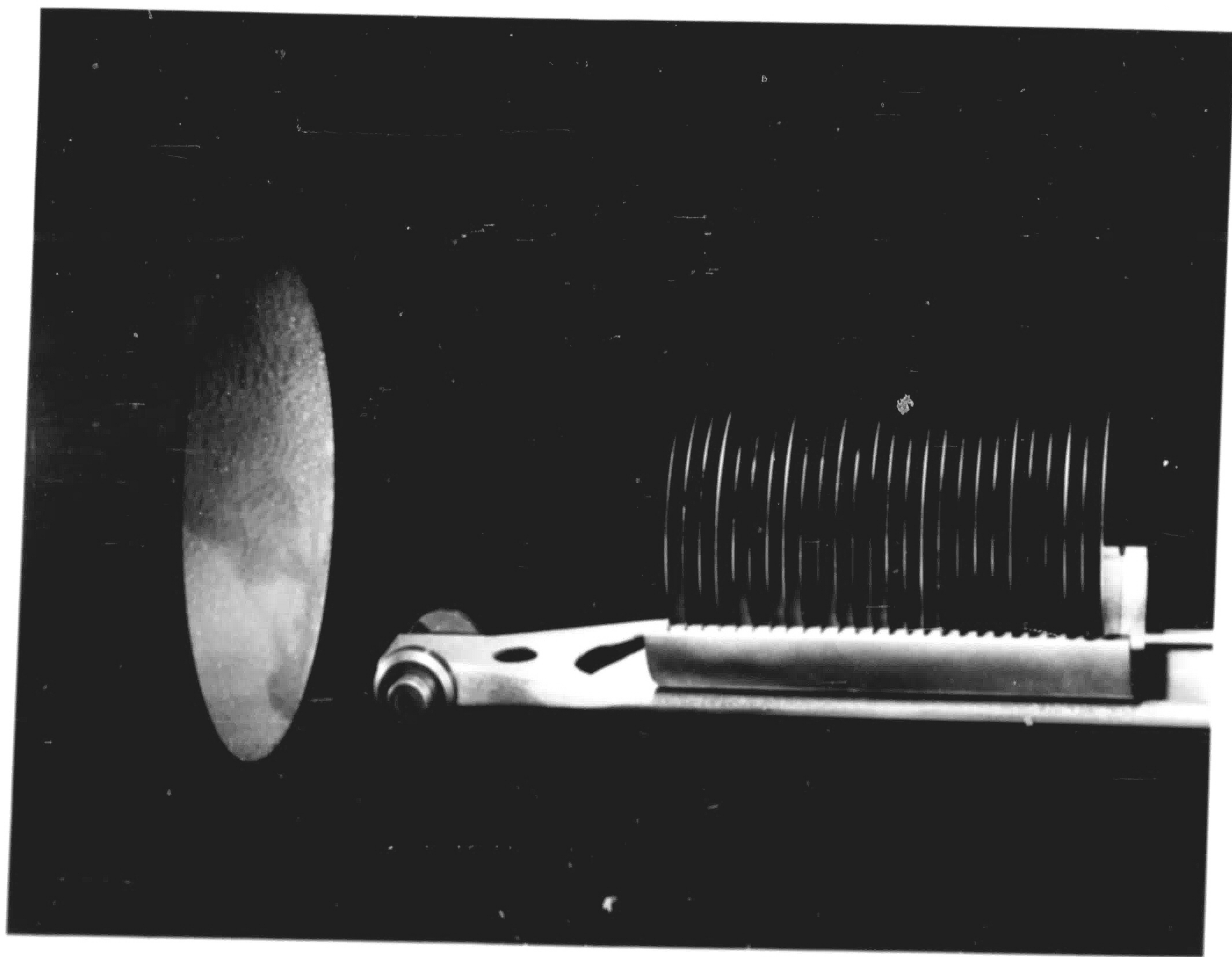


Figure 2B. Photograph of SIC Paddle and Rack. Courtesy of Norton Industrial Cermics, Worcester, Mass.

The second series of experiments involved the 256K Dynamic RAM. For this experiment all three silicon carbide tubes were used. Dry $O_2$ and $O_2$-HCL Oxidation processes were conducted in one tube, while steam oxidations were performed in the second tube. A phosphorus diffusion process was set up in the original single inlet tube. Once again temperatures, flow rates and wafer insertion speeds were determined. Control runs were then made using 125mm wafers in Microglass[a] quartz racks. Once these preliminary runs gave oxide thicknesses within specification, process lots were started.

[a] Quartz carrier manufactured Micro Glass Inc.

## Thermal Characteristics

### Transient Behavior

In this part of the study the transient temperature-time behavior of both the SiC process tube and the quartz process tube was determined and analyzed. First, a discussion of the terminology of the furnace zones is needed. In a Bruce BD-F 8 stack furnace there are three zones: load, center and source zones. With this type of furnace configuration there are also two different sets of thermocouples, the control or heater thermocouples and the process or profile thermocouples. The three control thermocouples (load, center, source) are positioned perpendicular to and approximately 0.2 cm away from the mullite liner. This mullite liner surrounds or encloses the fused quartz process tube. The three control thermocouples (load, center, source) are positioned at a distance of 126.37 cm (49.75 inches), 83.19 cm (32.75 inches) and 40.01 cm (15.75 inches) measured from the source end of the furnace (see Figure 3). The process thermocouples, enclosed in quartz sheaths, are inserted between the mullite liner and the quartz process tube. These thermocouples are positioned at a distance of 123.83 cm (48.75 inches), 83.19 cm (32.75 inches) and 42.55 cm (16.75 inches) measured from the source end of the furnace. Hence neither set of thermocouples measures the actual wafer temperature inside the furnace. Since the SiC process tube was used without a liner the three process thermocouples were positioned inside the SiC tube, inside a quartz sheath at the same axial location as given above. Therefore, it is important to realize that in the following section, we are comparing the transient response of thermocouples with different measurement conditions.

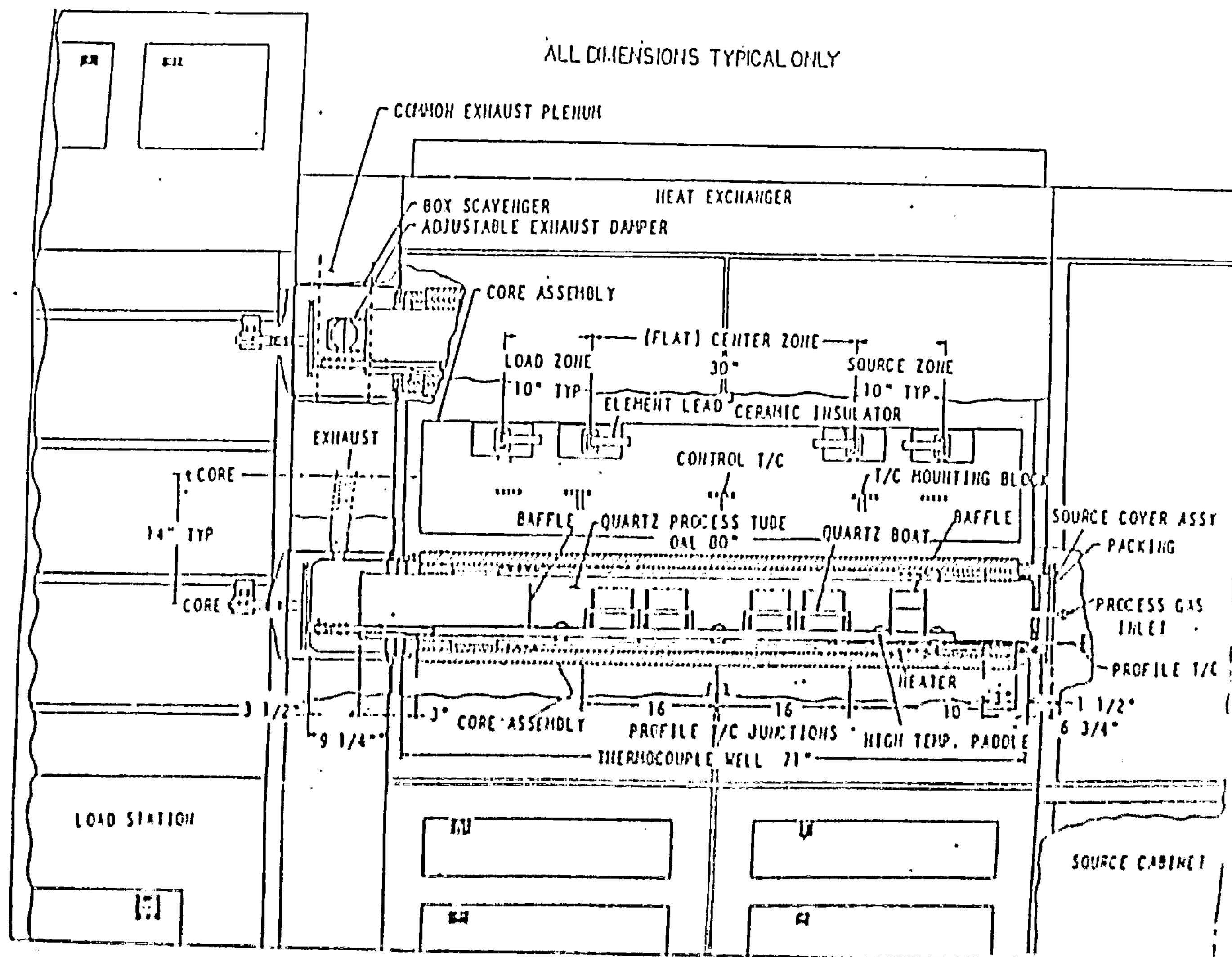



Figure 3

Bruce Furnace Section

Both process tubes were automatically profiled at 950°C in each zone with the paddles completely inserted. They were also profiled at 850°C with the paddles outside the furnace. One hundred 125mm wafers plus ten "baffle" wafers were loaded on the paddles each time the tube was profiled. These baffles were contained in short carriers and positioned at both ends of the work (see Figure 4). After profiling, a standard oxidation process was conducted in both tubes. Again one hundred 125mm wafers were used plus approximately ten baffle wafers. When the cycle was started each tube was at 850°C. After each paddle was inserted (taking 10 minutes) the furnace temperature was raised (ramped up) to 950°C in approximately 15 minutes. After approximately 65 minutes the furnace temperature was ramped back down to 850°C. The wafers were then withdrawn from the process tube at a rate of 5 cm per minute.

A plot of the transient response for the profile thermocouples for the two types of process tubes is shown in Figures 5A, 5B, and 5C. Especially notice Figure 5B, which shows the difference between SiC and the quartz/mullite system in the center zone region.

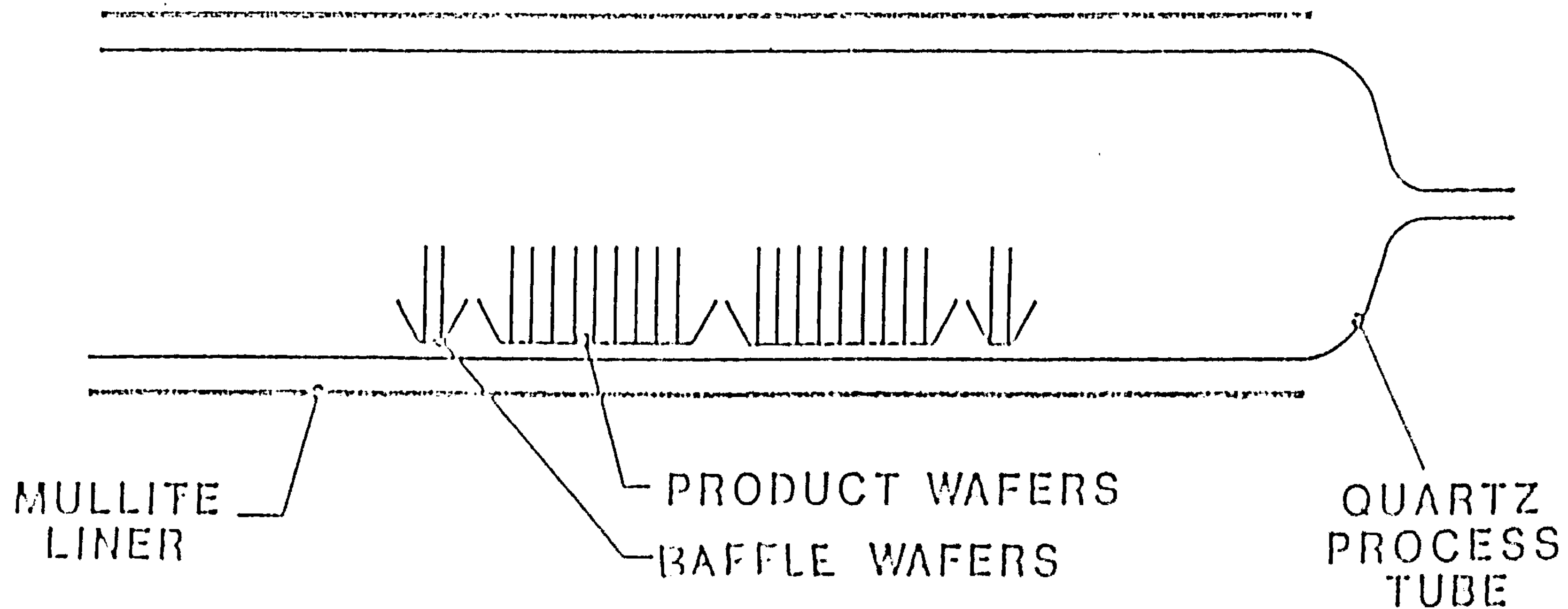



FIGURE 4

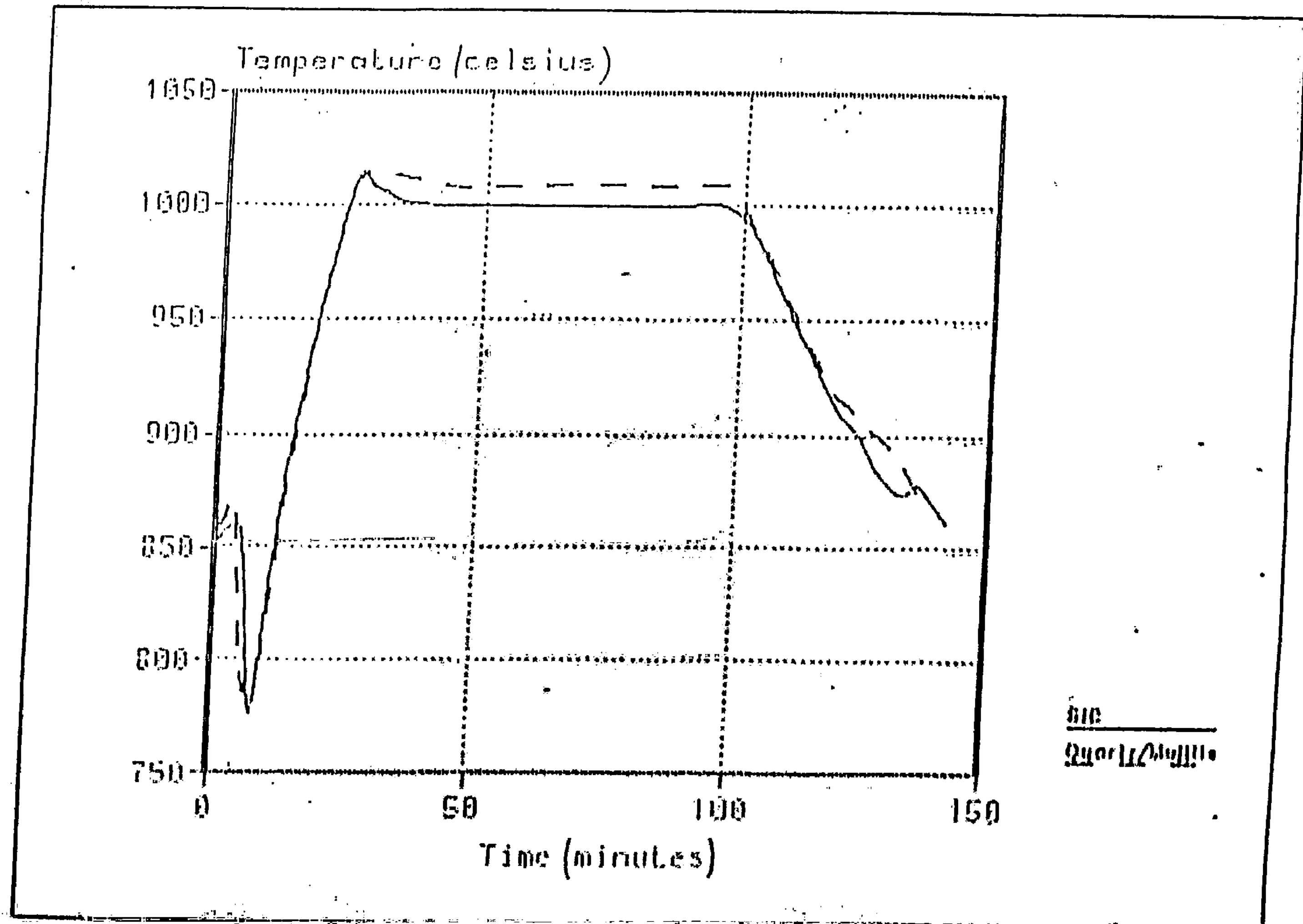



**Figure 5A. Transient Response - SiC vs. Quartz/Mullite Temperature vs. Time (load zone)**

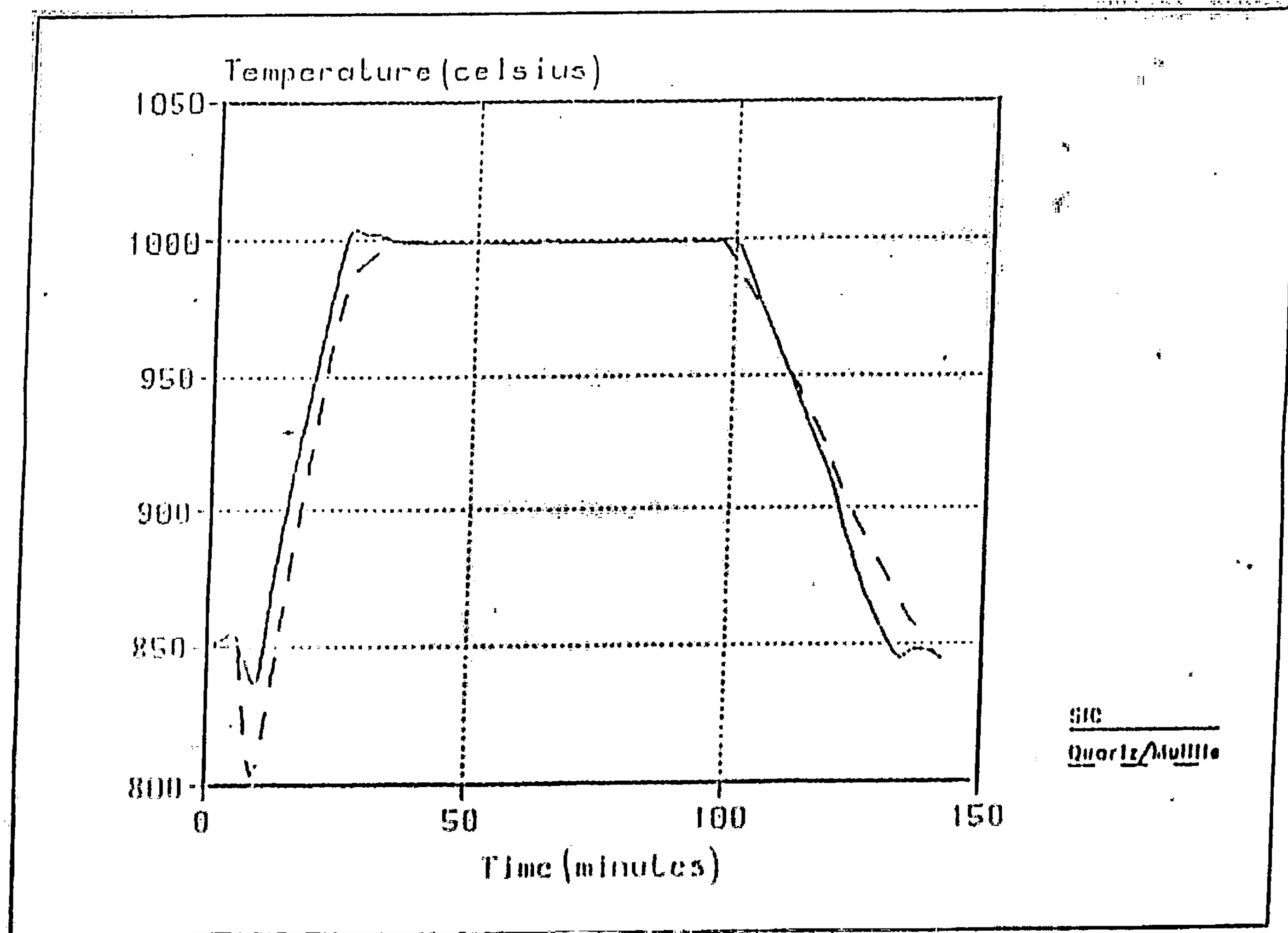
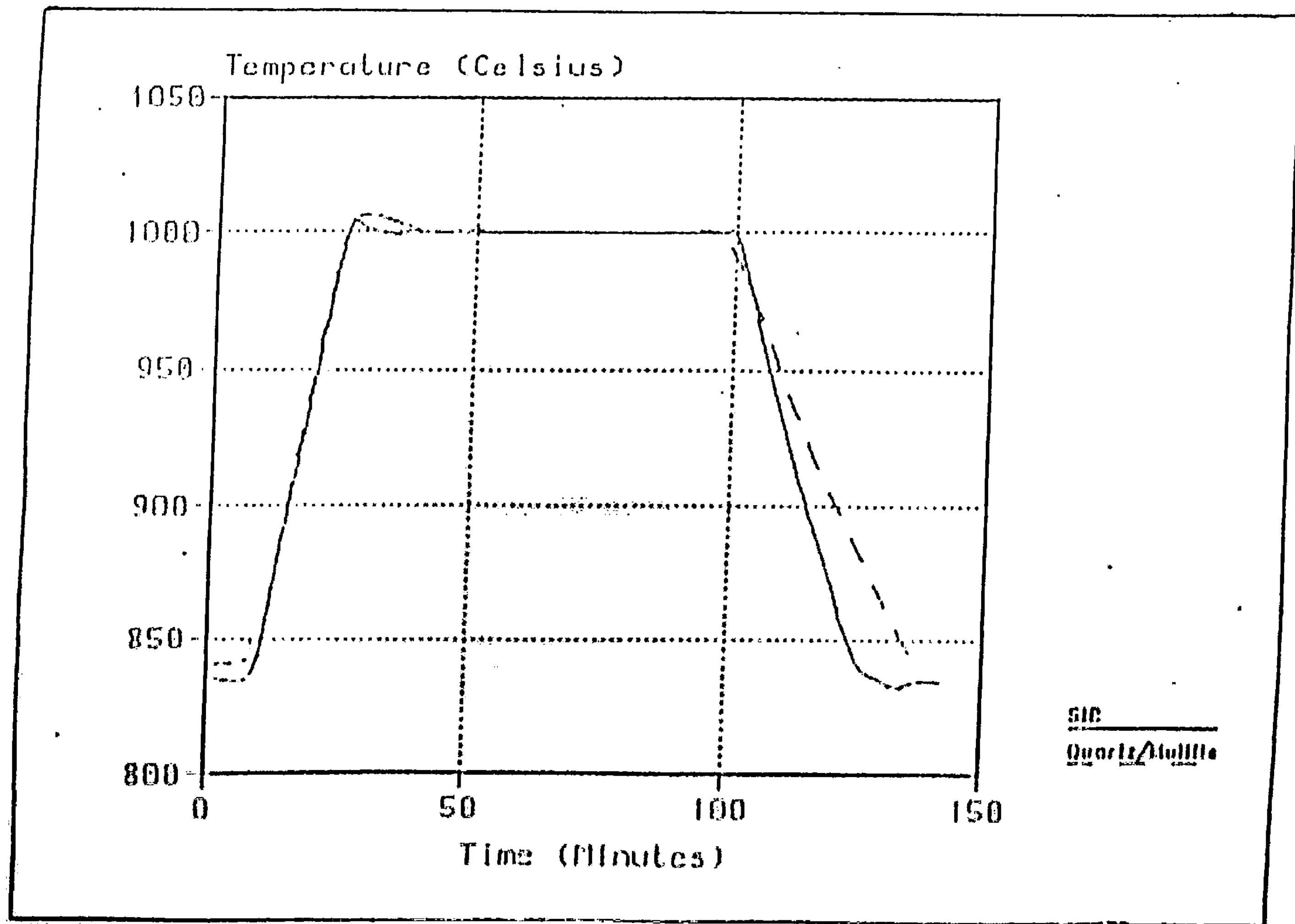



**Figure 5B.** Transient Response - SIC vs. Quartz/Mullite
Temperature vs. Time (center zone)




SIC
Quartz/Mullite

**Figure 5C. Transient Response - SIC vs. Quartz/Mullite Temperature vs. Time (source zone)**

Static Behavior

In order to determine the temperature profile inside the process tubes, a 106.68 cm (42 inch) platinum-platinum / 10% rhodium thermocouple enclosed in a quartz sheath was inserted into the open end of each tube. Both furnaces were originally profiled at 950°C with a paddle inserted into the tube. Initially the tip of the thermocouple was positioned approximately 2 cm (.75 inch) from the center of the flatzone. The thermocouple was connected to a direct reading digital meter, manufactured by Omega Engineering, Inc., model 407. Time was allowed for the thermocouple to equilibrate with the furnace. The temperature was measured and recorded. The thermocouple was then withdrawn 2.5 cm (1 inch), allowed to equilibrate again, then measured and recorded. This was repeated at 2.5 cm intervals until the thermocouple was completely withdrawn from the furnace tube. A plot of temperature versus position of the thermocouple was generated for both the silicon carbide and quartz process tubes (see Figure 6).

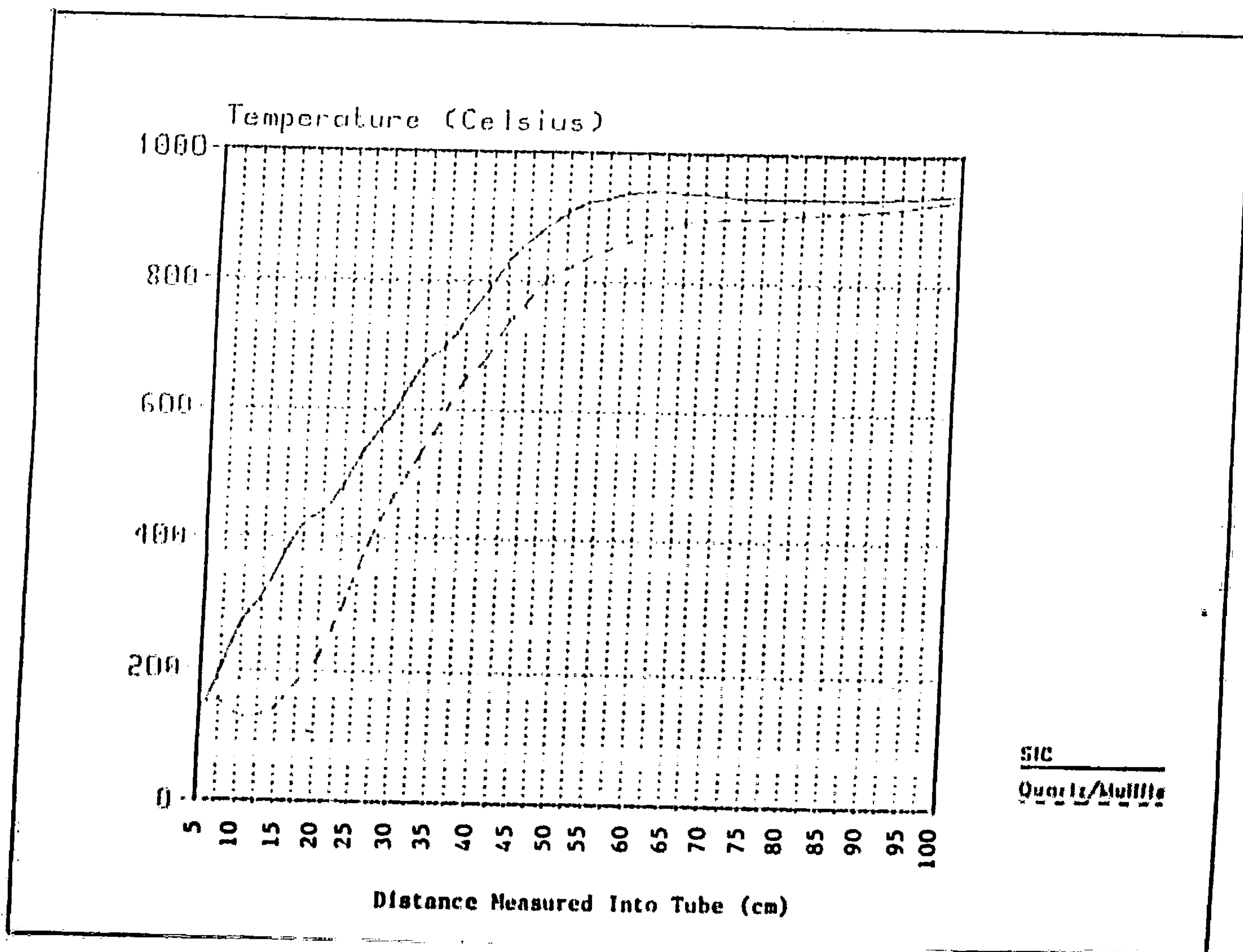



Figure 6. Static Behavior
SIC vs. Quartz/Mullite

## Material Characterization

### Microstructures

In an unpublished paper by Butler (15), the microstructure of crystar XP material was examined. Samples that were supplied by Norton Company, were polished through a 1/4 micron diamond in order to produce a surface suitable for examination.[b] The microstructure of an as-polished and cleaned sample is shown in Figure 7. From the photograph two different grain sizes are apparent in the structures. Both types of grains are SiC. There is also a matrix of unreacted silicon and some porosity. This porosity is largely due to the incomplete silicon impregnation (15).

When the material was oxidized the final result was an $SiO_2$ layer formed on top of the silicon carbide. The reaction is (16):

$$SiC + 2O_2 \dashrightarrow SiO_2 + CO_2$$

Figure 8 shows the sample after an oxidation process. Since the oxidation rate of SiC is anisotropic and is less than the oxidation rate of silicon, one can see this difference in the structure. According to Costello (16) the different growth rates, depending on the orientation of the individual grains, cause the interference colors. These interference colors are clearly shown in Figure 8.

[b] Samples polished by Mr. Fluck, Department of Geological Science, Lehigh University.

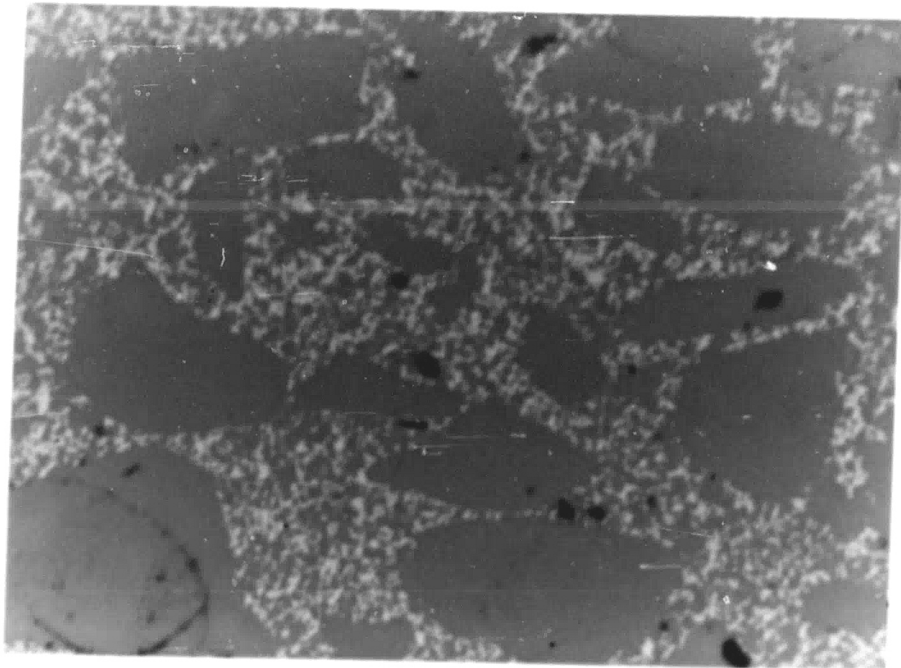


FIGURE 7. Optical Photograph of an as-received sample of high purity SiC. The sample was cleaned and polished. Magnification 250X.

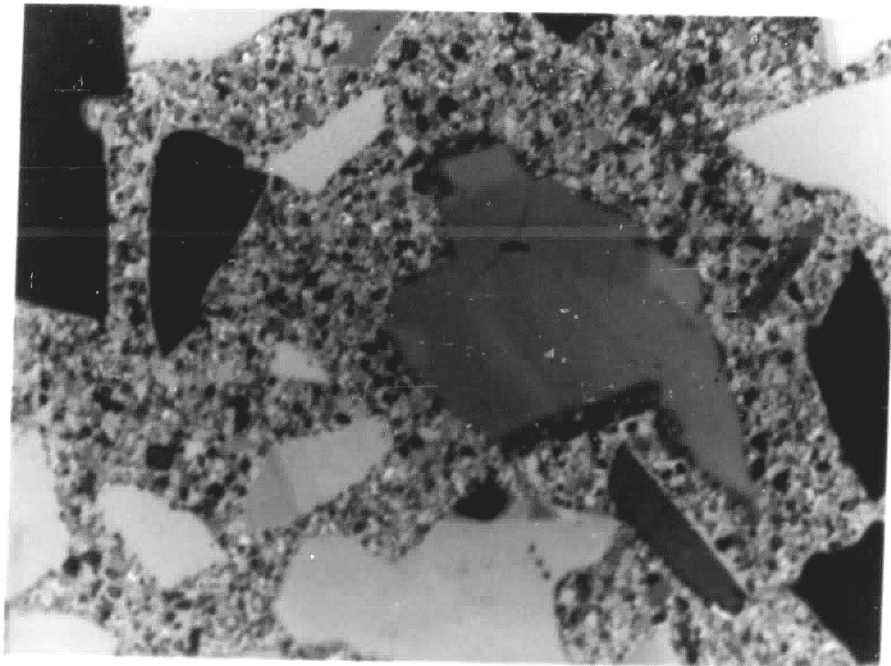


FIGURE 8. Optical Photograph of the SiC sample after oxidation. Magnification 500X

When another as-polished and cleaned sample was introduced to an ambient containing a mixture of oxygen, nitrogen and phosphorus tribromide, the result was quite different as shown in Figure 9. This figure shows, that after short exposure, there is some non-uniform attack of the SiC which is accentuated at pores. It was found that this attack results in a ring of bubbles in the oxide layer around the pore (see Figure 10). This non-uniform attack is considered to be undesirable. The concern is that after temperature cycling the thermal stresses may cause the phospho-silicate glass layer to flake off resulting in particles, although there was no evidence of particles after six months of operation.

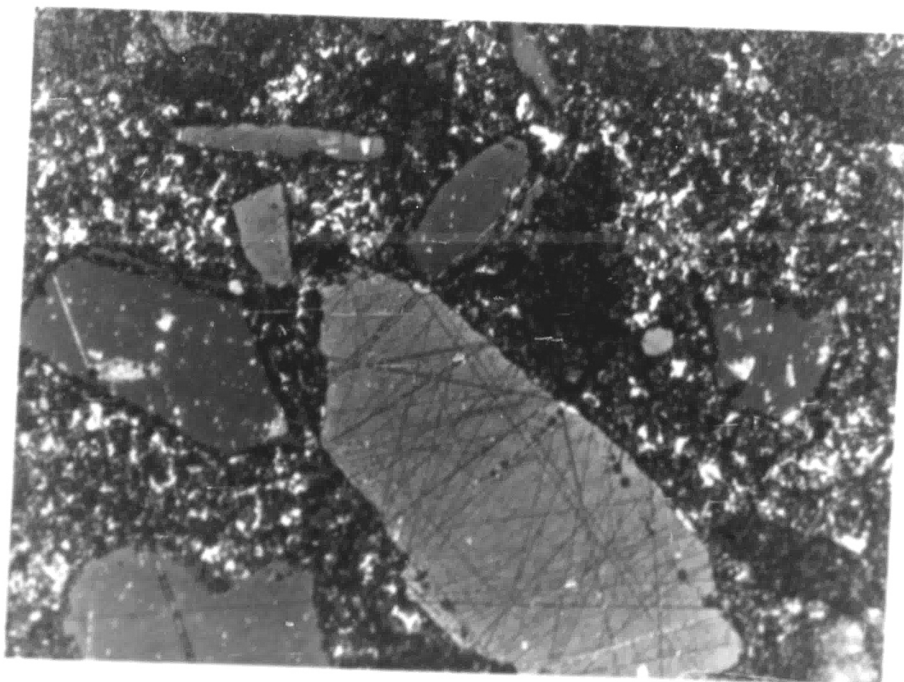


FIGURE 9. Optical Photograph of the SiC sample after being introduced to an ambient containing $N_2$, $O_2$, and Phosphorus Tribromide at 950°C. Magnification 500X.

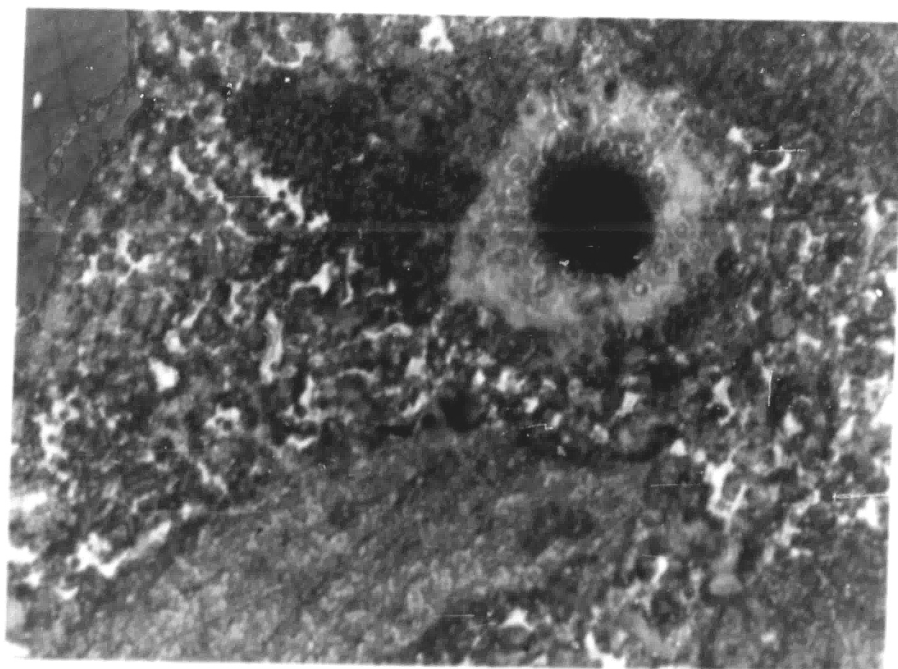


FIGURE 10. Optical Photograph of SiC sample after being introduced to an ambient containing $N_2$, $O_2$ and Phosphorus Tribromide. Magnification 500X.

Material Analysis Using NAA

The impurity concentration found in quartz, mullite and older SiC has been analyzed previously by Schmidt and Pearce (11). But only recently has the Crystar XP material been examined. Table 13 lists the impurities (in ppm) of the above components as well as the impurity concentration detected from samples taken from a (soon to be installed) Crystar XP liner. These latest NAA results were obtained by Filo (17).

Silicon Wafer Impurity Analysis

The NAA test previously done by Schmidt and Pearce (11) was repeated using the two double inlet high purity Crystar XP silicon carbide tubes. This test consisted of processing ten 125mm diameter wafers through these tubes. Prior to oxidation the wafers were cleaned in a standard $NH_4OH/H_2O_2/H_2O$, $HCL/H_2O_2/H_2O$, $HF/H_2O$ clean (13). Six wafers were processed in one tube, three with a 98% $O_2$ and 2% HCL ambient and three with a 100% $O_2$ ambient. After oxidation at 950°C, all six wafers were annealed insitu in nitrogen for ten minutes. Three additional wafers, which were processed in the second tube, were oxidized at 950°C in a steam ambient. The results of the NAA analysis on these nine wafers and on one unoxidized control wafer are shown in Table 14.

With the exception of the last column, Table 15 is a summary of the last eight tables (units in atoms/$cm^2$). This last column represents the average impurity concentrations on a typical wafer that has not gone through any furnace operation.

TABLE 13

IMPURITY CONCENTRATIONS (ppm) by NAA

| Element | Fused Quartz | Standard[1] Mullite | SiC[2] Liner 1982 | SiC[3] Liner 1983 |
|---|---|---|---|---|
| Cu | 1.45E-1 | | 0.17 | 3.75E-1 |
| Ta | 1.34E-3 | 3.6 | 0.003 | 7.72E-4 |
| W | - | 8.2 | - | - |
| Hf | 9.41E-2 | 6.2 | 0.31 | 1.94E-1 |
| Mo | - | - | 2.4 | 4.27E-1 |
| Br | - | - | - | - |
| As | - | - | - | - |
| Sb | 2.05E-3 | .77 | - | 1.27E-2 |
| Fe | 9.33E-1 | 8185 | 24.7 | 1.57E+1 |
| Sc | 2.13E-1 | 15.6 | - | 3.73E-2 |
| Co | 7.24E-4 | 5.7 | 0.17 | 1.14E-1 |
| Na | 1.54 | 980.0 | 85.1 | 1.86E-1 |
| Cr | 5.64E-2 | 62.9 | 0.37 | 3.97E-1 |
| Au | - | 0.12 | - | 1.40E-4 |
| Zr | 5.54 | 210 | 18.4 | 8.18E+0 |
| Zn | - | - | - | - |
| Ni | - | 9.4 | 12.3 | 6.62E+0 |
| K | 1.42 | 7570 | 32.9 | |
| Ca | - | 2200 | - | |
| Cs | - | 12.7 | - | |
| Ba | - | 152.3 | - | |
| Th | | | 0.74 | 5.24E-1 |
| U | | | | 6.82E-1 |

(-) defined as not detected

[1] From Table 6

[2] From Table 7

[3] Average of 6 pieces of 3 inch wide samples of the XP Crystar material that was cut from a soon to be installed liner. Results of analysis by A. Filo, reference (17).

TABLE 14

Impurity concentration per cc of wafer surface detected on furnace control wafers (125mm) processed in two separate silicon carbide tubes in MOS IVA in August of 1984.*

| Element | Control Wafer Clean Only | Oxidized in SiC Tube A1 No HCL | | | Oxidized in SiC Tube A1 with HCL | | | | Oxidized in SiC Tube B2 (Steam) | |
|---|---|---|---|---|---|---|---|---|---|---|
| Wafer # | 42 | 26 | 27 | 28 | 43 | 44 | 45 | 98 | 99 | 100 |
| Cu | 5.15E14 | 1.56E14 | 3.18E14 | 2.63E14 | 1.18E14 | 1.15E14 | 2.17E14 | 5.00E14 | 7.81E14 | 6.30E14 |
| Ni | 5.43E13 | 2.70E13 | 1.15E14 | 9.64E13 | 1.44E14 | 1.01E14 | 1.19E14 | 2.09E14 | 4.82E13 | 1.77E14 |
| Fe | 1.97E14 | 1.59E14 | 1.71E14 | 1.79E14 | - | 1.59E14 | 1.53E14 | 1.89E14 | 1.92E14 | 1.94E14 |
| Cr | 8.96E13 | 1.57E13 | 1.29E13 | 1.59E13 | 1.06E13 | 6.26E12 | 9.03E12 | 5.15E12 | 1.05E13 | 1.12E13 |
| Co | 3.10E12 | - | 2.80E13 | 1.82E13 | 2.08E12 | 1.77E13 | 2.04E13 | 2.97E12 | - | 1.86E12 |
| Au | 1.00E11 | 7.35E11 | 3.03E11 | 4.32E11 | 1.52E12 | 5.29E10 | 1.93E12 | 5.94E10 | 3.86E10 | 1.56E10 |
| Na | 6.63E15 | 1.36E15 | 2.49E15 | 1.46E15 | - | 2.54E14 | 1.15E15 | 1.66E15 | 1.44E15 | 6.11E14 |
| Sc | 3.46E10 | 1.11E11 | 1.26E11 | 1.21E11 | 7.48E10 | 7.81E10 | 1.14E11 | 4.88E10 | 3.35E10 | 3.37E10 |
| Zn | 1.52E13 | - | 2.26E14 | 5.37E13 | 9.27E13 | 3.73E13 | 4.82E13 | 4.07E13 | - | - |
| As | 6.56E12 | 1.13E12 | 3.76E12 | 5.31E11 | 4.92E12 | 8.95E11 | 1.87E12 | 2.93E12 | 2.13E12 | 1.17E12 |
| Sb | 4.49E11 | - | 2.13E11 | 1.00E14 | 7.62E13 | 3.92E11 | 3.94E11 | 7.68E11 | 1.11E12 | 3.13E11 |

*Analysis performed by A. Filo - BL-AL

TABLE 15

Summary of Neutron Activation Analysis of Wafers Processed With Furnaces With Various Tube Configurations
All Concentrations in Atoms/cm$^2$

| Element | Quartz/Mullite [1] 1974/75 DCL | Quartz/Mullite [1] 1974/75 MOS | Quartz/Mullite [1] 1977 DCL | SiC [2] Penn State 1983 | SiC [3] 1982 No HCL | SiC [3] 1982 HCL | Latest '84 SiC No HCL | Latest '84 SiC HCL | Latest '84 SiC Steam | Typical Wafer |
|---|---|---|---|---|---|---|---|---|---|---|
| Cu | 1.0E13 | 1.5E13 | 3.9E12 | 2E12 | 5.3E13 | 6.6E13 | 1.23E13 | 7.5E12 | 3.19E13 | 6E13 |
| Ni | 1.0E13 | 4.3E13 | 6.3E12 | 3E13 | 1.68E13 | 1.65E13 | 3.97E12 | 6.07E12 | 7.24E12 | 1.4E13 |
| Fe | 5.4E13 | 7.3E13 | 1.1E13 | 1.1E13 | - | - | 8.48E12 | 7.8E12 | 9.58E12 | Trace |
| Cr | 1.6E13 | 2.0E13 | 8.5E11 | 1.0E12 | - | - | 7.42E11 | 4.32E11 | 4.47E11 | 1.0E12 |
| Co | 1.7E11 | 2.4E12 | 2.3E11 | 4.8E12 | 4.57E11 | 4.33E11 | 1.16E12 | 6.7E11 | 1.21E11 | - |
| Au | 1.9E11 | 6.0E11 | 9.0E11 | 6.0E11 | 6.1E10 | 6.94E10 | 2.45E10 | 5.84E10 | 1.89E9 | - |
| Na | 8.3E12 | 2.4E13 | - | | 1.65E14 | 3.31E14 | 8.85E13 | 3.51E13 | 6.19E13 | - |
| W | | | | | - | 2.4E11 | - | - | - | - |
| Hf | | | | | 1.42E11 | 4.73E10 | - | - | - | - |
| Sc | | | | | 1.22E10 | 2.33E10 | 5.97E9 | 4.45E9 | 1.93E9 | |
| Zr | | | | | | 1.16E13 | - | - | - | |
| Zn | | | | | | 2.5E12 | 7.0E12 | 2.97E12 | 2.04E12 | |
| As | | | | | | | 1.81E12 | 1.28E11 | 1.04E11 | |
| Sb | | | | | | | 2.51E12 | 1.28E12 | 3.65E10 | |

[1] from Table 8   [2] from Table 10   [3] average concentration from Table 9

## Application to Device Processing

### Device Development

#### 64K DRAM

Three lots each containing fifty 100mm wafers were started in March of 1983. These lots were split at the four oxidation steps discussed previously. Half of each lot (wafers #1-25) were processed through the standard furnace operations using the conventional quartz tube and mullite liner. The balance of each lot was processed through the same operations using the high purity silicon carbide process tube.

Only one lot reached final test due to other processing problems. This lot reached primary test with 36 wafers. Of the 36 wafers, 21 were from the quartz/mullite half of the lot, the remaining 15 were from the silicon carbide processed half. The lot was tested and the control half averaged 4.5% better than the wafers processed through the silicon carbide tube. Although the yield on the silicon carbide half was lower, statistical analysis (T-test) showed that the difference was not significant.

#### 256K DRAM Device

The second series of experiments used 256K DRAM devices fabricated on 125mm diameter wafers. After each process was developed seven lots were started and processed through the two high purity silicon carbide tubes. The third SiC tube originally intended for the phosphorous diffusion operation was not used because of the microstructure analysis performed by Butler (15). Since this operation was deleted only 67% of the diffusion process steps were carried out in these two SiC tubes, the remaining steps were done in three conventional quartz tubes.

All furnace operations would have been done in SiC tubes had they been available. A summary of these seven silicon carbide processed lots is given in Table 16. With the exception of lot 2554, which had processing problems not associated with furnace operations all the lots achieved a satisfactory yield. Also included in this table are the start and finish (primary test) dates as well as the total number of wafers which reached primary test. Only seven wafers of lot 2575 reached primary test due to a problem with the hydrogen annealing furnace.

The average yield at primary test for SiC lots 2584 & 2585 averaged 10.48% better than forty-two control lots which started processing and reached final testing in approximately the same time period.

After these devices were fabricated and tested they were submitted for packaging. The packaged devices were then given nine hours of "pre-burn-in" and 500 hours of extended "burn-in". These "burn-in" tests are similar those desribed in Sze (18). The results showed 0.5% less failures from wafers processed through SiC tubes.

TABLE 16

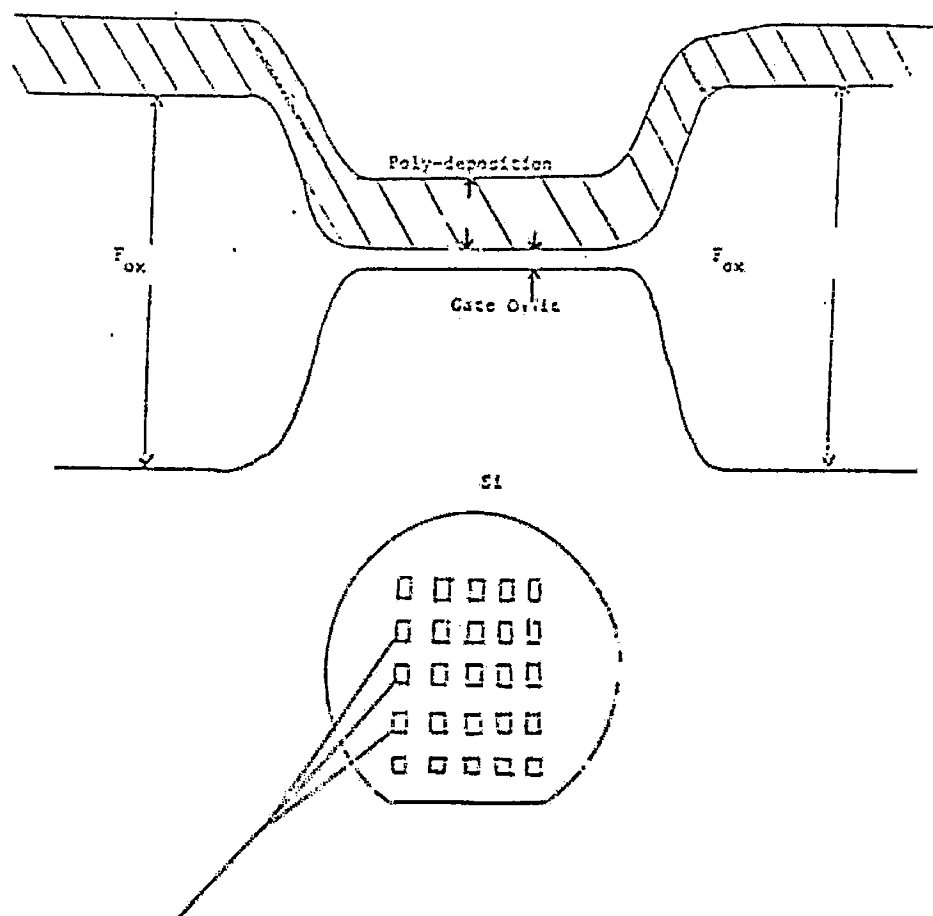
SUMMARY OF SILICON CARBIDE PROCESSED LOTS

| Lot ID | Date Started | Date at Primary Test | Number of Wafers at Primary Test |
|---|---|---|---|
| 2554 | 5-17 | 6-22 | 29 |
| 2555 | 5-17 | 6-11 | 35 |
| 2575 | 5-31 | 9-15 | 7 |
| 2578 | 6-2 | 7-24 | 16 |
| 2581 | 6-7 | 9-15 | 24 |
| 2584 | 7-12 | 9-17 | 36 |
| 2585 | 7-12 | 9-11 | 36 |

## Electrical Properties

### Oxide Integrity

The objective of this analysis was to compare the oxide integrity of thin oxides produced in high purity silicon carbide and quartz process tubes. The test structure for oxide integrity is an oxide, analogous to gate oxides, covered with a deposited polysilicon layer, doped with phosphorus, and then thermally oxidized in steam (see Figure 11). Therefore, two wafers were obtained from two lots processed through silicon carbide tubes after the polysilicon oxidation step. Eight wafers from different lots, which were processed in the standard quartz tubes, were also obtained after the same step. These 12 wafers were then combined and processed through the standard process operations to prepare the test structures for this specific test. Two specific measures of oxide integrity were determined: 1) The voltage required to produce a leakage current of 20 nA; and 2) a breakdown voltage, where breakdown is defined as the voltage at which 1uA of current flows through the oxide. Table 17 gives a statistical analysis of the 30 test structures evaluated on each wafer. The first two lots listed in the table were the silicon carbide lots. The remaining were processed in quartz tubes. The statistical results of Table 17 show no clear difference between wafers processed in silicon carbide or quartz process tubes.




Poly-deposition covers the whole chip; therefore all the gates on that chip are in parallel.

**Figure 11. Oxide Integrity Test Structure**

TABLE 17

OXIDE INTEGRITY ANALYSIS

Number of Samples for Each Wafer - 30

| Lot | Wfr ID | Leakage (20nA) Mean Bias | Leakage (20nA) Yield >10 V % | Leakage (20nA) Max Bias | Leakage (20nA) Yield >80% Max | Breakdown (1μA) Mean Bias | Breakdown (1μA) Yield >10 V % | Breakdown (1μA) Max Bias | Breakdown (1μA) Yield >80% Max | |
|---|---|---|---|---|---|---|---|---|---|---|
| 2554 | 17 | 13.1 $\pm$ 4.2 | 86.6% | 15.0 | 86.6% | 16.2 $\pm$ 4.6 | 86.6% | 19.0 | 83.3% | SiC Processed |
| | 37 | 12.8 $\pm$ 4.1 | 79.9% | 15.5 | 79.9% | 15.8 $\pm$ 4.3 | 86.6% | 19.0 | 76.6% | SiC Processed |
| 2555 | 25 | 13.0 $\pm$ 3.6 | 86.6% | 15.0 | 86.6% | 16.9 $\pm$ 4.6 | 89.9% | 19.5 | 86.6% | SiC Processed |
| | 09 | 14.4 $\pm$ 14.4 | 100.0% | 15.0 | 100.0% | 18.4 $\pm$ 1.1 | 100.0% | 19.5 | 93.3% | SiC Processed |
| | | $\bar{x}$ = 13.34 | | | | $\bar{x}$ = 16.88 | | | | |
| | | $\bar{\sigma}$ = 3.6 | | | | $\bar{\sigma}$ = 4.11 | | | | |
| F1563 | 08 | 13.0 $\pm$ 2.8 | 93.3% | 14.0 | 93.3% | 16.3 $\pm$ 3.2 | 93.3% | 17.5 | 93.3% | Quartz Processed |
| F1592 | 15 | 13.6 $\pm$ 1.2 | 96.6% | 14.0 | 93.3% | 15.8 $\pm$ 1.6 | 96.6% | 17.5 | 89.8% | Quartz Processed |
| 1613 | 33 | 11.6 $\pm$ 4.9 | 76.6% | 15.0 | 76.6% | 14.9 $\pm$ 5.4 | 79.9% | 20.0 | 76.6% | Quartz Processed |
| 1617 | 14 | 9.2 $\pm$ 5.9 | 66.6% | 14.5 | 66.6% | 12.6 $\pm$ 7.5 | 66.6% | 18.5 | 66.6% | Quartz Processed |
| 1617 | 42 | 14.0 $\pm$ 2.5 | 96.6% | 15.0 | 93.3% | 17.1 $\pm$ 3.1 | 96.6% | 18.5 | 93.3% | Quartz Processed |
| 1617 | 44 | 10.6 $\pm$ 5.0 | 69.9% | 14.0 | 69.9% | 14.1 $\pm$ 6.7 | 76.6% | 19.0 | 66.6% | Quartz Processed |
| 1619 | 44 | 12.7 $\pm$ 4.1 | 83.3% | 15.0 | 83.3% | 16.1 $\pm$ 4.3 | 89.9% | 18.5 | 86.6% | Quartz Processed |
| | | $\bar{x}$ = 12.16 | | | | $\bar{x}$ = 15.47 | | | | |
| | | $\bar{\sigma}$ = 4.45 | | | | $\bar{\sigma}$ = 5.12 | | | | |

## C-V Measurements

Capacitance voltage measurements were carried out on MOS capacitors in order to determine surface donor concentration, oxide fixed charge and flatband voltage shift due to bias-temperature stress. These values were determined through application of the equations explained in (19,20,21). Three separate methods were used to determine the above.

### Method I.

Sixteen control wafers were processed through the standard cleans prior to any furnace operation. Half of these wafers were oxidized using the two high purity silicon carbide process tubes discussed previously (one tube set up for dry oxidation, the other tube for steam oxidation) and the remaining half were oxidized in two quartz tubes with corresponsing process sequences. All sixteen wafers were then processed through the following six steps:

1) $N_2$ Anneal at 900°C, 30 minutes
2) Hydrogen Bake at 500°C, 2 hrs
3) Apply Photo-Resist
4) Buffered HF Clean to remove rear surface oxide
5) Chemical Clean used to remove Photo-Resist
6) Clean containing Sulfuric Acid and Hydrogen Peroxide

The wafers were then tested using a mercury probe, model 754, supplied by the Material Development Corporation (MDC). The results of these measurements are listed in Table 18.

Table 18

Capacitance Voltage Measurements Using Mercury Probe

| Wfr ID | DESC | $C_{Max}$ pf | $C_{Min}$ pf | $T_{ox}$ A | $W_{Max}$ | Doping Level | $C_{FB}$ pf | $V_{FB}$ V | $V_{th}$ V | $Q_{ss}$ ions/cm$^2$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 37 | S,S | 217.7 | 80.15 | 1228.9 | .650 | 1.91E15 | 174.20 | -2.12 | -.794 | 2.45E11 |
| 38 | S,S | 225.7 | 84.98 | 1185.7 | .602 | 2.24E15 | 182.12 | -1.83 | -.457 | 2.00E11 |
| 39 | S,S | 228.8 | 82.50 | 1169.7 | .635 | 1.98E15 | 181.94 | -1.74 | -.430 | 1.87E11 |
| 40 | S,S | 223.5 | 79.76 | 1197.3 | .660 | 1.82E15 | 177.02 | -1.70 | -.413 | 1.76E11 |
| 41 | Q,S | 169.0 | 66.60 | 1575.6 | .750 | 1.40E15 | 138.30 | -5.00 | -.367 | 5.80E11 * |
| 42 | Q,S | 183.3 | 80.40 | 1459.0 | .570 | 2.49E15 | 154.80 | -1.82 | -.216 | 1.62E11 |
| 43 | Q,S | 194.4 | 77.00 | 1376.0 | .640 | 1.93E15 | 159.20 | -1.90 | -.498 | 1.87E11 |
| 44 | Q,S | 199.3 | 80.50 | 1342.7 | .610 | 2.19E15 | 164.30 | -1.83 | -.374 | 1.78E11 |
| 45 | S,O | 397.6 | 102.00 | 673.07 | .598 | 2.27E15 | 280.30 | -1.70 | -.650 | 3.13E11 |
| 46 | S,O | 395.7 | 98.10 | 676.20 | .629 | 2.03E15 | 274.80 | -1.69 | -.670 | 3.11E11 |
| 47 | S,O | 391.6 | 101.28 | 683.29 | .600 | 2.25E15 | 276.90 | -1.73 | -.680 | 3.19E11 |
| 48 | S,O | 385.2 | 104.70 | 694.66 | .560 | 2.51E15 | 278.10 | -1.72 | -.634 | 3.109E11 |
| 49 | Q,O | 406.64 | 105.12 | 658.06 | .579 | 2.44E15 | 287.80 | -1.68 | -.622 | 3.14E11 |
| 50 | Q,O | 348.81 | 98.02 | 767.16 | .602 | 2.24E15 | 254.70 | -1.62 | -.510 | 2.52E11 |
| 173 | Q,O | 375.98 | 91.20 | 711.71 | .680 | 1.70E15 | 258.10 | -1.60 | -.610 | 2.69E11 |
| 174 | Q,O | 384.75 | 92.54 | 695.49 | .673 | 1.75E15 | 263.40 | -1.51 | -.510 | 2.45E11 |

where: S,S - SiC, Steam Oxide
S,O - SiC, Dry Oxide
Q,S - Quartz/Mullite, Steam Oxide
Q,O - Quartz/Mullite, Dry Oxide

* Wafer #41 was spotty, indicating non-uniform oxidation. It was probably a bad control wafer at the start.

Method II.

Wafers were processed in the same two high purity silicon carbide tubes and the same two quartz process tubes previously discussed. The actual process operations were identical to the first method with the exception of these additional steps after the hydrogen bake process:

1) Clean 15:1, $H_2O$:HF Solution
2) Aluminum Sputter
3) Apply Photo Resist
4) Expose, Bake, and Develop
5) Aluminum Wet Etch
6) Polysilicon Etch
7) Solvent Photo-Resist Strip
8) Aluminum Sputter (Backside Only)
9) Aluminum Sinter

With these additional steps a set of electrodes was photolithographically defined on each wafer. The final result was an array of aluminum electrodes each with an area of 2.2E-2 $cm^2$.

One capacitor near the center of each wafer was tested using a MDC C-V test set, model CSM-V-T2 . The results of this test are listed in Table 19.

TABLE 19

C-V Measurements on Aluminum Contacts 11/83

| Description | WfrID | $T_{ox}$ Å | $C_{Max}$ pf | $C_{Min}$ pf | $W_{Max}$ μ | $N_A$ x$10^{15}$ $cm^{-3}$ | $C_{FB}$ pf | $V_{FB}$ V | $V_{th}$ V | $Q_{ss}$ ions $cm^{-3}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | 31 | 961.71 | 779.75 | 233.86 | .688 | 1.66 | 581.3 | -1.43 | -.311 | 1.18E11 |
| Q,S | 32 | 941.96 | 796.14 | 237.67 | .6783 | 1.72 | 592.72 | -1.16 | -.039 | 5.87E10 |
| | 33 | 988.51 | 758.65 | 222.58 | .7297 | 1.46 | 560.23 | -2.62 | -1.52 | 3.7E11 |
| | 40 | 548.8 | 1366.41 | 259.39 | .7179 | 1.52 | 840.0 | -1.02 | -.136 | 4.58E11 |
| S,S | 41 | 589.89 | 1271.31 | 257.98 | .7102 | 1.56 | 806.58 | -1.37 | -.465 | 1.70E11 |
| | 42 | 601.06 | 1247.68 | 245.24 | .7530 | 1.37 | 778.4 | -1.33 | -.449 | 1.55E11 |
| | 43 | 906.57 | 827.22 | 218.69 | .7732 | 1.29 | 586.07 | -1.50 | -.480 | 1.41E11 |
| Q,O | 44 | 889.72 | 842.79 | 215.19 | .7954 | 1.21 | 588.39 | -1.37 | -.378 | 1.14E11 |
| | 45 | 863.9 | 868.04 | 194.36 | .9178 | 8.86 | 570.62 | -1.47 | -.567 | 1.44E11 |
| | 48 | ←-------------------Broken While Processing----------------------→ | | | | | | | | |
| S,O | 49 | 668.1 | 1122.5 | 256.3 | .692 | 1.65 | 751.12 | -1.97 | -.1007 | 3.40E11 |
| | 50 | 621.9 | 1205.9 | 263.5 | .682 | 1.70 | 791.95 | -1.65 | -.703 | 2.5E11 |

Where: Q,S - Quartz, Steam Oxide S,S - SIC, Steam Oxide
Q,O - Quartz, Dry Oxide S,O - SIC, Dry Oxide

Measurements using a MDC CV Test Set, Model CSM-V-T2

Method III.

A bias-temperature stress test was carried out on test capacitors on five 125mm finished device wafers processed through the 256K Dynamic RAM process. Three of the five wafers were processed using the two high purity silicon carbide tubes previously discussed. The remaining two wafers were from a lot that was processed in the conventional quartz tubes.

The actual test consisted of a standard high frequency C-V measurement on three gate contacts on each wafer in three different conditions:

Condition 1) Measure and plot C-V curve at room temperature (25oC).

Condition 2) Remeasure C-V curve at room temperature after the wafers were heated to 250oC, held for ten minutes, and cooled to room temperature, all with a +10 volt bias applied.

Condition 3) Remeasure C-V curve at room temperature after the wafers were reheated to 250oC, held for ten minutes, and cooled back to room temperature, all with a -10 volt bias applied.

A C-V plot of each of the gate contacts for each of the five device wafers is given in Figures 12 to 16. The initial C-V test results was analyzed to give the doping concentration ($N_a$); flatband voltage ($V_{FB}$) or surface charge density ($Q_{ss}$) and oxide thickness ($T_{ox}$) using a Hewlett Packard HP 9836 computer running a 6940B HP multi programmer. The MOS test set, [configured by T. D. Jones (BL)], consisted of a CV Plotter, model 410, manufactured by (EG&G) Princeton Applied Research and a thermochuck system manufactured by Temptronics.

The results of these CV measurements are listed in Table 20. The bias-temperature flatband voltage shift ($\Delta V_{FB}$) was also determined according to the relation:

$$\Delta V_{FB} = V_{FB}\ (-10V,\ 250^{o}C) - V_{FB}\ (+10V,\ 250^{o}C).$$

The average flatband voltage shift ($\Delta V_{FB}$) for each wafer was also calculated and listed in Table 21. Only one wafer, 2581-31 had a positive $\Delta V_{FB}$. Whether this value is significant or not could only be determined after further CV analysis and reliability testing. Since the yield at primary test on this particular lot was reasonably good, and since the average $\Delta V_{FB}$ on the standard processed lots was .013V, the .02V value is probably not significantly different.

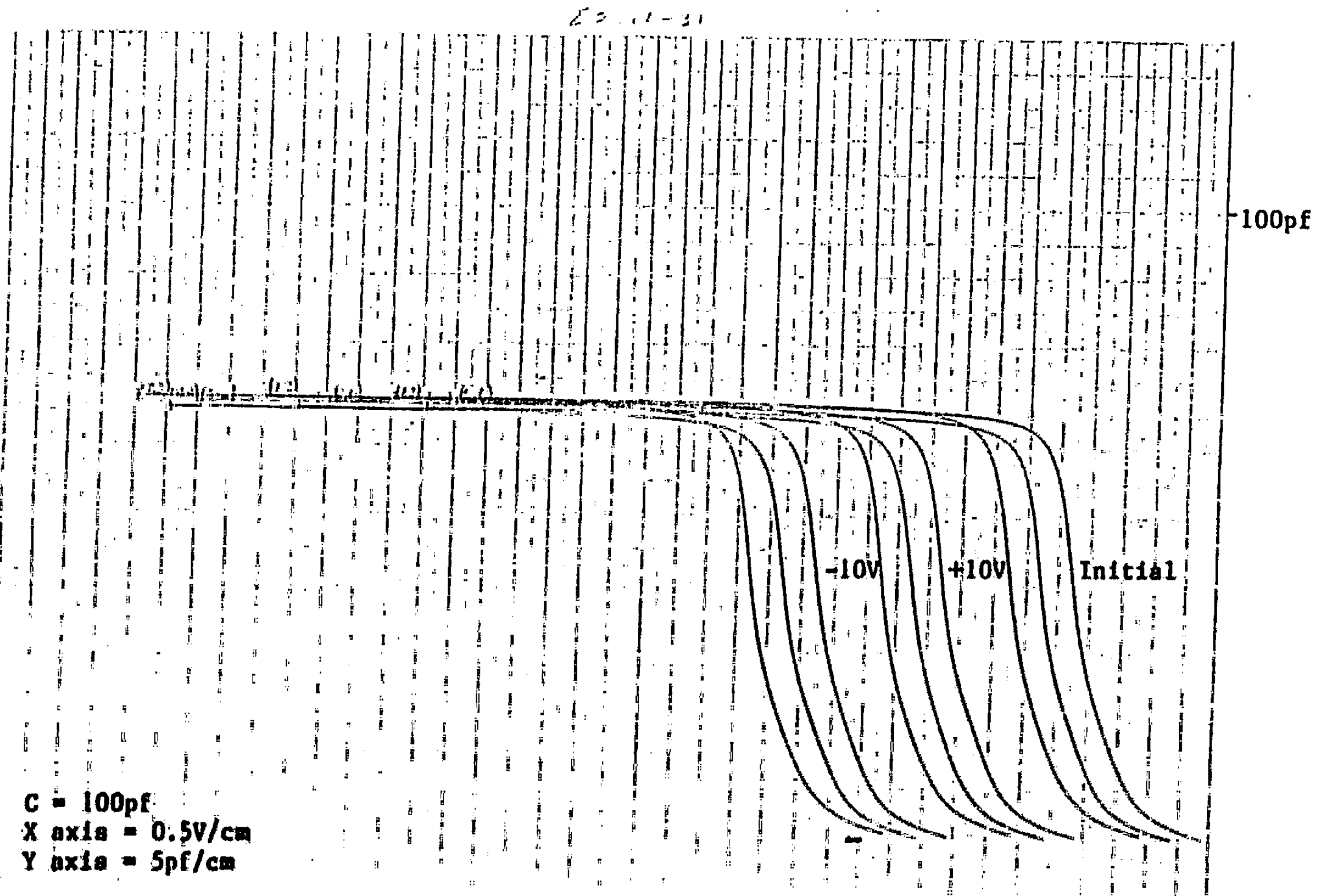



**Figure 12. Bias-Temperature Stress Test**
**Wafer 2581-31 (SiC)**

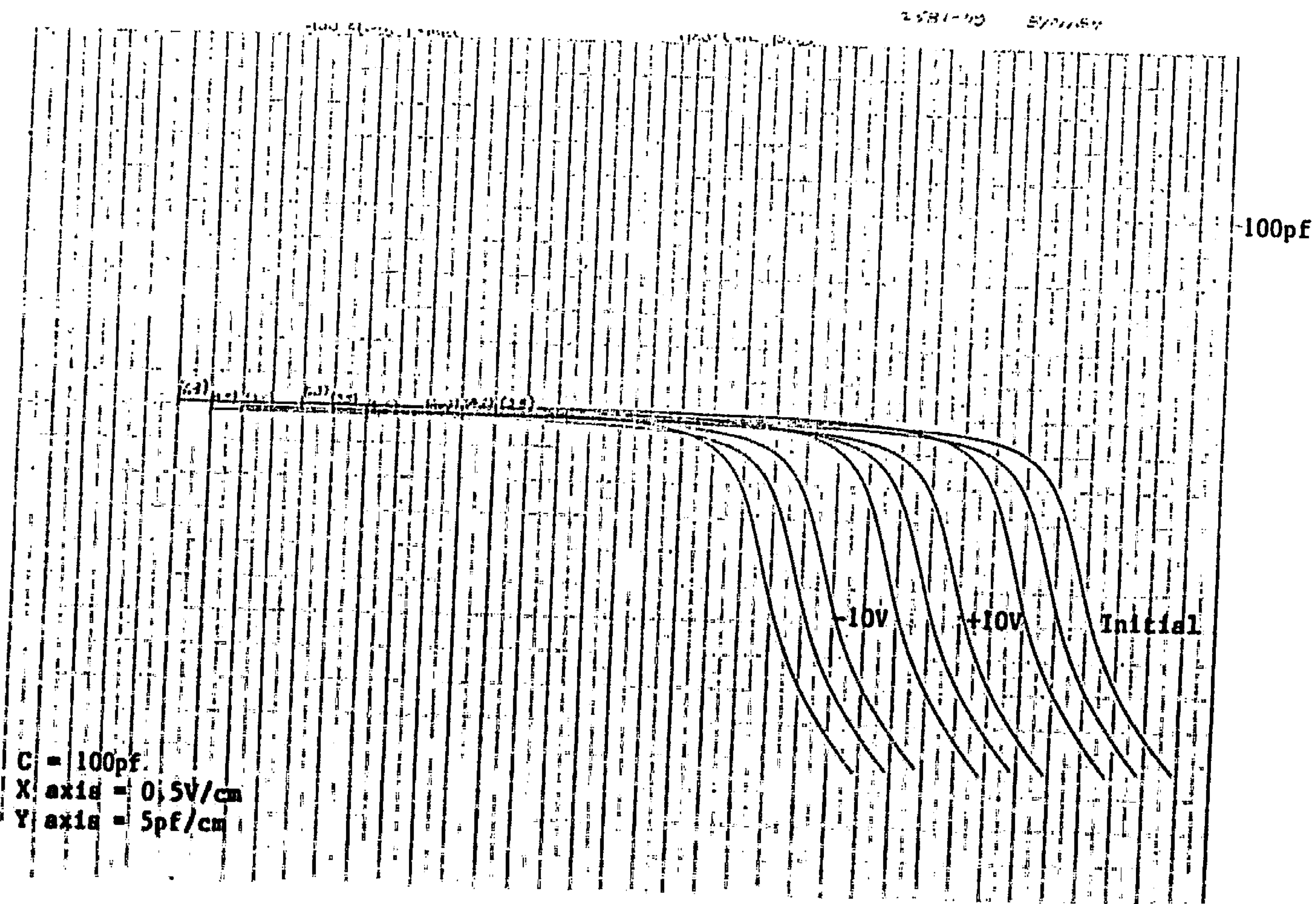



Figure 13. Bias-Temperature Stress Test
Wafer 2581-49 (Sic)

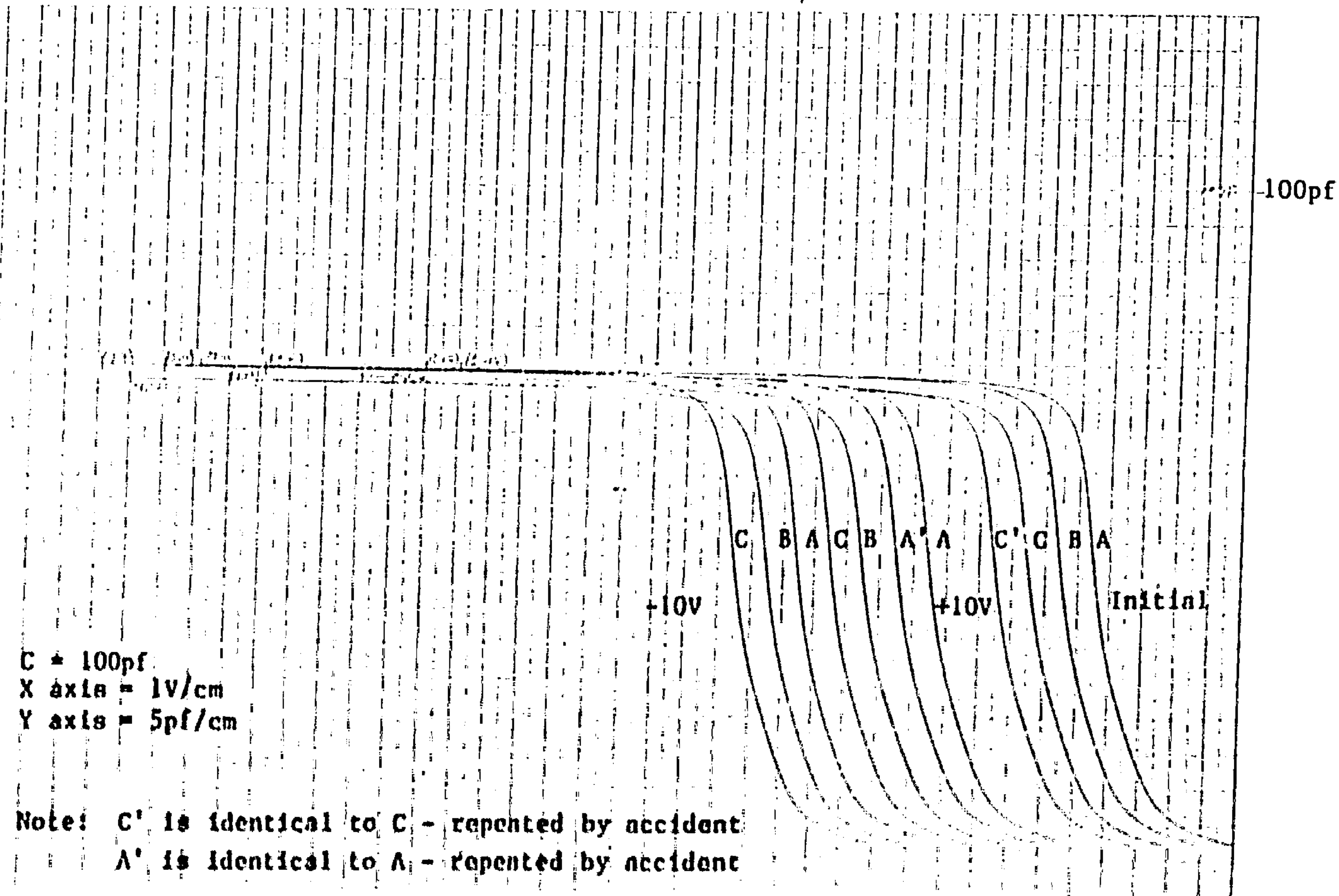



Figure 14. Bias-Temperature Stress Test
Wafer 2585-24 (SiC)

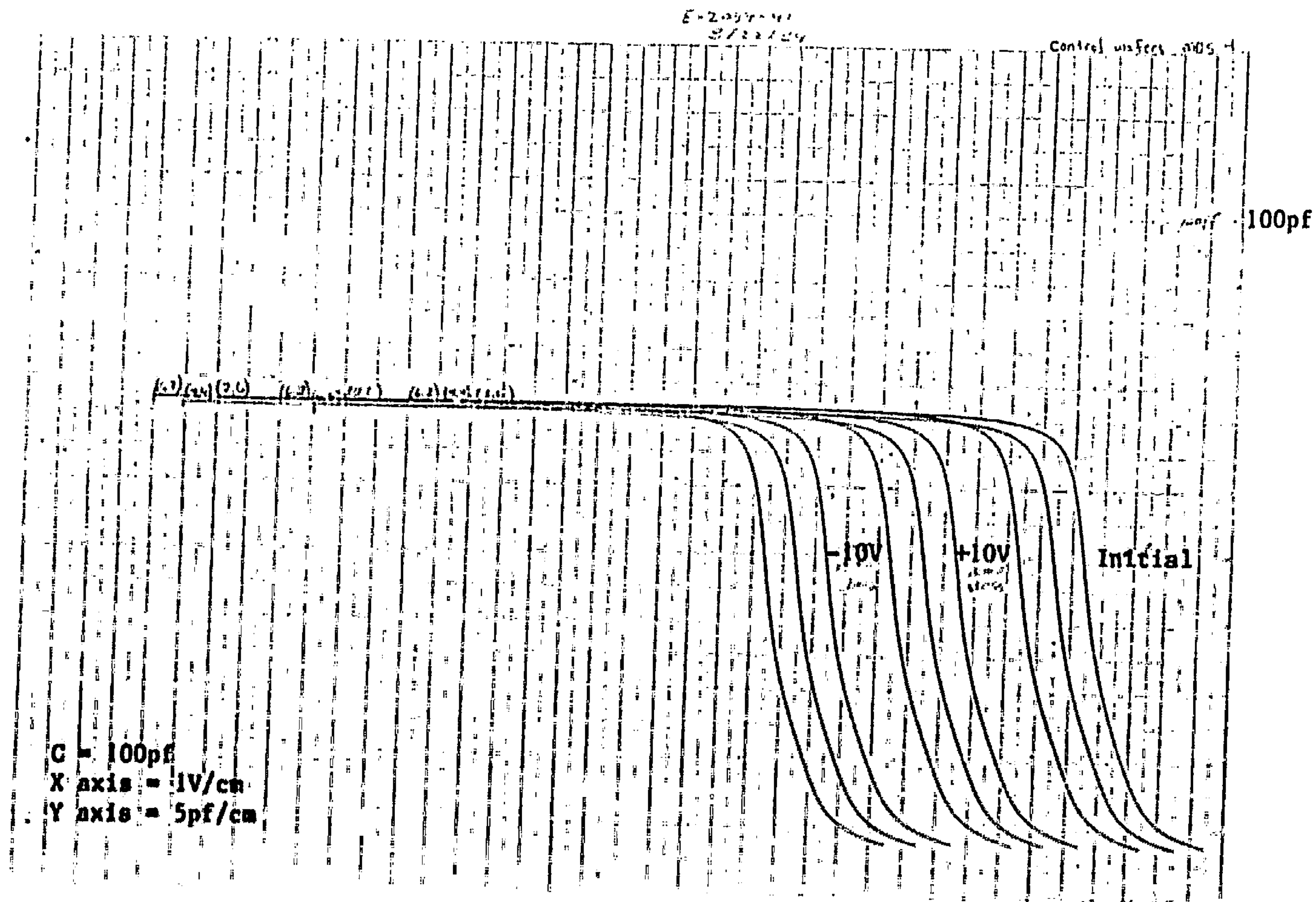



**Figure 15. Bias-Temperature Stress Test**
**Wafer 0259-41 (Quartz)**

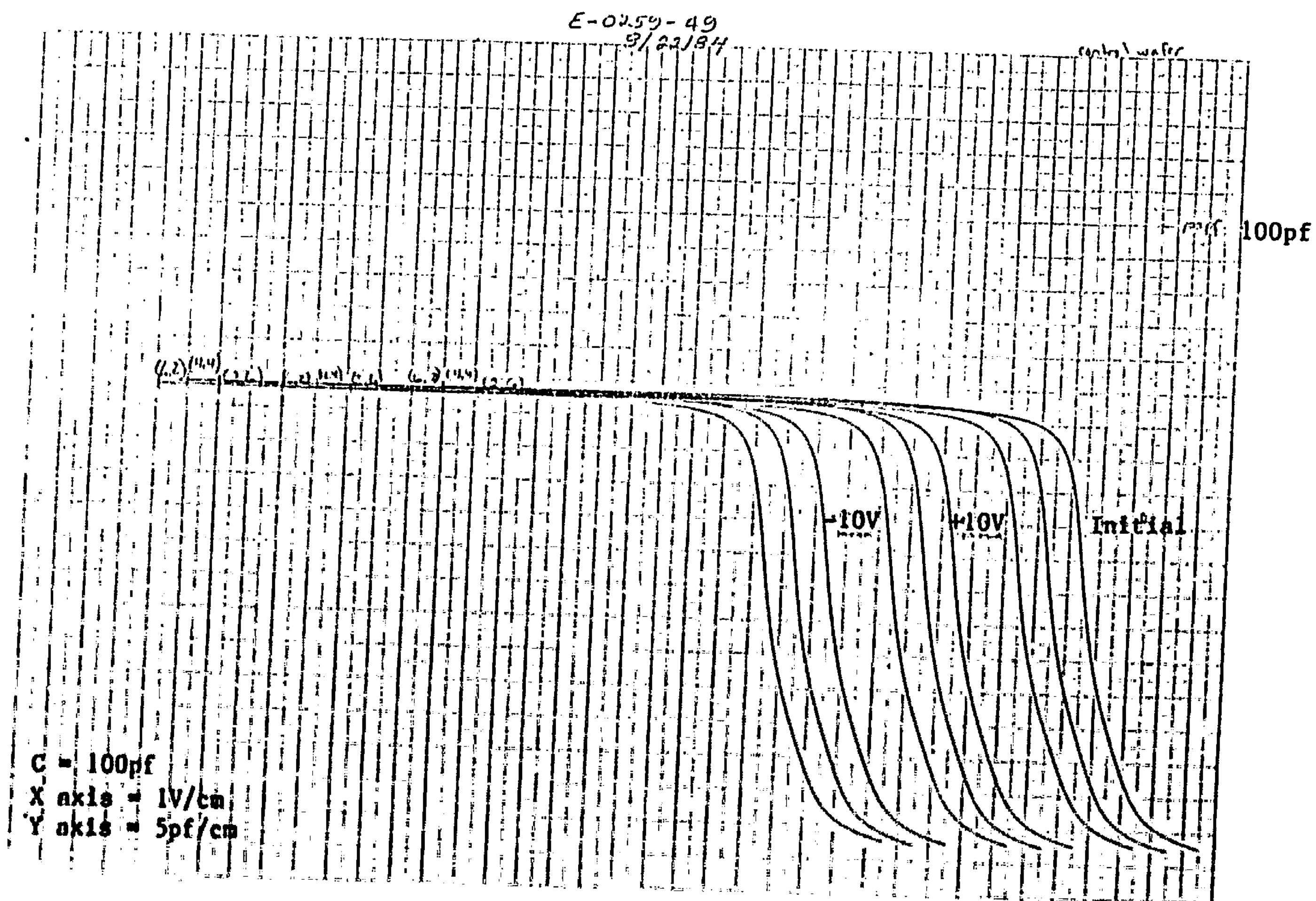



**Figure 16. Bias-Temperature Stress Test Wafer 0259-41 (Quartz)**

TABLE 20
Bias-Temperature Stress Test*

| Lot - Wfr ID | Dot | Pre-Stress (25°) Doping Level (ions/$cm^3$) | $V_{FB}$ (V) | $Q_{ss}$ (ions/$cm^2$) | $T_{ox}$ (Å) | +10V Bias after 250°C for 10 min Doping Level (ions/$cm^3$) | $V_{FB}$ (V) | $Q_{ss}$ (ions/$cm^2$) | $T_{ox}$ (Å) | -10V Bias after 250°C for 10 min Doping Level (ions/$cm^3$) | $V_{FB}$ (V) | $Q_{ss}$ (ions/$cm^2$) | $T_{ox}$ (Å) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (SiC) 2581-31 | (2,6) | 7.64E15 | -.85 | -4.57E9 | 511 | 7.93E15 | -.86 | -7.45E8 | 511 | 7.23E15 | -.85 | -3.95E9 | 512 |
| | (4,4) | 7.2E15 | -.84 | -8.03E9 | 518 | 7.37E15 | -.84 | -8.27E9 | 518 | 7.37E15 | -.86 | 5.28E7 | 518 |
| | (7,3) | 7.37E15 | -.80 | -2.55E10 | 507 | 7.38E15 | -.80 | -2.55E10 | 507 | 7.59E15 | -.83 | 1.30E10 | 507 |
| (SiC) 2581-49 | (2,5) | 7.8E15 | -.82 | -1.71E10 | 520 | 7.72E15 | -.82 | -1.7E10 | 520 | 7.6E15 | -.83 | -1.48E10 | 520 |
| | (4,5) | 7.3E15 | -.80 | -2.67E10 | 523 | 7.3E15 | -.80 | -2.67E10 | 523 | 7.22E15 | -.81 | -2.24E10 | 523 |
| | (6,3) | 7.3E15 | -.81 | -2.08E10 | 514 | 7.21E15 | -.81 | -2.38E10 | 514 | 7.16E15 | -.82 | -1.64E10 | 514 |
| (SiC) 2585-24 | (2,18) | 7.29E15 | -.78 | -3.49E10 | 492 | 7.4E15 | -.78 | -3.5E10 | 493 | 7.4E15 | -.80 | -2.63E10 | 492 |
| | (4,12) | 7.28E15 | -.77 | -3.83E10 | 504 | 7.29E15 | -.78 | -3.4E10 | 505 | 7.45E15 | -.78 | -3.43E10 | 505 |
| | (7,9) | 7.39E15 | -.76 | -4.31E10 | 501 | 7.22E15 | -.76 | -4.36E10 | 491 | 7.32E15 | -.77 | -3.9310 | 491 |
| (Quartz) E0259-41 | (2,6) | 6.23E15 | -.74 | -4.92E10 | 506 | 7.26E15 | -.76 | -4.24E10 | 506 | 7.26E15 | -.78 | 3.39E10 | 506 |
| | (4,4) | 7.05E15 | -.75 | -4.60E10 | 510 | 7.16E15 | -.75 | -4.6E10 | 511 | 7.16E15 | -.76 | 4.19E10 | 510 |
| | (6,2) | 6.97E15 | -.75 | -4.64E10 | 504 | 6.98E15 | -.75 | -4.6E10 | 504 | 6.98E15 | -.76 | 4.21E10 | 504 |
| (Quartz) E0259-49 | (2,6) | 6.8E15 | -.76 | -4.24E10 | 497 | 6.9E15 | -.76 | -4.27E10 | 497 | 6.83E15 | -.78 | 3.39E10 | 497 |
| | (4,4) | 6.9E15 | -.75 | -4.73E10 | 493 | 7.04E15 | -.75 | -4.75E10 | 493 | 6.94E15 | -.76 | -4.30E10 | 493 |
| | (6,2) | 7.2E15 | -.77 | -3.87E10 | 498 | 7.25E15 | -.77 | -3.88E10 | 498 | 7.25E15 | -.78 | -3.44E10 | 498 |

*Analysis performed by T. Jones - BL-AL

TABLE 21

Bias-Temperature Flatband Voltage Shift

| Lot Wfr ID | Dot | $\Delta V_{FB}$ Volts | Mean $\Delta V_{FB}$ Volts | $\sigma$ |
|---|---|---|---|---|
| | (2,6) | +.01 | | |
| 2581 - 31 | (4,4) | -.02 | .02 | .02 |
| | (7,3) | -.03 | | |
| | (2,5) | -.01 | | |
| 2581 - 49 | (4,5) | -.01 | .01 | 0 |
| | (6,3) | -.01 | | |
| | (2,18) | -.02 | | |
| 2585 - 24 | (4,12) | 0 | .01 | .01 |
| | (7,9) | -.01 | | |
| | (2,6) | -.02 | | |
| E0259 - 41 | (4,4) | -.01 | .013 | .006 |
| | (6,2) | -.01 | | |
| | (2,6) | -.02 | | |
| E0259 - 49 | (4,4) | -.01 | .013 | .006 |
| | (6,2) | -.01 | | |

# V. DISCUSSION AND CONCLUSION

## Material and Silicon Wafer Analysis

### Neutron Activation Analysis

Table 14 shows the NAA results of nine wafers that were oxidized in the two high purity silicon carbide tubes and one unoxidizd control wafer. Notice that the $O_2$-HCL data versus the $O_2$ data is similar except in the case of sodium. Here the average sodium concentration is lower in the wafers that had been run with the $O_2$-HCL ambient, but only by a factor of 2. Also note that there is little difference between the results of the steam versus the dry oxidations.

The first column shows the data from the control wafer that was cleaned with the original nine wafers, but had not seen any furnace operation. Comparing the results in column 1 to the results in columns 2 through 9 one can see that there is no significant difference in impurity level and in general there is a small decrease. Therefore the furnace operation, when using a silicon carbide tube, is not the contaminating step. The contamination seen on the control wafer could originate from chemical cleans or possibly from any prior operation.

Table 15 summarizes the NAA results from Schmidt (10), Pearce and Schmidt (11), Foster and Tressler (12) and the NAA results from above. Also included in this table is the average impurity concentration on a typical wafer that has not seen any furnace operation.

In comparing all these results the following conclusion can be made. Wafers processed through silicon carbide process tubes exhibit approximately the same or lower impurity concentrations as wafers processed in the standard quartz tube and mullite liner combination. And further, from the NAA analysis performed by Filo (19) on the most recent Crystar XP material one can conclude the purity of silicon carbide liners and process tubes is far superior to the standard mullite or the high purity $Al_2O_3$ or SiC liners previously analyzed.

## Process Development

### Furnace Parameter Evaluation

The programs developed for the silicon carbide tubes were very similar to the already developed programs for the quartz tubes. Insertion and withdrawal times, flow rates and times at maximum temperature either did not change or changed negligibly. The only major difference between the two process sequences was the shift in idle or starting temperatures. These shifts were in the range of $\pm$ 10°C. This difference can be attributed to the positions of the profile thermocouples. The thermocouples for the SiC tube were located inside the tube compared to the thermocouples used for the quartz/mullite system, where the profile thermocouples were located between the mullite liner and quartz tube.

## Thermal Characteristics

### Transient Behavior

From the plots in Figures 5A, 5B, and 5C one sees that the silicon carbide tube has a better transient temperature response than the quartz tube/mullite system. This is especially apparent in Figure 5B. The temperature of the center zone, as wafers are inserted into the SiC tube drops only 12.1$^{o}$C compared to a 46.7$^{o}$C drop in temperature for the center zone of the quartz tube. Notice that as the ramp period ends, the center zone temperature in the SiC tube slightly exceeds the peak temperature (1000$^{o}$C), but recovers in eight minutes. With the quartz tube, the temperature does not even reach this peak value until twelve minutes after the ramp period ended. Also notice that in all three figures, the SiC tube ramps down in temperature at a faster rate than the quartz tube. This can be attributed to the greater emissivity value for SiC (see Table 1). Therefore the final result is a more uniform temperature distribution and hence a uniform oxidation.

### Static Behavior

Figure 6 clearly illustrates that the better thermal conductivity of SiC compared to quartz results in an enlarged flat zone. This important property coupled with the higher emmisivity value shows how temperature gradients can be reduced and recovery times decreased. Therefore, because of the higher thermal conductivity and higher emmisivity in SiC components, better process uniformity and possibly increased wafer capacity can be achieved.

## Application To Device Processing

### Electrical Properties

#### Oxide Integrity

Although the sample population used in the experiment was small the result showed no indication of any problems associated with the gate oxides grown in SiC process tubes. This has been confirmed by results from a number of lots which have subsequently been processed through these tubes and achieved satisfactory yields.

#### C-V Measurements

The C-V analysis carried out in methods I & II, Tables 18 and 19, showed no clear difference between wafers processed in each tube. It also showed no difference in measurements taken from wafers processed in either dry or steam oxidations for either quartz or SiC tubes.

The only noticeable difference was in the $Q_{ss}$ values attained in methods I & II compared to the $Q_{ss}$ values attained in method III, Table 20. The values in method III were a factor of 10 lower than the values from method II. The reason for this difference is not understood.

In comparing these results it is important to realize that different metal contacts have been used on the surface of the wafer. In method I, the measurements were made on a bare silicon surface using a mercury probe. In method II, the measurements were made on aluminum contacts which have been sintered. And finally in method III, the measurements were made on gate contacts of finished device wafers. These gate contacts were covered with a polysilicon layer and subsequently saw a sequence of high temperature furnace operations.

Since the results from method III show no significant difference in the CV measurements taken on wafers processed in either tube we can conclude that SiC tubes can be substituted for the quartz/mullite system.

## Yield on Devices and Reliability

The resulting 10.48% increase in device yield and the favorable reliability results, from the two lots processed through SiC tubes, show the definite feasibility of substituting SiC for quartz tubes.

## VI. Summary

We have shown that high purity silicon carbide process tubes and paddles can be used as a furnace material in MOS furnace processing. The high purity, high resistance to thermal shock, and high thermal conductivity are important parameters which enable these components to withstand high temperatures and exhibit long lifetime. 256K DRAM devices have been fabricated using two silicon carbide process tubes and paddles, with better than average yield and reliability results. Finally, since there is a long range cost savings in using these high purity components it is concluded that silicon carbide process tubes and paddles should be substituted for the quartz and mullite liner configuration, except were the phosphorus diffusion operations are used.

## REFERENCES


1. Johnson, E. A., Kocher, H. S., and Pearce, C. W. "A Study of Power Line Disturbances at the Orlando Plant Site," Unpublished Technical Memorandum, AT&T Technologies, Inc., June 19, 1981.

2. Schmidt, P. F. "Furnace Contamination and Its Remedies" Solid State Technology, June 1983, p. 150.

3. Pearce, C. W. "Defect and Contamination Control in VLSI Fabrication Processes," Semiconductor Processing and Equipment Symposium, March 1983, p. 293.

4. Private Communication, C. W. Pearce.

5. Butler, G. M. "The Past and Future of Silicon Carbide," J. Electrochem Soc., 104 {10} pp. 640-644 (1957).

6. Ibid., p. 643.

7. Sze, S. M. Physics of Semiconductor Devices, John Wiley and Sons, New York, p. 27.

8. Schmidt, P. F. "Contamination-Free High Temperature Treatment of Silicon or Other Material," J. Electrochem Soc., January 1983, p. 196.

9. Pearce, C. W. and Kannan, V. D. "Saucer Pit Defects in Silicon," Proceedings of the Electrochemical Soc., Vol. 83-9, 1983, p. 396.

10. Schmidt, op. cit., pp. 147-151.

11. Schmidt, P. F. and Pearce, C. W. "A Neutron Activation Analysis Study of the Sources of Transition Group Metal Contamination in the Silicon Device Manufacturing Process," J. Electrochem, Soc., Vol. 128, pp. 630-637, 1981.

12. Foster, B. D. and Tressler, R. E. "Silicon Processing with Silicon Carbide Components," Solid State Technology, October 1984, p. 143.

13. Kern, W. "Radiochemical Study of Semiconductor, Surface Contamination I. Adsorption of Reagent Components," RCA Review, June 1970, p. 207.

14. Pearce, C. W. and Kannan, V. C. op. cit., pp. 396-405.

15. Butler, S. R. "Evaluation of Silicon Carbide Diffusion Components," Unpublished paper, AT&T Technologies, Inc., June 1984.

16. Costello, J. A. "Kinetics of and Microstructural Changes During Oxidation of Silicon Carbide," Unpublished Ph.D Dissertation, Pennsylvania State University, March 1983.

17. Filo, A., Unpublished data, Bell Labs, October 1984.

18. Bertram, W. J. "Yield and Reliability" in VLSI Technology edited by S. M. Sze, McGraw-Hill Book Company, New York, 1983.

19. Zaininger, K. H. and Heiman, F. P. "The C-V Technique as an Analytical Tool," Solid State Technology, May 1970, p. 49.

20. Berman, A. and Kerr D. "Inversion Charge Redistribution Model of the High-Frequency MOS Capacitance," Solid State Electronics, Vol. 17, 1974, pp. 735-742.

21. Gordon, J. "On-Line Capacitance - Voltage Doping Profile Measurement of Low-Dose Ion Implants," IEEE Transactions on Electron Devices, Vol. ED-27, No. 12, December 1980, pp. 2268-2272.

# VITA

Robert W. Schanzer was born to Mr. and Mrs. George O. Schanzer on May 20, 1958 in Jericho, New York. He received his secondary education at Amherst High School, Snyder, New York, graduating in June of 1976. In the fall of 1976 he entered the State University College at Potsdam, Potsdam, New York, and graduated magna cum laude with a Bachelor of Arts in Physics in May, 1980. While at the University, he was a member of IEEE and helped organize a chapter of The Society of Physics Students.

Since June, 1980, he has been employed by AT&T Technologies, Inc. (the former Western Electric) as an Engineering Associate. In September, 1980, he continued his graduate education in the Department of Electrical Engineering at Lehigh University, his education being funded by the Tuition Refund Program of AT&T.