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PIN DIODE CHARACTERIZATION STUDIES

by
Jia-Ming Li

A THESIS

Presented to the Graduate Faculty

of Lehigh University

in Candidacy for the Degree of

Master of Science

Lehigh University

1967

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science.

May 23, 1967
(date)

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Professor in Charge

Head of the Department
of Electrical Engineering

Acknowledgement

I would like to thank Dr. Daniel Leenov for his assistance and direction in the experimental application, theoretical development, and actual writing of this paper. Without his assistance this project could not have been completed.

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PIN DIODE CHARACTERIZATION STUDIES

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Jia-Ming Li

Abstract

Conversion efficiency, rectified current and impedance of a PIN diode were measured by using coaxial circuitry and slotted line in the microwave region. Conversion efficiencies were measured as a function of frequency at forward and reverse bias. The results indicate a distinct difference in the charge storage mechanisms responsible for the capacitance of the device in the two bias conditions. At forward bias the capacitance is due to carrier storage in the I region while at reverse bias it is due to the depletion capacitance. Rectified current was found to be approximately directly proportional to the signal input power and inversely proportional to signal frequency. The conversion efficiency was found to be a function of the bias current for forward D.C. bias, and dependent on the voltage for reverse D.C. bias. Impedance was found as a function of frequency and bias. D.C. bias current was shown to be much more effective than high frequency current for injecting carriers into the I layer.

I. Introduction

The silicon PIN diode has a considerable number of microwave applications due to its variable impedance. This device consists of a sandwich structure with two junctions, one a P^+I junction, the other a N^+I, (Figure 1), the P^+ region and N^+ region are highly doped (low resistivity), the I region has low impurity concentration (high resistivity). Its importance for high frequency applications lies in its variable resistance and charge storage properties. The resistance of the diode can be changed by independently varying the forward bias current, which controls the amount of stored charge in the I layer; therefore, the diode can function as a switch, variable attenuator, and modulator. Similarly, the variable capacitance of the diode is a function of the applied signal, hence it can be used for frequency conversion (frequency multiplication, division, and mixing).

To understand the basis of these properties consider the effect of applying a forward bias and reverse bias to the PIN diode. At forward bias, the I layer is filled with an equal number of holes and electrons injected by the highly doped P^+ and N^+ regions. At any level of constant current the concentration of carriers in the I layer reaches a steady value, at which the rate of recombination of holes and electrons equals the rate at which they are supplied by the applied current. At appreciable currents the number of injected charge carriers in the I region is very large as compared to the zero bias equilibrium concentrations, (Figure 2); and thus, according to the equation $R = \rho \frac{t}{A}$ (where ρ, t, and A are resistivity, uniform thickness, and uniform cross-sectional area of the I layer, respectively), the resistivity of

this region is considerably reduced; hence the resistance of the device can be varied by changing the applied current. The capacitance at forward bias is due to carriers (equal number of holes and electrons) in the I layer; therefore, the capacitance is considerably increased with increasing bias current.

At reverse bias the capacitance is due to the depletion layer. This layer in the PIN diode is the width of the I layer for a true I region, (Figure 3), otherwise the width of the depletion layer is usually less than the width of the I layer; and is a function of the reverse bias voltage. It does not appreciably penetrate the N or P region, because they are highly doped. The width is given by

$$W = \left[\frac{2\varepsilon}{qN_i} (\psi_0 - V) \right]^{1/2}$$

where

ε = dielectric constant of the semiconductor

N_i = concentration of impurity atoms in the I region

V = applied voltage

ψ_0 = contact potential or built-in voltage of the junction

The depletion layer capacitance is related to the applied voltage V by

$$C = \frac{\varepsilon A}{W} = A \left[\frac{q\varepsilon N_i}{2} \frac{1}{\psi_0 - V} \right]^{1/2}$$

This paper is concerned with the characteristics of the PIN diode, and is divided into two parts. The first part concerns the measurement of efficiency of frequency conversion; the second part the impedance and rectified current. The purpose of this work is to obtain information on the dependence of frequency conversion efficiency on

bias and signal level.

Two circuits [coaxial circuitry, (Figure 4), and slotted line, (Figure 5)] were designed for measurement of conversion efficiency, rectified current and impedance for this paper. Frequencies in the range from 200 MHz to 700 MHz were used for the first part, and from 50 MHz to 400 MHz for the second part.

The same PIN diode (0-98) was used for all experimental results.

II. Measurements

A. The circuit for the measurement of efficiency conversion

The circuit shown in Figure (4) was used for measuring the efficiency of frequency conversion. The high pass filter at the input was selected to pass only the generator frequency, the low pass filter at the output passed only the subharmonic (approximately one-half the input frequency) to the load. The tuning elements were placed between the generator and the diode for the impedance matching at the input frequency. At the other end of the diode, an adjustable line and stub matched the subharmonic (half-harmonic) to the low pass filter from the diode.

The diode was biased by the D.C. supply, using an r.f. choke for isolation. The bias voltage and current were measured by the meter in the D.C. supply. A coupling capacitor served to isolate the bias circuit from the load. The bias (positive or negative) was adjusted for maximum output. A slight deviation from optimum bias caused a sharp drop in output power. Measurements were made at three levels of input power.

B. Impedance and rectified current

1. Circuit for measurements

The circuit of Figure (5) was used for measurements of impedance and rectified current. The signal source consisted of an X-band klystron (10.8 GHz), which was amplitude modulated at the operating frequency of the standing wave indicator. Generally, square wave

modulation is used which reduces to a minimum the effects of harmonics and frequency modulation. An isolator was used to eliminate reflections from the load. A length of X-Band waveguide was used between klystron and isolator in order to prevent the magnetic interference from isolator to klystron. A directional coupler was used to separate the S.H.F. signal into two paths; one path through frequency meter, crystal detector and oscilloscope for frequency measurement, the other path through a variable attenuator to the slotted section. The attenuator changes the amplitude of signal and protects the slotted line carriage and standing wave indicator. The detector should be a square-law (output proportional to rf power input) device such as a barretter or a crystal diode operated at low signal levels. The S.H.F. signal passes through slotted line carriage directly to PIN diode. There were two circuits connected to the other side of PIN diode; one circuit consisted of r.f. choke, microammeter, variable resistor and D.C. source, which supplied the necessary D.C. bias to PIN diode, the other circuit consisted of a unit power supply, unit oscillator, G db attenuator and capacitor, which supplied the V.H.F. or U.H.F. signal to the PIN diode. The "A" part which arrounded by a dashed line in the Figure (5) was used for the rectified current measurement.

In order to get the characteristics of the PIN diode, such as impedance versus frequency, rectified current versus frequency + input power, we can change either D.C. bias current, V.H.F. (U.H.F.) frequency, or V.H.F. (U.H.F.) input power or all three.

All measurements of characteristics with this equipment were made at a constant S.H.F. frequency of approximately 10.8 GHz to keep the

results consistent.

2. Procedure for Smith Chart calculations for impedance measurement

The step by step procedure for employing the Smith Chart when solving transmission line problem is outlined below. It should be understood that there are various methods employed for entering the data obtained from the slotted line on the Smith Chart, and that the method outlined in this section has been found practical and simple.[1]

1) Set up slotted line in system as Figure (5).
2) Measure SWR (standing wave ratio).
3) Determine wavelength of transmission line (λL). The distance as measured on slotted line between two adjacent minima is equal to one-half the wavelength of the line.
4) Find a convenient minimum point.
5) Replace load (PIN diode) with shorting termination.
6) Measure Δd [the shift in centimeters of the minimum point with the short applied (step 5)].
7) Determine the shift of the minimum in terms of the wavelength

$$\Delta\lambda = \frac{\Delta d}{\lambda L}$$

8) Starting at center of Smith Chart draw circle with SWR as radius (read SWR on zero reactance line down from center, Figure 6).
9) The quantity $\Delta\lambda$ established in step (7) is entered on the Smith Chart by proceeding at the top in the direction of the probe movement (either toward the load or toward the generator) when the load was replaced by a short.

10) Draw a line to the center of the chart from the $\Delta\lambda$ point.

11) The intersection of this line and SWR circle is the normalized impedance.

12) It is important that the convention be followed of first finding the minimum reference with the load on the line and then sliding the probe to the new minimum when the line is shorted. Should it be necessary to establish the shorted minimum point first, $\Delta\lambda$ would be entered on the Smith Chart in a direction opposite to the direction of probe movement. That is, the probe movement toward the load would be entered on the chart in a direction toward the generator.

13) The following is an example of the previous procedure (Figure 6). The SWR measured is 3.15. Distance between two adjacent minima is 1.75 cm. Therefore, wavelength of the line is 3.5 cm. (λL). A convenient minimum for the unknown is located at 12.58; when the line is shorted the minimum point shifts to 12.09 cm. (toward generator, so in chart is toward load)

$$\Delta d = 12.58 - 12.09 = 0.49$$

$$\Delta\lambda = \frac{\Delta d}{\lambda L} = \frac{0.49}{3.5} = 0.14 \text{ wavelength}$$

Construct SWR circle on Smith Chart (1). Construct radius to wavelength shift point (2). Read normalized impedance at intersection of circle and radius (3).

$$Z_L = 0.675 - j\,0.95$$

Therefore, changing either D.C. bias, frequency, input power, or any combination of these, results in different Z_L.

III. Results

A. Efficiency of frequency conversion.

The results are shown in Figure (7) and (8), which were plotted in the form of conversion efficiency versus frequency. Each measurement was made two or three times by repeating the tuning operations. The maximum value of efficiency observed is plotted in each case.

1. Forward bias

The conversion efficiencies for all incident power levels (50 mw, 100 mw, and 200 mw) show a sharp decrease at frequencies greater than 200 MHz (Figure 7). There is no output above 400 MHz. Measurements were not made below 200 MHz because the necessary filters were not available. From the data obtained over a limited frequency range we conclude that a cut-off mechanism is in effect above 200 MHz. We shall now consider possible explanations of this effect, assuming that the capacitance at forward bias in the I layer is predominately associated with stored carriers.

The cut-off frequency may be explained by the results of an experiment described by Galvin and Uhler[2], in which a PIN diode was subjected first to a forward current pulse, and immediately thereafter to a reverse current pulse. The instantaneous microwave impedance was measured at regular intervals during the entire process. During the forward pulse the diode impedance is a pure resistance, while during the reverse pulse it is a series combination of capacitance and resistance. Thus the cut-off frequency observed for frequency division may be determined by either of two mechanisms[3]: (1) the product RC of the I

layer, (2) the transit time associated with the removal of stored carriers from the edge regions of the I layer where the density fluctuations occur.

2. Reverse bias

Plots of conversion efficiency versus frequency, (Figure 8) show an interesting fluctuation, with maxima at 300 MHz and 550 MHz, and minima at 450 MHz and 600 MHz. There was no appreciable output at frequency higher than 600 MHz. An assumption that the variable capacitance at reverse bias is due to variation of the depletion layer, is given for the possible explanation of these results[3].

Figure (9a) is a plot of carrier density throughout the I layer for an applied reverse voltage such that the depletion layer width W is approximately half the total I-layer width t. The depletion layer, being devoid of carriers, may be considered a pure capacitance; the undepleted portion, which has a resistivity of about 560Ω-cm, is represented by a shunt combination of conductance and capacitance, which are of the same order of magnitude in the frequency range under consideration. An electrical equivalent for the diode as a whole is shown in Figure (9b), where R represents the combined resistance of the P and N region which is in series with the I layer.

A plot of the static $Q = \frac{I_m Z}{R_e Z}$ for R = 0 and $R = \frac{1}{10G}$ of this circuit is shown in Figure (10). This curve possesses a minimum at $f \approx 0.8\ f_r$ (where $\omega_r = \frac{G}{C} = \frac{\sigma}{\varepsilon}$); a maximum at $f \approx 3\ f_r$, and steadily decreasing Q for $f > f_r$. In these respects its form is similar to that of the experimental data plotted in Figure (8). For the particular

diode used, f_r is calculated and gives f_r = 250 MHz. This implies a minimum of static Q at 0.8 f_r = 200 MHz, which agrees to order of magnitude with the value of 450 MHz for a minimum in conversion efficiency (Figure 8). The difference between these two values may be due to a large uncertainty in the value of the area of the diode, used to calculate σ.

Comparing Figures (8) and (11) we find that the plot of reverse D.C. bias voltage at maximum efficiency versus frequency (Figure 11), and the experimental data plotted in Figure (8) have similar shape. At the present time, it is not possible to explain this relation between the two.

B. Rectified current measurements

First of all we discuss the case that no external D.C. bias is applied; i.e. only a microwave signal is applied to the PIN diode. The results of rectified current measurements are presented as a plot of log $I_{rect.}$ versus log f, (Figure 12), and Table 1. It is seen that the rectified current is approximately directly proportional to the input signal power and inversely proportional to the signal frequency at frequency between 50 MHz to 180 MHz. At frequencies greater than 180 MHz, the slope of the log $I_{rect.}$ versus log f plot becomes steeper; the inverse proportionality between log $I_{rect.}$ and log f no longer holds.

Figure (13), (13a), (13b), (13c), and (13d) give data for the case that both D.C. forward bias and V.H.F. or U.H.F. signal were applied to the PIN diode. In these cases the carrier densities in the I region were not only controlled by the D.C. bias current, but also by the rectified current. The results of total current (I_o + rectified current)

measurements are indicated as a plot of total current versus frequency (Figure 13). It is seen that the total currents (D.C. bias current + rectified current) decrease with increasing frequency. At lower D.C. bias, the rectified current was predominant, while at higher D.C. bias the rectified current becomes very small compared with D.C. bias current. When the D.C. bias increases to above 300μa, the rectified current seems to be very small. At high frequencies (above 300 MHz), the total current nearly equals the D.C. bias current, the rectified current seems to be unimportant.

The rectified currents are no longer directly proportional to the signal input power and inversely to the frequency for every applied D.C. bias current, (Figure 13a, 13b, 13c, and 13d). It is seen that at $I_o = 20\mu a$, the rectified current is still approximately directly proportional to input signal power and inversely to frequency at lower frequency. When I_o increases above 20 μ a, they are no longer proportional for all power levels.

From the above discussion we can recognize that the D.C. bias is much more effective than high frequency current for injecting carriers into the I layer, especially at larger bias currents.

In comparing the results of Figure (7) and (12) we recognize a relation between the conversion efficiency and the rectified current. Both of these decreased with increasing frequency. Above 400 MHz the rectified current and conversion efficiency were approximately zero.

C. Impedance measurements

1. Reverse bias

The results are presented in the form of plots of capacitive

reactive and resistance versus bias voltage (Figure 14). It can be seen that the capacitance of the I layer is independent of the reverse bias voltage, and the resistance of the I layer decreases with increasing reverse bias voltage. An equivalent circuit is given, (Figure 9b) for explanation of the results. Assuming the I layer to have a small P type impurity atom concentration, a portion of the I layer next to the N layer is depleted at zero bias. The capacitance of the depletion layer C_1 is shown in series with a parallel G_1-C_2 combination representing the unswept portion of the I layer, Figure (9b). The values of C_1, C_2 and G_1 can be specified in terms of the device structure parameters, i.e.

$$C_1 = \frac{\varepsilon A}{W} \quad ------ (1)$$

$$C_2 = \frac{\varepsilon A}{t-W} \quad ------ (2)$$

$$G_1 = \frac{A}{\rho(t-W)} \quad --- (3)$$

In order to simplify the discussion, the series form, (Figure 9b) is obtained by calculating the series elements C_2' and R_1 from the parallel elements C_2 and G_1 representing the unswept I layer. C_2 is a high Q capacitance, so

$$C_2' \approx C_2 \quad ---- (4)$$

and

$$R_1 = \frac{G_1}{\omega^2 C_2^2 + G_1^2} \quad --- (5)$$

The total equivalent series capacitance

$$C_o = \frac{C_1 C_2'}{C_1 + C_2'} \quad ---- (6)$$

The depletion layer width W increases with increasing reverse bias

voltage; therefore, C_1 decreases, C_2 and G_1 increase. According to Eq. (5) and (6), the equivalent resistance R_1 decreases and the equivalent series capacitance is unchanged, with increasing reverse bias voltage. This explanation agrees with the experimental results shown in Figure (14).

2. Forward bias

The results of impedance measurements for forward bias are presented as plots of resistance R versus applied forward bias current (Figure 15) and capacitive reactance X_c versus applied forward bias current (Figure 16). It is seen that the resistance (Figure 15) increases as the D.C. bias current increases between zero bias to about 60 μa for each signal frequency. At 60 μa D.C. bias current the resistances generally reach a maximum. When the D.C. bias current exceeds 60 μa the resistance decreases for each frequency.

In Figure (16) it is seen that the capacitive reactance X_c decreases with the increasing D.C. bias current. The reactance X_c is a maximum at zero bias current, then decreases very sharply with increasing bias current, until bias current reaches 500 μa. Above 500 μa, the slope rate becomes smaller and X_c is nearly zero; i.e. at very high bias current, the capacitance approaches infinity. This phenomenon is considered due to the increase in the concentration of carriers (holes and electrons) stored in the high resistivity middle region ("I layer") with increasing forward bias.

IV. Conclusions

An investigation of the PIN diode has shown that this device functions as a variable capacitance in the V.H.F. and U.H.F. range.

The frequency dependence of conversion efficiency for forward bias is quite different than at reverse bias. The conversion efficiency is a sharply decreasing function with increasing frequency for forward bias, but an interesting fluctation with increasing frequency is found for reverse bias. It is a function of the rectified current and bias voltage for the forward and reverse bias, respectively. This phenomenon is considered due to the different charge storage mechanism; for forward bias the variable capacitance is due to carrier storage, while at reverse bias it is due to depletion capacitance.

The rectified current was found to be approximately proportional to the input signal power and inversely proportional to the frequency for the signal frequency between 50 MHz to 180 MHz. This dependence of rectified current on frequency at a given power level may result from the following. Assume that a given power level, the a.c. current has a particular value independent of frequency, then the a.c. current is related to stored charge by

$$I_1 = \frac{dQ}{dt} = j\omega Q$$

and to the number of stored carriers by

$$I_1 = \frac{d\,(Nq)}{dt} = j\omega Nq$$

On the other hand, the rectified current is determined by the recombination rate

$$I_o = \frac{qN}{\tau} \quad \text{or} \quad I_o = \frac{|I_1|}{\omega \tau}$$

The reason for the linear dependence of I_o on signal power is not now understood.

The impedance was measured as a function of D.C. bias and signal frequency for forward bias. In the forward bias state, the I layer is filled with an equal number of holes and electrons injected by the heavily doped N and P regions. At appreciable currents the number of injected charge carriers in the I layer greatly exceeds the number present at equilibrium (zero bias); and thus, according to the equations $R = \rho \frac{t}{A}$ and $C = \frac{dQ}{dV} = \frac{d\,(Nq)}{dV} = q\,\frac{dN}{dV}$, (where N, q, V are the number of carriers, carrier charge, and applied voltage in the I layer, respectively), the resistivity and capacity of this region are considerably reduced and increased with increasing forward bias, respectively.

In the reverse bias state, the capacitance of the I layer is independent of the reverse bias voltage, and the resistance of the I layer decreases with increasing reverse bias voltage.

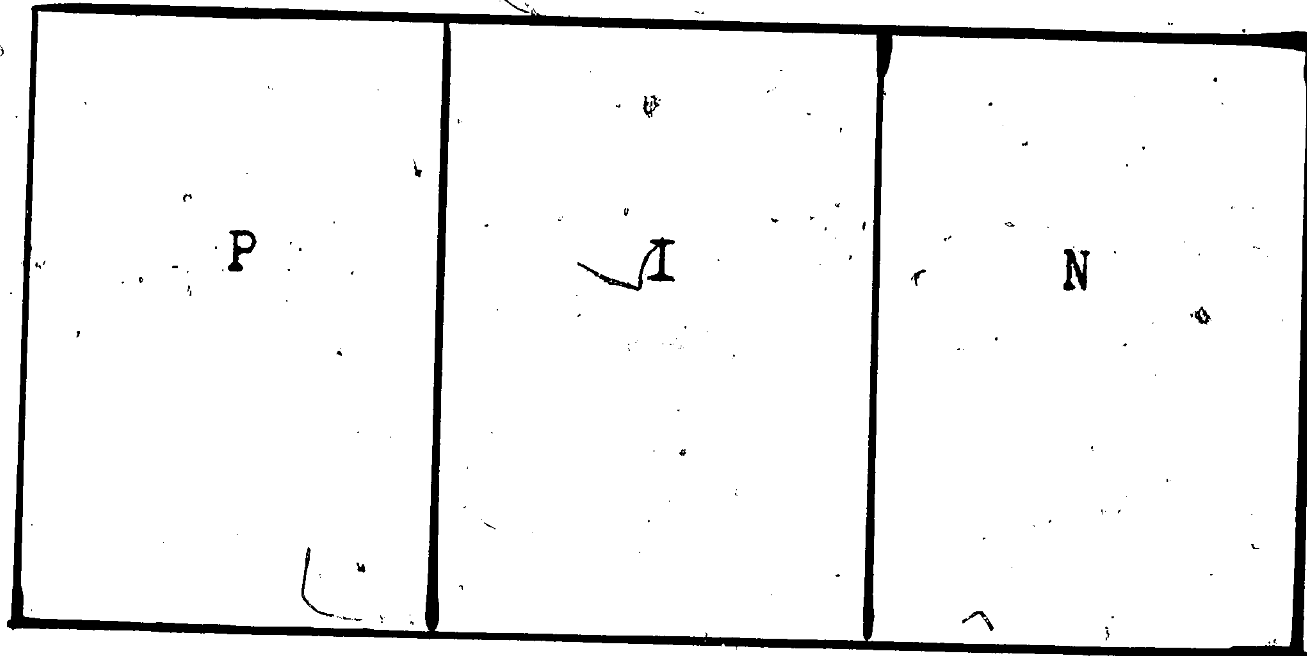

Fig. 1 PIN Structure

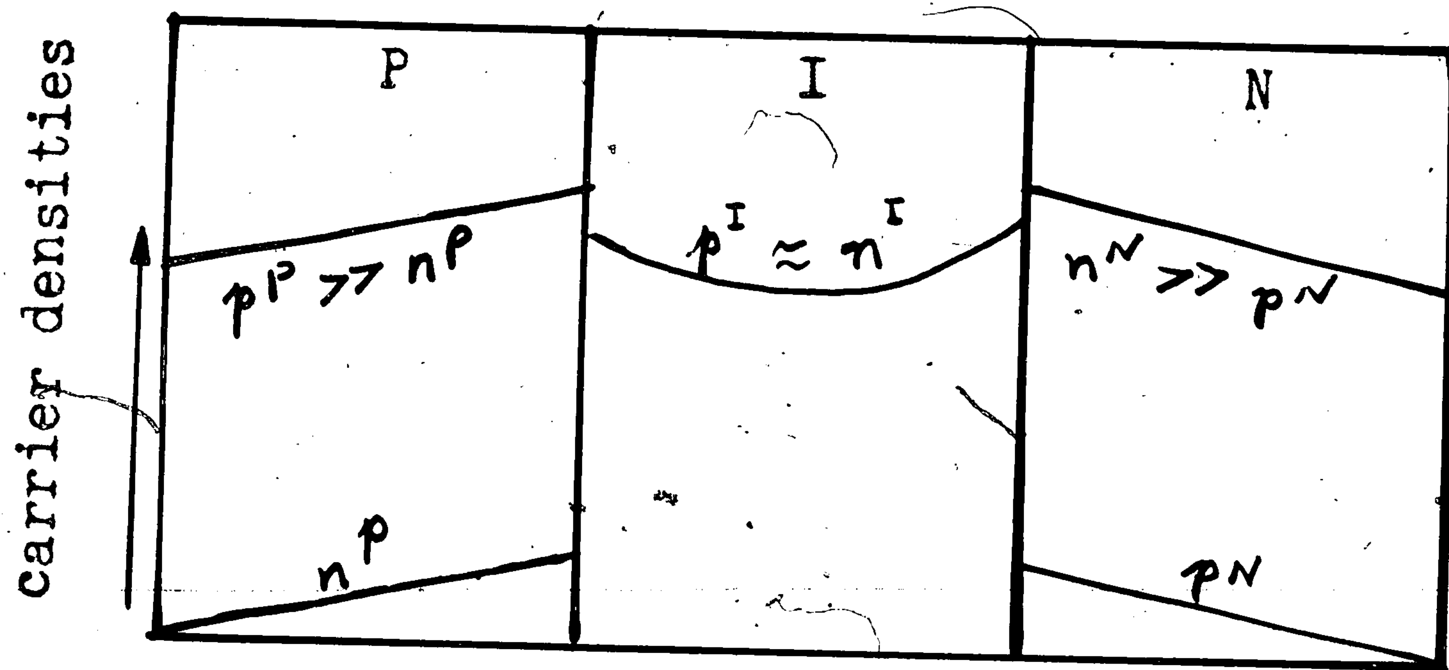

Fig. 2 The Distribution of Carrier Densities for Forward Bias

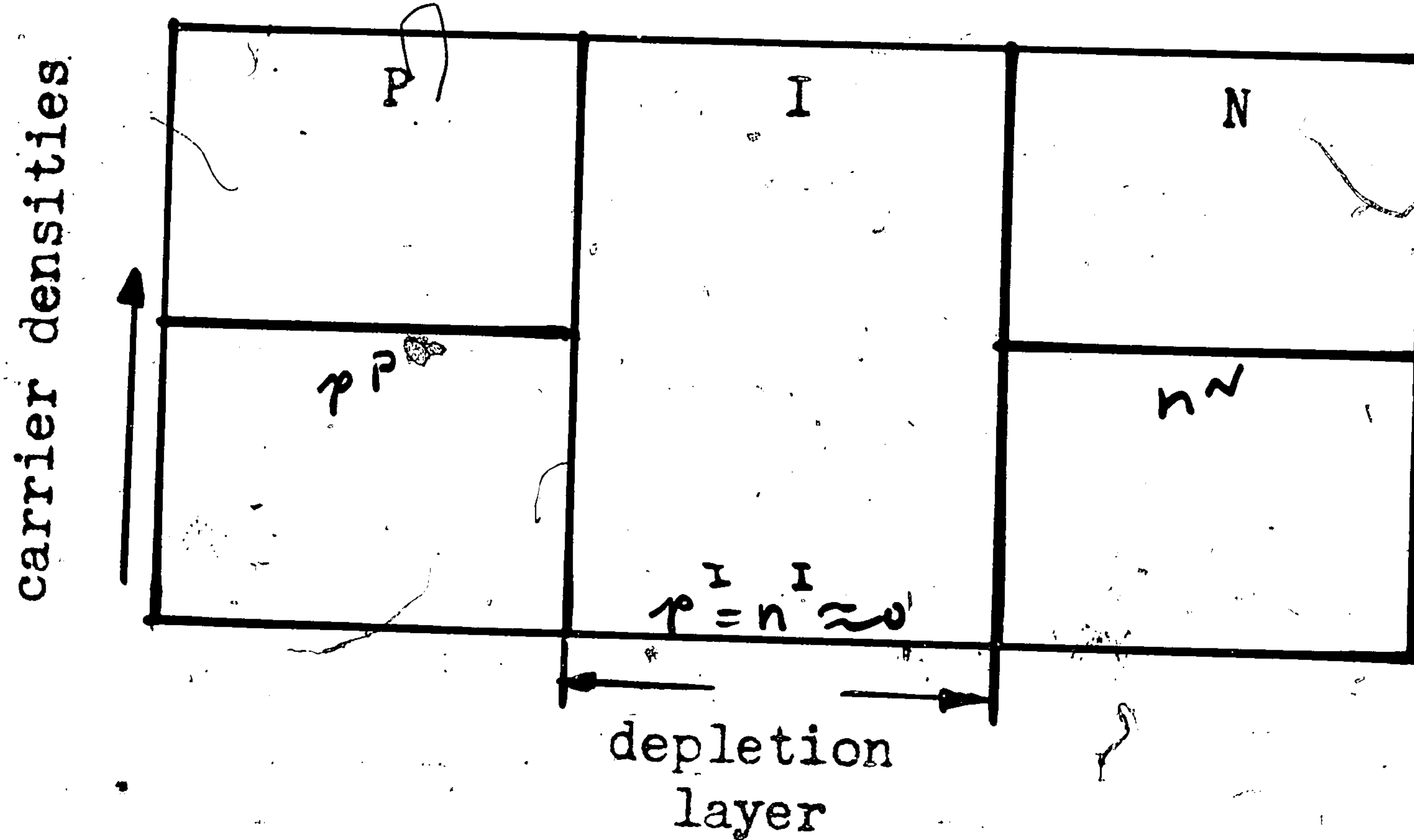

Fig. 3 The Distribution of Carrier Densities for Reverse Bias

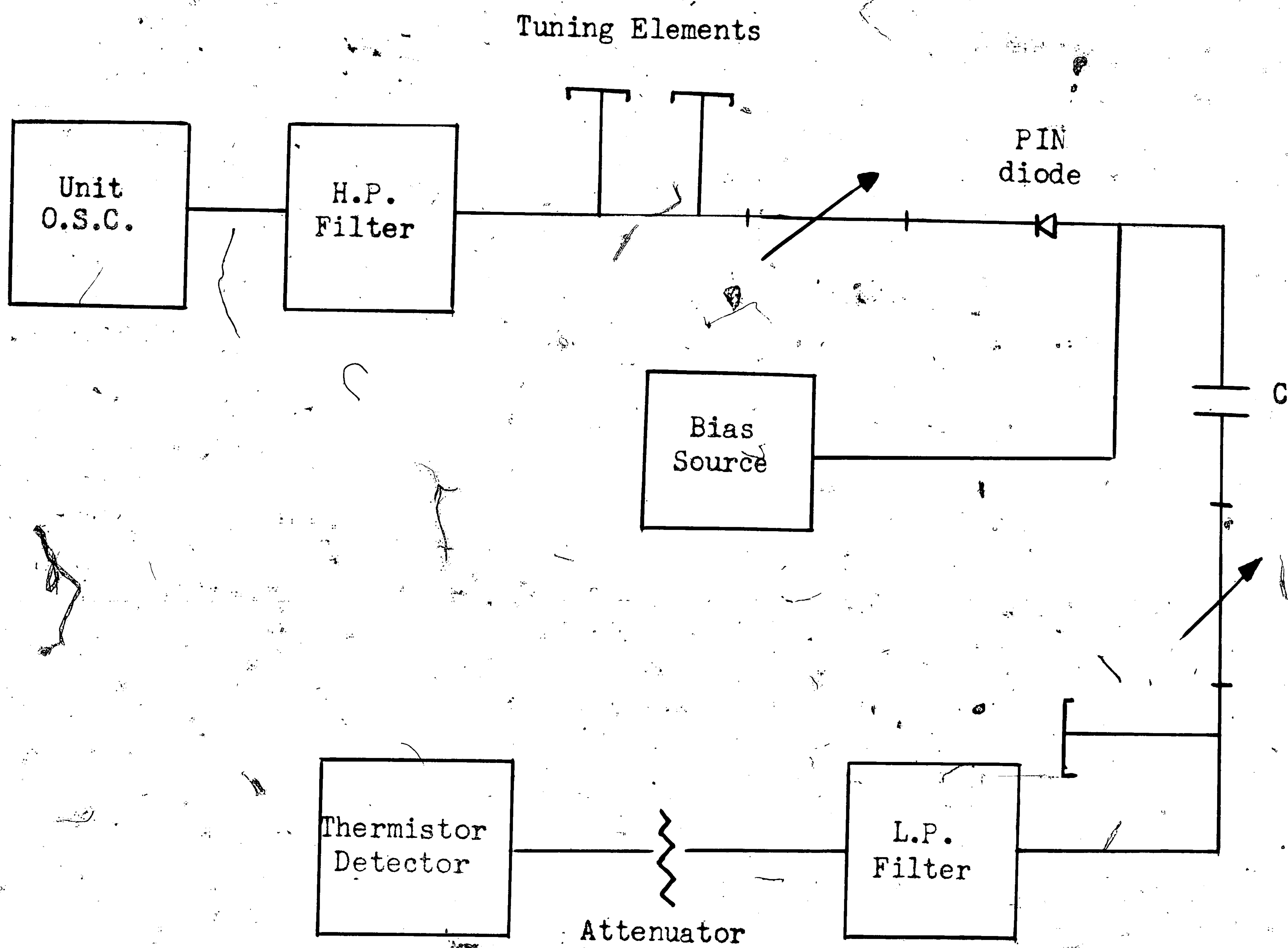

Fig. 4 Circuit for Frequency Conversion Measurements

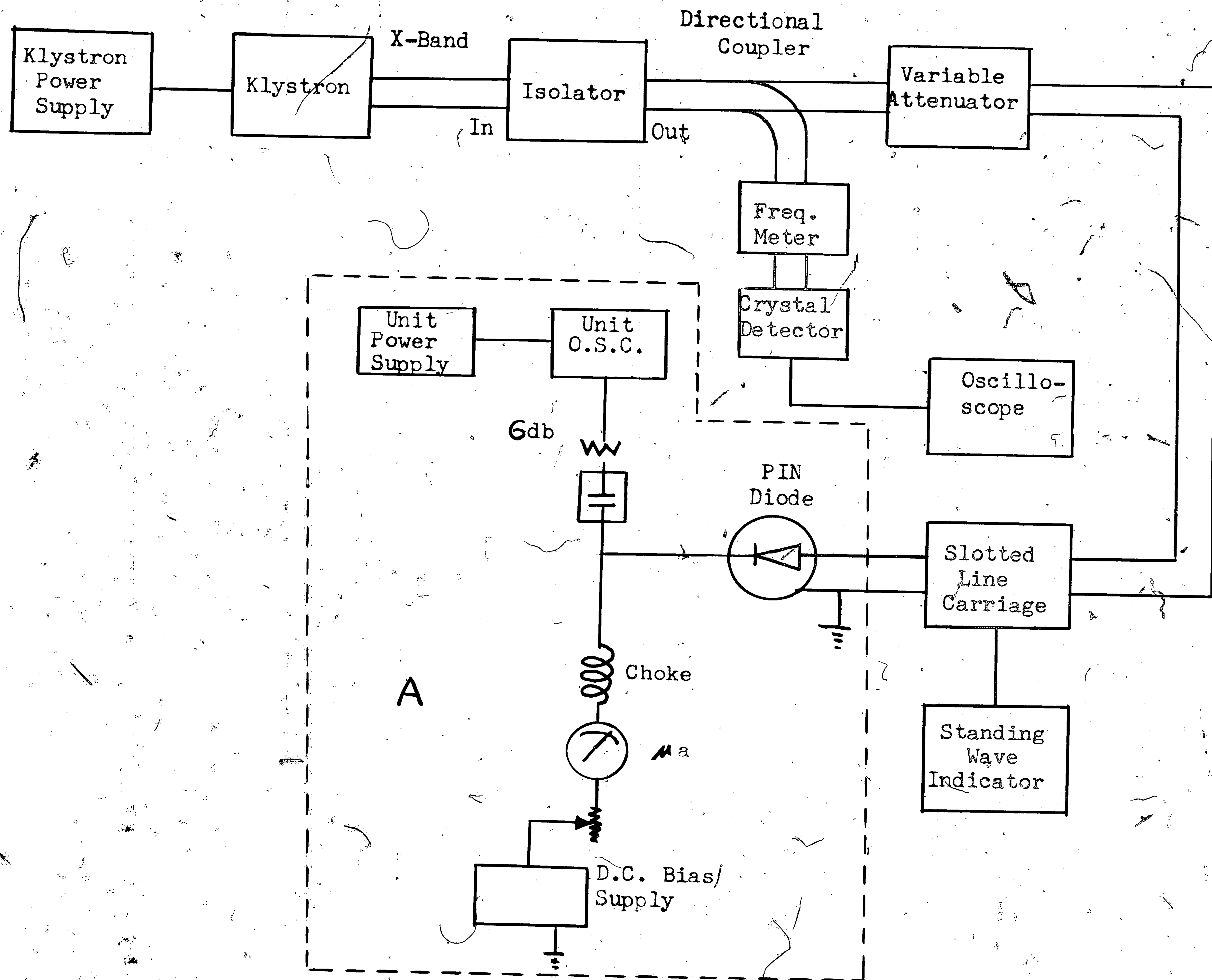

Fig. 5 Circuit for Impedance and Rectified Current Measurement

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IMPEDANCE OR ADMITTANCE COORDINATES

Fig. 6 Smith Chart Showing Normalized Impedance

WAVELENGTHS TOWARD GENERATOR

WAVELENGTHS TOWARD LOAD

ANGLE OF REFLECTION COEFFICIENT IN DEGREES

INDUCTIVE REACTANCE COMPONENT $\left(\frac{+jX}{Z_0}\right)$, OR CAPACITIVE SUSCEPTANCE COMPONENT $\left(\frac{+jB}{Y_0}\right)$

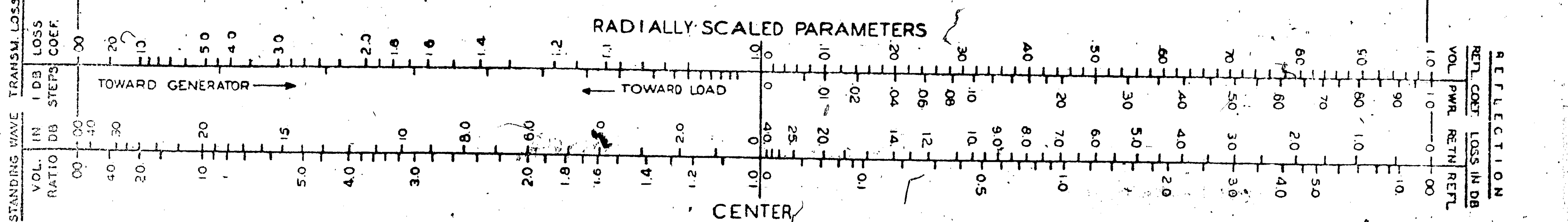
RESISTANCE COMPONENT $\left(\frac{R}{Z_0}\right)$, OR CONDUCTANCE COMPONENT $\left(\frac{G}{Y_0}\right)$

CAPACITIVE REACTANCE COMPONENT $\left(\frac{-jX}{Z_0}\right)$, OR INDUCTIVE SUSCEPTANCE COMPONENT $\left(\frac{-jB}{Y_0}\right)$

① DRAW SWR CIRCLE 3.15

② 0.14 TOWARD LOAD

③ 0.675-j0.95



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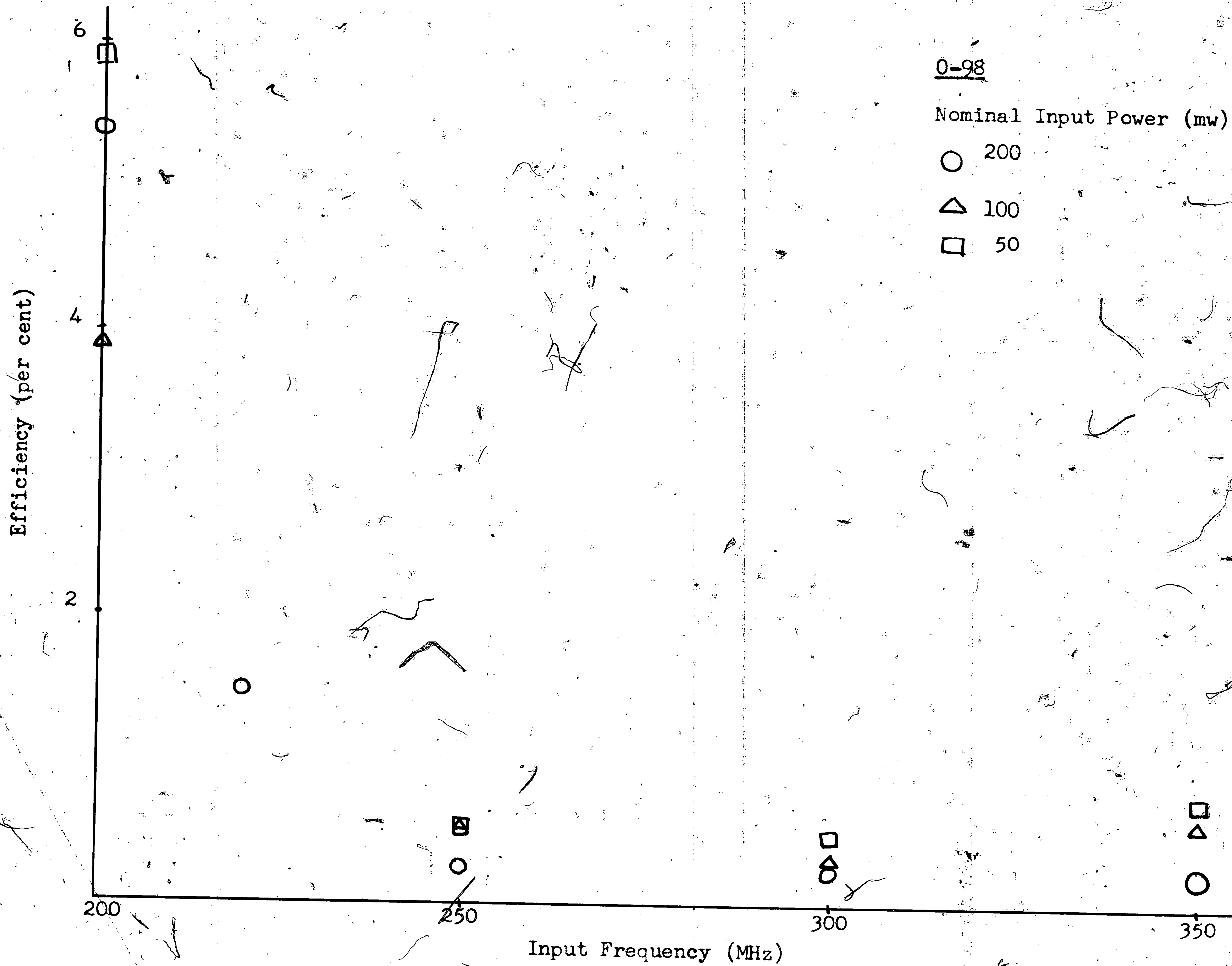


Fig. 7 Conversion Efficiency Versus Frequency (Forward Bias)

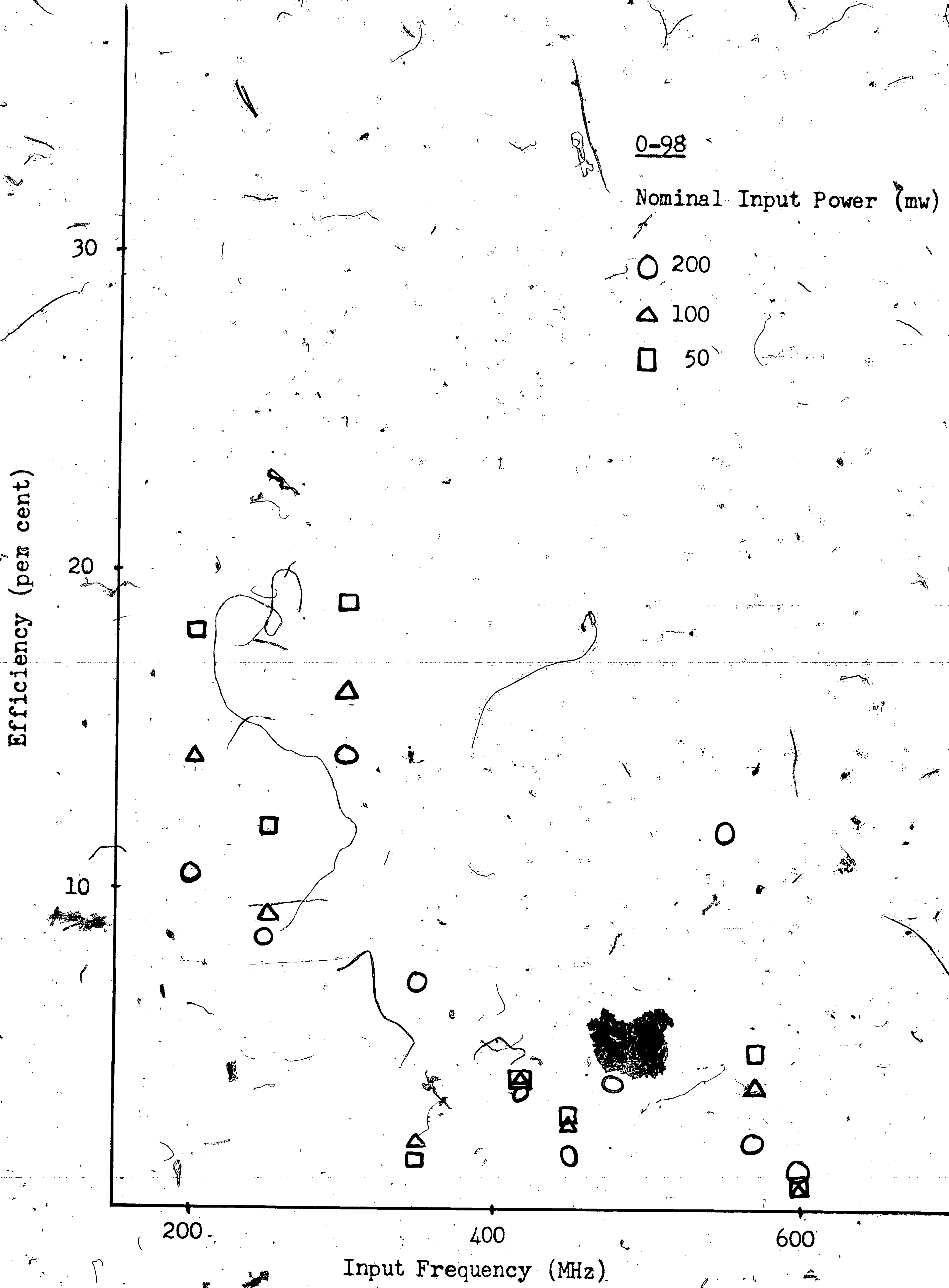


Fig. 8 Conversion Efficiency Versus Frequency (Reverse Bias)

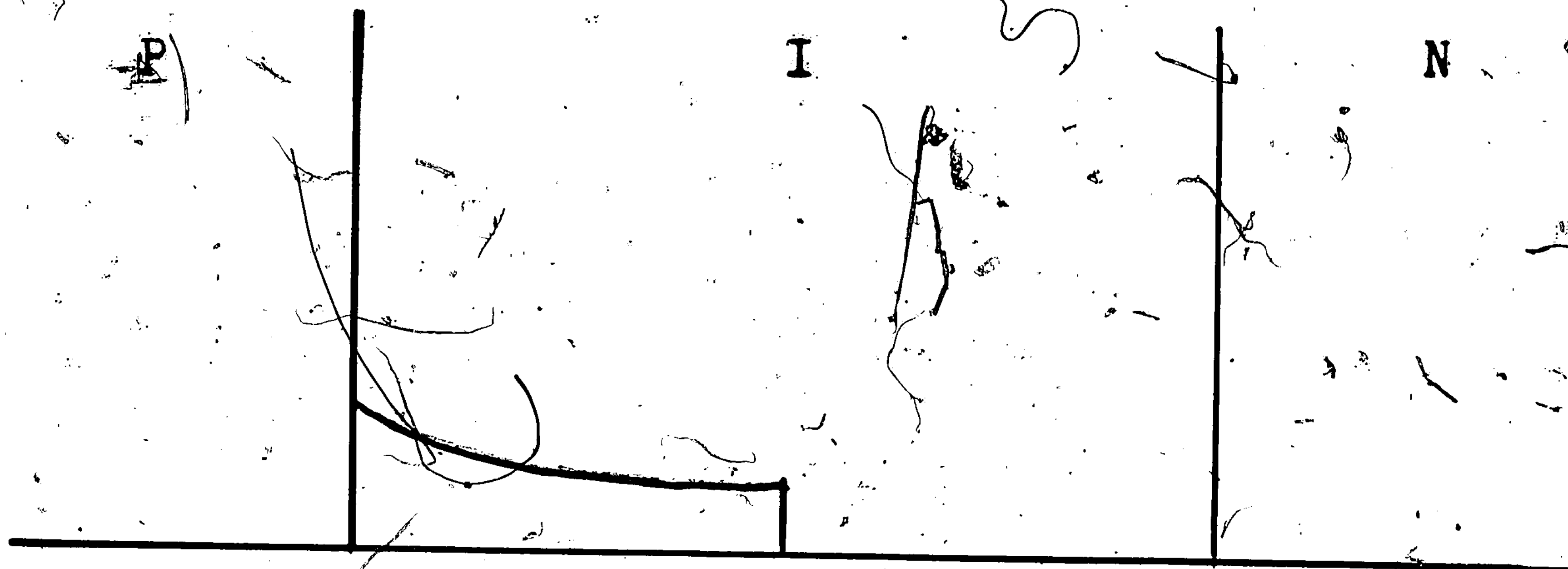


Fig. 9a Carrier Density in I-Layer at Reverse Bias

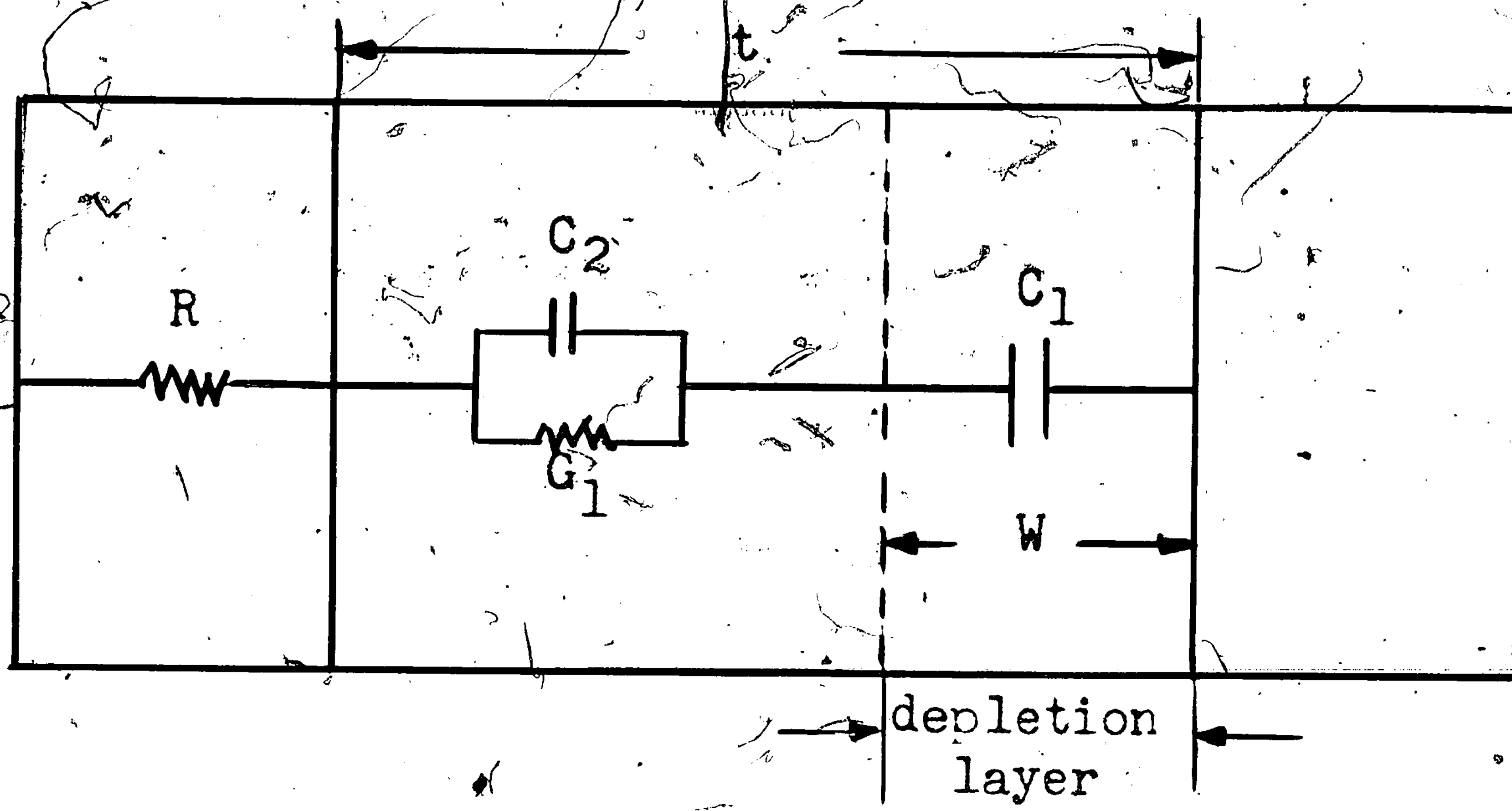
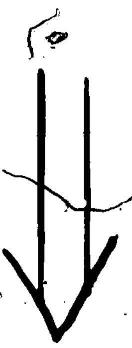


Fig. 9b Electrical Equivalent at Reverse Bias



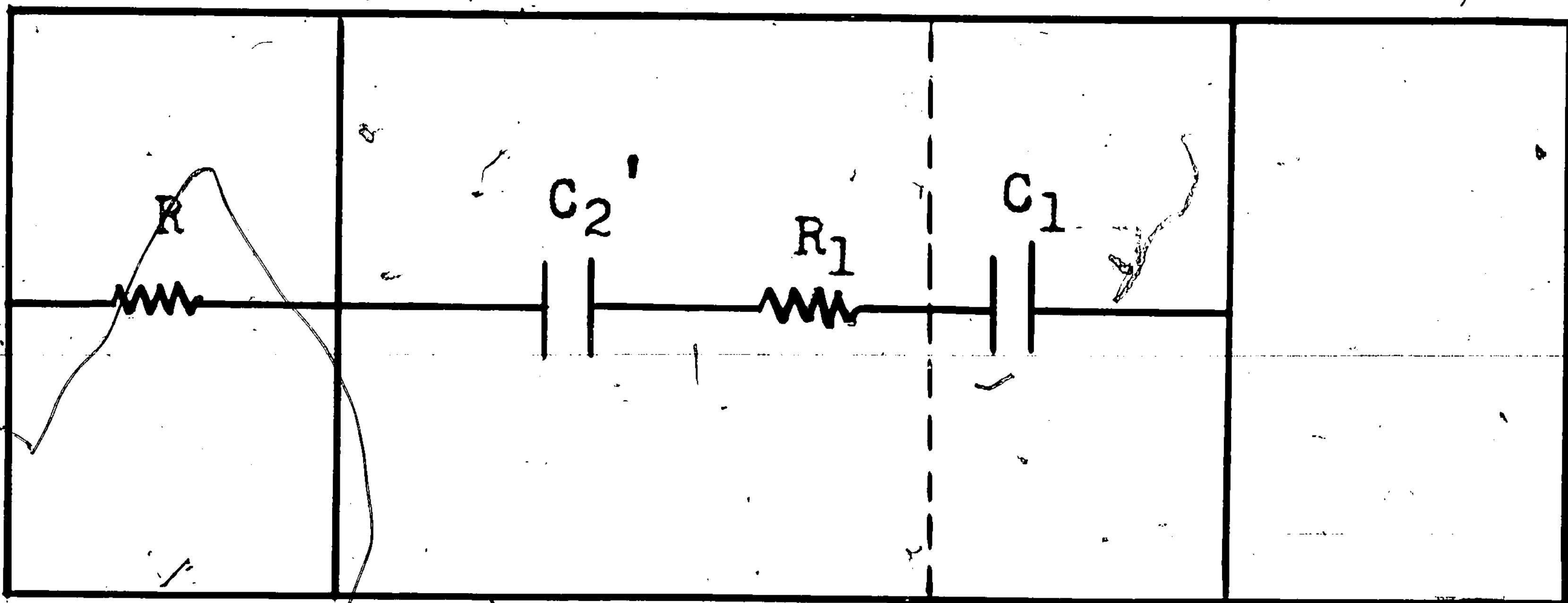


Fig. 9c

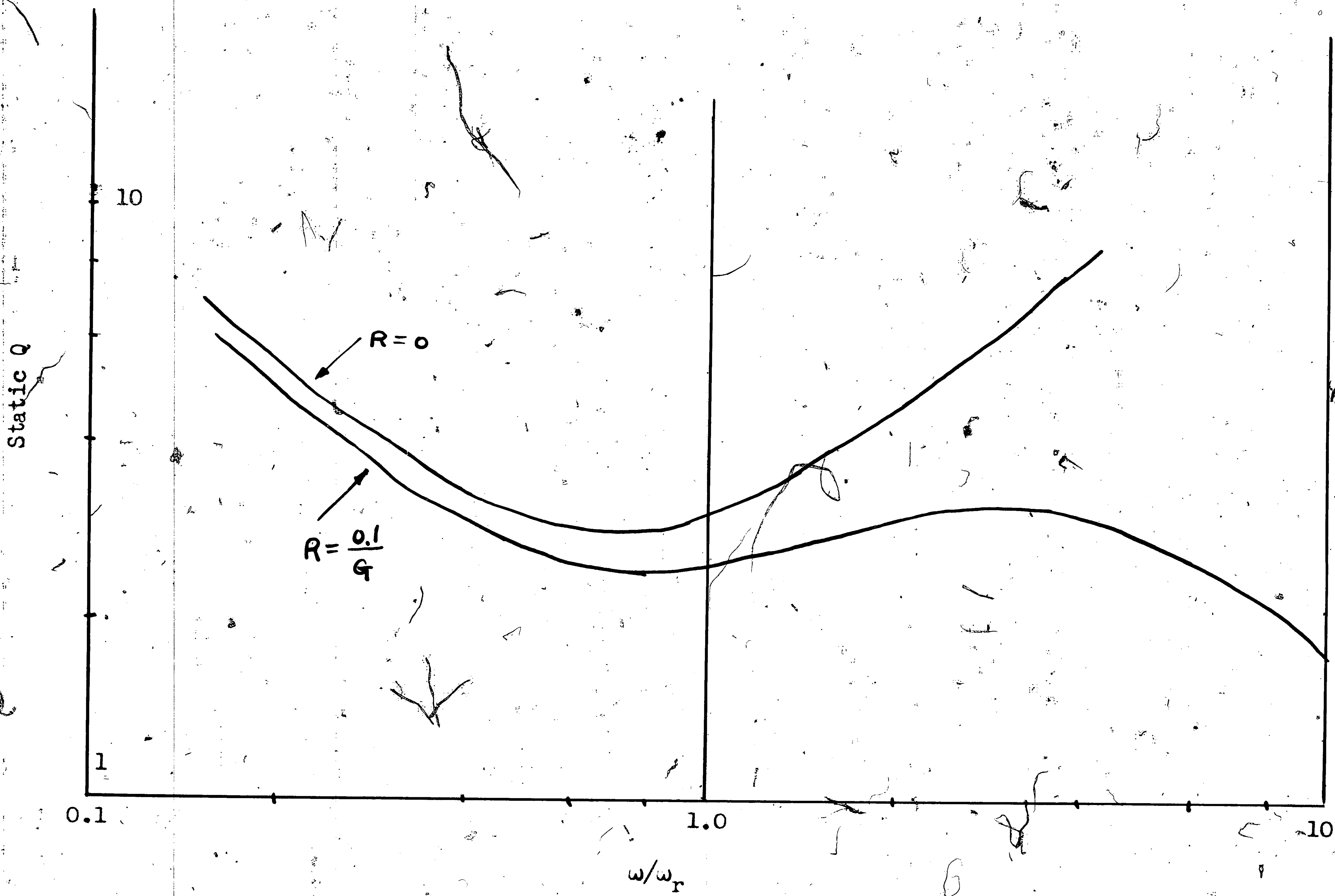


Fig. 10 Frequency Dependence of Static Q

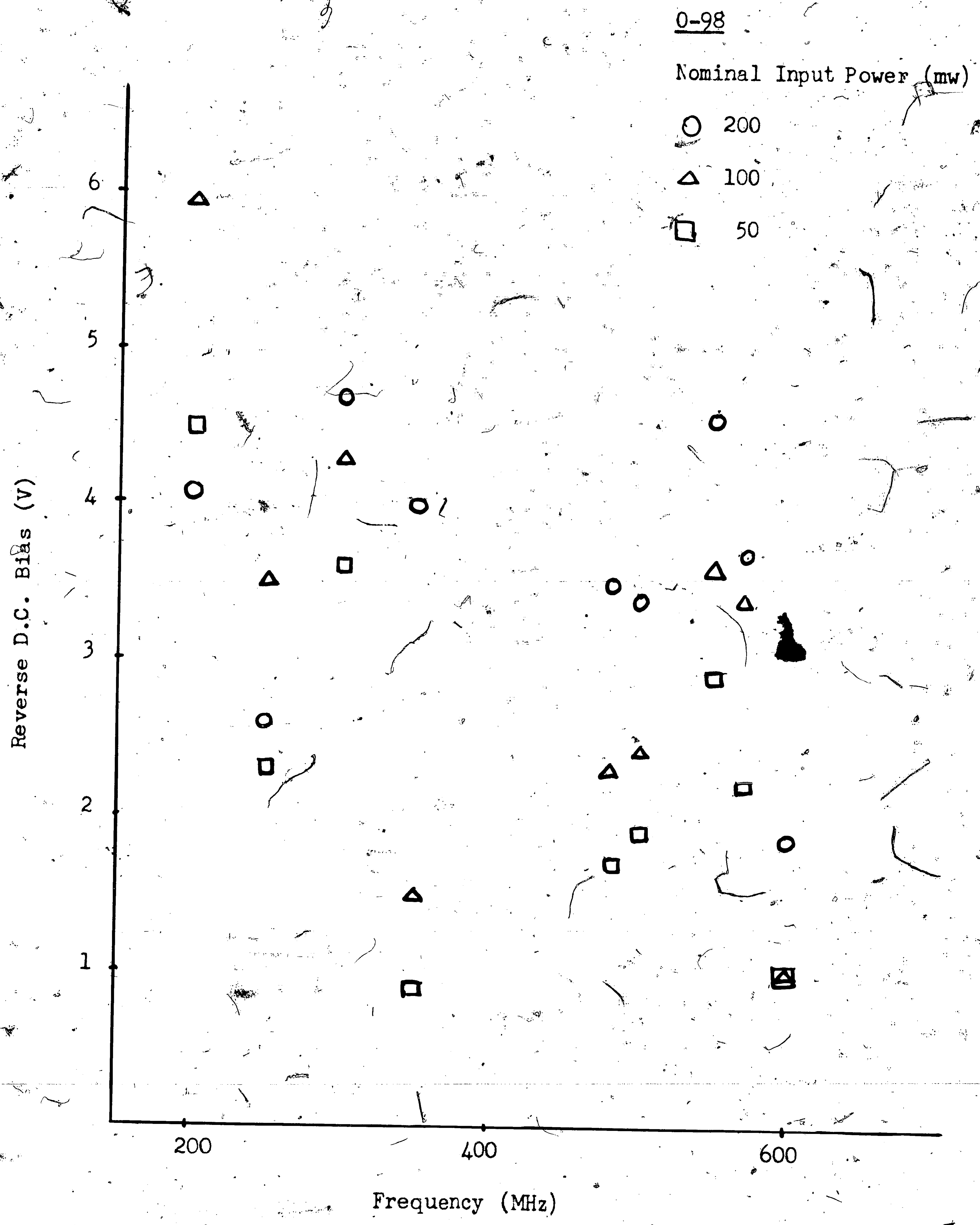


Fig. 11 Reverse D.C. Bias Voltage at Maximum Efficiency Versus Frequency

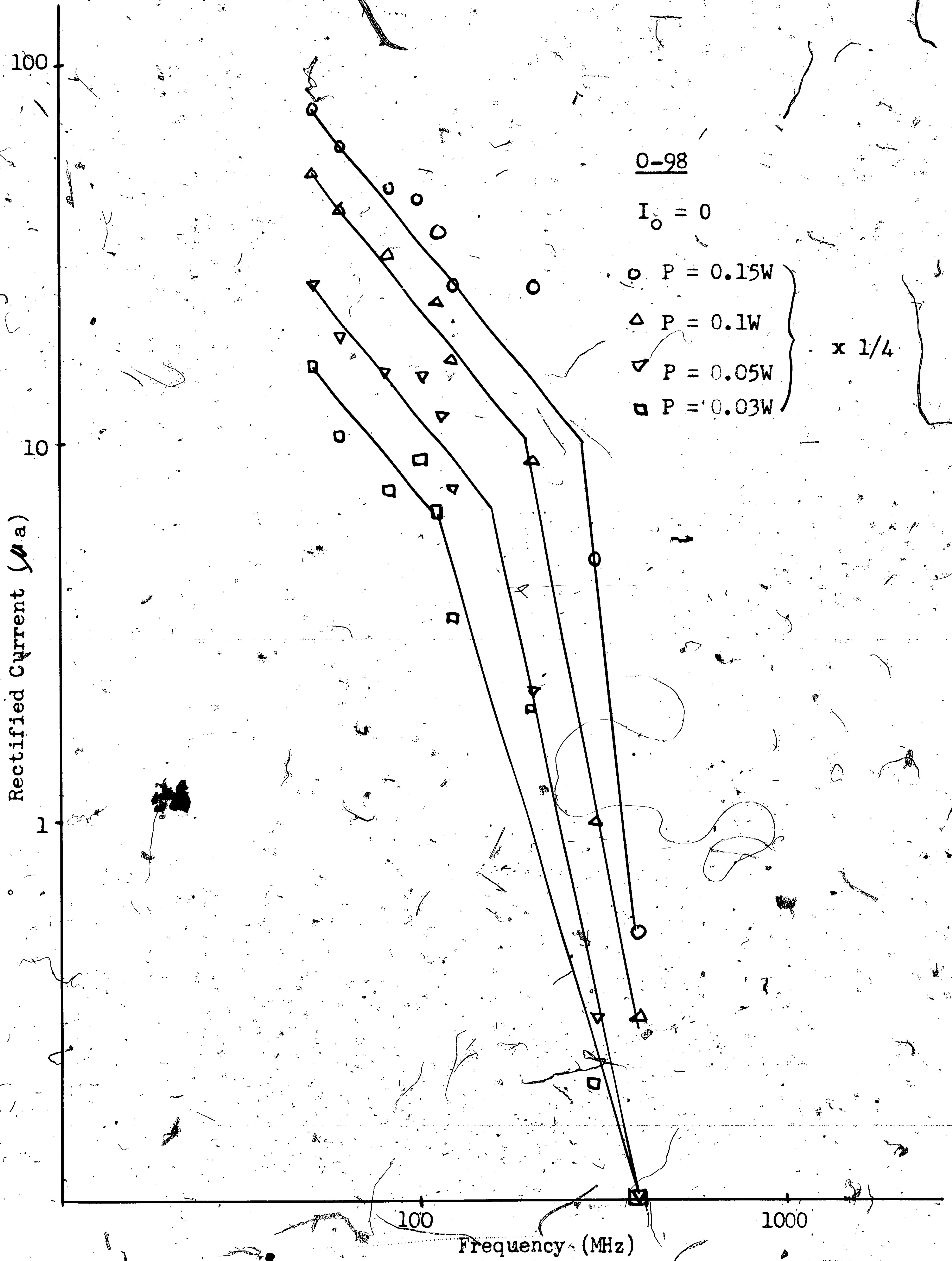


Fig. 12 Rectified Current Versus Frequency and Input Power

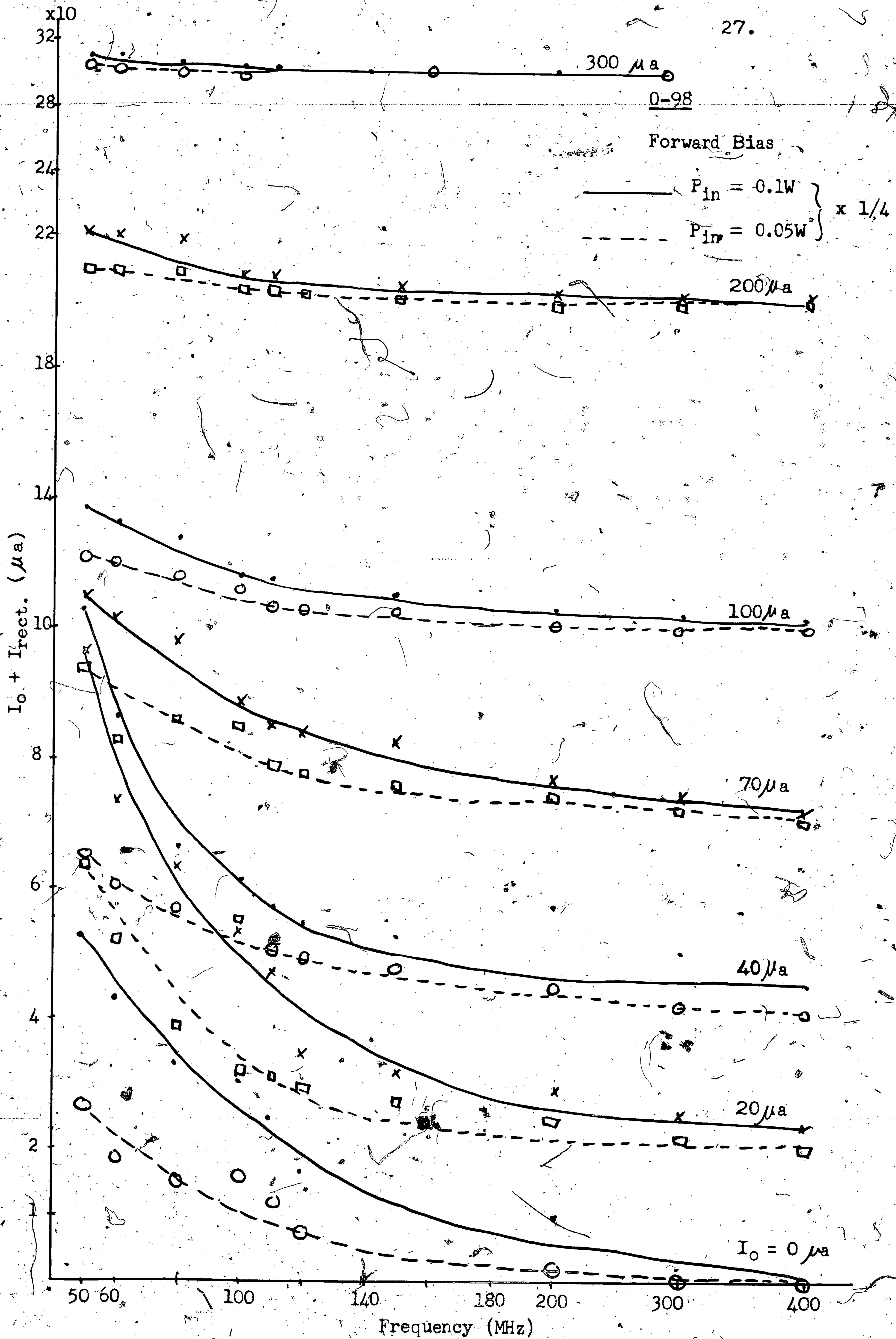


Fig. 13 Total Current (I_o + $I_{rect.}$) Versus Frequency

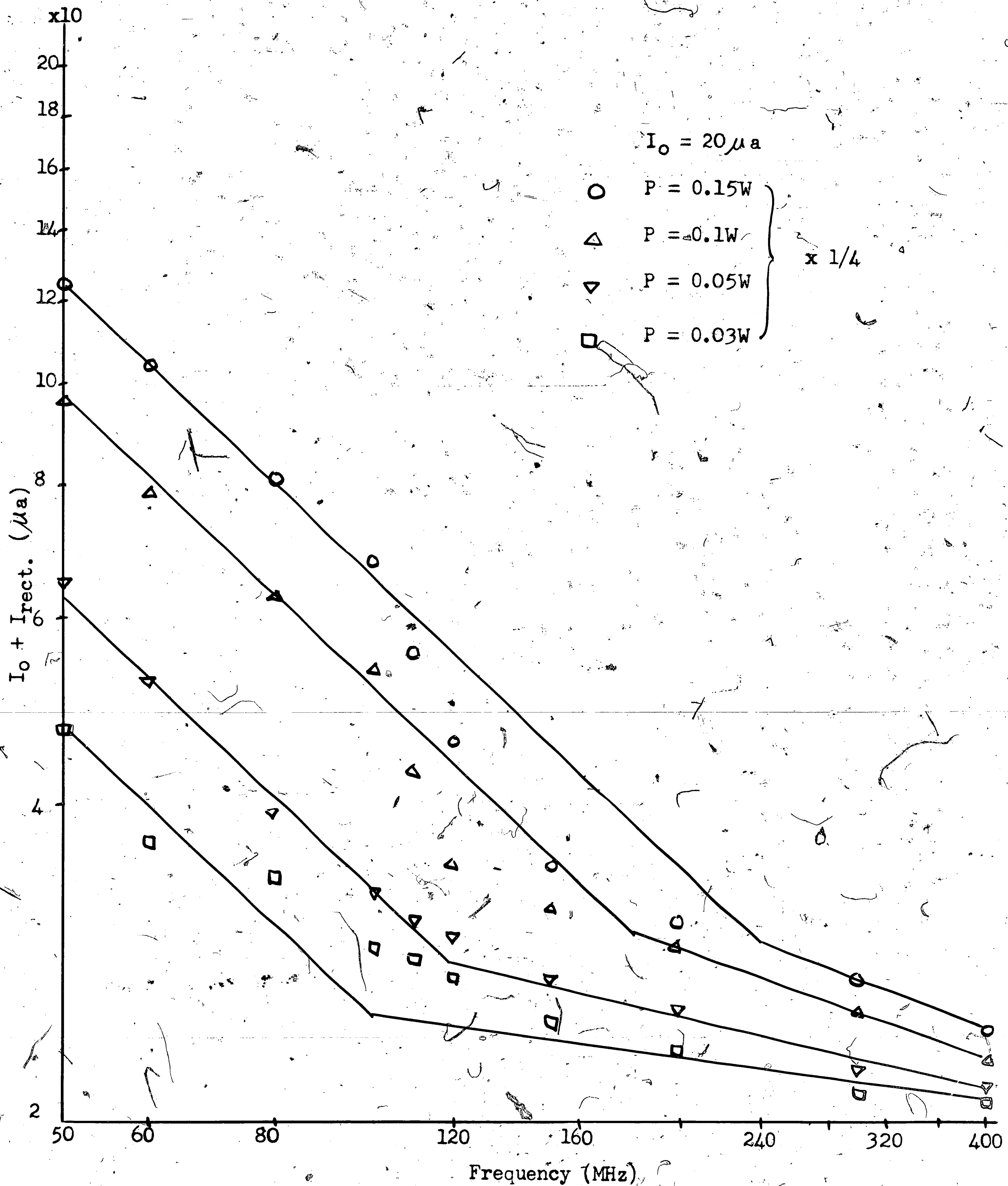


Fig. 13a Total Current ($I_o + I_{rect.}$) Versus Frequency and Input Power

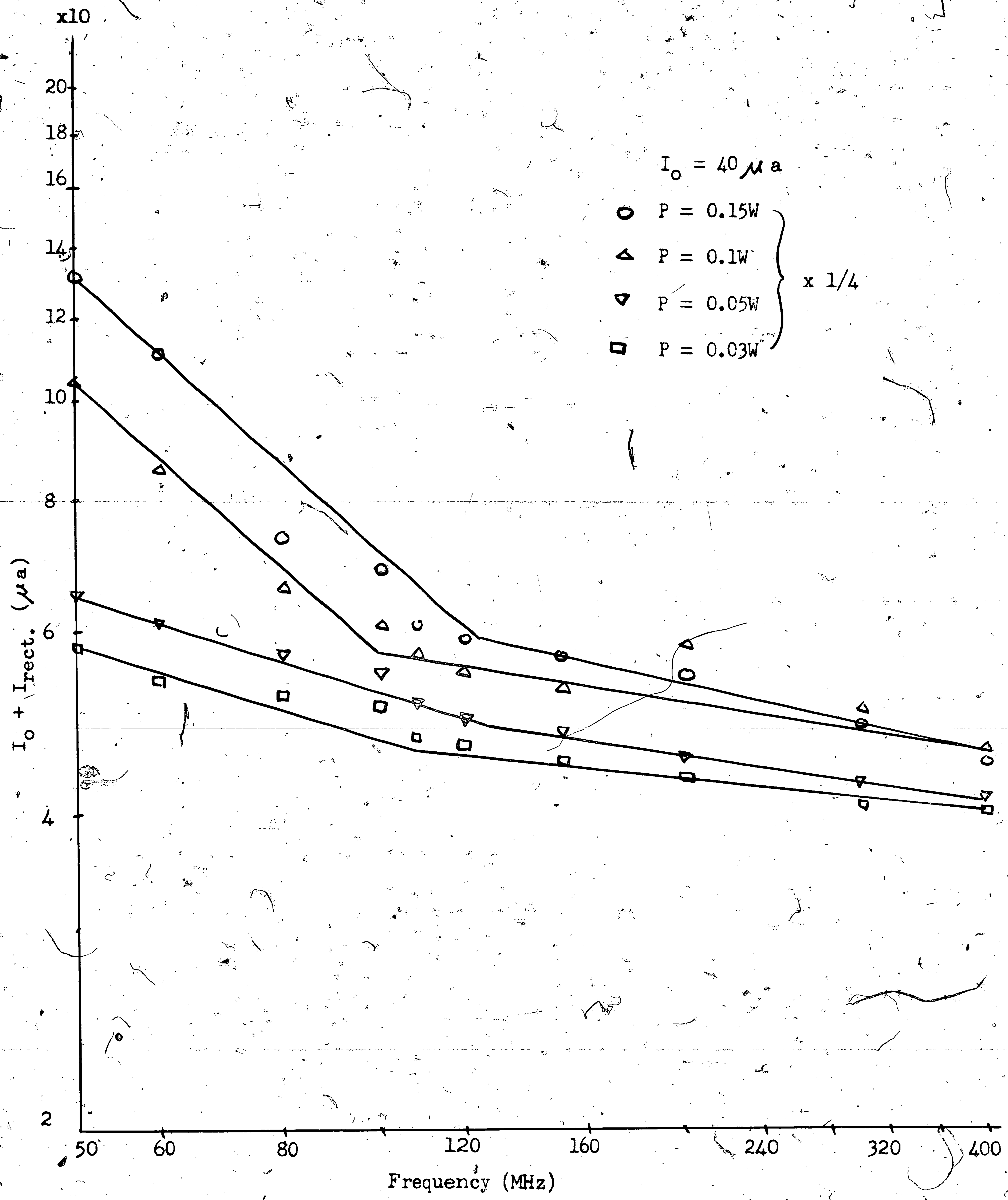


Fig. 13b Total Current (I_o + $I_{rect.}$) Versus Frequency and Input Power

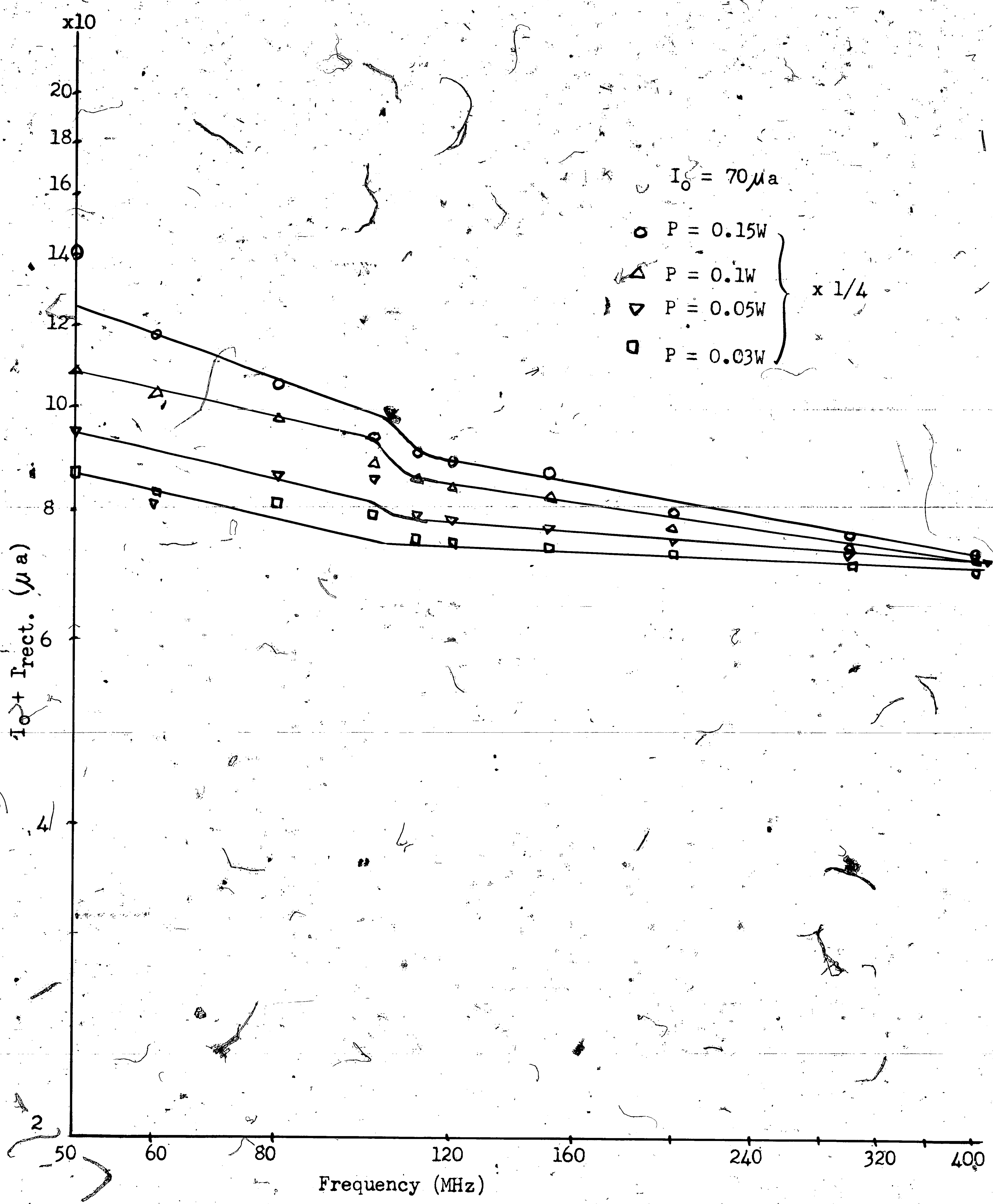


Fig. 13c Total Current ($I_o + I_{rect.}$) Versus Frequency and Input Power

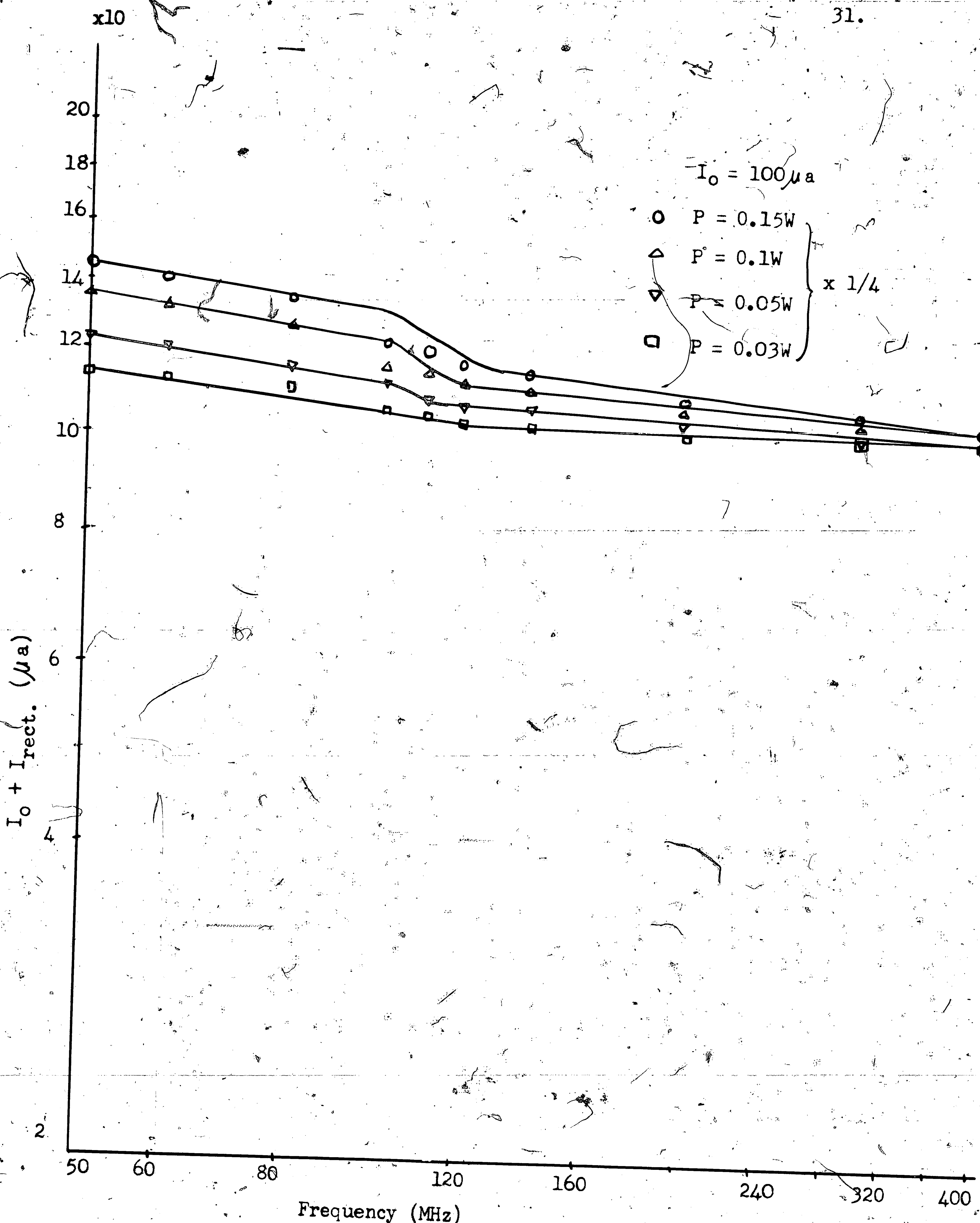


Fig. 13d Total Current ($I_o + I_{rect.}$) Versus Frequency and Input Power

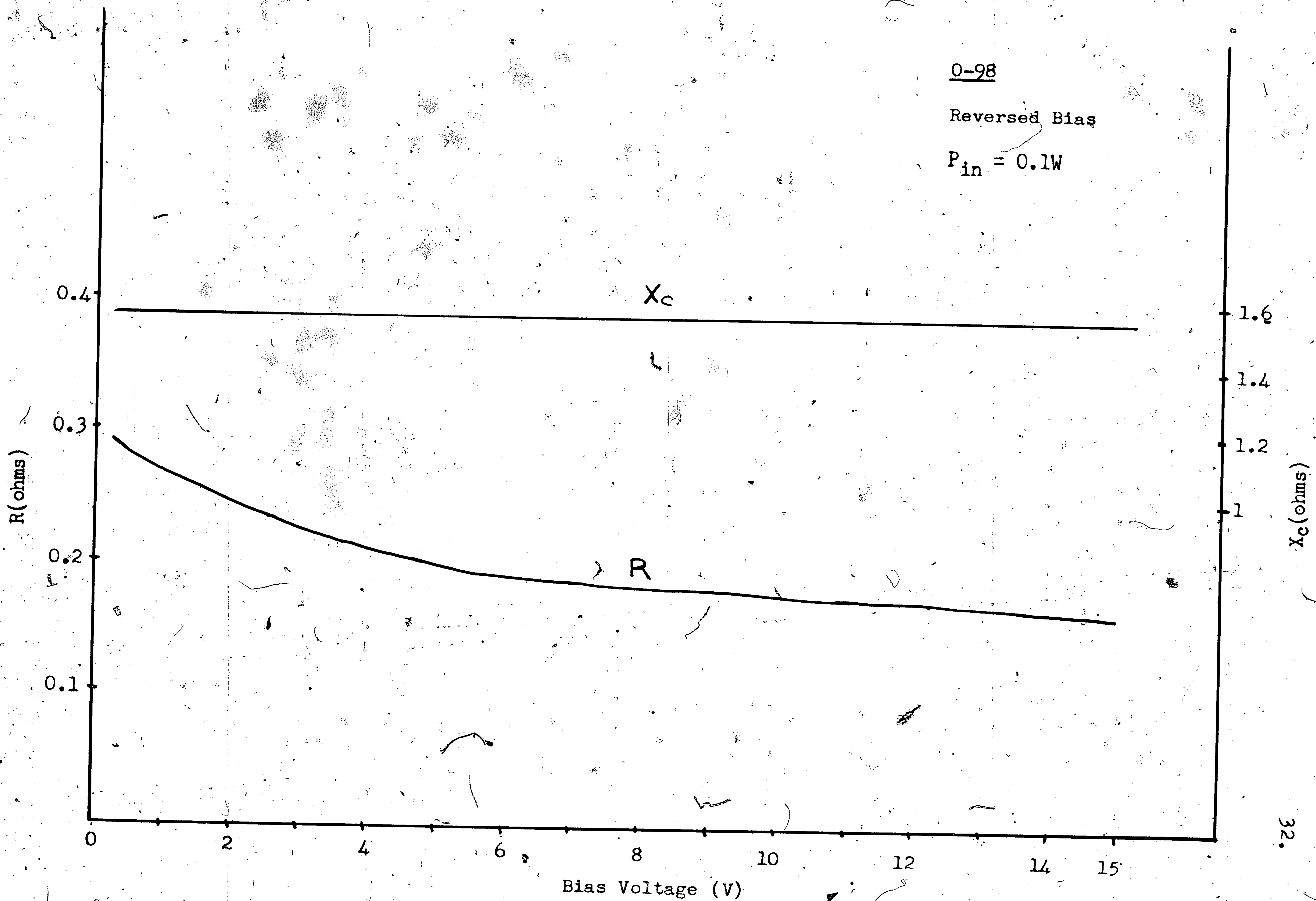


Fig. 14 R Versus V and X_c Versus V

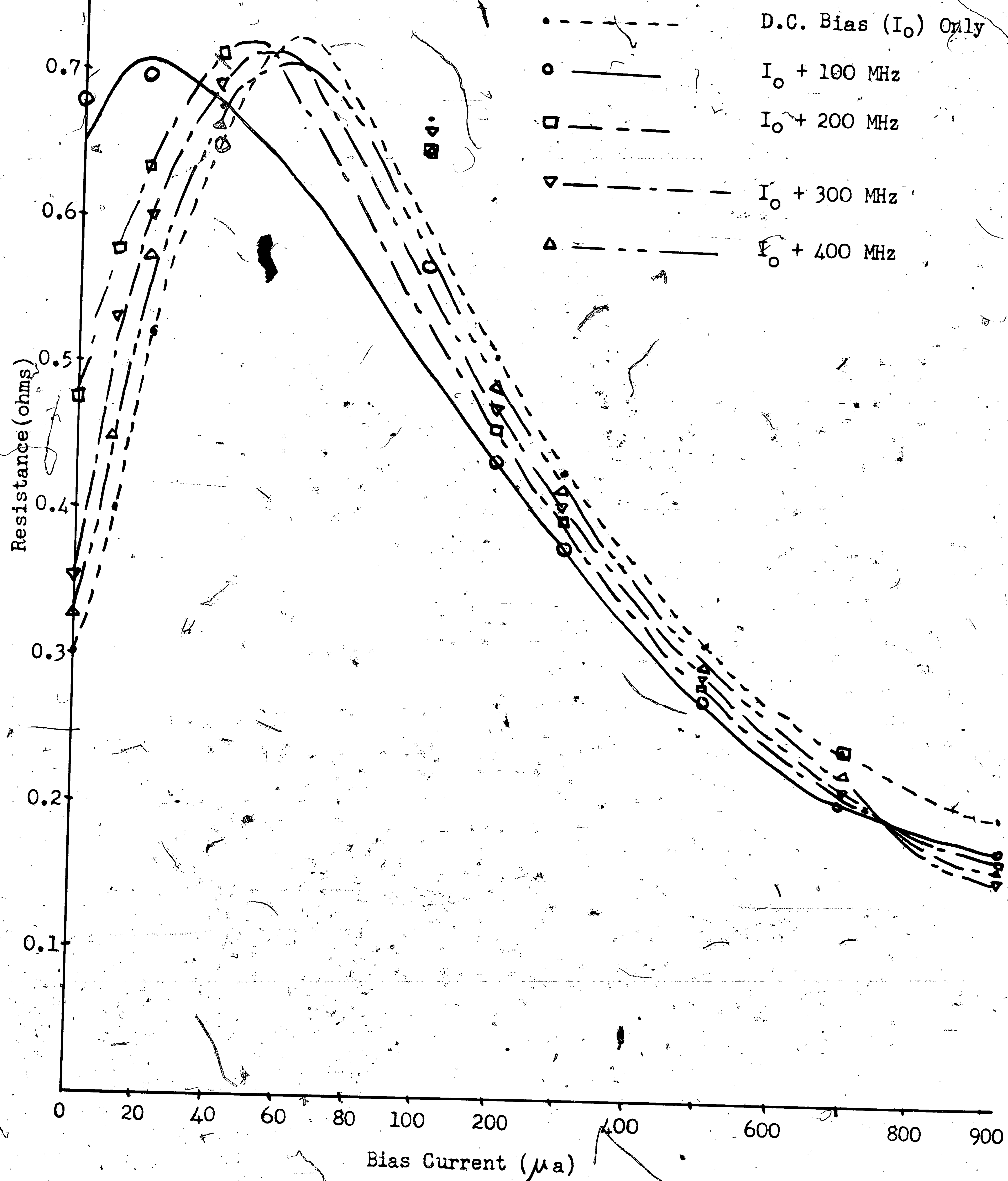


Fig. 15 Resistance Versus Bias Current

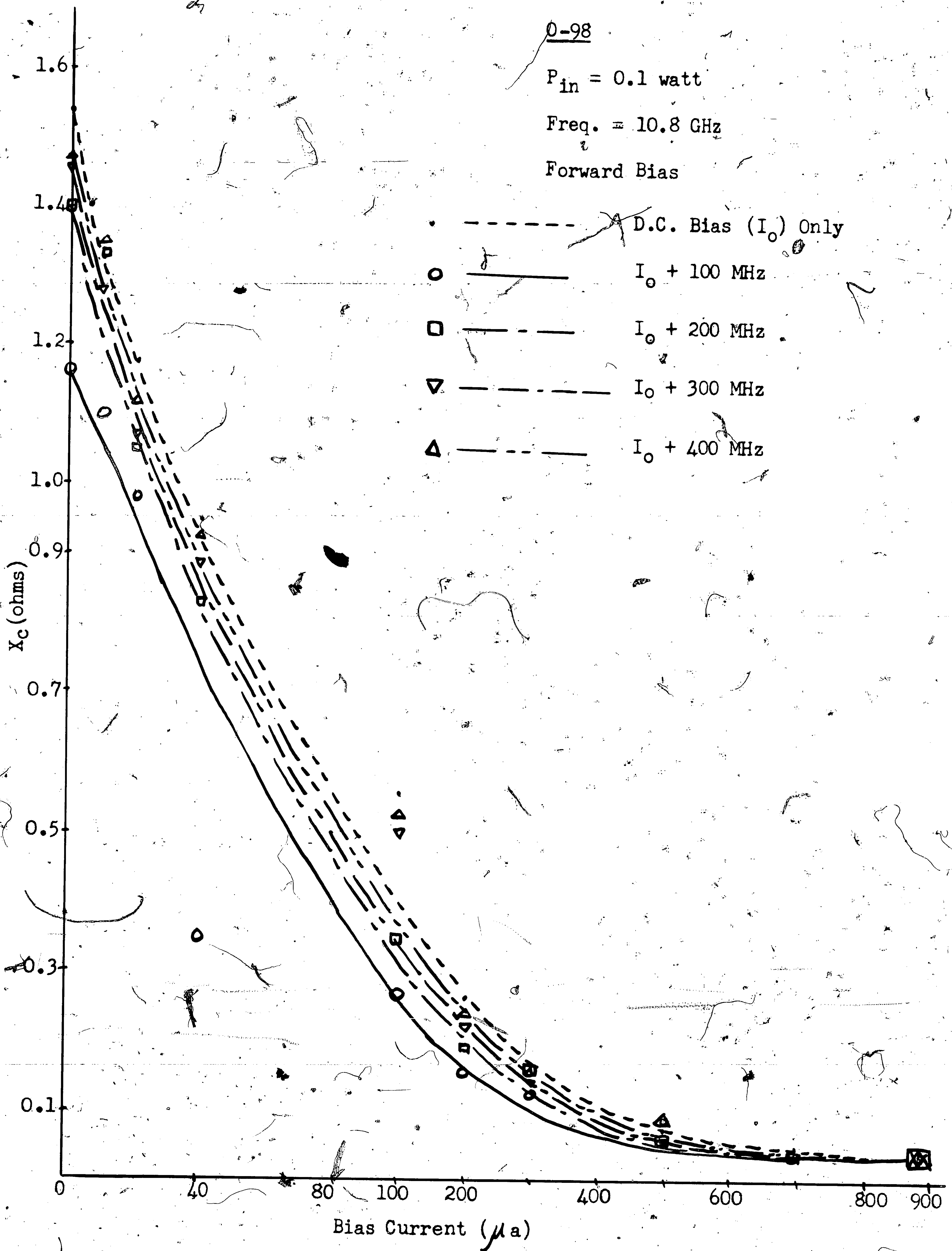


Fig. 16 Capacitive Reactance Versus Bias Current

TABLE I

Rectified Current for PIN Diode (0-98) at Zero D.C. Bias Current.

P_{in}	50 MH_z	60 MH_z	80 MH_z	100 MH_z	110 MH_z	120 MH_z	200 MH_z	300 MH_z	600 MH_z
0.03W	16.8 μa	10.5 μa	7.5 μa	9.2 μa	6.5 μa	3.5 μa	2.0 μa	0.2 μa	0.0
0.05W	26.5 μa	19.0 μa	15.5 μa	16.0 μa	12.0 μa	7.5 μa	2.2 μa	0.3 μa	0.0
0.10W	53.0 μa	43.0 μa	33.0 μa	31.0 μa	24.5 μa	16.75 μa	9.1 μa	1.0 μa	0.3 μa
0.15W	77.0 μa	62.0 μa	48.0 μa	45.5 μa	36.3 μa	26.0 μa	9.2 μa	1.5 μa	0.5 μa

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Vita

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