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A critical study of the chromium to n-type gallium-arsenide surface barrier

Richard W. Ralston
Lehigh University

A CRITICAL STUDY OF THE CHROMIUM TO ($\bar{1}\bar{1}\bar{1}$) N-TYPE GALLIUM-ARSENIDE SURFACE BARRIER

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Richard Wells Ralston

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Daniel Leenov

Professor in charge

John Karakash

Head of the Department

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ABSTRACT

A critical study has been made to clarify the causes of non-ideal behavior observed in the current-voltage characteristics of chromium to ($\bar{1}\bar{1}\bar{1}$) n-type gallium-arsenide surface barrier diodes. The means of analysis is a guard ring structure which greatly enhances the bulk components of diode current over the edge components.

At 300°K, the guarded forward current increases exponentially with voltage, the slope typically being q/1.06kT. This value is consistent with the simple diode theory in which image force lowering of the barrier is the only complication. At room temperature, it is the edge component of current which causes the non-ideal behavior of the unguarded diode.

At 77°K, the guard ring is not able to emphasize the ideal bulk current because of the thermionic nature of this current. Two current components are responsible for the non-ideal behavior of the cooled diode: an edge current with an anomolously low slope (range of q/2.46kT to q/4.59kT for various diodes) and a recombination current with a slope of approximately q/2kT (range of q/1.54 to q/2.27 for various diodes). The latter current, being the only one observed in the guarded characteristic, is a bulk

effect. It is attributed to a capturing of the electrons by fairly deep traps located within the space charge layer. From these traps, which are situated near the metal-semiconductor interface, the electrons enter the metal.

At both 300°K and 77°K, the reverse current is dominated by avalanche multiplication occurring as micro-plasmas.

On the basis of capacitance-voltage measurements and the Cowley-Sze model for such metal-semiconductor systems, the particular system employed is characterizable by an effective zero bias barrier height of 0.69 volts, a donor concentration of $2 \times 10^{16}/cm^3$, and an interfacial layer which is 10 Å thick and transparent to electrons.

I. INTRODUCTION

The purpose of this work is to clarify the causes of non-ideal behavior observed in the current-voltage characteristics of chromium to n-type gallium-arsenide surface barrier diodes. It is an outgrowth of a previous experimental evaluation[1] of certain metal to semiconductor rectifying contacts, in which the dependence of barrier height and current-voltage characteristic on the surface treatment and metal employed were investigated. Mead and Spitzer,[2] Cowley and Sze,[3] and many others have investigated the dependence of barrier height upon the metal work function, yet little effort has been made to understand the current-voltage characteristic of such surface barriers.

A major difficulty encountered by this author in earlier work was his inability to fabricate a surface barrier diode which would exhibit a current-voltage characteristic identical to that predicted by the theory of Schottky. The ideal surface barrier would possess

$$J = J_s \left(e^{qV/nkT} - 1\right)$$

as a current-voltage characteristic, with the parameter n equal to unity (1.00). Correction for the image force lowering of the barrier increases the ideal diode n slightly

(1.0?). Experimental values of n, however, were well above even the corrected parameter. The present analysis is an attempt to better understand the causes of this non-ideal behavior.

The metal-semiconductor contact, by its very nature, is expected to be greatly influenced by surface phenomena. For example, the sensitivity of the barrier height to the metal work function has been shown to be dependent upon the density of semiconductor surface states.[3,4] It is within reason, then, to propose that an excess component of current due to surface recombination is at least one cause of non-ideal behavior. A surface recombination component analogous to that hypothesized here was shown by Iwersen, et al[5] to exist in the base current of planar silicon transistors. The means of analysis was a guard ring structure which effectively isolated the active region of the emitter from surface recombination centers. A similar guarding device for surface barriers is not as easily fabricated as for junction emitters. The aim is to achieve a greater forward bias at the center of the metal contact than at the edge, thus confining the majority of current flow to a region not in intimate contact with the exposed semiconductor surface. Important details of fabrication will be mentioned later, as will the inherent awkwardness of the guard ring as an experimental tool for analyzing surface barriers.

Using chromium (Cr) to n-type gallium-arsenide (GaAs) surface barriers, this thesis shows that:

(1) This specific metal-semiconductor system may be characterized by an effective zero bias barrier height of 0.69 volts, and an interfacial layer which is 10 Angstroms thick and transparent to electrons.

(2) At room temperature the diode forward characteristic, when edge currents are suppressed, is consistent with thermionic diode behavior in which image force lowering of the barrier is the only complication.

(3) At liquid nitrogen temperature the unguarded diode forward characteristic is dominated by edge currents with anomolously low sensitivity to applied bias (n of 3 or more). The guarded diode characteristic is dominated by a recombination current in deep traps located at the metal-semiconductor interface (n of about 2).

(4) The reverse characteristic at both 300°K and 77°K is explainable by avalanche multiplication occurring as microplasmas.

II. FABRICATION DETAILS

1. Geometry

A structure with cylindrical symmetry lends itself to the problem at hand, that is; to crowd the current into the center region of the surface barrier. The potential difference between the center and the edge of the metal contact must be sustained in the metal, not in the semiconductor. The latter condition would cause emission crowding toward the edge, because the bias of the barrier would be greater at the periphery of the contact than at the center (assuming the metal contact to be an equipotential). Also, the power dissipation resulting from the guard ring current must not cause an appreciable rise in temperature. In junction devices such as the planar transistor, the bias difference can be supported in a shallow, high resistivity diffusion in the emitter region. Since a surface barrier is not a junction device, the structure shown in Figure 1 is the only possibility.

The underlying 18 mil diameter thin film is surmounted by a 4 mil diameter center dot and a guard ring with inner and outer diameters of 12 mils and 18 mils respectively. The ring and dot are much thicker than the underlying film, thus they may be considered to be of zero resistance, and so they make the inner and outer portions of the film equipotentials. It is the entire film which

forms the surface barrier with the semiconductor. The unprotected annulus between dot and ring must be thin enough to support the desired differential bias, yet thick enough to protect the semiconductor beneath from the atmosphere (or other diode ambient). Assuming uniformity of both sheet resistivity and current flow from dot to ring, the lateral resistance of the thin film annulus may be calculated as

$$R_a = \frac{\rho_s}{2\pi} \ln \frac{r_R}{r_D} .$$

For such conditions of uniformity, a logarithmic, radially symmetric voltage will result. See Figure 2.

2. Materials

GaAs is the logical semiconductor for this guard ring device, since previous experiments have shown n to be significantly greater than the ideal unity. The density of surface states for GaAs is high (order of 10^{14} states/cm^2-ev),(3) which makes GaAs surface barrier height rather insensitive to metal work function. Yet the dependence of metal-GaAs surface barriers on the surface states should cause such diodes to be readily affected by changes in surface conditions. If the diode current contains a significant surface component, then variation of surface conditions around the perimeter of the diode, but not under the actual metal contact, may produce a change in the diode's current-voltage

characteristic. A change in the interfacial states would most assuredly cause a variation in the I-V characteristic. The GaAs used is a .082 ohm-cm boat-grown crystal, doped with an impurity density of 2.8×10^{16} tellurium atoms/cm^3, and oriented in the [111] direction.

The choice of a metal for the rectifying contact is a severely limited one, because the resistive annulus between the dot and the ring must have sufficient resistance to support the desired bias difference without appreciable heating and yet be as thick as possible to protect the surface barrier beneath. At room temperature, a bias difference of .30 volts is expected to enhance the ideal (Schottky) diode current by four orders of magnitude. An acceptable power dissipation in the resistive annulus is 25 milliwatts or less, which means a resistance of 4 ohms or greater is desirable. Three metals often used in device fabrication possess room temperature resistivities of 10 micro ohm-cm or greater: chromium (13.0), tin (11.5), and platinum (10.0). Tin, however, readily alloys with GaAs and platinum is not easily evaporated, traits which make these two metals undesirable. For the background pressure and duration of evaporation of the chromium, it is expected that the sheet resistivity of the thin film will be a factor of two to three greater than that predicted by the bulk resistivity, that is; ρ_s is in the range 26 ohms per square to 39 ohms per square.(6) The desired 4 ohm Cr

annulus is expected to be between 110 Å and 170 Å thick. To maintain the non-porosity of this thin annulus the protective oxidation qualities of Cr will be helpful.

Gold (Au) or silver (Ag) is a satisfactory metal for the ring and the dot. Both are of low resistivity, are amenable to vacuum deposition techniques, and may be etched preferentially with respect to Cr and GaAs.

3. Processing

Mechanical polishing (Linde B abrasive) of both faces of the GaAs slice is a preliminary step. In addition the $(\bar{1}\bar{1}\bar{1})$ face (arsenic), or front, is given an electro-mechanical polish. A tin-nickel ohmic contact is fabricated on the (111) face (gallium), or back. This back contact is essentially that described by Sharpless.(7)

It is necessary to describe the chemical treatment of the front face because of the influence of surface states on the diode characteristics. The following surface preparation was chosen because of the good reproducibility of barrier height and current-voltage characteristics exhibited by surface barriers fabricated previously with it.(1) After formation of the back contact and immediately prior to the deposition of the Cr film, the specimen is:

(1) cleaned in hot trichloroethylene, then hot methanol;

(2) dipped for 60 seconds in a solution of 1 part hydrochloric acid and 1 part hydrofluoric acid, which is then decanted in methanol;

(3) ultrasonically agitated for 15 seconds in methanol;

(4) etched with ultrasonic agitation for 60 seconds in a phosphoric etchant (3 parts methanol, 1 part phosphoric acid, and 1 part hydrogen peroxide);

(5) ultrasonically rinsed in distilled deionized water to which a few drops of hydrochloric acid have been added;

(6) rinsed in flowing distilled deionized water;

(7) rinsed in warm methanol which is then decanted, so that the slice dries rapidly on the bottom of the beaker.

Immediately after the slice has been dried it is placed in an ionic vacuum system and evacuation is started. The precautions taken during the cleaning of the surface and the cleanness of the system should yield as clean a surface barrier as is presently attainable, except for cleaving the crystal in vacuum. Together with the GaAs, a sheet resistivity monitor is mounted in the vacuum chamber. Sublimation of the Cr from a tungsten filament is begun when the pressure reaches 2×10^{-8} Torr. A shutter placed between the filament and the targets allows accurate regulation of the film resistance. The evaporation of the upper metal is not as critical as that of the Cr, so a nominal layer of one micron is deposited.

Standard photoresist techniques are employed in etching the ring and dot pattern. First an 18 mil diameter sandwich of Ag (or Au) and Cr is formed. The dimensions of these spots are convenient when determining the barrier height of the rectifying contact by measurement of the capacitance-voltage characteristic. Subsequent to these capacitance measurements, an etching through a second photoresist mask produces the finished guard ring structure.

In order to achieve the minimum possible resistance in the contacts to the back, ring, and dot of the device, and to facilitate handling, each diode is mounted on a four pin header. Three 0.6 mil diameter gold leads are then thermocompression bonded to the device. Two of the leads are bonded separately to the dot. One will carry the large guard current and an appreciable voltage drop may result, but the other lead will carry only the actual diode current. Unfortunately the process of mounting the diodes on headers requires a temperature near the eutectic temperature of Au-GaAs and as was feared the Au on Cr units failed. Therefore the current-voltage characteristics of only the Ag on Cr units could be measured.

III. EXPERIMENTAL PROCEDURES

1. Capacitance-Voltage Measurements

The 18 mil diameter spots available after partial fabrication of the guard ring structure are subjected to capacitance measurements with a Boonton bridge at a test frequency of 1 Mc/s. An upward drift in capacitance with the diode under reverse bias is noticeable. The reason for this will be discussed later. It is found that the theoretical dependence of capacitance on the square root of the inverse of the bias is obtained for that capacitance value indicated by the bridge immediately after the application of the bias. Thus the technique adopted for all capacitance measurements is to set the conductance and capacitance scales such that a rough null is indicated, then remove the bias for 10 seconds, and upon reapplying the bias obtain a better null. This procedure is continued until a null is indicated immediately upon application of the bias. The voltage range for the capacitance-voltage measurements is 0.200 to -2.00 volts.

2. Forward Current-Voltage Characteristic

The circuit used to obtain the current-voltage characteristic is shown in Figure 3. All measurements are made with the diode in a dark enclosure. The technique employed is to hold the differential bias (V_G) between the

dot and the ring at a constant level while varying the forward bias (V_D) of the dot with respect to the ohmic back contact. Diode current (I) between 10^{-9} amperes and 10^{-2} amperes is investigated, with the corresponding guard current (I_G) and forward bias being recorded for each decade of diode current. For I no greater than 10^{-4} amperes the bias voltage must be corrected for the drop across the ammeter, which is in series with the diode, while for I values no less than 10^{-4} amperes the voltmeter is shunted directly across the diode and no such correction is necessary.

The forward I-V characteristic of each diode is evaluated under a variety of ambients. These ambients, together with the experimental procedure peculiar to each, are listed below in the order in which the diode is subjected to them.

(1) Room atmosphere at room temperature: All diodes are evaluated for guard voltage levels of .00, .10, .13, .20, .30, and .40 volts, and some are also subjected to V_G levels of 1.0 and 1.5 volts. Note that in all cases (1 - vii), the zero guard voltage condition is that of a short circuit. Because of the tendency of the device to guard itself, the upper range of diode current ($10^{-4} \leq I \leq 10^{-2}$) can not be fully investigated for low non-zero guard voltages ($.10 \leq V_G \leq .30$).

(ii) Immersed in liquid nitrogen (77°K): All diodes are evaluated for guard voltage levels of .00, .10, .13, .20, .30, and 1.0 volts, and in addition some are subjected to levels of 1.5 and 2.0 volts.

(iii) Wet nitrogen at room temperature: The diode under test is placed at the mouth of a plastic tube, through which wet nitrogen is directed at a rate of 1.0 standard liters per minute (SLPM). The moisture is introduced by bubbling the nitrogen through deionized water. The guard voltages used are identical to those listed for the atmospheric ambient (i).

(iv) Dry carbon dioxide at room temperature: The experimental procedure is similar to that for the wet nitrogen ambient, the change being the removal of the water bubbler from the gas line. In addition to the normal measurements, the sensitivity of the diode's I-V characteristic to the flow rate of the carbon dioxide is investigated. This is done by setting a particular diode current I for 0.0 SLPM, then recording the change in I after a 2.9 SLPM flow for 60 seconds. The change in I is recorded for various initial levels of I and V_G.

(v) Repeat with a waxed diode: A drop of apeizon wax dissolved in trichloroethylene is placed on a diode and allowed to dry for at least 24 hours at room temperature. The diode is then subjected to the wet nitrogen (iii) and dry carbon dioxide (iv) ambients in the same fashion as described above. This is done for only a few diodes.

(vi) Repeat with a dewaxed diode: The apeizon wax is dissolved in trichloroethylene, the diode is thoroughly dried, and it is then evaluated in room atmosphere as described in (i) above.

(vii) Repeat with an etched diode: The resistive Cr annulus is etched away. Current-voltage characteristics are then determined for the diode in room atmosphere (i), liquid nitrogen (ii), and carbon dioxide at 1.0 SLPM (iv) in the way peculiar to each ambient. Note that for the etched diode a change is made in the test circuit. Only those few diodes which are waxed (v) and dewaxed (vi) are etched.

3. Reverse Current-Voltage Characteristic

Measurements of the reverse characteristic are also made with the circuit depicted in Figure 3. All measurements are made with the diode in a dark enclosure and with the ring short circuited to the dot (zero V_G). At the time when the reverse characteristics are determined, the diode has been subjected to only the forward characteristic ambients of room atmosphere and liquid nitrogen. These same two ambients are employed here, with the reverse current (I_{rev}) being measured in decade steps between 10^{-9} amperes and 10^{-3} amperes.

4. Visual Inspection

At the conclusion of the electrical testing, all diodes are inspected with the aid of a microscope in an effort to detect any irregularities in the structure, particularly in the resistive Cr annulus. In an attempt to discover pin-holes in the Cr, some diodes are also inspected under interference-contrast, a microscopic illumination and viewing scheme that greatly enhances surface irregularities.

IV. EXPERIMENTAL RESULTS

1. Capacitance-Voltage Measurements

The energy band diagram for a Cr to n-type GaAs surface barrier is shown in Figure 4. This system is not an ideal Schottky barrier because provision is made for semiconductor surface states and an interfacial layer.[3] A typical experimental plot of the square of the reciprocal of the barrier capacitance as a function of applied voltage is shown in Figure 5.

Assuming uniform doping and complete ionization of donor impurities, absence of minority carriers, and an absence of space charge effects in the interfacial layer, the doping density is obtained from the slope of the $\frac{1}{C^2}$ - V plot as[8]

$$N_D = \frac{2}{\varepsilon_s \varepsilon_o q A^2} \frac{\Delta V}{\Delta \left(\frac{1}{C^2}\right)} = 4.2 \times 10^{12} \frac{\Delta V}{\Delta \left(\frac{1}{C^2}\right)} \text{ cm}^{-3} \qquad (1)$$

All symbols are defined in an appendix. The static dielectric constant (ε_s) of GaAs is taken as 12.5.[9] Once the donor concentration is determined, the barrier height (Φ_{Bn}) may be calculated, under the above assumptions, by the relation[3,8]

$$\Phi_{Bn} \cong V_{int} + V_F + \frac{kT}{q} - \Delta\Phi_n - \sqrt{2q\varepsilon_s\varepsilon_o N_D V_{int}} \frac{\delta}{\varepsilon_1 \varepsilon_o}$$

$$- \left[\frac{q\varepsilon_s\varepsilon_o N_D}{2}\right] \frac{\delta^2}{\varepsilon_1^2 \varepsilon_o^2}, \qquad (2)$$

where V_{int} is the voltage intercept (at infinite capacitance) of the experimental plot, V_F is the separation of the conduction band edge and the Fermi level, $-\Delta\Phi_n$ is the image force barrier lowering,[10] and δ is the interfacial layer thickness. In addition to the conditions imposed above, it is assumed that the interfacial layer is so thin (a few Angstroms) that it has the permittivity of free space ($\varepsilon_1 = 1$) and it is essentially transparent to electrons.

The voltage intercepts and slopes of all $\frac{1}{C^2} - V$ plots are tightly grouped, with no noticeable difference existing between those with Au on Cr contacts and those with Ag on Cr contacts. For each device the doping density and the corresponding conduction band edge to Fermi level separation is calculated. With these quantities the barrier height, as yet uncorrected for image force lowering, is determined for each diode assuming an interfacial layer thickness of 10 Å (approximately a double layer of atoms). The average of the uncorrected barrier heights ($\Phi_{Bn}+\Delta\Phi_n$) is subsequently corrected for the lowering due to the image force. This correction for a uniformly doped semiconductor is[10]

$$\Delta\Phi_n = \left[\frac{q^3 N_D}{8\pi\varepsilon_o{}^3\varepsilon_d{}^2\varepsilon_s}\left(V_B - \frac{kT}{q} - V\right)\right]^{1/4} \qquad (3)$$

where the built-in voltage (V_B) is simply V_{int} + kT/q and the image force dielectric constant (ε_d) may be taken as unity because the short transit time of electrons to the point of maximum potential energy allows little polarization of the dielectric.

A complete analysis as outlined above yields the following average quantities.

$$N_D = 2.0 \times 10^{16}/cm^3$$

$$V_F = 3.2\ kT/q$$

$$\Phi_{Bn} + \Delta\Phi_n \approx .800 + 4.2\ kT/q - .087 \text{ volts}$$

$$\Delta\Phi_n = .140\ (.800-V)^{1/4} \text{ volts}$$

The effective barrier height at room temperature and zero bias, Φ_{Bn_o}, is found to be .69 volts.

2. Forward Current-Voltage Characteristic

Figure 7 is a typical experimental I-V characteristic for the forward direction. Note that the current is plotted not as a function of the dot voltage (V_D) but rather as a function of the bias between the guard ring and the back contact ($V_R = V_D - V_G'$). It is this bias, V_R, which determines the amount of edge current. Hence for a specific value of V_R on the abscissa, each of the curves in Figure 7 contains an identical amount of edge current. The increase in current as one proceeds upward along a

(vertical) line of constant V_R is due entirely to enhancement of bulk current. Notice that V_G' is constant for a given I-V characteristic; hence this is also a plot of I versus V_D with the abscissa transposed. A resistance of .5 ohm has been ascribed to each thermocompression bonded lead, and the series combination of lead and annulus resistances is obtained experimentally. The values of differential bias employed in the respective translations of the I-V curves have been corrected for the IR drop in the two leads of the guard circuit, since it is only the actual voltage drop across the annulus which is the ring to back bias. It is the corrected V_G value (V_G') which is used to find the expected enhancement (I/I_{o_e}) of the non-edge current.

An IR drop also exists in the diode proper which will appear at appreciable current levels. This resistance is a series combination of lead resistance and substrate spreading resistance. For uniform current flow from a circular contact of radius r into a semi-infinite slab of resistivity ρ, the spreading resistance is $\rho/\pi r$. Because the current flow in the guard ring structure becomes non-uniform for a non-zero V_G', and because the resistive annulus presents significant resistance to that portion of the diode current not confined under the dot, $\rho/\pi r$ + .5 ohms is at best a crude approximation to the

actual resistance in the path of the diode current. No quantitative correction of the diode current for the IR drop has been undertaken. Qualitatively it is expected that for an increasing guard voltage between dot and ring the diode resistance should increase. And indeed all diodes possess such an increase in resistance. This increase is especially evident for currents of at least 10^{-3} amperes, a range not included in Figures 7 and 8. A quantitative correction is not necessary, because in the range of diode current where edge currents may be significant, the resistance is too small to noticeably affect the slope of the I-V plot.

For a Schottky diode in which thermionic diode theory is applicable, the current density is

$$J = A^{*}T^{2}e^{-q\Phi_{Bn}/kT}\,(e^{qV/kT}-1).$$

Ignoring, for now, the effect of the image force of the barrier height, and considering the forward bias, V, to be greater than 3kT/q, the current of the experimental diode is apt to follow

$$I \propto e^{qV/nkT}$$

quite closely. The parameter n is easily obtained from the I-V plot as

$$n = \frac{q}{kT}\left[dV/d(\ln I)\right].$$

Notice that although the plots in Figures 7 and 8 are made against an abscissa of $V_D - V_G'$, on a given characteristic curve $d(V_D-V_G') = d(V_D)$, and thus n can be obtained directly from such plots. It is expected that the value of n will approach the theoretical value for the bulk current as the bulk current of the diode is emphasized. Such bulk current, although it is expected to consist entirely of ideal Schottky current, may also contain a recombination component. The n for ideal Schottky current, uncorrected for image force lowering of the barrier height, is unity, while the n for recombination current is dependent upon the distribution of traps within the energy gap.[11] For the most effective trap level (deep traps), n is approximately two.

For a completely forward biased structure ($V_R>0$) the expected enhancement of a component of barrier current over the edge current is (see Appendix A)

$$\frac{I}{I_{o_e}} = 1 + \left(\frac{r_R}{r_o}\right)^2 \left(\frac{s}{s-2}\right)\left[\left(\frac{r_R}{r_D}\right)^{s-2} - 1\right] \tag{4}$$

$$\text{where } s = \frac{q}{kT}\left[\ln\left(\frac{r_R}{r_D}\right)\right]^{-1} \frac{V_G'}{n} . \tag{5}$$

The value assigned to n is dependent upon the type of barrier current. A plot of I/I_{o_e} as a function of s is shown in Figure 6. Notice that a transfer plot, for a constant V_R (constant edge current), of I_D vs. V_R+V_G' (taken from Figure 7) would possess, ideally, the same

shape as the plot of I/I_{o_e} vs. s. The parameter s, for a given temperature and guard voltage, will be approximately twice as great for the Schottky component of barrier current as for any appreciable recombination current (shallow traps have $n \approx 1$, but are far less effective in producing current than deep traps). From Figure 6 it is evident that the Schottky current is enhanced much more than any non-edge recombination current. It is expected, then, that for sufficiently high V_G' the experimental value of n will coincide with that value of n for pure Schottky emission. As a precaution only those portions of the I-V characteristics for which $V_R>0$ are used to deduce n. If $V_R<0$ the ring is biased in reverse with respect to the back, and reverse currents flowing in the outer portion of the device tend to decrease the indicated bulk current. Such a process would produce an indicated n lower than the true value.

(i) Atmosphere, 300°K

Figure 7 indicates the typical I-V characteristic in the forward direction for a diode subjected to room ambient. Both the nominal and corrected differential biases are indicated. Originally unguarded, this diode exhibits an n of 1.16 over 4 decades of current. A valid minimum n of 1.04 is reached over 2 decades of current at a nominal guard voltage of .30 volts. The actual enhancement of current I/I_{o_a} (evaluated at $V_R = V_D - V_G' = .100$ volts) is far below the expected enhancement I/I_{o_e}, even

though I/I_{o_e} is calculated using an n of 1.06 (appropriate to the image force on the barrier in the V_D bias range of interest) and the corrected guard voltage V_G'. The results for all diodes are summarized in Table 3. Entries for unit #8 are made more detailed as an aid to interpreting Figure 7. For all other diodes, only the parameters of the I-V characteristics relating to the unguarded and most effectively guarded surface barriers are shown. Diodes which visual inspection showed to be of faulty construction and those which were accidentally killed (guard ring lead melted due to excessive guard current) are not considered.

(ii) Liquid nitrogen, 77°K

Illustrated in Figure 8 are the typical I-V characteristics in the forward direction for a diode immersed in liquid nitrogen. These characteristics, and those displayed in Figure 7, are for the same diode. A significant decrease in the resistance of the Au leads and Cr annulus occurs upon immersion of the unit. Let it be assumed that Au and Cr have equal temperature coefficients of resistivity. Such an approximation is certainly within the limits of accuracy set by the initial assumption of .5 ohms resistance for each Au lead and contact. The condition of equal temperature coefficients of resistivity for the two metals implies that a voltage division between

though I/I_{o_e} is calculated using an n of 1.06 (appropriate to the image force on the barrier in the V_D bias range of interest) and the corrected guard voltage V_G'. The results for all diodes are summarized in Table 3. Entries for unit #8 are made more detailed as an aid to interpreting Figure 7. For all other diodes, only the parameters of the I-V characteristics relating to the unguarded and most effectively guarded surface barriers are shown. Diodes which visual inspection showed to be of faulty construction and those which were accidentally killed (guard ring lead melted due to excessive guard current) are not considered.

(ii) Liquid nitrogen, 77°K

Illustrated in Figure 8 are the typical I-V characteristics in the forward direction for a diode immersed in liquid nitrogen. These characteristics, and those displayed in Figure 7, are for the same diode. A significant decrease in the resistance of the Au leads and Cr annulus occurs upon immersion of the unit. Let it be assumed that Au and Cr have equal temperature coefficients of resistivity. Such an approximation is certainly within the limits of accuracy set by the initial assumption of .5 ohms resistance for each Au lead and contact. The condition of equal temperature coefficients of resistivity for the two metals implies that a voltage division between

the leads and the annulus will be of constant proportions regardless of the device temperature. It is upon this basis that the V_G' values employed in the respective voltage translations of the I-V curves for devices at 77°K have been corrected for IR drop in the two leads. Both the nominal and corrected guard voltages are indicated in Figure 8.

When in an unguarded state, diode #8 exhibits an n of 3.92 over 3 decades of current. A valid minimum n of 2.06 is reached over 5 decades of current at a nominal guard voltage of 1.0 volts. These slopes are markedly different than those recorded at room temperature for the same diode. It appears that barrier recombination current ($n \approx 2$) is enhanced over an edge recombination current. Despite the inherent tendency of the guard ring structure to enhance Schottky current to a much greater degree than it enhances current of higher n, no ideal Schottky current is visible in Figure 8. The results for all diodes are summarized in Table 4. Because of the pronounced recombination current present, the expected enhancement (I/I_{o_e}) of barrier current is calculated using an n of 2.0. The actual enhancement of current (I/I_{o_a}), which, when possible, is evaluated at a V_R value of .65 volts for consistency, falls far short of the expected value.

(iii) Wet nitrogen, 300°K

The results of this phase of the experiment are disappointing. Hypothetically, a change in the ambient will induce a change in the edge component of current, and this change would be evident in the characteristic of an unguarded diode. Yet if the Cr annulus is non-porous to the ambients (thus able to afford protection to the metal-semiconductor interface), there will be no change in the characteristic of a guarded diode for which the barrier currents have been sufficiently enhanced.

Wet nitrogen is unsuitable for such a study because leakage in the water film which condenses on the surface of both the diode and the header swamps out the lowest three decades (10^{-9} to 10^{-6} amperes) of the diode I-V characteristic. The great increase in current definitely can not be attributed to a change in surface states and a corresponding increase in edge current. A unit to which leads had not been stitched was completely covered with wax, then measured in the same manner as the actual diode. The I-V characteristic in the 10^{-9} to 10^{-6} ampere range was identical to that observed for the active diode. For the waxed, unstitched unit the only possible path of current flow is the film of condensate.

(iv) Dry carbon dioxide, 300°K

As a check of the dryness of the carbon dioxide, the waxed, unstitched unit was subjected to a flow rate

of 1.0 SLPM. Leakage currents no greater than 10^{-11} amperes were recorded, so this ambient was dry enough. Because of a four to five month time lag between initial atmospheric I-V measurements and those made in dry CO_2, those diodes which were to be subjected to the CO_2 ambient were first remeasured in room air. Unit #8, for instance, when re-measured shows an unguarded n of 1.17 (3 decades) which can be decreased only to 1.09 (4 decades) by the guard ring structure. Comparison with the earlier characteristic, which showed a decrease in n from 1.16 to 1.04, indicates deterioration of the guarding mechanism. That the deterioration is a direct result of the Cr annulus becoming more porous through oxidation is supported by an observed rise in resistance of the guard circuit (two leads and annulus) from 3.64 ohms to 3.83 ohms. Other diodes show similar increases in annulus resistance and degradation of guarding ability.

The flow (at 1.0 SLPM) of dry CO_2 over diode #8 causes no change in the unguarded characteristic, the n value still being 1.17 (3 decades). Now, however, n can be decreased to only 1.10 (4 decades). Hence the CO_2 is slightly affecting the non-edge components of current. An explanation of the manner in which the CO_2 affects the surface states of the diode is not readily given because of the anomolous results obtained by changing the ambient

flow rate. It is found that increasing the flow rate decreases the current for a constant dot bias. Furthermore, the percentage decrease in current increases with increasing differential bias between dot and ring. Characteristically, the percentage decrease in current is a peaked function of the reference current (at 0.0 SLPM), the peak occurring at higher reference currents for greater guarding voltages. This behavior is indicated in Table 1. It is of interest to note that the maximum sensitivity to the flow rate occurs when the ring has approximately zero bias with respect to the back contact.

Table 1

Typical Effect of CO_2 Flow Rate on Unwaxed Diode (Unit #14)

Nominal differential bias, V_G	.00	.20	.40
Ring bias, V_D-V_G', for maximum % current change	~.00	~.05	~.05
Reference current (at 0.0 SLPM CO_2)	10^{-11} to 10^{-10}	10^{-9} to 10^{-8}	10^{-8}
Maximum decrease in current (at 2.9 SLPM CO_2)	2%	3%	12%

(v) Waxed variations, 300°K

Those devices which are waxed show improved guarding qualities. In all cases the n for an unguarded waxed diode is higher than the n for the same unguarded unwaxed diode, yet upon application of sufficient guard

voltage the diodes show lower n values when waxed. As an example, unit #8, when waxed and subjected to 1.0 SLPM CO_2, possesses an unguarded n of 1.24 (5 decades) which can be reduced to 1.07 (2 decades). Table 5 facilitates comparison of the effectiveness of the guarding mechanism under various ambient conditions. Observe that even with wax, the minimum n obtained is greater than the n obtained months earlier for the then recently fabricated device. Also note that the dewaxed diode has characteristics identical to those measured prior to waxing. Since in the unguarded mode, the waxed diode has a significantly higher n than the unwaxed diode, it is deduced that the waxing process causes a reversible change in the surface states of the exposed GaAs. The wax also repairs, although not completely, the Cr annulus by stopping up the pores and thus shielding the GaAs beneath. This partial repair is indicated by both the change in minimum n and the decreased sensitivity to flow rate for the waxed devices (Table 2) as compared to the same unwaxed devices (Table 1).

Table 2

Typical Effect of CO_2 Flow Rate on Waxed Diode (Unit #14)

Nominal differential bias, V_G	.00	.40
Ring bias, V_D-V_G' for maximum % current change	.00	-.05
Reference current (at 0.0 SLPM CO_2)	---	10^{-8}
Maximum decrease in current (at 2.9 SLPM CO_2)	0%	8%

That the repair of the guarding mechanism is only partial may be attributed to the porosity of the wax and/or to a reversible change in the surface states below the annulus. Just as with the unwaxed diodes, the anomoly of a sensitivity to flow rate which increases with increasing differential bias is present.

(vi) Etched variations

Etching away the resistive annulus destroys the guard mechanism. The absence of the annulus causes any bias differential between the dot and the ring to be dropped across the semiconductor itself rather than the metal contact. Such a distribution causes a crowding of current toward the edges of the dot and the ring rather than the enhancement of the dot current achieved with the annulus intact. Hence the diode is expected to behave like an ideal Schottky barrier to a lesser degree as the bias differential is increased, because the edge current will be enhanced. Indeed, an increasing differential bias, for all three ambients investigated, is accompanied by an increasing n. The results for a typical diode are summarized in Table 4. At 77°K the increase in leakage current is especially evident; the lower (10^{-9} to 10^{-7} ampere) range of the I-V plot becomes progressively more concave upward as V_G is increased.

3. Reverse Current-Voltage Characteristic

Log-log plots of typical reverse characteristics of a diode at room temperature and at liquid nitrogen temperature are presented in Figure 9. Notice that the abscissa is the applied reverse bias plus the built-in voltage of the barrier. Sah, Noyce, and Shockley have shown that for the reverse component of current due to generation-recombination a relationship of the form

$$I_{gr} \propto (V_B + V_{rev})^m$$

is to be expected. For moderate reverse bias the Schottky current, because it is saturable (the image force lowering of the barrier is small), will be negligible with respect to the non-saturating generation component, and so the experimental plot of I_{rev} should follow the exponential dependence on $V_B + V_{rev}$. Ideal volume or edge space charge generation (i.e., generation at the surface of the semiconductor around the perimeter of the ring, where the edge of the space charge layer comes to the surface) will possess an $m = \frac{1}{2}$ because of the dependence of the width of the layer on the square root of the voltage.[11] The numbers shown on Figure 9 indicate the values of m for the adjacent portions of the curves. For all diodes, the m values are at least two in the lower voltage range. Such high values may not be ascribed to volume space charge

generation or to pure edge space charge generation. The m values for the upper voltage range are relatively insensitive to temperature change, and the increase in current with voltage is very rapid. This behavior is characteristic of avalanche multiplication.[12]

An activation energy plot, based on the procedure of Sah, Noyce, and Shockley,[11] is shown in Figure 10. The reverse current at a bias of four volts is normalized by $T^{3/2}$ and plotted in a semi-log fashion against the reciprocal of the temperature. The activation energy of the dominant generation centers is obtained from the slope of the plot as

$$E_a = -k10^3 \frac{\Delta\left\{\ln(I_{rev}/T^{3/2})\right\}}{\Delta\left\{\frac{10^3}{T}\right\}} .$$

Very low activation energies are observed (~.015 ev), implying the existence of extremely shallow generation centers. The trap level (E_t) is separated from the intrinsic Fermi level (E_i) by approximately[11]

$$E_t - E_i = \frac{1}{2} E_g - E_a .$$

This places the level within kT (at room temperature) of the conduction band edge.

V. DISCUSSION

Certain of the experimental results will now be discussed in further detail. Significant implications concerning the porosity or non-porosity of the thin chromium film are pointed out in Section 1. Section 2 concerns the capacitive measurements of the doping density and barrier height. A trapping mechanism is used to explain the observed upward drift in capacitance for a reverse-biased diode. The existence of such traps, the presence of an interfacial layer, and an overestimation of the barrier area are considered as possible causes of error in the experimental values for doping density and barrier height. Also in Section 2, comparison is made between the experimental barrier height and that predicted by the theory advanced by Cowley and Sze.

Section 3 is concerned with the room temperature current-voltage characteristics. Four reasons why the actual (experimental) enhancement of bulk current is less than the expected (theoretical) enhancement are explored. For the forward characteristic, the theoretical n, corrected for the appropriate image force, is found to be in reasonable agreement with the experimental value. The reverse characteristic is probably caused by localized avalanching. Of particular interest are the current-voltage

characteristics at liquid nitrogen temperature, discussed in detail in Section 4. Absence of a Schottky current is ascribed to its strong thermal dependence. The presence of an $n \approx 2$ current for the guarded diode implies that a recombination current is flowing, and that it is central rather than peripheral in nature. Two mechanisms, one of field assisted minority carrier injection and the other of electron trapping by centers located within the space charge layer, are explored as possible causes of the predominant central recombination current.

1. Non-porosity of Chromium Layer

Several phases of the experiment yield information on the nature of the thin film of Cr lying between the dot and the ring. A continuous film will allow maximum possible enhancement of bulk currents over edge currents by allowing the edge of the space charge layer to rise to the surface of the GaAs only beyond the perimeter of the ring. Should pinholes exist in the film, the effective value of the perimeter would increase and the enhancement of bulk current would not be as easily realized.

That pinholes of an appreciable density did exist on the diodes soon after deposition of the Cr is indicated by the failure of the Au on Cr units while bonding the individual diodes on headers. What probably occurred here is that gold, lingering in the pinholes

after etching and directly in contact with the semiconductor, alloyed into the substrate when the eutectic temperature for Au-GaAs was reached during the bonding process. Yet the pinhole density was not too high originally, because the barrier heights were the same for the (partially fabricated) Au on Cr diodes as for the Ag on Cr diodes. Also, the enhancement of the bulk current for the fresh diodes at room temperature was sufficient to show pure Schottky behavior. No pinholes could be detected visually, but this is attributed to insufficient magnification. With the passing of time, the guard ring structure definitely began to fail, as evidenced by the inability to attain pure Schottky behavior with the same diodes which behaved "ideally" at an earlier date. The deterioration is ascribed to slow oxidation of the Cr. Although Cr is a member of the group of metals which forms protective oxides, it must be that over a span of months the very thin film does become porous. The hypothesized increase in porosity is corroborated by the observed increase in guard circuit resistance.

Directing a regulated stream of dry CO_2 at the diode does cause a slight increase in the observed minimum n as compared to the same diode in room atmosphere. This

is attributed to some unknown mechanism by which the CO_2 changes the surface states of the GaAs, thus making the edge current contribution of the pinholes significant. The edge current arising at the perimeter of the ring, even though similarly affected by the CO_2, can be nullified by the application of sufficient differential bias. The pinhole edge current, however, can not be so nullified, especially for those pinholes immediately surrounding the dot. Even covering the diode with wax does not completely repair the guarding capabilities of the structure, but the incompleteness may be due to a reversible change in the surface states of the GaAs caused by the trichloroethylene and wax. No clue to understanding the mechanism by which CO_2 affects the surface states has yet been found If a clue exists, it lies hidden in the manner in which the change in CO_2 flow rate changes the diode current. Why does an increase in flow rate decrease the edge current, why does an increase in differential bias increase the sensitivity of the edge current to changes in the flow rate, and why does maximum sensitivity occur when the ring is at zero bias with respect to the back? These questions will not be answered here. The fact that waxing the diode does decrease the sensitivity to the flow rate is offered as further evidence that pinholes exist and that they do contribute edge currents. Yet the sensitivity

of diode current is still present in the wax covered diode, and the thick layer of wax is not suspected of being porous, so even a completely non-porous Cr film would presumably fail to shield the surface barrier from the mysterious influence of CO_2.

2. Doping Density and Barrier Height

The calculation to determine the donor density involves the slope of the experimental $\frac{1}{C^2}$ - V plot. Monsanto, the supplier of the GaAs, claims an impurity density of 2.8×10^{16} atoms/cm^3, while the differential capacitance method indicates a density of only 2.0×10^{16} atoms/cm^3. Although this discrepancy is not of drastic proportion, and the experimental result is more reliable than Monsanto's estimate, it is of interest to discuss the possible causes for obtaining a low doping density. First to be considered is the upward drift in capacitance seen when the diode is under reverse bias. Such a phenomenon was also observed by Goodman,[8] when making similar measurements on cadmium-sulfide (CdS). He offers a simple explanation in terms of a trapping mechanism. Under reverse bias, traps which are normally full and neutral might slowly ionize by emptying down to a level ΔE below the conduction band, the energy ΔE being dependent on the duration and the magnitude of the applied bias. It was found that for CdS a period of 20 minutes at a given reverse bias was sufficient to reach a steady

capacitance value. Under such conditions the reverse bias portion of the $\frac{1}{C^2}$ - V plot is expected to have a downward curvature, since in this region

$$\frac{\Delta(1/C^2)}{\Delta V} = \frac{2}{\varepsilon_s q A^2} \frac{1}{(N_D+\beta N_t)}$$

N_t is the trap density and β is that fraction of the traps which are empty (ionized) for a certain magnitude and duration of bias. As either magnitude or duration of bias increases, β is expected to increase, finally reaching unity for sufficiently large bias and time. Since the experimental procedure employed was to take capacitance readings "simultaneous" to the application of bias, it is probable that β approaches zero for traps of sufficiently long release times. Hence the drift observed indicates the presence of slow trapping levels below the conduction band, but because of the measurement technique, such traps could not have produced the low N_D value obtained.

Also to be considered is the possible effect of the insulating interfacial layer on the slope of the $\frac{1}{C^2}$ - V plot. This layer is postulated to have a permittivity equal to that of free space and to be free of space charge effects. Let it be assumed that the surface charge density (Q_{ss}) does not vary with applied bias, and also that the voltage drop (V_1) across the layer is constant.(8)

These assumptions are logical extensions of the fact that the high density of surface states "pins" the Fermi level at the surface, and of the previous assumption relating to the electron transparency of the interfacial layer. In other words, the surface state charge density is a function only of the semiconductor surface, and all of the applied bias is superimposed on the effective barrier, Φ_{Bn}. Now the capacitance measured is a dynamic capacitance, where the capacitance per unit area is given by

$$\frac{C}{A} = \frac{d(Q_{ss} + Q_{sc})}{dV}$$

Under the supposed conditions, dQ_{ss}/dV equals zero, and $(A/C)^2$ varies linearly with V. Hence the interfacial layer does not affect the experimental determination of N_D. There exists a simple reason for the discrepancy between Monsanto's value for N_D and the capacitively measured value, and that is an overestimation of the diode area. Since A^2 appears in the denominator of the expression giving N_D, undercutting of the 18 mil diameter photoresist mask by the etchant, to form a 16.6 mil diameter barrier, will cause the noted discrepancy in N_D. Such drastic undercutting is not necessary in light of the presence of pinholes in the Cr annulus, which also decrease the actual area of the barrier. In all probability the

the experimental value of $2.0 \times 10^{16}/cm^3$ is low, but the true value is not as high as the Monsanto estimate of $2.8 \times 10^{16}/cm^3$.

Possible errors in the experimental value for the built-in voltage will now be discussed. Normally the existence, under reverse bias, of slowly emptying traps would raise the "infinite capacitance" intercept of the $\frac{1}{C^2}$ - V plot. The experimental procedure, however, avoids such an error. Because of its capacitance, which appears in series with the capacitance of the space charge layer, the presence of an interfacial layer will erroneously raise the value of the built-in voltage ($V_{int} + kT/q$). What should be done to find the value of applied bias at which the semiconductor space charge layer vanishes is to find the voltage at which $C/A = \varepsilon_o/\delta$, the interfacial capacitance per unit area. Instead, the plot is extrapolated to the infinite capacitance point, giving rise to the last two correction terms[3,8] in Eq. 2. These corrections have been made in the $\Phi_{Bn} + \Delta\Phi_n$ value shown on page 18. An error in the measurement of diode area, however, by affecting N_D, also affects V_F and the interfacial and image force correction terms. For this reason the important parameters of the surface barrier are recalculated using $N_D = 2.8 \times 10^{16}$ impurity atoms/cm^3.

$$V_F = 3.0\ kT/q$$

$$\Phi_{Bn}+\Delta\Phi_n \approx .800 + 4.0\ kT/q - .103$$

$$\Delta\Phi_n = .151(.800 - V)^{1/4} \text{ volts}$$

The effective barrier height at room temperature and zero bias, Φ_{Bn_o}, is found to be .66 volts. Hence there is a .03 volt drop in the effective room temperature barrier height for the higher N_D value.

It is of interest to compare the barrier height, corrected for image force lowering, with the results obtained by Cowley and Sze[3] for just such a model of the metal-semiconductor system as employed here. They derive an expression for the barrier height

$$\Phi_{Bn} = \gamma(\Phi_M - \chi) + (1-\gamma)(E_g - \Phi_o) - \Delta\Phi_n \qquad (6)$$

where $$\gamma = \varepsilon_o / (\varepsilon_o + q\delta D_s) \qquad (7)$$

Reasonable agreement was found between this theoretical expression and experimental results for metals on Si, GaP, GaAs, and CdS. In particular, data by Mead and Spitzer[2] for (110) GaAs give the empirical expression

$$\Phi_{Bn} = .055\ \Phi_M + .599$$

Chromium has a vacuum work function of 4.37 ev. The corresponding Φ_{Bn} is .84 ev, much higher than the .66-.69 ev barrier height obtained here. The present experiment, however, employs $(\bar{1}\bar{1}\bar{1})$ GaAs and so possible differences exist in the electron affinity (χ), the density of surface states (D_S), and the interfacial layer. A previous experiment[1] showed that surface barriers

fabricated on the ($\bar{1}\bar{1}\bar{1}$) face of GaAs are relatively insensitive to the metal work function. It may be argued, then, that the density of surface states on ($\bar{1}\bar{1}\bar{1}$) GaAs is of the same order of magnitude as for (110) GaAs. Let it be assumed that

$$D_S \approx 1.9 \times 10^{14} \text{ states/cm}^2\text{-ev}$$

$$\chi \approx 4.07 \text{ ev}$$

$$\Phi_o \approx 0.48 \text{ ev}$$

$$\delta \approx 10 \text{ Å}$$

The quantities D_S and Φ_o are calculated for the Cowley-Sze model (Eqs. 6 and 7) using the (110) data of Mead and Spitzer. The electron affinity is known for (110) GaAs, but it is unavailable for ($\bar{1}\bar{1}\bar{1}$) GaAs. In other words, the one change between ($\bar{1}\bar{1}\bar{1}$) and (110) GaAs is that the interfacial layer is assumed to be 10 Å thick as opposed to the monolayer (4 Å) which likely existed on the vacuum cleaved samples of Mead and Spitzer. The theoretical expression (Eq. 6) for barrier height becomes

$$\Phi_{Bn} = .029\ \Phi_M + .534$$

for a donor concentration of $2.0 \times 10^{16}/\text{cm}^3$, and

$$\Phi_{Bn} = .029\ \Phi_M + .523 \text{ ,}$$

for a donor concentration of $2.8 \times 10^{16}/\text{cm}^3$. For the Cr contact the theoretical barrier heights become .66 ev

and .65 ev for the respective donor densities. This .65-.66 ev range agrees favorably with the experimental .66-.69 ev range in barrier height, and the agreement is offered as a justification of the assumed thickness (10 Å) and permittivity (8.85×10^{14} f/cm) of the interfacial layer.

3. Current-Voltage Characteristics, 300°K

In Appendix A it is shown that for a completely forward biased structure, the expected enhancement of a component of bulk current over the edge current is given by

$$\frac{I}{I_{o_e}} = 1 + \left(\frac{r_R}{r_O}\right)^2 \left(\frac{s}{s-2}\right) \left[\left(\frac{r_R}{r_D}\right)^{s-2} - 1\right] \qquad (4)$$

where $$s = \frac{q}{kT} \left[\ln (r_R/r_D)\right]^{-1} \frac{V_G'}{n} \qquad (5)$$

The results summarized in Table 3 indicate that the theoretical enhancement of bulk current (assumed to be entirely Schottky current of n = 1.06) is not attainable. A variety of factors cause the discrepancy between I/I_{o_e} and I/I_{o_a}.

Firstly, the values for I/I_{o_a} are obtained for V_R = .10 volts, and here the unguarded characteristic contains a relatively high degree of edge current, thus I_o is higher than if it were merely ideal Schottky current. Pinholes in the resistive annulus have already been mentioned as a probable source of a barrier current

component over which the Schottky current can not be easily enhanced. Thirdly, the potential distribution between the dot and the ring will lose its radial symmetry as the differential bias is increased.(13) The resistance seen by a current flowing within the guard ring, from a given point to the diametrically opposite point, is approximately 0.1 ohm at room temperature. Certainly this resistance becomes appreciable for the high guard currents (on the order of 100 milliamps for V_G = 0.40 volts at room temperature). Since only one lead is stitched to the ring, the guard current will tend to take the shortest path between the dot lead and the ring lead. The resulting asymmetric voltage distribution is one in which that portion of the guard ring opposite the site of the stitched lead is at about the same potential as the dot, and thus the enhancement qualities of the device are not fully realized. Evidence of such a radially asymmetric guard potential distribution is present in the guard circuit resistance measurements made at 77°K. Because each diode is mounted on an adequate header and immersed in liquid N_2, it is reasonable to assume that the power dissipated in the guard circuit does not increase the temperature of the diode. Yet small increases in guard circuit resistance are observed for increases in the guard voltage. These resistance increases must be ascribed to a radially asymmetric current flow.

A fourth cause of decreased enhancement is possible only for the room temperature measurements, and that is an increase in temperature and a subsequent decrease in the enhancement exponent s. Resistive measurements on the guard circuit provide a means of deducing the approximate temperature rise. Increases in resistance observed at room temperature are attributed to both non-uniformity of current flow and thermal power dissipation, while similar increases at liquid N_2 temperature are ascribed to only the former cause. Let the temperature dependence of the guard circuit resistance be written as

$$R_G = R_o \left[1 + \alpha\ (T - 77°K)\right],$$

where R_o is the resistance at 77°K and α is the temperature coefficient of resistivity. Implicit in the above formula are the reasonable assumptions that α is independent of temperature, and that the Au leads, Ag dot and ring, and Cr annulus all have essentially the same α. It is also reasonable to assume that no heating occurs for the modest guard voltage of .13 volts (corresponds to less than 6 milliwatts). Then α is easily calculated as

$$\alpha = \frac{\left.\frac{R_G}{R_o}\right|_{I_G(.13)} - 1}{T - 77°K}$$

The term $\left.\frac{R_G}{R_O}\right|_{I_G(.13)}$ denotes the ratio of the resistance at room temperature (T) to the resistance at 77°K, where both resistances are evaluated at the same level of guard current (I_G). This particular ratio is taken because the degree of asymmetry of the annular potential distribution will be determined solely by the guard current level. The specific guard current chosen is that which is observed for a guard voltage (V_G) of .13 volts when the device is at room temperature. An average temperature coefficient of resistivity of $1.47 \times 10^{-3}/°K$ is found for the devices, the spread being from $1.26 \times 10^{-3}/°K$ to $1.68 \times 10^{-3}/°K$. Once α has been found, the formula below yields the true temperature of the device at the given (nominal) guard voltage V_G

$$T = \frac{\left[\left.\frac{R_G}{R_O}\right|_{I_G(V_G)} - 1\right]}{\alpha} + 77°K$$

Notice that the ratio of resistances is always between resistance values for identical potential distributions. Figure 11 is a typical plot of R_G and R_O, with the amount of heating above room temperature indicated for various guard voltages. Generally, the minimum valid n for a guarded diode at room temperature is observed at or below a nominal guard voltage of .20 volts. Calculations concerning the resistive heating typically show that the

temperature increase is not significant (i.e., $\leq$ 1°K) for such modest guard voltages, and thus the minimum valid n values do not need correcting. There are two exceptions: unit #11 shows a 4°K rise in temperature at its point of minimum n, and unit #14 shows a 9°K rise at its point of minimum n. The corrected values of n are entered in Table 3.

Despite the inability to obtain as great an enhancement of bulk current as is predicted by Equations (4) and (5), it is possible to achieve essentially ideal Schottky barrier behavior. For a Schottky diode in which the thermionic diode theory is applicable and image force barrier lowering is the only complication, the forward characteristic for a bias greater than 3kT/q is of the form

$$I \propto e^{qV/nkT}$$

where $$n = \left[1 - \Delta\Phi_n/4(V_{int}-V)\right]^{-1}$$

That is, n is a function of the applied bias because of the field dependence of the image force lowering term in the expression for the effective barrier height. Consult Appendix B for details. Figure 12 is a plot of the ideal Schottky n as a function of the applied bias, V. Two curves are plotted, corresponding to the two doping concentrations. A complication enters because the guarded structure is in reality a distributed diode. Each small annular portion of the device is at a different forward

bias, and thus the experimentally observed current is in fact a summation of bulk currents of varying n. Ideally, the n of the Schottky current varies continuously as a function of the annular radius, with the minimum value determined by the potential V_D of the dot.

Provided the Schottky current is enhanced sufficiently over the non-Schottky components, the minimum experimental n will fall between the limits set by the theoretical values corresponding to V_D and V_R. It would be absurd to actually compute the summation of bulk currents for the purpose of finding the theoretical effective n of the total Schottky current, since the experimental value of n is little more accurate than the full range of theoretical n values between V_D and V_R. The range of theoretical n of special interest is replotted in Figure 13, and superimposed on the theoretical curve are horizontal lines which indicate the minimum experimental n obtained for each diode. The data must be represented as a line of length $V_{D_{max}}-(V_{D_{min}}-V_G')$ because it is this range of voltages which exist on the diode for the portion of the experimental I-V plot (Fig. 7) from which n is taken. Table 3 lists the V_G' and the range of V_D for each minimum experimental n. It is seen that only unit #1 disagrees significantly with the theoretical n value, and this discrepancy is likely due to a greater than usual

number of pinhole imperfections in this particular Cr annulus. The group of diodes as a whole may be characterized as possessing an n of 1.06, a value which is in agreement with Schottky diode theory.

Nothing can be added to what has already been stated about the results of the various other room temperature forward I-V characteristics of the diodes. The controlled introduction of ambients, the waxing of the diodes, and the etching of the annulus all serve to emphasize the sensitivity of the non-Schottky components to the condition of the semiconductor surface, and they also serve to highlight the gradual deterioration of the guard ring structure with time.

The reverse current at room temperature, even for moderate applied bias ($\leq$ 5 volts), can not be attributed to volume space charge generation ($m = \frac{1}{2}$), because the experimental m is at least two. Kahng[12] and Kuper[14] have reported edge space charge generation with m=1 rather than $m = \frac{1}{2}$. Yet even this current has too slow a voltage dependence to explain the reverse characteristic observed at room temperature. It is probable that both the upper range of this reverse characteristic and the entire range of the 77°K reverse characteristic are experiencing a high degree of avalanche multiplication.

The likely explanation for the lower portion of the 300°K

characteristic is also avalanche multiplication, although of a lesser degree, and occurring as microplasmas. A microplasma is a localized avalanching produced by a high local field at the site of a crystal defect. Because of avalanching, the edge currents are not dominant in the range of reverse bias used. This means that the activation energy plot to find the generation-recombination centers is useless. In fact, the activation energy plot had been regarded with great suspicion because of the extremely shallow trap level which the analysis suggested. As will be discussed soon, such a shallow trap level is not consistent with the $n \approx 2$ observed for the guarded forward characteristics at 77°K.

4. Current-Voltage Characteristics, 77°K

At first glance, one might expect that lowering the diode temperature to 77°K would greatly increase the enhancement capability of the guard ring structure, for a fixed differential bias, because of the inverse dependence of s on T (Eq. 5). Such is not the case, however, because n values in the neighborhood of two, rather than one, are seen for the diodes immersed in liquid nitrogen. It is likely that the same factors which caused the observed enhancement values to be below the expected enhancement values at room temperature are also operating for the cooled diode. A rise in temperature due to resistive

heating is not likely for this case, but the other factors, such as pinholes and asymmetric voltage distribution, should be no more nor less degrading than at room temperature. That is, imperfections in the structure of the device can not be blamed for the absence of Schottky current at 77°K. In fact at 77°K the guarding mechanism will still be operative, the differential bias will still enhance the barrier current over the edge current, and, within the barrier current, the component of lowest n will be most enhanced. If n's of two are observed at 77°K, then the Schottky current ($n \approx 1.06$) must be so small as to be essentially out of reach of the enhancement mechanism. The resulting predominance of recombination current is caused by the great temperature sensitivity of the Schottky current.

Let the recombination current be described as

$$J_t \propto T^{3/2} e^{-E_a/kT} e^{qV/2kT} \tag{8}$$

The appropriateness of this expression will be discussed later. It is known that the Schottky current is of the approximate form

$$J \propto T^2 e^{-q\Phi_{Bn_o}/kT} e^{qV/kT}$$

The ratio of the two components is

$$\frac{J_t}{J} \propto \frac{1}{T^{1/2}} \frac{e^{(q\Phi_{Bn_o} - E_a)/kT}}{e^{qV/2kT}} \qquad (9)$$

For purposes of making an order of magnitude calculation, the activation energy is taken as .35 ev (implying deep traps), and the barrier height is approximated as .69 volts. A drop in temperature from 300°K to 77°K results in increases in the ratio J_t/J of 10^{10}, 50, and 10^{-10} for respective forward biases of 0, .5, and 1 volts. The temperature sensitivity of the ratio (Eq. 9) is changed drastically by a variation in activation energy. Identical calculations for a shallower (but still fairly deep) trap of .20 ev activation energy yield corresponding values for J_t/J of 10^{23}, 10^{7}, and 10^{-2} for 0, .5, and 1 volt biases respectively.

Now at room temperature and .5 volts forward bias, the unguarded current characteristic probably contains an edge component about two orders of magnitude smaller than the Schottky current, because the observed n's are closer to unity than to two. When in the guarded mode, the theoretical enhancement, even at low guard voltage, is able to swamp out the edge component. For the same .5 volt forward bias at 77°K, however, the unguarded

characteristic contains an edge component ($E_a \approx .20$ ev), say, five orders of magnitude larger than the Schottky component. Table 4 indicates that the lower limit of the bias range in which the n's of two are observed is greater than .5 volts, thus the ratio of n=2 current to n=1 current is even less than 10^5. In addition, the expected enhancement values for the n=1 current, for the guard voltages at which the n=2 current is seen, are 10^{12} to 10^{44}, certainly enough to emphasize Schottky current over edge current, even at 77°K.

In Figure 8, it is evident that the estimate of V_G' is too low, because each curve should lie above those of lesser guard voltage. Portions of curves (2) and (3), however, are below curve (1). A higher V_G' estimate would shift them further to the left, placing them above curve (1), the characteristic for zero guard voltage. This error made in reducing V_G to account for lead IR drop is of little consequence, what matter are the values of n which are observed. Recalculation of the expected enhancement of Schottky current over edge current would yield even higher values of I/I_{o_e}, and yet the edge current persists in the experimental evaluation of the diodes.

Notice that most of the diodes, when unguarded, possess an n of at least three, often it is greater than four. Suppose that this component of current arises due to channels, or some other leakage phenomenon which occurs

on the surface of the GaAs, from the perimeter of the ring outward. Exactly why the unguarded n is so high is not known, but the mechanism must be extremely sensitive to surface conditions, since there is much variation in n between the various diodes. Because this edge current possesses such a high n, it is readily swamped out by the guarding mechanism; swamped out, in fact, by an n≈2 current rather than Schottky current. It has been shown that the guard ring structure at 77°K is capable of swamping out even n≈2 currents should they arise at the edge of the ring and beyond. Hence the n≈2 current must be flowing in the central portion of the surface barrier, where the guard ring structure is not able to differentiate so easily between currents of various n values. That is, the guard ring will enhance both the Schottky current and this other barrier current over the edge current, and although the relative enhancement of the Schottky current is greater (s is approximately twice as great), the low temperature allows the other (central) current to predominate.[15] Entries in Table 4 show that the theoretical guard ring enhancement of n=1 Schottky current relative to n=2 barrier current is of the order of 10^{16} to 10^{18}. This is well below the 10^{23} zero bias thermal enhancement of the hypothesized n=2 central current ($E_a \cong .20$ ev). Granted, the thermal enhancement at .5 volts bias is only 10^7, but previously discussed imperfections in the guarding mechanism will decrease the actual guard ring enhancement from 10^{16} to below 10^7, thus making the thermal mechanism predominant.

Given that a current component of n≈2 exists, it has been established that it can only be observed if it is a bulk phenomenon. More can be said about the origin of this barrier current. Drift-field hole current, arising from the injection of minority carriers, is one possibility. For moderate to heavy forward bias, the injection ratio is given by (16)

$$J = \frac{n_i^2 J}{b N_D^2 J_s},$$

where n_i is the intrinsic concentration, b is the mobility ratio, J_s is the Schottky diode saturation current density, and J is the diode forward current density. Taking

$$n_i = 4 \times 10^6/cm^3 \text{ (at } 300°K)$$
$$b = 5.7$$
$$N_D = 2 \times 10^{16}/cm^3$$
$$J/J_s = 10^7$$

yields an injection ratio of 7×10^{-14}. The extremely low intrinsic concentration for GaAs is what makes injection unreasonable, and of course n_i decreases with decreasing temperature, so the injection ratio at 77°K will be even less than 10^{-14}.

It is proposed that a current of the form described in Eq. (8) is produced by electrons falling into deep traps in the space charge layer. The electrons subsequently

enter the metal by tunnelling. Such a model has been proposed, and substantiated experimentally, by Dumin[17]. Deep traps are required, because current due to shallow traps would exhibit an n≈1 rather than an n≈2. The assumed activation energy of .20 ev, which gives sufficient thermal enhancement of J_t over J (Eq. 9), corresponds to a trap located .50 ev above the intrinsic Fermi level. A schematic representation of the electron path is presented in Figure 14.

Despite the many precautions taken during fabrication of the diode, a wide variation in surface conditions exists. This difference in surface properties among the diodes is most evident in the unguarded n of 1.74 for diode #4 at 77°K. For this one unit, no channels (or whatever the cause of edge current possessing high n) develop, yet for all other diodes, edge components in a range of high unguarded n values (2.46 to 4.59) are present. A large spread in the guarded n (1.54 to 2.27) also exists. Evidently the trapping level in the space charge layer is influenced by the variation in semiconductor surface conditions between the various diodes. Certainly the bulk properties of the GaAs could not vary drastically enough to produce the observed spread in the guarded n values.

VI. CONCLUSIONS

Despite imperfections in the guard ring structure, the enhancement mechanism at 300°K is sufficient to yield ideal Schottky forward characteristics with n typically equal to 1.06. This value for the guarded n is consistent with a lowering of the barrier caused by the image force. At room temperature, then, it is the edge component of current which causes the non-ideal behavior of the unguarded diode.

Schottky current is extremely sensitive to temperature, and at 77°K it is so small, relative to the recombination currents, that the guard ring is unable to make the Schottky current predominant. Two current components are visible in the unguarded forward characteristic of the cooled diode: an edge current with an anomolously high n (2.46 to 4.59), and a bulk recombination current with an n of about two (1.54 to 2.27). The guarded, cooled diode exhibits only the bulk component. This current is hypothesized as resulting from a capturing of electrons by fairly deep traps located within the space charge layer. From these traps, which are situated near the metal-semiconductor interface, the electrons tunnel to the metal. The appreciable spread in guarded n values (1.54 to 2.27) indicates that the traps are at

different levels in different diodes. This difference is ascribed to variations, between diodes, in the condition of the semiconductor surface below the metal contact.

At both 300°K and 77°K, the reverse current is dominated, even at low bias, by localized avalanche multiplication occurring as microplasmas. Hence the study of the reverse characteristics yields no useful information on the nature of the hypothesized deep traps.

Capacitance measurements show the Cr to n-type $(\bar{1}\bar{1}\bar{1})$ GaAs diode to have a donor concentration of $2.0 \times 10^{16}/cm^3$ and an effective zero bias barrier height of 0.69 volts. These results are consistent with the Cowley and Sze model for a metal-semiconductor system having an interfacial layer which is 10 Å thick and transparent to electrons. An upward drift in capacitance for a given reverse bias is ascribed to slowly emptying traps distributed below the conduction band.

Because of the limitation to high resistivity metals, the particular method employed to guard the surface barrier from edge currents is not amenable to a general study of a wide variety of metal-semiconductor systems. Indeed, the guard ring structure is even awkward for the investigation of Cr to n-type GaAs diodes. Significant degradation of the guarding mechanism results from both the radial asymmetry of the distribution of guard potential (caused by non-zero ring resistance), and the porosity of the resistive annulus.

APPENDICES

A. Expected Enhancement of Barrier Current (after Iwersen, et al[5])

Consult Figure 2 for a representation of the voltage distribution of the diode. This distribution will be radially symmetric provided the sheet resistance of the thin film is uniform and the current flow from dot to ring is radially symmetric. The mathematical expression of such a distribution is

$$V(r) = V_D - V_G' \qquad r_R \leq r \leq r_O$$

$$V(r) = V_D - V_G' + V_G' \left[\ln(r_R/r_D)\right]^{-1} \ln(r_R/r) \qquad r_D \leq r \leq r_R$$

$$V(r) = V_D \qquad 0 \leq r \leq r_D$$

Suppose that, initially, the diode is at a uniform potential $V_D - V_G'$ with current density J_o, where J_o refers separately to the Schottky current or the recombination (bulk, not edge) current, depending on the value assigned to n. The corresponding total diode current for a given n is

$$I_o = \pi r_O^2 J_o.$$

Now suppose a voltage V_G' is applied between the dot and the guard ring, the dot being positive with respect to the guard ring, but the latter remaining at an unchanged bias $V_D - V_G'$ relative to the back. Such an increase in the

forward bias of the dot will enhance the ideal Schottky and bulk recombination components of current, while the edge current will remain unchanged. (In actuality, the experimental procedure was to hold the dot at constant forward bias and depress the ring bias. There is no significant difference.)

Let

$$\Delta V(r) = V(r) - (V_D - V_G')$$

Then the corresponding current densities are

$$J(r) = J_o \qquad r_R \leq r \leq r_0$$

$$J(r) = J_o \exp\left[\frac{q}{nkT}\Delta V(r)\right] = J_o \left(\frac{r_R}{r}\right)^s \qquad r_D \leq r \leq r_R$$

$$J(r) = J_o(r_R/r_D)^s \qquad 0 \leq r \leq r_D$$

where

$$s = \frac{q}{kT}\left[\ln(r_R/r_D)\right]^{-1}\frac{V_G'}{n}$$

The total current is

$$I = \pi J_o\left[(r_o^2 - r_R^2) + r_D^2\left(\frac{r_R}{r_D}\right)^s + 2\int_{r_D}^{r_R} r\left(\frac{r_R}{r}\right)^s dr\right]$$

so that the expected emphasis of barrier current over edge current is

$$\frac{I}{I_{o_e}} = 1 + \left(\frac{r_R}{r_o}\right)^2\left(\frac{s}{s-2}\right)\left[\left(\frac{r_R}{r_D}\right)^{s-2} - 1\right].$$

This function is plotted in Figure 6.

B. Effect of Image Force on Barrier Height

A Schottky barrier for which thermionic diode theory is applicable and image force lowering is the only complication has a forward characteristic describable by

$$J \approx A^*T^2 e^{-q\Phi_{Bn}/kT}\, e^{qV/kT},\quad V > 3kT/q.$$

The amount by which the image force lowers the barrier is a function of the field at the metal-semiconductor interface. Of course, the field can be related to the total voltage across the space charge layer. A complete treatment yields the following expression for the barrier lowering[10]

$$\Delta\Phi_n = \left[B(V_{int}-V)\right]^{1/4},$$

where

$$B = \frac{q^3 N_D}{8\pi\varepsilon_0{}^3\varepsilon_d{}^2\varepsilon_s}$$

Now

$$\Phi_{Bn} = (\Phi_{Bn}+\Delta\Phi_n) - \Delta\Phi_n,$$

and from Eq. (2) it is seen that the quantity $(\Phi_{Bn}+\Delta\Phi_n)$ is not a function of the bias voltage. The theoretical Schottky current may be written as

$$J \approx \left\{A^*T^2 e^{-q(\Phi_{Bn}+\Delta\Phi_n)/kT}\right\} e^{q(V-\Delta\Phi_n)/kT}$$

The term enclosed by $\{\ \}$ does not change with applied bias, hence

$$J \propto e^{q(V-\Delta\Phi_n)/kT} .$$

Let

$$J \propto e^{qV/nkT},$$

where

$$n \equiv \frac{q}{kT}\left[dV/d(\ln J)\right]$$

Thus

$$\ln J \propto \frac{q}{kT}\,(V-\Delta\Phi_n)$$

$$\propto \frac{q}{kT}\left[B(V_{int}-V)\right]^{1/4}$$

$$\frac{d(\ln J)}{dV} = \frac{q}{kT}\left[1 - \frac{B^{1/4}}{4(V_{int}-V)^{3/4}}\right]$$

$$= \frac{q}{kT}\left[1 - \frac{\Delta\Phi_n}{4(V_{int}-V)}\right]$$

Hence

$$n = \left[1 - \frac{\Delta\Phi_n}{4(V_{int}-V)}\right]^{-1} = \left[1 - \frac{B^{1/4}}{4(V_{int}-V)^{3/4}}\right]^{-1}$$

Thus a higher bias produces a higher n, because as the bias increases, the effective barrier height also increases. Figure 12 displays the theoretical Schottky n as a function of applied bias for an intercept voltage (V_{int}) of 0.80 volts and donor concentrations (N_D) of $2.0 \times 10^{16}/cm^3$ and $2.8 \times 10^{16}/cm^3$.

C. List of Symbols

A = area of surface barrier, cm^2

A^* = effective Richardson constant, $amp/°K\text{-}cm^2$

C = capacitance of barrier, f

D_s = density of surface states, $1/cm^2\text{-}ev$

E_a = activation energy of traps, ev

E_g = forbidden energy gap, ev

E_i = intrinsic Fermi level, ev

E_t = trap level, ev

I = diode forward current, amp

γ = injection ratio

I_G = guard current, amp

I_o = current for (hypothetical) diode uniformly biased at $V_R = V_D - V_G'$, amp

I_{rev} = diode reverse current, amp

I/I_{o_a} = actual enhancement of barrier current over edge current

I/I_{o_e} = expected enhancement of barrier current over edge current

J = diode current density, amp/cm^2

J_o = current density for diode uniformly biased at $V_D\text{-}V_G'$, amp/cm^2

J_s = saturation current density, amp/cm^2.

J_t = density of barrier current due to traps, amp/cm^2

m = avalanche multiplication parameter

n = $\frac{q}{kT}\left[\frac{dV}{d(\ln J)}\right]$, see Appendix B

N_D = donor impurity density, cm^{-3}

N_t = trap density, cm^{-3}

q = charge of electron (positive quantity), 1.6×10^{-19} coul

Q_M = surface charge density on metal, $coul/cm^2$

Q_{sc} = space charge density in semiconductor, $coul/cm^2$

Q_{ss} = surface state charge density on semiconductor, $coul/cm^2$

r_D = radius of dot, mil

r_O = outside radius of ring, mil

r_R = inside radius of ring, mil

R_a = annulus resistance, ohm

R_G = guard circuit resistance (annulus and leads), ohm

R_o = guard circuit resistance at 77°K

s = $\frac{q}{kT}\left[\ln (r_R/r_D)\right]^{-1} \frac{V_G'}{n}$

V_B = built-in voltage or diffusion potential, volt

V_D = dot bias with respect to back contact, volt

V_{D+A} = dot bias uncorrected for ammeter IR drop, volt

V_F = potential separation of Fermi level and conduction band, volt

V_G = nominal guard voltage, negative with respect to dot, volt

V_G' = guard voltage corrected for resistive drop, volt

V_{int} = infinite-capacitance voltage intercept of $\frac{1}{C^2}$ - V plot, volt

V_l = voltage drop across interfacial layer, volt

V_R = V_D-V_G' = guard ring bias with respect to back contact, volt

V_{rev} = reverse bias applied to dot and ring, volt

α = temperature coefficient of resistivity, 1/°K

β = fraction of traps which are empty

γ = $\varepsilon_o/(\varepsilon_o+q\delta D_s)$

δ = thickness of interfacial layer, Å

ε_d = image force dielectric constant of semiconductor, f/cm

ε_l = dielectric constant of interfacial layer, f/cm

ε_o = permittivity of free space, 8.85×10^{-14} f/cm

ε_s = static dielectric constant of semiconductor, f/cm

ρ_s = surface resistivity, ohm/square

Φ_M = vacuum work function of metal, volt

Φ_o = energy difference between Fermi level and valence band edge at surface before the metal-semiconductor contact is formed, volt

Φ_{Bn} = effective barrier height, volt

Φ_{Bn_o} = effective barrier height at zero bias, volt

$\Delta\Phi_n$ = image force barrier lowering, see Appendix B, volt

χ = electron affinity of semiconductor, volt

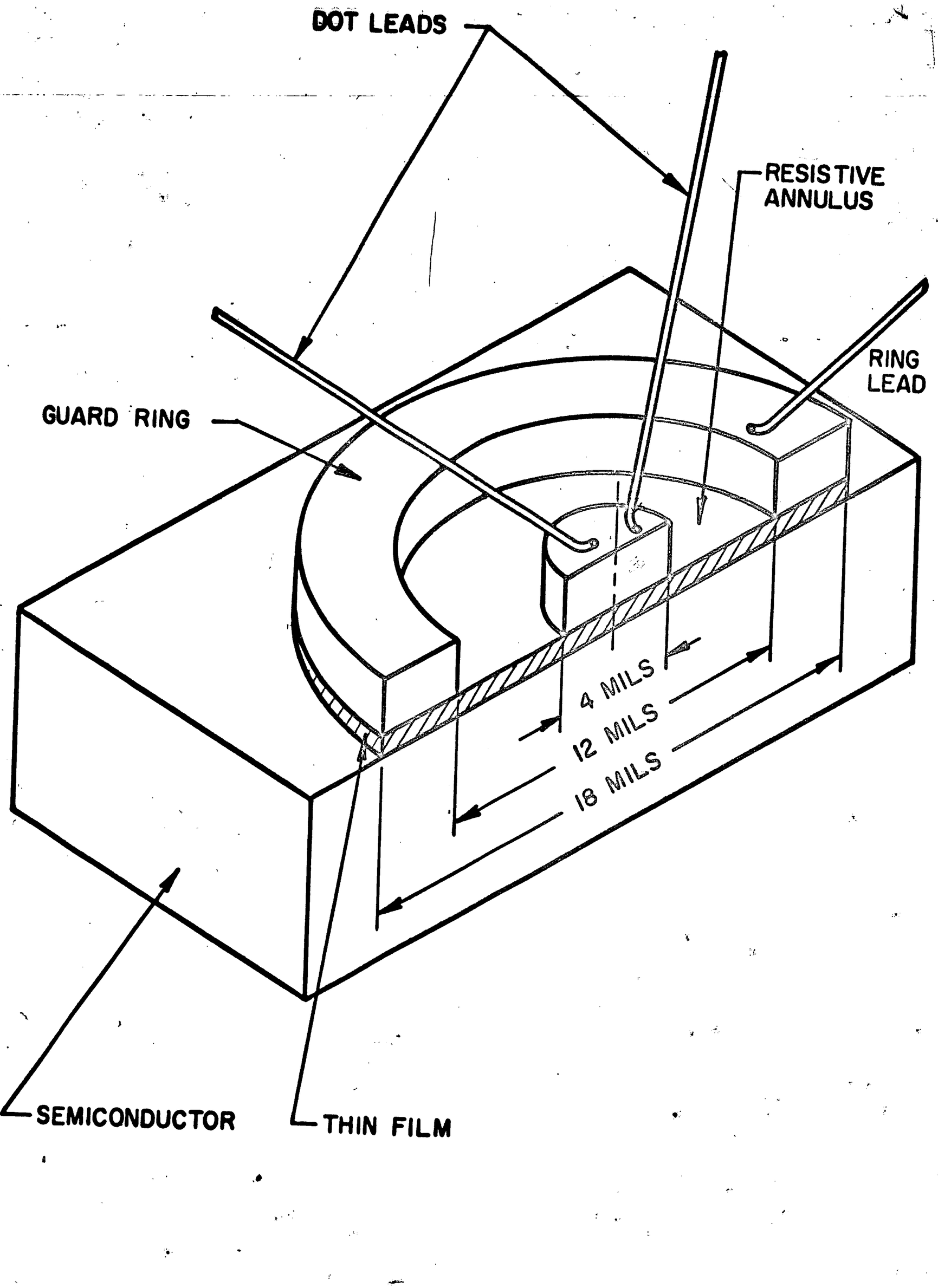

FIG. 1 SURFACE BARRIER WITH GUARD RING

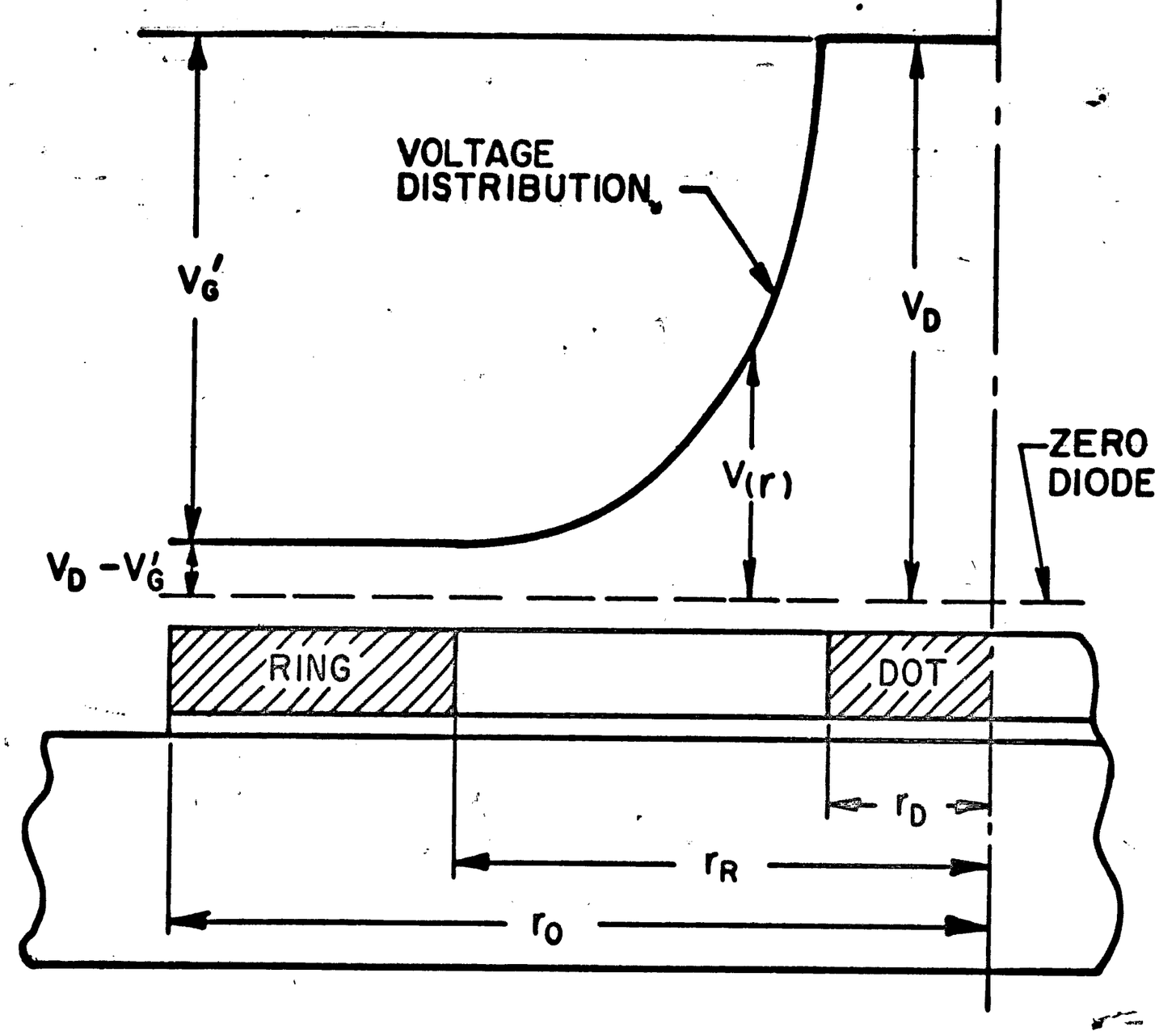

FIG. 2 GUARD VOLTAGE DISTRIBUTION

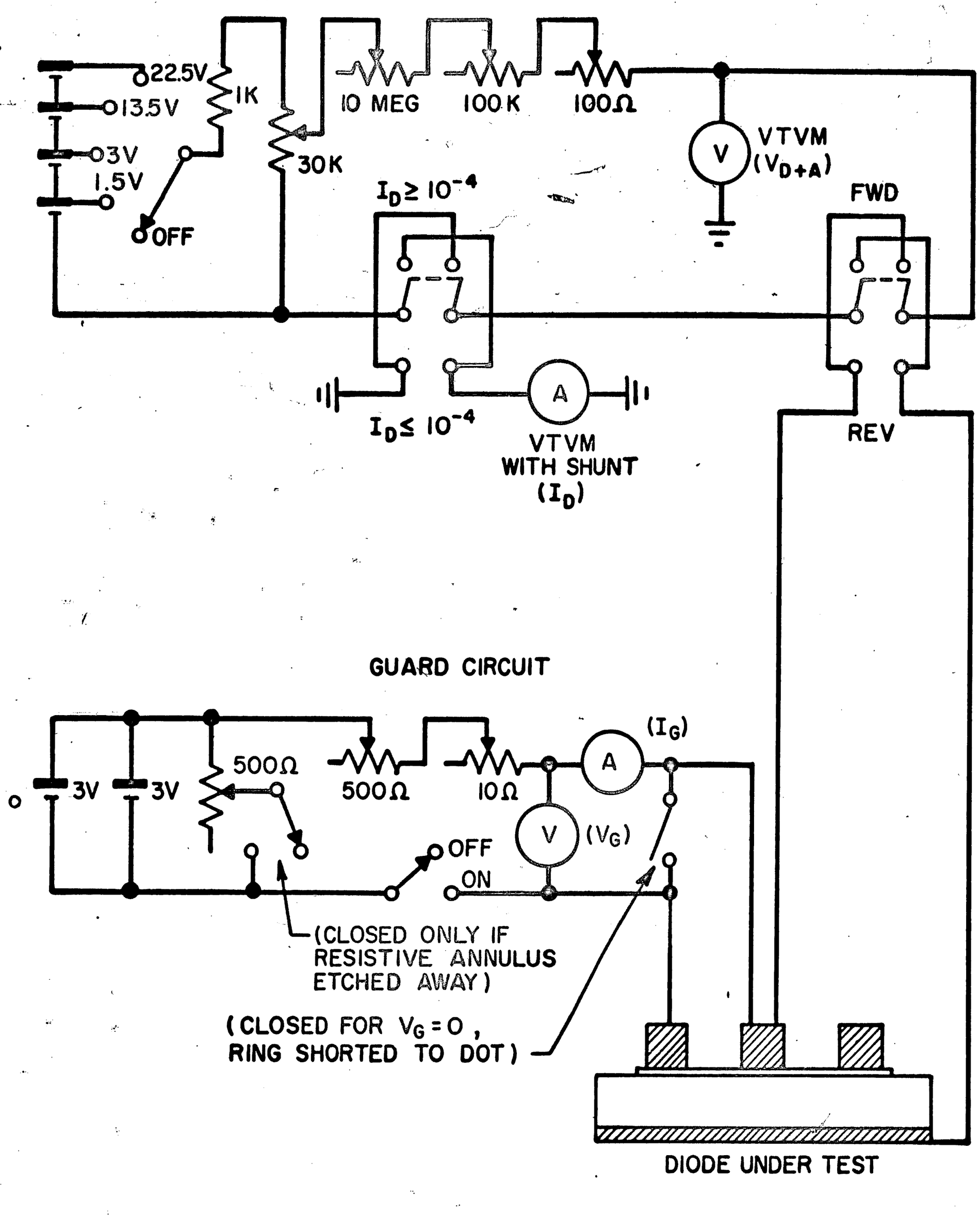

FIG. 3 CIRCUIT FOR CURRENT-VOLTAGE MEASUREMENT

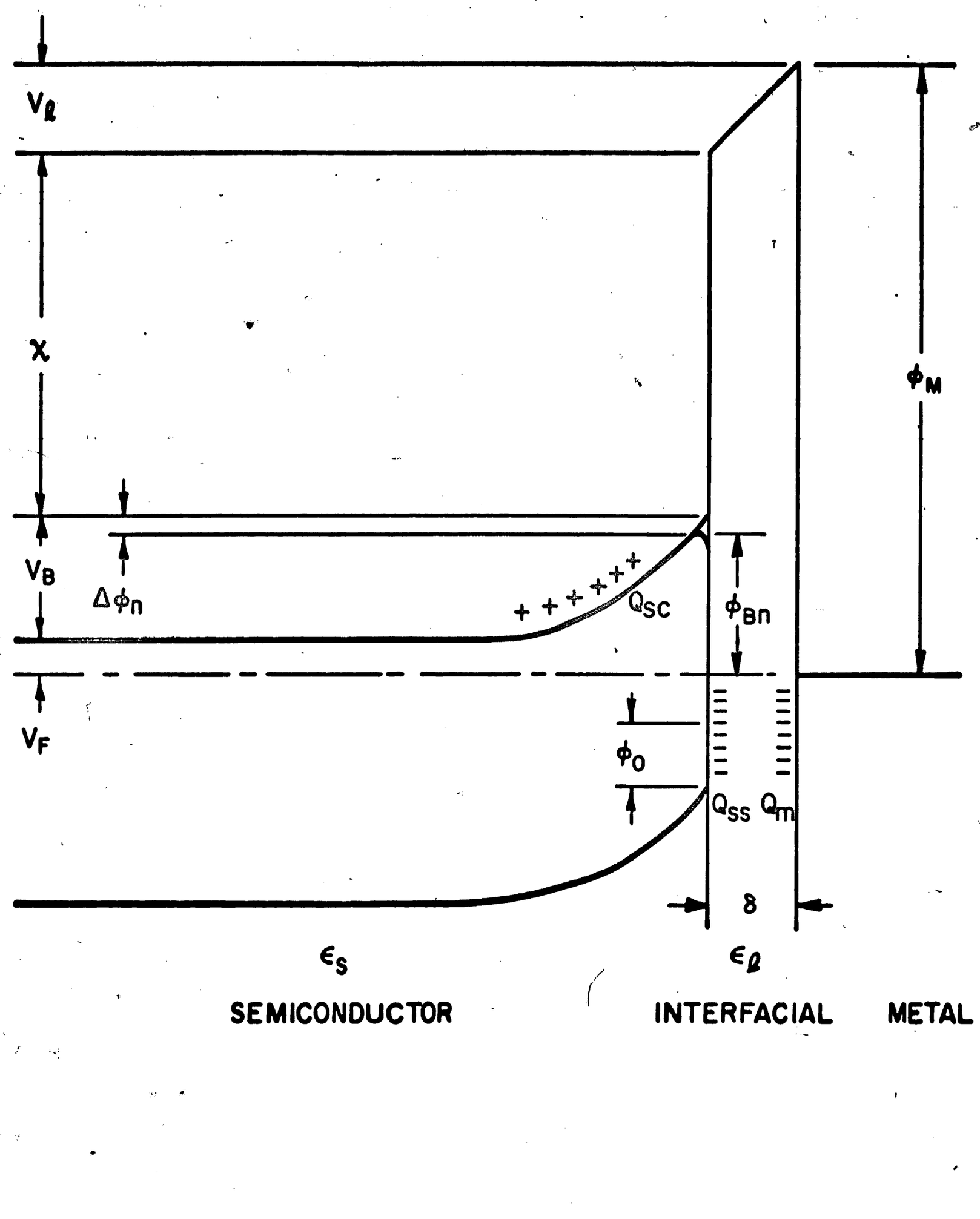

FIG. 4 ENERGY BAND DIAGRAM FOR A SURFACE BARRIER WITH AN INTERFACIAL LAYER (AFTER COWLEY & SZE[3])

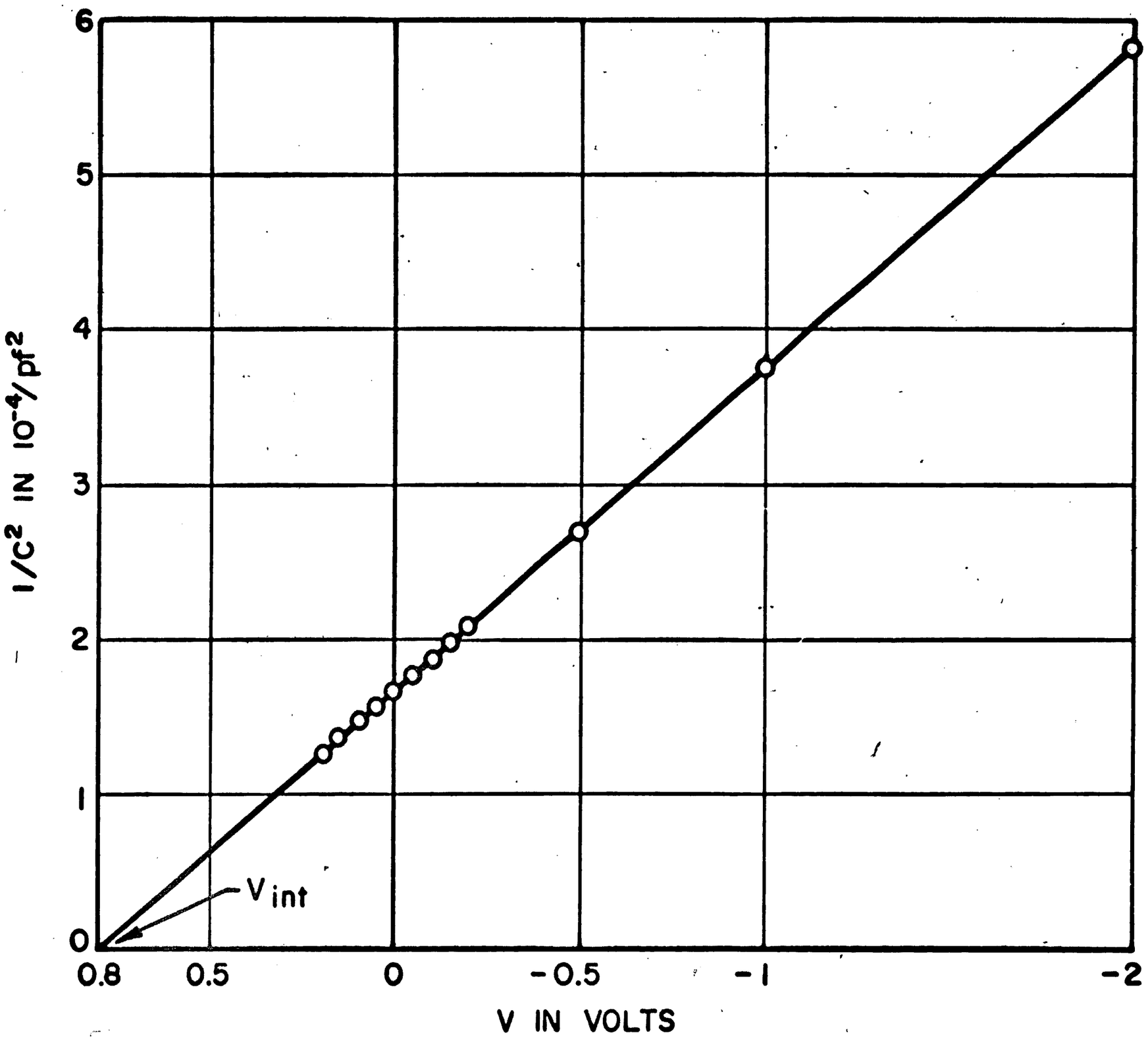

FIG. 5 TYPICAL SQUARED ELASTANCE -VOLTAGE PLOT

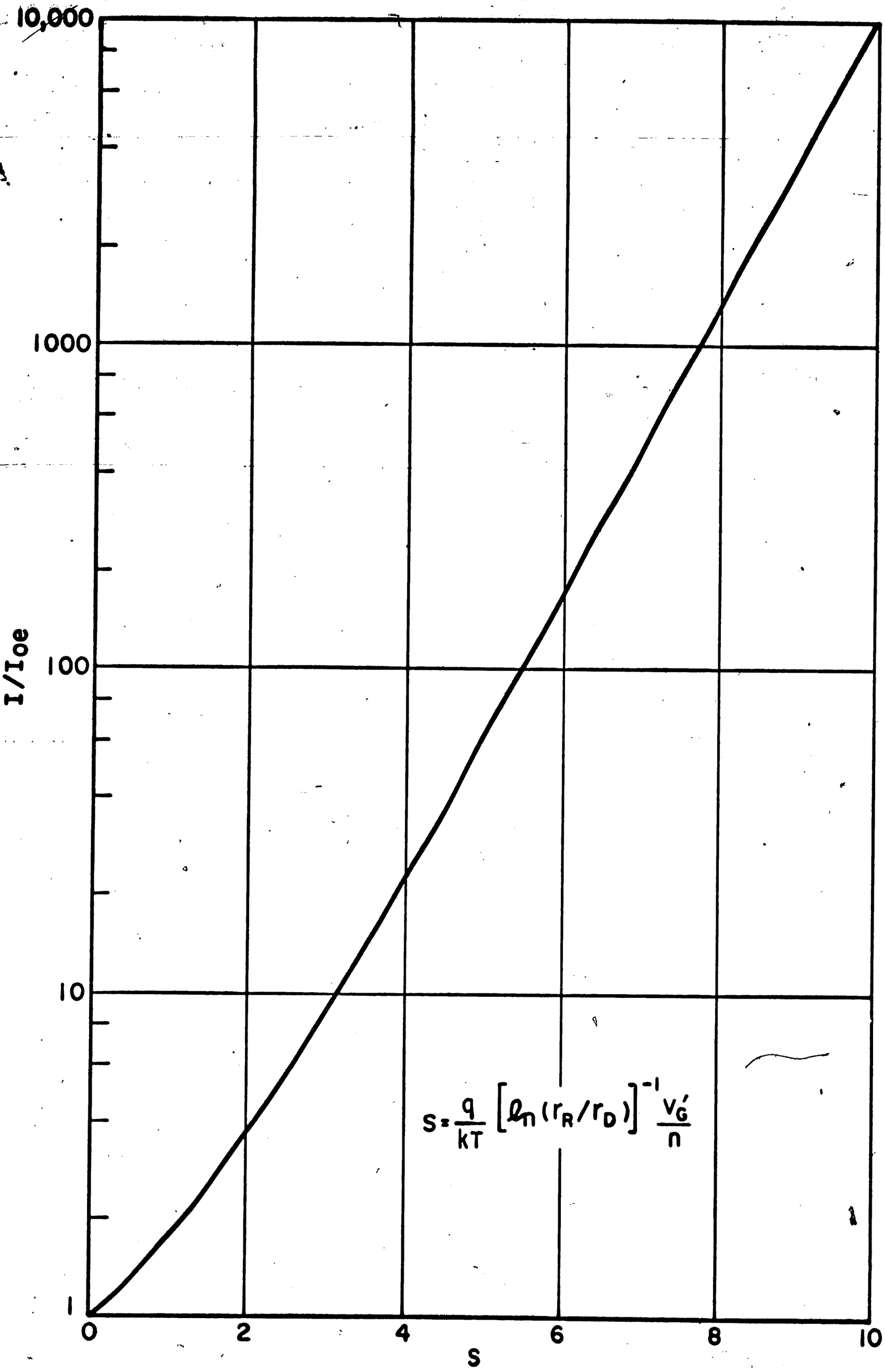

FIG. 6 EXPECTED ENHANCEMENT OF BARRIER CURRENT

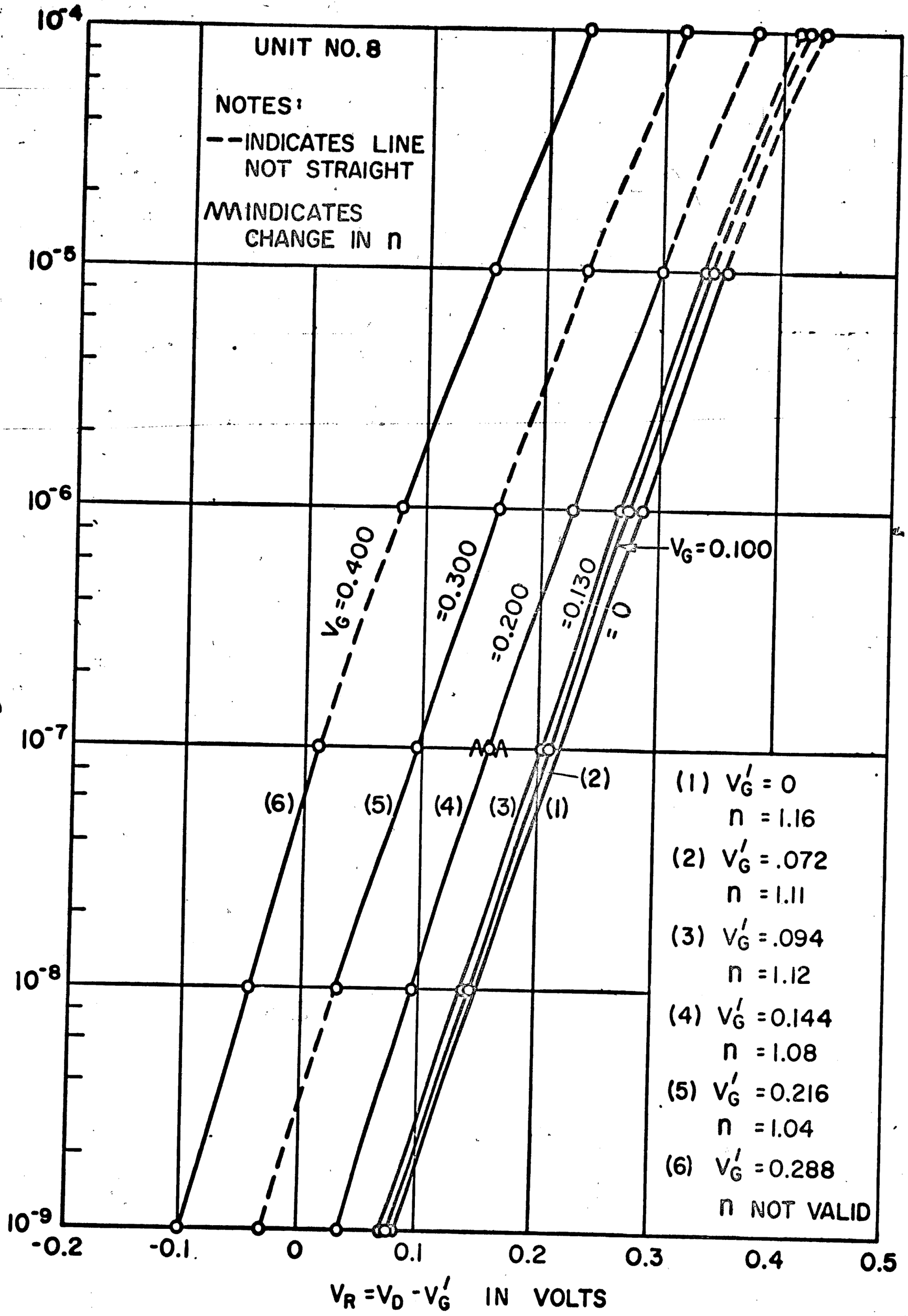

FIG. 7 TYPICAL CURRENT-VOLTAGE CHARACTERISTIC AT 300°K

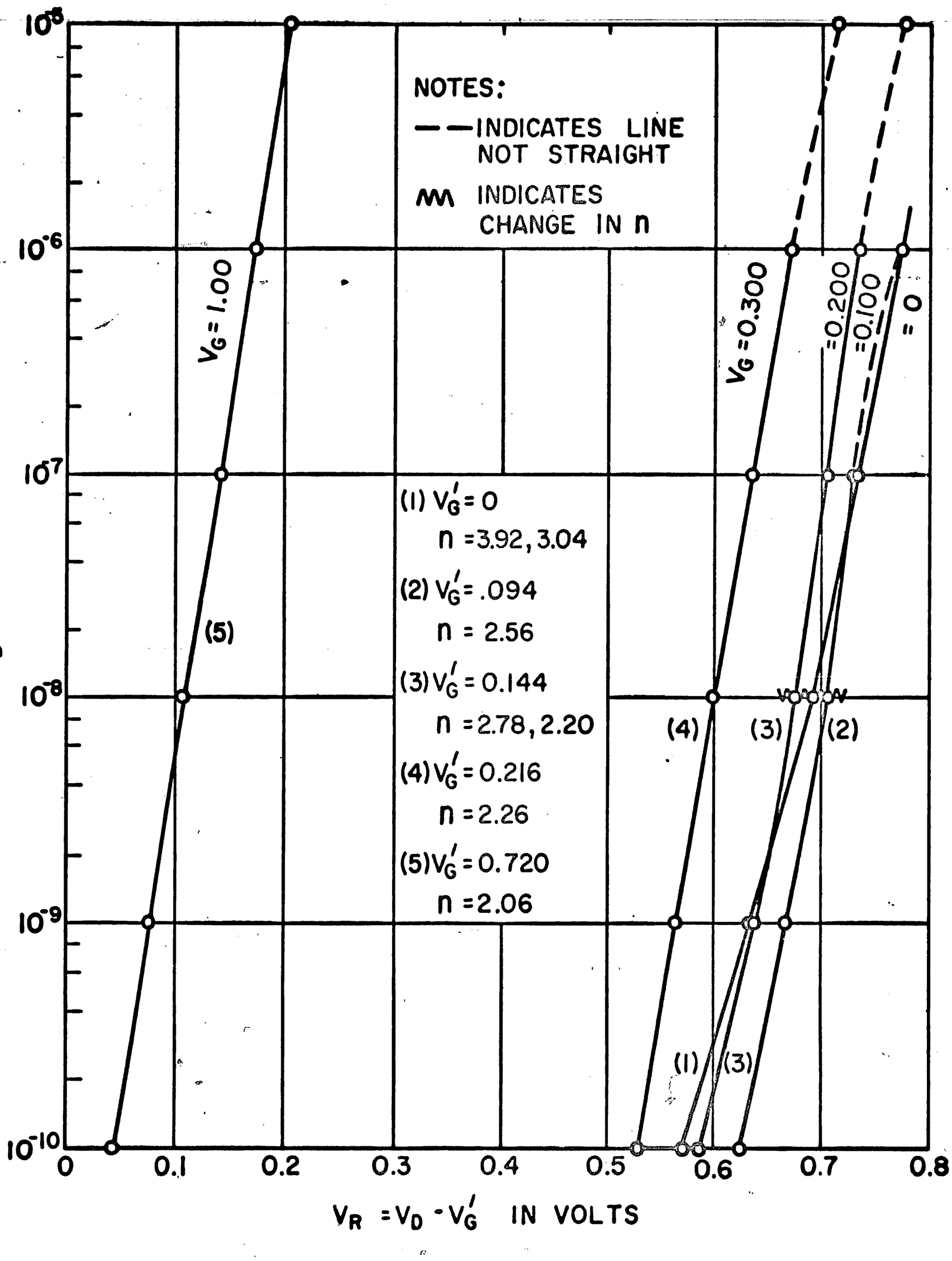

FIG. 8 TYPICAL CURRENT-VOLTAGE CHARACTERISTIC AT 77°K

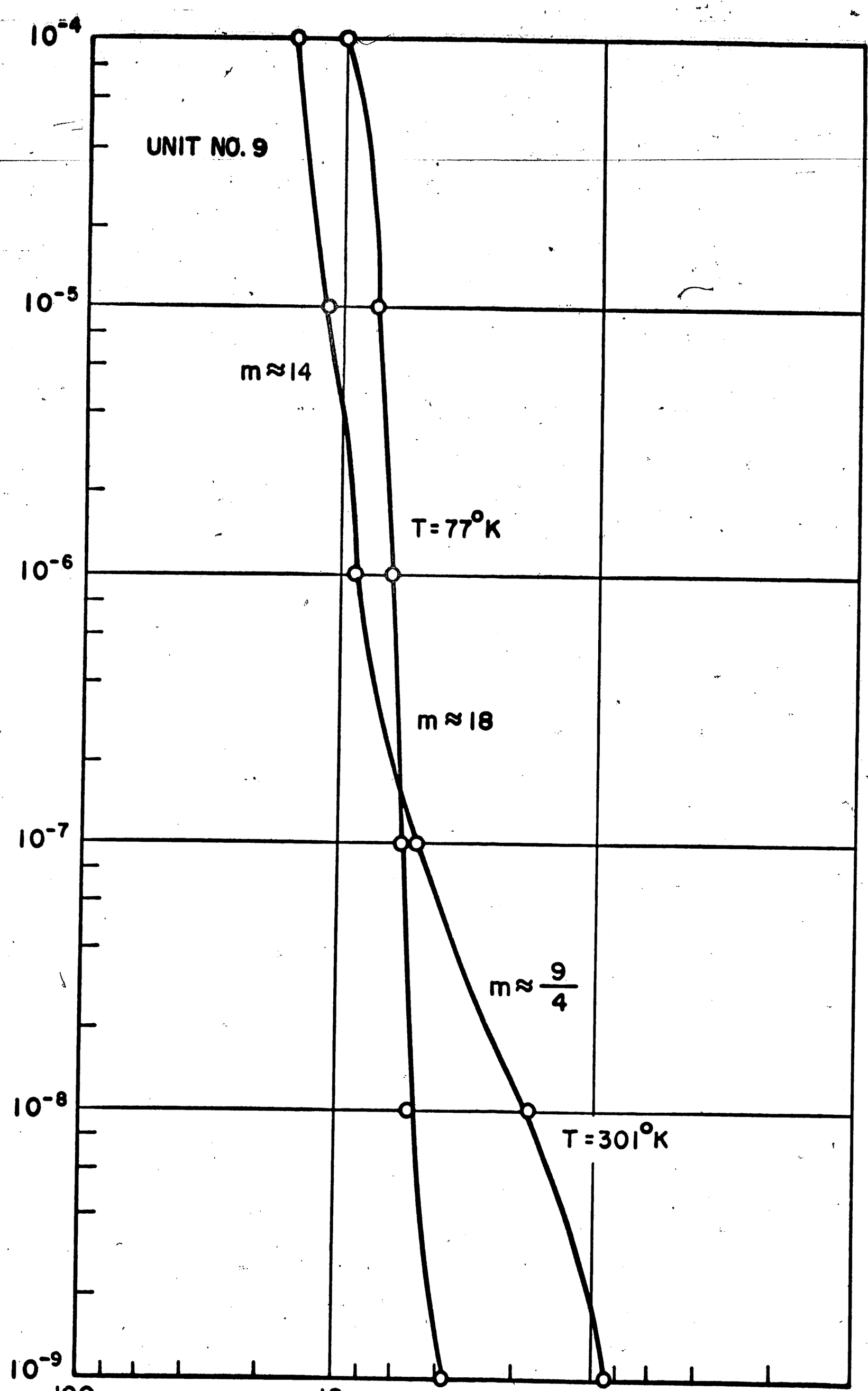

FIG. 9 TYPICAL REVERSE CHARACTERISTIC AT 300°K & 77°K

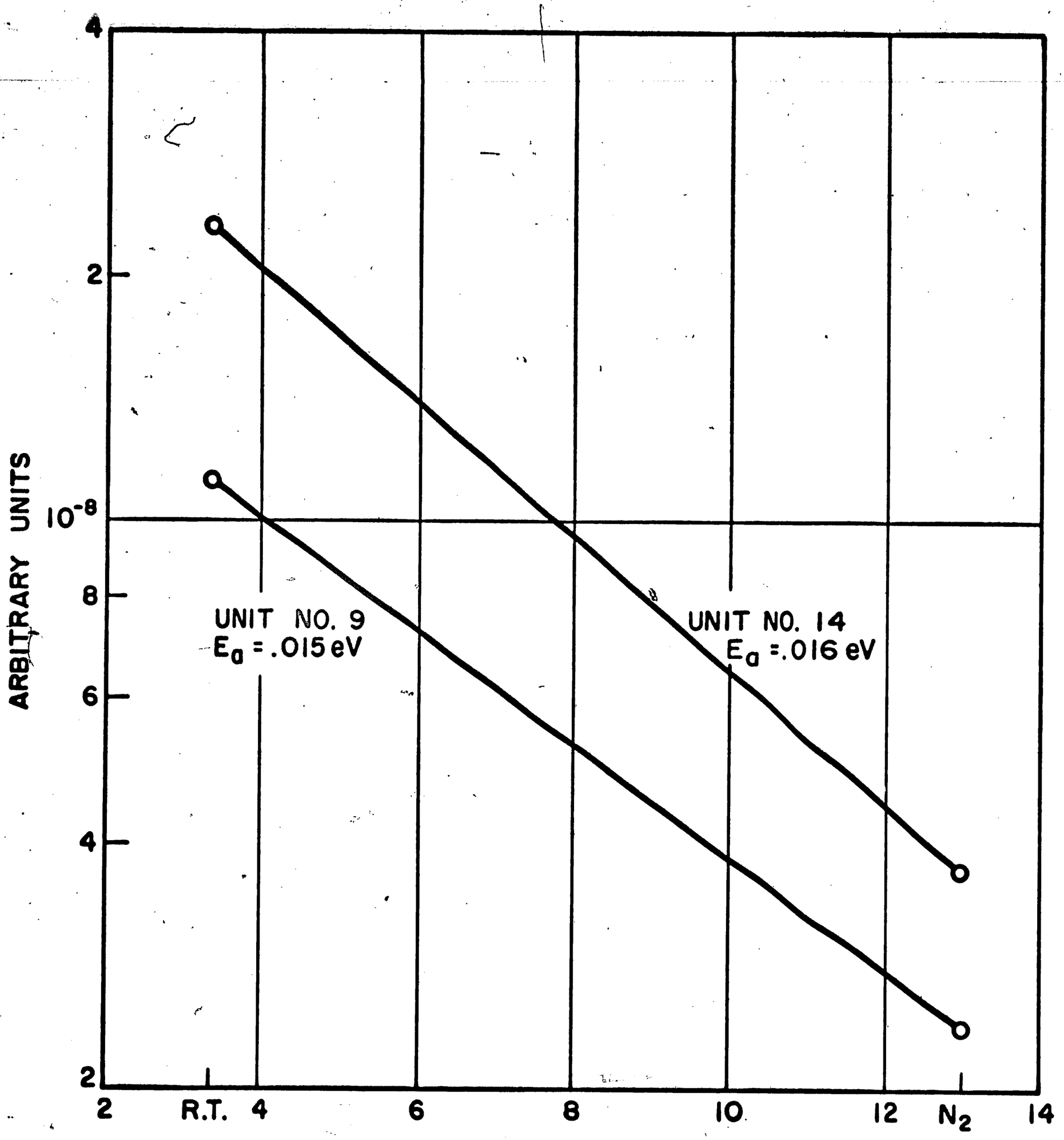

FIG. 10 ACTIVATION ENERGY PLOT

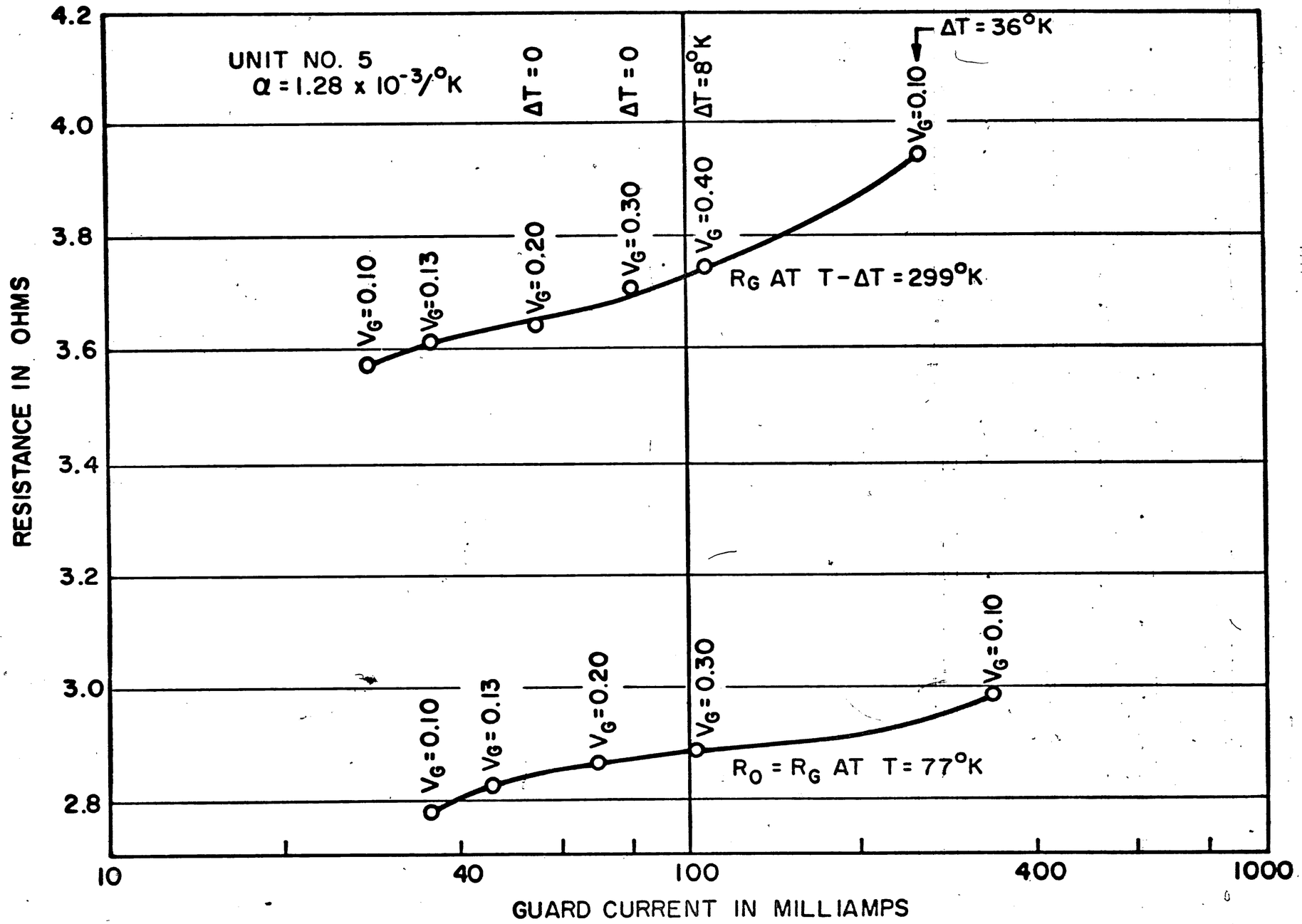

FIG. 11 TYPICAL VARIATION OF GUARD CIRCUIT RESISTANCE

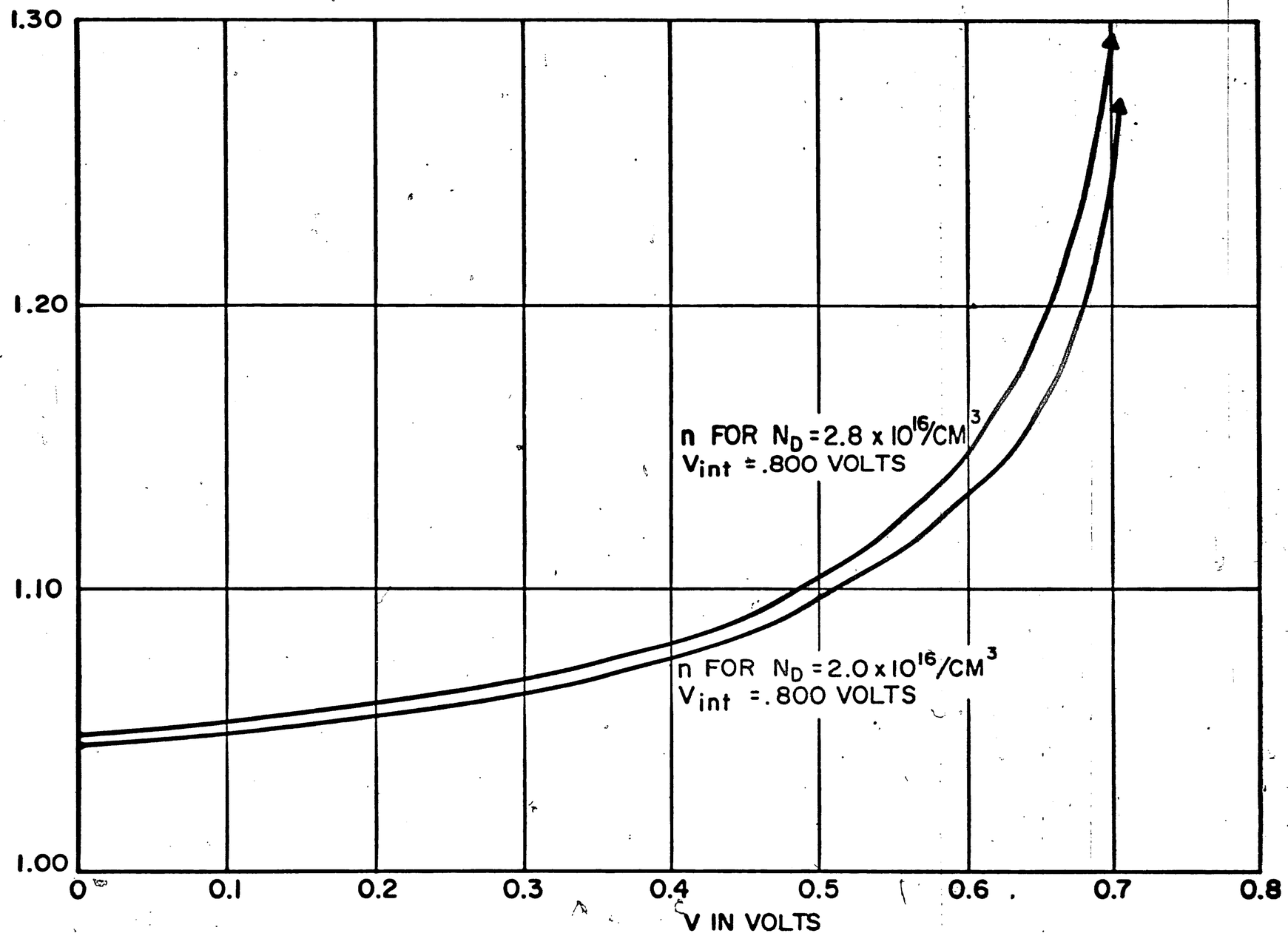

FIG. 12 IDEAL SCHOTTKY n AS A FUNCTION OF BIAS

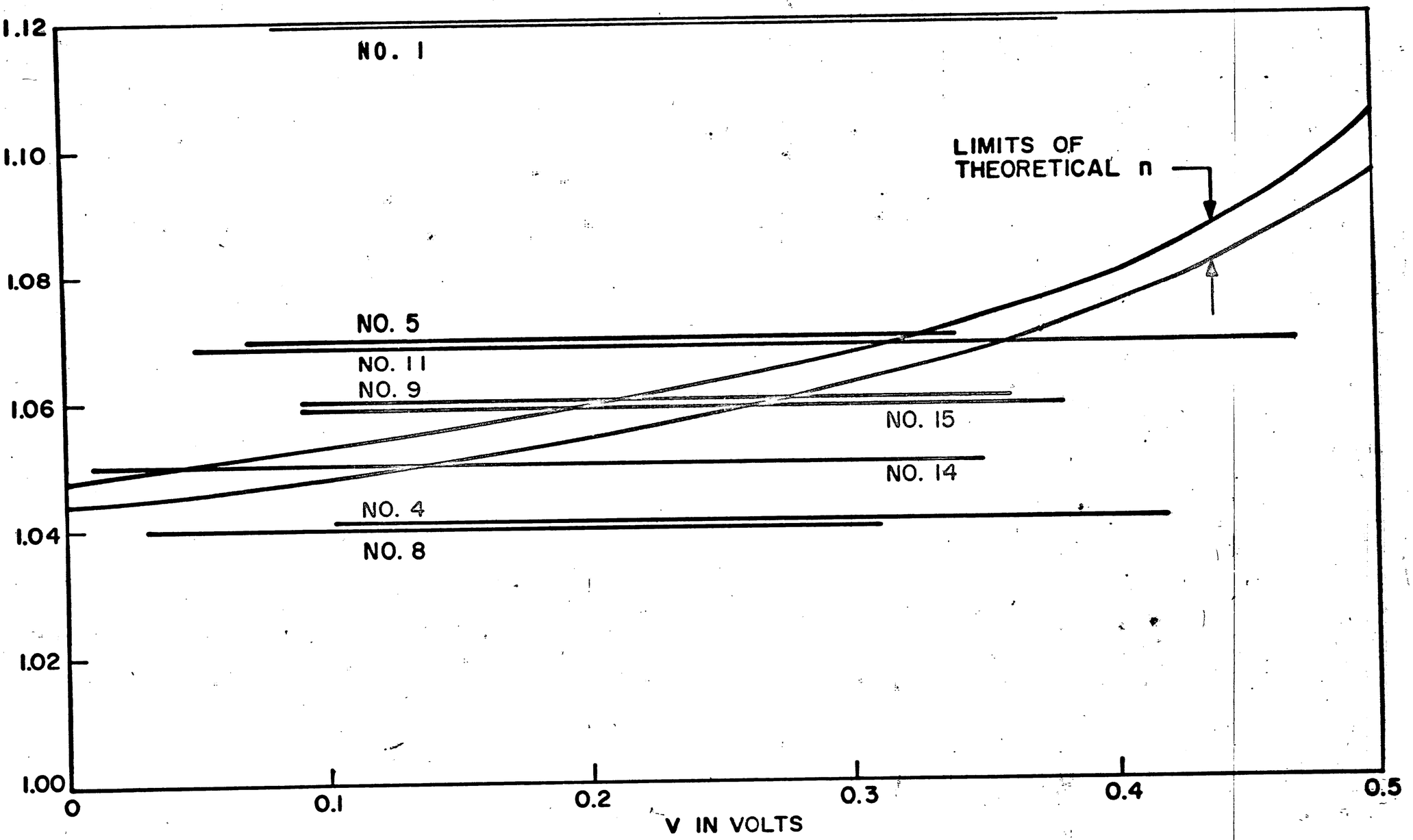

FIG. 13 COMPARISON OF EXPERIMENTAL AND THEORETICAL n

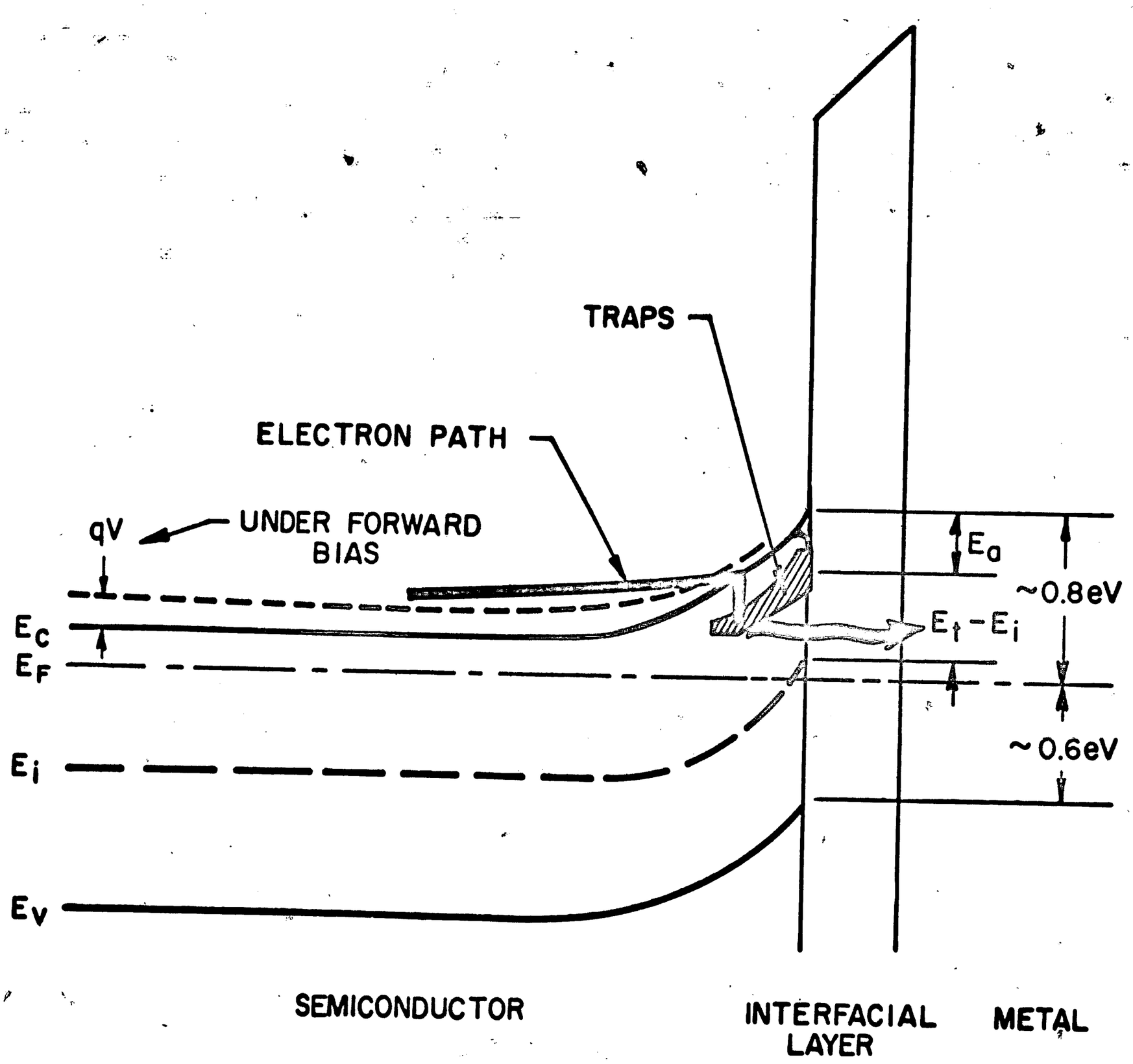

FIG. 14 SCHEMATIC OF TRAPPING MECHANISM

TABLE 3

Emphasis of Barrier Current at 300°K, Predominance of Schottky Current

unit	V_G' (volt)	n	I_D range (amp)	V_D range (volt)	$\frac{I}{I_{o_e}}$ at n = 1	$\frac{I}{I_{o_a}}$
#8	.000	1.16	10^{-9} to 10^{-5}	.08 to .35	1.0	1.0
	.072	1.11	10^{-9} to 10^{-5}	.15 to .36	5.3	1.1
	.094	1.12	10^{-9} to 10^{-5}	.17 to .36	10	1.4
	.144	1.08	10^{-9} to 10^{-7}	.18 to .30	47	5.9
	.216	1.04	10^{-8} to 10^{-6}	.25 to .31	640	59
	.288	nv*				

*not valid, because $V_D - V_G' < 0$

#1	.000	1.18	10^{-9} to 10^{-5}	.08 to .35	1.0	1.0
	.095	1.12	10^{-9} to 10^{-6}	.18 to .38	10	1.2
#4	.000	1.08	10^{-9} to 10^{-5}	.09 to .35	1.0	1.0
	.089	1.04	10^{-9} to 10^{-5}	.16 to .42	8.8	2.1
#5	.000	1.08	10^{-9} to 10^{-5}	.07 to .34	1.0	1.0
	.072	1.07	10^{-9} to 10^{-6}	.14 to .34	5.3	1.3
#9	.000	1.10	10^{-9} to 10^{-5}	.10 to .37	1.0	1.0
	.073	1.06	10^{-9} to 10^{-6}	.16 to .36	5.4	1.5
#11	.000	1.21	10^{-9} to 10^{-5}	.09 to .38	1.0	1.0
	.146	1.08*	10^{-9} to 10^{-5}	.20 to .47	50	4.3

*when corrected for resistive heating, n = 1.07

#14	.000	1.12	10^{-9} to 10^{-5}	.07 to .34	1.0	1.0
	.153	1.08*	10^{-9} to 10^{-6}	.16 to .35	62	12

*when corrected for resistive heating, n = 1.05

#15	.000	1.15	10^{-8} to 10^{-5}	.18 to .39	1.0	1.0
	.152	1.06	10^{-8} to 10^{-6}	.24 to .38	60	25

TABLE 4

Emphasis of Barrier Current at 77°K Predominance of Recombination Current

unit	V_G' (volt)	n	I_D range (amp)	V_D range (volt)	$\frac{I}{I_{o_e}}$ at n = 2	$\frac{I}{I_{o_e}}$ at n = 1	$\frac{I}{I_{o_a}}$
#8	.000	3.92	10^{-10} to 10^{-8}	.57 to .59	1.0	1.0	1.0
		3.04	10^{-8} to 10^{-5}	.69 to .82			
	.094	2.56	10^{-10} to 10^{-8}	.72 to .80	6.0×10^{2}		0.2
	.144	2.78	10^{-10} to 10^{-9}	.73 to .78	2.6×10^{4}		1.0
		2.20	10^{-8} to 10^{-6}	.82 to .88			
	.216	2.26	10^{-10} to 10^{-6}	.74 to .88	1.0×10^{7}		1.4×10^{2}
	.720	2.06	10^{-10} to 10^{-5}	.76 to .94	1.0×10^{25}	5.0×10^{41}	2.0×10^{16}
#1	.000	3.05	10^{-9} to 10^{-4}	.65 to .88	1.0	1.0	1.0
	.219	2.27	10^{-9} to 10^{-6}	.79 to .88	1.0×10^{7}	1.0×10^{13}	1.9×10^{2}
#4	.000	1.74	10^{-9} to 10^{-6}	.58 to .67	1.0	1.0	1.0
	.206	1.54	10^{-9} to 10^{-7}	.63 to .69	6.5×10^{6}	1.6×10^{12}	4.8×10^{3}
#5	.000	3.08	10^{-10} to 10^{-8}	.63 to .72	1.0	1.0	1.0
	.216	2.00	10^{-10} to 10^{-8}	.72 to .78	1.0×10^{7}	1.0×10^{13}	2.2×10^{4}
#9	.000	4.59	10^{-9} to 10^{-7}	.60 to .74	1.0	1.0	1.0
	.752	2.18	10^{-9} to 10^{-7}	.75 to .85	1.7×10^{26}	4.0×10^{43}	2.5×10^{19}
#14	.000	4.39	10^{-10} to 10^{-8}	.51 to .60	1.0	1.0	1.0
	.765	2.12	10^{-10} to 10^{-7}	.73 to .83	5.0×10^{26}	4.0×10^{44}	7.5×10^{18}
#15	.000	2.46	10^{-9} to 10^{-6}	.53 to .61	1.0	1.0	1.0
	.758	2.00	10^{-10} to 10^{-6}	.62 to .74	2.4×10^{26}	1.0×10^{44}	6.2×10^{21}

TABLE 5

Effectiveness of Guarding Mechanism
(Unit #8)

ambient	unguarded n	minimum n	V_D range for minimum n (volt)
atmosphere at prior date	1.16 (4 decades)	1.04 (2 decades)	.25 to .31
atmosphere	1.17 (3 decades)	1.09 (4 decades)	.16 to .42
CO_2 at 1.0 SLPM	1.17 (4 decades)	1.10 (4 decades)	.18 to .45
CO_2 at 1.0 SLPM waxed diode	1.24 (5 decades)	1.07 (2 decades)	.20 to .33
atmosphere dewaxed diode	1.17 (3 decades)	1.09 (4 decades)	.16 to .42

TABLE 6

Effect of Crowding the Current Toward the Edges of an Etched Diode (Unit #14)

ambient	V_G (volt)	n	I_D range (amp)
atmosphere at 300°K	.00	1.18	10^{-8} to 10^{-5}
	.10	1.30	" "
	.20	1.33	" "
	.30	1.33	" "
CO_2 at 1 SLPM and 300°K	.00	1.15	10^{-7} to 10^{-5}
	.10	1.34	10^{-8} to 10^{-4}
	.30	1.37	10^{-9} to 10^{-6}
	.40	1.37	" "
liquid N_2 at 77°K	.00	3.28	10^{-6} to 10^{-4}
	.10	3.37	10^{-7} to 10^{-4}
	.13	3.64	10^{-6} to 10^{-4}

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VITA

Richard W. Ralston was born to Elizabeth M. and Albert E. Ralston in Meriden, Connecticut, on October 11, 1942. He attended Southington High School in Southington, Connecticut, where he graduated valedictorian in 1960. In 1964, he received his Bachelor of Science degree in electrical engineering from Lehigh University, graduating with both highest and interdepartmental honors. Mr. Ralston is a member of the IEEE, Eta Kappa Nu, Tau Beta Pi, and Phi Beta Kappa. Since June, 1964, the author has been a member of the technical staff at Bell Telephone Laboratories, Incorporated.