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CHARACTERIZATION OF THE ANOMALOUS DIFFUSION EFFECT: EMITTER PUSH-OUT FOR A N-P-N TRANSISTOR

by

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ABSTRACT

The effects of the diffusion anomaly emitter push-out on the physical and electrical parameters of a n-p-n transistor structure has been investigated. The standard buried collector n-p-n transistor structure, which is simply a double diffused epitaxial process with a buried layer was used. The process steps of concern here consisted of a phosphorus diffused emitter and a boron diffused base.

Two groups were processed, with one group having shallow base depths and "push-thru" which occurs when the emitter depth becomes greater than the base depth. The other group had deeper base depths and longer emitter diffusion times, but no occurrence of push-thru. Push-out was observed in both groups and found to be greatly influenced by emitter depth, emitter diffusion time, and base depth. Emitter push-out also altered the transistor structure so that the electrical parameters could be influenced by two distinct base widths, W1 and W2. W1 is the base width under the base while W2 is at the curved part of the

periphery. This study found the dominant base width affecting the electrical paramters to be W2, after push-thru.

1. INTRODUCTION [1]

The semiconductor industry makes extensive use of the diffusion phenomenon (developed by Dr. Adolf Fick in 1855) as a basic fabrication step in the manufacture of electronic semiconductor devices.

Fick, in order to explain the movement of salts in solution through porous membranes, developed the famous diffusion laws which bear his name, i.e.

(1) $J = -D \, (\partial c / \partial x)$

(2) $\partial c / \partial t = D \, (\partial^2 c / \partial^2 x)$

These equations lack precision because the diffusion coefficient D is assumed constant whereas in reality it could be a function of the extensive properties of the substances involved, such as impurity concentration. The correct equation in this case is:

(3) $\partial c / \partial t = (\partial / \partial x) \, [D(c) \, (\partial c / \partial x)]$

Initial studies were of gases and liquids because the distances involved were greater than in solids, hence easier to measure. Metals which were next to be studied proved to be very complex.

On a microscopic scale metals are composed of grains of a uniform crystalline structure randomly orientated with respect to each other. Therefore diffusion occurs both within a grain and along the grain boundaries.

More recently, diffusion in semiconductor single crystals have been investigated. Studies have been made of diffusion not only in germanium and silicon, but also in III-V compounds such as gallium arsenide. Because of its prevalence, silicon is the focus of most of the diffusion studies in semiconductors.

The first order diffusion theory developed by Fick provided an adequate foundation for processing of the first semiconductor devices but as devices became smaller a need arose for understanding the second order effects. Apart from those caused by incorrectly defined boundary conditions, the observed departures from first order theory have been attributed to a variety of interactions of diffusing species with silicon lattice defects or with other impurities. These second order effects are referred to as anomalies because they were not well understood.

This thesis concerns itself with one of these anomalies, called emitter push, push-out or emitter dip. Emitter push-out occurs during the fabrication of diffused transistors. An n-p-n diffused transistor is made by first diffusing boron, an p-type dopant, into an n-type silicon wafer in selected areas to form the base layer. Phosphorus is diffused into an area within the base region to form an n-type emitter region. The emitter push-out effect, shown in figure 1, is an enhancement of the boron layer under the phosphorus diffused layer. This effect is significant in the fabrication of semiconductor devices because of the impact on the electrical characteristics of the individual devices.

A study has been made here in which emitter push-out is correlated to certain transistor characteristics, such as transistor gain and breakdown voltages.

2. BACKGROUND ([2],[3])

Fabrication of a typical transistor starts with a flat polished slice of n-type silicon. Figure 2, shows a sequence followed when fabricating a simple n-p-n bipolar transistor. An oxide masking layer is first grown on the wafer. Windows are then opened in the oxide by a photolithographic process to allow the diffusion of a p-type dopant into the n-type substrate in the opened areas. In those areas a reversal of conductivity type occurs by a process known as compensation doping. [4] Another oxide layer is grown and smaller windows are opened, followed by the diffusion of an n-type dopant. The p-type region forms the base of the transistor, the n-type substrate the collector and the n-type diffused region the emitter. Figure 3, depicts the concentration profiles which ideally result from such a process. This process produces a higher impurity concentration in the emitter than in the base.

One of the problems inherent in controlling a double diffused process is that every subsequent heat treatment causes further diffusion of the dopant introduced during the previous stage. This can cause contamination, introduction of dislocations and other defects which can have spurious effects on lifetime and other device parameters. One common effect of this fundamental limitation is "emitter push-out". It is the enhanced penetration of the base junction directly below the emitter diffusion, as shown in figure 4. Emitter push-out has been categorized as an anomalous diffusion effect due to its non-adherence to simple solutions of Fick's laws.

3. OCCURRENCE OF EMITTER PUSH-OUT [5]

It is now generally accepted by persons in this field (Fair [6], et al), that the diffusion of particular dopants, such as phosphorus into silcon from a high surface concentration is accompanied by an injection or generation of point defects which causes an enhancement in the diffusion of background dopants. [7]

Point defects can be generated by moving dislocations. When the phosphorus concentration is sufficently high, the size mismatch of the phosphorus and silicon can produce stresses which exceed the elastic limit resulting in dislocations. The simplest point defects are vacancies and interstitial atoms, both of which have been proposed as mechanisms for diffusion. [8]

Consequently, conditions which increase the number of dislocations and/or point defects in local areas will also locally enhance diffusion. This results, for example in "emitter push-out". The magnitude of push-out has been strongly correlated to the phosphorus surface concentration, the phosphorus diffusion time and the boron diffusion depth. [9] This thesis will attempt to substantiate these claims and test some aspects of Lee's [10] theory with the direct measurement of emitter push-out and the analysis of transistor parametric data. It is also aimed at establishing other correlations between push-out and transistor parameters. In addition, it will explore the effective base width in a pushed-out structure, ie. Is the dominant base width under the base or at the curved part of the periphery?

4. EXPERIMENTAL METHODS

4.1. DESCRIPTION OF THE STANDARD BURIED COLLECTOR NPN TRANSISTOR

The transistor studied in this thesis uses the standard buried collector structure. It is the oldest of the bipolar technologies. Thru the years it has evolved into a versatile structure which can be used for many typical logic circuit configurations.

In figure 5A, we have the circuit symbol for an NPN transistor. Figure 5B, shows a top view of the standard buried collector n-p-n vertical transistor and the appropiate places for the collector, base and emitter transistor terminals. Below that, figure 5C gives a cut away view of the transistor with the numbered areas described as follows:

1-	p+	isolation ring (boron)
2-	n+	buried layer collector contact (antimony)
3-	n+	contact for buried layer (phosphorus)
4-	p	base (boron)
5-	n+	emitter (phosphorus)
6-	n	epitaxial layer (phoshorous)

7- p- <111> oriented silicon substrate doped with boron

Typical design parameters for integrated circuit transistors are shown in table 1.

Since this study concerns itself with emitter push-out, only the base and emitter diffusions will be described in detail here.

4.2. BORON BASE DIFFUSION

The boron base diffusion was done in two steps. A deposition to provide a limited source of diffusant was implemented first and then a drive-in to increase the base depth. The deposition for group 1 was carried out at 905*C for 50 minutes. For group 2, the deposition temperature was 880*C for 45 minutes. The source was liquid boron tribromide maintained at 30*C. The furnace gas consisted of nitrogen as the carrier with 1.0% of oxygen in the total flow.

The base drive-in was carried out at 1100*C in a nitrogen environment with 1.0% oxygen. Sample 1 was driven-in for 80 minutes while group 2 had 88 minutes.

4.3. PHOSPHORUS EMITTER DIFFUSION

The phosphorus emitter diffusion was done at 950*C, with 10% oxygen in a nitrogen ambient. The source was liquid phosphorus tribromide kept at 35*C. Both groups 1 and 2 had varied diffusion times of (55 + t) minutes.

4.4. INTERFERNCE FRINGES METHOD

Diffusion depths were measured by using interference fringes. A sodium light source was used on half degree bevelled samples which were stained with hydrofluoric acid. A full explanation of the interference fringes method can be found in Lee [11]. For ease in bevelling and measurement, larger areas were used where the base and emitter diffusions were done. A bevelled and stained sample is shown in the photographs of figures 6A and 6B. The same sample is shown in figure 6C with the interference fringes.

4.5. SPREADING RESISTANCE TECHNIQUE

The spreading resistance technique determines the doping profile of a multilayer integrated circuit from the surface thru the p-n junctions and thru to the substrate. Resistance values were obtained by a two probe spreading resistance method and then converted to a concentration profile by a computer program. Refer to Maes [12] for a description of the spreading resistance technique. A cross section of the diffusion profile of a typical standard buried collector n-p-n transistor is illustrated in figure 7. Figure 8 shows the resulting diffusion profile generated by the spreading resistance method, with a ASR-100 Spreading Resistance Probe System, using 5 micron steps. This sample is the same one that was used for the interference measurement in figure 6.

The emitter surface concentration, emitter depth and pushed-out base depth can be extracted from the spreading resistance concentration profile plot. The graphs of figures 9 and 10 compare the emitter depths and pushed-out base depths measured by the interference fringe method with those obtained by the spreading resistance method. The two methods tracked very favorably as can be seen from the graphs, proving that the data is accurate for these measurements. Data for the non pushed-out base depth was only obtainable from the interference fringe method, because the area of the non-pushed-out base was too small for a spreading resistance measurement to be taken. So for consistency only data from the interference fringe method will be used for the emitter, non-pushed-out base, and pushed-out base depths.

4.6. TRANSISTOR BREAKDOWN VOLTAGES

A breakdown voltage is defined as the maximum voltage that can be applied to a junction before the current increases very rapidly as an additional increment of voltage is applied. The collector emitter breakdown voltage is of interest in this study because it is an important electrical parameter.

4.6.1. βV_{ces}

The collector emitter breakdown voltage with the base shorted to the emitter (βV_{ces}) was measured by putting a 10ua source across the collector and emitter terminals and using a digital voltmeter (DVM) as shown in figure 11. [13]

4.6.2. βV_{ceo}

The collector emitter breakdown voltage with the base open (βV_{ceo}) was measured in a similar fashion as the βV_{ces} and is depicted in figure 12. [14]

4.7. TRANSISTOR GAIN

4.7.1. FORWARD GAIN

The forward gain can be calculated by dividing a known emitter current by a measured base current,

(4) $\beta_f = I_e/I_b$

A 100ua current source is put across the collector and emitter terminals, and a precision ammeter (PAM) is is used to measure the base current as shown in figure 13. [15]

4.7.2. REVERSE GAIN

The reverse gain can be calculated by dividing a known collector current by a measured base current,

(5) $\beta_r = I_c/I_b$

This is the same procedure as for the forward gain with the differences shown in figure 14. [16]

5. ANALYSIS OF PHYSICAL DATA

This chapter focuses on the variance of in process parameters such as emitter diffusion time, push-out, base width, and non-pushed-out base depth. Two groups were processed with different base depths and emitter diffusion times to give resultant populations at both ends of the data spectrum. Group 1 had an average base depth of $\overline{B}$=1.46 um while group 2 had a deeper base depth of $\overline{B}$=2.46 um. Also group 2 received emitter diffusion times of t=110-135 minutes which were longer than the t=57-89 minutes done for group 1. Figure 15 gives a description of the variables used in this analysis. Since emitter diffusion time was varied in this experiment, it will be used in most of the graphs. Increasing emitter diffusion time can be correlated to increasing emitter depth as shown previously in figure 9. The data for these variables can be found in tables 2, 3, 4, and 5. All data plots in this thesis have been curve fitted by nth order regressions using the method of least squares.

Sections 5.1 and 5.2 deal with results of push-out that have also been obtained by Lee [17], et al. This allows the data to be used with confidence later in answering the question: what is the effective base width of the pushed-out transistor? Figure 15 indicates two possible base widths W1 and W2. W1 is the vertical distance between the emitter depth and the pushed-out base depth, while W2 is the shortest distance between the curved part of the emitter periphery and the curved part of the non- pushed-out base periphery. It will be shown later that the data tends to suggest W2 as the dominant effective base width, after "push-thru". Push-thru used here is defined as the condition after which the emitter depth is greater than the non-pushed-out base depth as shown in figure 16.

5.1. PUSH-OUT vs EMITTER DIFFUSION TIME

The results for groups 1 and 2 in figures 17 and 18 respectively show an increase in push-out for increasing emitter diffusion time. The slope for group 1 is greater than group 2, indicating that push-out effects decrease with deeper base depths. These results agree with the theoretical and experimental data obtained by Lee [18]. Figure 19 indicates the position of the data obtained here with Lee's theoretical curve, and shows that group 2 as expected had less push-out than group 1.

5.2. PUSH-OUT vs NON-PUSHED-OUT BASE DEPTH

Figures 20 and 21 show that less push-out occurs for group 2 base depths, even though group 2 had longer diffusion times. This implies that push-out depends on the proximity of the emitter depth to the base depth. The data in this section agrees with Lee's [19] theoretical and experimental data. Figure 22 indicates the data for groups 1 and 2 plotted with respect to Lee's theorectical curves, showing as in section 5.1 that group 2 as expected had less push-out than group 1.

5.3. BASE WIDTH vs EMITTER DIFFUSION TIME

As mentioned previously, there are two possible base widths W1 and W2 for the newly formed pushed-out transistor structure. Figures 23 and 24 for group 1 and figures 25 and 26 for group 2 show that W2 decreases more rapidly than W1 for increasing emitter diffusion times. It should be noted that W2 is always less than W1 for a given emitter diffusion time and that data for W2 in general fits better with emitter diffusion time than W1 for both groups. In the case of group 1, "push-thru" starts at an emitter time of about t=75 minutes, as indicated previously by figure 16. At this point the emitter depth equals the base depth and W2 becomes the fixed lateral distance between the emitter wall and base wall. The effects of push-thru will be seen later in the electrical data. Group 2 which had a deeper base depth did not exhibit this phenomenon for the emitter diffusion times used.

5.4. PUSH-OUT vs BASE WIDTH

Figures 27 and 28 for group 1 and figures 29 and 30 for group 2 show that base widths W1 and W2 both tend to decrease with increasing push-out. Figure 29 for group 2 shows poor a correlation of data points but the trend of smaller W1 for larger push-out is still evident. As in section 5.3, the graphs for W2 have a better correlation factor to push-out than W1 for both groups.

5.5. BASE WIDTH W2 vs BASE WIDTH W1

For group 1, W2 = (K1)(W1) before push-thru and W2 = (K2)(W1) afterwards. The slope K2 is less than K1 because after push-thru W2 remains constant. The change in slope occurs at about W1 = 0.5um as shown by figure 31. The graph for group 2 in figure 32 does not indicate an abrupt change in slope. This is consistent for the data obtained for group 2 because no push-thru has occured.

6. ANALYSIS OF ELECTRICAL DATA

This section will correlate the physical data with the electrical data. Such parameters as forward gain, reverse gain, and collector-emitter breakdown voltages will be discussed.

6.1. FORWARD GAIN vs EMITTER DIFFUSION TIME

The data for group 1 in figure 33 shows a shift to higher forward gains after push-thru at approximately t=75 minutes. It will be shown later that after push-thru the dominant effective base width is W2. Figure 34 shows a consistent increase in forward gain for group 2 with no drastic shift in gain, because no push-thru has occured.

6.2. REVERSE GAIN vs EMITTER DIFFUSION TIME

Figure 35 indicates a gradual increase in reverse gain for group 1 with increasing emitter diffusion time. No reverse gain data was obtained for group 2, because no reverse gain computer program was available for group 2.

6.3. βV_{ces} vs EMITTER DIFFUSION TIME

Group 1 data in figure 36 shows an abrupt downward shift in breakdown voltage at about t=75 minutes. This coincides with the abrupt upward shift in forward gain at the same emitter diffusion time. The data for group 2 in Figure 37 shows a gradual decrease in βV_{ces} as the emitter diffusion time is increased. Since base width decreases with increasing emitter diffusion time, it can be stated that smaller base widths cause lower breakdown voltages. This is consistent with theory. [20]

6.4. βV_{ceo} vs EMITTER DIFFUSION TIME

The graphs for both groups 1 and 2 in figures 38 and 39 show a decrease in βV_{ceo} with increasing emitter diffusion time. It should be noted that no shift occurs for group 1 as in figure 36 (βV_{ces} vs t), because the base is open and not shorted to the emitter. This eliminates the shift caused by push-thru.

6.5. FORWARD GAIN vs 1/(BASE WIDTH)

The graphs in figures 40 and 41 for group 1 show a good curve fit for both 1/W1 and 1/W2 against forward gain prior to push-thru. This indicates that both W1 and W2 contribute significantly to the forward gain before push-thru. After push-thru W2 fits better than W1 with forward gain. For group 2, figures 42 and 43 give an increase in forward gain for increasing 1/W1 and 1/W2, respectively. Both groups 1 and 2 show, as in previous sections, a statistically better fit for W2 data than W1 data when plotted against forward gain.

Assuming a graded base and low current levels, the approximate forward gain equation in terms of the base width for a grounded emitter n-p-n transistor, from Phillips [21] is:

$$(6) \quad \frac{1}{\beta_f} = \frac{R_{ee}}{R_{bb}} + \frac{W^2}{4 L_{nb}} + \frac{s A_s W}{A_e D_{nb}}$$

where W = base width

β_f = forward gain

L_{nb} = diffusion length of electrons in base

D_{nb} = electron diffusion coefficient in base

A_s = surface recombination area

A_e = emitter area

The first term on the right-hand side represents the emitter efficency and [22]

$$(7) \quad R_{ee} = \rho_e / L_{pe}$$

$$(8) \quad R_{bb} = \rho_b(x)/W.$$

where ρ_e = emitter resistivity

$\rho_b(x)$ = graded base resistivity

L_{pe} = diffusion length of holes in emitter

R_{ee} and R_{bb} are the sheet resistances of the emitter and base respectively. The second term on the right is the bulk recombination and since $W<<L_{nb}$, it can be neglected. The third term on the right is a measure of the surface recombination, and since s is small and $A_s >> A_e$, it can also be neglected.

Substituting equations 7 and 8 into 6 and approximating equation 6 further,

(9) $1/\beta_f = W/c$

where $c = \rho_b(x)\ L_{pe}/\rho_e$

re-writing equation 9 gives,

(10) $\beta_f = c/W$

Assuming that the possible base widths W1 and W2 each add to the forward gain, equation 10 becomes,

(11) $\beta_f = c\ [(1/W1) + (1/W2)]$

Looking at Table 5, 1/W1 and 1/W2 are both about the same magnitude for group 1 until t=75 minutes when push-thru occurs and 1/W2 becomes much greater than 1/W1. For group 2, 1/W1 and 1/W2 are the same magnitude because no push-thru has taken place.

The approximation for forward gain in a pushed-out transistor can now be written as:

(12) $\beta_f = c\ [(1/W1) + (1/W2)]$ for $t < t_p$

(13) $\beta_f = c\ (1/W2)$ for $t > t_p$

where t_p = emitter diffusion time at push-thru

$c = \rho_b(x)\ L_{pe}/\rho_e$

The variable slope c increases for increasing 1/(base width) as shown in figures 40 and 41. After push-thru when 1/W2 becomes constant, c still increases due to increasing average base resistivity, as shown in table 3 and again in table 5 for group 1. This explains why the data in table 5 indicates an increasing forward gain after push-thru even though 1/W2 remains constant.

Since gain is essentially proportional to the area of the base, the variable c must take into account the areas for both W1 and W2. [23] A better approximation for equations 12 and 13 would be

(14) $\beta_f = A1/W1 + A2/W2$ for $t<t_p$

(15) $\beta_f = A2/W2$ for $t>t_p$

where A1 = the area contributing to forward gain for W1

A2 = the area contributing to forward gain for W2

Figure 44 indicates that before push-thru A1 and A2 are almost equal and can be lumped into c, since both W1 and W2 contribute equally to the forward gain. After push-thru A2/W2 >> A1/W1, because W2 remains constant while A2 continues to increase. And now the gain can be represented by equation 15.

This section proves that W2 is the dominant effective base width after push-thru and shows that the relationship of forward gain to base width can be approximated by equations 14 and 15.

7. RESULTS AND CONCLUSIONS

Emitter push-out has been observed in this study to have a significant impact on the physical and electrical parameters of the n-p-n transistor.

An important result substantiating the accuracy of the physical data is that similar measurements were obtained from two different methods, the spreading resistance method and the interference fringes method.

The following is a summary of the effects of push-out on the transistor structure:

1- Emitter push-out increases with increasing emitter diffusion time and emitter depth.

2- The amount of push-out depends on the initial base depth. Shallow base depths will give more push-out than deep base depths.

3- Both base widths W1 and W2 decrease with increasing push-out.

4- Forward and reverse gain both increase with increasing push-out because of smaller base width.

5- Breakdown voltages βV_{ces} and βV_{ceo} both decrease with increasing push-out due also to smaller base width.

6- Both the forward gain and the βV_{ces} breakdown voltage graphs had an abrupt change at $t=t_p$ when push-thru occured in group 1.

7- The effective base width after "push-thru" was found to be W2.

In concluding, we can say that push-out effects in general followed the theory developed by Lee [24]. Measurements of the physical parameters by two methods produced similar results which proved the validity of the data. Two effective base widths were used to correlate the physical and electrical measurements up until the emitter, "pushed-thru" the original base, making W2 the controlling base width. Very high gain transistors with reasonable collector-emitter breakdown voltages can be realized by utilizing this pushed-out base phenomenon. The main problem in manufacturing such a device would be the ability to control the reproducibility of the emitter push-out effect. The author recognizes that further studies are necessary to determine the feasibility of mass producing devices using this phenomenon.

	Amplifying	Switching
Epitaxial Film		
Thickness	10 μm	3.5 μm
Resistivity	1 Ω-cm	0.3 – 0.8 Ω-cm
Sheet resistance	1000 Ω/□	1500 Ω/□
Buried Layer		
Sheet resistance	~20Ω/□	
Up diffusion	2.5 μm	1.4 μm
Emitter		
Diffusion depth in base	2.5 μm	0.8 μm
Sheet resistance	5 Ω/□	12 Ω/□
Base		
Diffusion depth	3.25 μm	1.3 μm
Sheet resistance	100 Ω/□	200 Ω/□
Oxide Thickness		
1. Background	0.8 μm	0.5 μm
2. Base	0.4 μm	0.33 μm
3. Emitter	0.3 μm	0.3 μm
Substrate		
Resistivity	~10 Ω-cm	
Orientation	⟨111⟩	

Table 1 - Typical Design Parameters for Integrated Circuit Transistors (from Muller and Kamins, Device Electronics for Integrated Circuits, Wiley, 1977)

TABLE 2

INTERFERENCE FRINGES DATA

	t	A	B	C	X	W1	W2
	min	um	um	um	um	um	um
group 1	57	1.18	1.50	1.87	.37	.69	.32
	65	1.34	1.61	1.87	.26	.53	.27
	65	1.34	1.47	1.82	.35	.48	.13
	67	1.20	1.44	1.77	.33	.57	.24
	67	1.31	1.52	1.87	.35	.56	.21
	71	1.31	1.42	1.82	.40	.51	.11
	77	1.36	1.42	1.87	.45	.51	.06
	81	1.44	1.44	1.87	.43	.43	.04
	89	1.44	1.34	1.74	.40	.30	.04
group 2	110	1.69	2.33	2.49	.16	.80	.64
	110	1.74	2.41	2.62	.21	.88	.67
	120	1.74	2.41	2.59	.18	.85	.67
	130	2.03	2.59	2.78	.25	.81	.56
	135	1.93	2.57	2.78	.21	.85	.64

t = emitter diffusion time
A = emitter depth
B = non-pushed-out base depth
C = pushed-out base depth
X = push-out (C-B)
W1 = base width 1 (C-A)
W2 = base width 2 (B-A) at A>B fixed width

TABLE 3

SPREADING RESISTANCE DATA

	t	A	C	N_s	$\overline{\rho_b}$
	min	um	um	1/cm3	ohm-cm
group 1	57	1.13	1.75	4.48E19	2.2
	65	1.14	1.81	5.18E19	3.3
	65	1.26	1.82	5.36E19	3.8
	67	1.33	1.96	4.83E19	3.1
	67	1.25	1.84	5.17E19	3.1
	71	1.27	1.83	4.61E19	3.8
	77	1.18	1.71	4.17E19	6.1
	81	1.40	1.73	4.87E19	5.3
	89	1.27	1.58	7.42E19	5.1
group 2	NO DATA				

t = emitter diffusion time
A = emitter depth
C = pushed-out base depth
N_s = emitter surface concentration
$\overline{\rho_b}$ = average base resistivity

TABLE 4

TRANSISTOR DATA

	t min	β_f	β_r	βV_{ces} volts	βV_{ceo} volts
group 1	57	99.60	2.10	38.63	13.65
	65	140.80	3.35	38.47	12.54
	65	154.30	4.76	38.19	11.65
	67	128.20	3.71	38.85	12.79
	67	136.20	5.76	37.94	11.95
	71	183.20	5.94	36.82	10.72
	77	357.95	9.63	20.64	9.39
	81	361.32	10.74	18.88	9.62
	89	439.53	12.91	11.77	7.74
group 2	110	64		24.31	7.33
	110	62		20.73	6.20
	120	80		24.27	6.95
	130	91		21.55	6.47
	135	100		20.02	5.72

t = emitter diffusion time
β_f = forward gain
β_r = reverse gain
βV_{ces} = collector-emitter breakdown voltage with base shorted to the emitter
βV_{ceo} = collector-emitter breakdown voltage with base open

TABLE 5

BASE WIDTH DATA

	β_f	1/W1 1/um	1/W2 1/um	$\overline{\rho}_b$ ohm-cm
group 1	99.60	1.45	3.13	2.2
	128.20	1.75	4.17	3.1
	136.20	1.79	4.76	3.1
	140.80	1.89	3.70	3.3
	154.30	2.08	7.69	3.8
	183.20	1.96	9.09	3.8
	357.95	1.96	16.67	6.1
	361.32	2.33	25.00	5.3
	439.53	3.33	25.00	5.1
group 2	62	1.14	1.47	
	64	1.25	1.56	
	80	1.18	1.49	
	91	1.23	1.78	
	100	1.18	1.56	

β_f = forward gain
W1 = base width 1 (C-A)
W2 = base width 2 (B-A) at A > B fixed width
$\overline{\rho}_b$ = average base resistivity

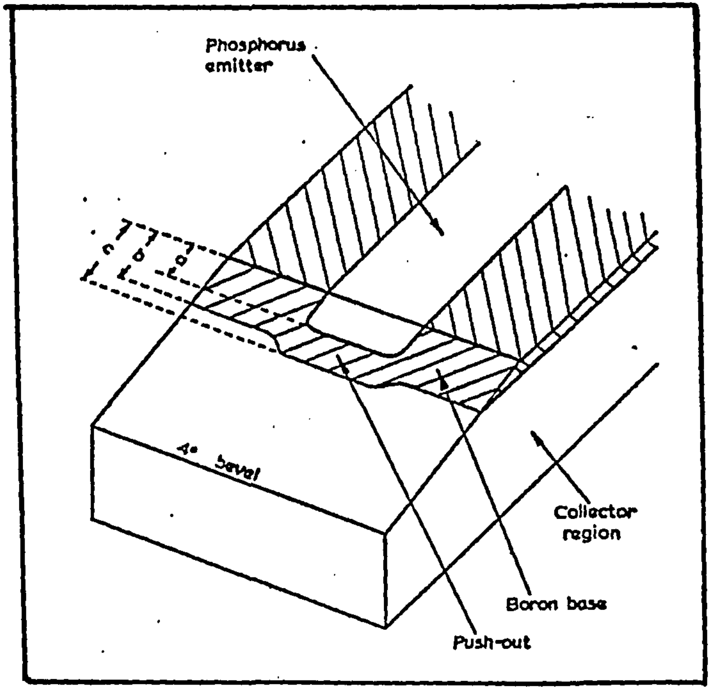


Figure 1 - Typical Structure after Bevelling and Staining (from Lee,"The Push-Out Effect in Silicon n-p-n Diffused Transistors", Phillips Research Laboratories, no. 5, 1974)

a= emitter depth
b= base depth
c= pushed-out base depth

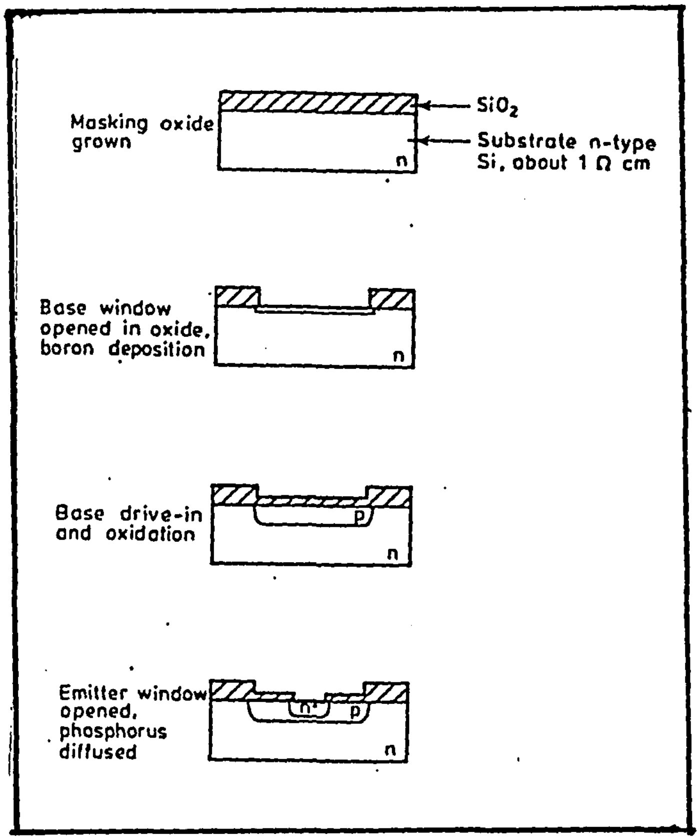


Figure 2 - Typical Fabrication Sequence for a n-p-n Planar Transistor (from Willoughby, "Double-Diffusion Processes in Silicon", in Wang, Impurity Doping Processes in Silicon, North-Holland, 1981)

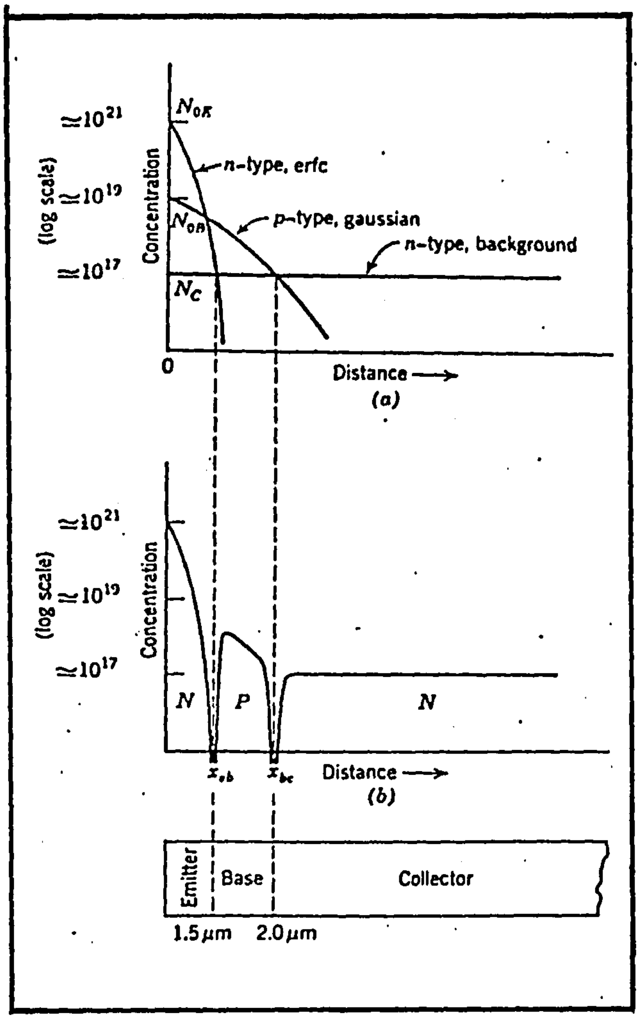


Figure 3 - Transistor formation by Diffusion (from Ghandhi, The Theory and Practice of Microelectronics, Wiley,1968)

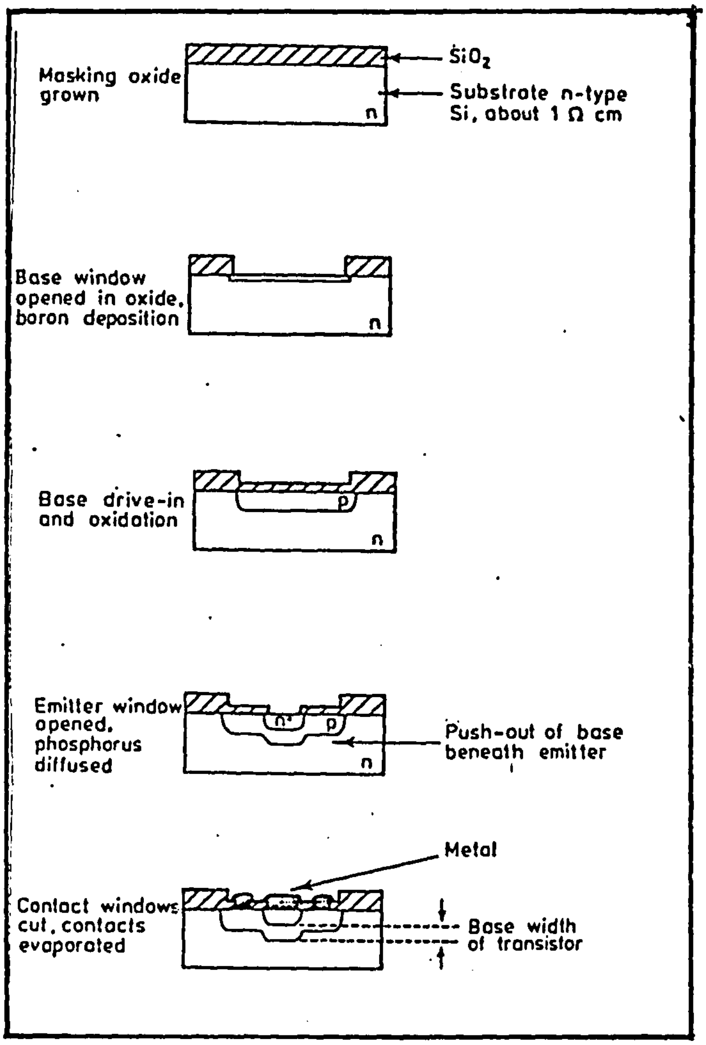


Figure 4 - The Emitter Push-Out Effect in an n-p-n Transistor (from Willoughby, "Double Diffusion Processes in Silicon", in Wang, Impurity Doping Processes in Silicon, North-Holland, 1981)

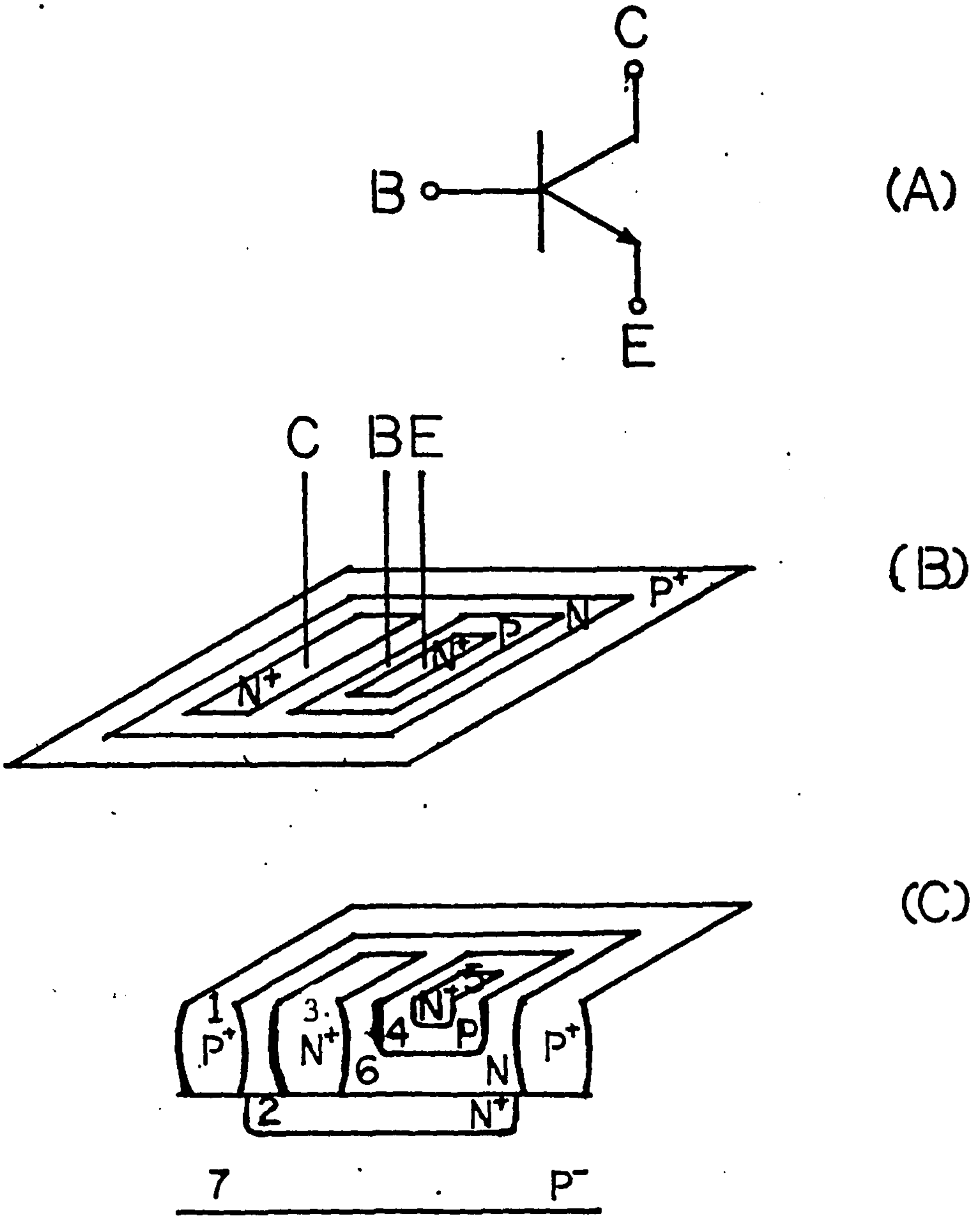


Figure 5 - Standard Buried Collector n-p-n Transistor

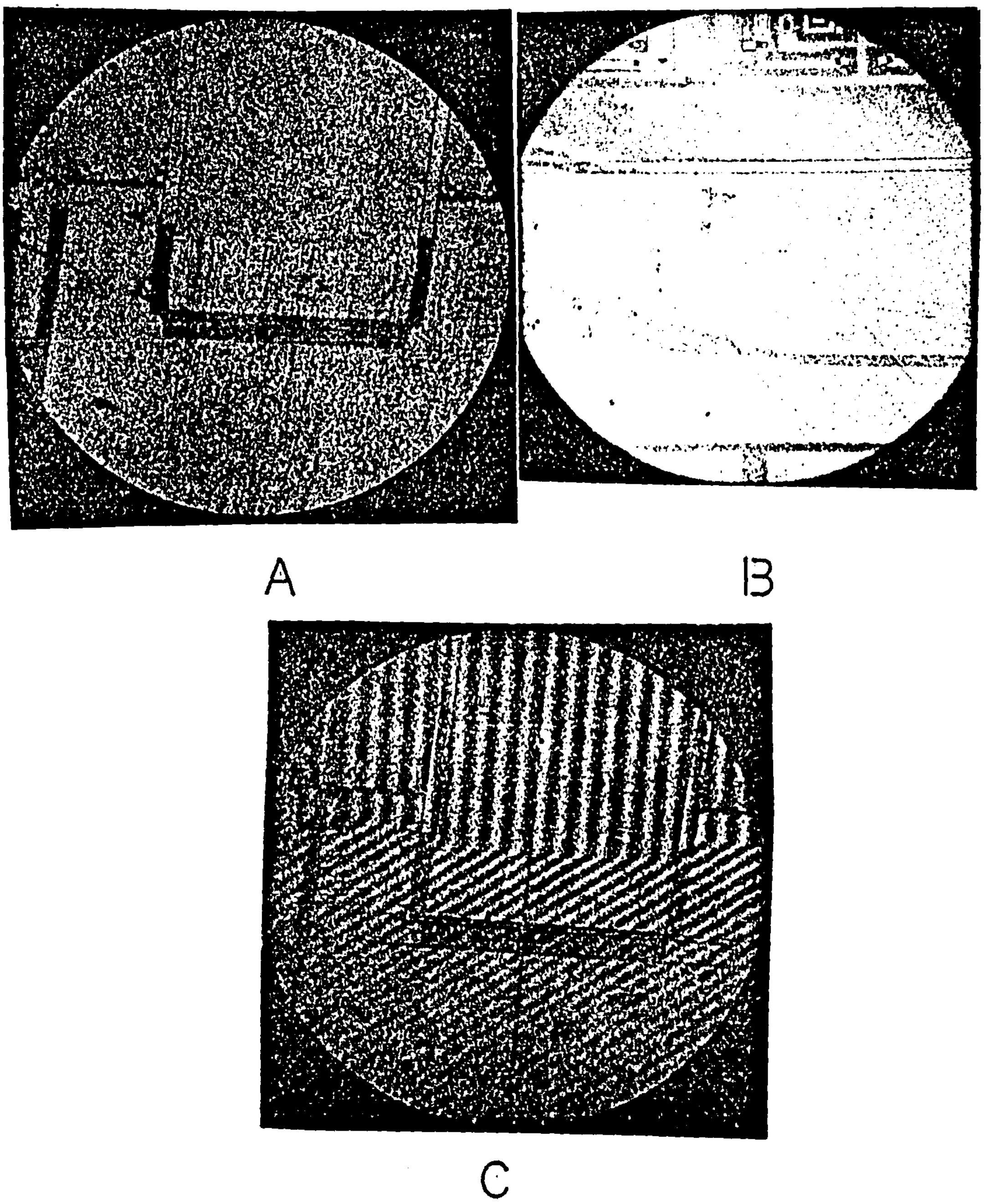


Figure 6 - Bevelled and Stained Sample, Interference Fringes Method

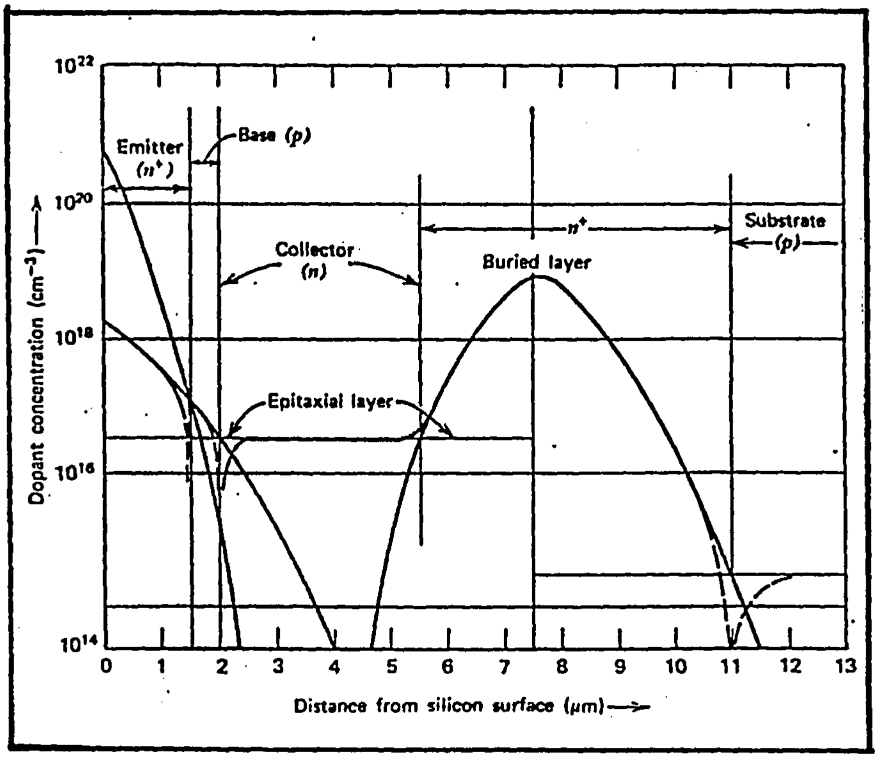


Figure 7 - Cross Section of the Diffusion Profile of an n-p-n Transistor (from Muller and Kamins, Device Electronics for Integrated Circuits, Wiley, 1977)

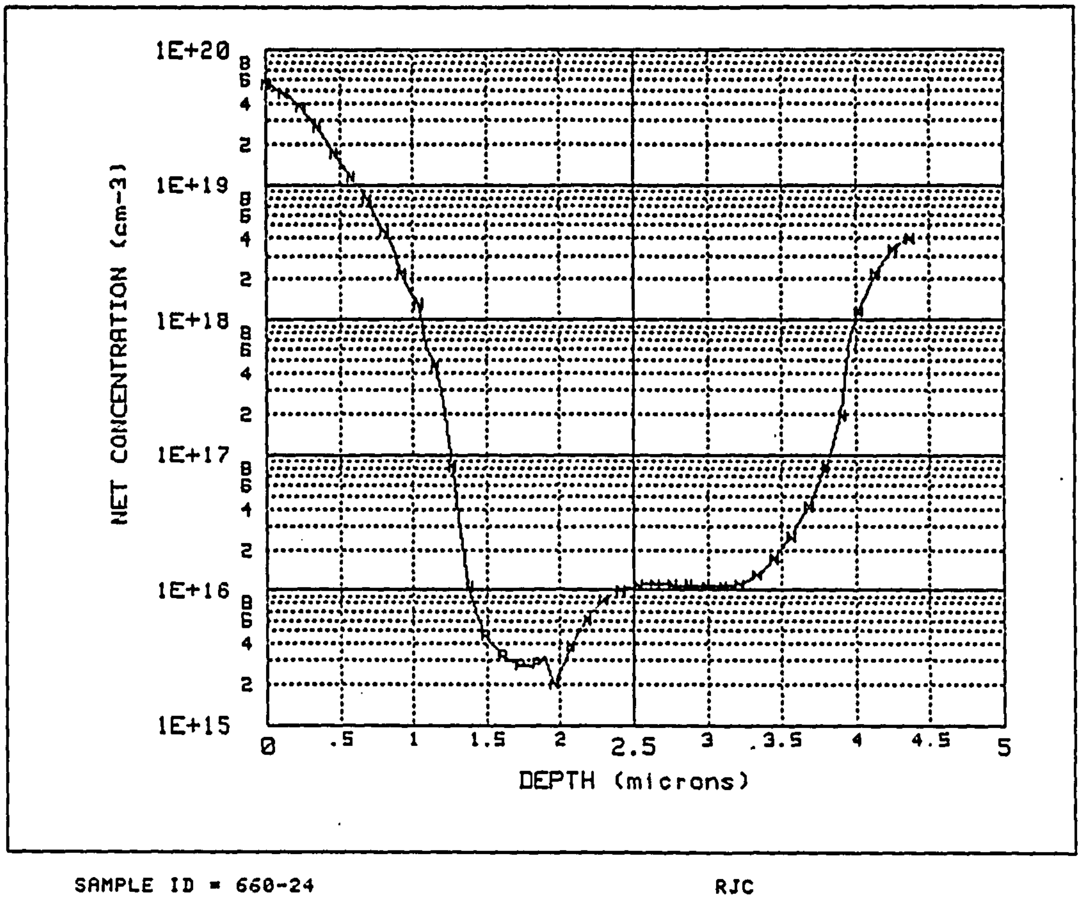


Figure 8 - Diffusion Profile of an n-p-n Transistor Generated by the Spreading Resistance Technique

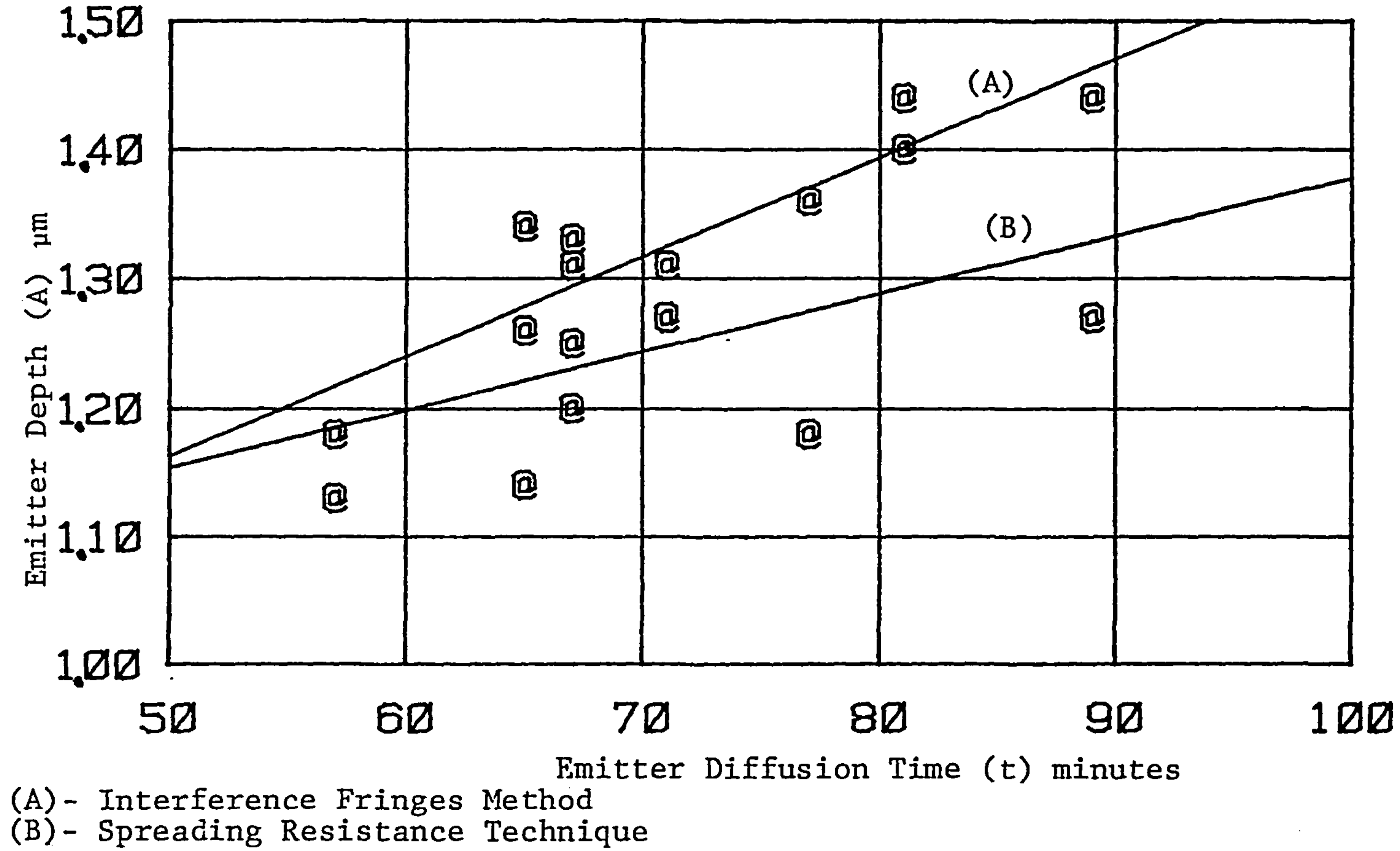
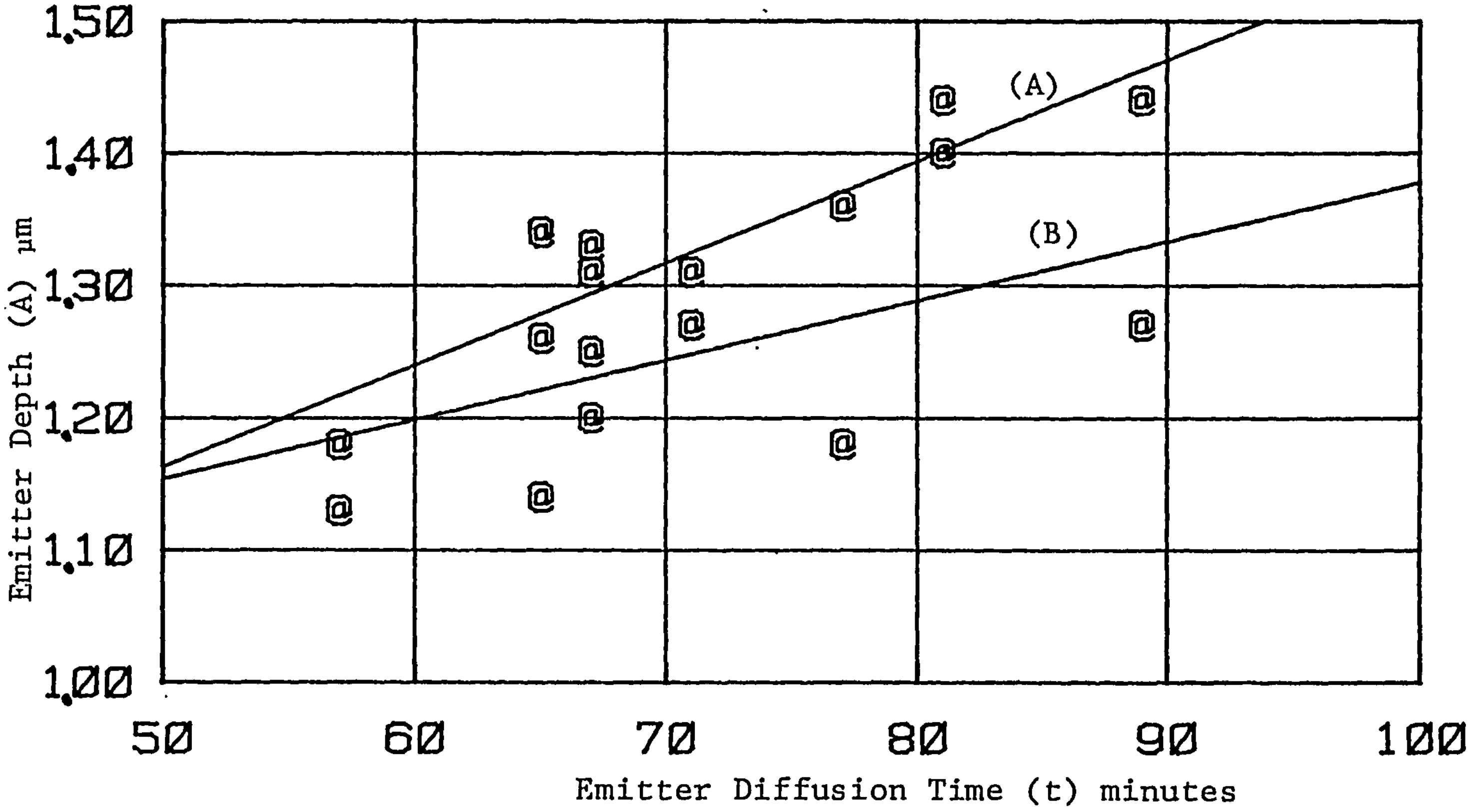
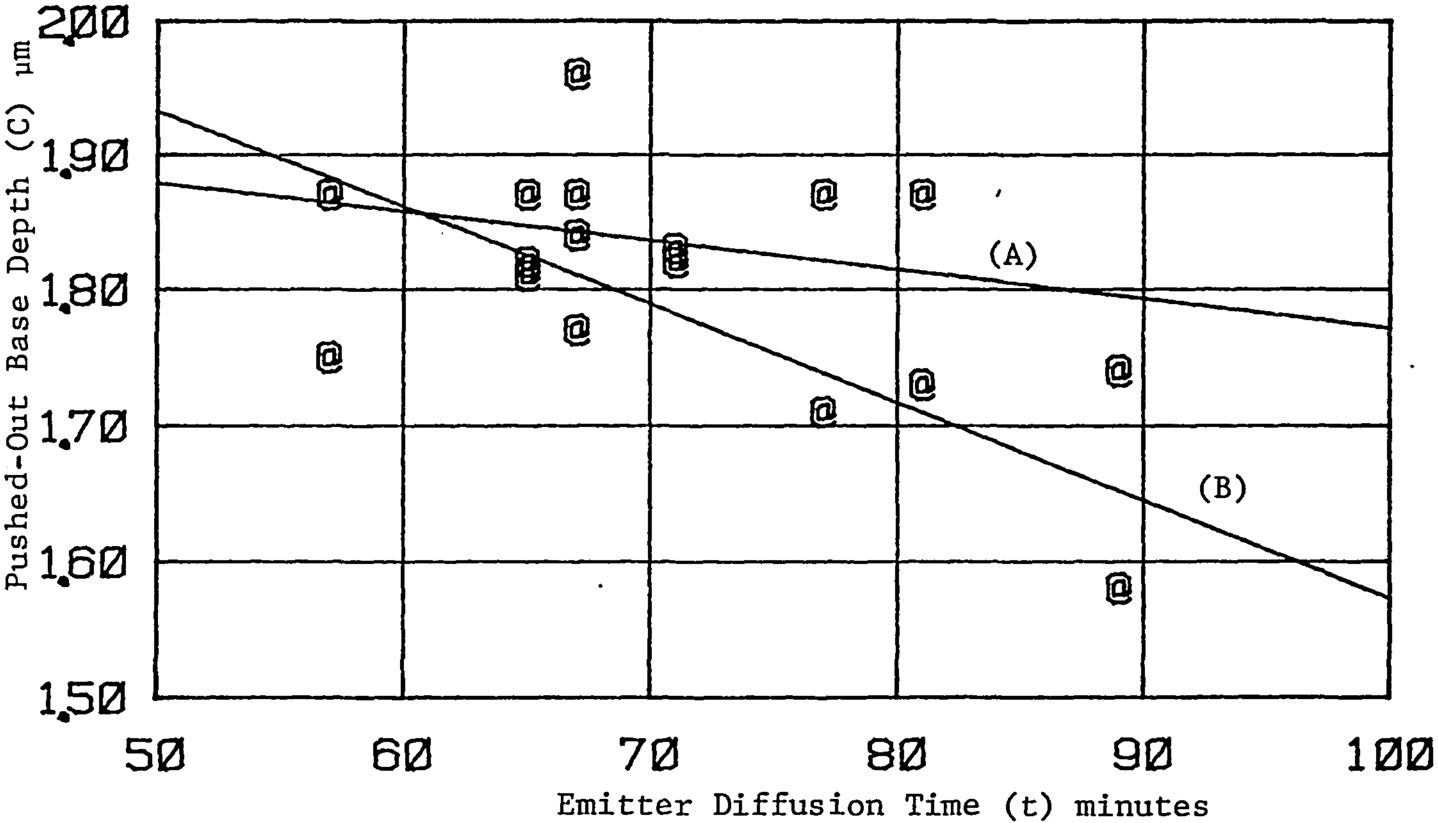


Figure 9 - Comparison of the Interference Fringes Method against the Spreading Resistance Technique



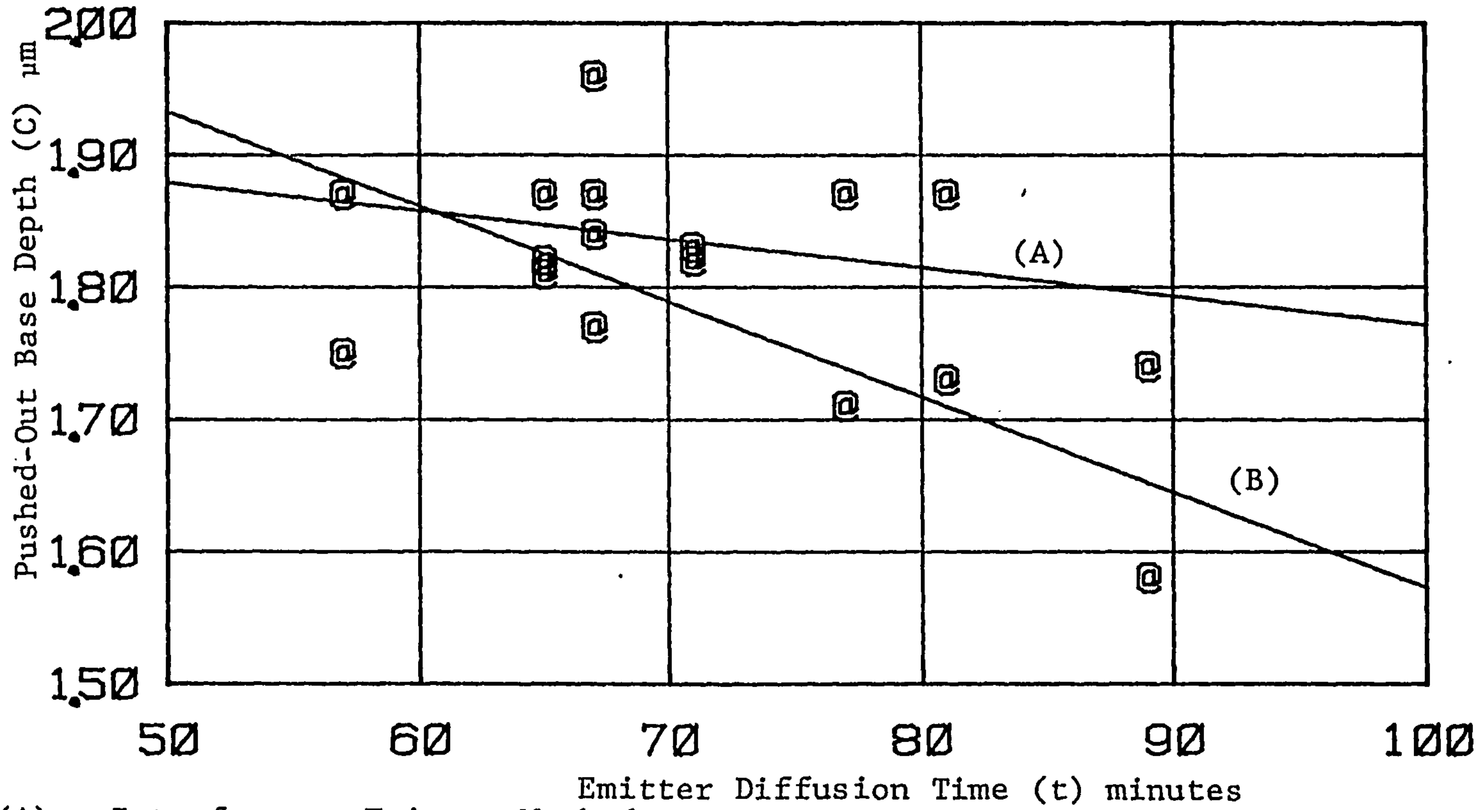
(A)- Interference Fringes Method
(B)- Spreading Resistance Technique

Figure 9 - Comparison of the Interference Fringes Method against the Spreading Resistance Technique



(A) - Interference Fringes Method
(B) - Spreading Resistance Technique

Figure 10 - Comparison of the Interference Fringes Method against the Spreading Resistance Technique



(A) - Interference Fringes Method
(B) - Spreading Resistance Technique

Figure 10 - Comparison of the Interference Fringes Method against the Spreading Resistance Technique

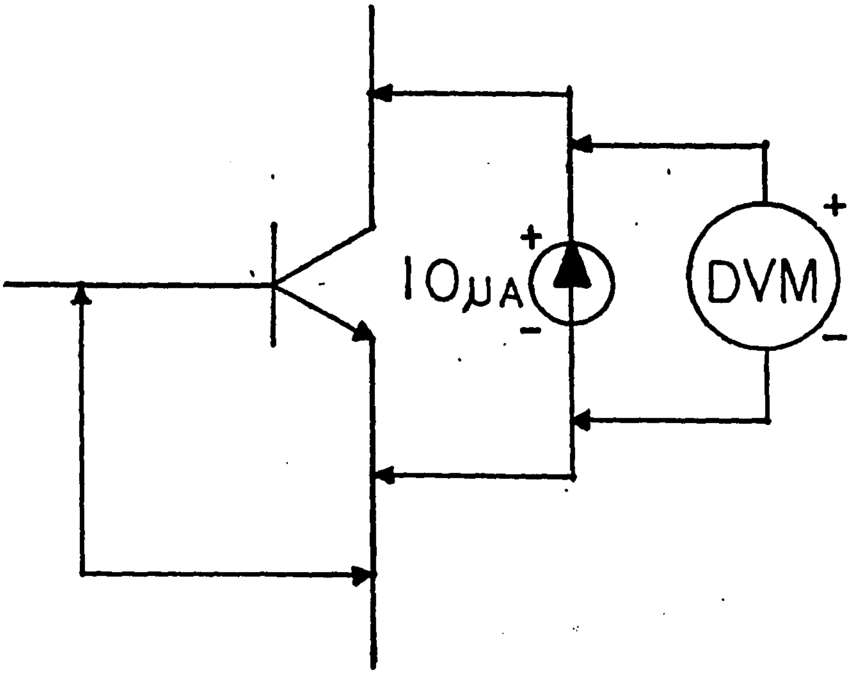


Figure 11 - βV_{ces} Breakdown Voltage

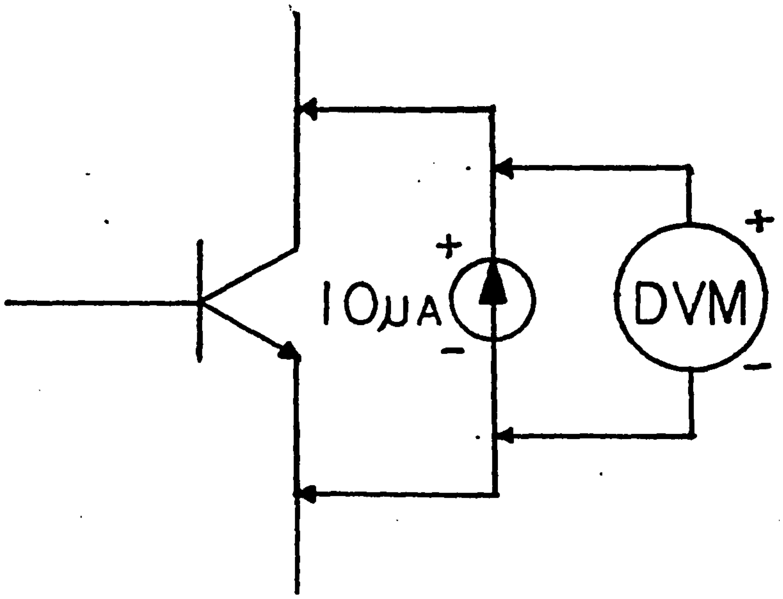


Figure 12 - βV_{ceo} Breakdown Voltage

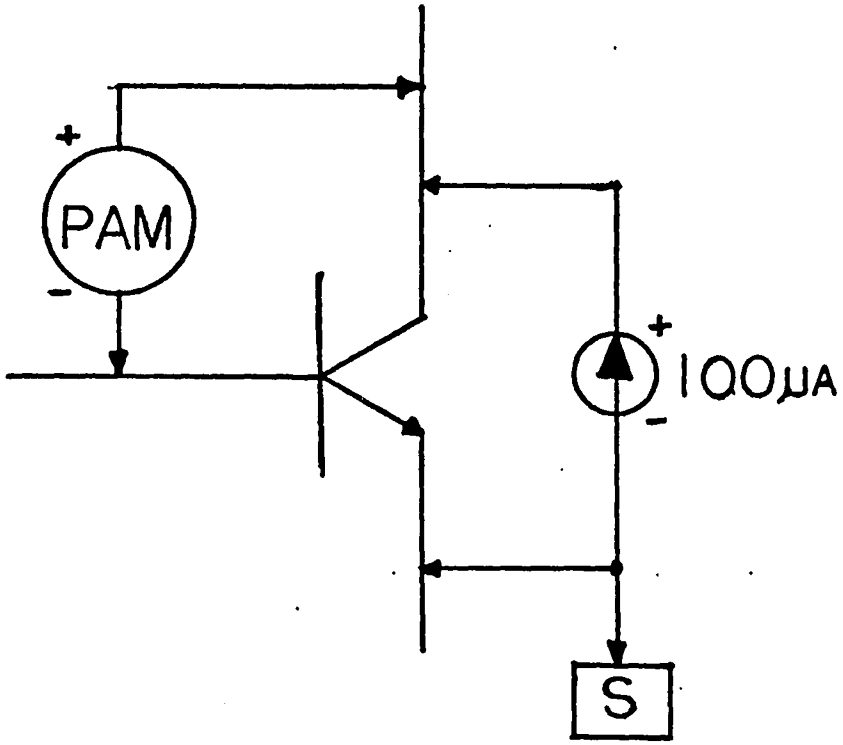


Figure 13 - β_f Forward Gain

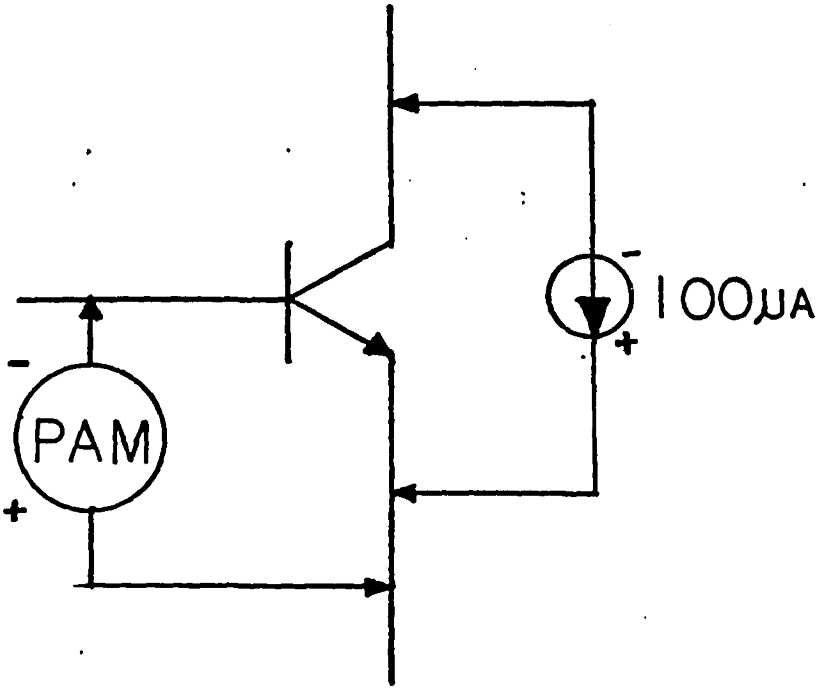
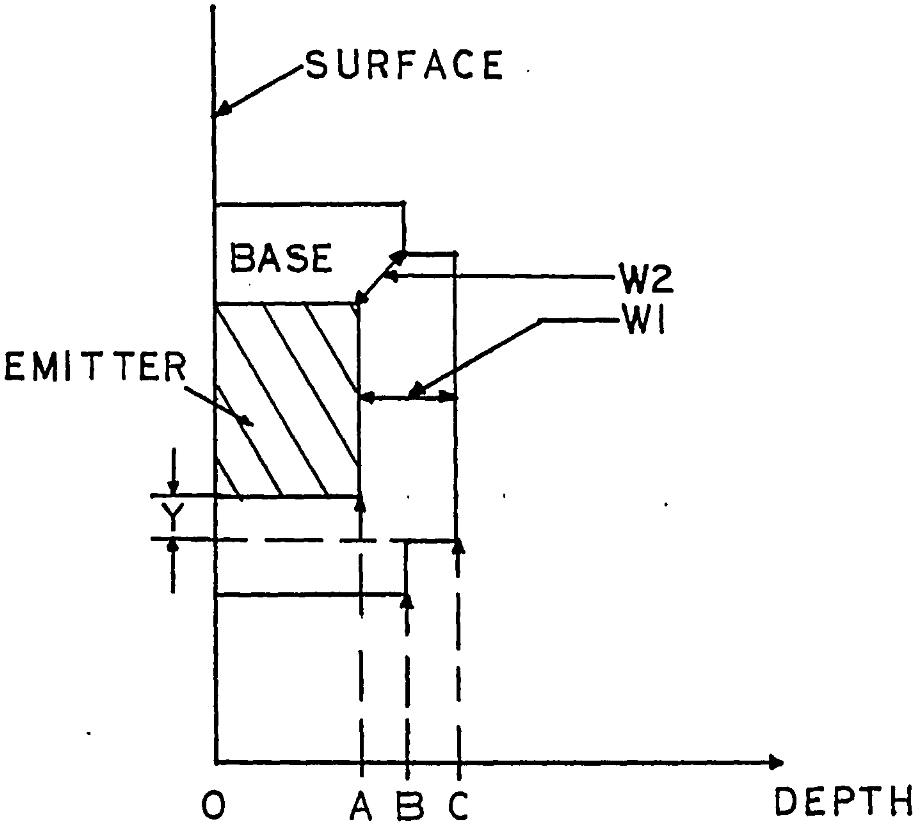
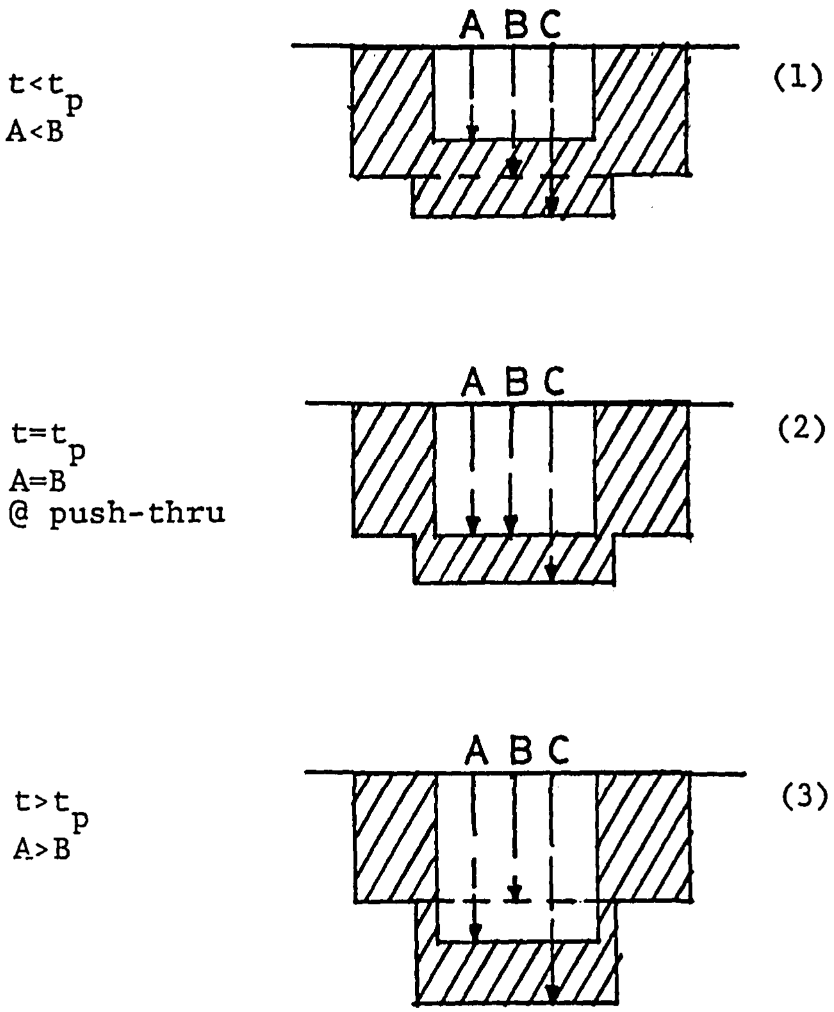


Figure 14 - β_r Reverse Gain



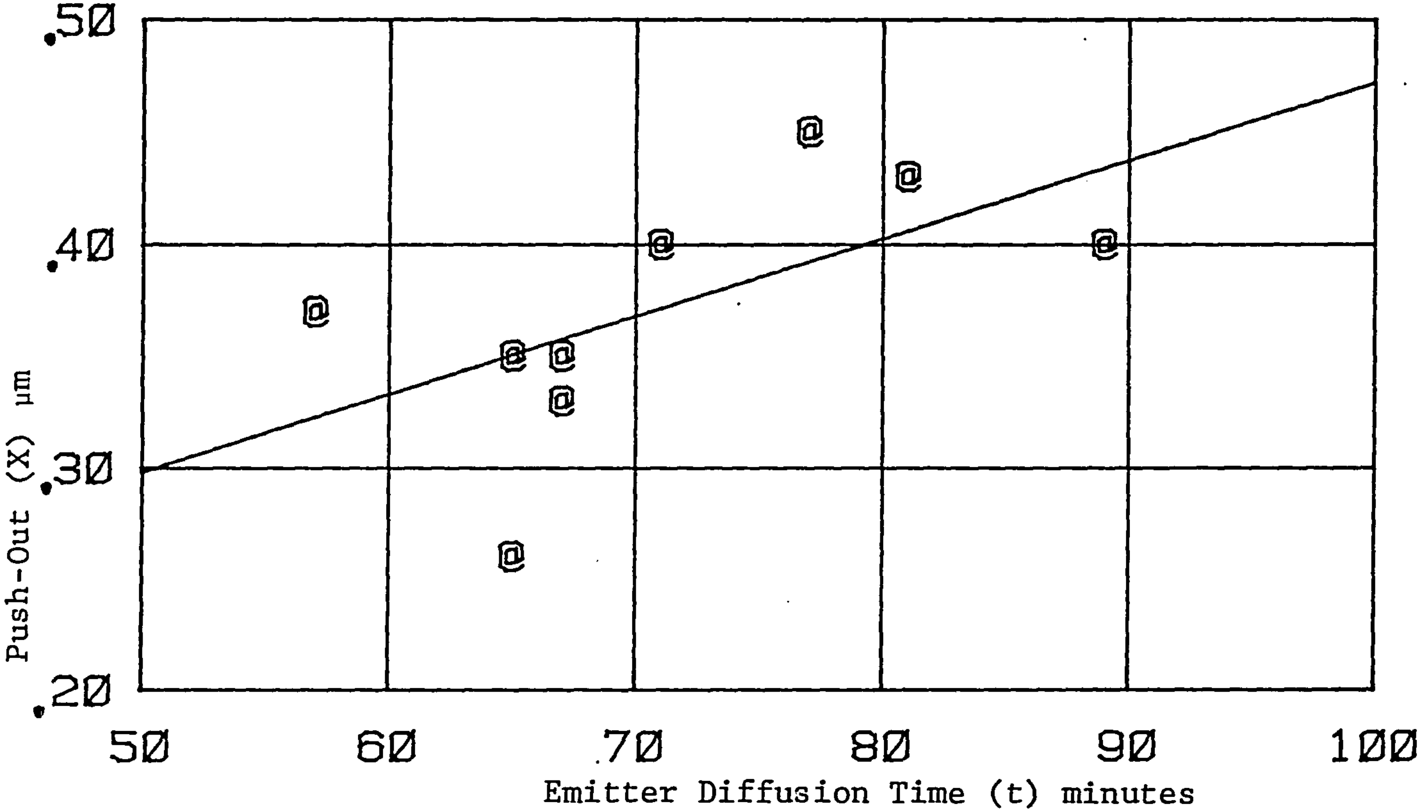
A = Emitter depth
B = Non-pushed-out base depth
C = Pushed-out base depth
W1= Base Width W1= C-A
W2= Base Width W2= $[(B-A)^2 + Y^2]^{1/2}$

Figure 15 - Description of Physical Variables



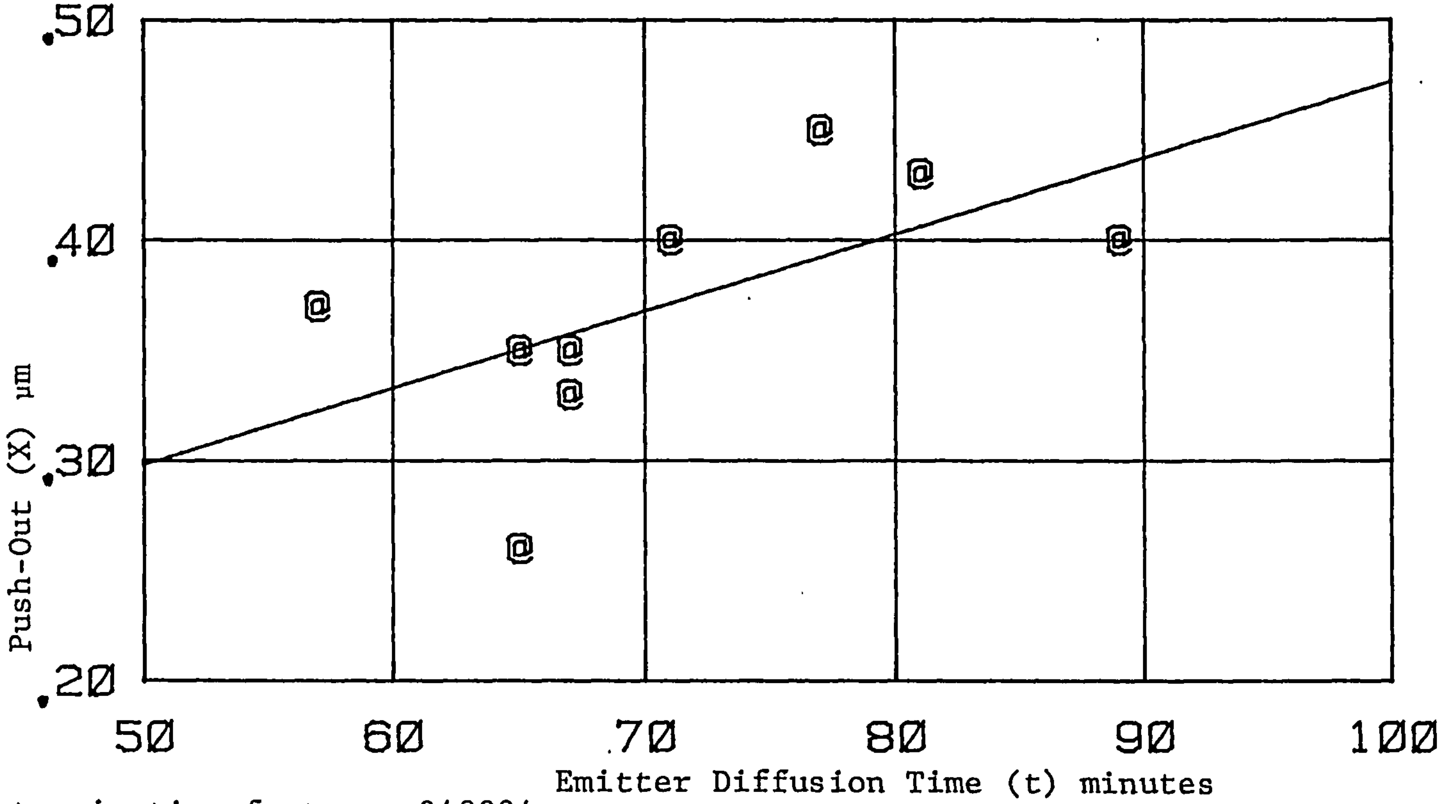
t_p = emitter diffusion time at "push-thru"
A = emitter depth
B = non-pushed-out base depth
C = pushed-out base depth

Figure 16 - Description of "Push-Thru"



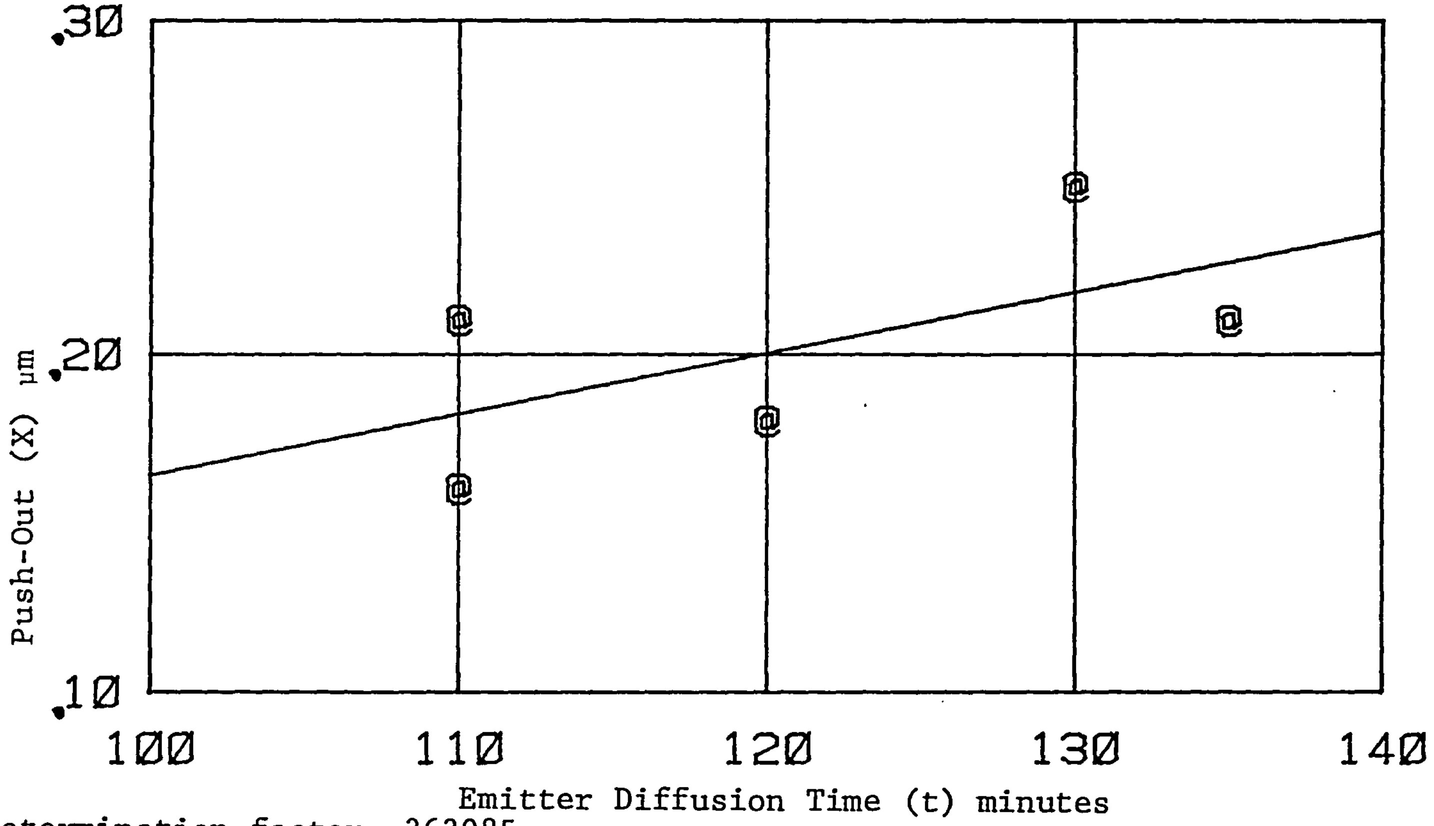
determination factor	.348824
correlation factor	.590613
standard error	4.94532

Figure 17 - Push-Out vs Emitter Diffusion Time for group 1



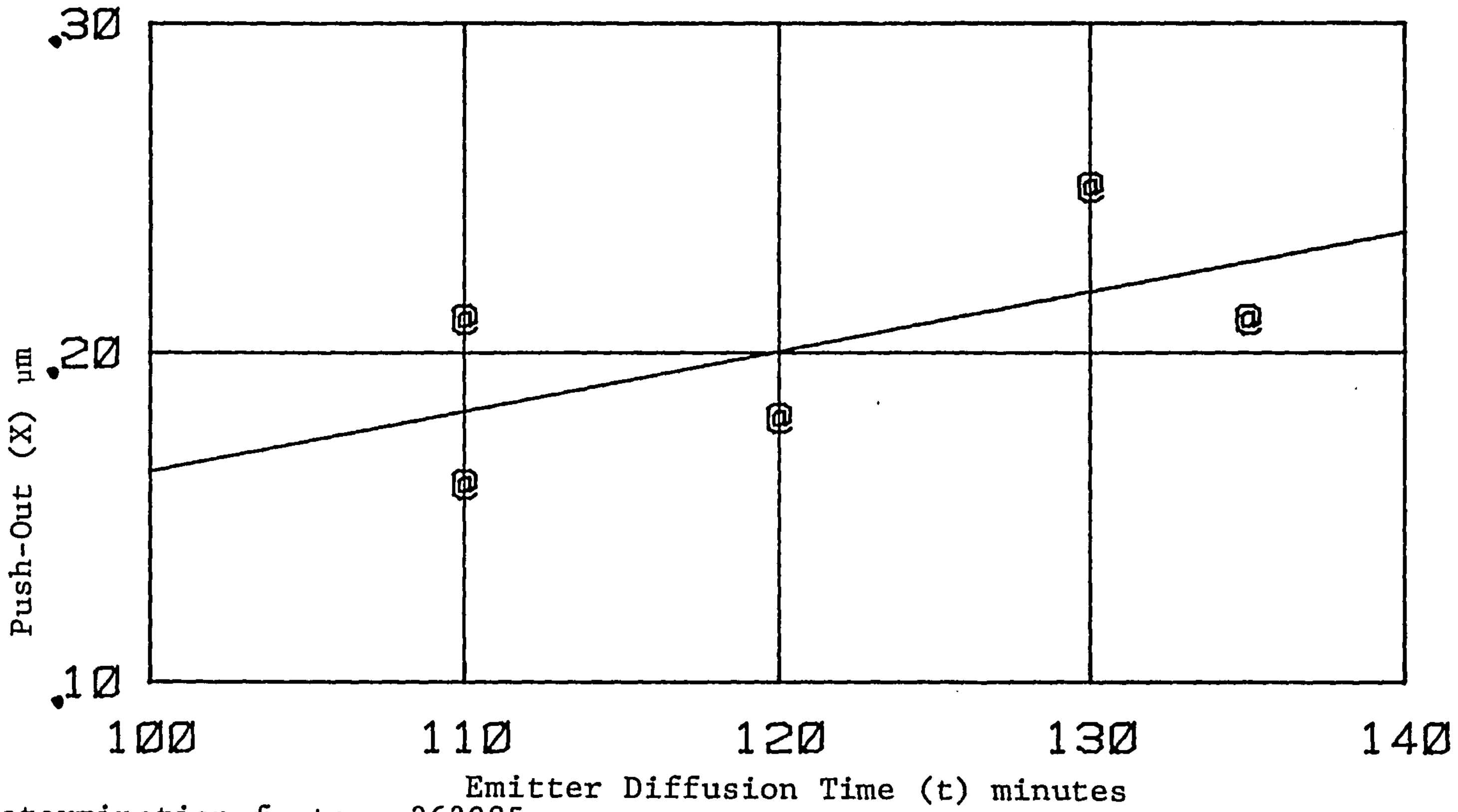
determination factor .348824
correlation factor .590613
standard error 4.94532

Figure 17 - Push-Out vs Emitter Diffusion Time for group 1



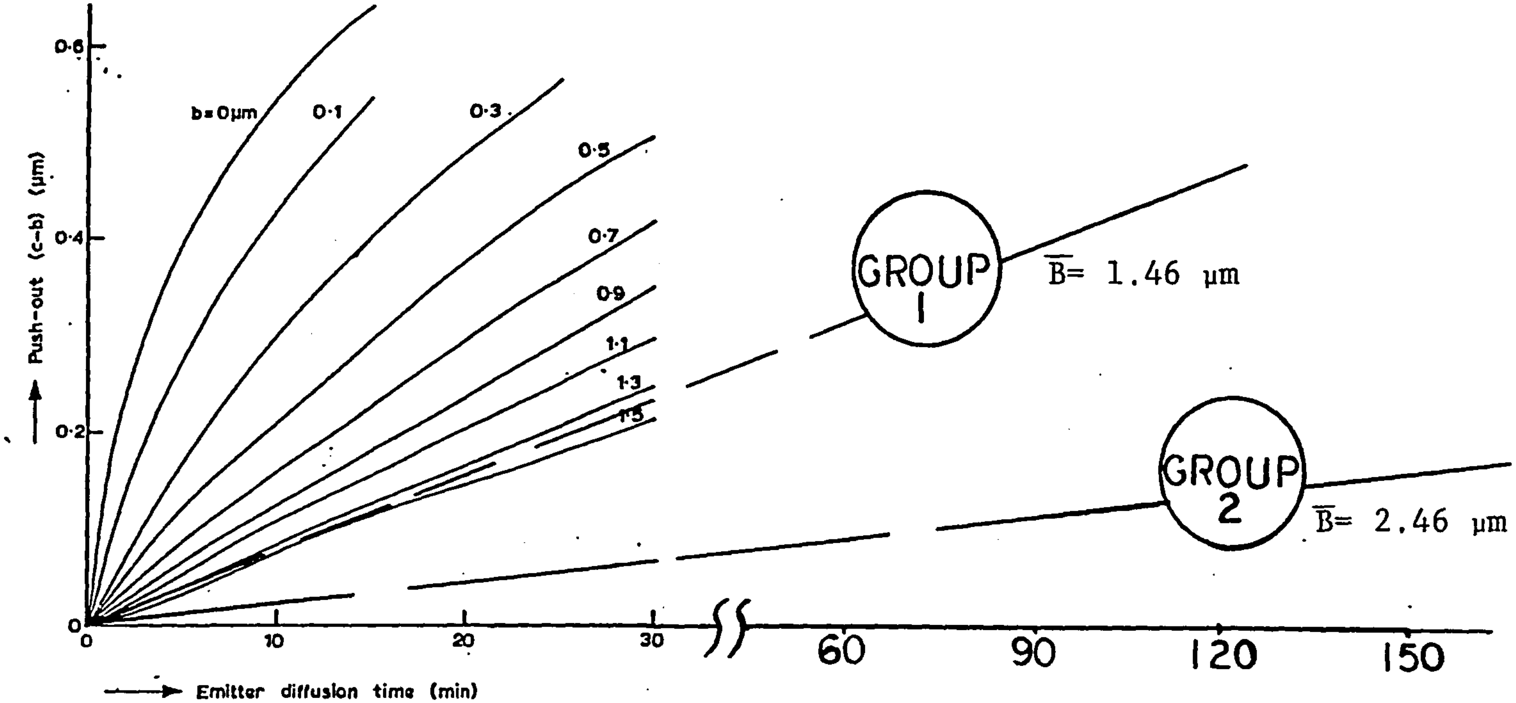
determination factor .363085
correlation factor .602565
standard error 3.15208

Figure 18 - Push-Out vs Emitter Diffusion Time for group 2



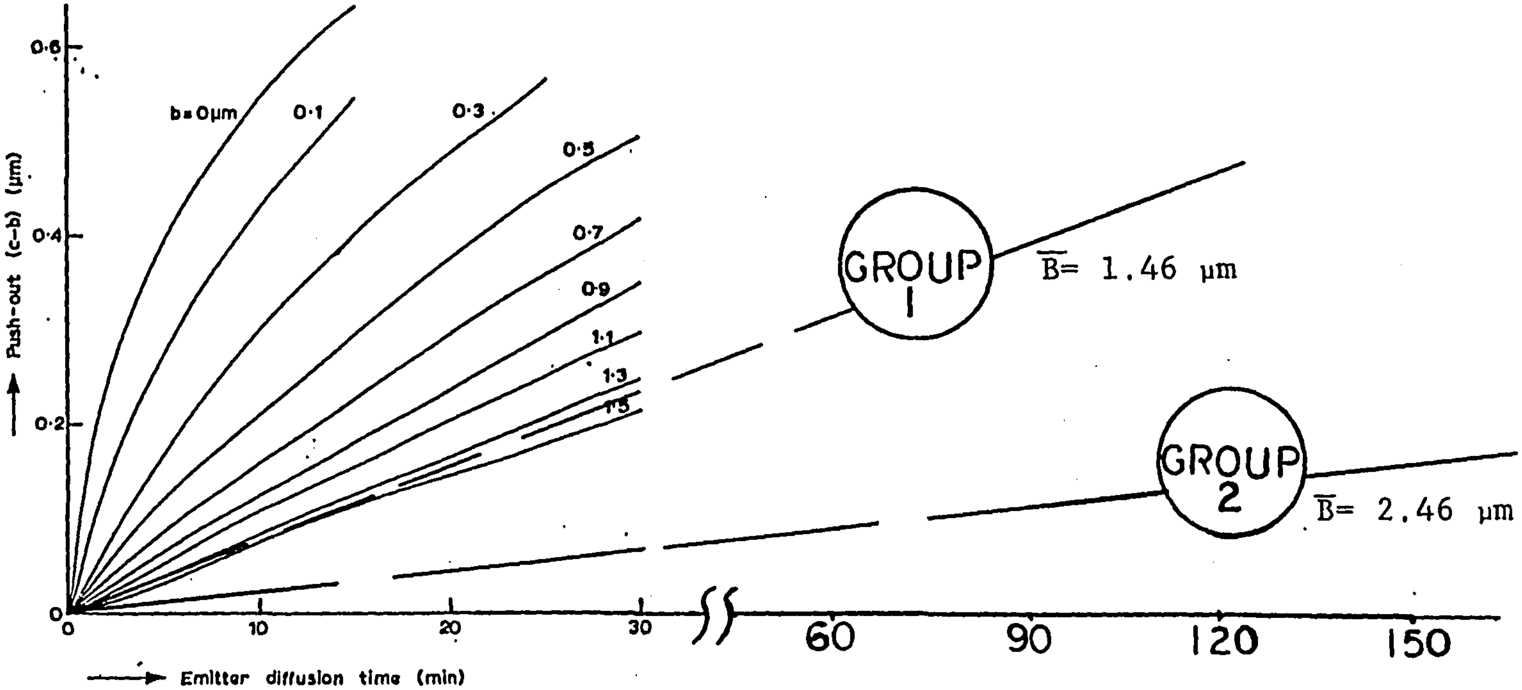
determination factor .363085
correlation factor .602565
standard error 3.15208

Figure 18 - Push-Out vs Emitter Diffusion Time for group 2



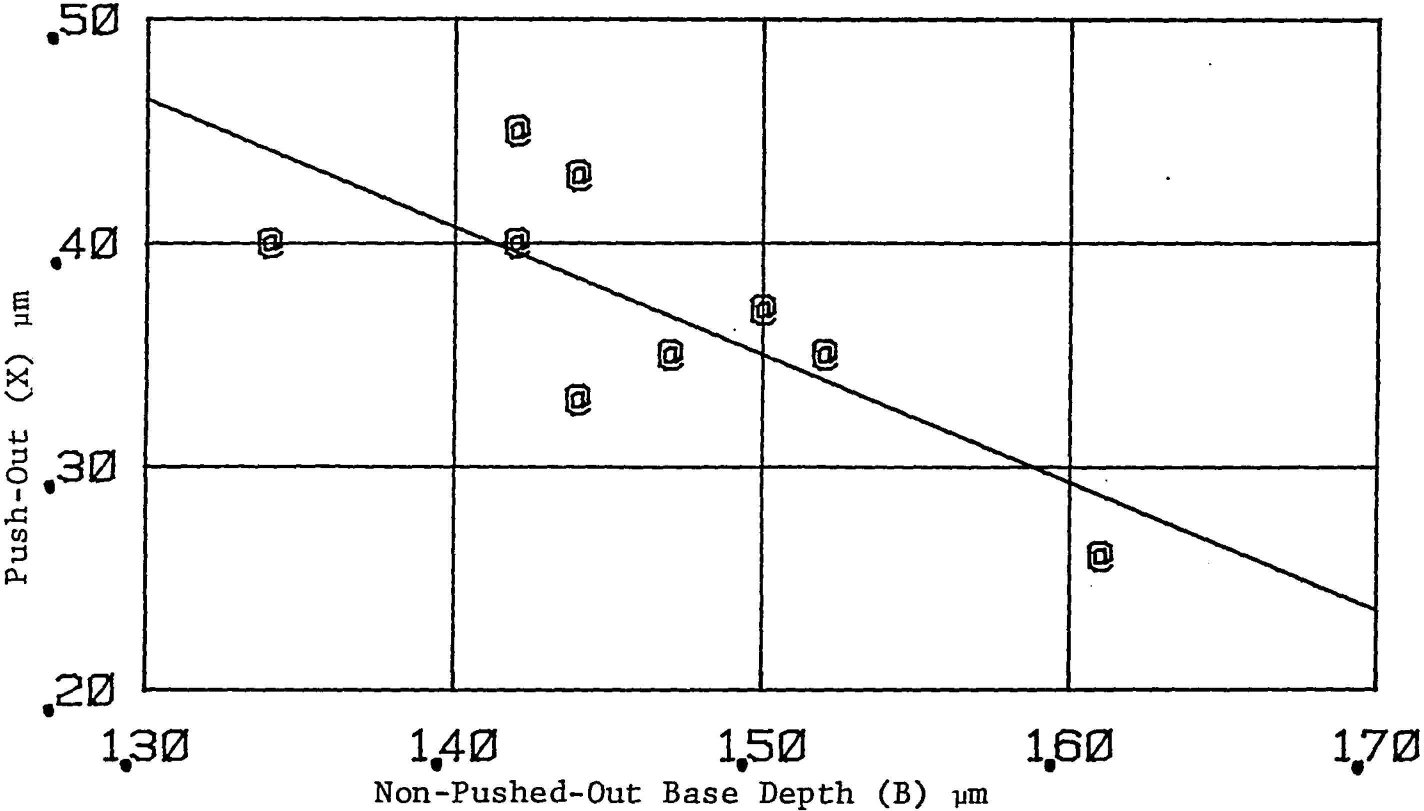
b= non-pushed-out base depth

Figure 19 - Comparison of theoretical curves against experimental data for Push-Out vs Emitter Diffusion Time (curves from Lee, "The Push-Out Effect in Silicon n-p-n Diffused Transistors", Phillips Research Laboratories, no. 5,1974)



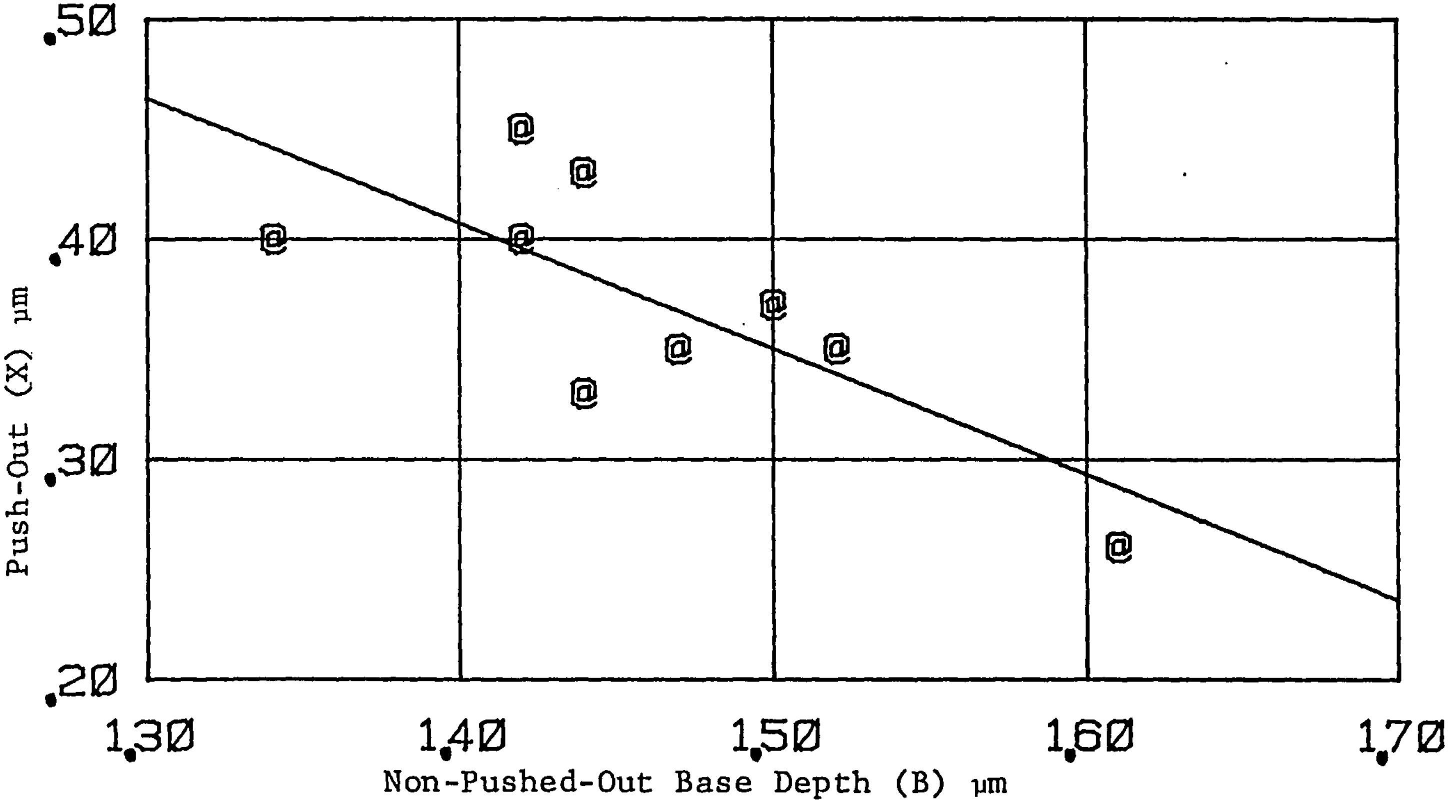
b= non-pushed-out base depth

Figure 19 - Comparison of theoretical curves against experimental data for Push-Out vs Emitter Diffusion Time (curves from Lee, "The Push-Out Effect in Silicon n-p-n Diffused Transistors", Phillips Research Laboratories, no. 5,1974)



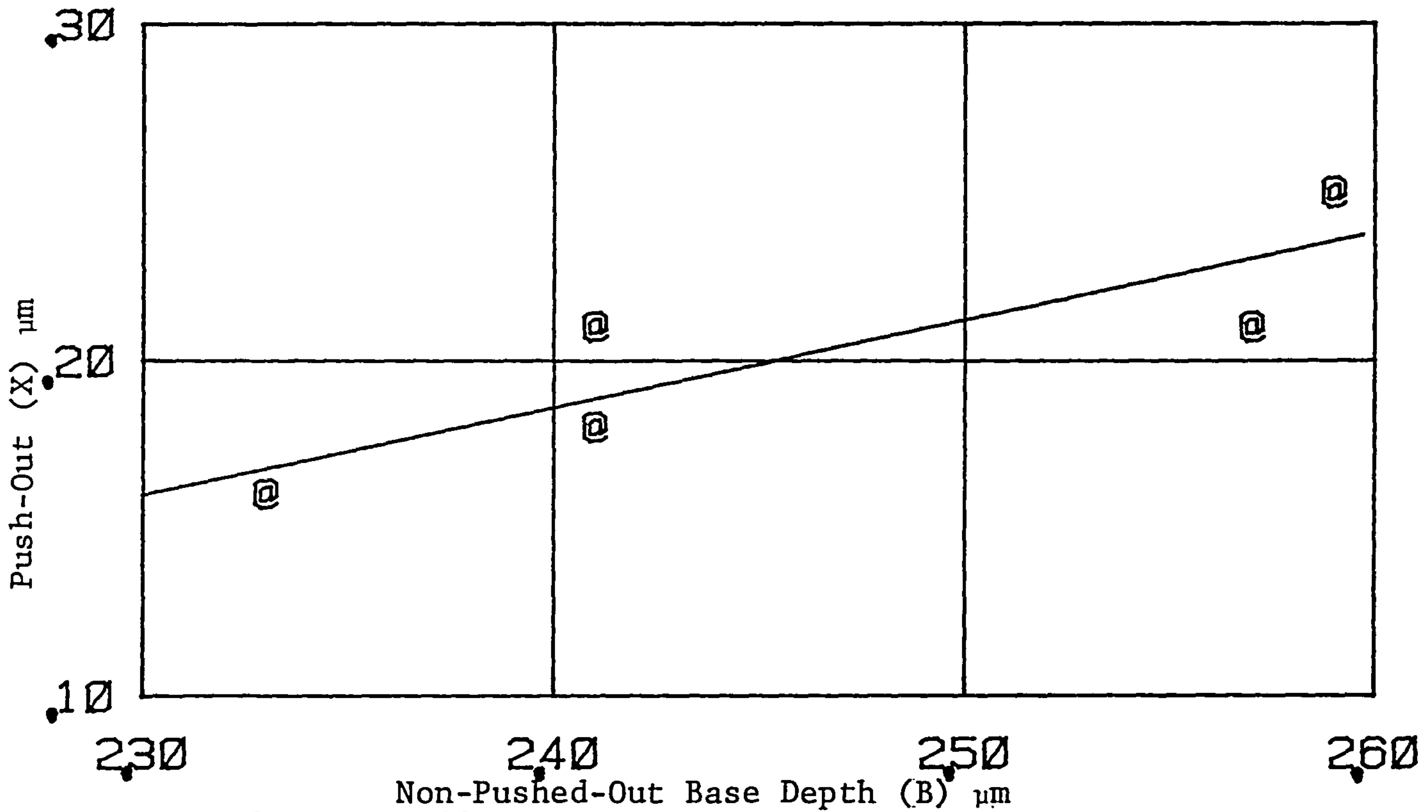
determination factor	.571152
correlation factor	.755746
standard error	4.01326

Figure 20 - Push-Out vs Non-Pushed-Out Base Depth for group 1



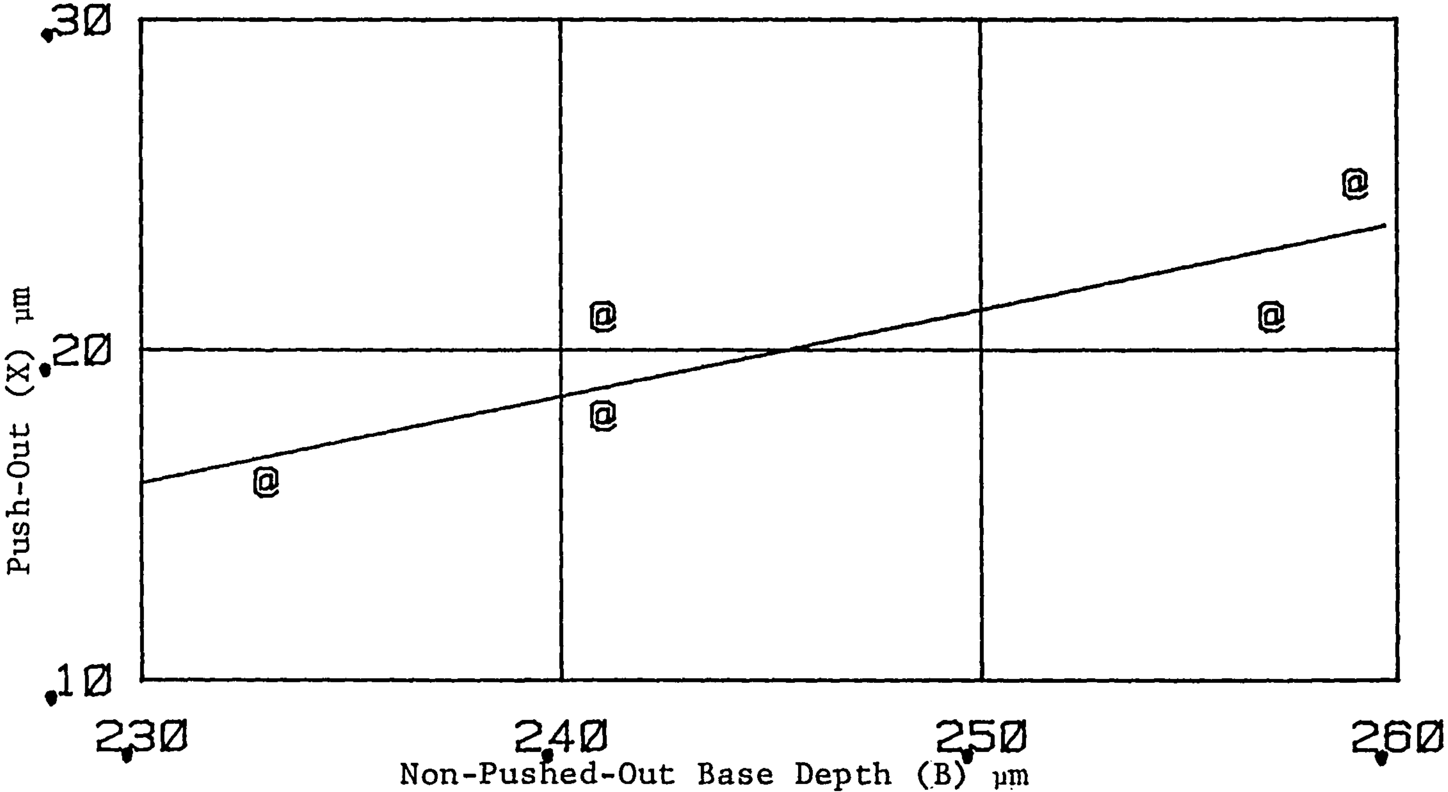
determination factor .571152
correlation factor .755746
standard error 4.01326

Figure 20 - Push-Out vs Non-Pushed-Out Base Depth for group 1



```
determination factor  .740767
correlation factor    .860679
standard error       2.01095
```

Figure 21 - Push-Out vs Non-Pushed-Out Base Depth for group 2



determination factor .740767
correlation factor .860679
standard error 2.01095

Figure 21 - Push-Out vs Non-Pushed-Out Base Depth for group 2

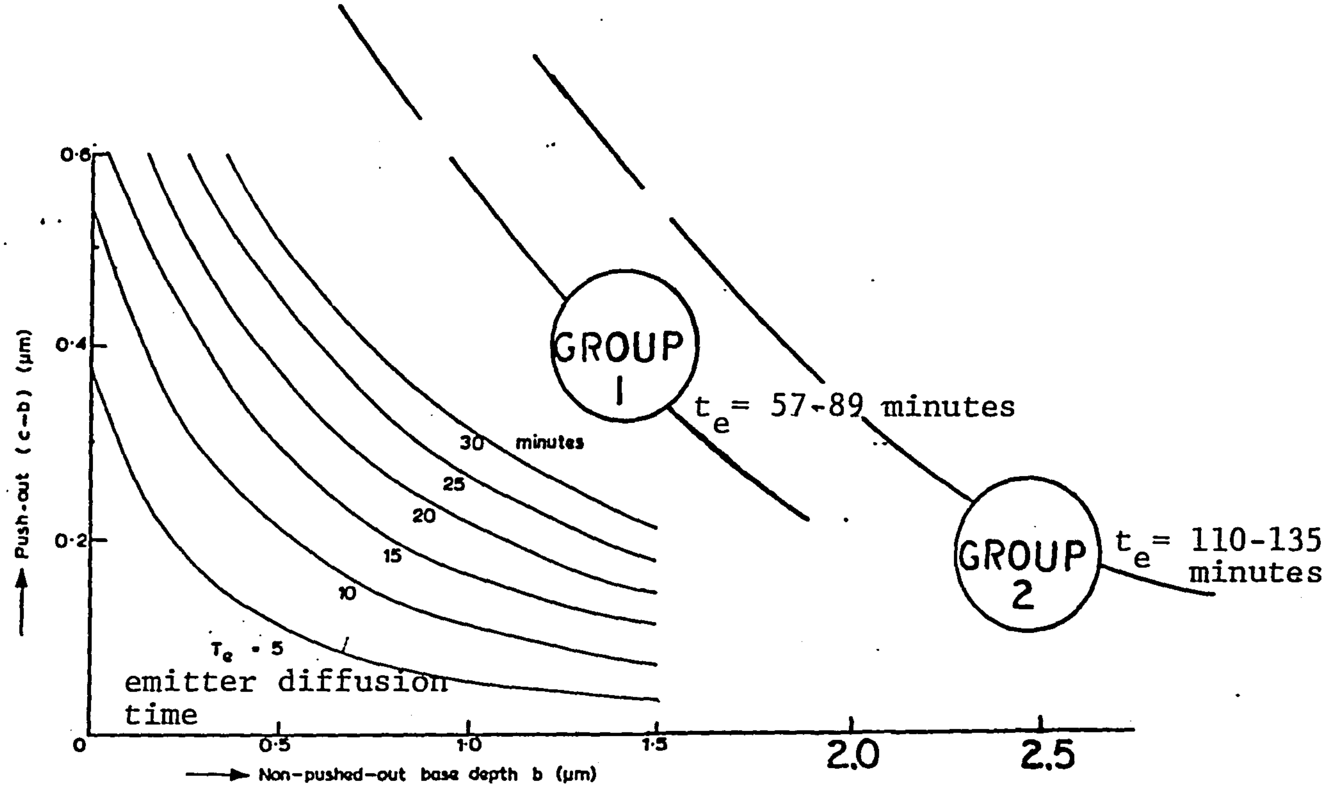


Figure 22 - Comparison of theoretical curves against experimental data for Push-Out vs Non-Pushed-Out Base Depth (curves from Lee, "The Push-Out Effect in Silicon n-p-n Transistors", Phillips Research Laboratories, no. 5,1974)

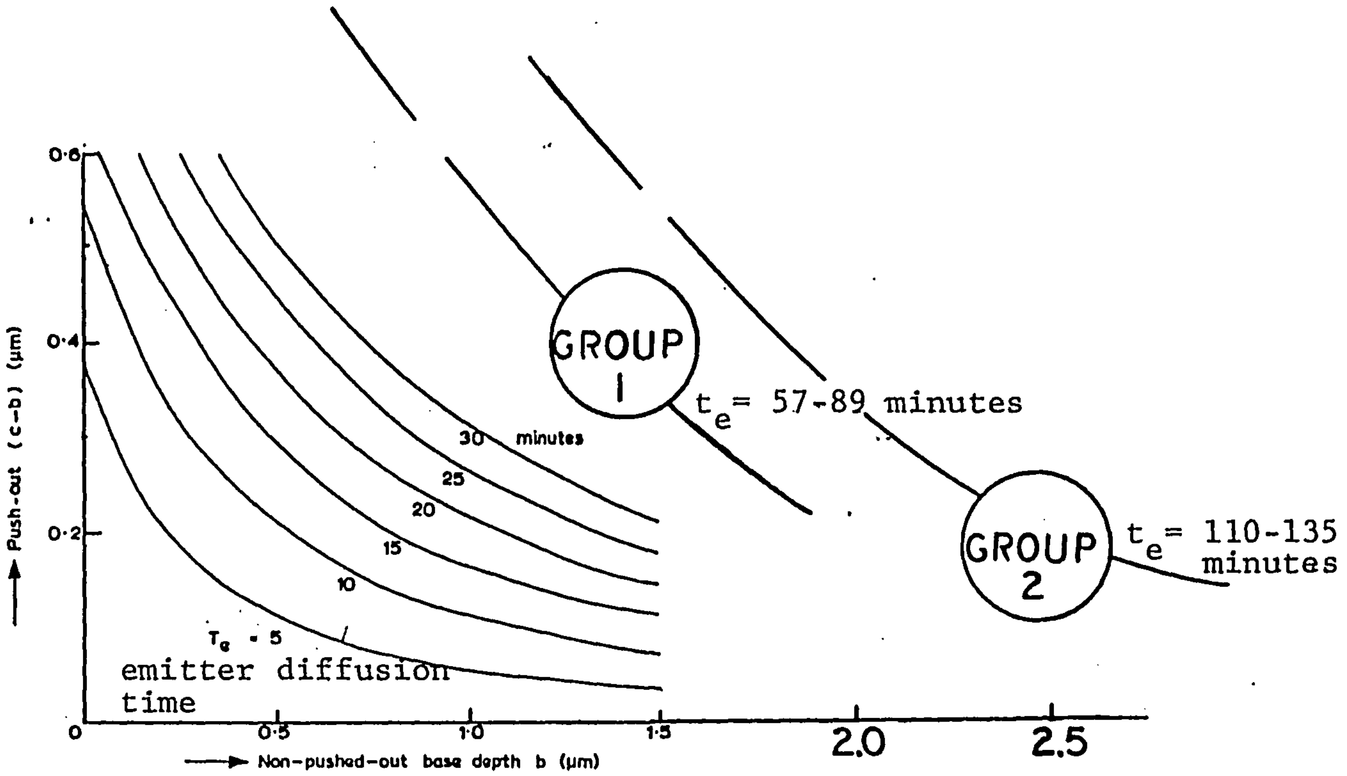
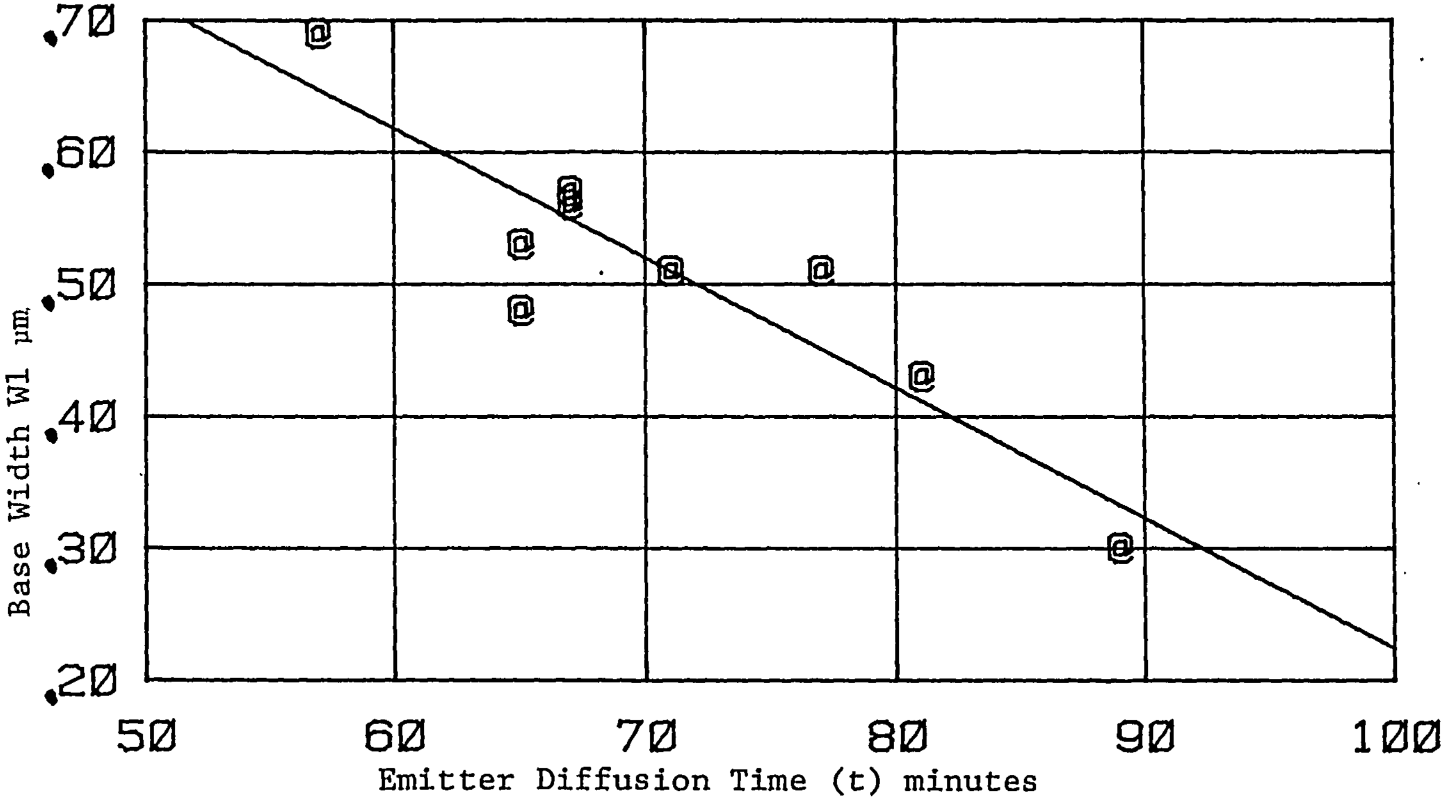
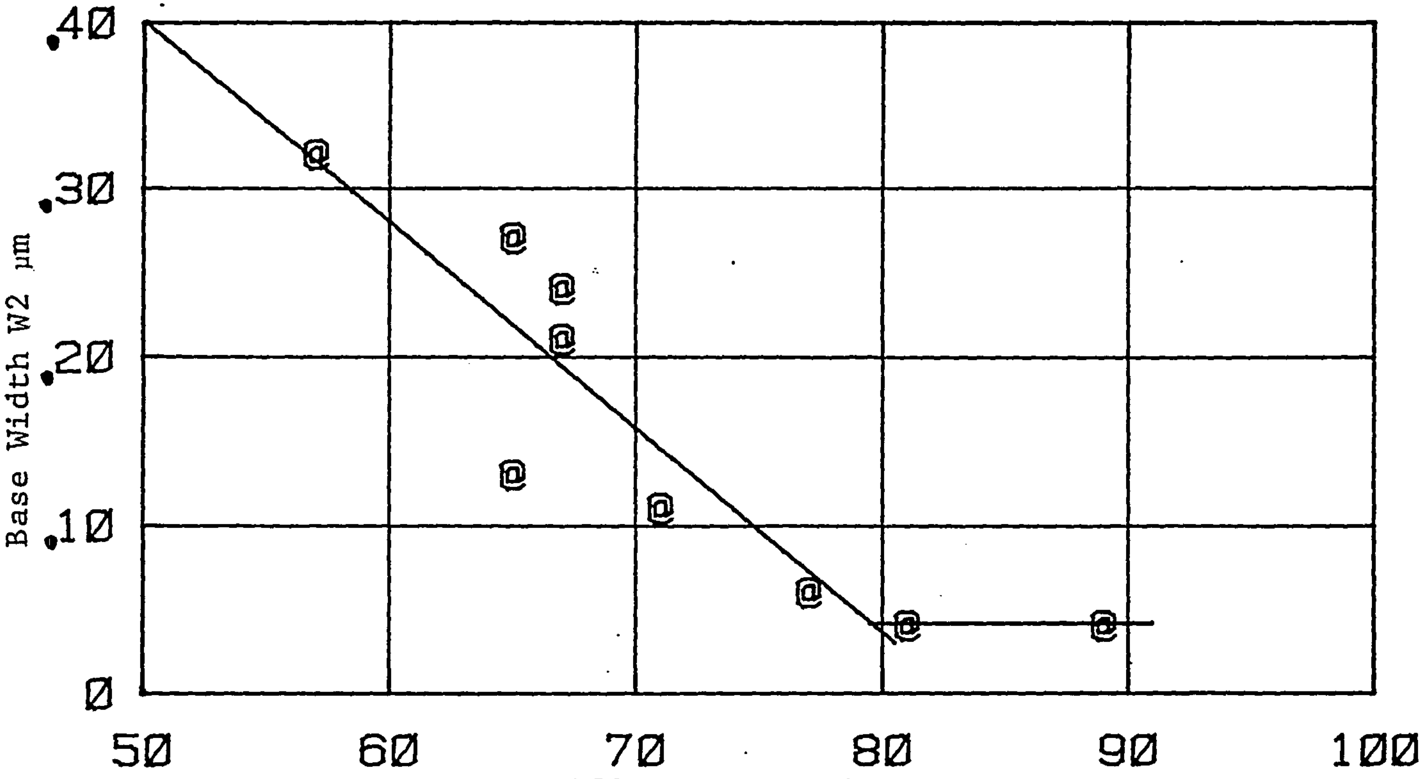


Figure 22 - Comparison of theoretical curves against experimental data for Push-Out vs Non-Pushed-Out Base Depth (curves from Lee, "The Push-Out Effect in Silicon n-p-n Transistors", Phillips Research Laboratories, no. 5,1974)



determination factor .815366
correlation factor .902976
standard error 4.88006

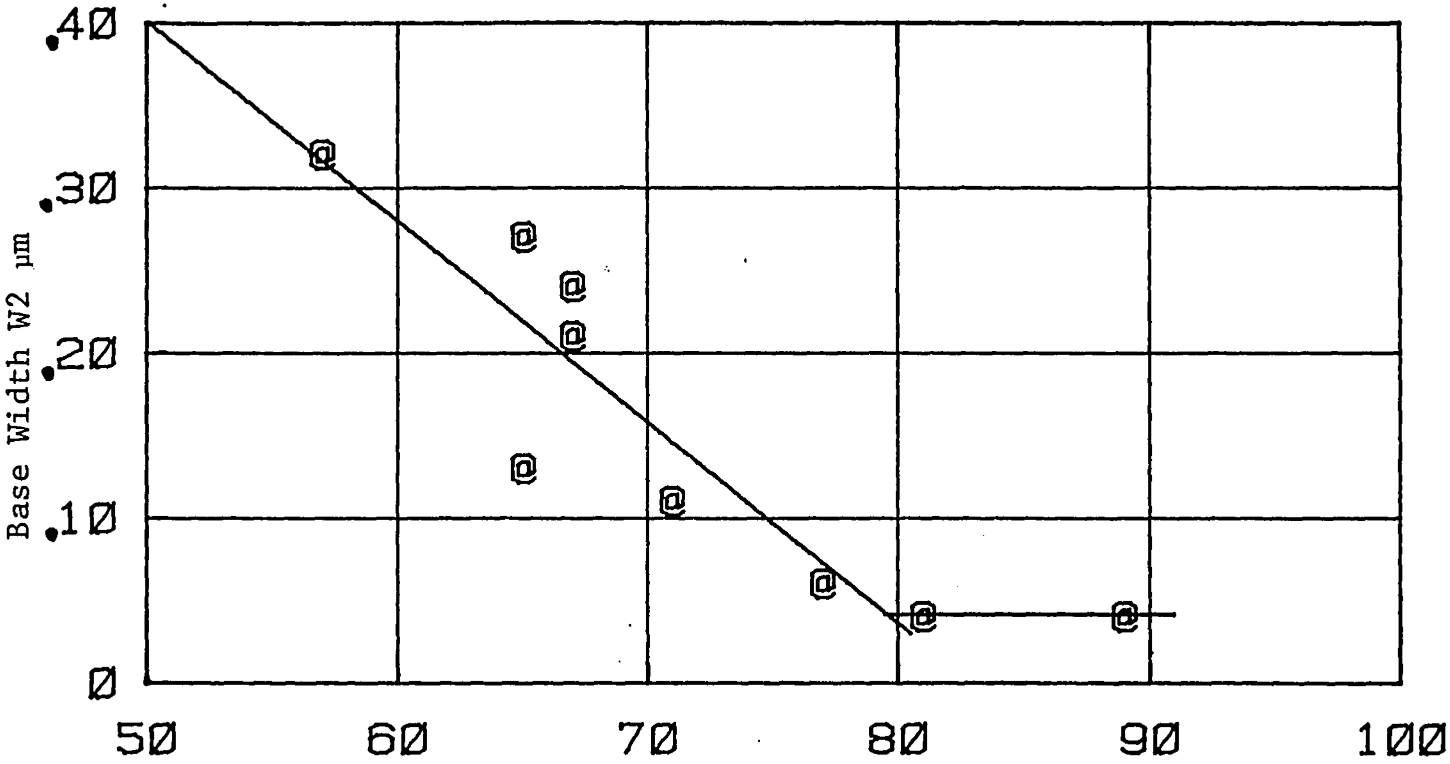
Figure 23 - Base Width W1 vs Emitter Diffusion Time for group 1



Emitter Diffusion Time (t) minutes

determination factor .801358
correlation factor .895186
standard error 4.92116

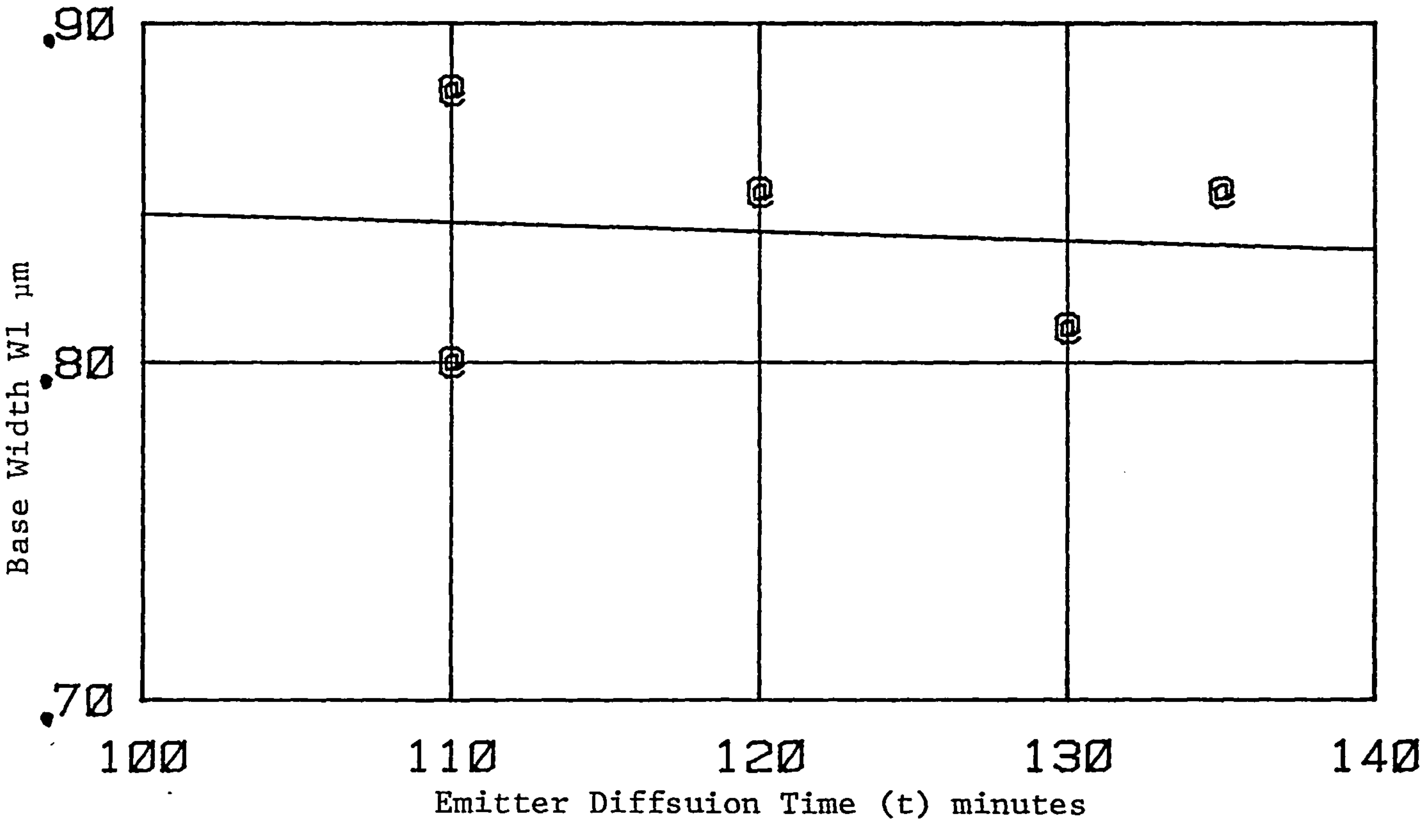
Figure 24 - Base Width W2 vs Emitter Diffusion Time for group 1



Emitter Diffusion Time (t) minutes

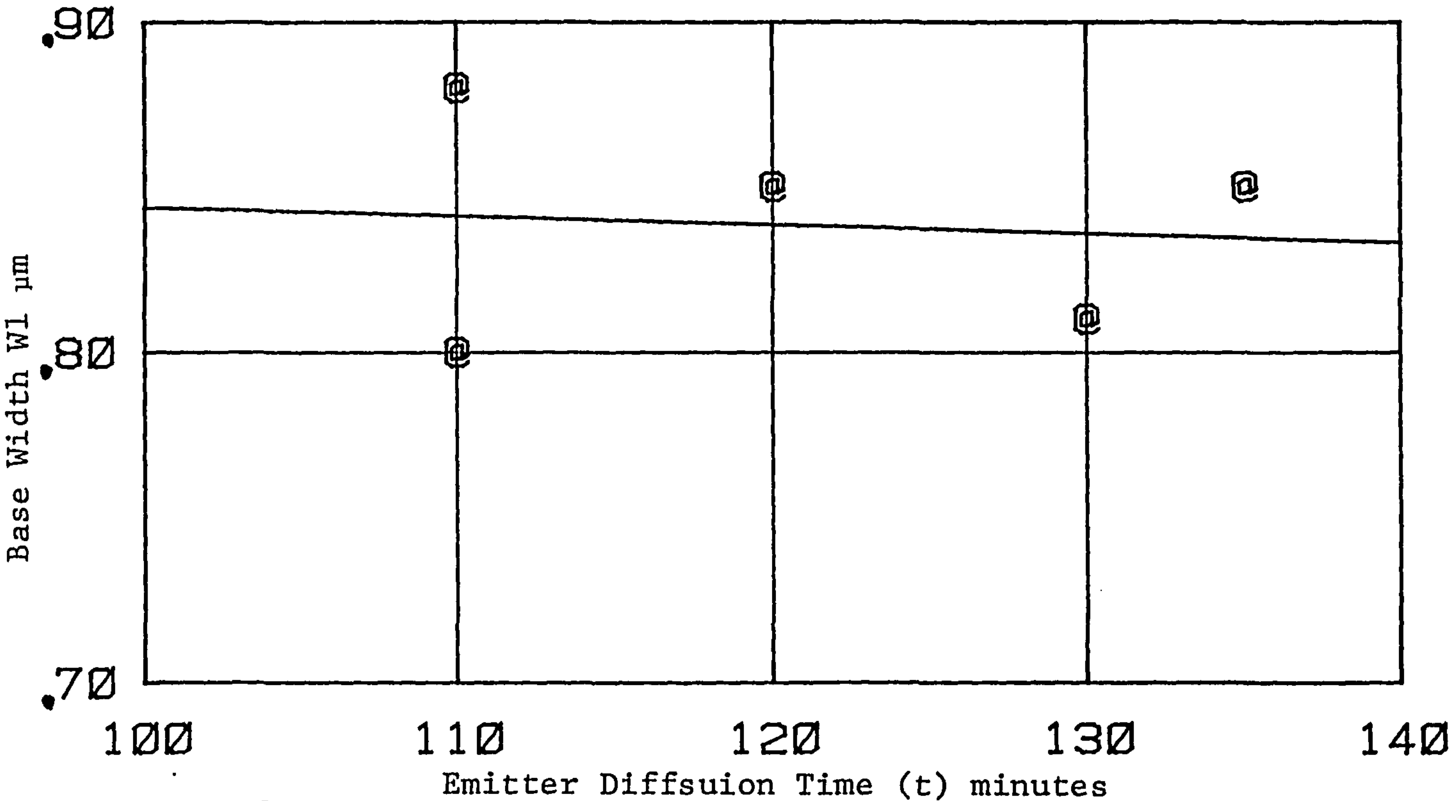
```
determination factor  .801358
correlation factor    .895186
standard error       4.92116
```

Figure 24 - Base Width W2 vs Emitter Diffusion Time for group 1



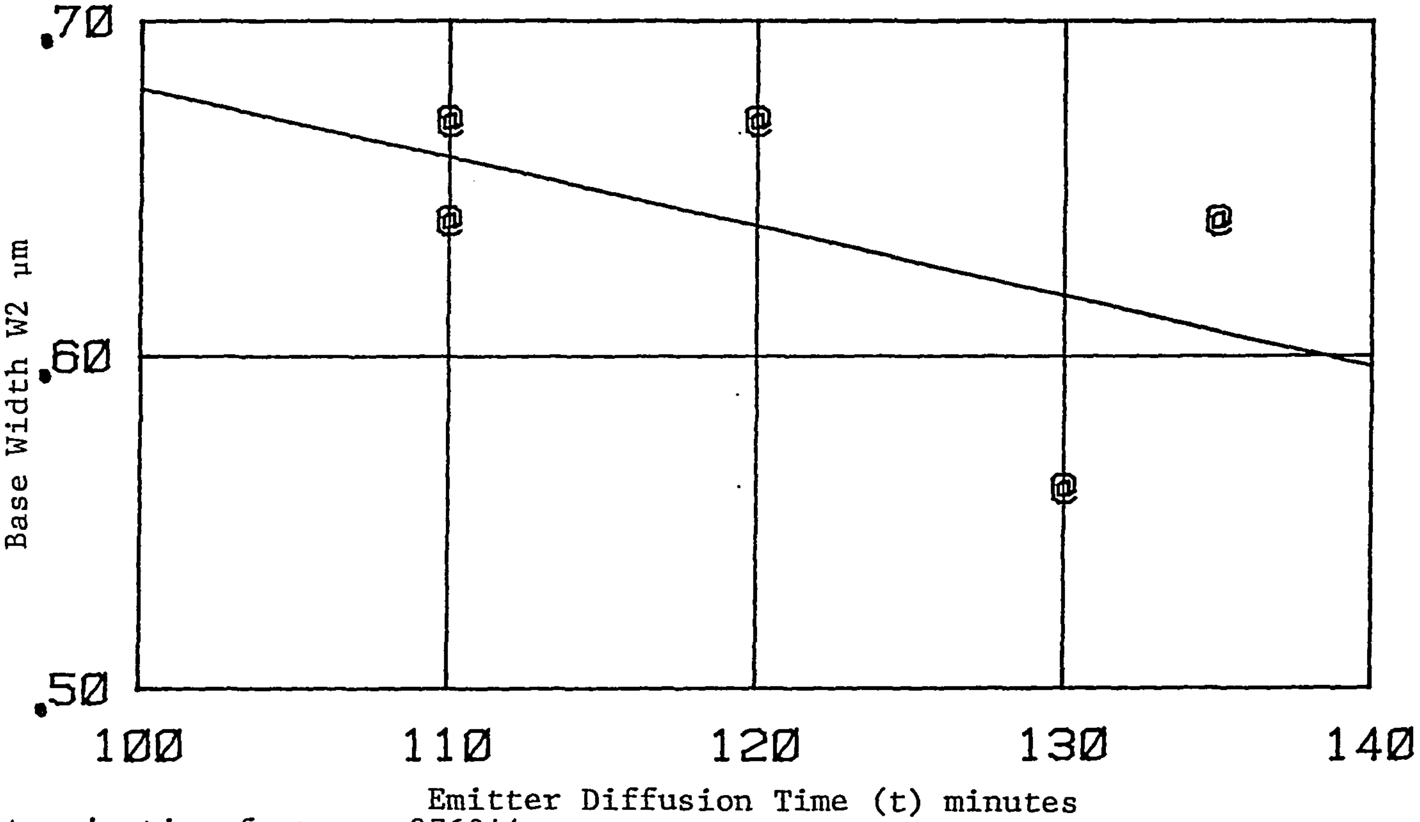
determination factor	.008814
correlation factor	.093884
standard error	3.75876

Figure 25 - Base Width W1 vs Emitter Diffusion Time for group 2



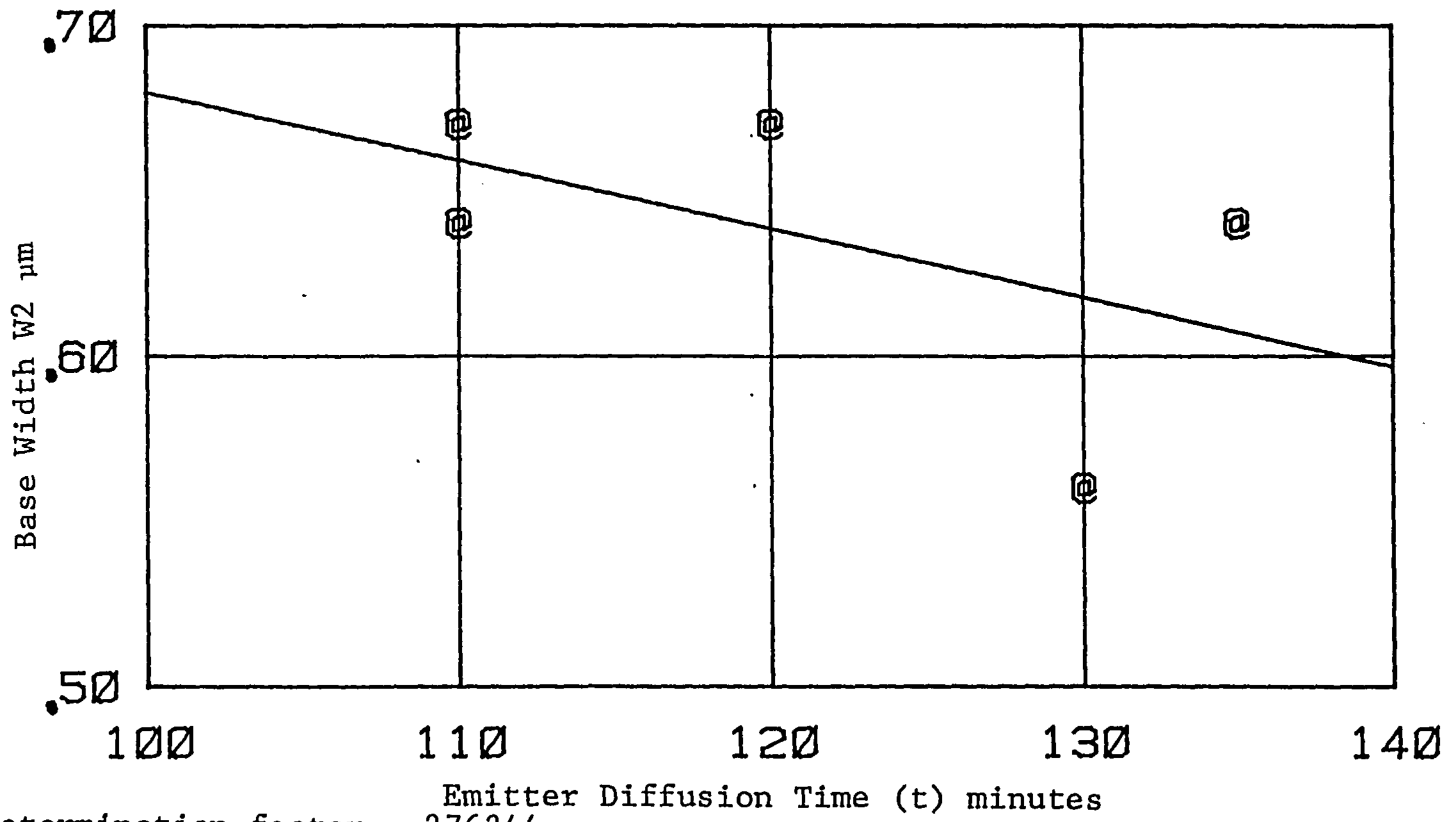
determination factor .008814
correlation factor .093884
standard error 3,75876

Figure 25 - Base Width W1 vs Emitter Diffusion Time for group 2



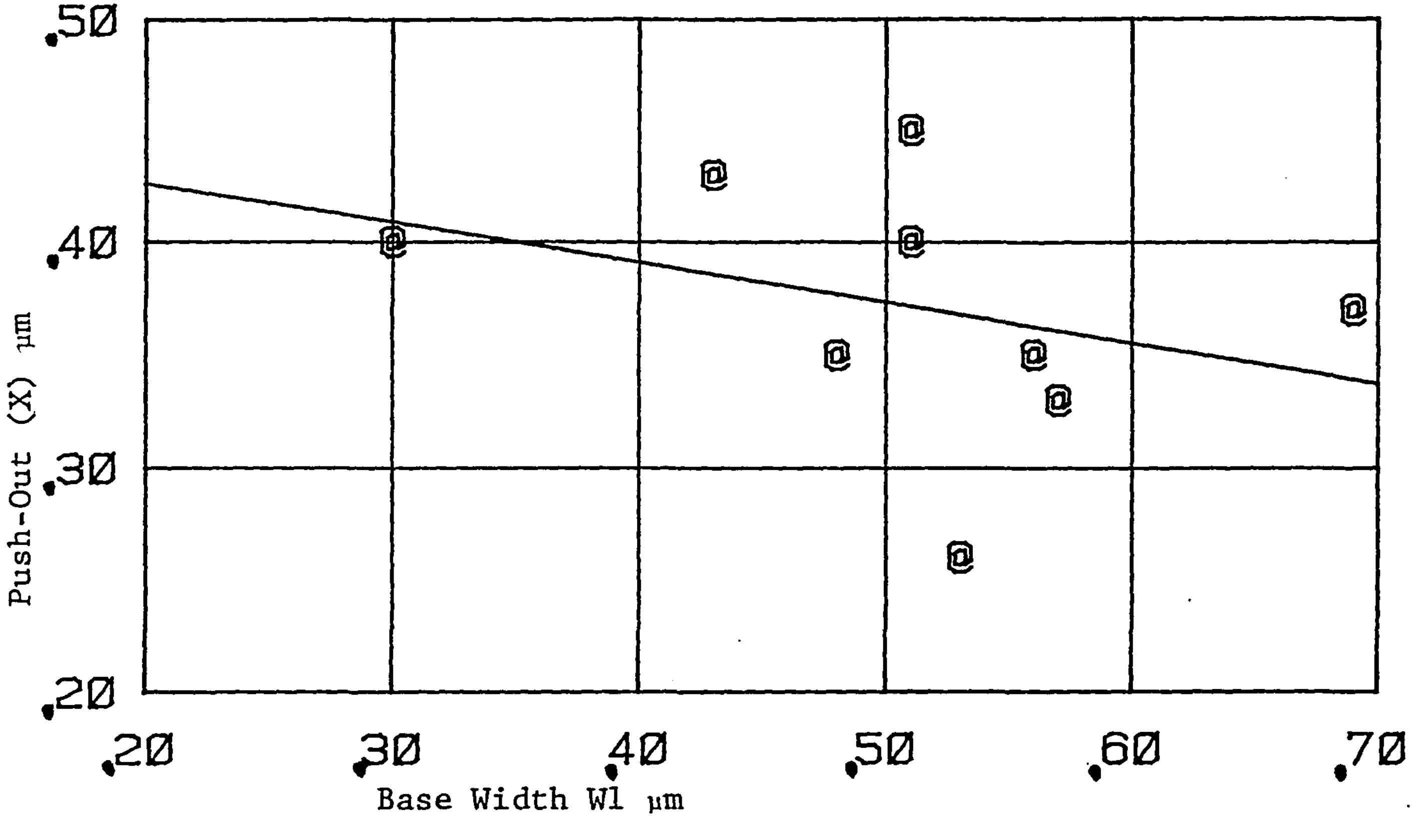
determination factor .276244
correlation factor .525589
standard error 4.42595

Figure 26 - Base Width W2 vs Emitter Diffusion Time for group 2



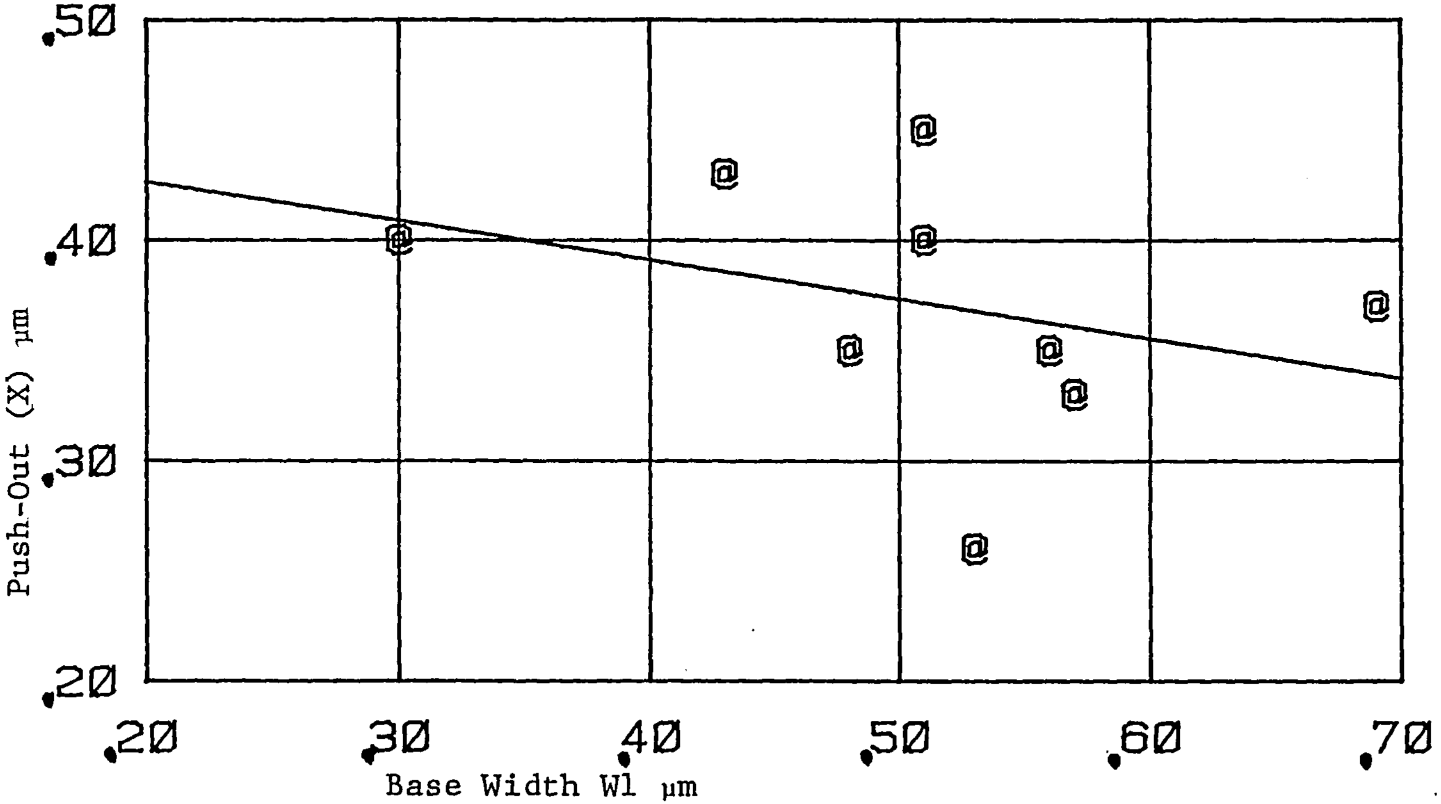
determination factor .276244
correlation factor .525589
standard error 4.42595

Figure 26 - Base Width W2 vs Emitter Diffusion Time for group 2



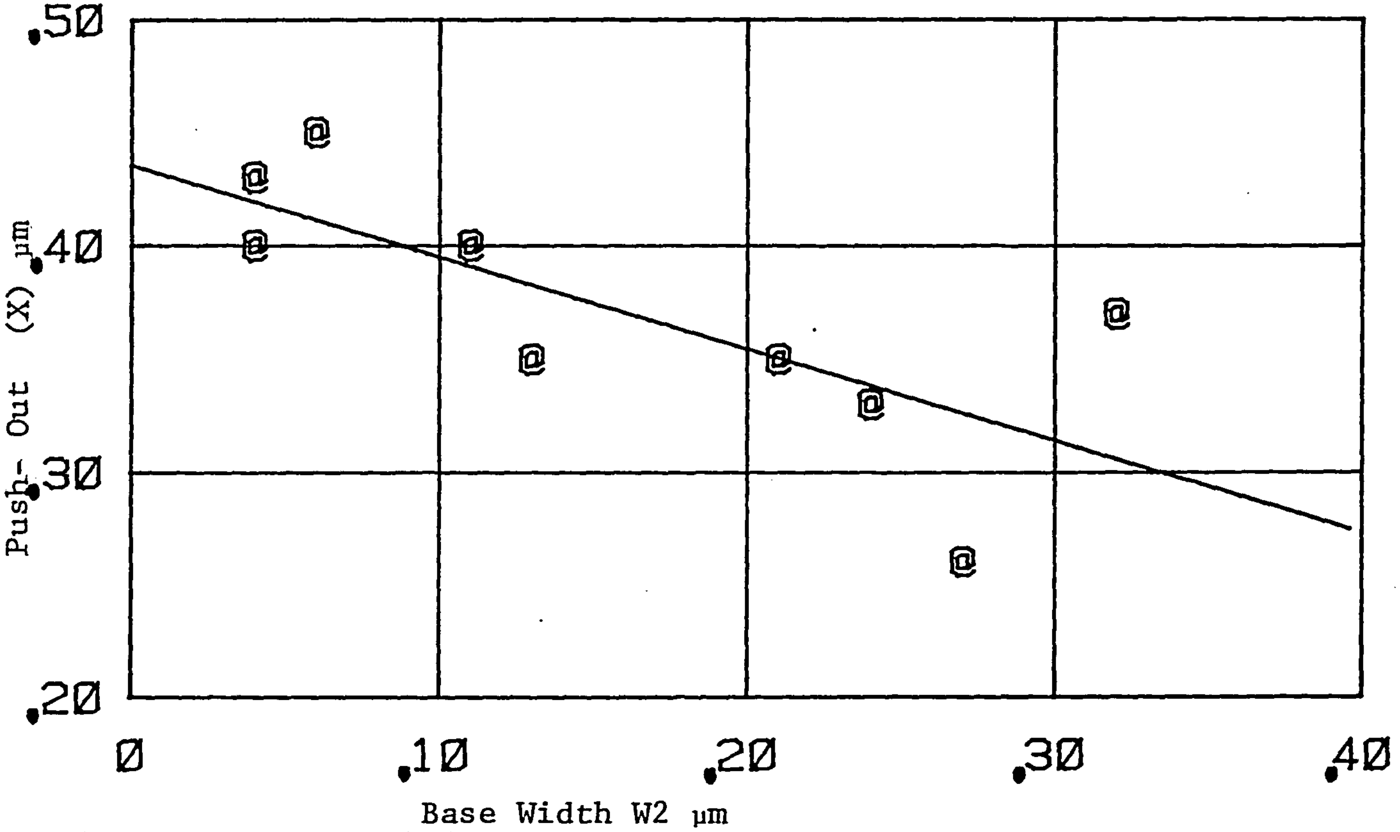
determination factor .10905
correlation factor .330229
standard error 5.78458

Figure 27 - Push-Out vs Base Width W1 for group 1



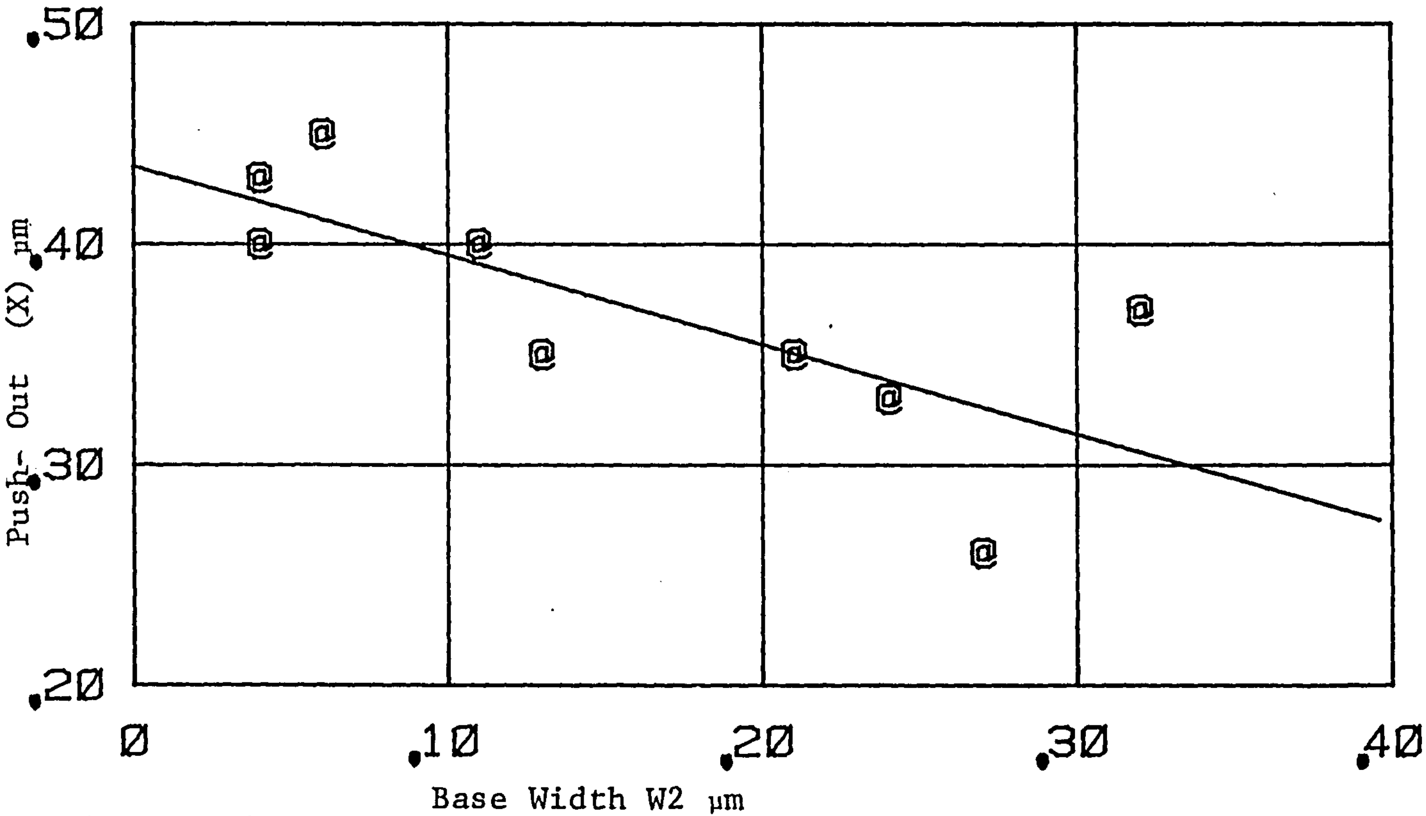
determination factor	.10905
correlation factor	.330229
standard error	5.78458

Figure 27 - Push-Out vs Base Width Wl for group 1



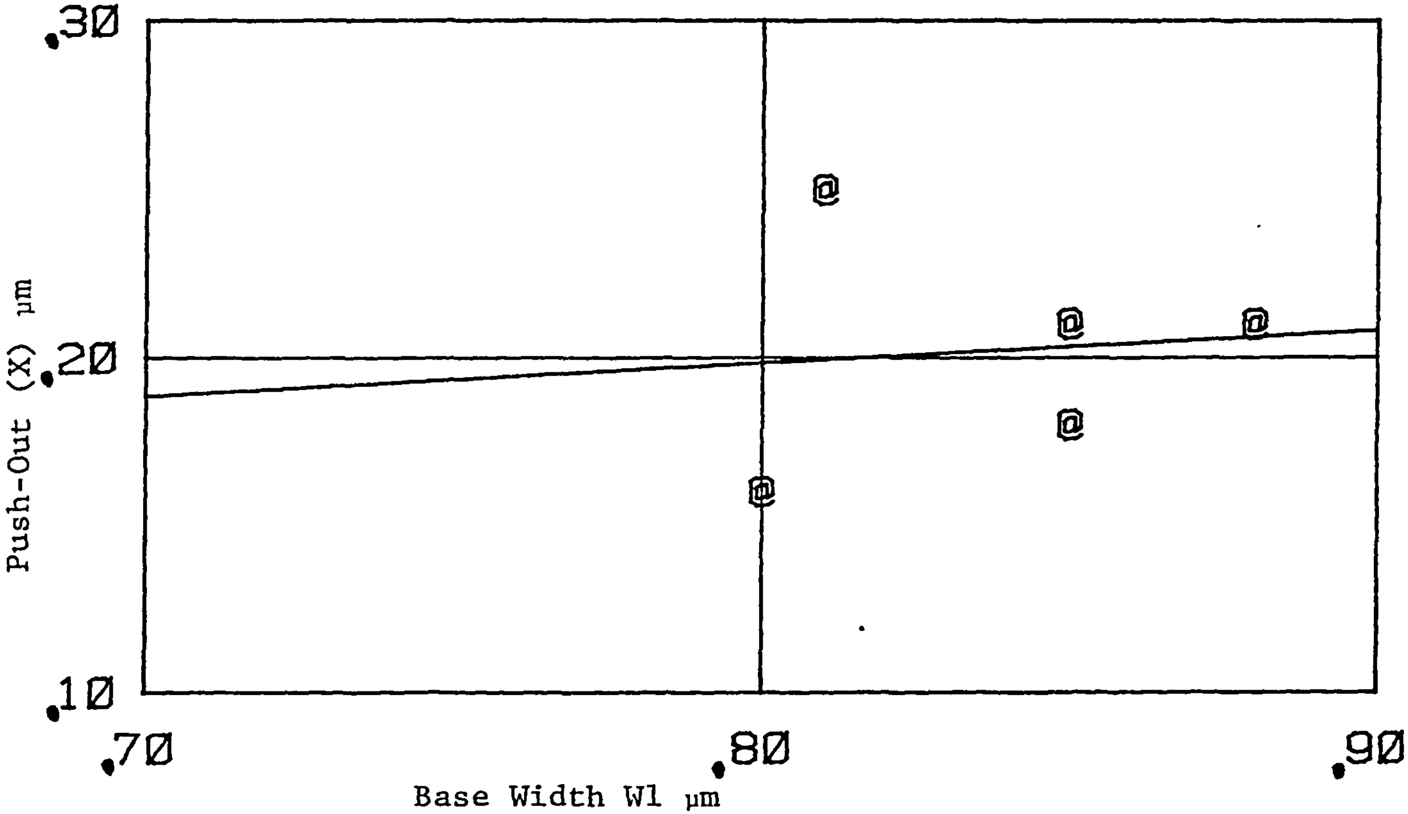
determination factor	.554734
correlation factor	.744805
standard error	4.08935

Figure 28 - Push-Out vs Base Width W2 for group 1



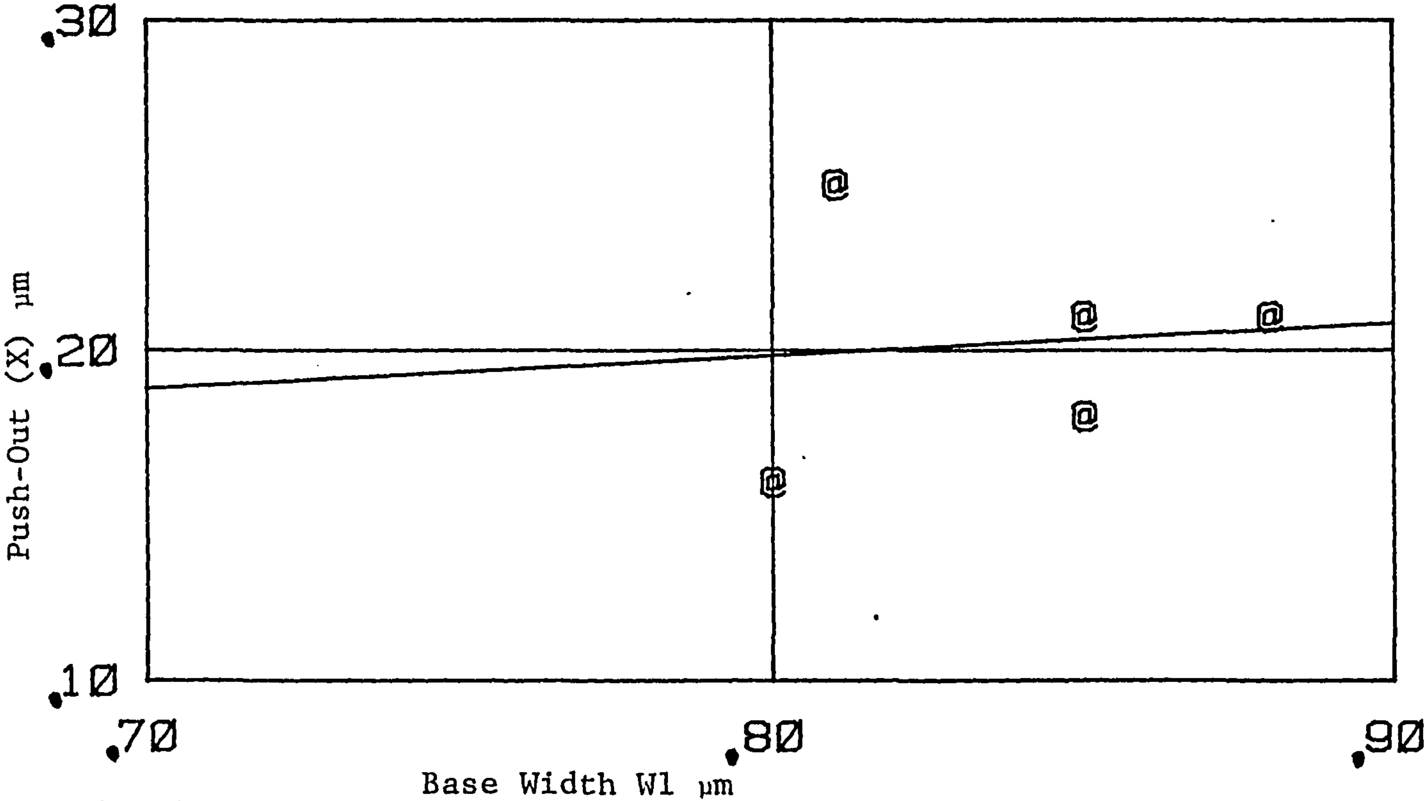
determination factor .554734
correlation factor .744805
standard error 4.08935

Figure 28 - Push-Out vs Base Width W2 for group 1



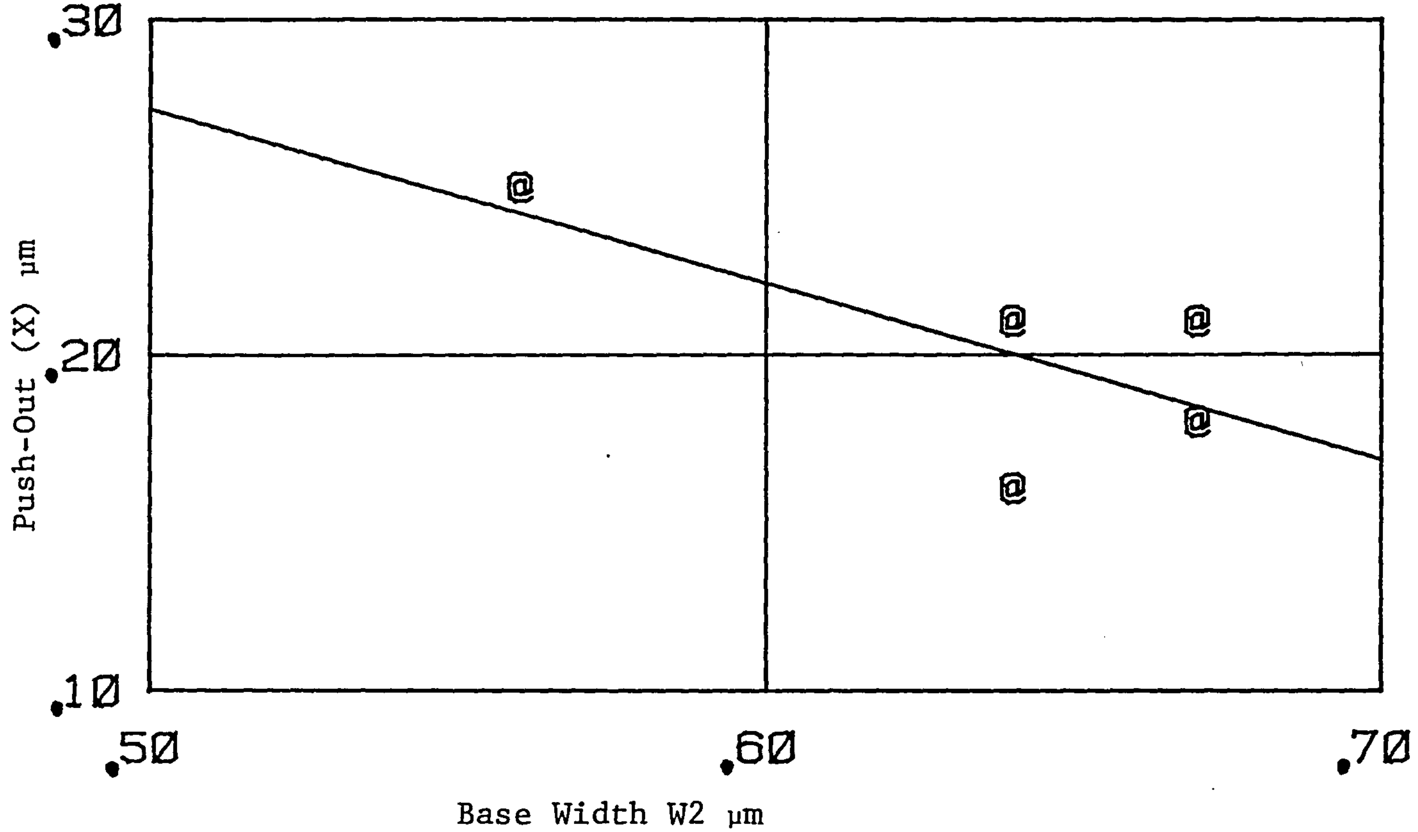
```
determination factor  .008815
correlation factor    .093888
standard error       3.93218
```

Figure 29 - Push-Out vs Base Width W1 for group 2



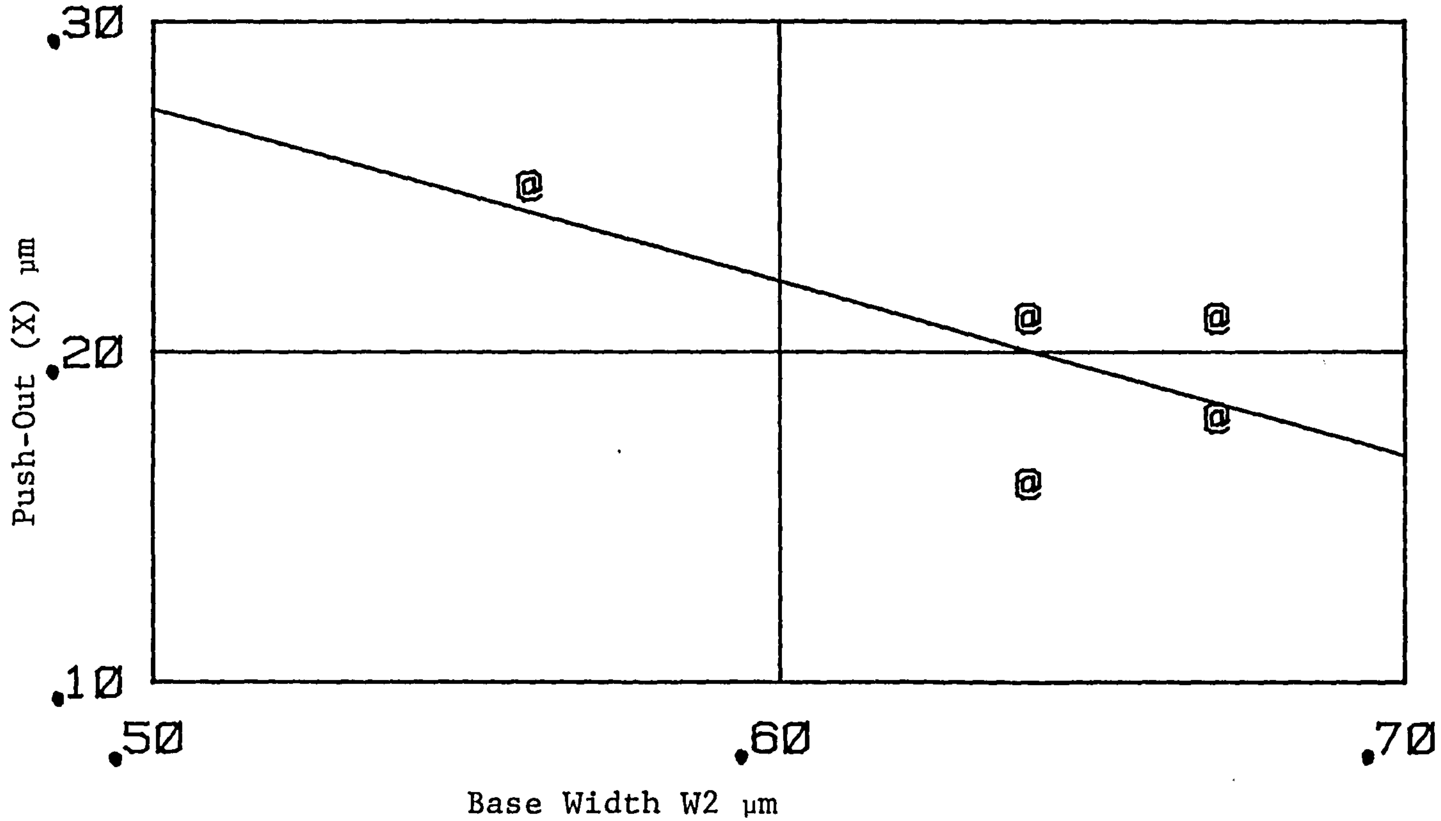
determination factor .008815
correlation factor .093888
standard error 3.93218

Figure 29 - Push-Out vs Base Width W1 for group 2



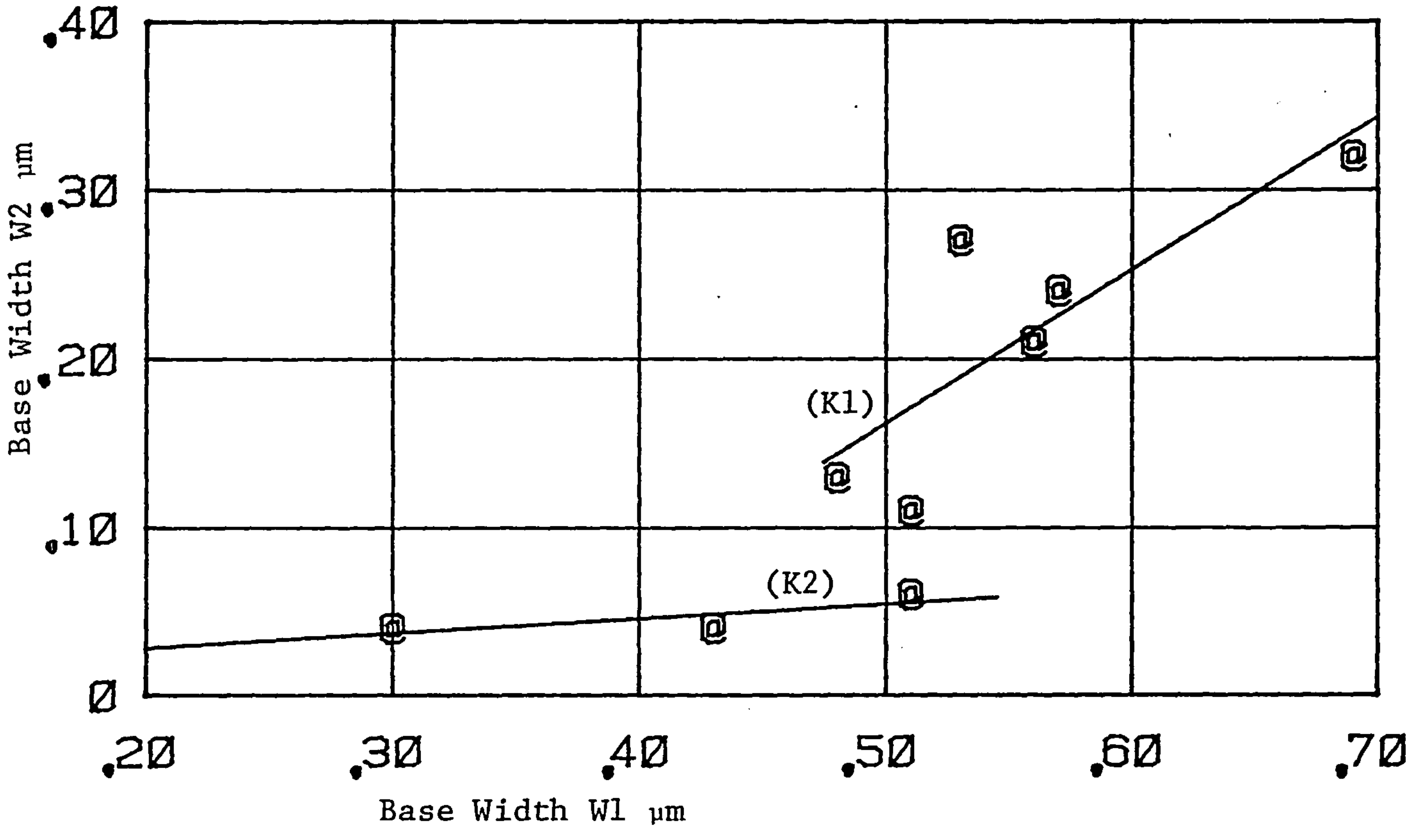
determination factor .477572
correlation factor .691066
standard error 2.85476

Figure 30 - Push-Out vs Base Width W2 for group 2



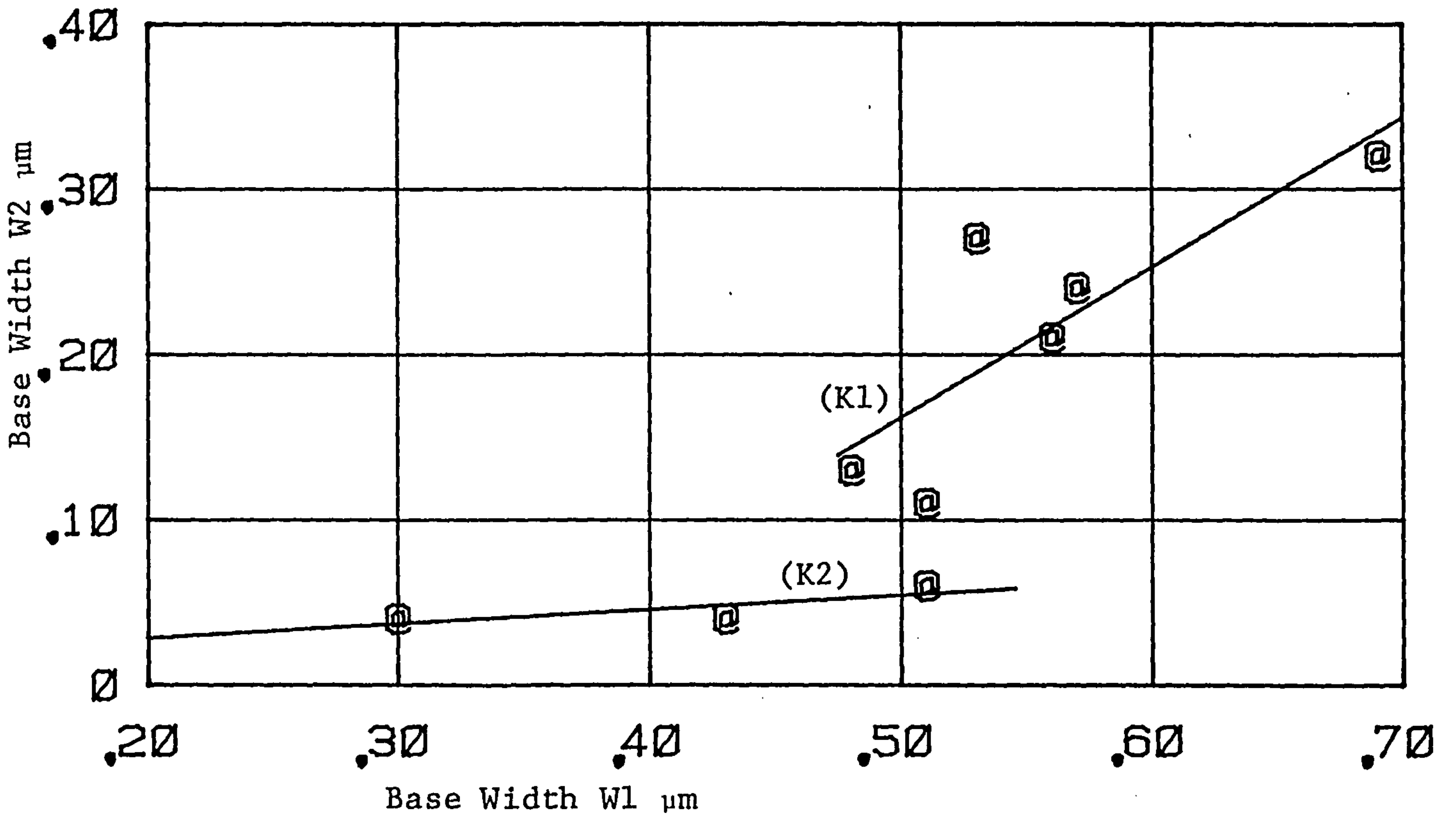
determination factor .477572
correlation factor .691066
standard error 2.85476

Figure 30 - Push-Out vs Base Width W2 for group 2



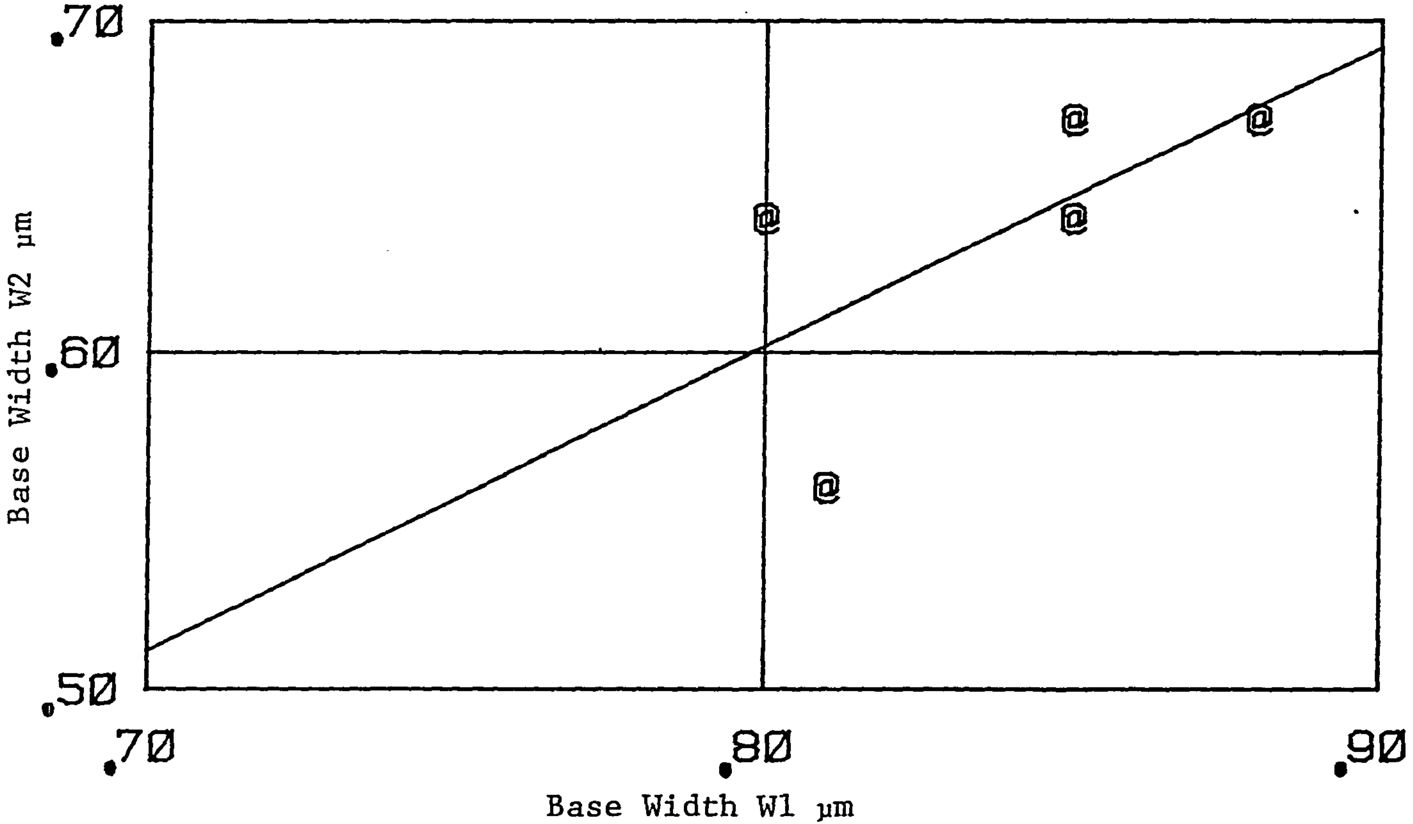
determination factor K1= .668871, K2= .62388
correlation factor K1= .817813, K2= .789861
standard error K1= 5.22183, K2= 1.00149

Figure 31 - Base Width W2 vs Base Width W1 for group 1



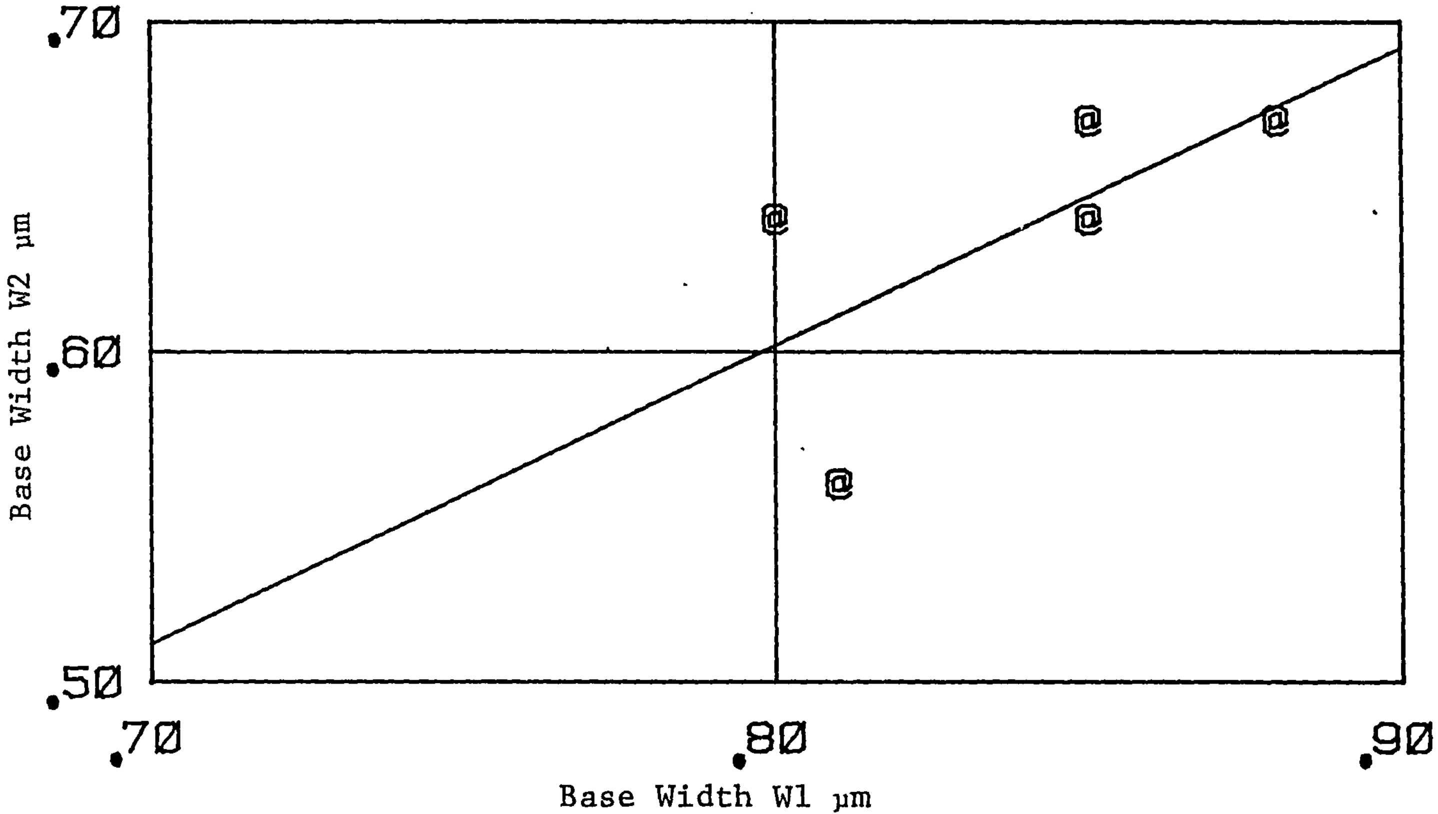
determination factor K1= .668871, K2= .62388
correlation factor K1= .817813, K2= .789861
standard error K1= 5.22183, K2= 1.00149

Figure 31 - Base Width W2 vs Base Width W1 for group 1



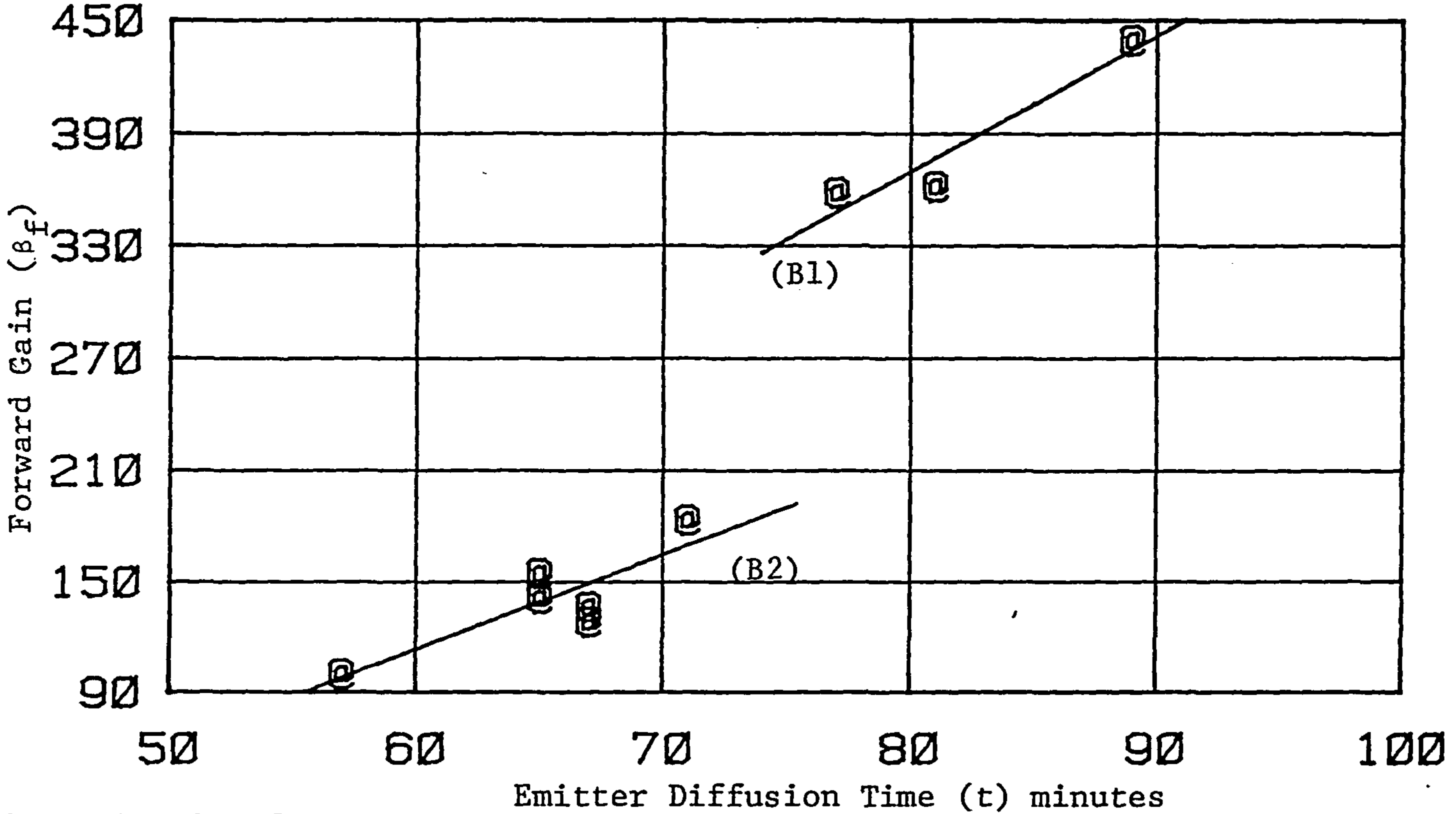
determination factor .429107
correlation factor .655063
standard error 3.93086

Figure 32 - Base Width W2 vs Base Width W1 for group 2



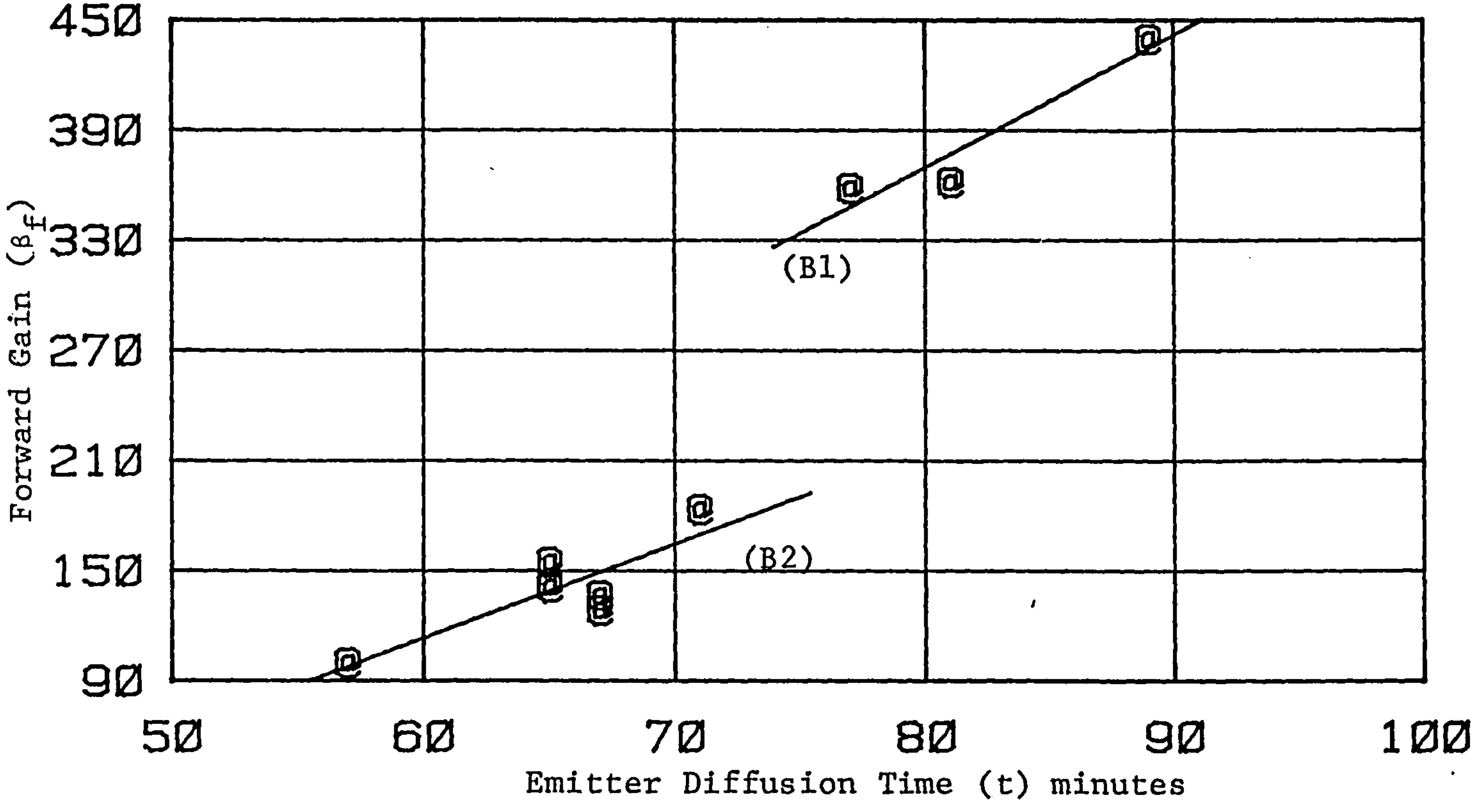
determination factor .429107
correlation factor .655063
standard error 3.93086

Figure 32 - Base Width W2 vs Base Width W1 for group 2



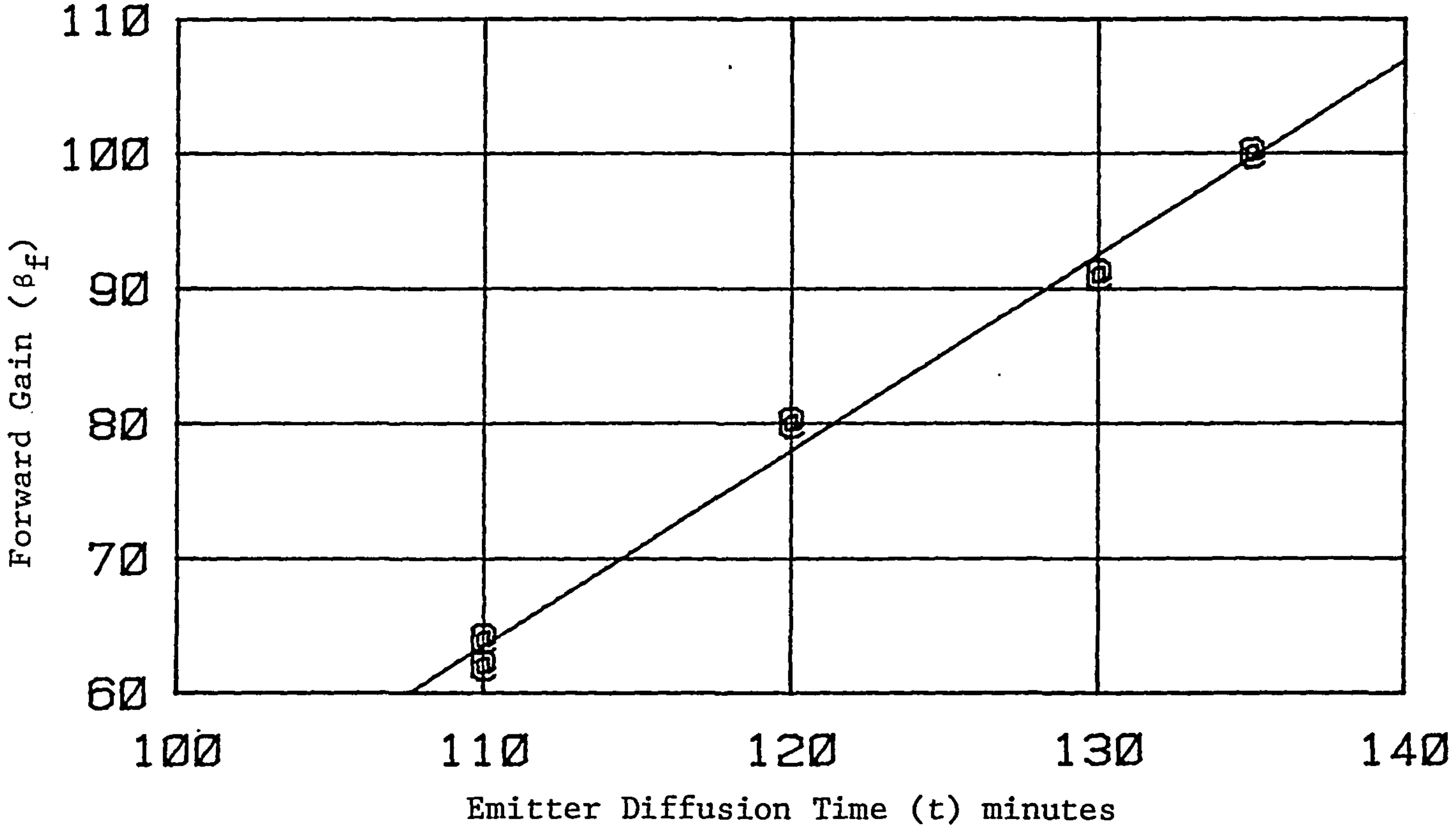
determination factor B1= .731995, B2= .914561
correlation factor B1= .855567, B2= .956327
standard error B1= 16.0743, B2= 19.0799

Figure 33 - Forward Gain vs Emitter Diffusion Time for group 1



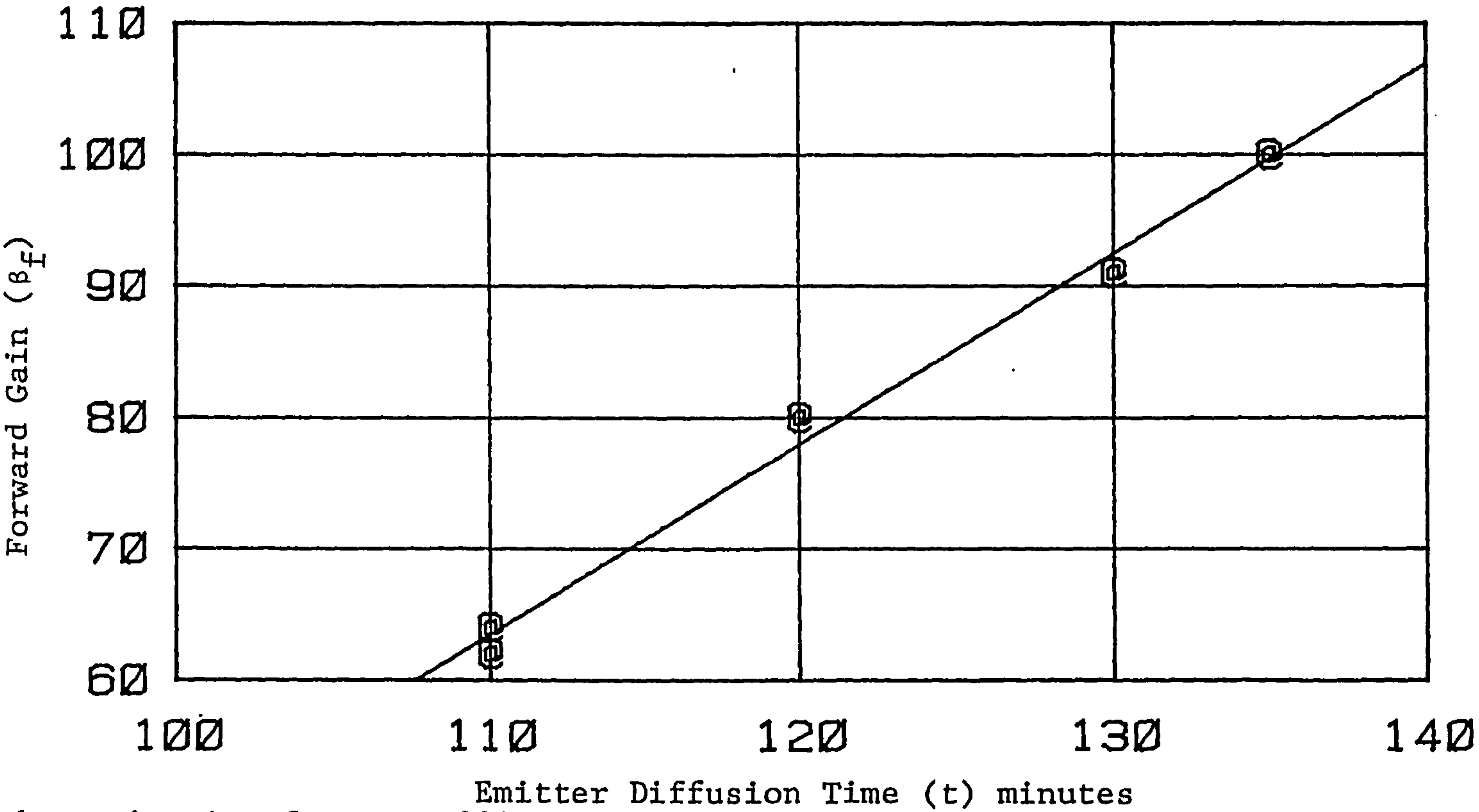
determination factor B1= .731995, B2= .914561
correlation factor B1= .855567, B2= .956327
standard error B1= 16.0743, B2= 19.0799

Figure 33 - Forward Gain vs Emitter Diffusion Time for group 1



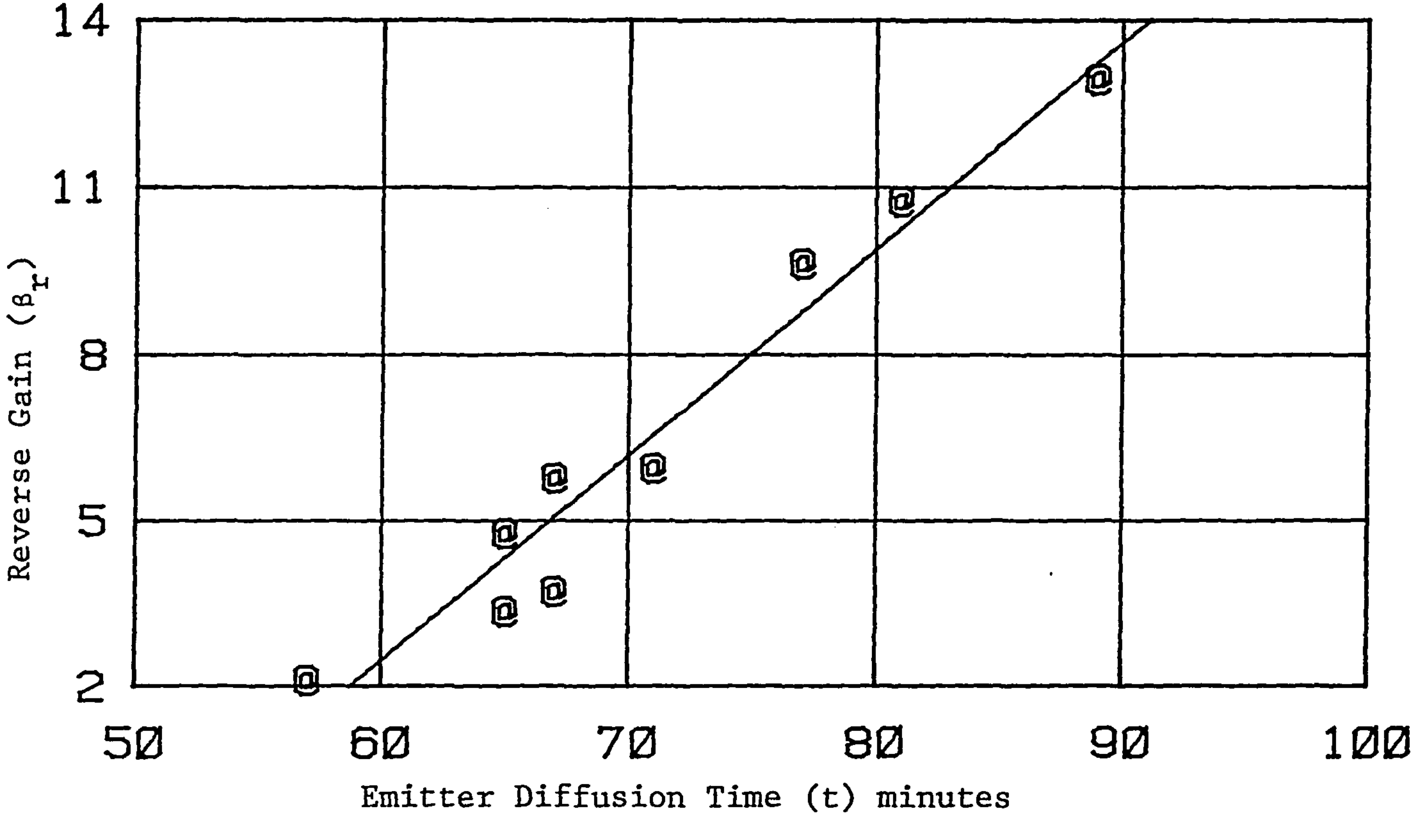
determination factor .991998
correlation factor .995991
standard error 1.71232

Figure 34 - Forward Gain vs Emitter Diffusion Time for group 2



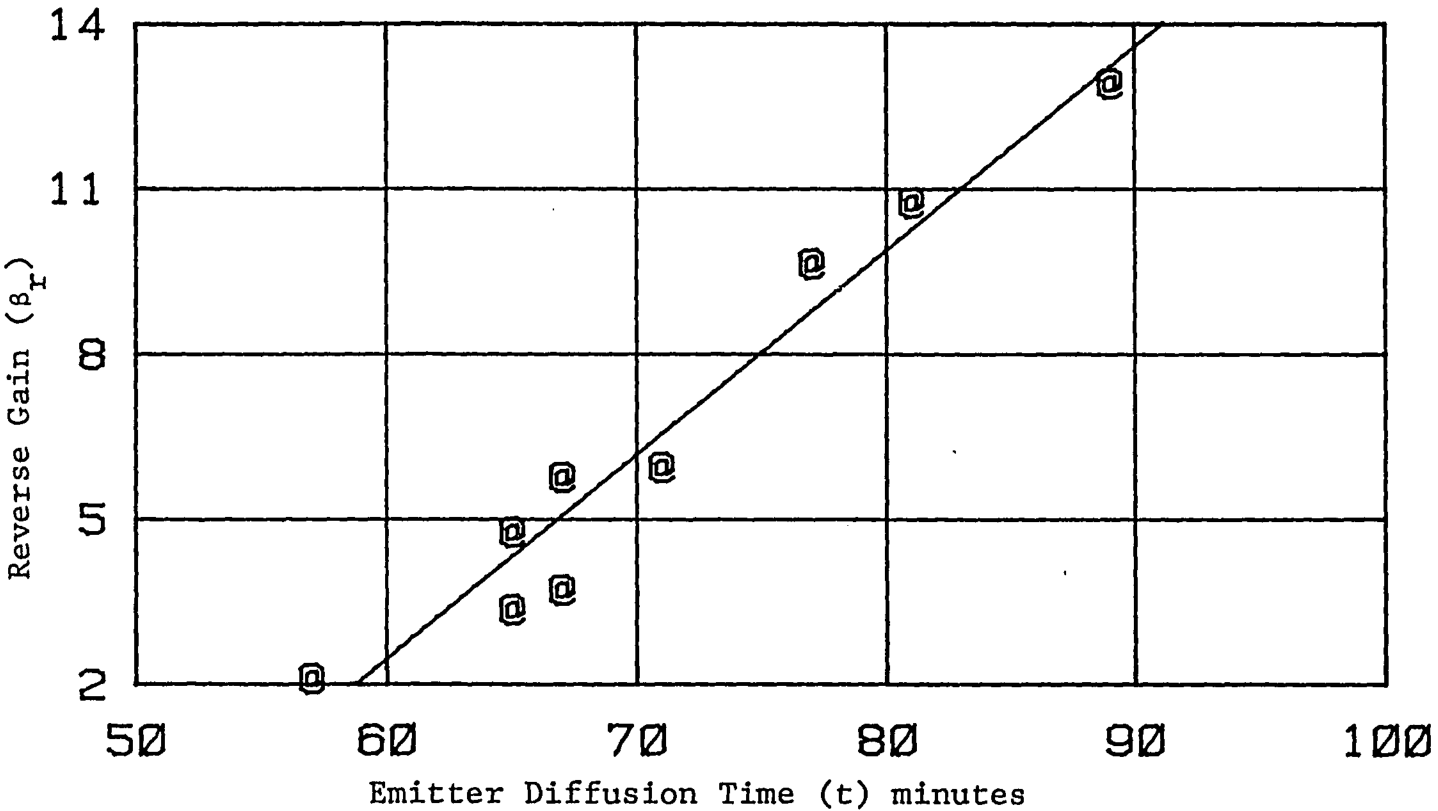
determination factor .991998
correlation factor .995991
standard error 1.71232

Figure 34 - Forward Gain vs Emitter Diffusion Time for group 2



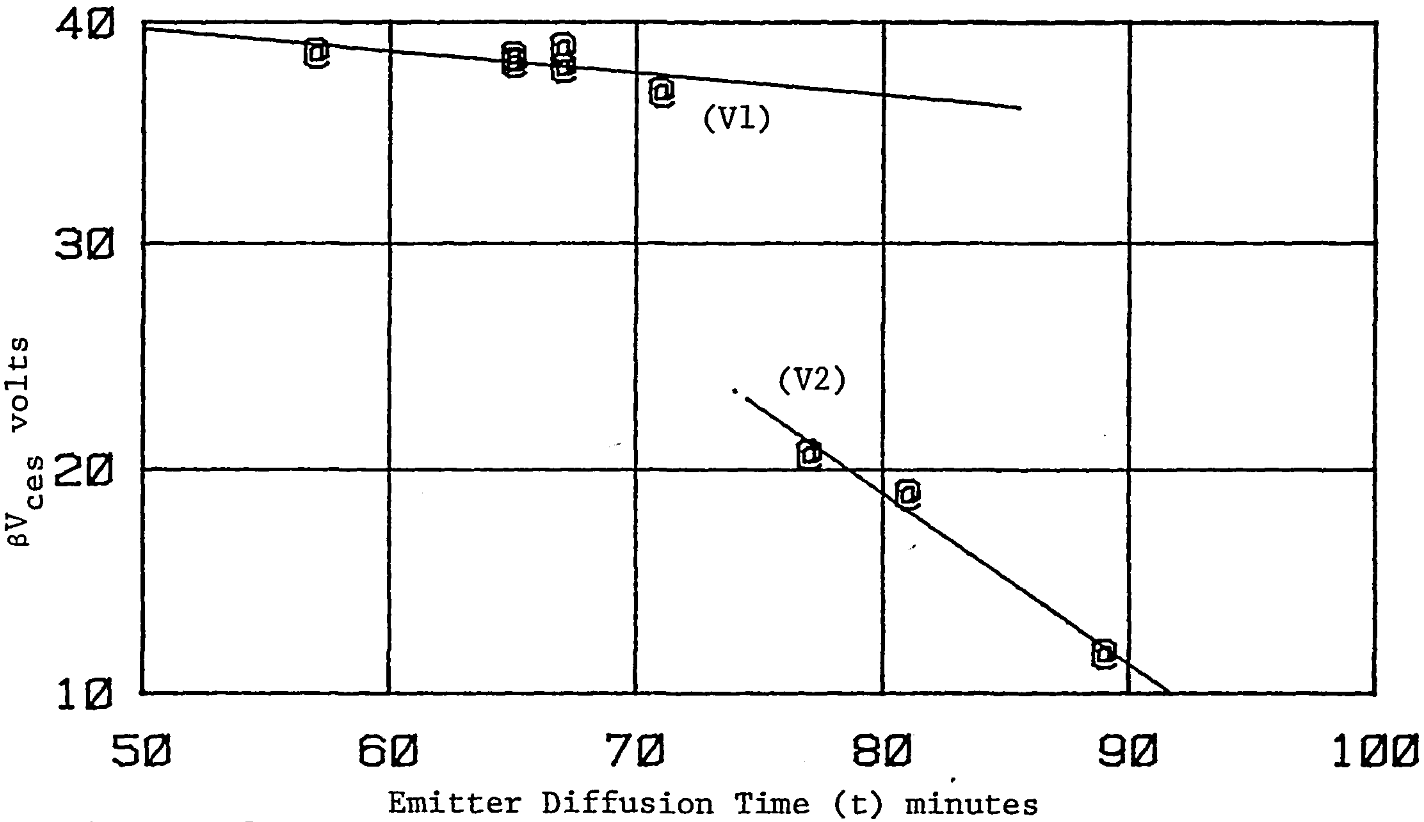
determination factor .950406
correlation factor .974888
standard error 88.2002

Figure 35 - Reverse Gain vs Emitter Diffusion Time for group 1



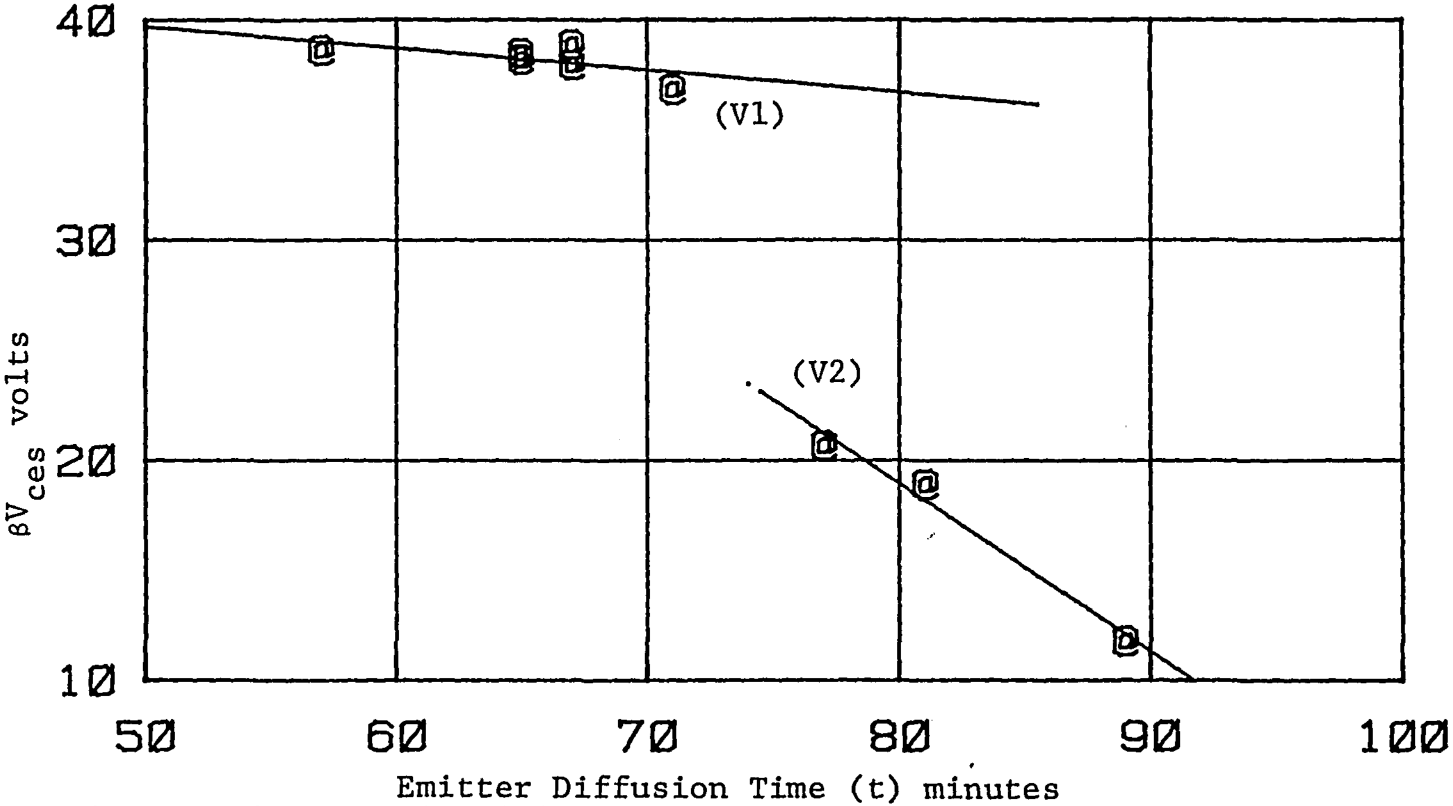
determination factor .950406
correlation factor .974888
standard error 88.2002

Figure 35 - Reverse Gain vs Emitter Diffusion Time for group 1



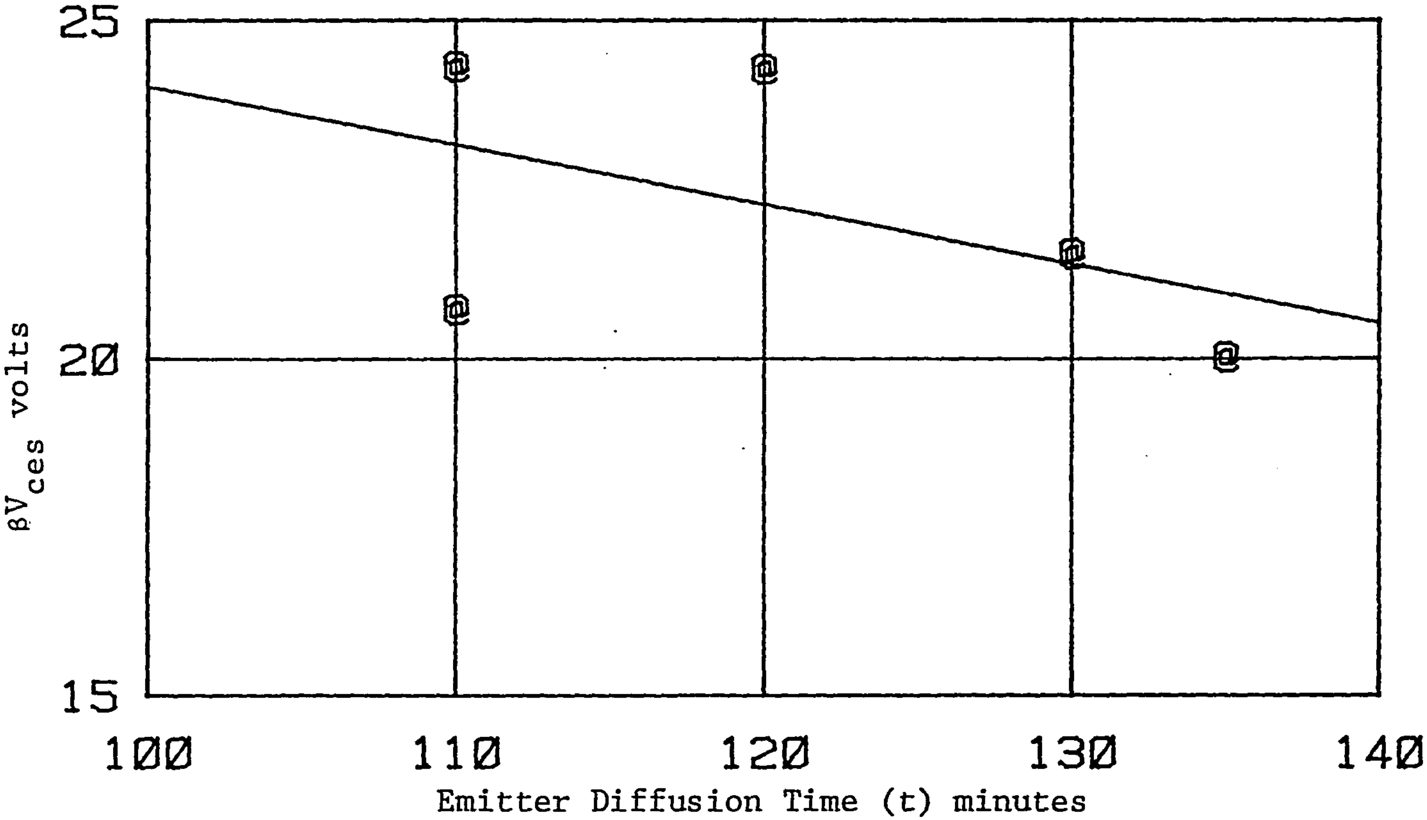
determination factor V1= .414684, V2= .979289
correlation factor V1= .64396 , V2= .989591
standard error V1= .621611, V2= .955783

Figure 36 - βV_{ces} Breakdown Voltage vs Emitter Diffusion Time for group 1



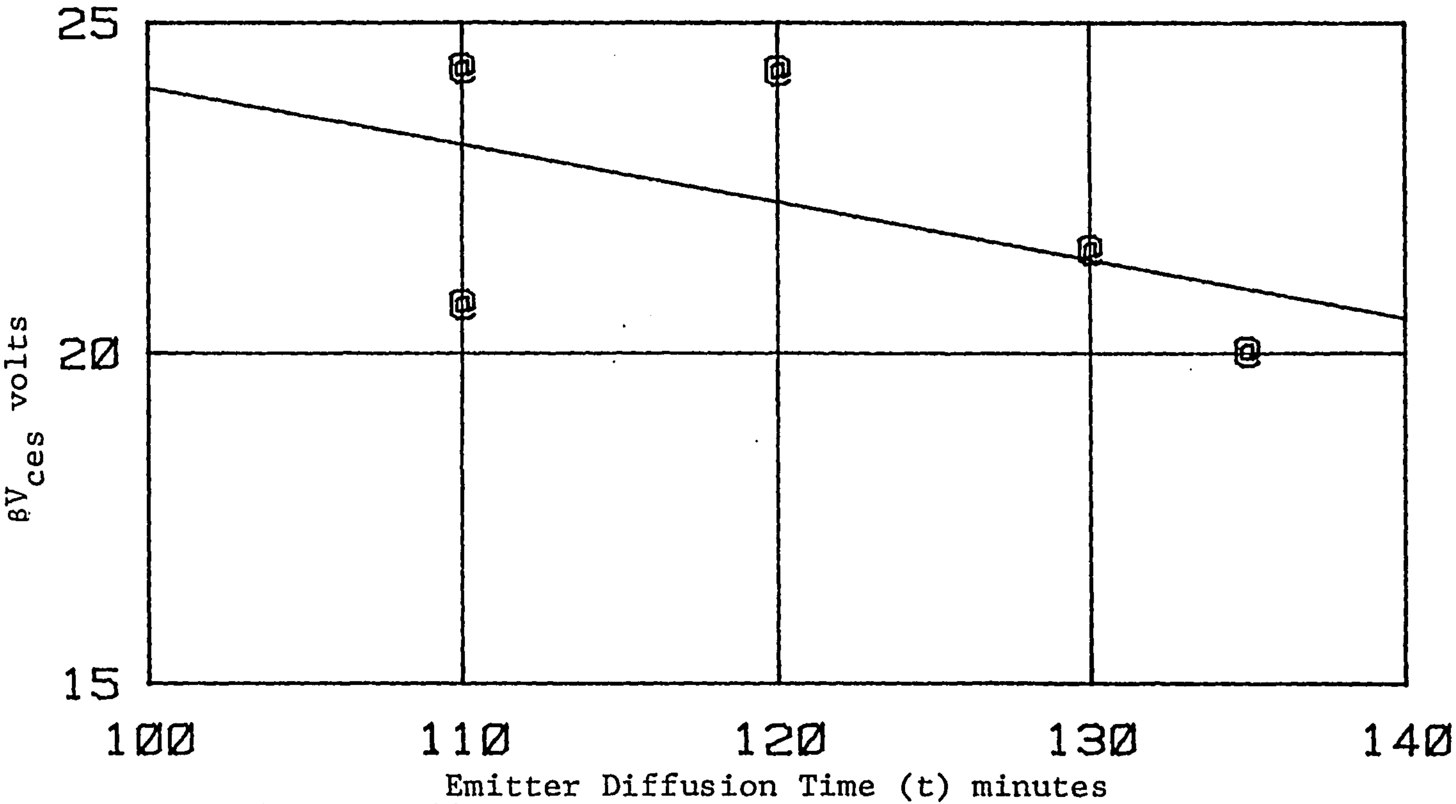
determination factor V1= .414684, V2= .979289
correlation factor V1= .64396 , V2= .989591
standard error V1= .621611, V2= .955783

Figure 36 - βV_{ces} Breakdown Voltage vs Emitter Diffusion Time for group 1



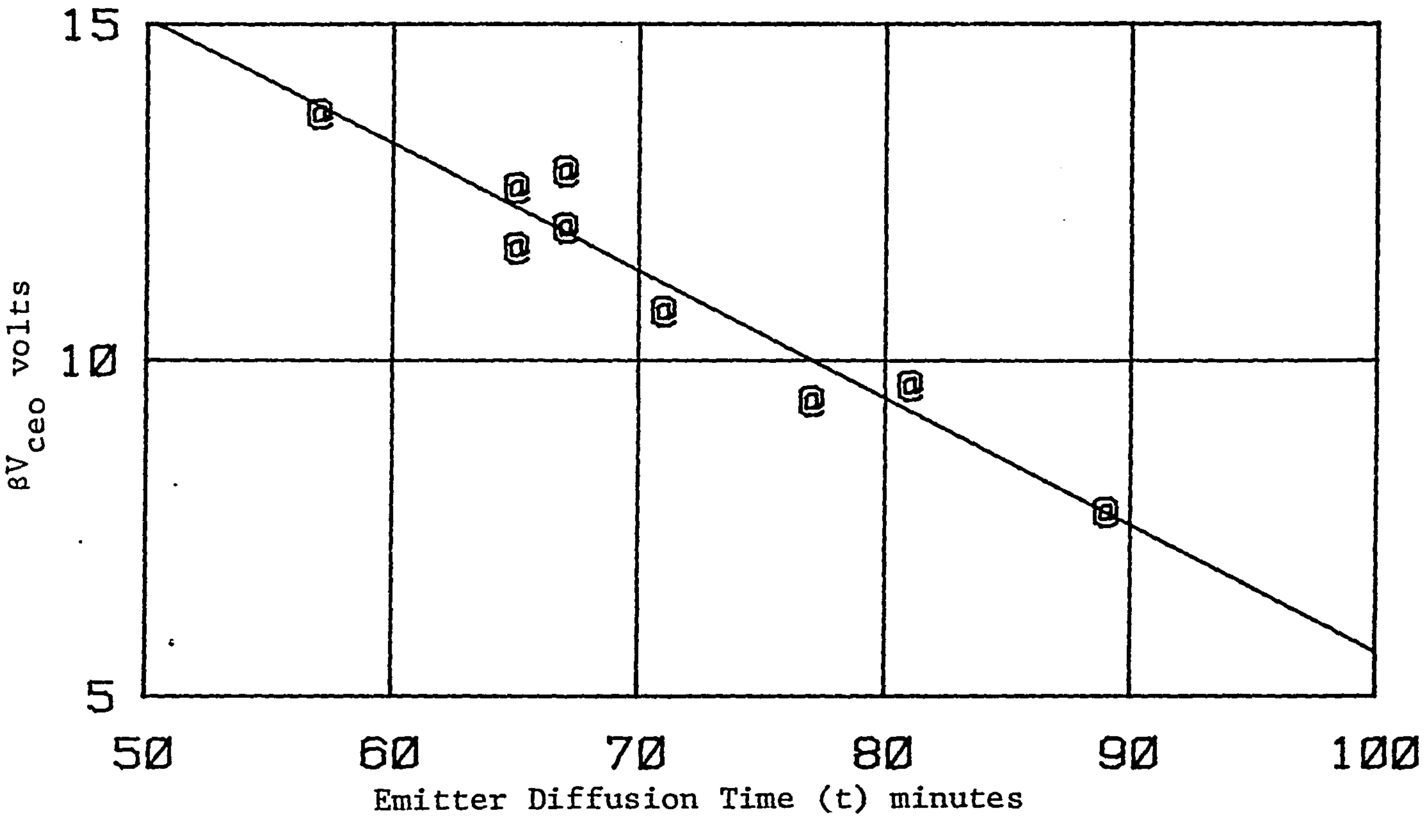
determination factor .247535
correlation factor .497529
standard error 2.0076

Figure 37 - βV_{ces} Breakdown Voltage vs Emitter Diffusion Time for group 2



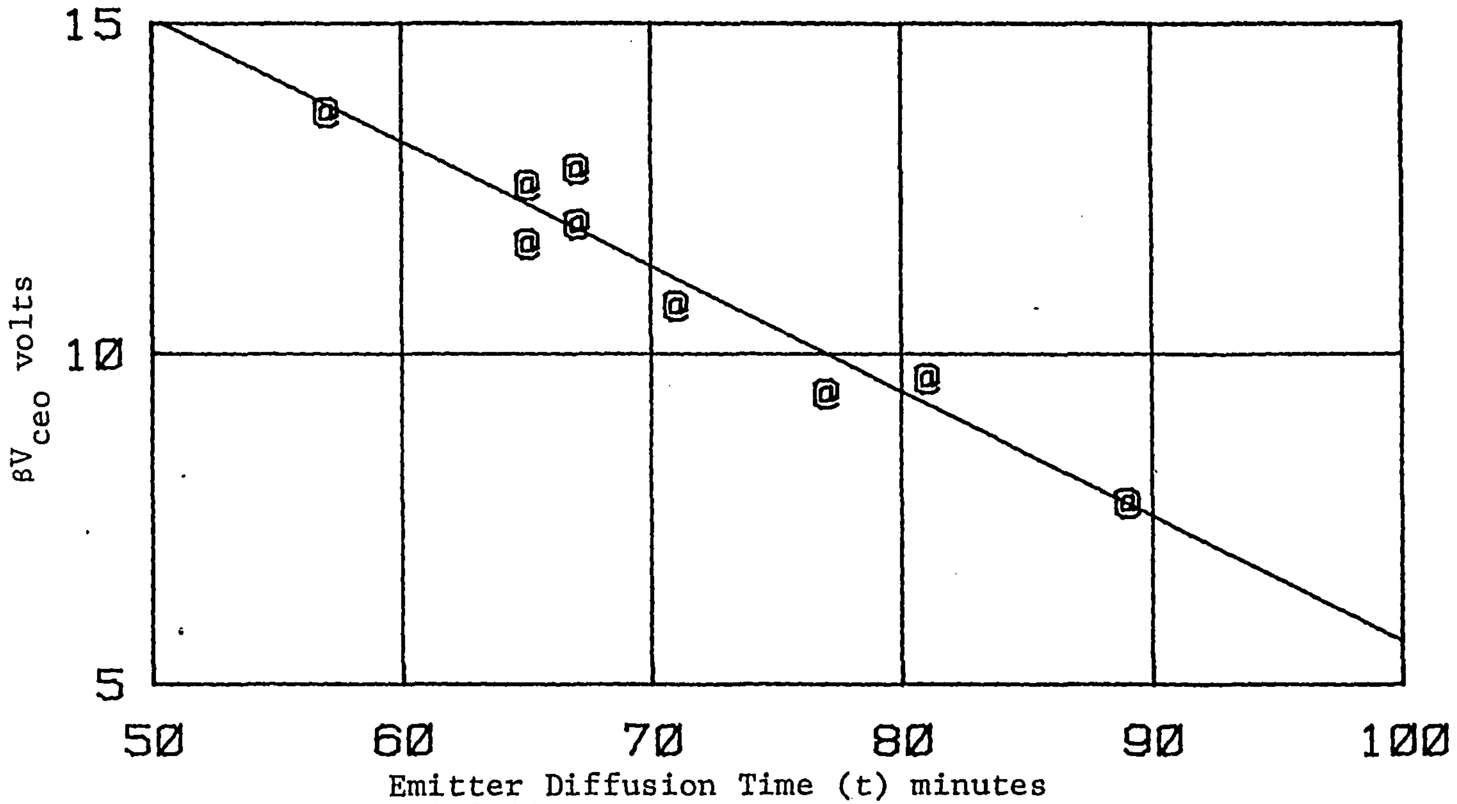
determination factor .247535
correlation factor .497529
standard error 2.0076

Figure 37 - βV_{ces} Breakdown Voltage vs Emitter Diffusion Time for group 2



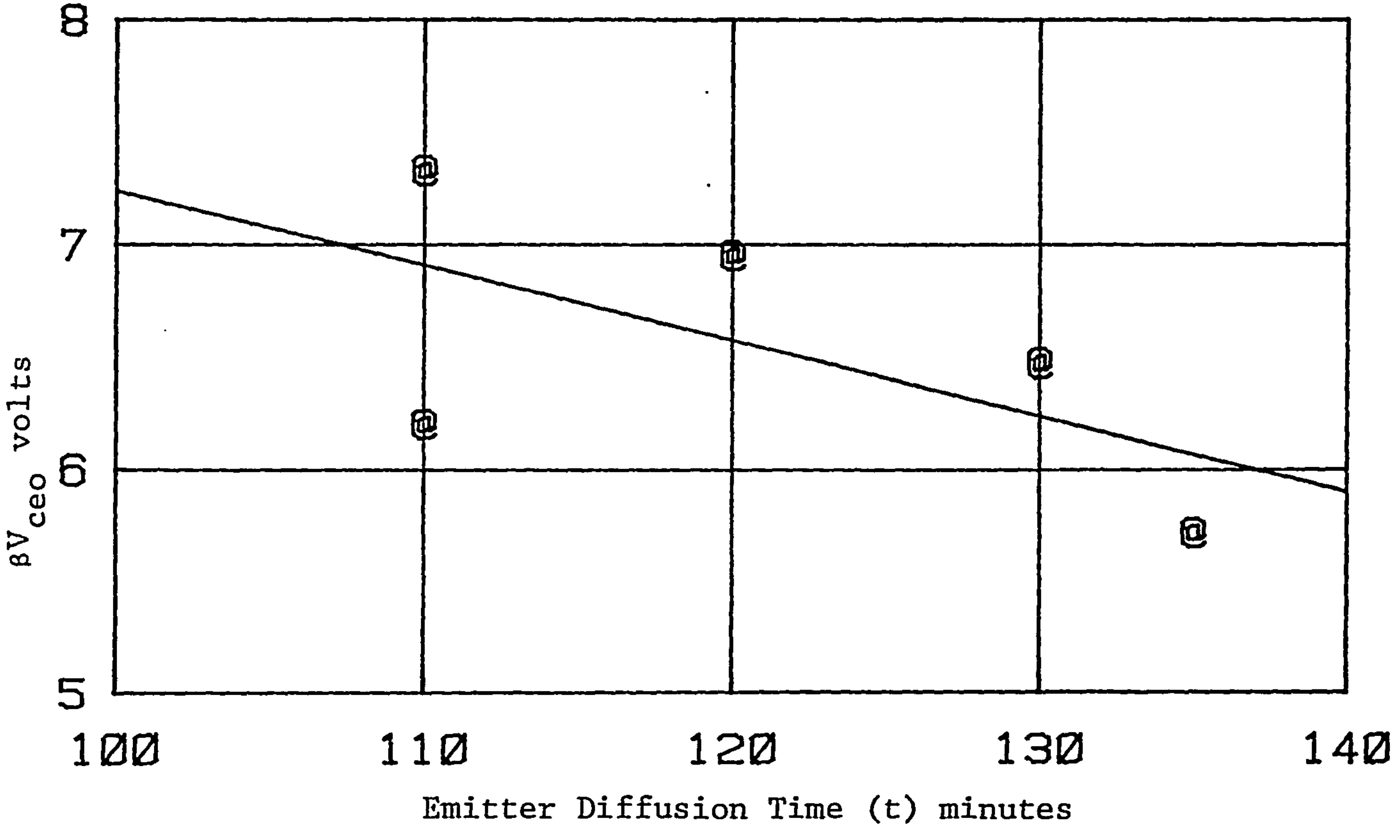
determination factor	.932114
correlation factor	.965461
standard error	.530353

Figure 38 - βV_{ceo} Breakdown Voltage vs Emitter Diffusion Time for group 1



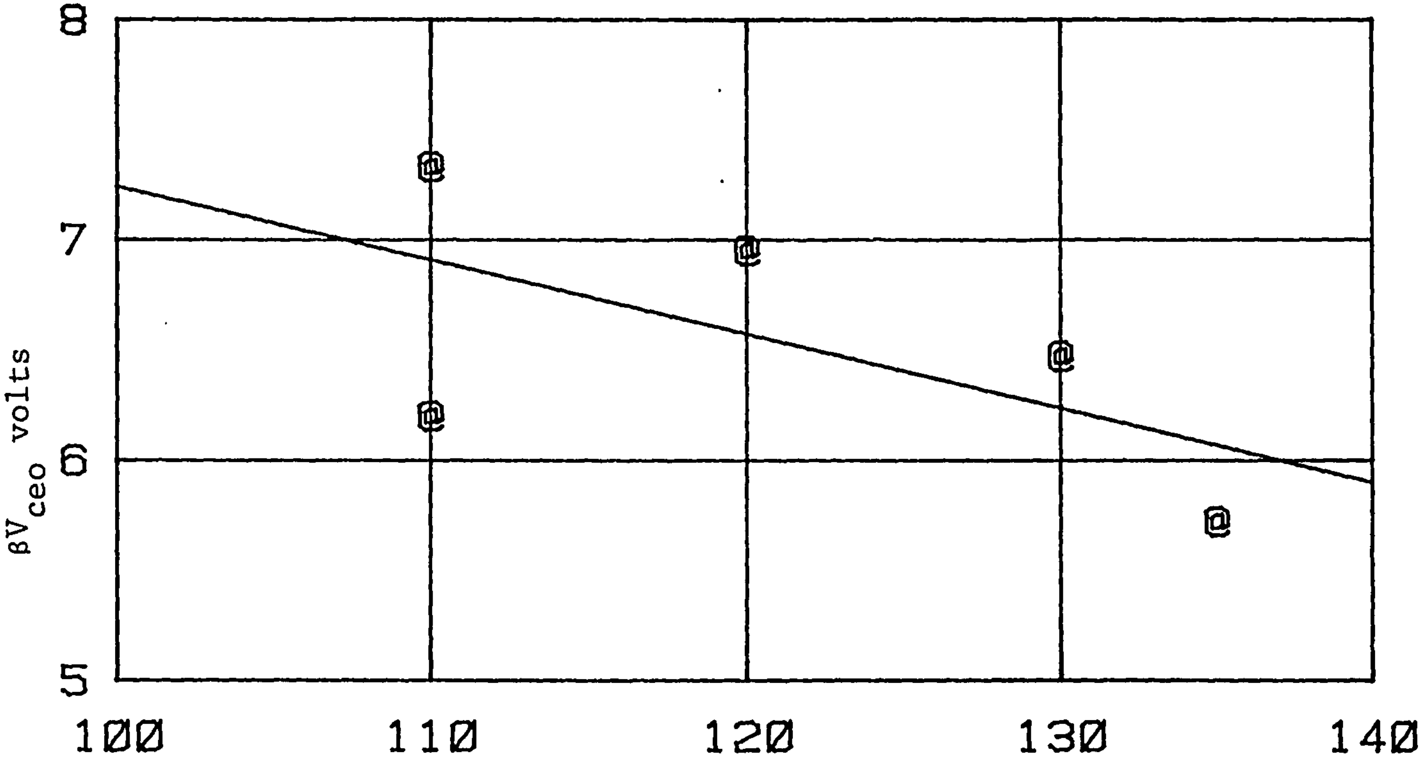
determination factor	.932114
correlation factor	.965461
standard error	.530353

Figure 38 - βV_{ceo} Breakdown Voltage vs Emitter Diffusion Time for group 1



determination factor .370297
correlation factor .60852
standard error .5768

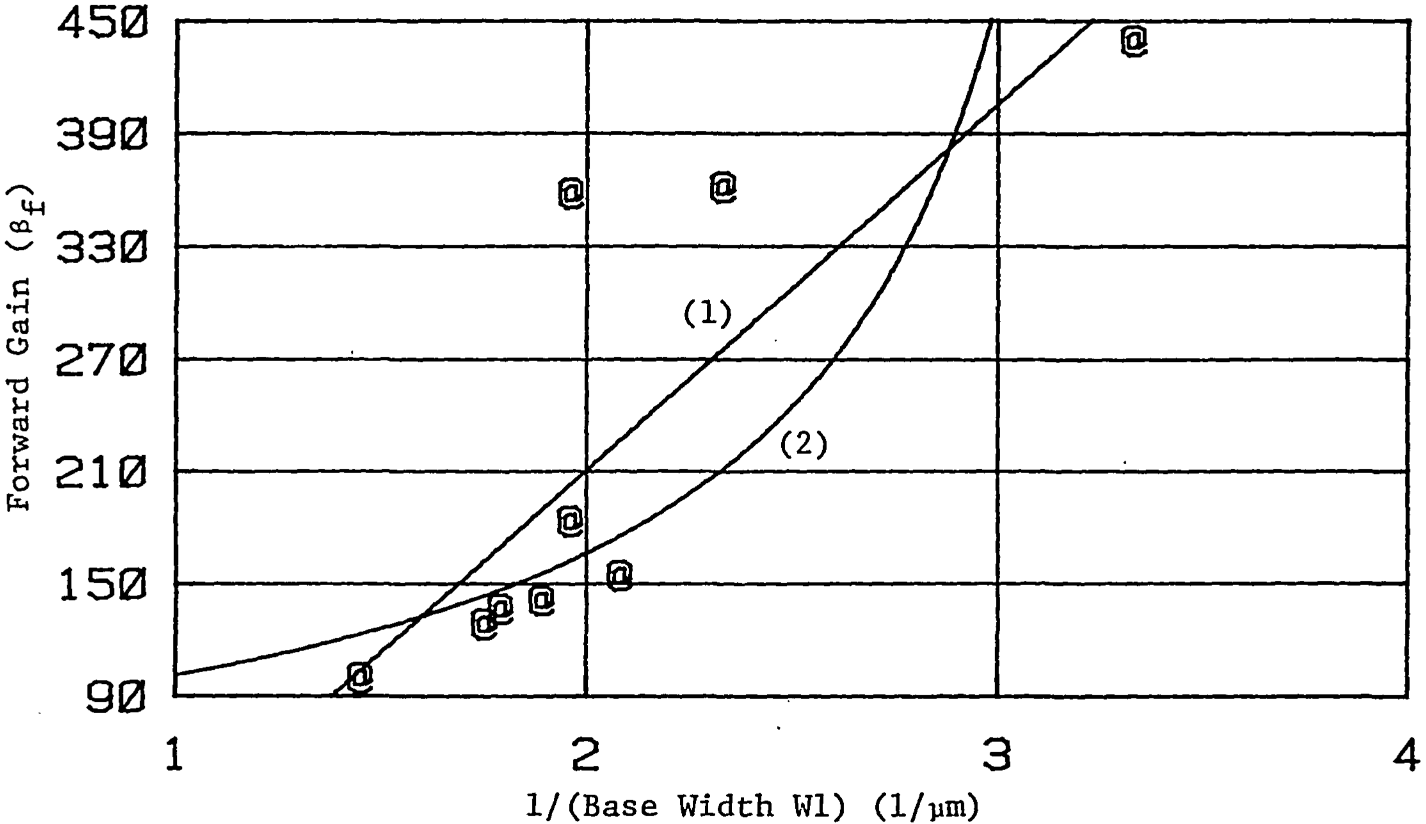
Figure 39 - βV_{ceo} Breakdown Voltage vs Emitter Diffusion Time for group 2



Emitter Diffusion Time (t) minutes

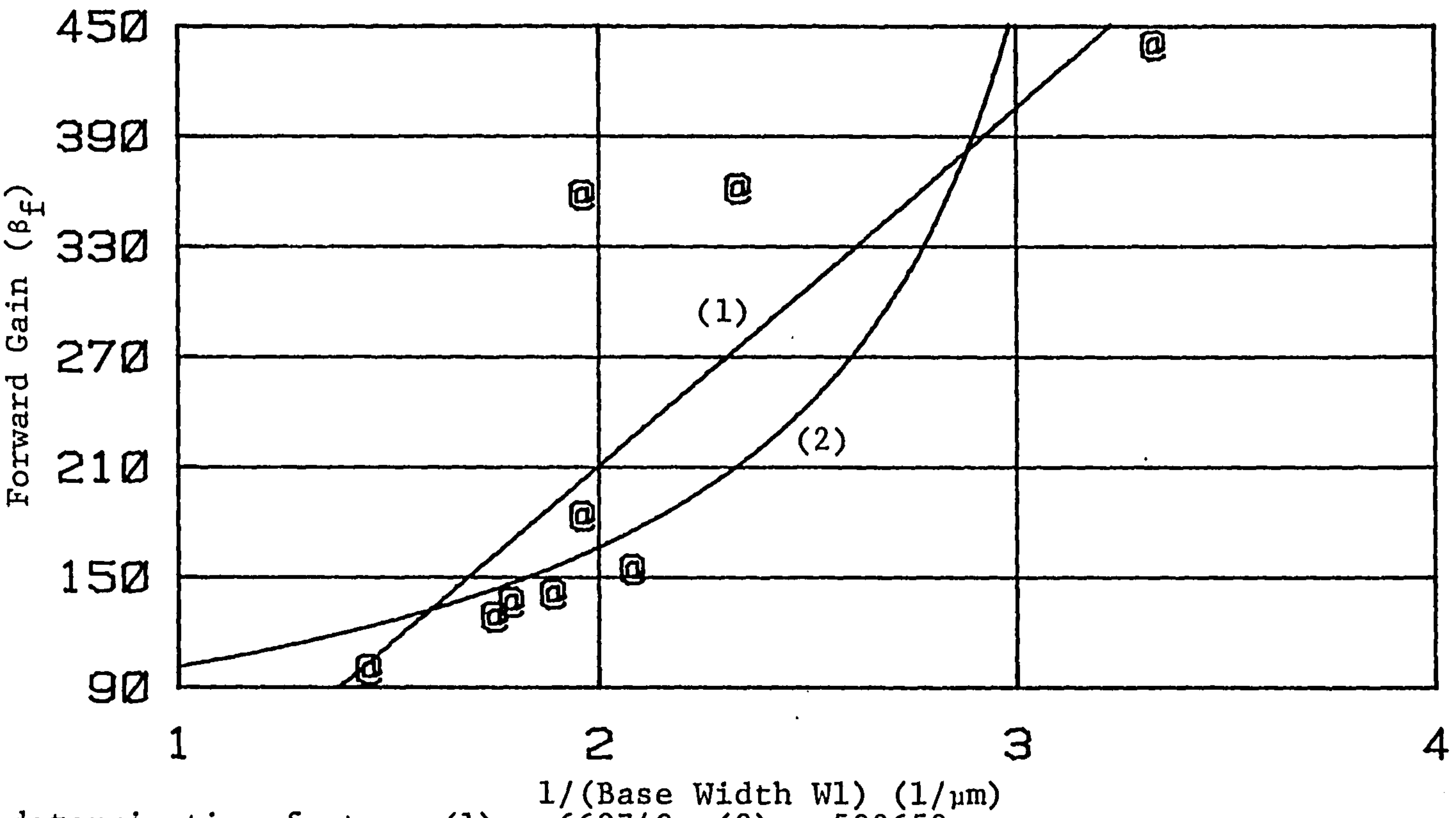
determination factor	.370297
correlation factor	.60852
standard error	.5768

Figure 39 - βV_{ceo} Breakdown Voltage vs Emitter Diffusion Time for group 2



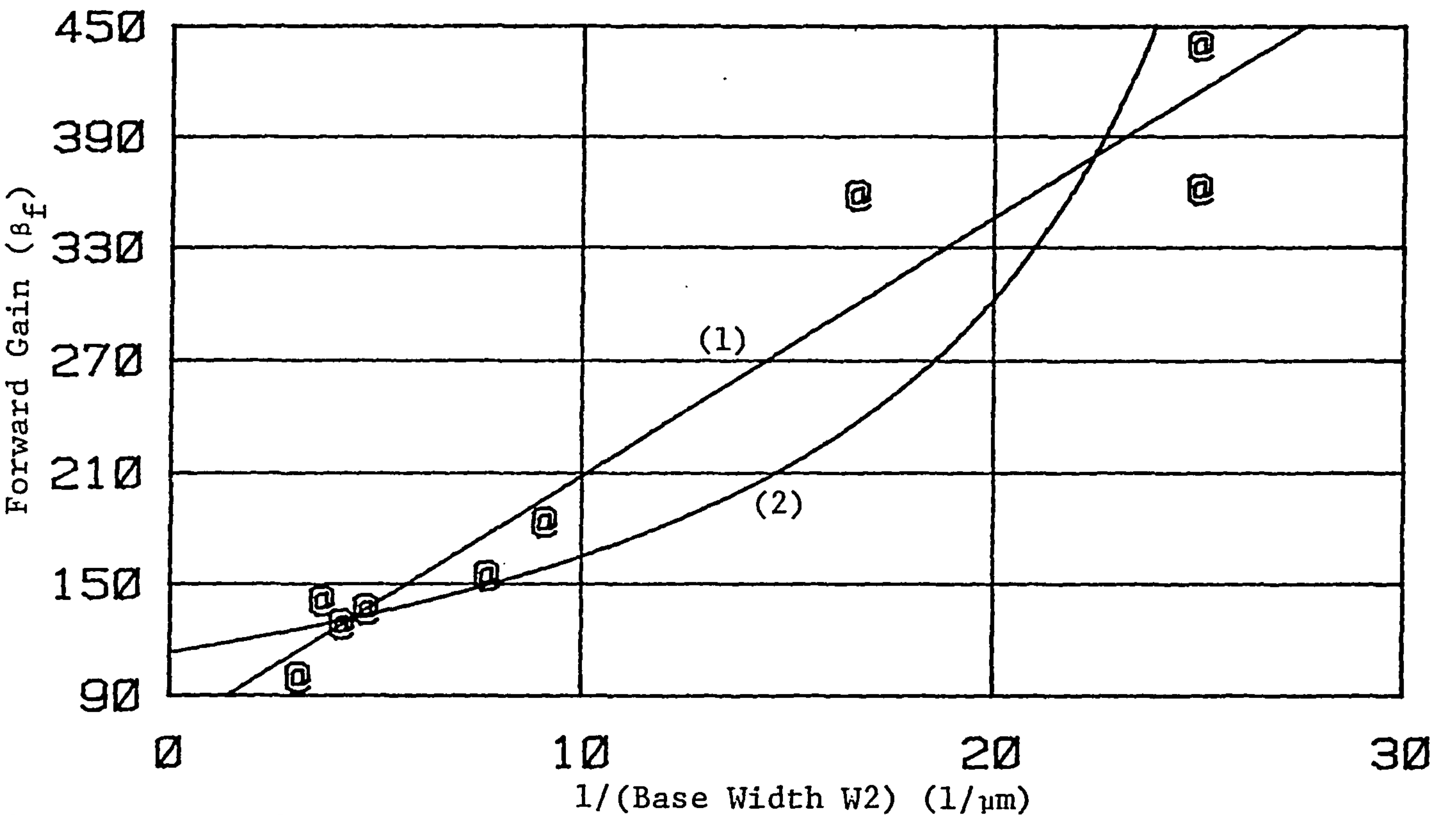
determination factor (1)= .669749, (2)= .592659
standard error (1)= 78.0 , (2)= .0018

Figure 40 - Forward Gain vs 1/(Base Width W1) for group 1



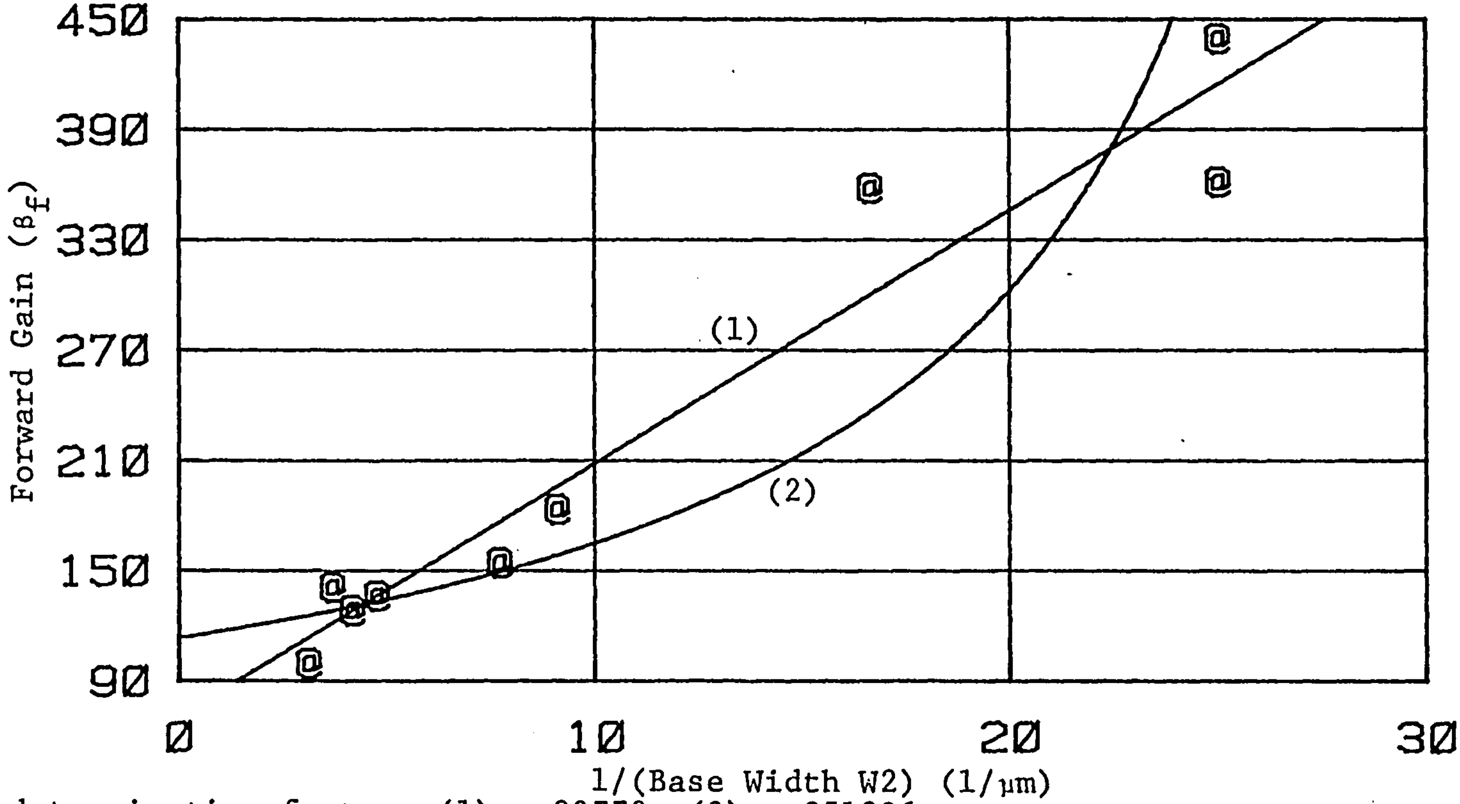
determination factor (1)= .669749, (2)= .592659
standard error (1)= 78.0 , (2)= .0018

Figure 40 - Forward Gain vs 1/(Base Width W1) for group 1



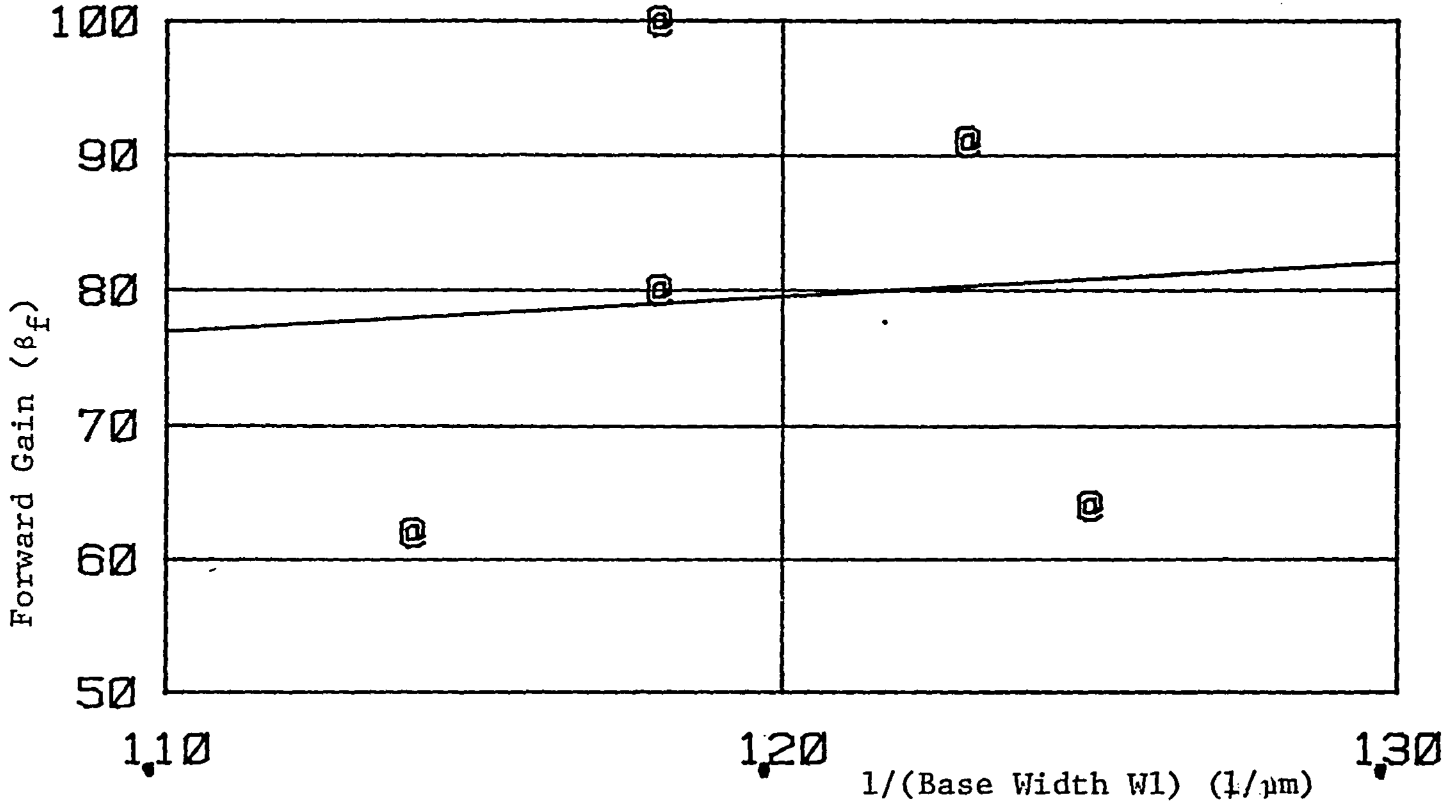
determination factor (1)= .93773, (2)= .851236
standard error (1)= 33.9 , (2)= .0011

Figure 41 - Forward Gain vs 1/(Base Width W2) for group 1



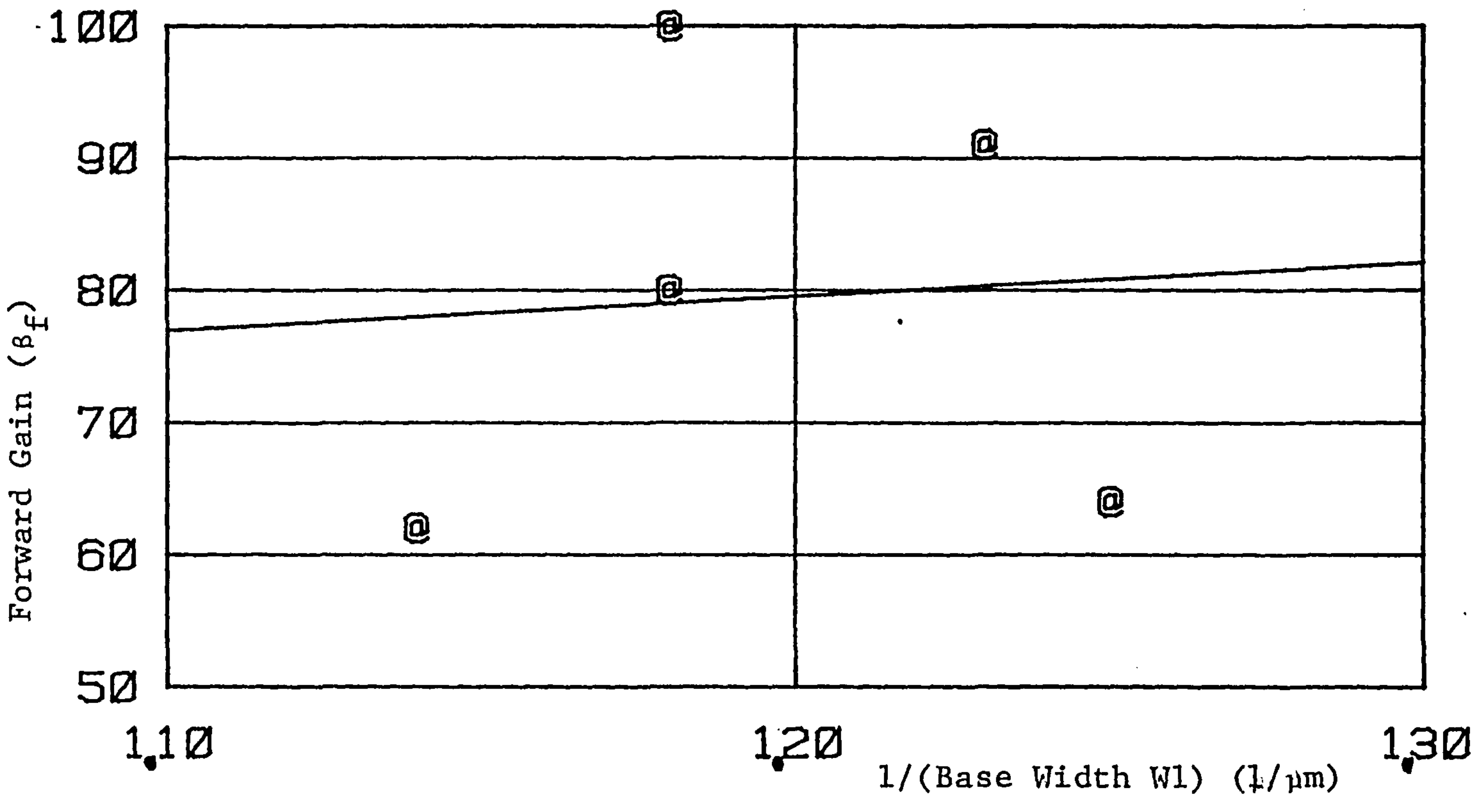
determination factor (1)= .93773, (2)= .851236
standard error (1)= 33.9 , (2)= .0011

Figure 41 - Forward Gain vs 1/(Base Width W2) for group 1



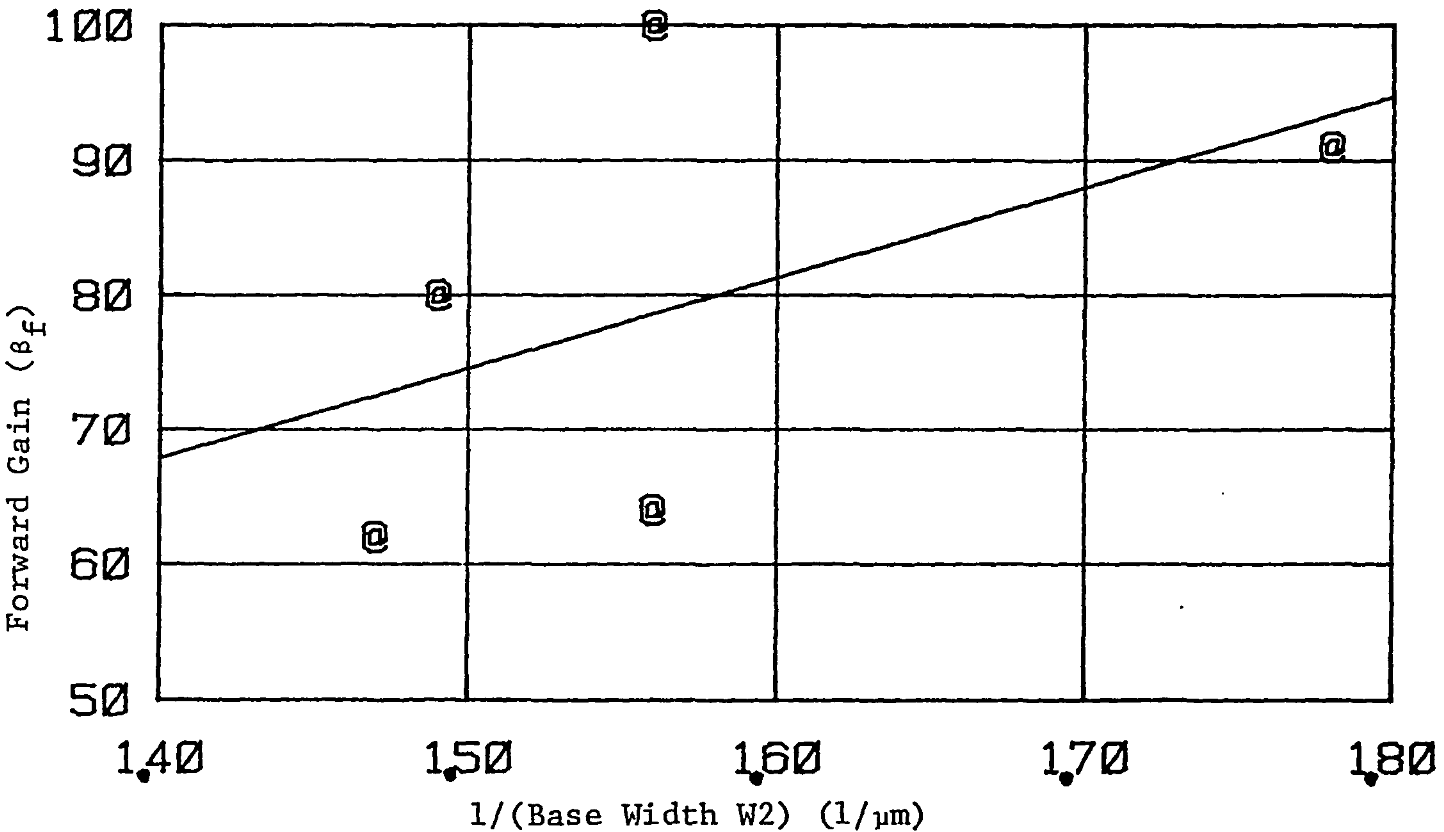
determination factor .004619
correlation factor .067964
standard error 19.0971

Figure 42 - Forward Gain vs 1/(Base Width W1) for group 2



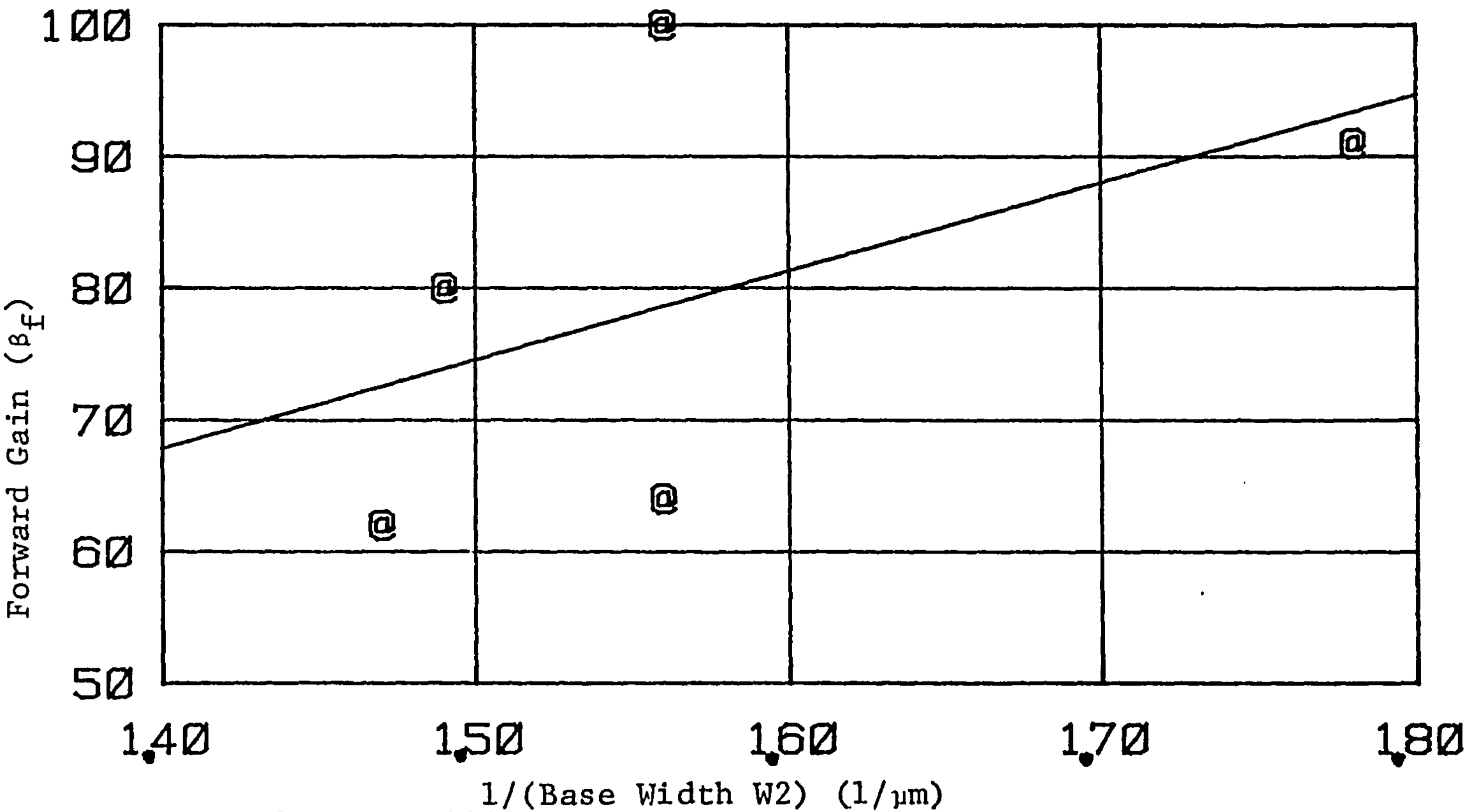
determination factor .004619
correlation factor .067964
standard error 19.0971

Figure 42 - Forward Gain vs 1/(Base Width W1) for group 2



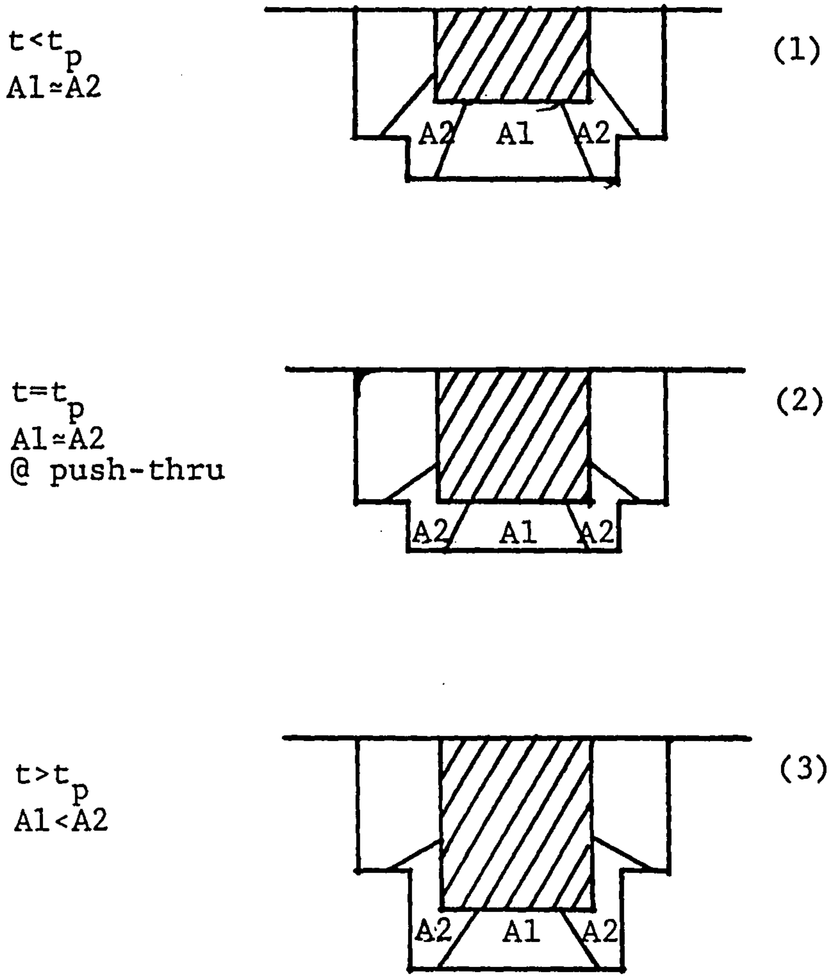
determination factor .239243
correlation factor .489125
standard error 16.1833

Figure 43 - Forward Gain vs 1/(Base Width W2) for group 2



determination factor .239243
correlation factor .489125
standard error 16.1833

Figure 43 - Forward Gain vs 1/(Base Width W2) for group 2



t_p = emitter diffusion time at "push-thru"
A1= area for base width W1
A2= area for base width W2

Figure 44 - Change in Base Area with increasing Emitter Depth

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VITA

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At Western Electric, he is presently a Product Engineer for bipolar integrated circuits designed in OXIL, an oxide isolation technology.