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Development and design of a power monitor circuit.

Takashi Tsuda

DEVELOPMENT AND DESIGN OF A POWER MONITOR CIRCUIT

by

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December 10, 1982
(date)

Professor in Charge

Chairman of Department

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Table of Contents

List of Figures

List of Tables

Abstract

The object of this work is to develop and design a microprocessor based power monitor circuit for use in office, commercial or light industrial buildings.

Voltage and current transformers with capabilities up to 277 V and 230 A respectively are used to assure ease of installation and accurate measurement.

After surveying the existing power distribution systems currently in use, and studying in detail the characteristics of the required instrument transformers, a circuit based on the Intel 8051 microcomputer and the Exar Integrated System XR-2208 operation multiplier is developed.

A detailed study of the effects of harmonics in the measured current waveforms and flow charts for the microcomputer program are included.

Both a detailed mathematical error analysis and an experimental study show that power measurements of 1.9 % accuracy are provided at powers up to 231 kW.

1. Introduction

This work presents the development and design of a microprocessor based power monitoring circuit for use in office, commercial or light industrial buildings. With the ever rising energy costs it is becoming very important to institute automatic control of the energy usage in such buildings. An very important component of any serious energy management system is the ability to accurately measure the flow of electrical power into the building.

There are several features which are required in such a power monitor. First, the output of the power monitor circuit should be in digital form in order to easily interface with the remaining parts of the control system. Second, easy installation of the metering device is important. However, ordinary power meters have to be installed in the power lines. That is, the power lines have to be cut. This is quite inconvenient. Transformers can solve this problem and are employed for the voltage and current measurement of the power monitor circuit. Because of the importance of the transformers their characteristics are analyzed in detail later on.

There are several kinds of power distribution systems commonly used in office, commercial or light industrial buildings. Therefore, for the third feature

the power monitor circuit is designed to have the flexibility to measure power in different kinds of power distribution system.

2. Power Distribution Systems and Power Measurement

2.1 Common Power Distribution Systems

There are several power distribution systems commonly used in office, commercial and light industrial buildings [1, 2]. The frequency of all the systems is 60 Hz in most cases. These systems are:

(1) 120 V, single-phase, 2-wire system (see Figure 2-1): This is used for the smallest of facilities such as small residences, out-buildings and isolated small loads. This is also the arrangement of the usual branch circuit.

(2) 120/240 V, single-phase, 3-wire system (see Figure 2-2): This is a commonly used system in many residences, small apartments and commercial buildings. The single phase transformer is center-tapped to establish a neutral. The neutral connection is always grounded.

(3) 120/208 V, 3-phase, 4-wire system (see figure 2-3): This system is the most widely used 3-phase arrangement for medium sized facilities. The neutral connection is connected to the system ground.

(4) 277/480 V, 3-phase, 4-wire system (see Figure 2-4): This system is ideally suited for multistory office buildings and large single-level or multilevel

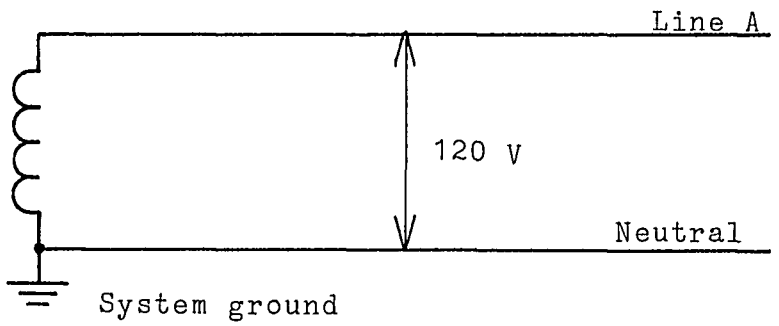


Figure 2-1: 120 V, single-phase, 2-wire system

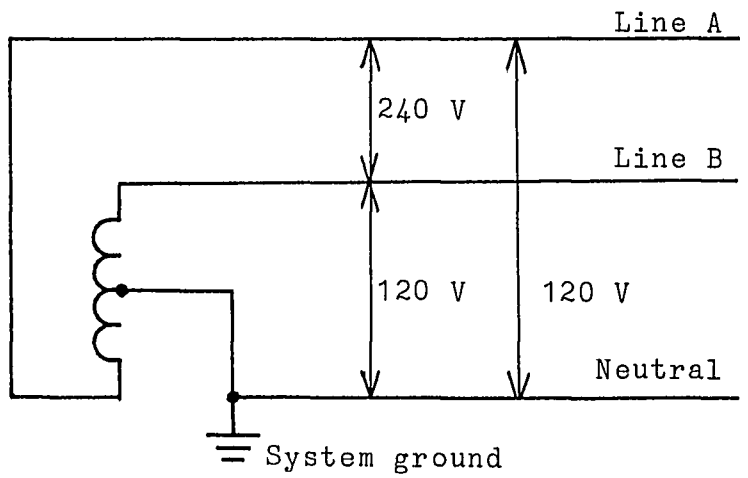


Figure 2-2: 120/240 V, single-phase, 3-wire system

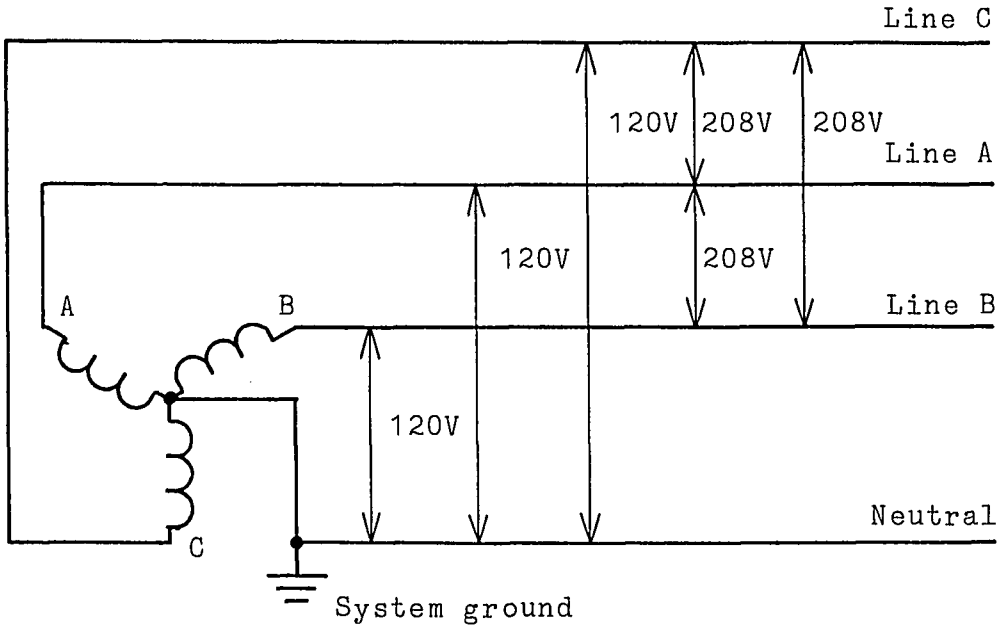


Figure 2-3: 120/208 V, 3-phase, 4-wire system

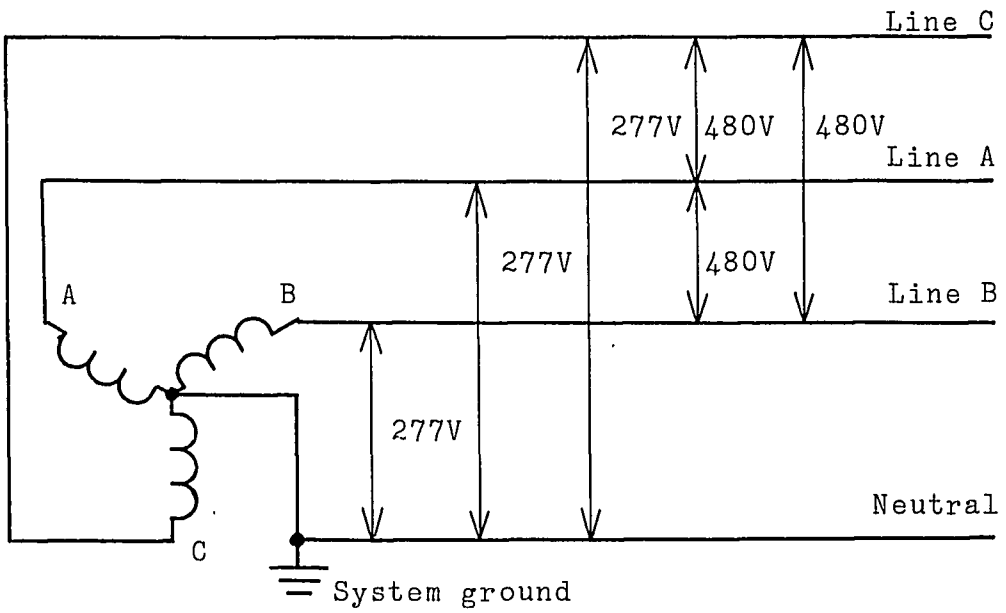


Figure 2-4: 277/480 V, 3-phase, 4-wire system

industrial buildings. Many fluorescent lamps are designed to work off 277 V. This is identical in configuration to the 120/208 V system.

(5) 240/416 V, 3-phase, 4-wire system (see Figure 2-5): This is used only in very large commercial or industrial buildings. This system is again identical in configuration to the 120/208 V system.

(6) 120/208/240 V, 3-phase, 4-wire delta system (see Figure 2-6): This system is used where the motor load represents a large part of the total load. One of the transformers is center-tapped to establish a neutral which is connected to the system ground.

In this paper all wires, except the neutral, may be called lines and each line is designated as Line A, Line B or Line C. Sometimes the configuration of a system is expressed by using the number of lines. For example, 3-phase, 4-wire system may be called 3-phase, 3-line system or just 3-line system.

2.2 Power Measurement

Power is defined to be the time rate of flow of energy. The power in a one port circuit at any instant, called the instantaneous power p(t), equals the product of the instantaneous current, i(t), in the circuit and the instantaneous voltage, v(t), across its terminal at

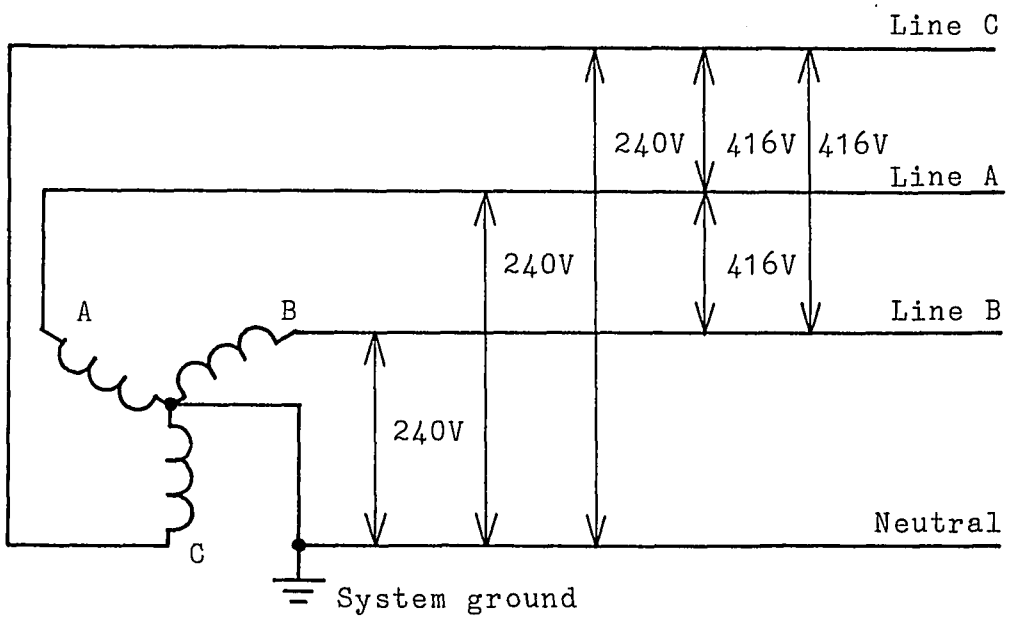


Figure 2-5: 240/416 V, 3-phase, 4-wire system

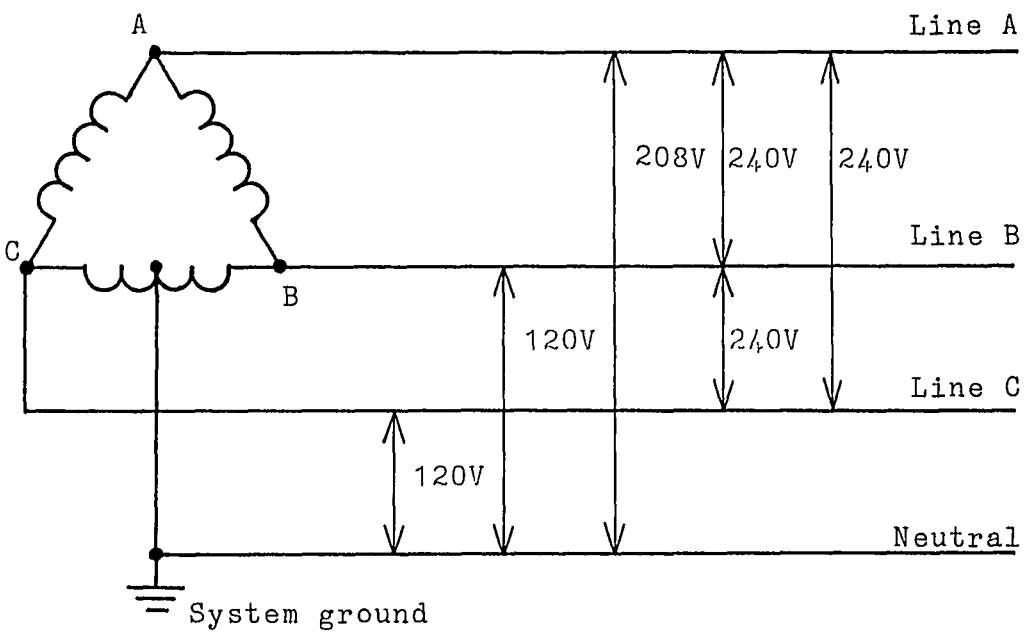


Figure 2-6: 120/208/240 V, 3-phase, 4-wire delta system

that moment; that is,

$$p(t) = v(t)i(t) \quad . \tag{2-1}$$

The average power P, often just called power, is the time average of the instantaneous power in the circuit. If steady-state conditions exist, the power is given by

$$P = \frac{1}{T}\int_0^T p(t)\, dt \quad , \tag{2-2}$$

where T is the period of the instantaneous power.

Since the voltage waveform of normal power distribution systems is 60 Hz sinusoidal, only this voltage waveform is considered for the analysis of power in this work. Thus, the instantaneous voltage of a system is expressed as

$$v(t) = V_m \cos(\omega_o t + \theta) \quad , \tag{2-3}$$

or

$$v(t) = \sqrt{2}\, V \cos(\omega_o t + \theta) \quad , \tag{2-4}$$

where V_m, V and θ are the peak value, the root-mean-square (rms) value and the phase angle of the voltage of the system respectively and $\omega_o = 2\pi 60$. Usually the current in power distribution systems can be assumed to be stable for some short duration because the current in such

systems is not continually changing. Moreover, for this stable duration, the current in the systems can be assumed to be periodic with a period that is the same as that of the voltage of the systems. Thus, the stable periodic current for some duration is used for the calculation of the power for that duration. In this case the instantaneous power is also stable.

The simplest case is one in which the current in a system is 60 Hz sinusoidal. the instantaneous current is expressed as

$$i(t) = I_m \cos(\omega_o t + \varphi) \quad , \tag{2-5}$$

or

$$i(t) = \sqrt{2}\, I \cos(\omega_o t + \varphi) \quad , \tag{2-6}$$

where I_m, I and φ are the peak value, the rms value and the phase angle of the current. The power is calculated by using equations 2-1 and 2-2. The result of the calculation is given by

$$P = \frac{1}{2} V_m I_m \cos(\varphi - \theta) \quad , \tag{2-7}$$

or

$$P = V I \cos(\varphi - \theta) \quad . \tag{2-8}$$

In this case the power is determined by V (V_m), I (I_m)

and the phase angle difference between the voltage and the current of the system.

Because of nonlinear loads on power distribution systems the current in the systems is generally a distorted wave. Because of periodicity the current can be expressed by the Fourier series,

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t + \varphi_n) \quad , \qquad (2\text{-}9)$$

where I_0 is the magnitude of the dc component and I_n and φ_n are the peak value and the phase angle of the nth harmonic of the current. The instantaneous power is given by

$$\begin{aligned} p(t) &= V_m \cos(\omega_0 t+\theta)\{I_0 + \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t+\varphi_n)\} \\ &= V_m I_0 \cos(\omega_0 t+\theta) \\ &\quad + \sum_{n=1}^{\infty} V_m I_n \cos(\omega_0 t+\theta)\cos(n\omega_0 t+\varphi_n) \\ &= V_m I_0 \cos(\omega_0 t+\theta) \\ &\quad + \tfrac{1}{2} V_m I_1 \{\cos(\varphi_1-\theta)+\cos(2\omega_0 t+\varphi_1+\theta)\} \\ &\quad + \tfrac{1}{2} V_m I_2 \{\cos(\omega_0 t+\varphi_2-\theta)+\cos(3\omega_0 t+\varphi_2+\theta)\} \\ &\quad + \text{ - - - - } \\ &\quad + \tfrac{1}{2} V_m I_n \{\cos((n-1)\omega_0 t+\varphi_n-\theta) \\ &\qquad\qquad +\cos((n+1)\omega_0 t+\varphi_n+\theta)\} \\ &\quad + \text{ - - - - } \end{aligned} \quad . \qquad (2\text{-}10)$$

The power is calculated by integrating the instantaneous power for the one period of 60 Hz, T_0, to yield

$$
\begin{aligned}
P &= \frac{1}{T_o}\int_0^{T_o} p(t)\,dt \\
&= \frac{1}{T_o}\Big[\int_0^{T_o} V_m I_o \cos(\omega_o t+\theta)\,dt \\
&\qquad + \frac{1}{2}\int_0^{T_o} V_m I_1 \cos(\varphi_1-\theta)\,dt \\
&\qquad\qquad + \frac{1}{2}\int_0^{T_o} V_m I_1 \cos(2\omega_o t+\varphi_1+\theta)\,dt \\
&\qquad + \frac{1}{2}\int_0^{T_o} V_m I_2 \cos(\omega_o t+\varphi_2-\theta)\,dt \\
&\qquad\qquad + \frac{1}{2}\int_0^{T_o} V_m I_2 \cos(3\omega_o t+\varphi_2+\theta)\,dt \\
&\qquad + \quad - \quad - \quad - \quad - \\
&\qquad + \frac{1}{2}\int_0^{T_o} V_m I_n \cos((n-1)\omega_o t+\varphi_n-\theta)\,dt \\
&\qquad\qquad + \frac{1}{2}\int_0^{T_o} V_m I_n \cos((n+1)\omega_o t+\varphi_n+\theta)\,dt \\
&\qquad + \quad - \quad - \quad - \quad - \qquad\qquad \Big] \\
&= \frac{1}{2T_o}\int_0^{T_o} V_m I_1 \cos(\varphi_1-\theta)\,dt \\
&= \frac{1}{2} V_m I_1 \cos(\varphi_1-\theta) \quad , \qquad\qquad (2\text{-}11)
\end{aligned}
$$

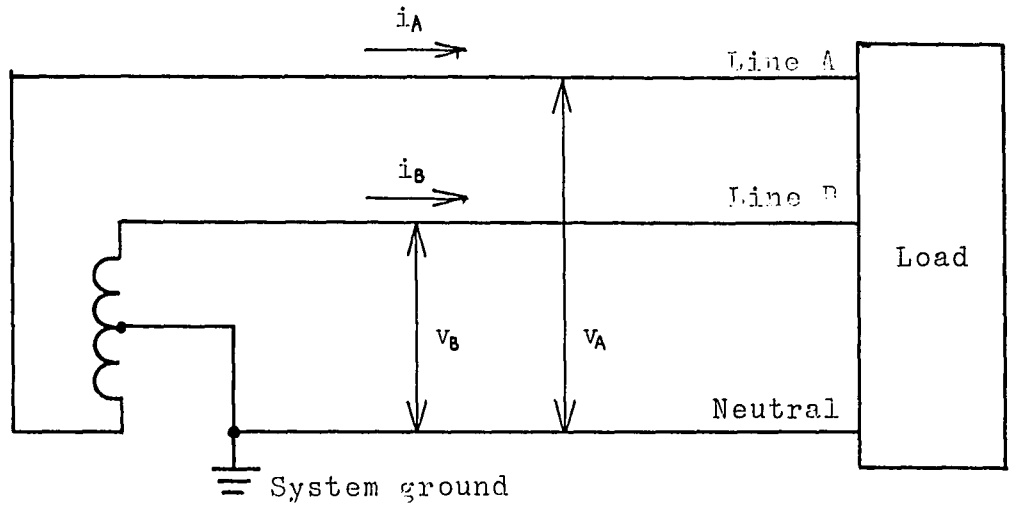
where $\int_o^{T_o}\cos(n\omega_o t+\alpha)dt=0$ is used. This equation shows the same result as the 60 Hz sinusoidal current case, equation 2-7; that is, the power in power distribution systems is determined by only the voltage waveform and the 60 Hz component of the current waveform of the systems. Moreover, comparing equations 2-10 and 2-11 the

power in power distribution systems is exactly the same as the dc component of the instantaneous power.

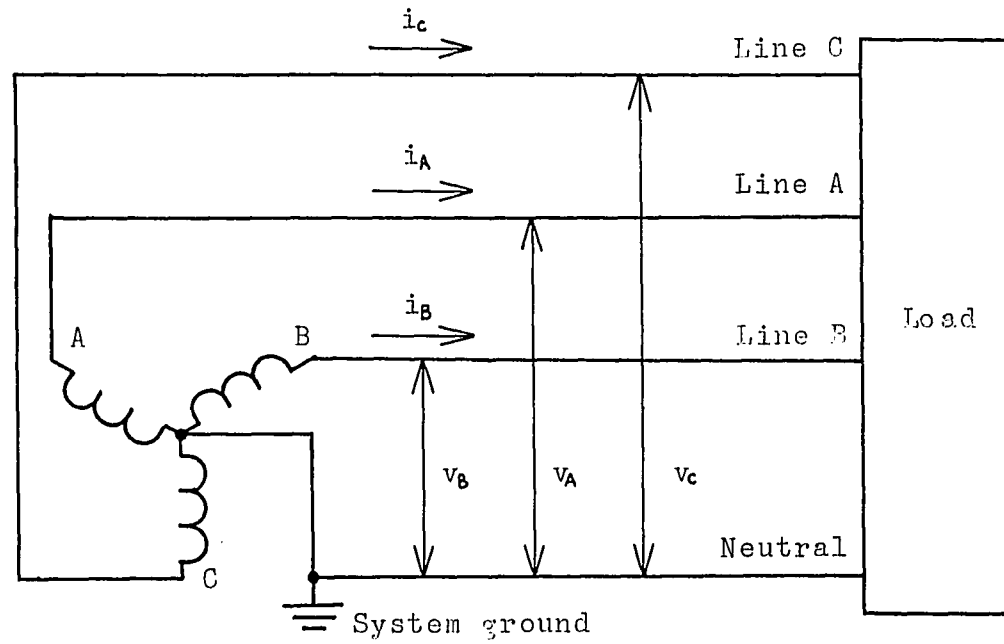
For a system with more than two wires, there are many ways to connect loads. According to the discussion up to now, it seems that it may be troublesome to measure the total power of such a system. Thus, a convenient theorem of power measurement of a multiconductor or polyphase power distribution system is next introduced.

> "Blondel's Theorem: The total power delivered to a load system by means of n conductors is given by the algebraic sum of the indications of n wattmeters so inserted that each of the n wires cotains one wattmeter current-coil, its potential coil being connected between that wire and some point of the system in common with all the other potential coils; if that common junction of the potential leads is on one of the n wires, the total power is obtainable from the indications of n-1 wattmeter elements. [3]"

In other words, the total power can be calculated from voltages between lines and the neutral (common) and the currents in the lines. Applications to the single-phase, 3-wire system and the 3-phase, 4-wire system are shown in Figure 2-7. The total power of these systems are calculated by



(a) single-phase, 3-wire system case



(b) 3-phase, 4-wire system case

Figure 2-7: Measurement for the total power calculation

(a) single-phase, 3-wire system case

$$P = \frac{1}{T_o}\int_0^{T_o} v_A\, i_A\, dt + \frac{1}{T_o}\int_0^{T_o} v_B\, i_B\, dt \quad , \text{ or} \qquad (2\text{-}12)$$

(b) 3-phase, 4-wire system case

$$P = \frac{1}{T_o}\int_0^{T_o} v_A\, i_A\, dt + \frac{1}{T_o}\int_0^{T_o} v_B\, i_B\, dt + \frac{1}{T_o}\int_0^{T_o} v_c\, i_c\, dt \quad . \qquad (2\text{-}13)$$

3. Transformers

3.1 Transformer Equivalent Circuit

The power monitor circuit uses transformers for voltage and current measurment of power distribution systems. There are several advantages of the use of transformers. However, the characteristics of real transformers differ from these of ideal ones and are quite important factors for the power measurement. In this chapter the characteristics, especially transfer characteristics, are discussed.

Before real transformers are discussed ideal transformers are considered. The circuit representation of an ideal transformer is shown in Figure 3-1. There are two lossless windings, the primary with N_p turns, and the secondary with N_s turns, and an ideal core whose hypothetical material has a linear B-H curve with infinite permeability. Under these conditions no leakage flux escapes from the core, and the total flux is proportional to the net magnetomotive force. The voltage and current relationships between the primary and the secondary are

$$v_s = (N_s/N_p) v_p = N v_p \quad , \qquad (3-1)$$

and

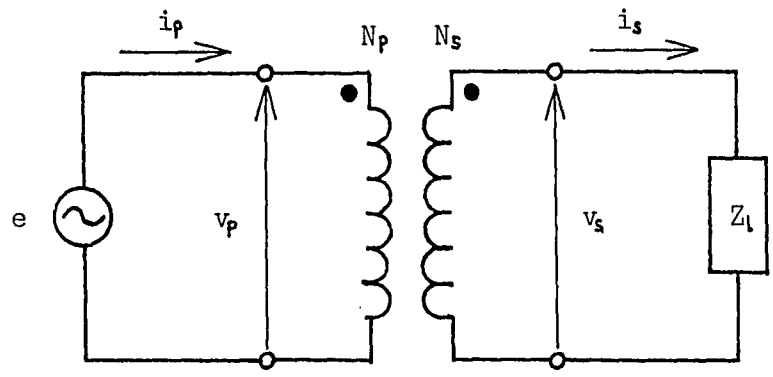


Figure 3-1: Circuit representation of an ideal transformer

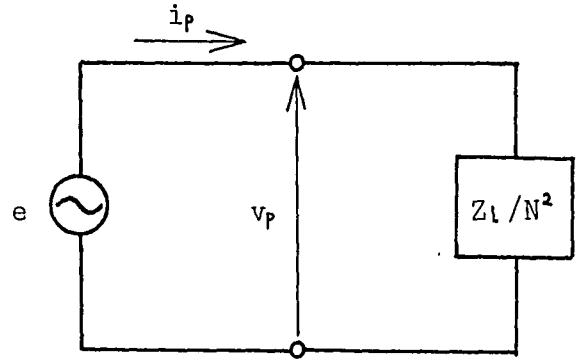


Figure 3-2: Equivalent circuit of Figure 3-1

$$i_P = (N_S/N_P) i_S = N i_S \quad , \qquad (3\text{-}2)$$

where v_P, v_S, i_P and i_S are the primary voltage, the secondary voltage, the primary current and the secondary current respectively, and N is the secondary-to-primary turns ratio,

$$N \triangleq N_S/N_P \quad . \qquad (3\text{-}3)$$

Using these relationships the various circuit elements can be referred to either as the primary or secondary by multiplying or dividing by the square of the secondary-to-primary turns ratio, N^2. For instance, the equivalent circuit of Figure 3-1 viewed from the primary circuit is shown in Figure 3-2.

Because of equations 3-1 and 3-2 the voltage or current of power distribution systems can be measured using ideal transformers. When the primary winding is connected between a line and the neutral, the voltage of the line is sensed by measuring the secondary voltage (see Figure 3-3). In this case the transformer is called an instrument voltage transformer or just a voltage transformer, (VT). When the primary winding is inserted in a line the current in the line is sensed by measuring the secondary current (see Figure 3-3). Note that the secondary load in this case should be resistive. A

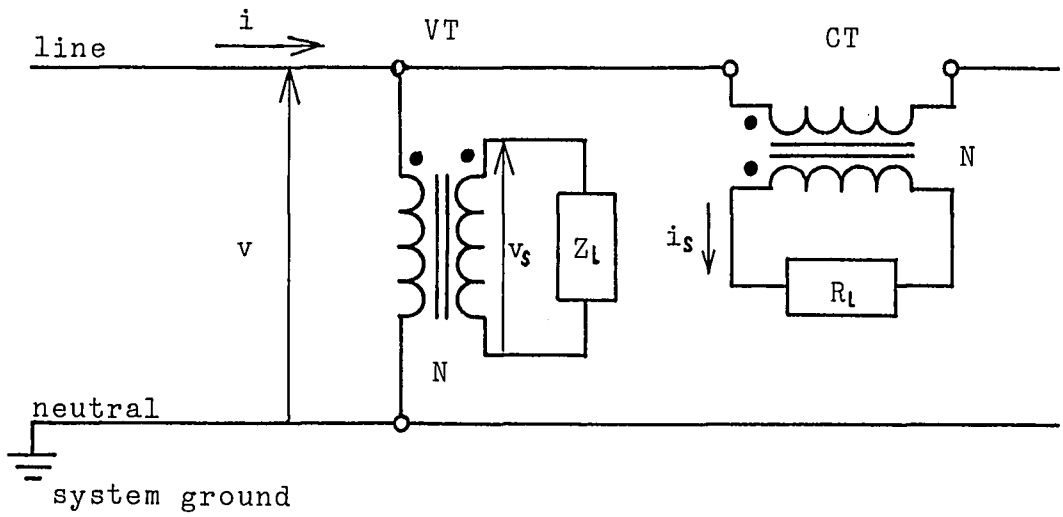


Figure 3-3: Instrument transformers in the power distribution system

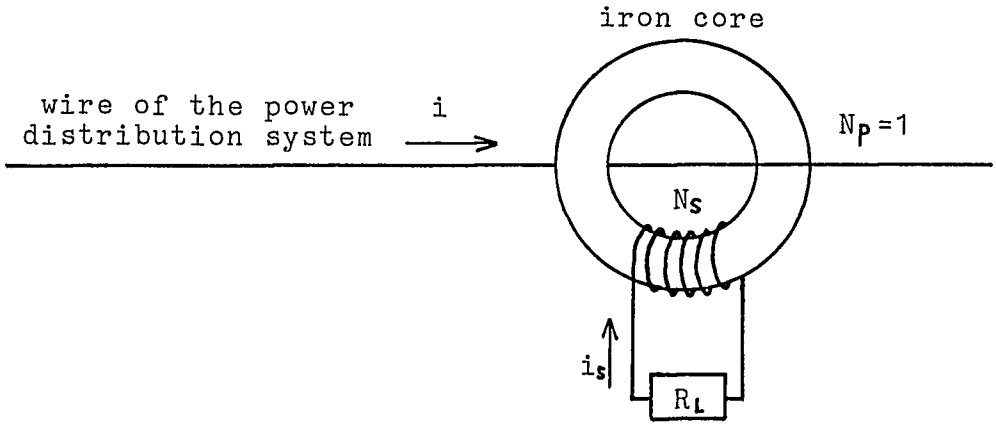


Figure 3-4: Current transformer

transformer for this use is called an instrument current transformer or just a current transformer, (CT). In many cases an iron core with a secondary winding is used so that a wire in the system is encircled by this iron core and becomes the primary winding of a CT (see Figure 3-4). The primary winding of this CT is one, and the wire does not have to be cut. Insertion of a transformer affects voltage and current of the power distribution system since the secondary load of the transformer is also the load of the system. Therefore, the secondary load and N are chosen carefully so that the effect of transformer insertion is reduced.

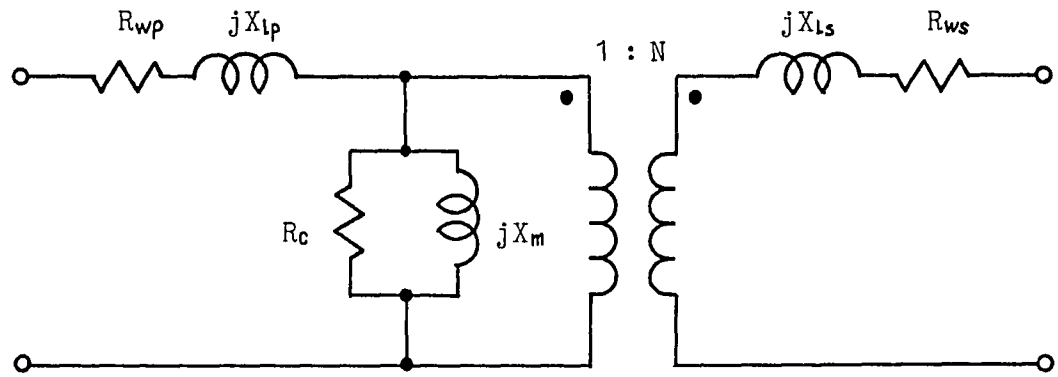
There are several advantages to using transformers in the power distribution system. These are:

- VT's permit low-voltage measurement of high-voltage systems.
- CT's provide a means for reducing large values of current to lower values of current or voltage across the secondary load resistance.
- Transformers supply the insulation between power distribution systems and the power monitor circuit. Therefore, the power monitor circuit can be employed safely.
- Transformers provide a high degree of

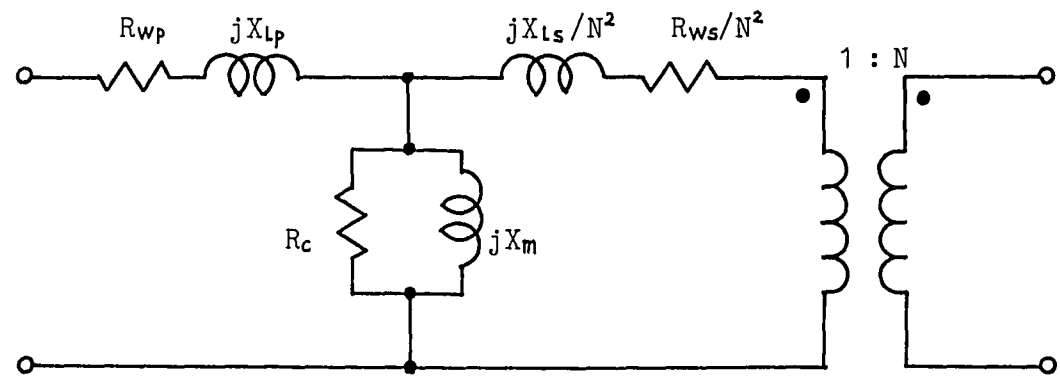
flexibility in locating the power monitor circuit.

A real transformer differs from an ideal one in several respects. The iron core is nonlinear, with finite permeability and hysteresis, and the windings have some resistance. Not all the flux linking the windings goes through the core. The approximate linear equivalent circuit is shown in Figure 3-5(a). Because of the iron core's nonlinearity each element in the equivalent circuit changes when frequency, voltage or current of the primary circuit changes. The resistances R_{wp} and R_{ws} represent copper losses of the primary and secondary winding. The resistance R_c accounts for core losses caused by eddy currents and hysteresis. The reactances X_{lp} and X_{ls} represent the leakage reactances of the primary and secondary winding. The magnetizing reactance X_m is caused by the magnetizing current. Both the leakage and the magnetizing reactance reflect the iron core's finite permeability. The transformer in the equivalent circuit is an ideal one. Figures 3-5(b) and (c) show the equivalent circuits with secondary or primary elements referred to on the opposit side.

The behavior of a real transformer at a certain frequency, voltage and current is predictable from its

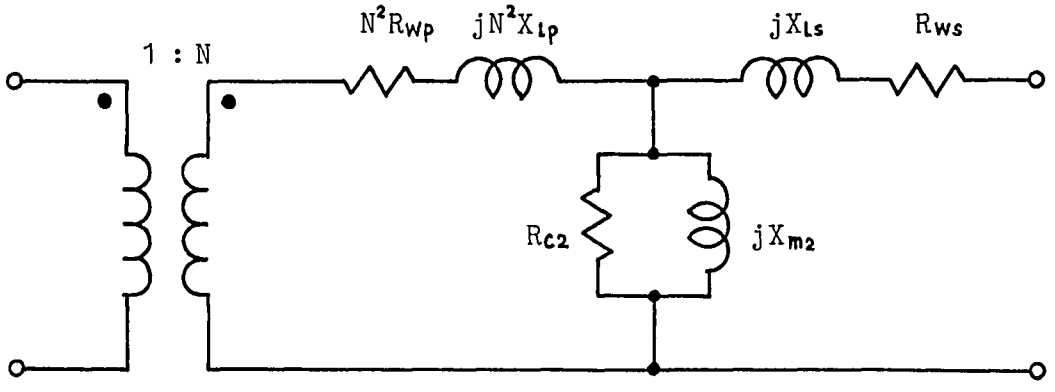


(a) equivalent circuit of a real transformer



(b) equivalent circuit with secondary elements referred to the primary

Figure 3-5: Equivalent circuit of a real transformer (1 of 2)



(c) equivalent circuit with primary elements referred to the secondary

Figure 3-5: Equivalent circuit of a real transformer (2 of 2)

equivalent circuit. When a certain frequency and magnitude of voltage (current) is applied to the primary winding, and a certain resistance load is connected to the secondary winding, the following characteristics can be noted:

- The secondary voltage (current) is less than that of the ideal transformer case.
- The secondary voltage (current) waveform might be phase shifted a small amount from the primary voltage (current) waveform.

Thus, unlike the ideal transformer case, it is difficult to calculate the primary voltage or current of the real transformer by measuring the secondary voltage or current.

Consider the case in which real transformers are used to measure the voltage or current of a power distribution system. First, it will be assumed that the insertion of the transformer which is used for measuring the voltage or the current does not have any effect on the system. This is a good assumption because the load of the system is usually a much more dominant factor of the voltage and the current of the system than that of the transformer. Therefore, the primary voltage or current of the transformer is the same as that of the

system without this transformer.

Because the voltage of a power distribution system is a steady 60 Hz sinusoid, one equivalent circuit is sufficient to describe the behavior of the VT. Thus, the voltage of the system can be sensed by measuring the secondary voltage. The current of a system is generally a distorted wave and varries widely in magnitude. Since a transformer has different transfer characteristics for different frequency components, or different current levels, the secondary current waveform of a CT can differ from the current waveform of the system. It is impossible to precisely determine the current of the system by measuring the secondary current of a CT. Some compensation circuit of the CT's transfer characteristics may be needed in order to employ the CT for the current measurement.

3.2 Transfer Characteristics of Current Transformers

In this section the transfer characteristics of a CT are analyzed and experimentally verified. This work is required because current measurements of a power distribution system depends critically on the transfer characteristics of the CT. When the current of a system is measured by a CT the current of the system should be the input of the CT, that is, the primary current of the

CT. The output of the CT is usually taken as the voltage across a load resistance connected across the secondary winding. Normally the primary is one turn. Thus, the transfer function, gain G and phase shift α, between the primary current and the secondary voltage of the CT with one primary turn is considered. When the phase shift α is expressed by the time delay t_α the transfer function is given by Ge^{-st_α}.

An Amprobe Instrument Model SA60EN-1 CT is used for this analysis. The main features of this CT are as follows,

- nominal primary current range: 0 - 300 A (with one primary turn),
- maximum secondary output: 90 mA (continuous duty),
- secondary turns: 2325,
- recommended secondary load: 30 Ω resistor.

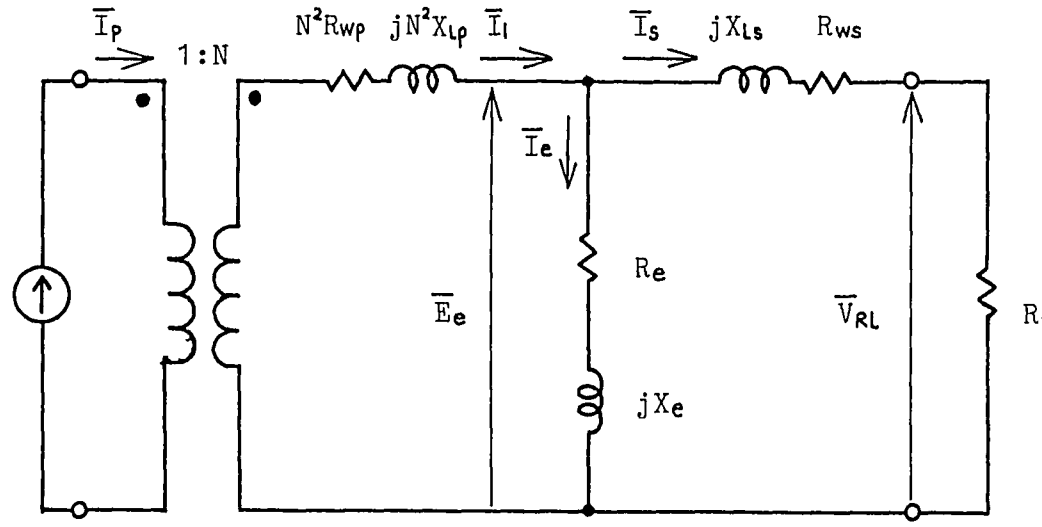
Two different methods are used to determine the transfer characteristics of this CT. One is based upon direct testing and the other upon calculations using the equivalent circuit. Although direct testing is sufficient to determine the transfer characteristics of a particular CT, predicting the transfer characteristics using the equivalent circuit can be helpful for direct

testing.

In the laboratory it is difficult to obtain 0 - 300 A currents (the nominal primary current range of the CT) over the frequency range which is needed to test the CT directly. For convenience, the primary turns of the CT can be increased in order to decrease the secondary-to-primary turns ratio. With this approach smaller primary currents are required to test the CT.

Before the effect of changing the primary turns on the transfer characteristics of a CT is discussed the equivalent circuit of a CT is introduced [4]. The equivalent circuit whose load is resistive is shown in Figure 3-6. This circuit is obtained from the one in Figure 3-5(c) whose parallel circuit of R_{c2} and X_{m2} are changed to series form. The voltage and current are denoted in phasor form whose magnitudes are rms values. In this paper the capital letter of voltage or current with a bar denoted the phasor and the capital letter without a bar denotes the rms values. Moreover, the small letter denotes the instantaneous value. These notations are understood unless otherwise stated. For instance, the primary current $\bar{I}_p$ is expressed as $\bar{I}_p = I_p e^{j\varphi}$.

Since the transformer in the equivalent circuit is ideal, the primary current $\bar{I}_p$ is transformed perfectly,



$\bar{I}_P$: primary current

$\bar{I}_S$: secondary current

$\bar{I}_I$: primary current referred to the secondary

$\bar{I}_e$: secondary excitation current

$\bar{V}_{RL}$: secondary voltage

$\bar{E}_e$: secondary excitation voltage

N: secondary-to-primary turns ratio

$R_{WP}+jX_{LP}$: primary winding impedance

$R_{WS}+jX_{LS}$: secondary winding impedance

R_e+jX_e: secondary excitation impedance

R_L : load resistance

Figure 3-6: Equivalent circuit of a current transformer

with no ratio or phase error, to the current $\bar{I}_1$, the primary current referred to the secondary,

$$\bar{I}_1 = \bar{I}_p / N \quad . \tag{3-4}$$

The secondary current $\bar{I}_s$, and the secondary exciting current $\bar{I}_e$, are determined by $\bar{I}_1$ and the circuit elements, irrespective of the values of the primary winding impedance, R_{wp} and X_{lp}. That is, the relation between the primary current and the secondary current does not depend on the primary winding impedance. The number of the primary turns affects only the secondary-to-primary turns ratio N and the impedance inserted into the primary circuit by the CT. Thus, decreasing N can make it possible to test the CT with smaller primary currents than the nominal primary current, all with no effect on the transfer characteristics.

Next, the calculation of the CT's transfer characteristics from the equivalent circuit is discussed. In the equivalent circuit $\bar{I}_1$ flows into the secondary exciting impedance, R_e and X_e; this current is called the secondary excitation current, $\bar{I}_s$. It is evident that the secondary excitation voltage $\bar{E}_e$ is a function of $\bar{I}_e$, R_e and X_e. Also, $\bar{I}_s$ is a function of $\bar{E}_e$ and the secondary winding impedance, R_{ws} and X_{ls}, and load resistor R_L. Thus, once $\bar{I}_e$, R_e, X_e, R_{ws}, X_{ls} and R_L are

determined $\bar{I}_p$ ($\bar{I}_1$) and $\bar{I}_s$ can be calculated and therefore the transfer characteristics between $\bar{I}_p$ and $\bar{I}_s$ can be determined. Because of CT's nonlinearity R_e and X_e are functions of $\bar{I}_e$, and R_{ws} and X_{Ls} are functions of $\bar{I}_s$.

Using this equivalent circuit the transfer characteristics at various current levels of 60 Hz are determined. These transfer characteristics of the CT are important for the power measurement of the power distribution system. The reason is given later. First, several assumptions are made to facilitate calculation and measurement. One is that R_{ws} is a constant for any reasonable current levels of operation. Moreover, R_{ws} at 60 Hz is assumed to be the same as the dc resistance of R_{ws}. Because of the skin effect of conductors R_{ws} is a function of frequency. However, R_{ws} at 60 Hz does not much differ from the ac resistance of R_{ws}. Therefore, using the dc resistance of R_{ws} in circuits operated at 60 Hz does not introduce segnificant error. X_{Ls} is also assumed to be a constant for any reasonable current levels because X_{Ls} is smaller and more linear than X_e. Thus, measurement of R_e and X_e vs. $\bar{I}_e$ and X_{Ls} at 60 Hz can determine the CT's transfer characteristics at 60 Hz.

The circuit used to determine R_e, X_e and X_{Ls} is shown in Figure 3-7, where the primary is left open and a 60 Hz sinusoidal voltage source $\bar{E}$ is connected to the

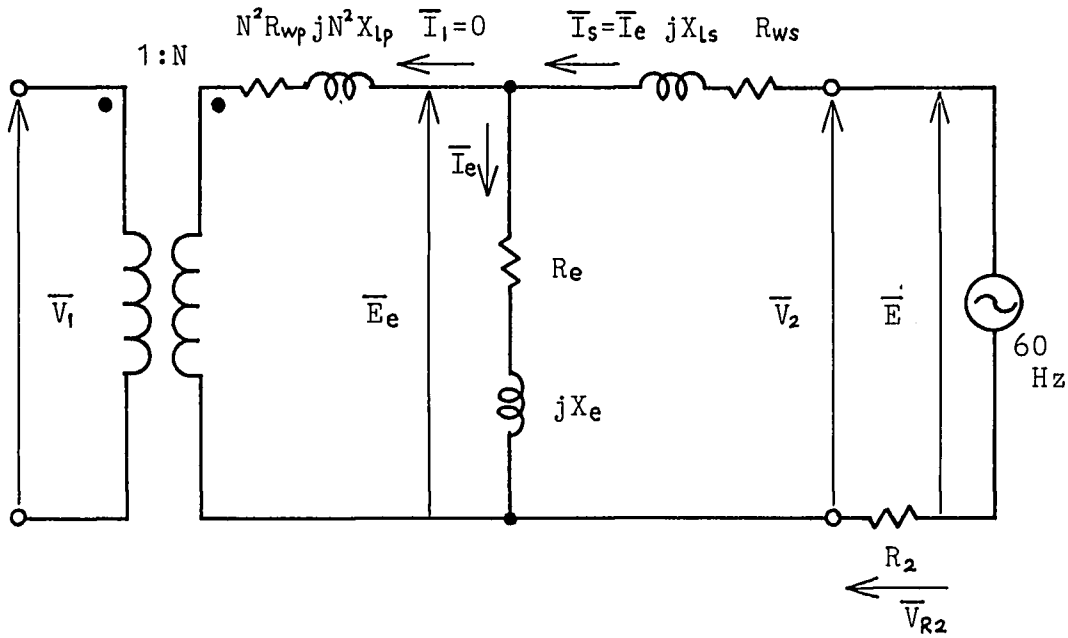


Figure 3-7: Circuit used to determine the excitation impedance and the secondary leakage reactance of the CT

secondary. Because the primary is open, $\overline{I}_1$ is zero, $\overline{I}_S$ equals $\overline{I}_e$, and $\overline{V}_1$ equals $\overline{E}_e/N$. In this circuit voltages $\overline{E}$, $\overline{V}_{R2}$, $\overline{V}_2$ and $\overline{V}_1$ can be measured. R_2 and the dc resistance of Rws is measured directly. R_2 is not necessarily equal to the secondary load resistance R_L. From these measurements I_e, R_e, X_e and X_{LS} are calculated as follows:

$$I_e = V_{R2}/R_2 \tag{3-5}$$

$$R_e = (V_2/I_e)\cos[\sin^{-1}((E/V_2)\sin\zeta)]-R \tag{3-6}$$

$$X_e = \sqrt{(N^2V_1^2/I_e)-R_e} \tag{3-7}$$

$$X_{LS} = (E/I_e)\sin\zeta-X_e \quad , \tag{3-8}$$

where ζ is the phase angle difference between $\overline{E}$ and $\overline{V}_{R2}$. The details of these calculations are given in Appendix A. Using these calculated values the equivalent circuit for a certain secondary excitation current level is determined. The currents $\overline{I}_1$ and $\overline{I}_S$ can also be determined as follows:

$$I_S = I_e\sqrt{R_e^2+X_e^2}/\sqrt{(R_L+P_{WS})^2+X_{LS}^2} \tag{3-9}$$

$$I_1 = \sqrt{(I_e\cos(\xi-\nu)+I_S)^2 + (I_e\sin(\xi-\nu))^2} \tag{3-10}$$

$$\alpha = \sin^{-1}((I_o/I_1)\sin(\xi-\nu)) \quad , \tag{3-11}$$

where α is the phase angle difference between $\overline{I}_S$ and $\overline{I}_1$, and

$$\nu = \tan^{-1}(X_{Ls} / (R_{ws}+R_L)) \quad \text{and}$$

$$\xi = \tan^{-1}(X_e / R_e) \quad .$$

The positive α means that $\overline{I}_s$ leads $\overline{I}_1$. The details of these calculations are again given in Appendix A. Then the primary current of the CT with one primary turn, $\overline{I}_{p1}$, is given by

$$\overline{I}_{p1} = N_s \overline{I}_1 \quad . \tag{3-12}$$

The relation between the primary current $\overline{I}_{p1}$ and the secondary voltage $\overline{V}_{RL}$ can be calculated. The recommended secondary load for the Amprobe SA60EN-1 CT is a 30 Ω resistor. Thus, the following work will assume this value load. The gain G is given by

$$G = 30 I_s / I_{p1} \quad . \tag{3-13}$$

The phase shift equals α because $\overline{V}_{RL}$ and $\overline{I}_s$ are in phase. The positive α means that $\overline{V}_{RL}$ lead $\overline{I}_{p1}$.

The transfer characteristics at various current levels of 60 Hz were determined by the method stated above. For the test circuit a 150.3 Ω resistor was used as R_2 and a 60 Hz, 120 V power line run through a step-down transformer was used as the sinusoidal voltage source in the secondary circuit. The primary turns was set at 200, yielding N=11.625. The secondary winding

resistance, R_{ws}, was measured to be 174.5 Ω, which is the dc resistance value. The nominal secondary leakage reactance, X_{ls}, at 60 Hz was determined to be 180 Ω by averaging the calculated values at various current levels. The resulting transfer characteristic curves of gain G vs. the primary current I_{pl}, and phase shift α vs. the primary current I_{pl}, are shown in Figures 3-11 and 3-12 respectively. These transfer characteristic curves will be discussed later.

Finally, the transfer characteristics of the CT were tested directly. The test circuit is shown in Figure 3-8. To permit the use of small primary currents this is done by making the primary turns equal to N_p instead of only one. The primary current of the CT with one primary turn, $\overline{I}_{pl}$, can be inferred from the measurement of $\overline{V}_R$; that is,

$$I_{pl} = N_p V_{Rl} / R_l \quad , \tag{3-14}$$

and the phase angle of $\overline{I}_{pl}$ equals that of $\overline{V}_{Rl}$. The secondary voltage, with a load of 30 Ω, $V_{RL=30}$, is given by

$$V_{RL=30} = 30 V_{RL} / R_L \quad , \tag{3-15}$$

and the phase angle of $\overline{V}_{RL=30}$ equals that of $\overline{V}_{RL}$. The gain G is then

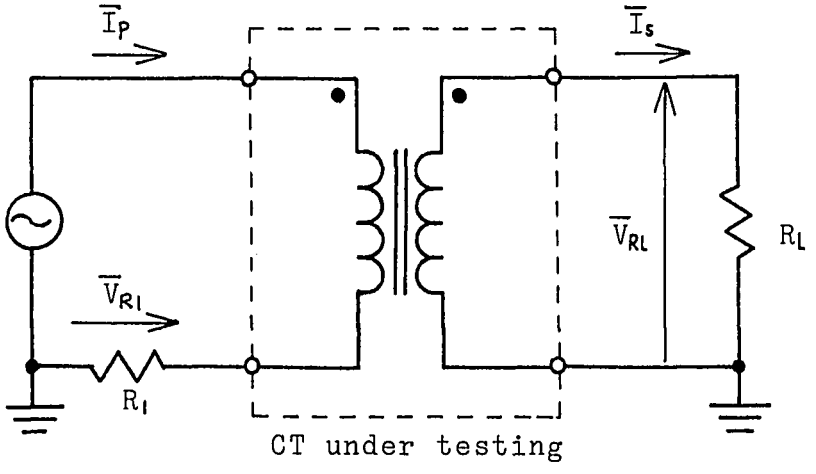


Figure 3-8: Test circuit used to measure the CT's transfer characteristics

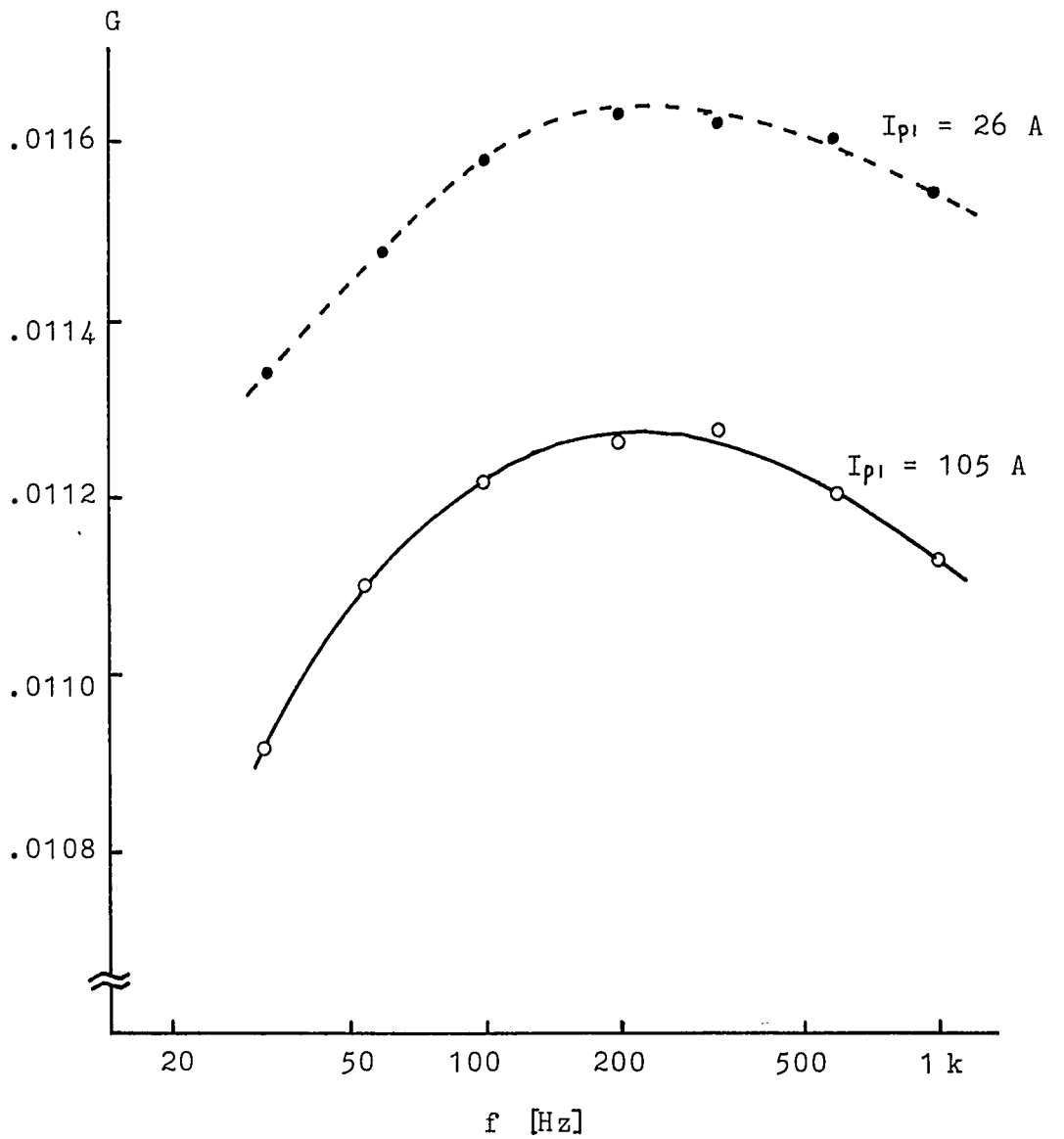
$$G = V_{RL=30}/I_{pl} \quad . \qquad (3\text{-}16)$$

The phase shift α equals that between $\overline{V}_{Rl}$ and $\overline{V}_{RL}$. When $\overline{V}_{RL}$ leads $\overline{I}_{pl}$, α is positive.

The transfer characteristics at various frequencies were determined by direct testing. Resistors of 3.8 Ω and 31.6 Ω were used as R_l and R_L respectively. A sinusoidal wave generator and a power amplifier were used as the power supply in the primary circuit. The primary turns was fixed at 200. The resulting transfer characteristics, gain G vs. frequency, f, and phase shift α vs. frequency, are shown in Figures 3-9 and 3-10 respectively. In each figure there are shown two curves showing the characteristic at a different primary current level I_{pl}. Gain G and phase shift α are seen to be nonlinear functions of frequency f and current level I_{pl}.

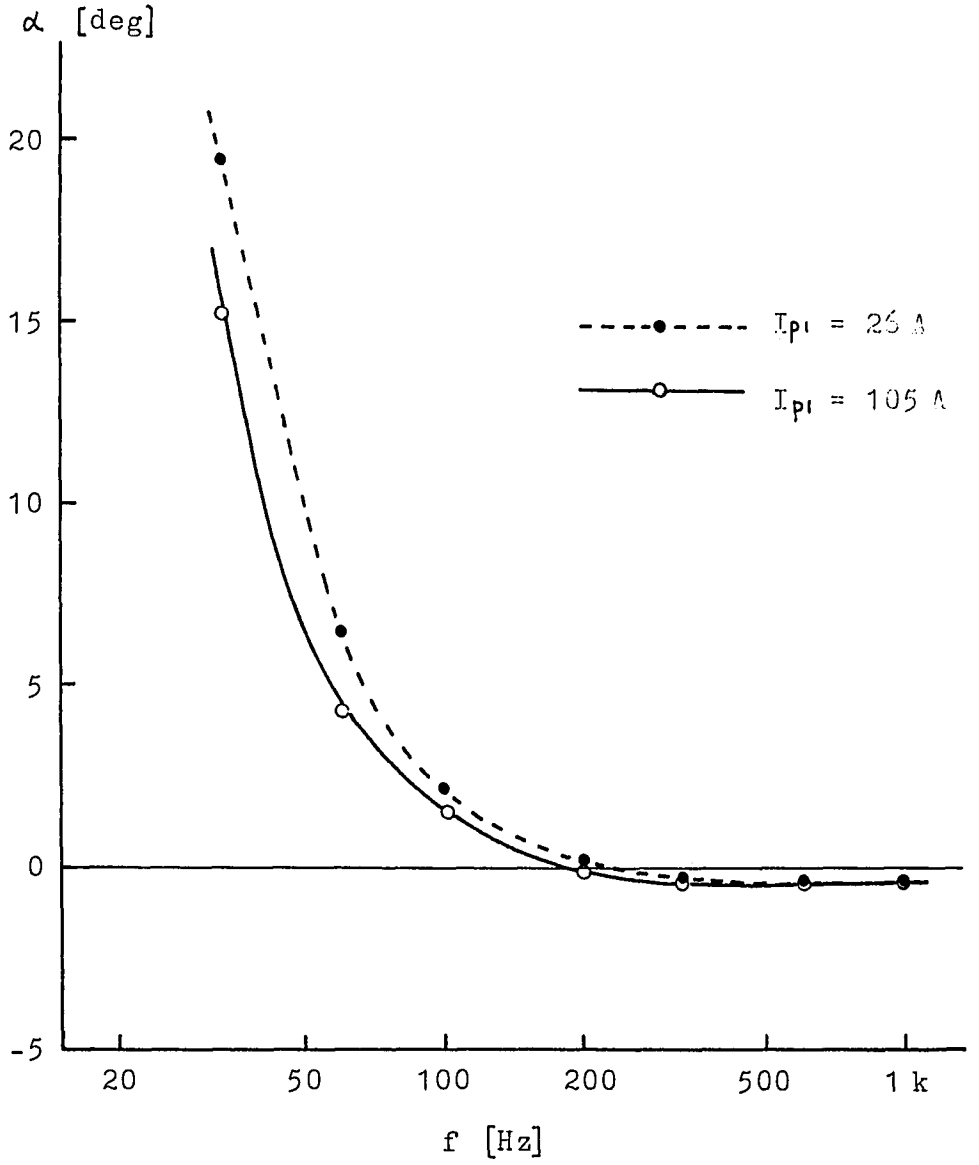
When the primary current is a distorted sinusoidal wave this CT can not transform the primary waveform to the secondary circuit perfectly. In this case it is impossible to determine the primary current precisely from the secondary voltage.

The transfer characteristics at various current levels at 60 Hz were also measured. Here resistors of 5.1 Ω and 31.6 Ω were used as R_l and R_L respectively. The 60 Hz, 120 V power line and a step-down transformer



gain G vs. frequency f

Figure 3-9: Gain of the SA60EN-1 CT

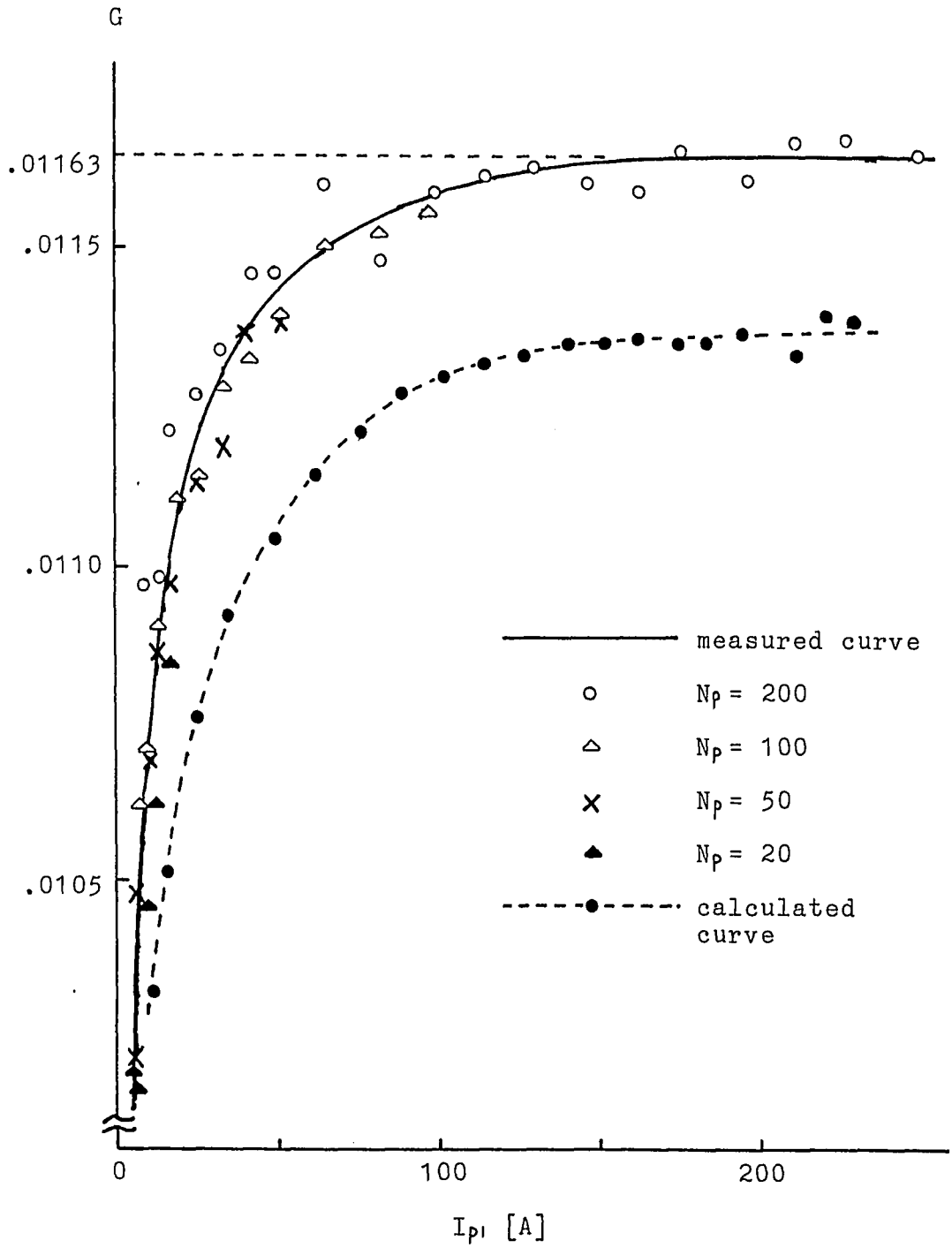


phase shift α vs. frequency f

Figure 3-10: Phase shift of the SA60EN-1 CT

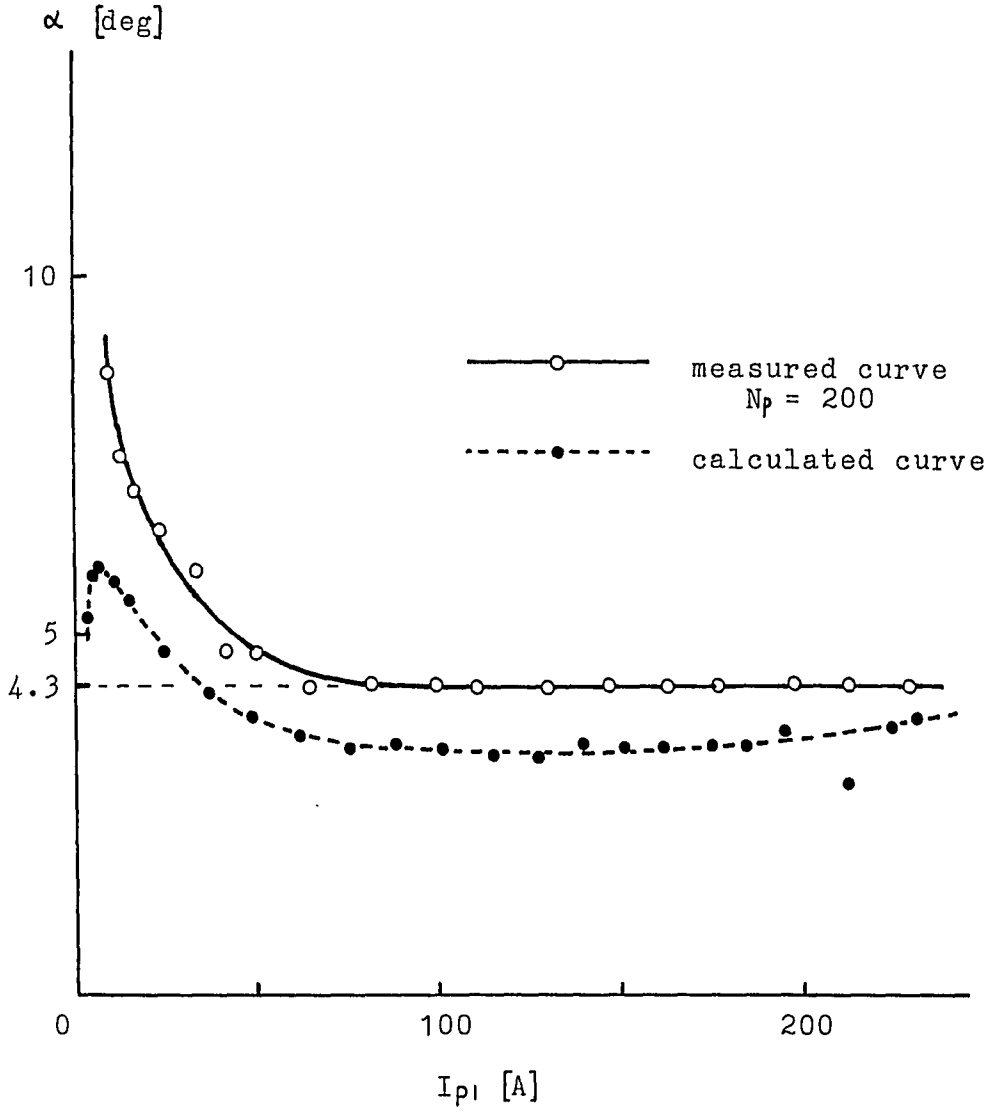
were used as the voltage supply in the primary circuit. Four different primary turns, 200, 100, 50 and 20, were used to test the CT. Testing at small current levels, using fewer primary turns, gives more reliable transfer characteristics of the CT. The resulting transfer characteristics, gain G vs. the primary current I_{pi} and phase shift α vs. the primary current I_{pi}, are shown in Figures 3-11 and 3-12 respectively. Phase shift α is shown only for the N_p=200 case since identical results are obtained for the lesser turns used. Thus, only phase shift α, when N_p equals 200, is shown. These figures also show the calculated characteristics as determined from the equivalent circuit. The directly measured characteristics and the calculated ones show good agreement. Therefore, the measurement is considered to be reasonable. An analysis of the effect of these transfer characteristics on the current measurement will be done in section 4.3.

Although different CT's of the same model usually have slightly different characteristics, any CT of this model is assumed to have exactly the same characteristics for convenience sake.



gain G vs. primary current I_{p1}

Figure 3-11: Gain of the SA60EN-1 CT



phase shift α vs. primary current I_{pl}

Figure 3-12: Phase shift of the SA60EN-1 CT

4. Power Monitor Circuit Overview

4.1 Circuit Specification

A few target power distribution systems were selected as the first step in the design of the power monitor circuit. The power monitor will be able to measure power in any of the following four systems:

- 120 V, single-phase, 2-wire system,
- 120/240 V, single-phase, 3-wire system,
- 120/208 V, 3-phase, 4-wire system,
- 277/480 V, 3-phase, 4-wire system.

This selection will cover the systems in the typical office, commercial or light industrial building.

The current range of these target systems is now discussed. The range depends on the device used for current measurement, i.e. the CT. An Amprobe SA60EM-1 CT, whose transfer characteristics are determined in section 3.2, is employed. The specification of this CT shows that the maximum secondary current is 90 mA - continuous duty. The current in power distribution systems is often steady for some short period. Therefore, 90 mA is considered to be the maximum secondary current, I_{Smax}. A 30 Ω resistor is used as the secondary load, R_L. The resulting maximum secondary

voltage, V_{RLmax}, is computed as $V_{RLmax}=R_L I_{smax}=2.7$ [V]. Consulting the gain curve in Figure 3-11 shows that the gain G, at the high current level, is 0.01163. Thus, the maximum primary current, I_{plmax}, which induces V_{RLmax}, is computed as $I_{plmax}=V_{RLmax}/0.01163=230$ [A]. Instead of the nominal primary current range of the CT, the current range 0 - 230 A is adopted as the primary current range. Therefore, the current range of the target systems is 0 - 230 A.

The range 0 - 230 A restricts only the rms value of the current. Since the rms value does not have information about the peak value one more restriction on the current of the target systems is made for convenience. The peak value of the current is limited to 325 A, which is the peak value of the 230 A sinusoidal current.

The voltage of power distribution systems varies slightly from the nominal value. Therefore, ±10 % of the nominal voltage is considered as a variable in the input of the circuit. The change of the voltage may cause a change in the current. Thus, a ±10 % current is also considered a variable in the input of the circuit.

Next, outputs of the power monitor circuit are considered. The circuit displays total power of the power distribution system. The power of each line in the

system, which is useful in ascertaining the balance of the system, is also displayed. The measured power is displayed in decimal format for easy reading. The range of the power is 0 to 231,267 W. This maximum value is the total power in the 277/480 V, 3-phase, 4-wire system with voltage of 10 % above the nominal value and current of 10 % above the maximum value. Because of the wide range three significant digits with a floating decimal point are displayed. This output indication shows the power in units of kW. The number of significant digits displayed depends on the measurement accuracy. This number of digits will be decided after the measurement accuracy is further studied. Usually three significant digits of power are sufficient for most power distribution systems.

Selection for the specific power distribution system being measured is done by manual switches. That is, the manual switches select the number of the lines and the voltage of the system. Moreover, the manual switches select which power option is to be displayed; that is, total power or power of Line A, Line B or Line C. It may happen that the selected line whose power is to be displayed is not a part of the system under measurement. In this case, no-line-indication is displayed.

4.2 Basic Circuit Diagram

The basic block diagram of the power monitor circuit is shown in Figure 4-1. This diagram is not the complete one because the transformer's transfer characteristics have not been considered. The complete block diagram is shown after consideration of the transformer's transfer characteristics. Explanations of the building blocks of this diagram are now presented.

(A) Voltage and current measurement circuit: This circuit measures voltage and current of the power distribution system. There are, at most, three lines in the power distribution system. According to the discussion in section 2.2 at most three pairs of voltage and current are needed to measure the total power in the system. A VT whose maximum primary voltage is greater than 277 V can be used to measure voltages of 277 V and 120 V on the line. Therefore, three pairs of VT's and CT's are employed. This configuration can also measure power in the 2-wire and 3-wire system.

The multiplier constants K_V and K_I are used for voltage trimming of the VT and CT outputs to match the input of the following power computation circuit. The constant K_V is controlled by the manual switches because the voltage of the line is 120 V or 277 V.

The power monitor circuit measures power in one line

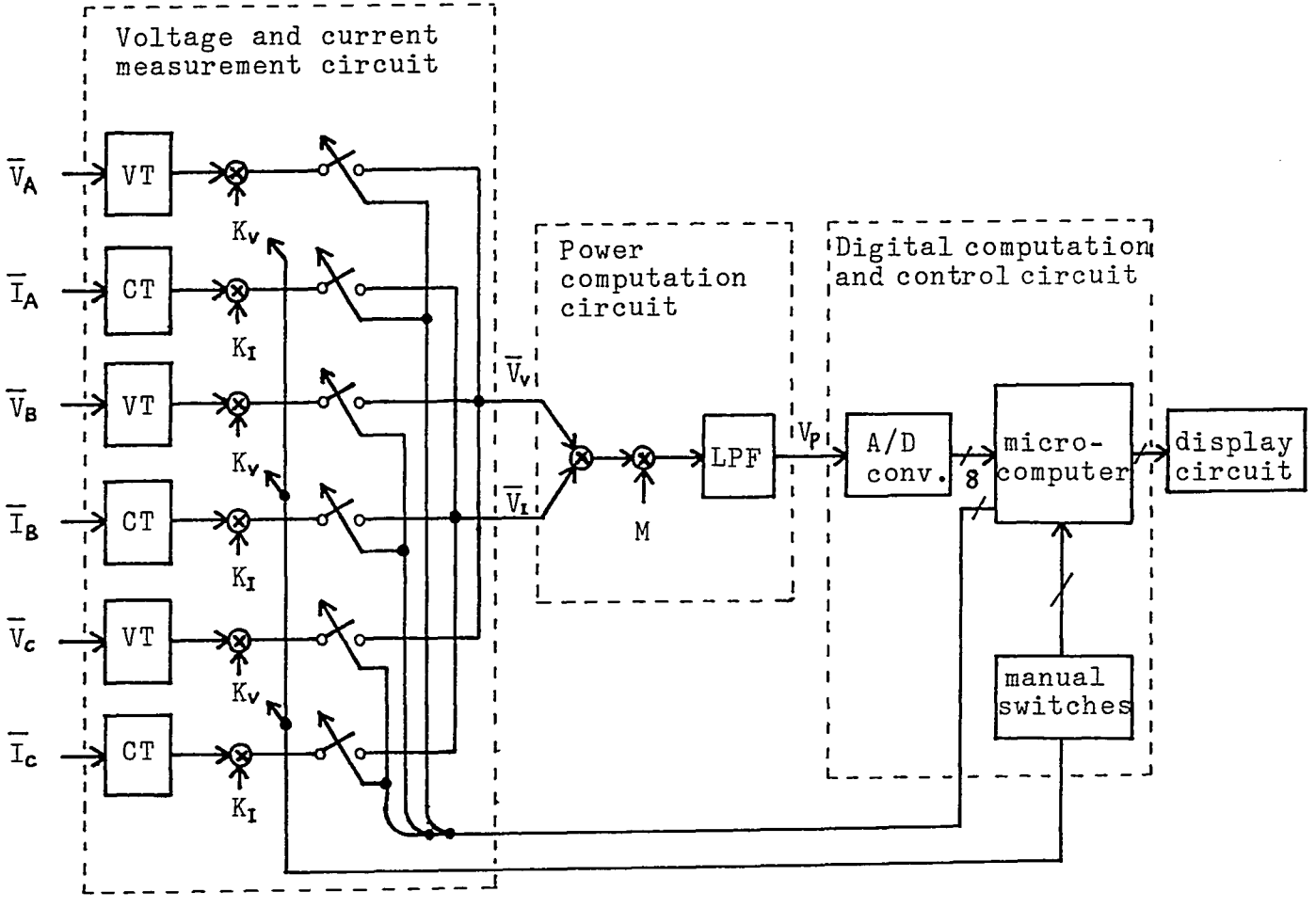


Figure 4-1: Basic block diagram of the power monitor circuit

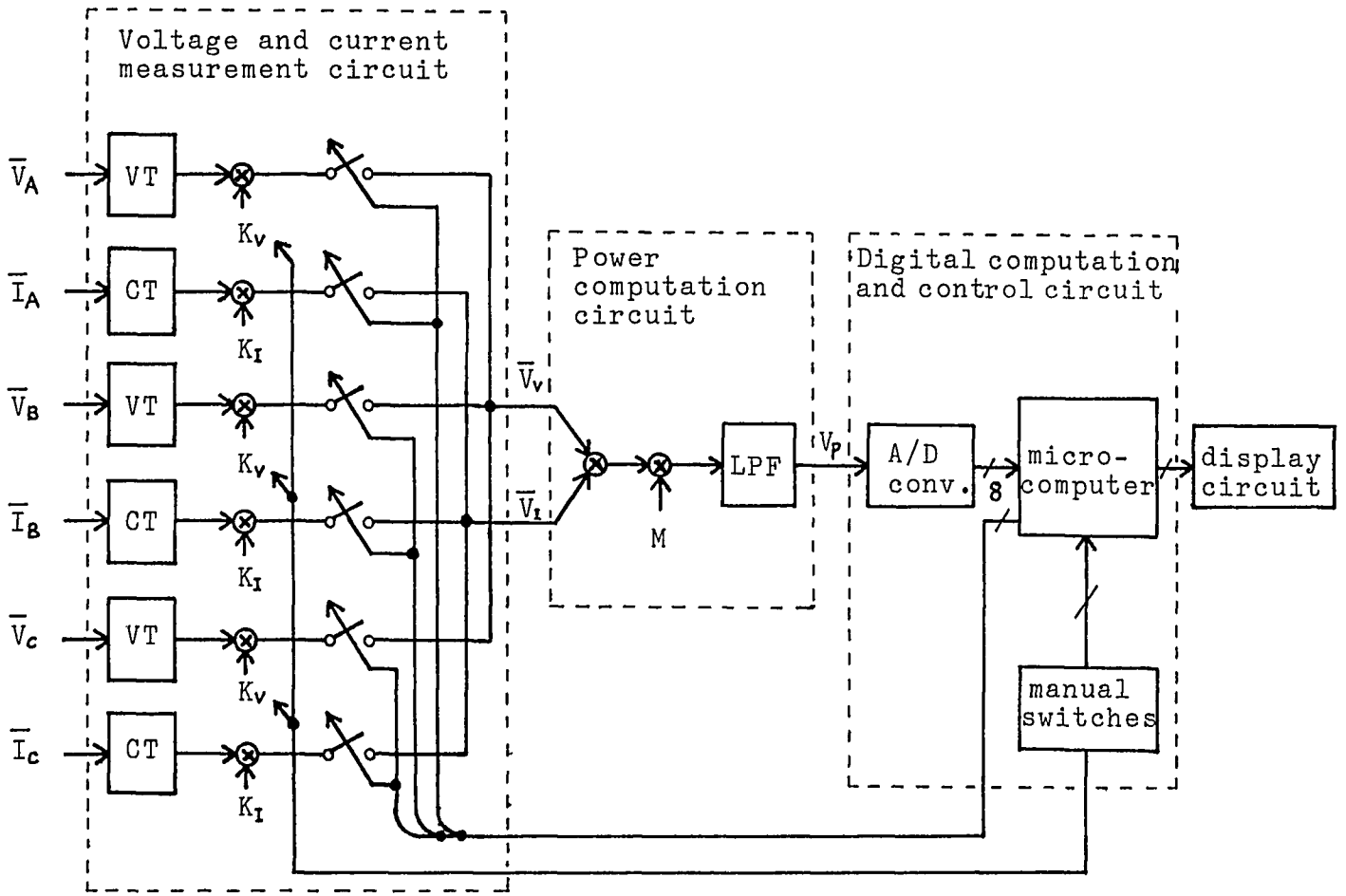


Figure 4-1: Basic block diagram of the power monitor circuit

at a time. Three pairs of analog switches select one line at a time in which the power is measured. Since instantaneous power in the lines is stable for some duration, power in the lines remains constant for this duration. The "on" time of these switches should be shorter than this duration. These switches are controlled by the microcomputer, which is explained later.

(B) Power computation circuit: This circuit multiplies the input voltages, $\overline{V}_V$ and $\overline{V}_I$, and extracts the dc component from this product. The constant M adjusts the output voltage of this circuit to match the voltage of the input of the following digital computation and control circuit.

According to the discussion in section 2.2, the power in power distribution systems equals the dc component of the instantaneous power of the system, which furthermore is determined only by the voltage waveform and the 60 Hz component of the current waveform of the system. Therefore, the output of this circuit, V_p, is proportional to the power in the system if inputs of this circuit satisfy the following conditions:

- $\overline{V}_V$ is proportional to the voltage waveform of the system,

- the 60 Hz component of $\overline{V}_I$ is proportional to that of the current waveform in the system,
- the phase angle difference between $\overline{V}_V$ and the 60 Hz component of $\overline{V}_I$, i.e. δ, are the same as that of the voltage waveform and the 60 Hz component of the current waveform of the system.

However, the outputs of the voltage and current measurement circuit do not precisely satisfy the conditions above because of the transfer characteristics of the transformers. Additional circuits are needed to compensate for the transfer characteristics of the transformers. These additional circuits are discussed in section 4.4.

(C) Digital computation and control circuit: In order to display the measured power in decimal format the output of the power computation circuit must be converted to digital form. Then the resulting digital data is changed to the appropriate form for the following display circuit. There are several methods for this conversion. An analog to digital (A/D) converter and a microcomputer are employed. The microcomputer also controls the other circuits. The operation of the microcomputer is controlled by the manual switches.

(D) Display circuit: This circuit displays the measured power in decimal format. That is, three significant digits and a floating decimal point. The no-line-indication is also displayed.

4.3 Transfer Characteristics of the Basic Circuit Diagram

The block diagram in section 4-2 does not include circuitry to correct for the transfer characteristics of the transformers. The effect, and compensation thereof, of the transformers are discussed from the point of measurement accuracy in the next section. Although the circuit block diagram is not a complete one the transfer characteristics of this circuit block is now determined in order to facilitate the discussion in the next section. The final transfer characteristics of the circuit will be given after the complete circuit block diagram is determined at the end of the next section.

First, the block diagram in Figure 4-1 is divided into two parts, the analog part and the digital part. Let A be the transfer function of the analog part, and B the transfer function of the digital part; that is

$$V_p = A\ P \quad , \tag{4-1}$$

and

$$P' = B\ V_{pd} \quad , \tag{4-2}$$

where P is the power in the power distribution system, P' is the output display of the power monitor circuit, and Vpd is the digital representation of V_p. In order to reduce the measurement error B should be close to the inverse of A. However, A includes the nonlinear transfer characteristics of the CT. The B term is constant unless additional circuits are used to inform the microcomputer of the overall current level in the power distribution system. That is, B is calculated from the inverse of A by assuming constant gain and phase shift of the CT's transfer characteristics. In this section only A is discussed. Consideration of B is left to the next section.

The features of some circuits in the diagram have to be selected in order to determine the transfer characteristics. The A/D converter converts a 0 - 10.24 V analog voltage to an 8-bit digital word. The input range of the power calculation circuit is 0 - 10 V and the output range is also 0 - 10 V. All other analog circuits also work over the voltage range 0 - 10 V.

The block diagram of the transfer characteristics of the analog part is shown in Figure 4-2. In this diagram the VT is represented by the transfer function He^{-st_θ}, where H is the gain and t_θ is the time delay which causes the phase shift from the primary voltage waveform to the

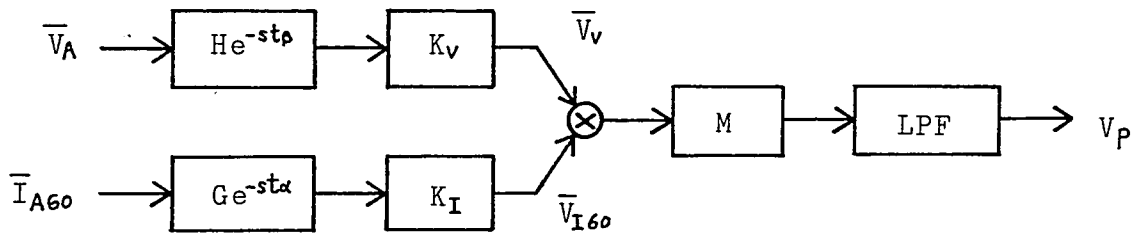


Figure 4-2: Block diagram of the transfer characteristics of the analog part

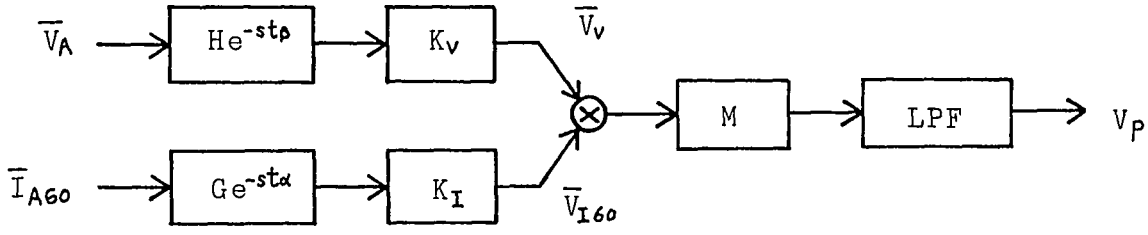


Figure 4-2: Block diagram of the transfer characteristics of the analog part

secondary voltage waveform, β. Since the voltage waveform of the power distribution system is 60 Hz sinusoidal, H and β are the values at 60 Hz. According to the discussion in sections 2.2 and 4.2, V_P is determined only by the voltage waveform and the 60 Hz component of the current waveform of the system. Therefore, only the 60 Hz component of the current waveform $\overline{I}_{A60}$ and $\overline{V}_{I60}$ are considered. The transfer characteristics of the CT are also those at 60 Hz. Although the diagram shows only the case of Line A, exactly the same argument can be used for the other lines.

In this block diagram V_V and V_{I60} are expressed by

$$V_V = H\ K_V\ V_A \quad , \tag{4-3}$$

and

$$V_{I60} = G\ K_I\ I_{A60} \quad . \tag{4-4}$$

According to the discussion in section 4.2 the output of the power computation circuit, V_P, is given by

$$V_P = M\ V_V\ V_{I60} \cos\delta \quad , \tag{4-5}$$

where δ is the phase angle difference between $\overline{V}_V$ and $\overline{V}_{I60}$. Using equations 4-3, 4-4 and 4-5, V_P is expressed as a function of V_A, I_{A60} and δ, i.e.

$$V_P = (H K_V V_A)(G K_I I_{A60}) M \cos \delta \quad . \qquad (4\text{-}6)$$

Since δ is not the phase difference at the input of the circuit, equation 4-6 is not the complete expression for the transfer characteristics of the analog portion. The relation between δ and the phase angle difference of $\overline{V}_A$ and $\overline{I}_{A60}$ will be considered and complete transfer characteristics will be given in the next section.

Next, the constants in equation 4-6 are discussed. First, HK_V is selected. The value of V_A is allowed to vary ±10 % from the nominal value, and the peak voltage of V_V is 10 V. Thus, the following two relations are derived from equation 4-3;

$$120 * 1.1 * \sqrt{2} * H K_V|_{120} = 10 \quad ,$$

and

$$277 * 1.1 * \sqrt{2} * H K_V|_{277} = 10 \quad ,$$

where $HK_V|_{120}$ and $HK_V|_{277}$ are the values of HK_V with 120 V and 277 V systems. Therefore, HK_V is set to

$$H K_V|_{120} = 0.05357 \quad , \qquad (4\text{-}7)$$

or

$$H K_V|_{277} = 0.02321 \quad . \qquad (4\text{-}8)$$

When V_A is the nominal value in both cases V_V is given by

$$V_V = 6.428 \quad . \tag{4-9}$$

The GK_I in equation 4-6 is calculated in the same manner. When I_{A60} is the maximum allowable value of 230+1.1, i.e. 253 A, then

$$G\,K_I = 0.02795 \quad .$$

The G equals 0.01163 for the maximum allowable value of I_{A60} (see Figure 3-11). Therefore, K_I is given by

$$K_I = 2.4 \quad . \tag{4-10}$$

Next, the constant M is selected. The maximum V_p is 10 V. This happens when both V_V and V_{I60} are maximum and δ is zero in equation 4-5. Because the largest peak voltages of V_V and V_{I60} are 10 V the following relation is derived from equation 4-5;

$$(10/\sqrt{2})(10/\sqrt{2})\,M \cos 0 = 10 \quad .$$

Therefore,

$$M = 0.2 \quad .$$

However,

$$M = 0.1967 \qquad (4\text{-}11)$$

is adopted instead of 0.2. This value of M is selected to reduce the error of digital calculation since the microcomputer can only deal with a finite number of digits of data. Details of this argument can be found in the next section. In this case V_P still satisfies the output range of the power computation circuit.

Using equations 4-6, 4-7, 4-8, 4-10 and 4-11 the next two equations are obtained. For the 120 V system

$$V_P = 0.02529\ G\ V_A\ I_{A60} \cos\delta \quad . \qquad (4\text{-}12)$$

For the 277 V system

$$V_P = 0.01096\ G\ V_A\ I_{A60} \cos\delta \quad . \qquad (4\text{-}13)$$

In both cases V_P with the nominal V_A is given by

$$V_P = 3.035\ G\ I_{A60} \cos\delta \quad , \qquad (4\text{-}14)$$

where equation 4-9 was used.

4.4 Consideration of Current Transformer Nonlinear Transfer Characteristics

The circuit block diagram in Figure 4-1 is valid when $\overline{V}_V$ and $\overline{V}_I$ satisfy the conditions which are discussed in section 4.2. However, $\overline{V}_V$ and $\overline{V}_I$ can not precisely satisfy these conditions because of the transformers'

transfer characteristics. The transformers introduce measurement errors. The voltage of the power distribution system is normally a steady sinusoidal wave. Therefore, the error caused by the VT is easily removed by additional circuits because gain and phase shift are constant. However, the 60 Hz component of the current of the system takes on different magnitude levels. The transfer characteristics of the CT vs. the various primary current levels are nonlinear. Therefore, the error caused by the CT can not be removed perfectly. In order to reduce the error additional circuits, which compensate the effect of the nonlinear transfer characteristics of the CT, are discussed.

Although elimination of error is desirable, it is impossible to completely eliminate the error caused by the CT. Now a criterion of maximum allowable error is needed. The error caused by analog devices in the circuit, including the CT, is converted to the bit error of the digital data by the A/D converter. The output error of the power monitor circuit reflects this bit error. Because of quantization by the A/D converter, the error by analog devices does not necessarily cause the bit error. Conversely, relatively small errors caused by analog devices might cause the bit errors. It is meaningful to express the maximum allowable error caused

by analog devices in terms of the bit error of the digital data.

At most one least significant bit (LSB) of error of the digital data is allowed to be caused by the CT. This error causes at most one level error of the output of the circuit. The input range of the A/D converter is 0 - 10.24 V while the output is 8-bit data. Therefore, the error of V_p caused by the CT may at most be 40 mV, the weight of the LSB.

The following method is used to determine the measurement error of the designed circuit as caused by the CT. First, the transfer characteristics of the designed circuit is determined. In this case the analog part of the circuit is regarded as the ideal one with the exception of the nonlinear transfer characteristics of the CT. The transfer function of the digital part is the inverse of that of the analog part with constant gain G and phase shift α of the CT. The output error of this circuit is caused only by the transfer characteristics of the CT. Now, one more circuit, the ideal circuit, is assumed. The transfer function of the digital part of this circuit is exactly the same as that of the designed circuit. However, the transfer function of the analog part of this circuit is the inverse of that of the digital part. Therefore, the output of this circuit is

an error free version of the power in the power distribution system. If the designed and the ideal circuits were connected to the same power distribution system the difference between the output of the analog part of the two circuits would cause the measurement error of the designed circuit. Therefore, this difference represents the error caused by the CT and should be less than the maximum allowable error.

An additional circuit which compensates for the phase shift of the VT and the CT is designed to reduce errors. In the block diagram in Figure 4-2 the phase shift of the VT, i.e. β, is constant. The phase shift of the CT, i.e. α, is a function of the primary current level, which is shown in Figure 3-12. However, at high current levels α is constant at 4.3°. Now an additional circuit, a phase shifter, is employed following the CT. This circuit shifts phase by $-4.3^{\circ}+\beta$. The block diagram is shown in Figure 4-3. Therefore, δ in equations 4-12, 4-13 or 4-14 is given by

$$\delta = \varphi_{A60} - \theta_A + \alpha - 4.3^{\circ} \quad , \qquad (4\text{-}15)$$

where θ_A and φ_{A60} are the phase angles of the voltage waveform and the 60 Hz component of the current waveform of Line A respectively. The voltage of the line of the power distribution system is 120 V or 277 V. Because

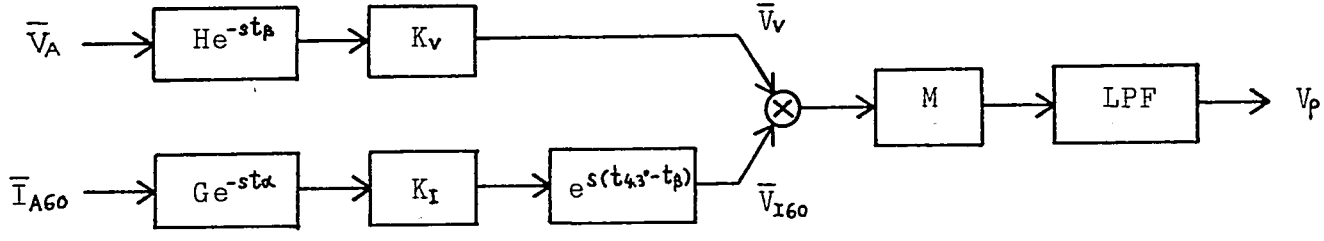


Figure 4-3: Block diagram of the transfer characteristics of the analog part with the phase shifter

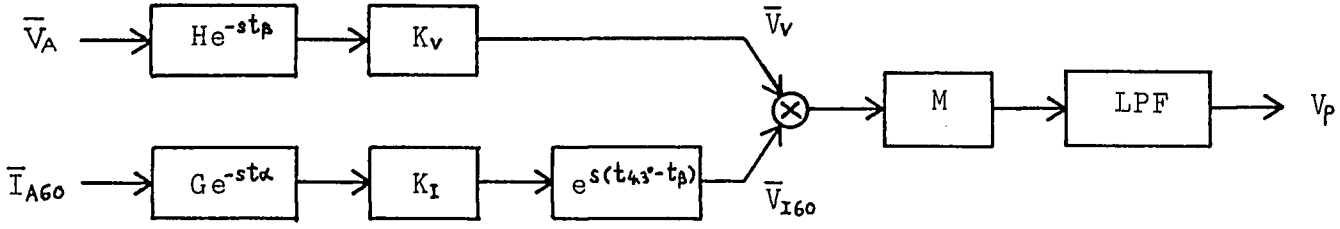


Figure 4-3: Block diagram of the transfer characteristics of the analog part with the phase shifter

different primary voltages of the VT cause different phase shifts this phase shifter can compensate two different phase shifts which are controlled by the manual switches.

Now the error of the circuit with the phase shifter caused by the CT is computed. The transfer characteristics of the analog part of this circuit is given by

$$V_p = 3.035\ G\ I_{A60} \cos(\varphi_{A60} - \theta_A + \alpha - 4.3^\circ) \quad , \qquad (4\text{-}16)$$

where equations 4-14 and 4-15 are used. The transfer function of the digital part of this circuit uses 0.01163 and 4.3° as G and α, which are appropriate for the flat part of the CT transfer characteristic curves. These choices will eliminate errors caused by the CT at high current levels. Therefore, the transfer characteristics of the analog part of the ideal circuit is given by

$$V_{pI} = 0.03530\ I_{A60} \cos(\varphi_{A60} - \theta_A) \quad , \qquad (4\text{-}17)$$

where V_{pI} is the output of the analog part of the ideal circuit. Figures 4-4 and 4-5 show the error of this circuit caused by the CT, $V_p - V_{pI}$ vs. I_{A60} and $V_p - V_{pI}$ vs. $\varphi_{A60} - \theta_A$. Usually the power factor angle of the power distribution system is not greater than 60°. Therefore, values of $\varphi_{A60} - \theta_A$ greater than 60° are not calculated.

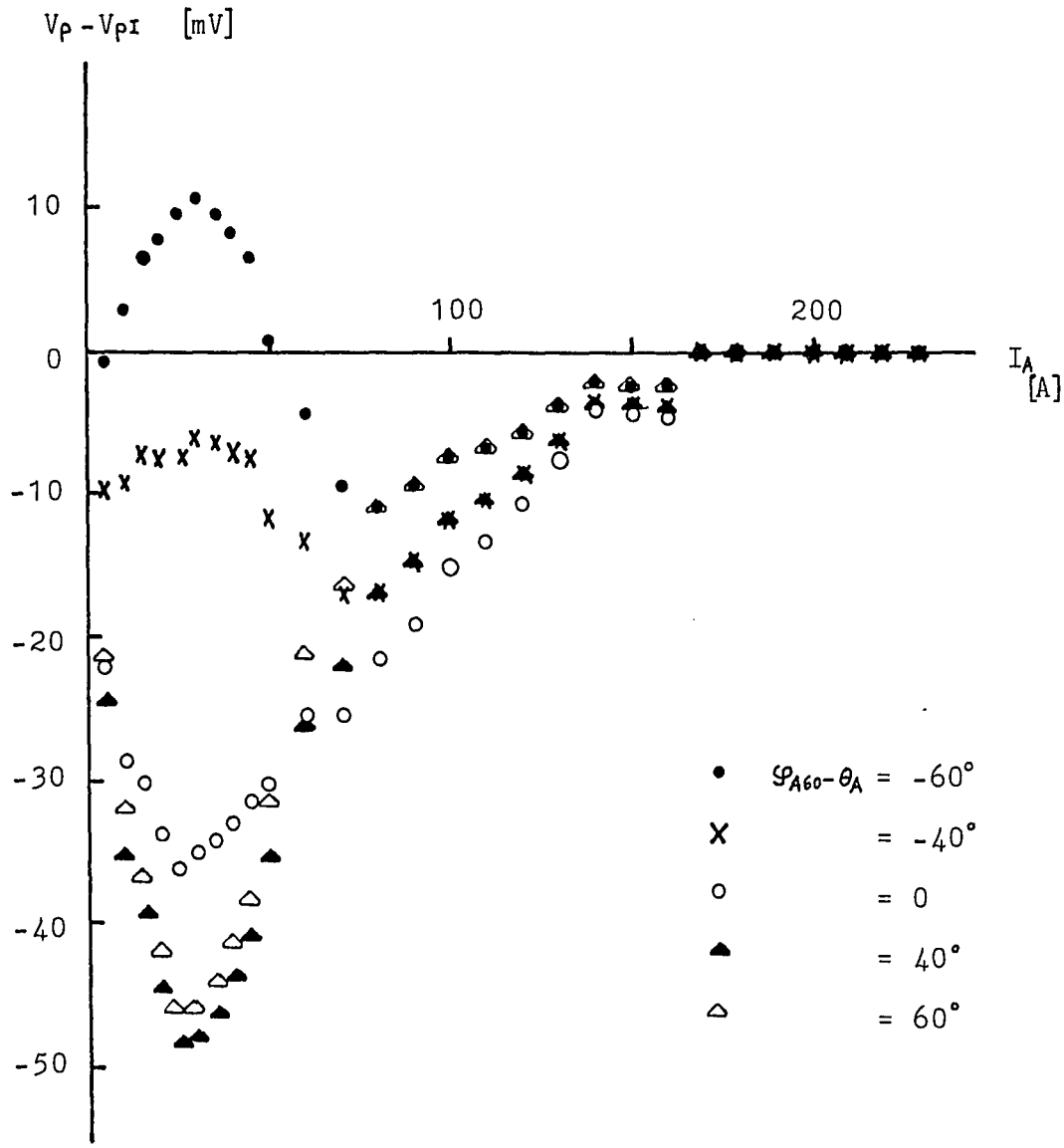
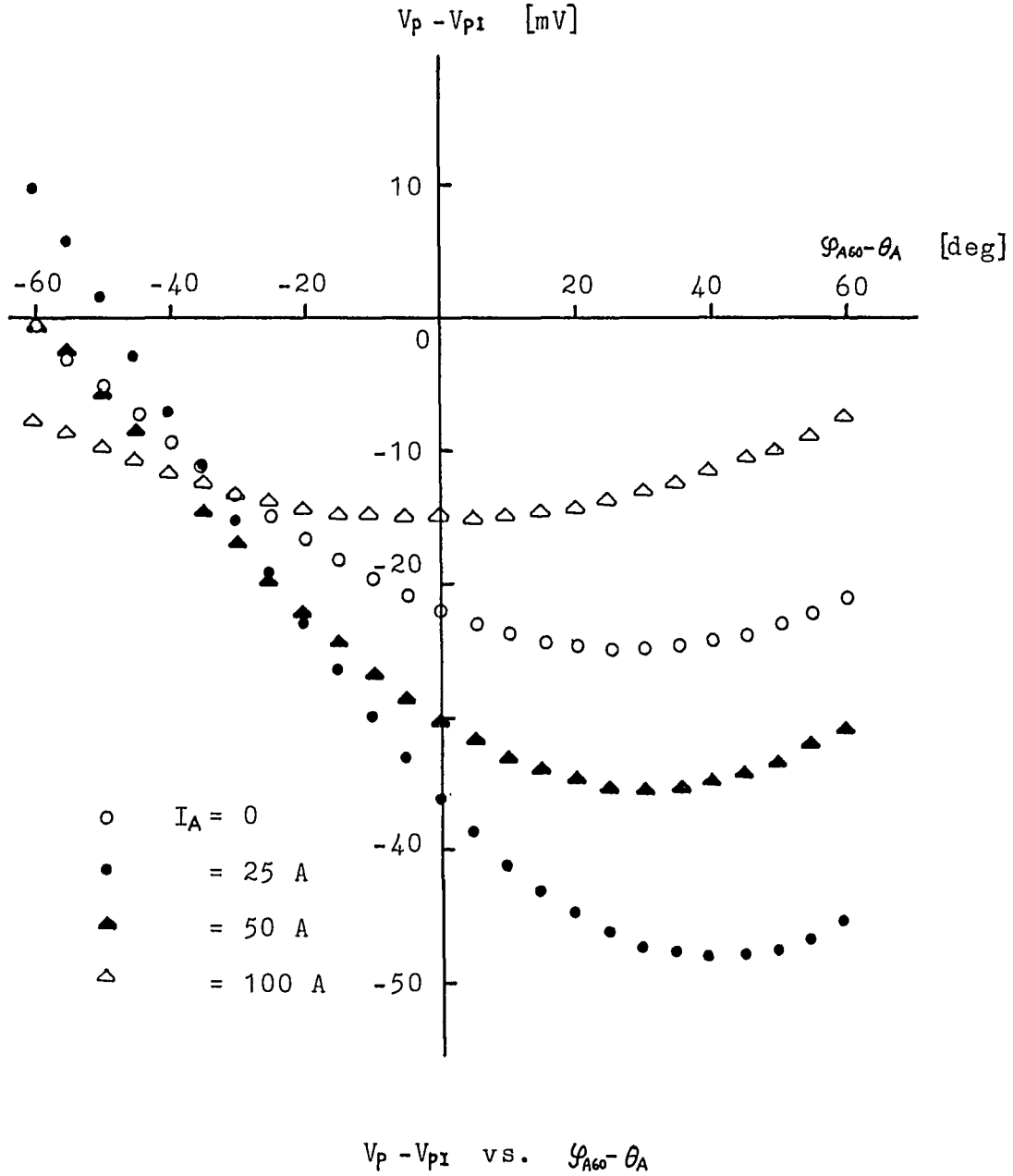


Figure 4-4: Error caused by the CT for the circuit with the phase shifter



Vp - VpI vs. φA60 - θA

Figure 4-5: Error caused by the CT for the circuit with the phase shifter

These curves show that the CT of this circuit causes errors greater than the maximum allowable error. However, at the current level above 50 A the error does not exceed the maximum allowable error. The gain fall off of the CT at the low current levels would be the cause of most errors.

One more circuit is now added. This circuit is designed for compensation of the gain drop of the CT at the low current level. This circuit detects the current levels less than 50 A in the power distribution system. Therefore, the microcomputer can use a different gain constant for the CT at low current levels. In other words, the error at low current levels in Figures 4-4 and 4-5 can be reduced. This additional circuit is called the current level detector.

The transfer characteristics of the analog portion of the circuit with the phase shifter and the current level detector are also given by equation 4-16. The transfer function of the digital part of this circuit uses 0.01130 as the gain at the low current level. Therefore, the next equation, 4-18, gives the transfer characteristics of the analog part of the ideal circuit in the event that the current level is lower than 50 A.

$$V_{PI} = 0.03130\ I_{A60} \cos(\varphi_{A60} - \theta_A) \quad . \qquad (4\text{-}18)$$

For current levels higher than 50 A the transfer characteristics of the ideal circuit is the same as given by equation 4-17. Figures 4-6 and 4-7 show the error of this circuit caused by the CT, i.e. $V_P - V_{PI}$ vs. I_{A60} and $V_P - V_{PI}$ vs. $\varphi_{A60} - \theta_A$. These figures show that the error caused by the CT never exceeds the maximum allowable error of 40 mV.

For the complete block diagram of the power monitor circuit the phase shifter and the current level detector are added to the basic circuit block diagram. Figure 4-8 shows this complete circuit block diagram. The transfer characteristics of the analog part of this diagram are given by equation 4-16. This is also rewritten as the following:

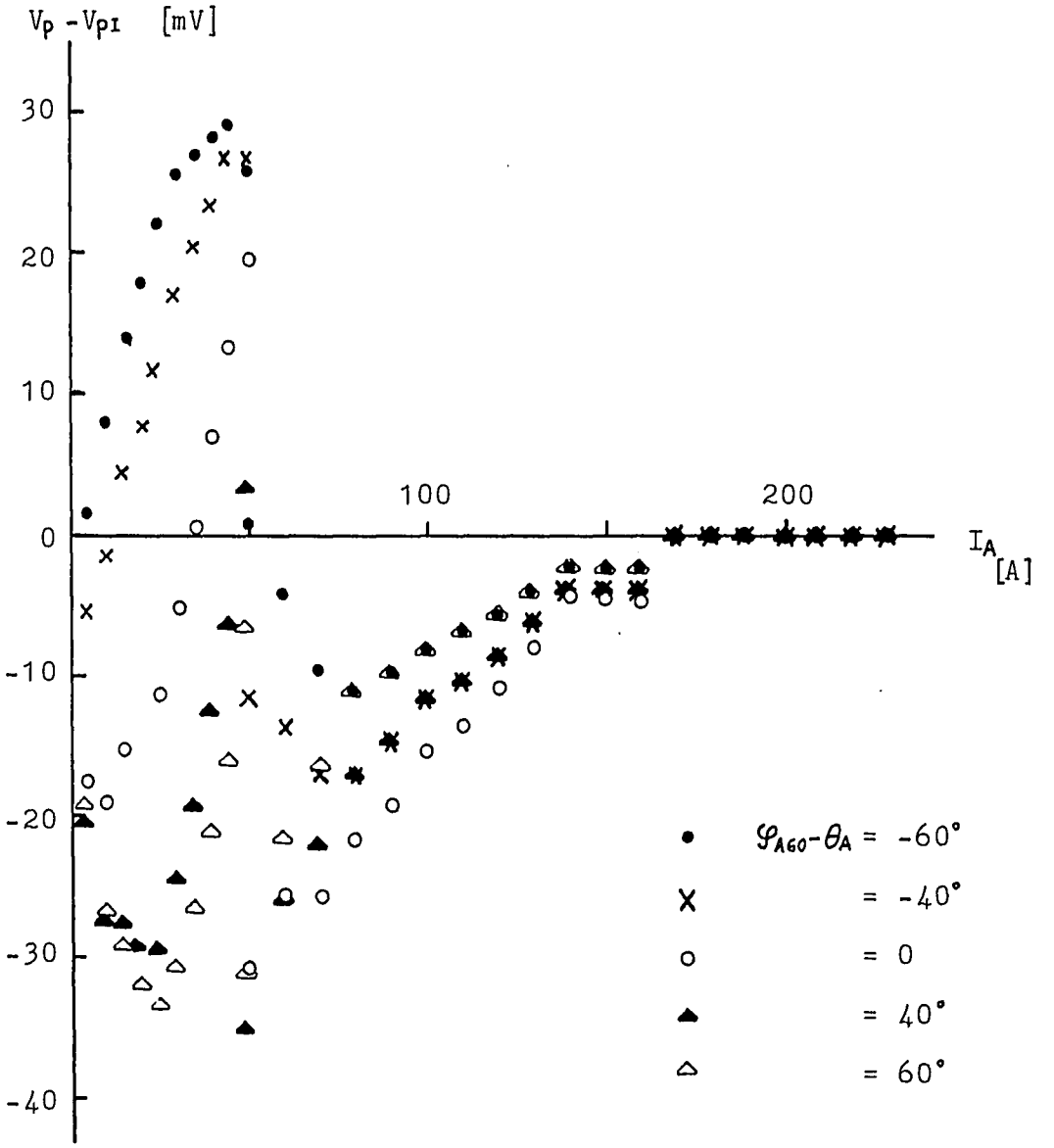
- for the 120 V system

$$V_P = 0.02529 G V_A I_{A60} \cos(\varphi_{A60} - \theta_A + \alpha - 4.3^\circ) , \qquad (4-19)$$

- for the 277 V system

$$V_P = 0.01096 G V_A I_{A60} \cos(\varphi_{A60} - \theta_A + \alpha - 4.3^\circ) , \qquad (4-20)$$

where equations 4-12, 4-13 and 4-15 are used. The transfer characteristics of the digital part are easily obtained by modifying and inverting equations 4-17 and



$V_p - V_{pI}$ vs. I_A

Figure 4-6: Error caused by the CT for the circuit with the phase shifter and the current level detector

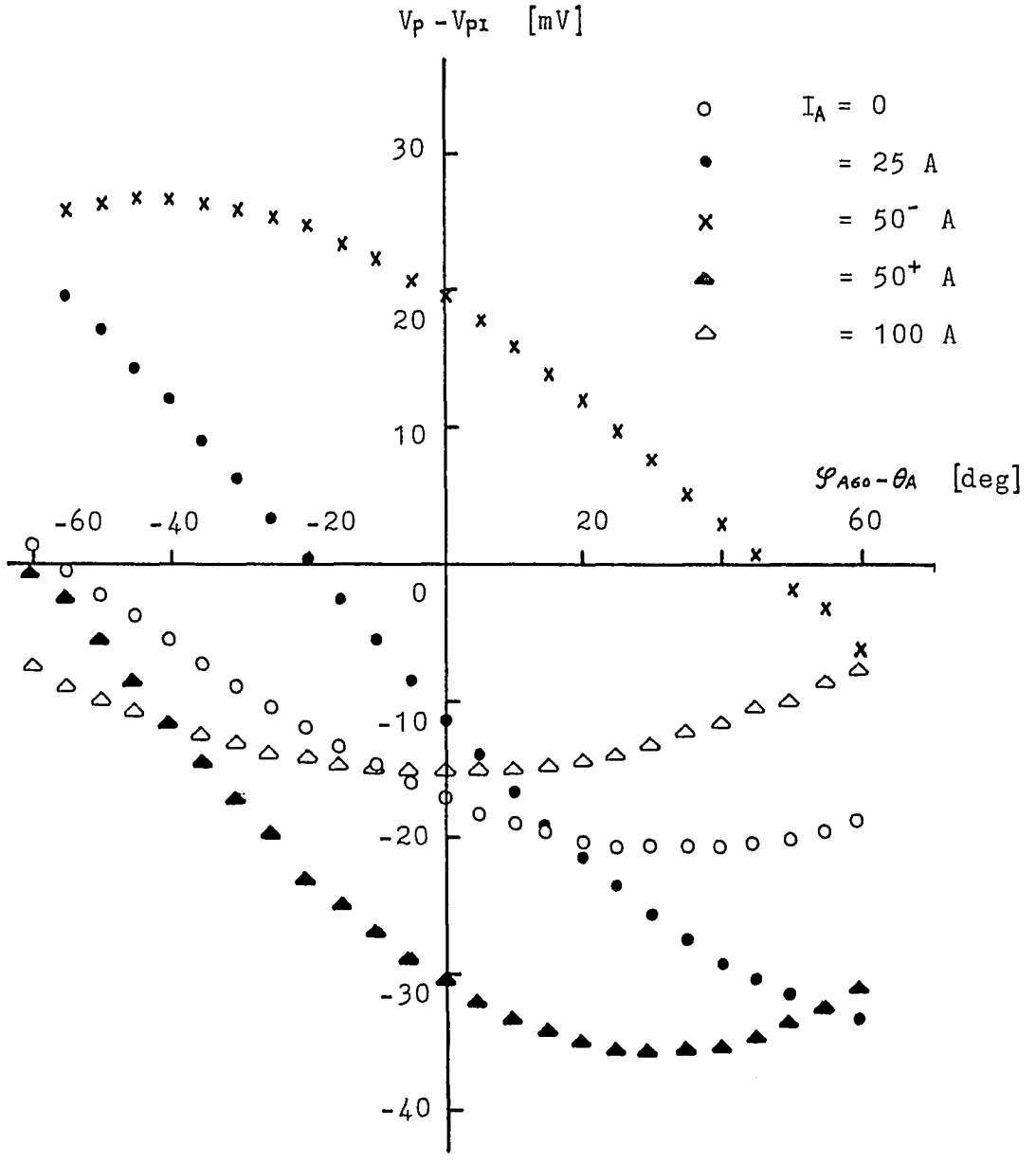


Figure 4-7: Error caused by the CT for the circuit with the phase shifter and the current level detector

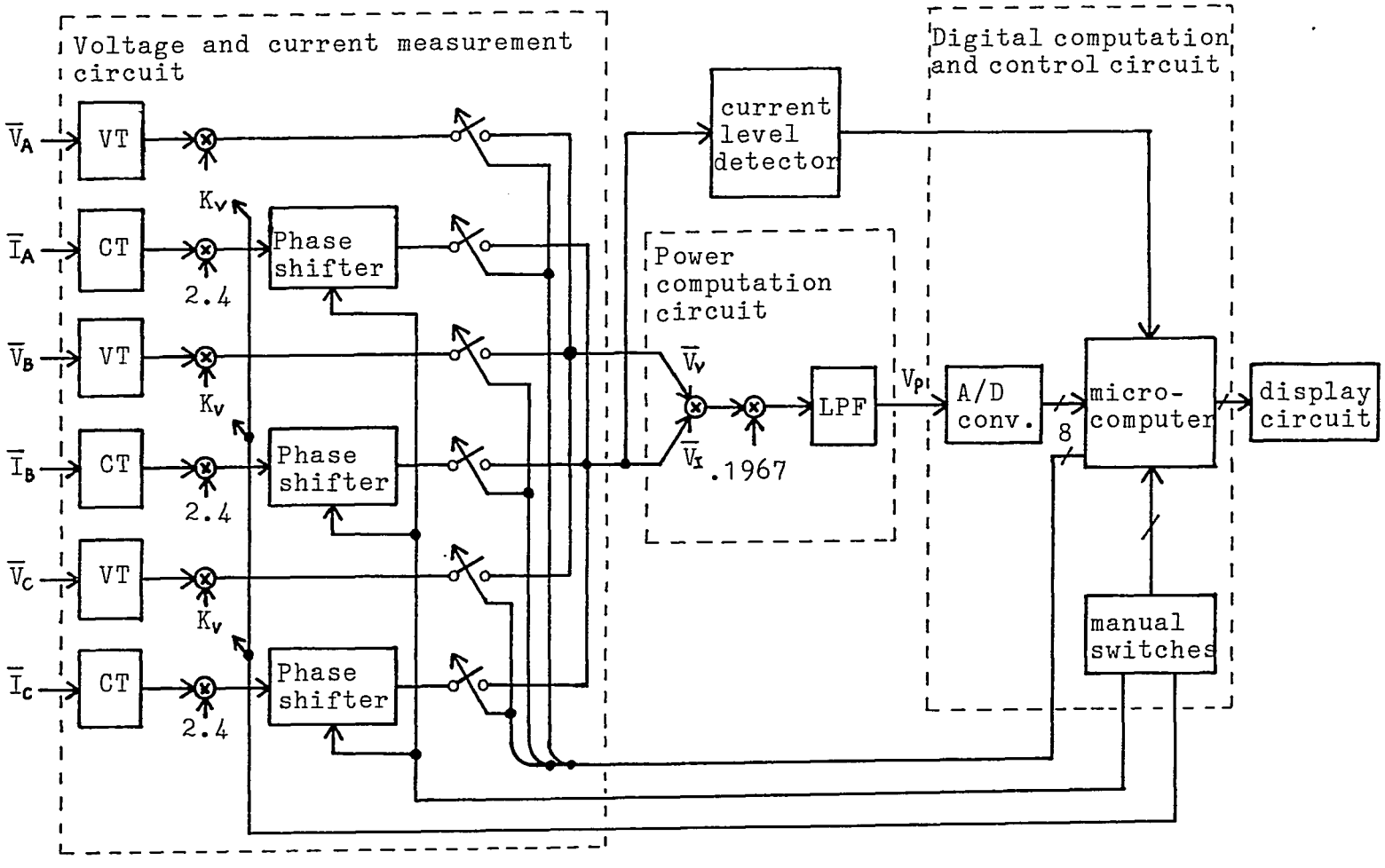


Figure 4-8: Block diagram of the power monitor circuit

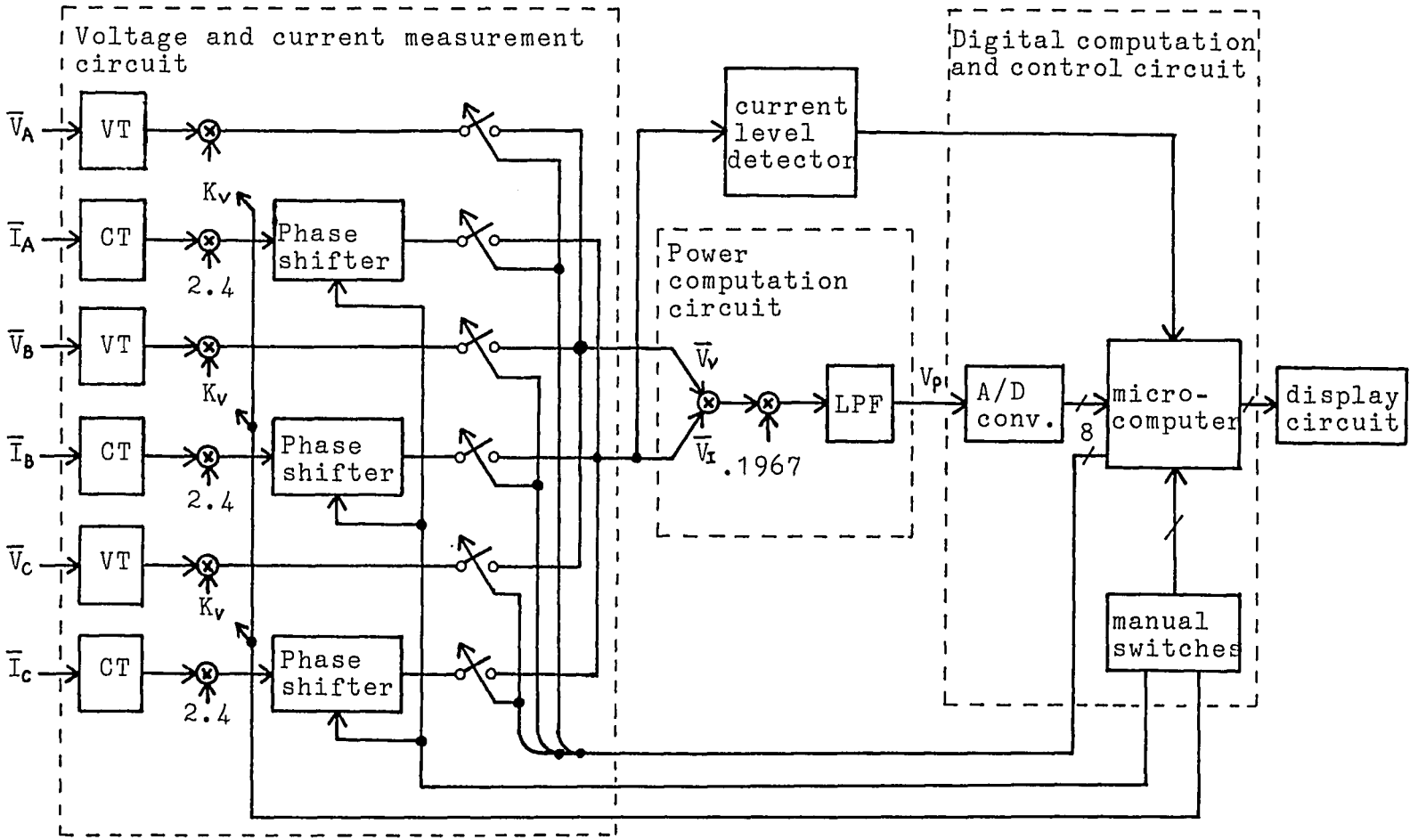


Figure 4-8: Block diagram of the power monitor circuit

4-18.

Now the weight of one bit of the A/D converter output is determined. First, the weight of one bit for the 120 V system at the low current level is considered. Equation 4-17 is rewritten as

$$V_{PI} = 0.0002858\ V_A\ I_{A60} \cos(\varphi_{A60} - \theta_A)$$
$$= 0.0002858\ P \quad . \qquad (4\text{-}21)$$

The transfer function of the digital part is obtained by inverting the transfer function in the equation 4-21. Therefore,

$$P' = (\ 1/0.0002858\ )\ V_P \quad .$$

Since 40 mV of the V_P is converting one bit, the digital representation of V_P, V_{Pd}, equals $V_P/0.04$. Thus,

$$P' = (\ 0.04/0.0002858\ )(\ V_P/0.04\ )$$
$$= 140\ V_{Pd} \quad .$$

The constant 140 is the weight of one bit in this case.

The weights of one bit in other cases are easily obtained in the same manner. The weights of one bit for other situations are given in table 4-1.

Line voltage	Current level low: I <50 A high: I ≥50 A	Weight
120 V	low	140 W
	high	136 W
277 V	low	323 W
	high	314 W

Table 4-1: Weight of one bit of the output of the A/D converter

5. Hardware Construction

5.1 Voltage and Current Measurement Circuit

The schematic of the voltage and current measurement circuit is shown in Figure 5-1. The circuits for Line B and C are the same configuration as that of Line A.

A VT whose maximum primary voltage is greater than 277 V is used for the voltage measurement. In addition, the peak secondary voltage of this VT is greater than 10 V when the primary voltage is 120 V. When the voltage of the line is 277 V the switch a_1 is closed. When the voltage of the line is 120 V the switch b_1 is closed. In both cases the potentiometers are adjusted to make the peak voltage of V_V equal to 9.09 V when the 60 Hz sinusoidal nominal voltage waveforms are applied to the primary winding. These adjustments set the proper values of the constant K_V; that is, the peak voltage of V_V is 10 V when the voltage of the system is 10 % above the nominal value.

An Amprobe SA60EN-1 CT and a 30 Ω secondary load resistor are used for the current measurement. An active first order low pass filter (LPF) is employed after the CT as the amplifier and the phase shifter. Because the input part of the LPF affects the secondary load resistance of the CT a voltage follower is used before

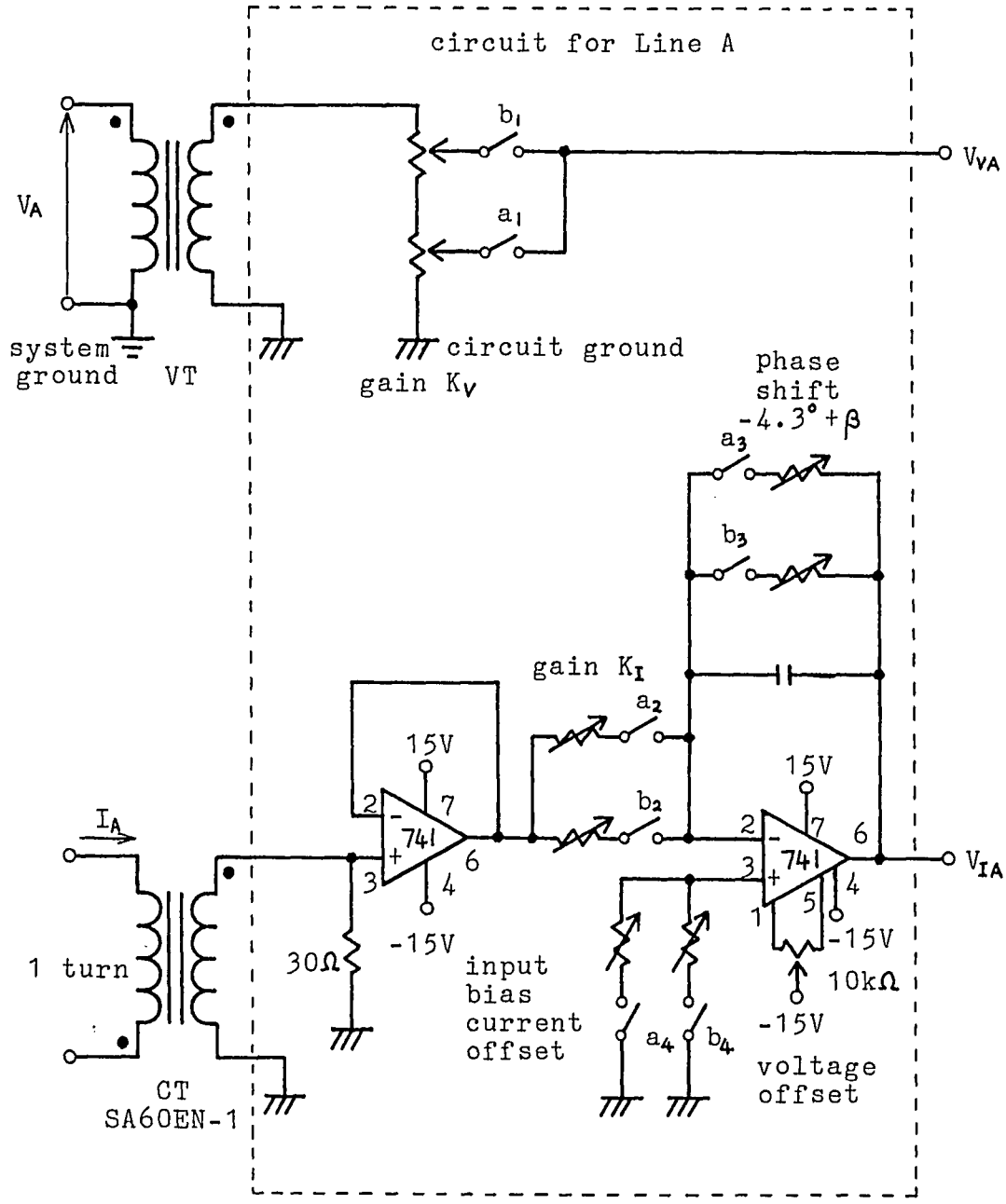


Figure 5-1: Voltage and current measurement circuit (1 of 2)

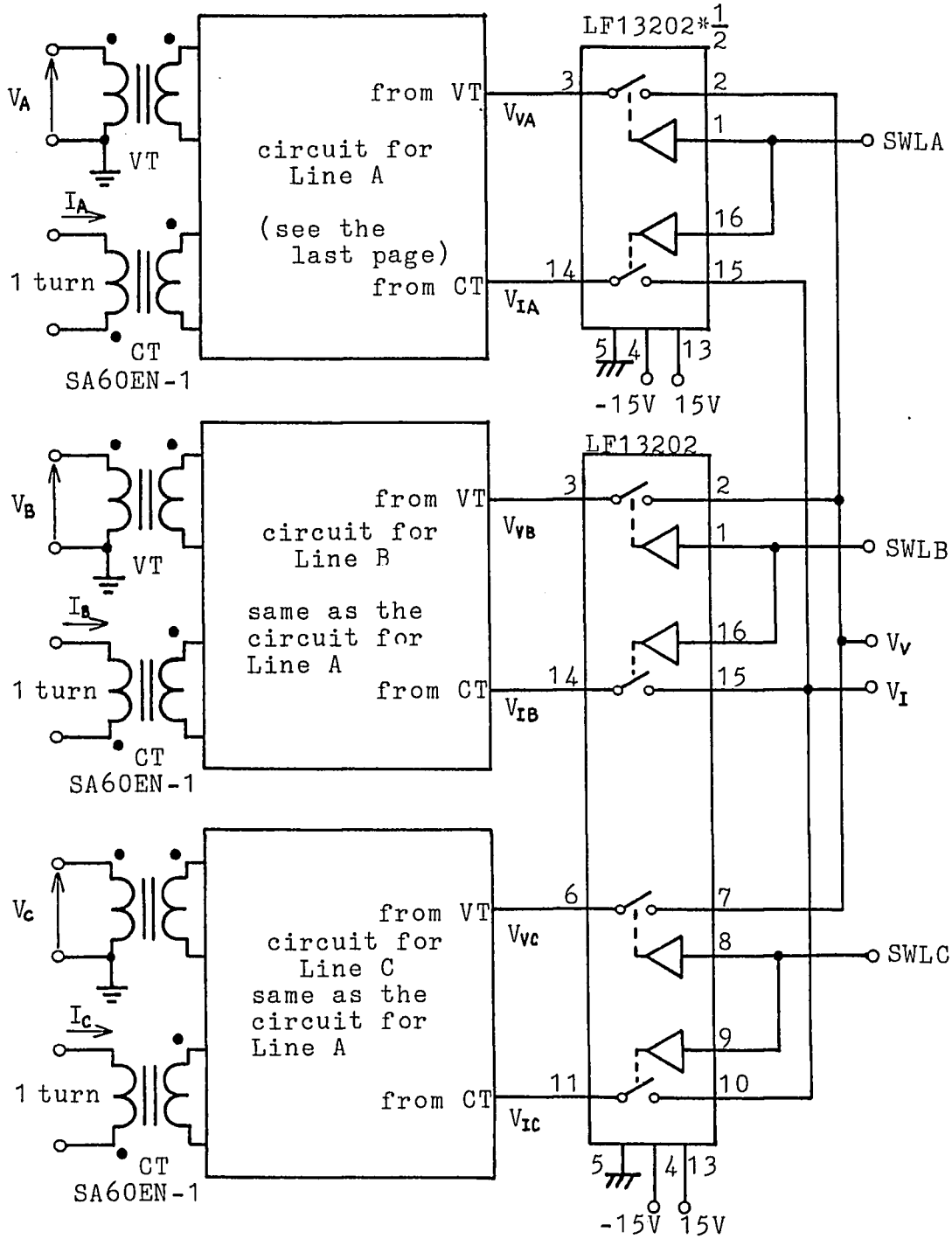


Figure 5-1: Voltage and current measurement circuit (2 of 2)

the LPF.

Because the LPF is employed the higher frequency components of the input (the current in the power distribution system) are damped and phase shifted more. However, the power can be accurately measured when the gain and phase shift at 60 Hz are accurate known. When the voltage of the line is 277 V the switches a_2, a_3 and a_4 are closed. When the voltage of the line is 120 V the switches b_2, b_3 and b_4 are closed. In both cases the gain at 60 Hz from the inout of the voltage follower to V_I is adjusted to a K_I of 2.4. This adjustment should be made by connecting the power computation circuit because the input part of the power computation circuit affects this gain adjustment. The phase difference between the outputs of the LPF and the VT is adjusted to zero when more than 100 A of the 60 Hz sinusoidal current and the nominal voltage, which is in phase with the current, are applied to the CT and the VT. A current of more than 100 A guarantees that the CT is operated at the flat part of its phase shift characteristic curve. The voltage offset and input bias current offset adjustments are provided to nullify the output voltage for zero input.

National Semiconductor LF13202 analog switches are employed as the switches for the line selection. These devices can operate with ±10 V analog signal levels. The

digital input of this device is designed to accept TTL levels. These switches are controlled by the microcomputer.

5.2 Power Computation Circuit

The power computation circuit consists of an Exar Integrated System XR-2208C operation multiplier. This device contains an analog multiplier and an operational amplifier.

The schematic of this circuit appears in Figure 5-2. The multiplier output V_o, i.e. the voltage difference between pins 1 and 2, is the product of two input voltages: V_V and V_I, and a gain constant. The operational amplifier part performs the function of a differential amplifier whose input is V_o. The gain of the multiplier and the differential amplifier results in a gain constant M of 0.1967. The 6.6 μF and 0.24 μF capacitors operate as a LPF which cuts off all high frequency ac components. The gain constant M is adjusted by the gain control potentiometer. The X offset and Y offset adjustments compensate for the output voltage for a zero input and the output offset adjustment nullifies the output voltage for a zero input simultaneously on the X and Y inputs.

The LPF is designed to extract the dc component from

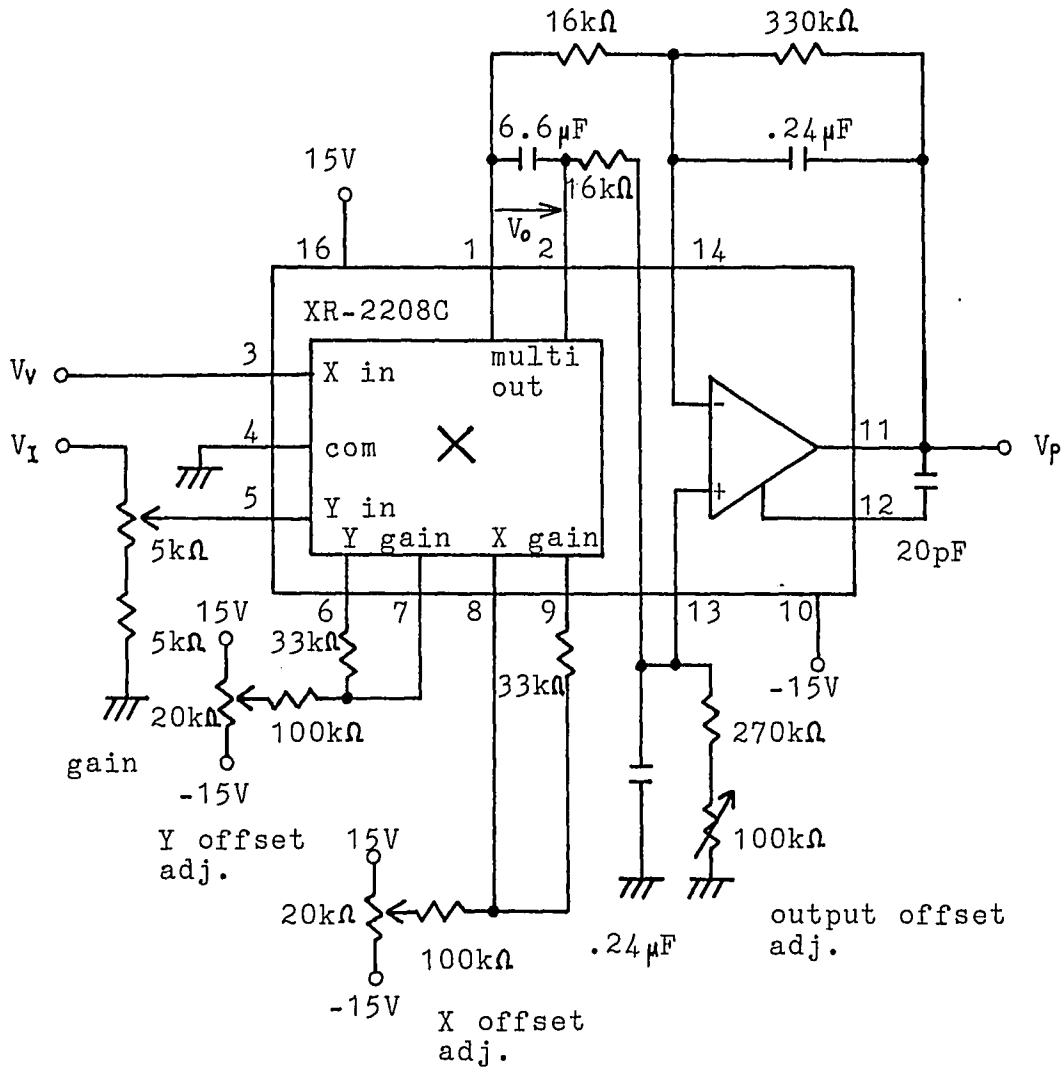


Figure 5-2: Power computation circuit

the instantaneous power. However, the ac components of the instantaneous power can pass through the LPF while sustaining some attenuation because the LPF is not ideal. The ac ripple at the output of this circuit can cause measurement errors. Since 60 Hz could be the lowest of the ac components of the instantaneous power, the cut off frequency of the LPF is designed to be 2.02 Hz. The gain at 60 Hz is then -58.9 dB. The magnitude of the 60 Hz ripple is determined by the 120 Hz component of the current in the power distribution system because the CT cannot pass the dc component (see section 2.2). Thus, theoretically the greatest magnitude of the 60 Hz component happens when the current in the line is 230 A, 120 Hz. Even in this case the ripple at V is 22.3 mV peak to peak. This ripple causes, at most, 1 bit error at the output of the A/D converter. This ripple can be reduced by changing the LPF characteristics. However, reducing the ripple causes a long response time which is discussed next.

The step response of the LPF determines the minimum "on" time of the line selection switches. The "on" time of these switches should be substantially longer than the settling time of the output of the LPF, V_p. The settling time, zero to 95 % of the final value, is 0.38 sec. A time of one second is substantially longer than this

settling time and is selected to be the "on" time of the line selection switches. In this case V_p reaches 99.996 % of the final voltage. The "on" time of the switch should be shorter than the duration in which the current in the line can be considered unchanged. One second is normally short enough for this duration. The power of each line is measured once every three seconds since there are, at most, three lines.

After construction, the LPF was tested to experimentally measure both the gain at 60 Hz and the settling time. The gaine at 60 Hz was -54.4 dB and the settling time was 0.31 sec. These results are still acceptable.

5.3 Current Level Detector

The current level detector measures the peak voltage of the V_I's 60 Hz component and then compares this measured voltage with a threshold voltage. This threshold voltage corresponds to the peak value of a 50 A, 60 Hz sinusoidal current on the line. If the measured voltage is less than the threshold voltage the output of this circuit is at the high level of the microcomputer input voltage; i.e. it is about 5 V. Otherwise, the output is about 0 V. This circuit consists of three parts: a band pass filter (BPF), a

rectifier and smoothing circuit, and a comparator. The schematic diagram of this circuit is shown in Figure 5-3.

The BPF extracts the 60 Hz component of V_I. The center frequency of this BPF is 60 Hz and the bandwidth is 12 Hz. Because the input impedance of the BPF could load the V_I source a voltage follower is used before the BPF. The offset adjustment nullifies the output voltage of the BPF to zero for $V_I = 0$.

The rectifier and smoothing circuit changes the BPF output to dc voltage whose magnitude equals the peak voltage of the BPF output. The discharging current of the 0.1 μF capacitor is extremely small. Therefore, the response of the output of this circuit is very slow when the input changes from high voltage to low voltage. In order to improve the response time a 3 V zenner diode is employed in the rectifier. This zenner diode confines the input voltage of this circuit so that the input cannot exceed 3 V. By using this zenner diode the current level detector responds to the change of V within one second, the "on" time of the line selsction switches.

The comparator portion compares the output of the rectifier and smoothing circuit with the threshold voltage. Because the output of the rectifier and smoothing circuit has a ripple the comparator is designed

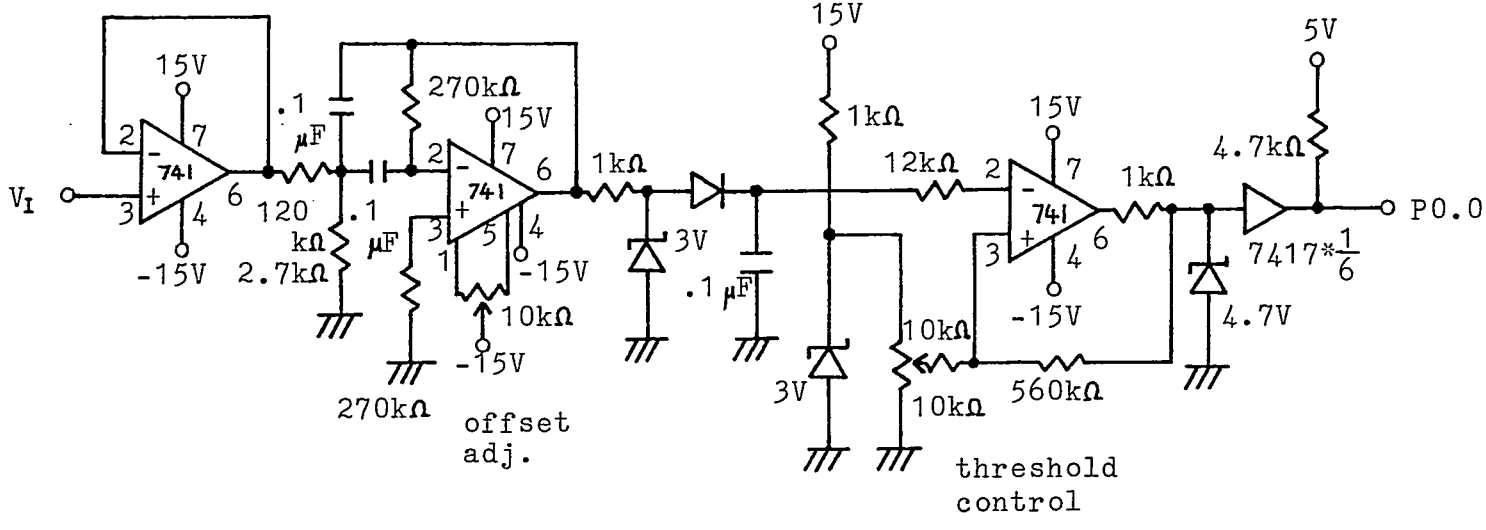


Figure 5-3: Current level detector

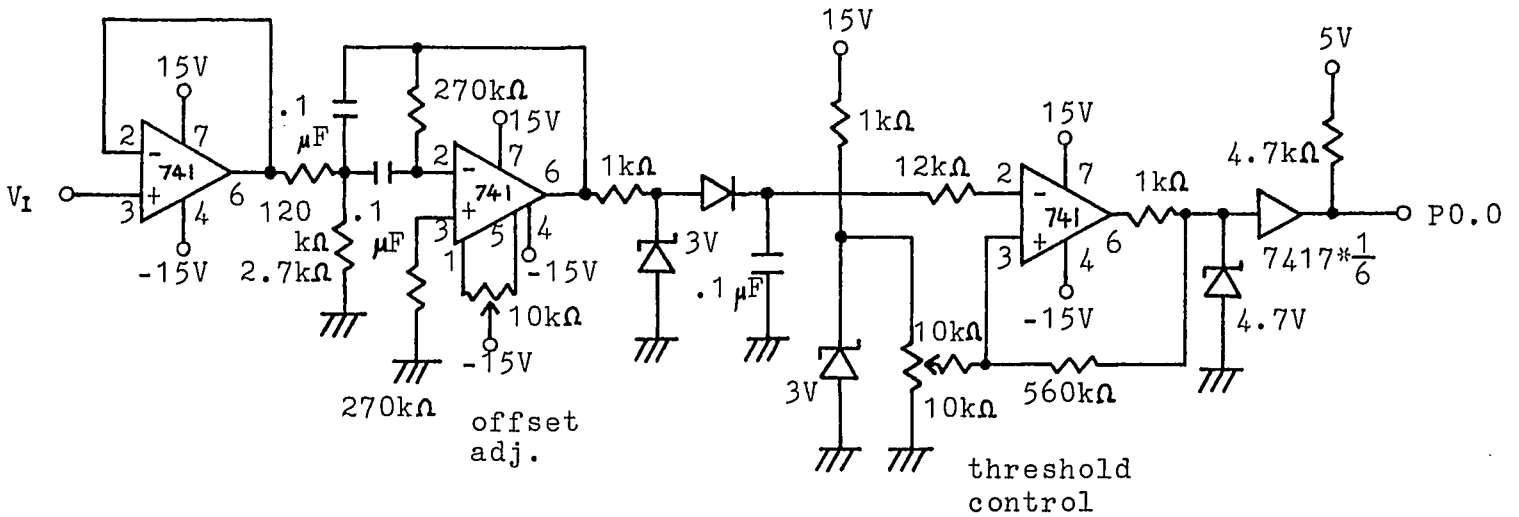


Figure 5-3: Current level detector

to be a schmitt trigger type. When V_I is 1.37 V, 60 Hz sinusoidal the threshold voltage control potentiometer is adjusted so that the output of the current level detector is at the transition between the high level and low level voltage. This threshold voltage corresponds to a 50 A, 60 Hz sinusoidal current in the line. The output of this circuit is then fed to microcomputer. Therefore, the 4.7 V zenner diode and the TTL gate, 7417, are used for the output part of the comparator.

5.4 Digital Computation and Control Circuit

The digital computation and control circuit is shown in Figure 5-4. This circuit is divided into two parts, the A/D converter and the microcomputer.

The A/D converter converts the output of the power computation circuit, V_p, into 8-bit binary data. An Analog Devices AD570 8-bit A/D converter is employed. The input range of the converter is 0 - 10.24 V. Therefore, the weight of one bit is 40 mV. The code transitions are between the bit weights shown in Figure 5-5. The two potentiometers control the bit weights and code transtions.

The data output circuit of the A/D converter is a tri-state configuration. When the A/D converter is in the stand-by state the data output pins are in the

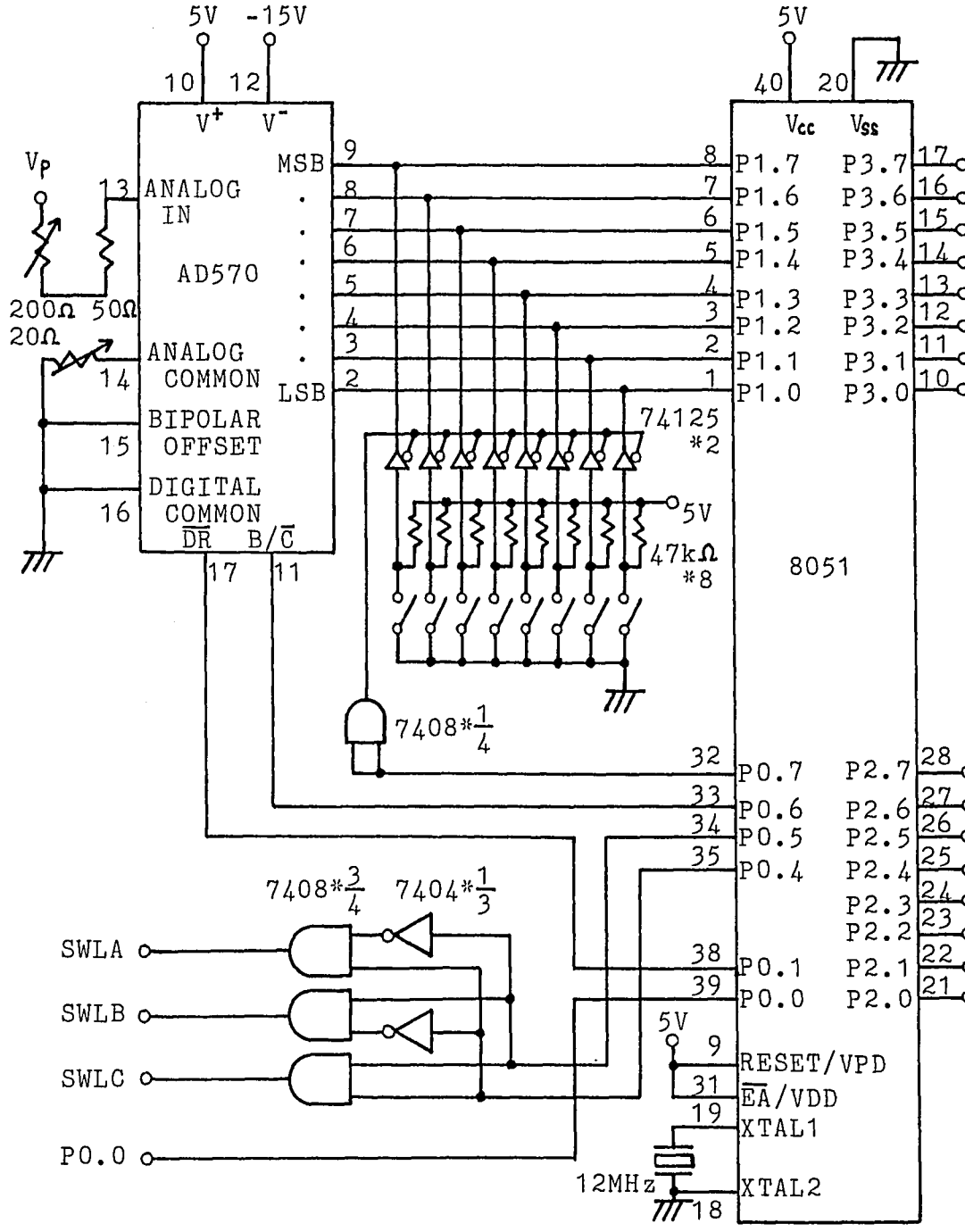


Figure 5-4: Digital computation and control circuit

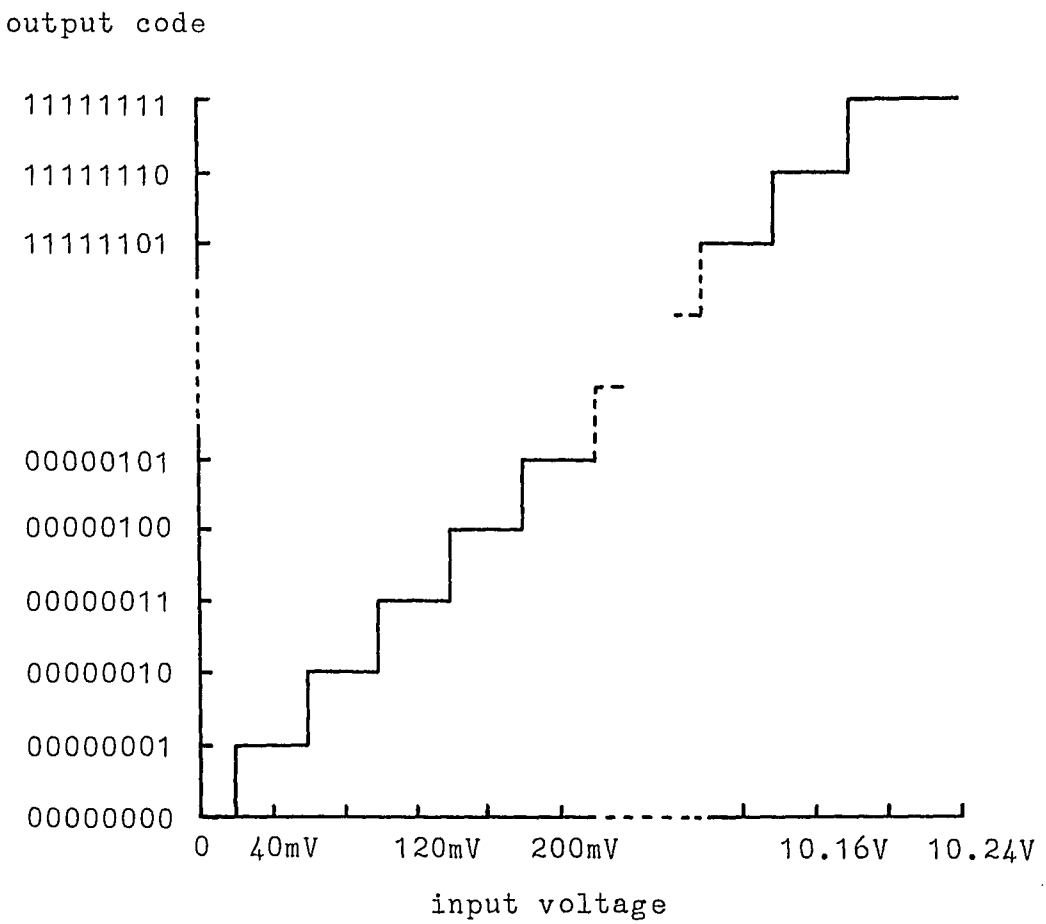


Figure 5-5: Transfer curve of the A/D converter

high-impedance (high-Z) state. Holding the BLANK and $\overline{\text{CONVERT}}$ (B/$\overline{\text{C}}$) pin high brings the A/D converter into the high-Z state. In this state the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) pin is high. When the B/$\overline{\text{C}}$ pin is brought low the conversion starts; but the $\overline{\text{DR}}$ and data output pins do not change states. When the conversion is complete, in typically 25 sec, the $\overline{\text{DR}}$ pin goes low and within 50 nsec the data output pins become active with the new data. When the B/C pin is driven high again the A/D converter enters the high-Z state within about 1.5 μsec. This control sequence is performed by the microcomputer. The diagram of the sequence appears in Figure 5-6.

The microcomputer computes the power using the A/D converter output. Then, the microcomputer translates the power which is to be displayed into 3-digit binary-coded-decimal (BCD) data with a floating decimal point. This BCD data is the input of the display circuit. In order to perform this computation the microcomputer must have knowledge of which type power system configuration one is dealing with. The manual switches inform the microcomputer of this configuration and which power option is to be displayed. The current level detector is used to inform the microcomputer whether the CT is carrying large or small currents. The microcomuter also controls the line selection swiches and the A/D

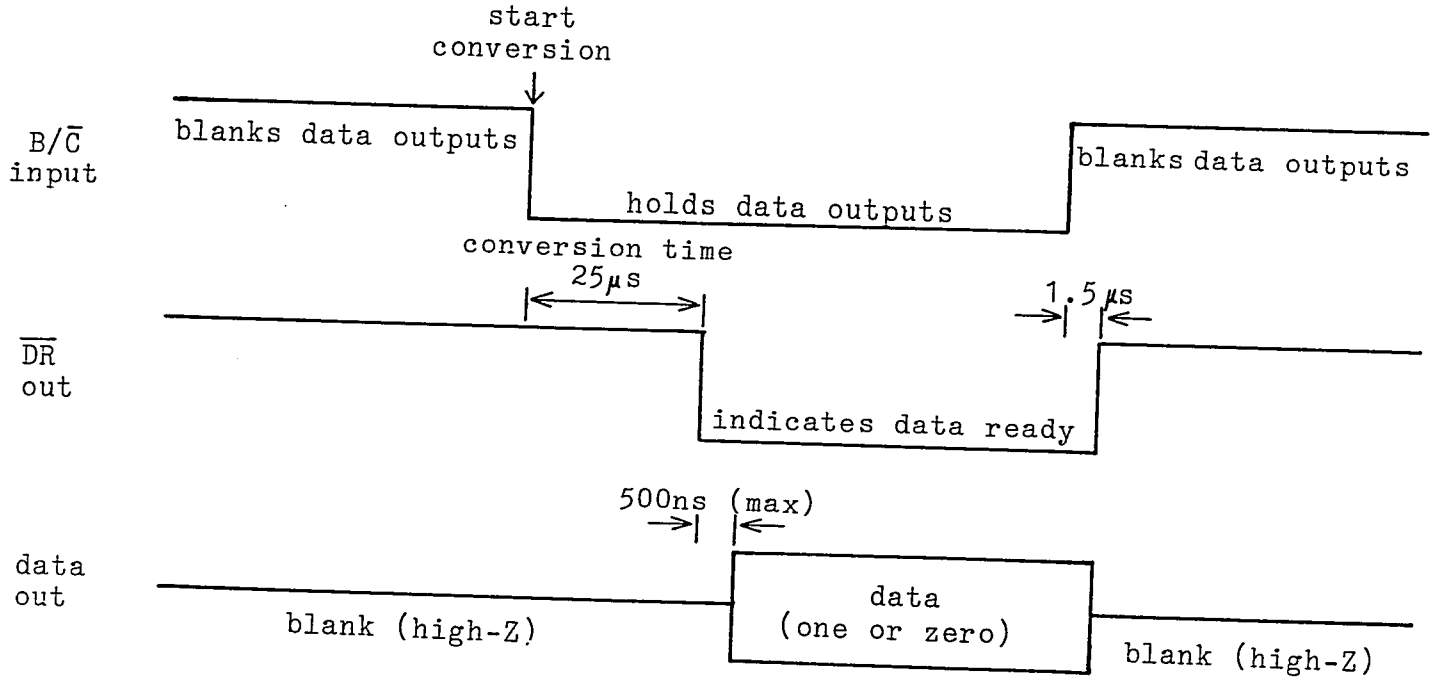


Figure 5-6: Timing and control sequence of the A/D converter

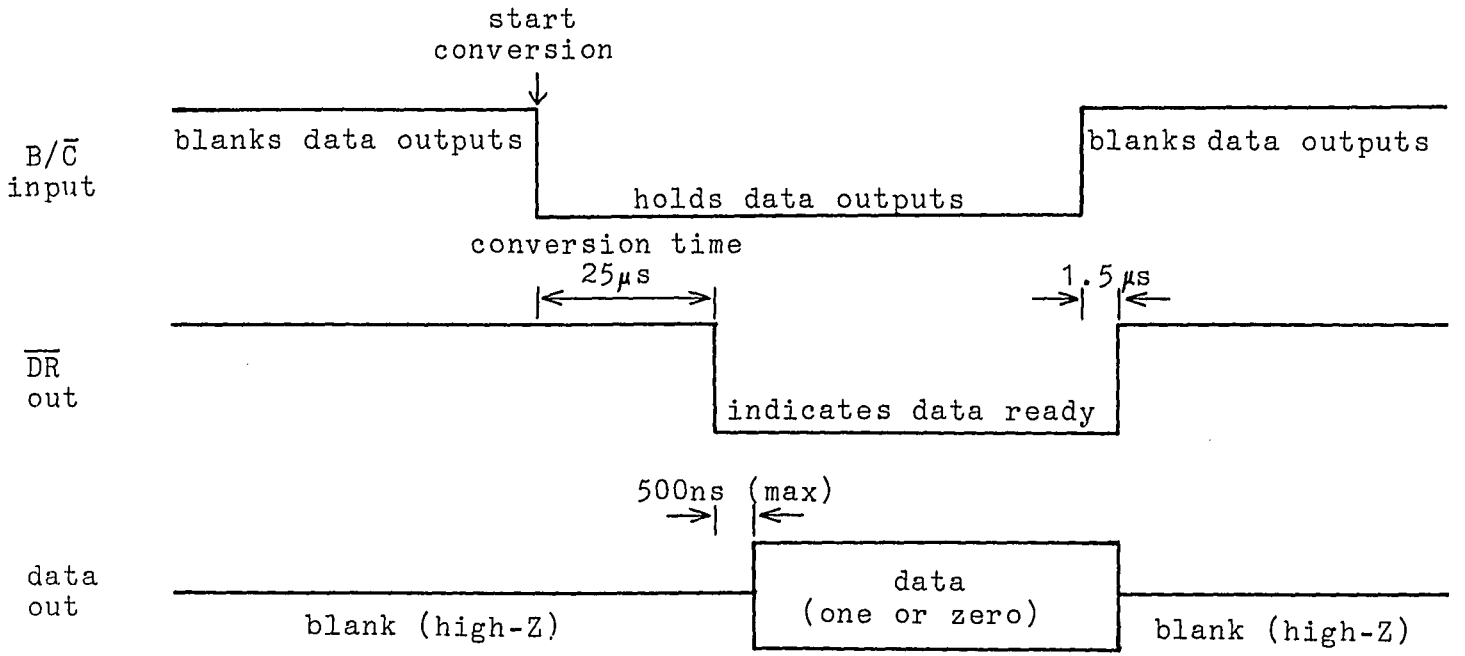


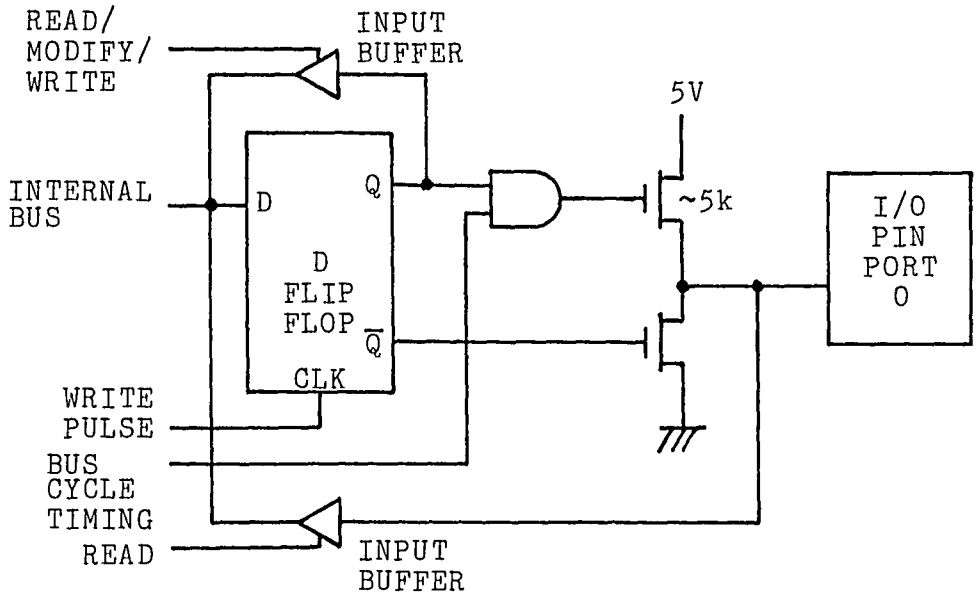
Figure 5-6: Timing and control sequence of the A/D converter

converter. Details of the computation are discussed in chapter 6.

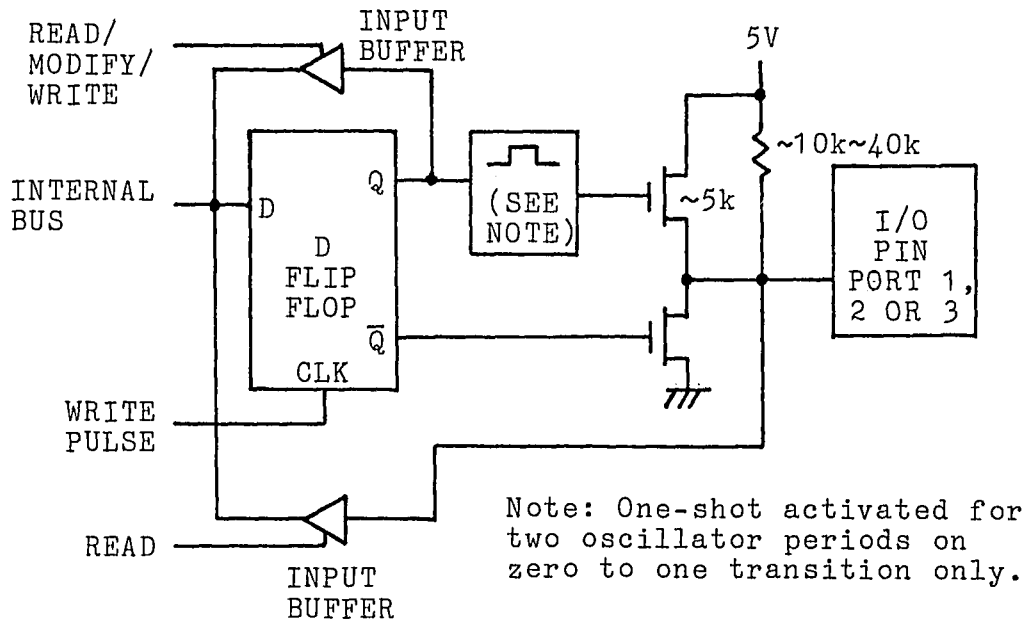
An Intel 8051 single-component 8-bit microcomputer is employed. This microcomputer has 4096 bytes of program memory and 128 bytes of data memory on the chip. The instruction cycle is one microsecond when using a 12 MHz crystal. This microcomputer can perform hardware multiples and divides in 4 μsec. More information is provided by the user's manual [5].

There are 32 I/O pins configured as four 8-bit ports, Port 0, Port 1, Port 2 and Port 3. Each pin can be individually and independently programmed as an input or output. Each I/O pin has a D flipflop and an output driver as shown in Figures 5.7(a) and (b). The input operation can be performed by the following: First, one uses an instruction which writes a "one" to an I/O pin. This forces the D flipflop to store the value on the I/O pin which is applied by external device. Then, one reads the D flipflop output. The output operation can be performed simply by writing a "one" or "zero" to an I/O pin. Because of the D flipflops the last value written on the flipflop is retained on the I/O pin.

Assignment of I/O pins is shown in table 5-1. The role of Port 0 is to control other circuits. Port 1 is the input port from the A/D converter and manual



(a) I/O pin in Port 0



(b) I/O pin in Port 1, 2 or 3

Figure 5-7: Configuration of I/O pin of the 8051

port	pin	function
Port 0	P0.0	input from the current level detector H: low current level L: high current level
	P0.1	input from DR of the A/D converter H: data is not ready L: data is ready
	P0.2	————
	P0.3	————
	P0.4 P0.5	control of the line selection switches SWLA SWLB SWLC P0.4 H L H P0.5 L H H
	P0.6	control of R/C of the A/D converter H: do not convert L: convert
	P0.7	control of the buffers of the manual switches H: high impedance state L: active state
Port 1	P1.0 ∫ P1.7	input from bit outputs of the A/D converter P1.7: MSB P1.0: LSB
	P1.0	input from the manual switch indicating 2-wire system
	P1.1	input from the manual switch indicating 3-wire system
	P1.2	input from the manual switch indicating 4-wire system

Table 5-1: I/O pin assignment of the 8051

port	pin	function
Port 1	P1.3	input from the manual switch indicating the voltage of the system H: 277 V L: 120 V
	P1.4	input from the manual switch indicating that the output is the total power
	P1.5	input from the manual switch indicating that the output is the power of Line A
	P1.6	input from the manual switch indicating that the output is the power of line B
	P1.7	input from the manual switch indicating that the output is the power of Line C
Port 2	P2.0 $\wr$ P2.3	output of the BCD low-digit P2.3: MSB P2.0: LSB
	P2.4 $\wr$ P2.7	output of the BCD medium-digit P2.7: MSB P2.4: LSB
Port 3	P3.0 $\wr$ P3.3	output of the BCD high-digit P3.3: MSB P3.0: LSB
	P3.4	position of the decimal point when the data is greater than 10 kW
	P3.5	position of the decimal point when the data is greater than 1 kW
	P3.6	position of the decimal point when the data is smaller than 1 kW
	P3.7	no-line-indication

Table 5-1: I/O pin assignment of the 8051

(2 of 2)

switches. Ports 2 and 3 are the output ports to the display circuit. Since the manual switches use the same port as the A/D converter 74125 TTL tri-state buffer gates are employed. These buffer gates are controlled by pin P0.7. The output circuit of the A/D converter is a tri-state configuration. The I/O pins, P0.6 and P0.1, are connected to the B/$\overline{C}$ pin and the $\overline{DR}$ pin of the A/D converter, and control the A/D converter. Pins P0.5 and P0.4 control the line selection switches. TTL 7408's and 7404's are employed to convert codes on P0.5 and P0.4 to the control signal of the line selection switches. The I/O pin P0.0 is the input pin from the current level detector. Because the minimum input low voltage of the microcomputer is -0.5 V the output part of the current level detector uses a 7417 TTL gate.

The instruction cycle is one microsecond. The pin $\overline{EA}$/VDD is held at a TTL high level because the microcomputer has no external memory. In order to reset the microcomputer at powering up the RST/VPD pin is connected to the +5 V power supply.

5.5 Display Circuit

The display circuit displays the measured power on three seven-segment LED's. The input of this circuit is a 3-digit BCD data word and the position of the decimal point. This circuit also shows the no-line-indication. The schematic of this circuit is shown in Figure 5-8.

In order to control the seven-segment LED's 7447 TTL BCD-to-seven-segment decorders/drivers are used. The output configuration of these devices is an open-collector configuration. Therefore, 220 Ω resistors and common-anode seven-segment LED's are used. The 7417 TTL open-collector buffers are employed to control decimal points of the seven-segment LED's. The no-line-indication circuit uses the same configuration as the decimal point control.

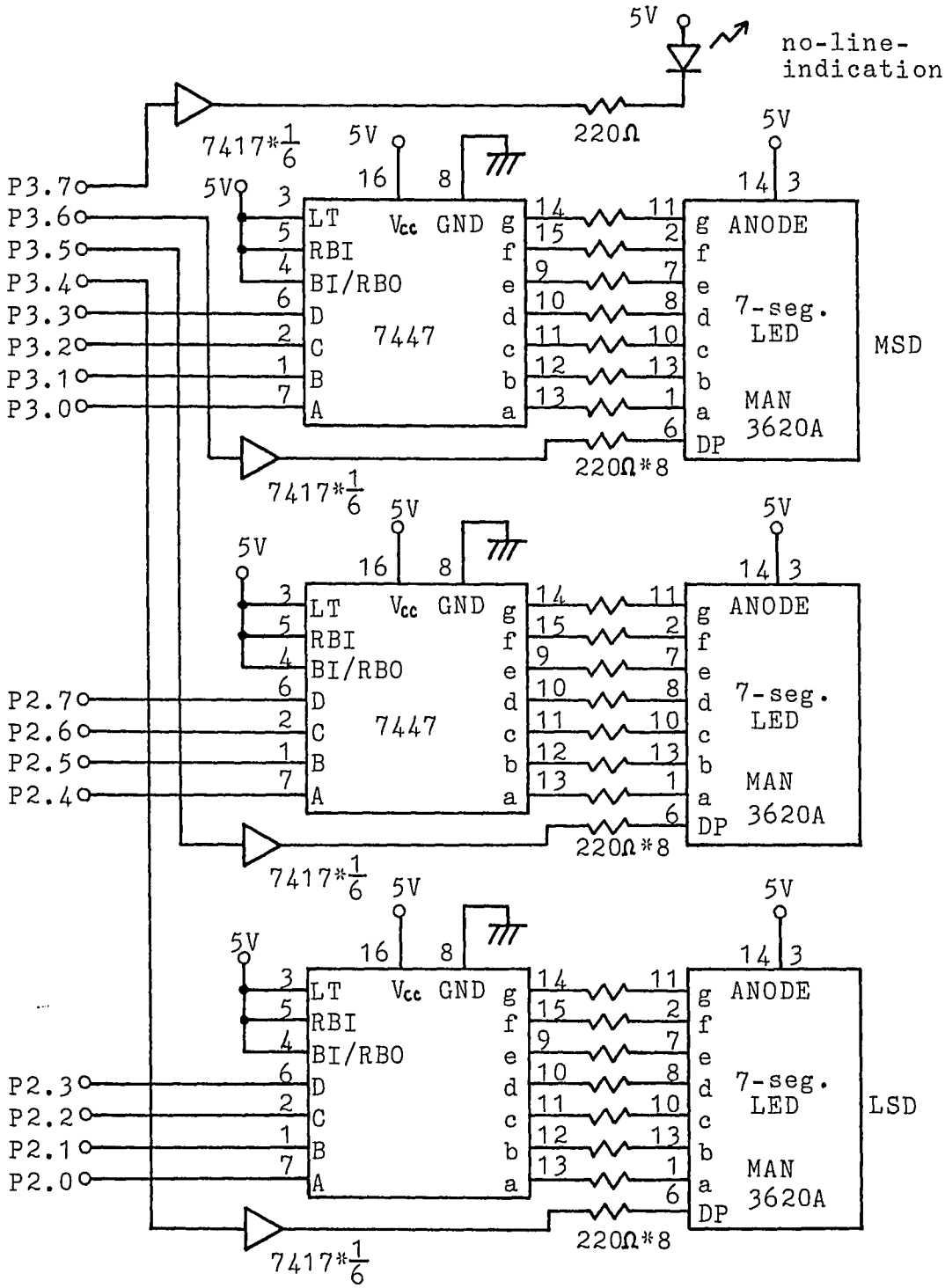


Figure 5-8: Display circuit

6. Microcomputer Program

6.1 Program Outline

The program of the microcomputer is discussed in this chapter. This program computes the power in the power distribution system and translates the computed power to the BCD form. This program also controls other circuits; that is, the line selection switches, the A/D converter and so on. Information about the Intel 8051 microcomputer can be found in the user's manual [5, 6].

The outline of the program is shown in the flow chart in Figure 6-1. A loop in the flow chart takes one second which is controlled by the internal timmer, Timer 0. This microcomputer is reset at powering up time and then the execution begins. Now, each block of the flow chart is explained.

The first block, INITIATION, readies the special function registers, the user-defined flags and the status bytes, I/O ports and memories. The special function registers are set so that Timer 0, and the Timer 0 interrupt, are enabled. The explanations of the user-defined flags and status bytes are given in section 6.3. Port 0 is initiated so that the A/D converter is in the stand-by situation and Line A is connected to the power computation circuit. Ports 2 and 3 are set to display

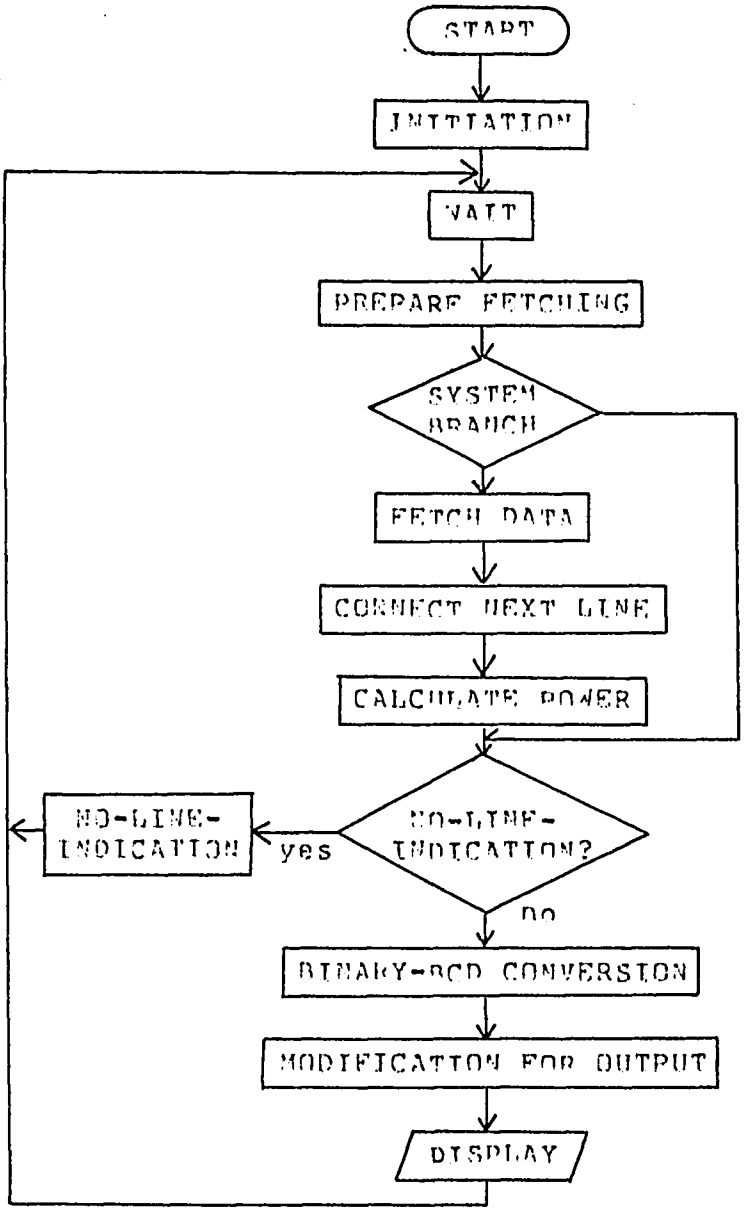


Figure 6-1: Outline of the program

zero. All the memories for measured power are set at zero.

The WAIT block halts the execution until one second has passed since the last time the execution of the loop began. One second is the chosen interval for the power measurements.

The PREPARE FETCHING block sets the user-defined flags and satus bytes in preparation for fetching the output of the A/D converter. This block examines the manual switches and decides the memory location which is to be addressed when the power is to be displayed. This block also decides whether the no-line-indication is needed or not.

Depending upon the configuration of the power distribution system, the number of the lines is different. Because power of each line is measured every three seconds the microcomputer does not have to measure power every second for the one or two line system. The SYSTEM BRANCH block decides whether or not to read the A/D converter or wait until it is time to do so. Table 6-1 shows the criteria of branching.

The FETCH DATA block controls the A/D converter and fetches the output of the A/D converter. This block also examines the output of the current level detector. The memory location for measured power is also selected.

system	destination of SYSTEM BRANCH			time to calculate the total power
	1st second *	2nd second *	3rd second *	
1-line system	FETCH DATA	NO-LINE-INDICATION?	NO-LINE-INDICATION?	1st second *
2-line system	FETCH DATA	FETCH DATA	NO-LINE-INDICATION?	2nd second *
3-line system	FETCH DATA	FETCH DATA	FETCH DATA	3rd second *

* NOTE: The overall cycle of time of the program is 3 seconds. 1st second, 2nd second and 3rd second mean the 1st, the 2nd and the 3rd second of this cycle time respectively.

Table 6-1: Destination of the SYSTEM BRANCH block and time to calculate the total power

system	destination of SYSTEM BRANCH			time to calculate the total power
	1st second *	2nd second *	3rd second *	
1-line system	FETCH DATA	NO-LINE-INDICATION?	NO-LINE-INDICATION?	1st second *
2-line system	FETCH DATA	FETCH DATA	NO-LINE-INDICATION?	2nd second *
3-line system	FETCH DATA	FETCH DATA	FETCH DATA	3rd second *

* NOTE: The overall cycle of time of the program is 3 seconds. 1st second, 2nd second and 3rd second mean the 1st, the 2nd and the 3rd second of this cycle time respectively.

Table 6-1: Destination of the SYSTEM BRANCH block and time to calculate the total power

In order to prepare for the next measurement the CONNECT NEXT LINE block controls the line selection swiches to connect the line whose power is to be measured next.

According to the discussion in section 4.4 the power in a line is the product of the fetched binary data and the weight of a bit. The CALCULATE POWER block calculates this product, i.e. the power of a line, using the weight listed in Table 4-2. The calculated power is stored in memory whose location was decided in the FETCH DATA block. The total power is calculated every three seconds. If it is time for calculating the total power the total power is also determined. The time for the total power is decided according to Table 6-1.

Up to now the program calculates power in binary form. Now the process of retrieving the data for display is considered. First, the no-line-indication is considered. If the no-line-indication is needed then the display of power is not needed. Therfore, in this case it is decided to display the no-line-indication and skip the blocks which display power. Otherwise it is decided to go to the following blocks which display power. This is performed in the blocks, NO-LINE-INDICATION? and NO-LINE-INDICATION.

The power to be displayed is stored in the memory

whose location was decided in the PREPARE FETCHING block. This data is in binary form. Since the output of the microcomputer is in BCD form a binary-BCD conversion is needed. This conversion is performed in the BINARY-BCD CONVERSION block. In this program a special scheme is employed to perform this conversion. This is explained in the next section.

The output of the microcomputer is in a three-digit BCD code with a floating decimal point at the kW unit. The MODIFICATION FOR OUTPUT block selects the proper three, out of six, significant digits and the position of the decimal point.

Finally, the DISPLAY block sends the output to the display circuit. After this block the excution returns to the WAIT block.

6.2 Binary to BCD Algorithm

The algorithm which is used in the BINARY-BCD CONVERSION block in Figure 6-1 is explained next. This algorithm is designed for that block alone. That is, the 8051 microcomputer instruction set is used and the lengths of the binary and the BCD data are restricted by the use of that block.

First, the length of the binary and the BCD data are considered. The binary data is the product of the

fetched data and the weight of a bit. Therefore, the largest binary word occurs in a 3-phase system when the fetched data is at a maximum and the weight is also a maximum. The largest binary word is then

$$3 * 250 * 323 = 242250 \quad .$$

This is an 18-bit data word in binary representation. An 8051 memory is only one byte long (8-bits). Therefore, the largest binary word uses 3 bytes. The BCD representation of this data is obviously 6 digits long. Therefore, the algorithm should be able to convert 18-bit (3-byte) binary data into 6-digit BCD data.

This algorithm employs a number of multiplication and division instructions. These instructions can manipulate 1 byte long binary data. Memories are also only one byte long. Therefore, it is convenient to treat binary data by one byte increments. Let BL, BM and BH be the decimal representation of the low byte, the medium byte and the high byte of the binary data. Thus, the integer representation of the binary data is given by

$$BH * 2^{16} + BM * 2^{8} + BL \quad , \qquad (6\text{-}1)$$

where $0 \le BH \le 3$, $0 \le BM < 2^8$ and $0 \le BL < 2^8$. Now, let D0, D1, D2, D3, D4 and D5 be the digits of the BCD representation of this binary data where D0 is the least significant digit

and D5 is the most significant digit. Therefore, the integer representation of this data is also given by

$$D5*10^5+D4*10^4+D3*10^3+D2*10^2+D1*10+D0 \quad ,$$

or

$$((((D5*10+D4)*10+D3)*10+D2)*10+D1)*10+D0 \quad . \qquad (6-2)$$

First, the basic idea of this algorithm is introduced. From expressions 6-1 and 6-2 the next equation is obtained.

$$BH*2^{16}+BM*2^8+BL$$
$$=((((D5*10+D4)*10+D3)*10+D2)*10+D1)*10+D0 \quad .$$

When both sides are divided by 10 one has

$$(BH*2^{16}+BM*2^8+BL)/10$$
$$=(((D5*10+D4)*10+D3)*10+D2)*10+D1+D0/10 \quad . \qquad (6-3)$$

The remainder of this division is D0. When the quotient of this division is divided by 10 the remainder is D1. In the same manner D2, D3, D4 and D5 are calculated.

A problem arises when this algorithm is executed by the 8051 microcomputer instruction set. The dividends of the divisions in this algorithm are, at most, 3 bytes long. However, the division instruction of 8051 can only deal with 1 byte long data. Therefore, a special

calculation is needed in order to perform these divisions.

The right hand side of equation 6-3 is changed as the following;

$$(BH*2^{16}+BM*2^{8}+BL)/10$$
$$=BH*65536/10+BH*256/10+BL$$
$$=BH*(6553+3/5)+BM*(25+3/5)+BL/10$$
$$=BH*6553+(BH/5)*3+BM*25+(BM/5)*3+BL/10 \quad . \quad (6-4)$$

The dividends in expression 6-4, BH, BM and BL, are all 1 byte long. Therefore, the 8051 can execute these divisions directly. Since BH is smaller than 4 the quotient of BH/5 is zero and the remainder is BH. Thus, BH/5 does not have to be done.

Let QM and RM be the quotient and the remainder of BM/5. QL and RL are similarly related to BL/10. Therefore,

$$BM/5 = QM + RM/5 \quad , \quad (6-5)$$

and

$$BL/10 = QL + RL/10 \quad , \quad (6-6)$$

where QM≤51, RM≤4, QL≤25 and RL≤9. From expression 6-4 and equations 6-5 and 6-6 the next expression is obtained.

$$(BH*2^{16}+BM*2^{8}+BL)/10$$

$$=BH*6553+(BH/5)*3+BM*25+(QM+RM/5)*3+QL+RL/10$$

$$=BH*6553+BM*25+QM*3+QL+(BH*6+RM*6+RL)/10 \quad . \qquad (6-7)$$

The dividend, BH*6+RM*6+RL, is at most 3*6+4*6+9=51. Therefore, it is one byte long and the division is performed easily.

When QR and RR represent the quotient and the remainder of the division in expression 6-7 this division is expressed by

$$(BH*6+RM*6+RL)/10 = QR + RR/10 \quad , \qquad (6-8)$$

where QR≤5 and RR≤9. Then expression 6-7 is changed as the following;

$$(BH*2^{16}+BM*2^{8}+BL)/10$$

$$=BH*6553+BM*25+QM*3+QL+QR+RR/10 \quad . \qquad (6-9)$$

According to equation 6-3, the remainder of expression 6-9 is equal to D0. Therefore, D0 is calculated using equation 6-8. In order to determine the higher digits, D1, D2, ···· , the integer part of expression 6-9 is treated as the original data, $BH*2^{16}+BM*2^{8}+BL$, and equation 6-8 is used.

The multipication BH*6553 in expression 6-9 can not be executed by the 1-byte long multipication instruction

easily. However, this is easily executed by the addition instruction because BH is smaller than 4. Therefore, the 8051 microcomputer instructions can easily convert binary data into BCD data using this algorithm. The flow chart of this algorithm is shown in Figure 6-2.

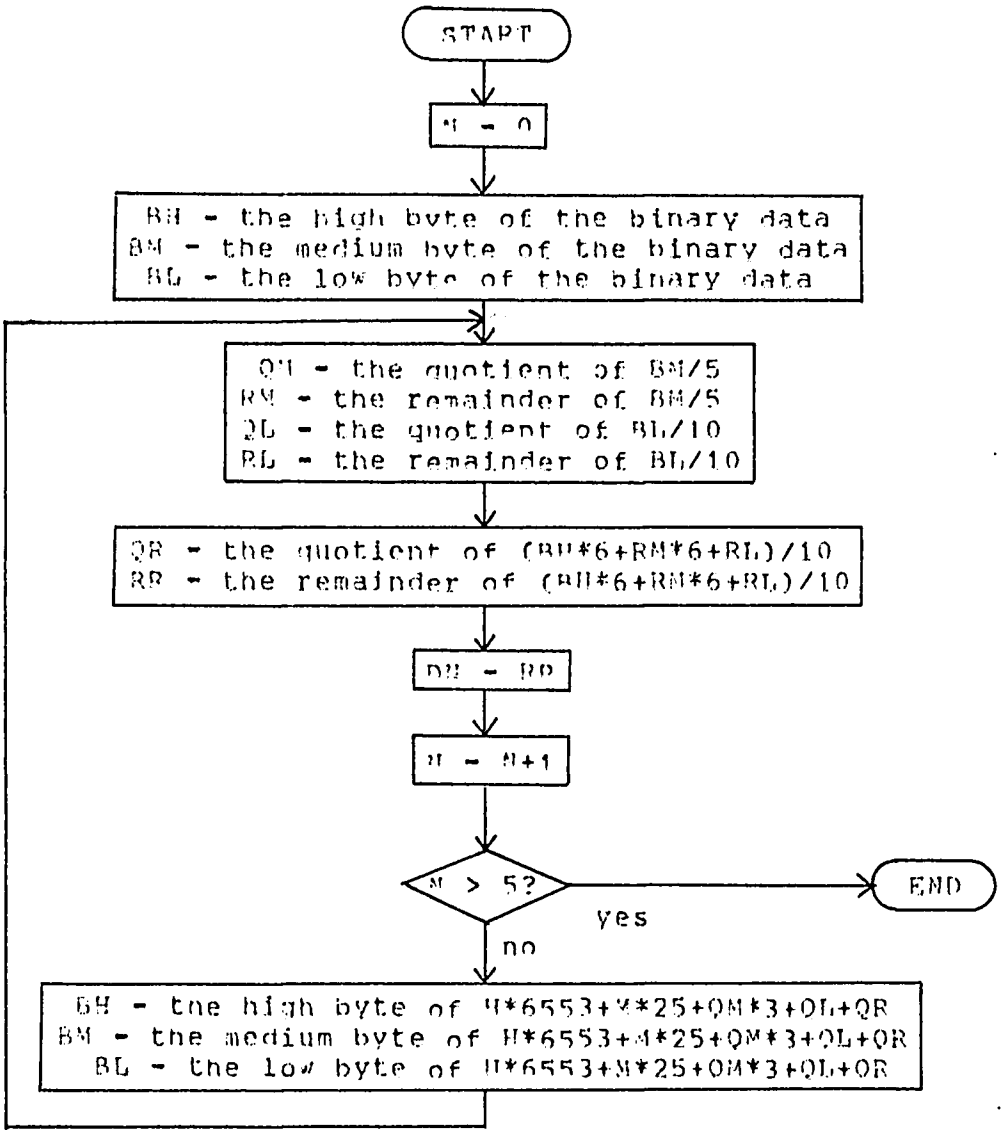


Figure 6-2: Binary to BCD algorithm

7. Circuit Performance

7.1 Theoretical Performance

The measurement accuracy depends on the following four factors:

- the nonlinear transfer characteristics of the CT,
- nonlinearity of the multiplier,
- conversion accuracy of the A/D converter,
- quantization error of A/D conversion.

These four factors can not be trimmed out by external means. The ripple at the output of the power computation circuit is also a factor in the measurement accuracy. However, the 120 Hz component of the current in the power distribution system, which determines the magnitude of the 60 Hz ripple (see sections 2.2 and 5.2), is not generally significant. Therefore, the ripple is not generally significant and is not figured in the analysis in this section. The following analysis is to determine the accuracy of the power monitor circuit for the maximum possible error.

The Amprobe SA60EM-1 CT causes, at most, 1 bit error at the output of the A/D converter according to the discussion in section 4.4. The Exar Integrated System

XR-2208C multiplier has a maximum irreducible output error of 1.0 % of full scale, or 100 mV. This error causes 2.5 bits of error at the output of the A/D converter. The conversion accuracy of the Analog Devices AD570 A/D converter is within 0.5 bits difference. Since the reconstruction level of the quantization is the middle of the decision levels the maximum quantization error is 0.5 bits. Therefore, the total error caused by these four factors is, at most, 4.5 bits at the output of the A/D converter.

Note that more than half the amount of this error is caused by the nonlinearity of the multiplier. Therefore, the measurement accuracy of the circuit is easily improved by employing a multiplier with smaller nonlinearity errors.

The maximum output error of the power monitor circuit is determined by using the maximum bit error and the weight of one bit. The result is shown in Table 7-1. In this table the maximum power in each case is when the voltage is 10 % above the nominal value and the current is 10 % above the maximum value.

The maximum output error is 1.89 % of the maximum value. Therefore, the output display of the three significant digits is considered to be meaningful.

power distribution system	current level	output error	(% of the maximum power)
		power of a line	total power for 3-line system
120 V line	low	630 W (1.89%)	1890 W (1.89%)
	high	612 W (1.83%)	1836 W (1.83%)
277 V line	low	1453.5 W (1.89%)	4360.5 W (1.89%)
	high	1413 W (1.83%)	4239 W (1.83%)

Table 7-1: Output error of the power monitor circuit

power distribution system	current level	output error	(% of the maximum power)
		power of a line	total power for 3-line system
120 V line	low	630 W (1.89%)	1890 W (1.89%)
	high	612 W (1.83%)	1836 W (1.83%)
277 V line	low	1453.5 W (1.89%)	4360.5 W (1.89%)
	high	1413 W (1.83%)	4239 W (1.83%)

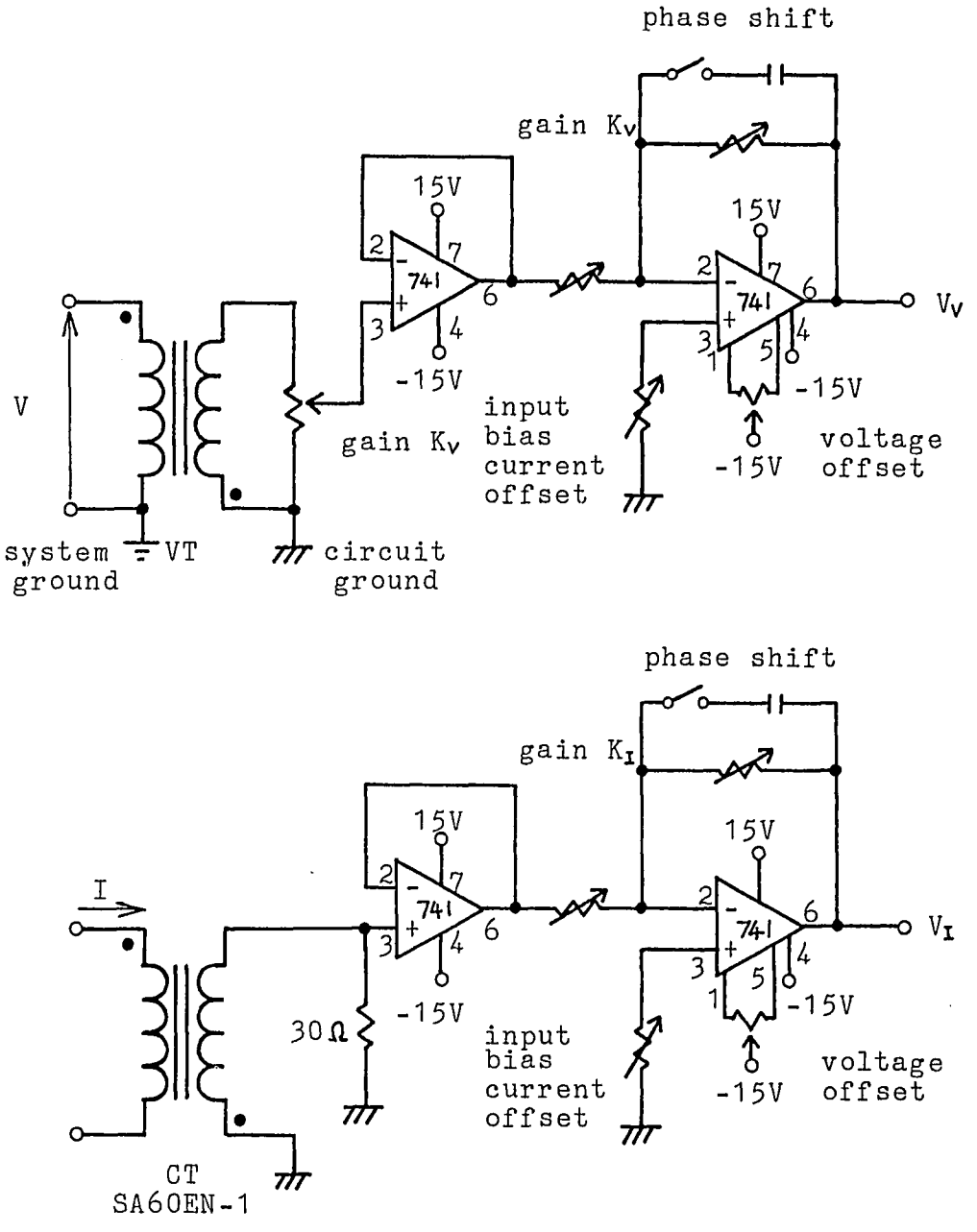
Table 7-1: Output error of the power monitor circuit

7.2 Test of Circuit Performance

The measurement accuracy was experimentally tested. The accuracy of power measurement on a 120 V, 1-line system was used. Such a test is sufficient because the measurement accuracy depends only on the four factors mentioned before. Moreover, only the case of various magnitude levels and phase angles of the 60 Hz sinusoidal current waveform was tested since the power in the specific power distribution system is a function of these current waveforms.

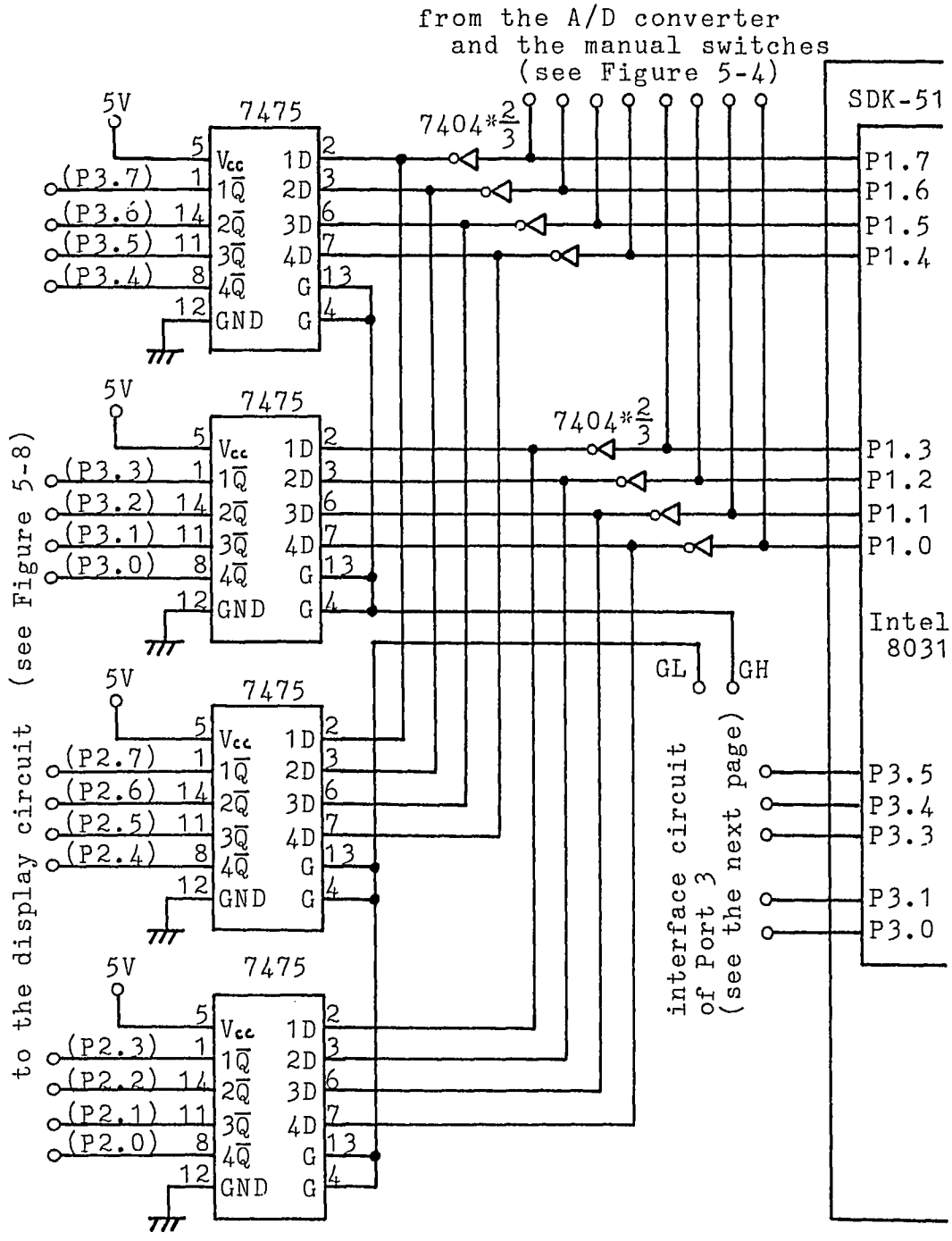
For convenience the designed power monitor circuit was modified so that the modification does not affect the measurement accuracy. In place of the power distribution system a special test circuit was used to examine the modified power monitor circuit since it is difficult to obtain 0 - 230 A currents in the laboratory. The modifications of the power monitor circuit and the test circuit are discussed first. Then, the result of the tests are shown.

The power monitor circuit for the test is shown in Figure 7-1. This circuit uses the SDK-51 (MCS-51 System Design Kit [7]) as the 8051 microcomputer in order to facilitate the programing. The use of the SDK-51 changes the interface circuit of the microcomputer. However, the change of the interface circuit does not affect the



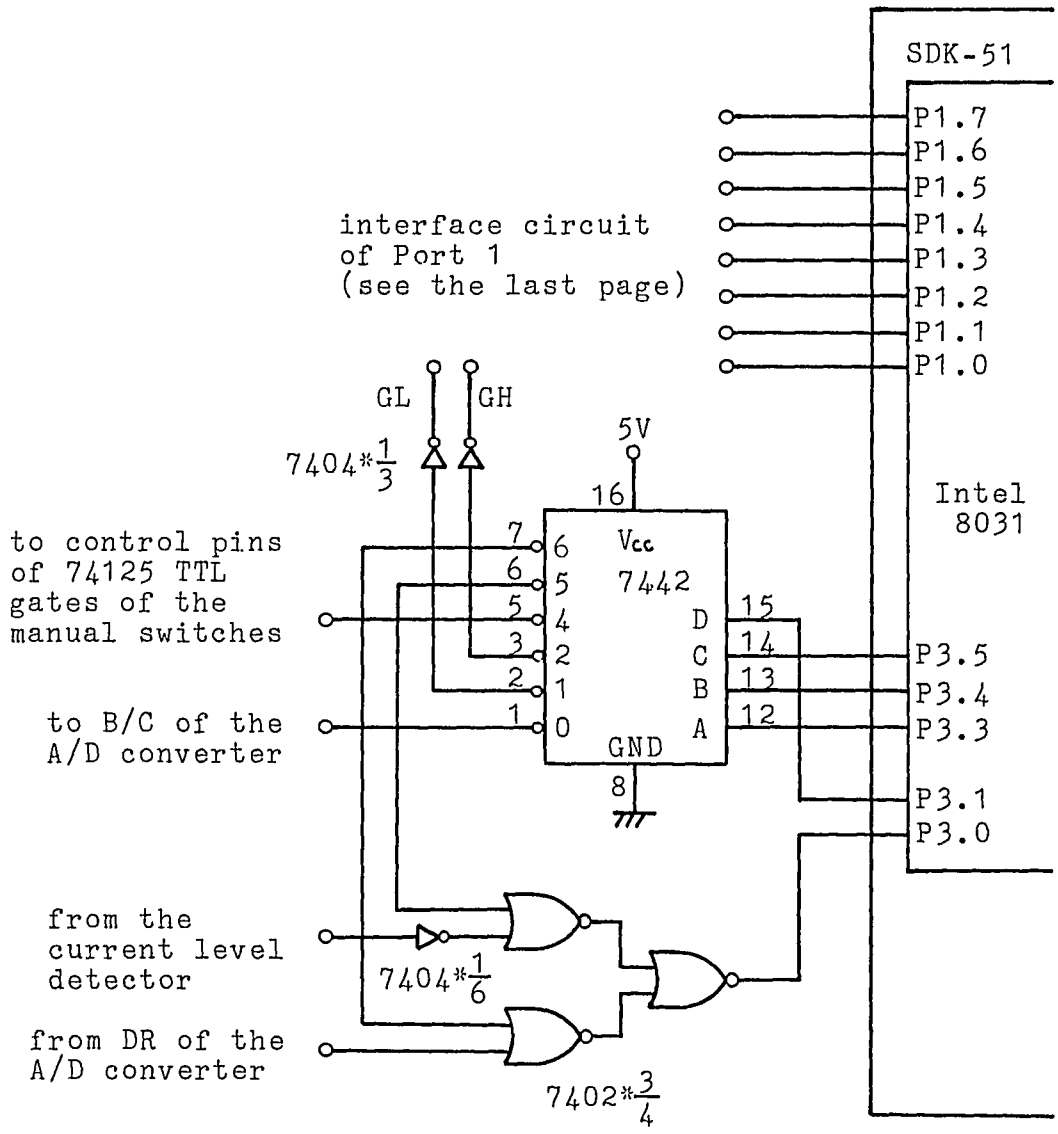
(a) voltage and current measurement circuit

Figure 7-1: Modified power monitor circuit
(1 of 3)



(b) interface circuit of SDK-51 Port 1

Figure 7-1: Modified power monitor circuit
(2 of 3)



(c) interface circuit of SDK-51 Port 3

Figure 7-1: Modified power monitor circuit
(3 of 3)

accuracy of the power measurement. The microcomputer program is also changed for this interface circuit. In order to measure the power of the 1-line system only one voltage and current set need be measured. Therefore, the voltage and current measurement circuit is modified and the line selection switches are removed. The configuration of the voltage and current measurement circuit is explained later because it is related to the test circuit of this modified power monitor circuit.

The test circuit and a part of the modified power monitor circuit are shown in Figure 7-2. The voltage of the 120 V power distribution system, $\overline{V}_{120}$, is fed to the VT. $\overline{V}_{120}$ is also fed to the step-down transformer. The secondary winding of the step-down transformer is connected to the CT through the resistor R_1 in order to supply current to the CT's primary winding. The secondary voltage of this step-down transformer is controllable. Therefore, the magnitude of the CT's primary current can be changed by controlling the secondary voltage of the step-down transformer. The magnitude of the CT's primary current can be determined by the voltage across R_1, V_{R1}. The primary turns of the CT is 200. The equivalent primary current when the CT's primary turn is one, I_{p1}, is obtained from

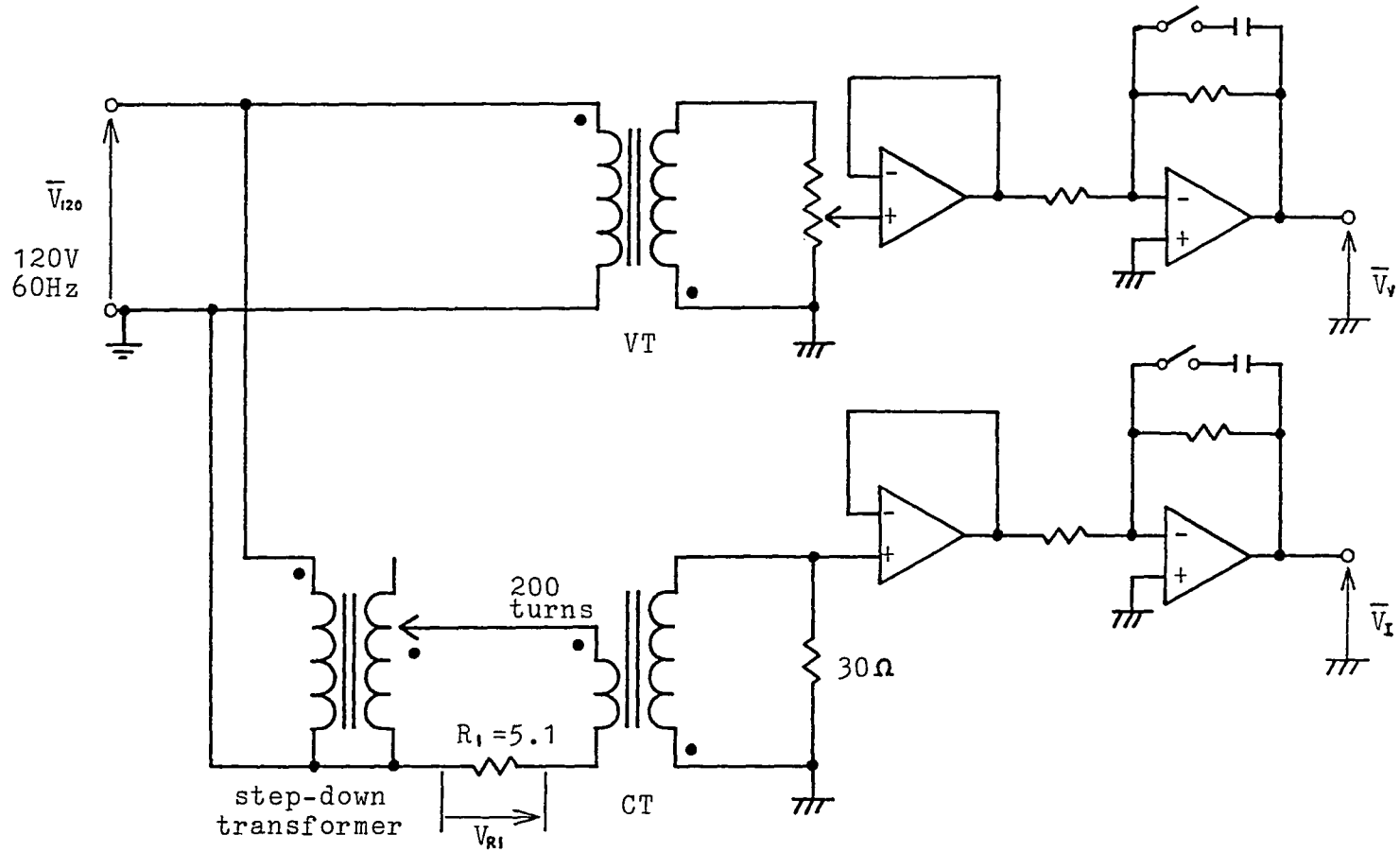


Figure 7-2: Test circuit and a part of the modified power monitor circuit

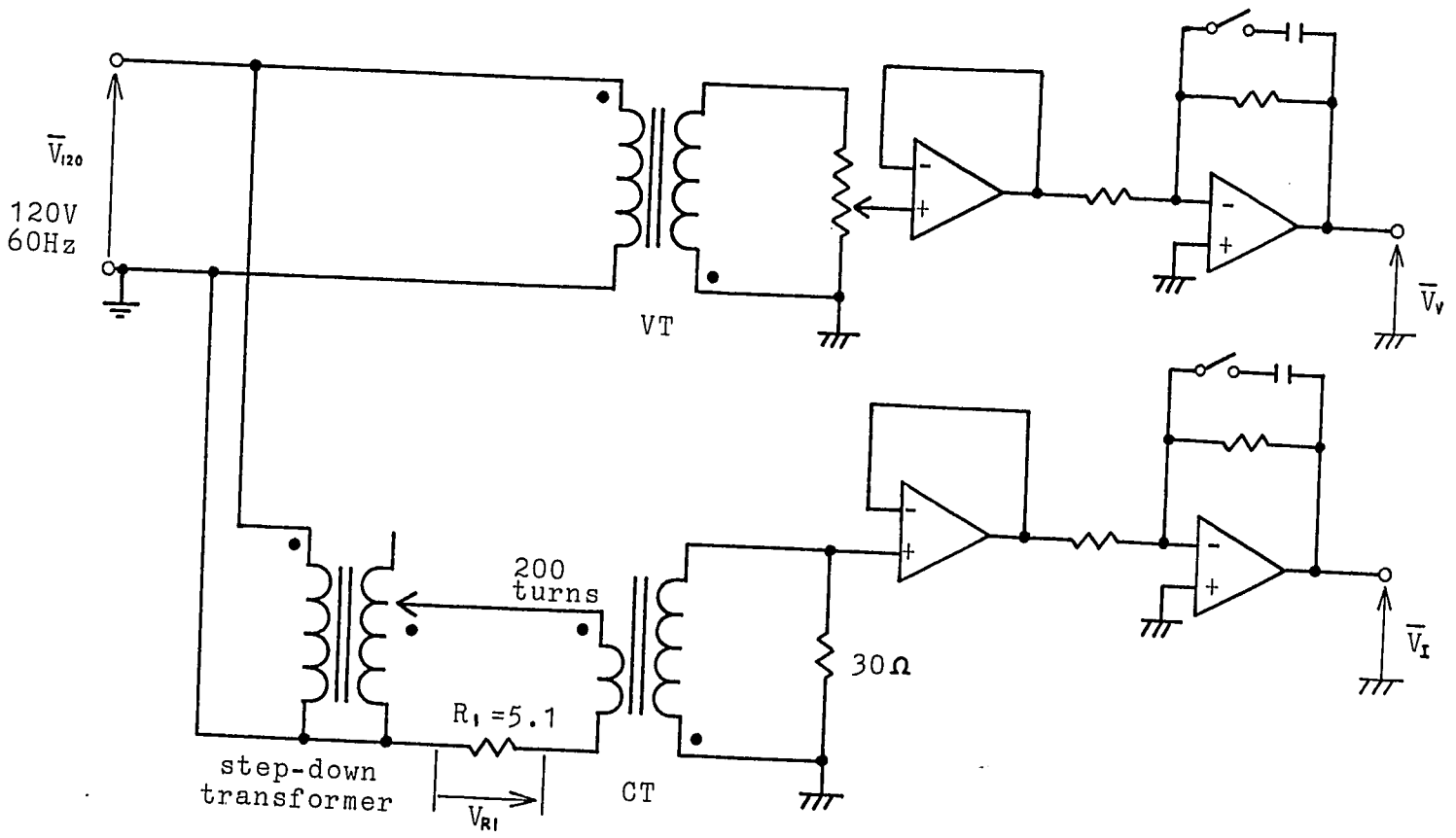


Figure 7-2: Test circuit and a part of the modified power monitor circuit

$$I_{pl} = 200\ V_{RI}/R_I \quad .$$

Now this current, I_{pl}, can be assumed to be the magnitude of the current in the power distribution system.

Because of the step-down transformer and the secondary loads of this transformer $\overline{V}_{120}$ and $\overline{I}_{pl}$ have some phase angle difference. However, the phase angle difference between $\overline{V}_{120}$ and $\overline{I}_{pl}$ was experimentally measured and found to be constant at the magnitude range 0 - 230 A of $\overline{I}_{pl}$. In other words, current waveforms of various levels are obtained by controlling the secondary voltage of the step-down transformer. However, the phase angle of that waveform remains constant.

According to the discussion in section 4.4 the phase angle difference between $\overline{V}_V$ and $\overline{V}_{I60}$, i.e. δ, of the designed power monitor circuit equals that between the voltage and the 60 Hz component of the current of the system, $\varphi_{60}-\theta$, when the current in the system is in the high levels. Thus, δ of this circuit can be assumed to equal $\varphi_{60}-\theta$ when I_{pl} is in the high level. The δ of this circuit can be changed by the function of the LPF after the VT or CT. That is, changing the δ can imitate the various phase angles of the current waveform in the power distribution system. The magnitude of V_V and V_I can be adjusted to the proper values by the potentiometers.

The two assumptions about I_{p1} and δ do not affect the measurement accuracy of the circuit. Therefore, using this test circuit and the modified power monitor circuit the accuracy of the power measurement of the designed power monitor circuit can be determined. The power of the power distribution system (imitative power of the test circuit) can be calculated by using the relation $120I_{p1}\cos\delta$. Figures 7-3 through 7-7 show the output indications of the power monitor circuit vs. the magnitude of the current in the system for different phase angles. The figures also show the imitative power of the test circuit and the maximum possible error mentioned in the last section. Errors of all the output indications of the power monitor circuit are less than the predicted maximum possible error.

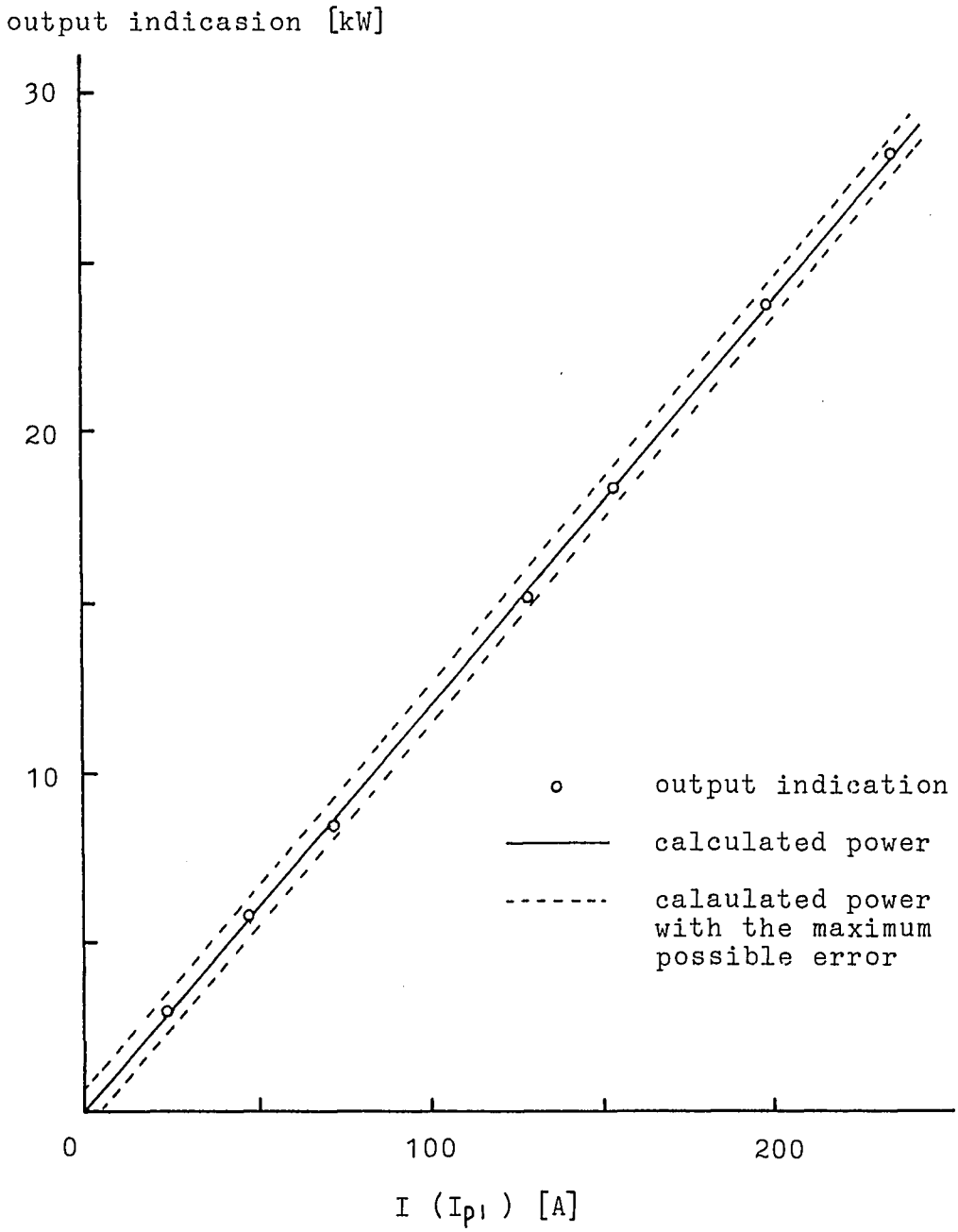


Figure 7-3: Output indications of the power monitor circuit when $\varphi_{60} - \theta = 0$ ($\delta = 0$)

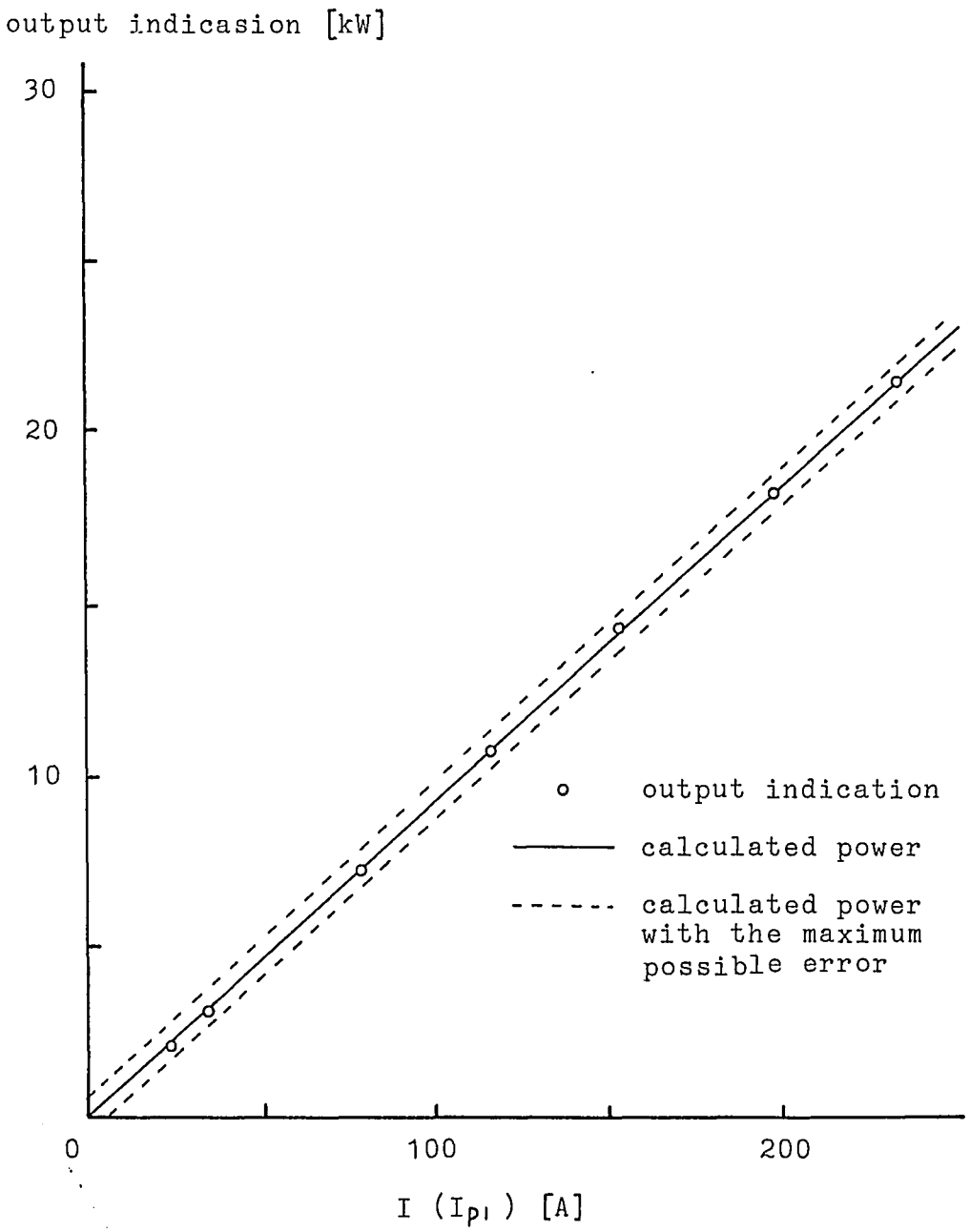


Figure 7-4: Output indications of the power monitor circuit when $\varphi_{60} - \theta = 20°$ ($\delta = 20°$)

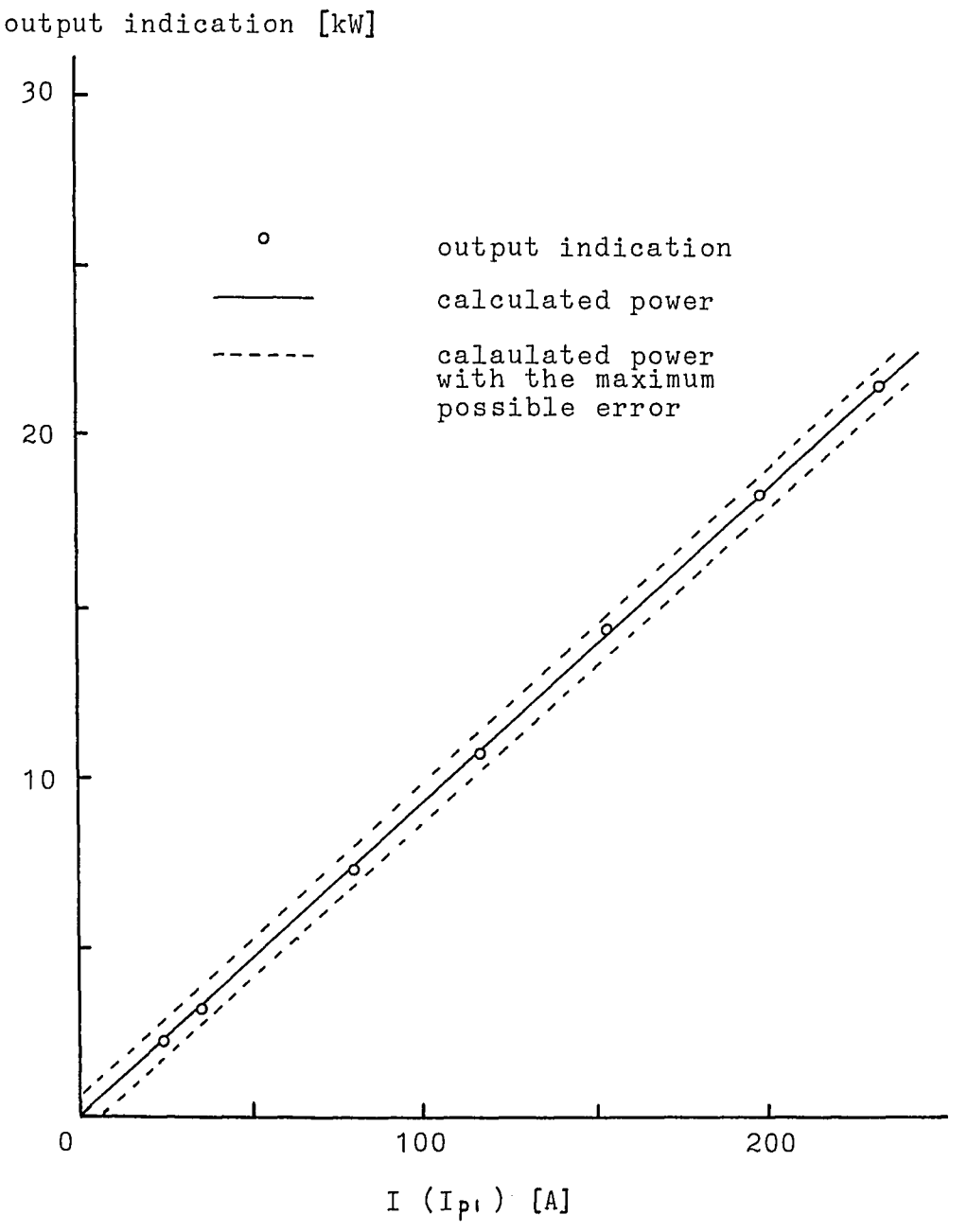


Figure 7-5: Output indicasions of the power monitor circuit when $\varphi_{60} - \theta = 40°$ ($\delta = 40°$)

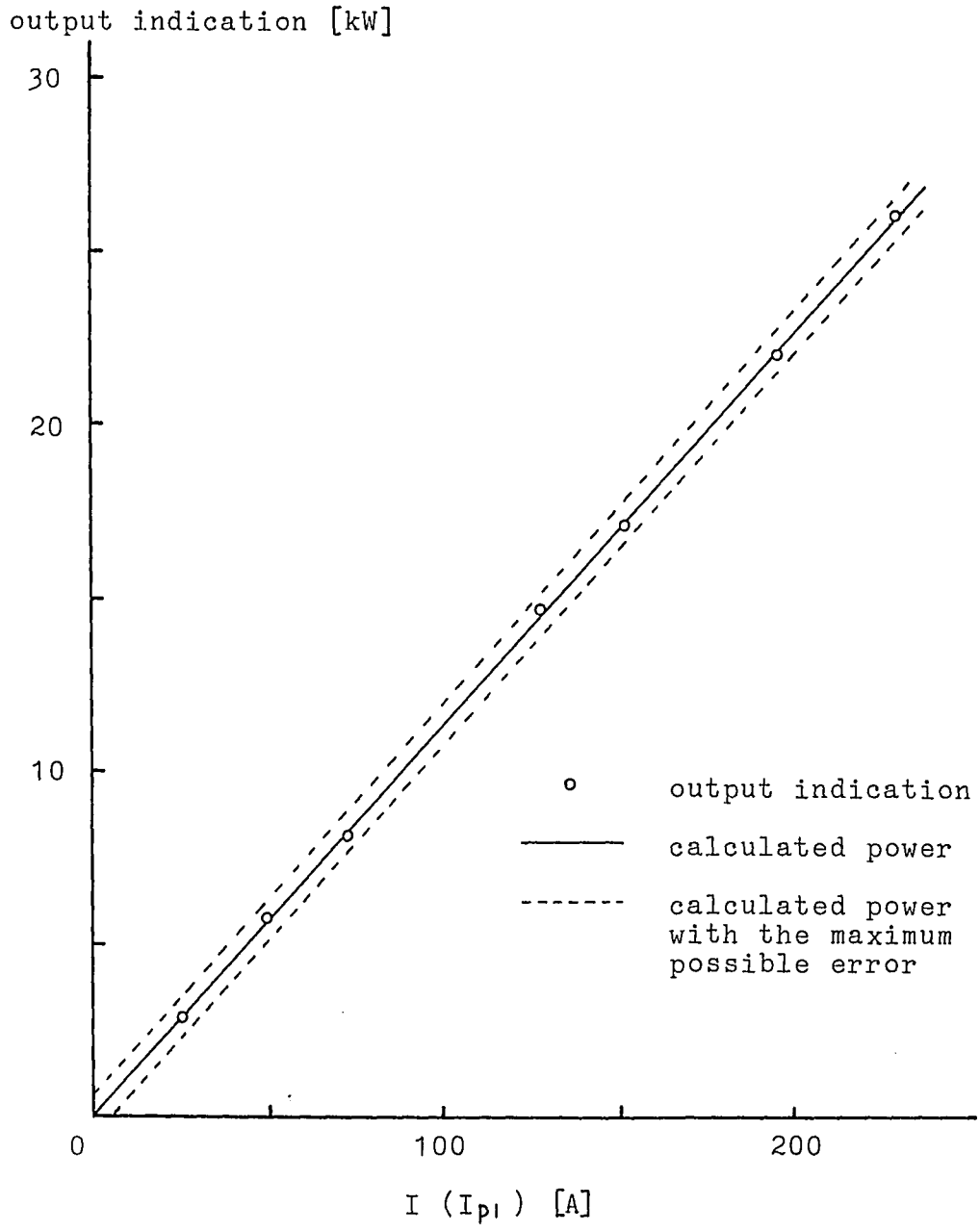


Figure 7-6: Output indications of the power monitor circuit when $\varphi_{60} - \theta = -20°$ ($\delta = -20°$)

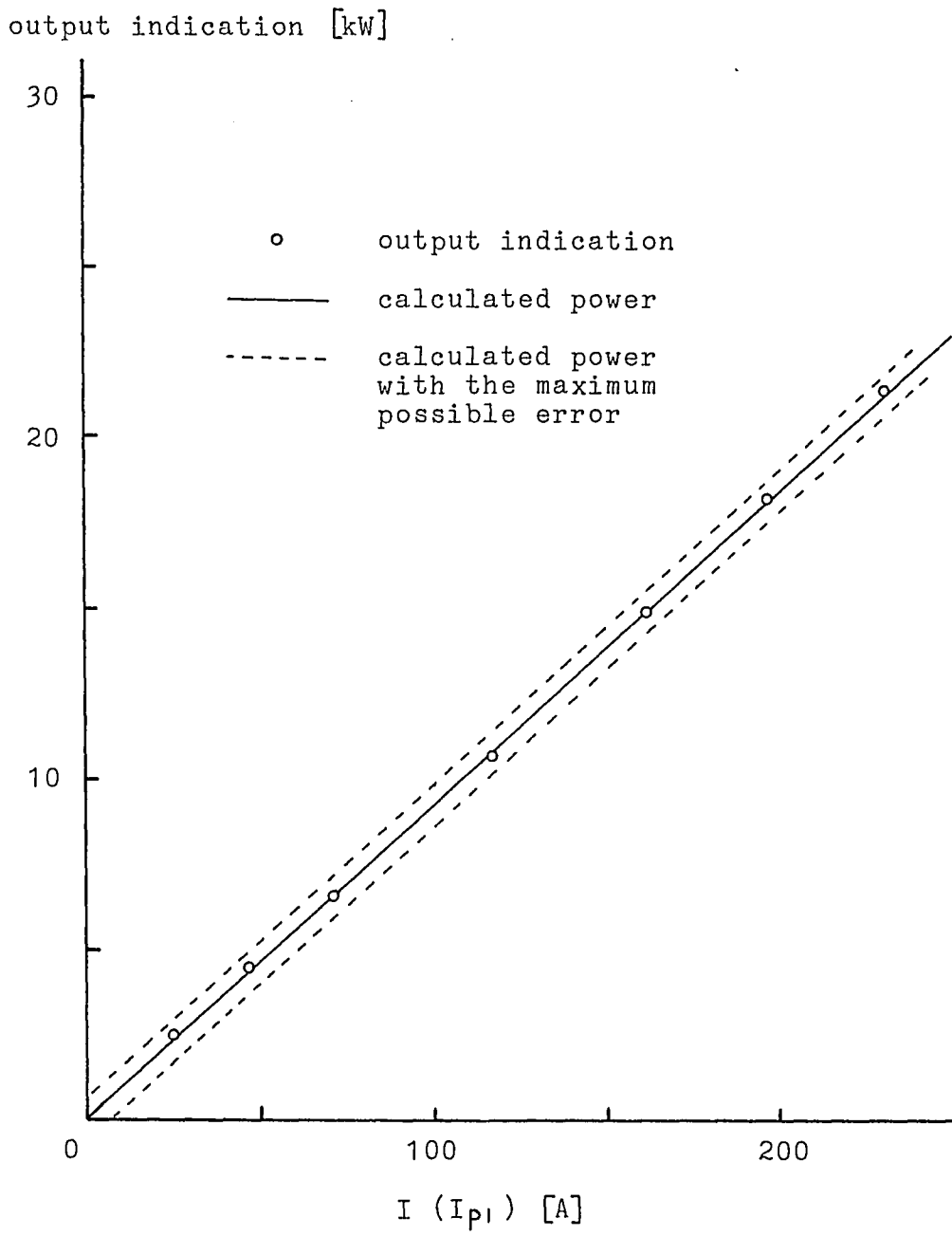


Figure 7-7: Output indications of the power monitor circuit when $\varphi_{60} - \theta = -40°$ ($\delta = -40°$)

8. Conclusion

In the power monitor circuit CT's are used for current measurement. In this case the power measurement in the power distribution system must be based on the fact that the power in the system is determined by the voltage waveform and the 60 Hz component of the current waveform of the system. The reason is that it is impossible to measure the exact waveform of the current by a CT because the CT's transfer characteristics depend upon frequency. Moreover, in order to reduce the error caused by the CT some special circuits are needed to compensate for the CT's transfer characteristics for the various current levels. The design of the power monitor circuit is based on these arguments and the error caused by a particular CT is held within 1 bit out of 2^8 bit for the full scale.

In this work the power monitor circuit employs a microcomputer for the digital computation. Usually a power monitor circuit works in a control system. Therefore, the microcomputer can be also used to communicate to the other circuits in the control system. Because of the powerful function of the microcomputer several different circuits including other power monitor circuits can share the same microcomputer for calculation or control uses. Moreover, the microcomputer can easily

add new functions to the power monitor circuit: e.g., energy and peak power measurements in the power distribution system. These additional quantities are also useful to know in power distribution systems.

In this work it is assumed that all other CT's of the same model have exactly the same transfer characteristics determined for one particular CT. However, different CT's of the same model usually have slightly different transfer characteristics. In other words, the difference of the transfer characteristics among CT's in the same model has not been considered in this work. However, this is as important as the consideration of the transfer characteristics themselves because well matched CT's are important. Further research could be done to consider this difference and chose CT's which cause the smallest measurement error.

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Appendix A

Analysis of the Equivalent Circuit for a Current Transformer

The quantities I_e, X_e, R_e and R_{ws}, as shown in Figure 3-7, are now calculated. The phasor diagram of this circuit is shown in Figure A-1. N, R_{ws} and R_2 are assumed known, whereas E, V_{R2}, V_2, V_1 and ζ are assumed to be measured quantities. I_e is given by

$$I_e = V_{R2} / R_2 \quad , \tag{3-5}$$

where $\overline{V}_{R2}$ is the voltage across R_2. The imaginary parts of $\overline{V}_2$ and $\overline{E}$ are equal

$$V_2 \sin\eta = E \sin\zeta \quad ,$$

where η is the phase angle difference between $\overline{V}_2$ and $\overline{I}_e$. Thus, η is given by

$$\eta = \sin^{-1}\{(E/V_2)\sin\zeta\} \quad . \tag{A-1}$$

The real part of $\overline{V}_2$ is the voltage across the resistance R_{ws} and R_e,

$$V_2 \cos\eta = I_e (R_{ws} + R_e) \quad . \tag{A-2}$$

By using equations A-1 and A-2 R_e is given by

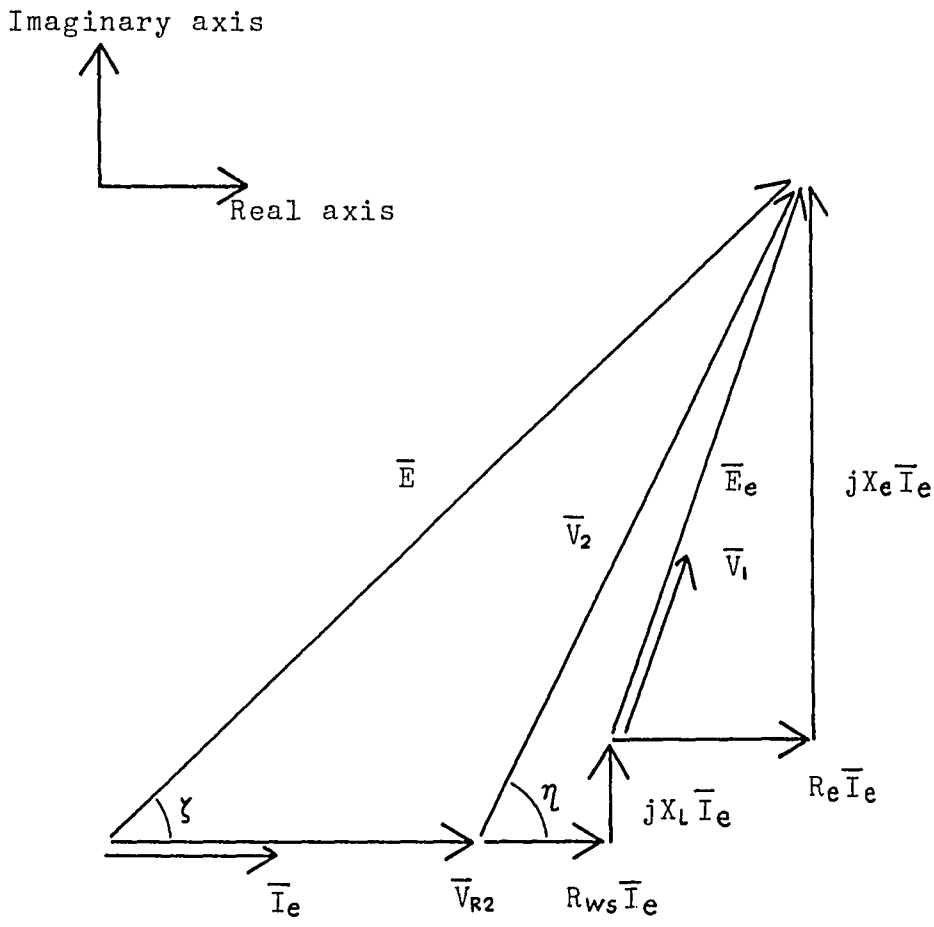

Figure A-1: Phasor diagram of the circuit in Figure 3-7

$$R_e = (V_2 / I_e)\cos[\sin^{-1}((E/V_2)\sin\zeta)] - R_{ws} \quad . \qquad (3\text{-}6)$$

Because the primary current is zero E_e is given by

$$E_e = N V_1 \quad . \qquad (A\text{-}3)$$

E_e is the sum of the voltages across R_e and jX_e. Therefore,

$$E_e = \sqrt{I_e^2 R_e^2 + I_e^2 X_e^2} \quad . \qquad (A\text{-}4)$$

Using equations A-3 and A-4 X_e is given by

$$X_e = \sqrt{(N^2 V_1^2 / I_e^2) - R_e^2} \quad . \qquad (3\text{-}7)$$

The imaginary part of $\overline{E}$ is the sum of the voltages across X_e and X_{Ls}. Therefore,

$$E \sin\zeta = I_e X_e + I_e X_{Ls} \quad .$$

Thus, X_{Ls} is given by

$$X_{Ls} = (E/I_e)\sin\zeta - X_e \quad . \qquad (3\text{-}8)$$

Using these calculated values, I_e, R_e, X_e and X_{Ls}, I_s and I_1 of the circuit in Figure 3-6 can be calculated. In this circuit R_{ws} and R_L are also known. The phasor diagram in the complex plane of this circuit is shown in Figure A-2. $\overline{E}_e$ is the voltage across R_e and jX_e when $\overline{I}_e$ flows. Therefore, E_e is given by

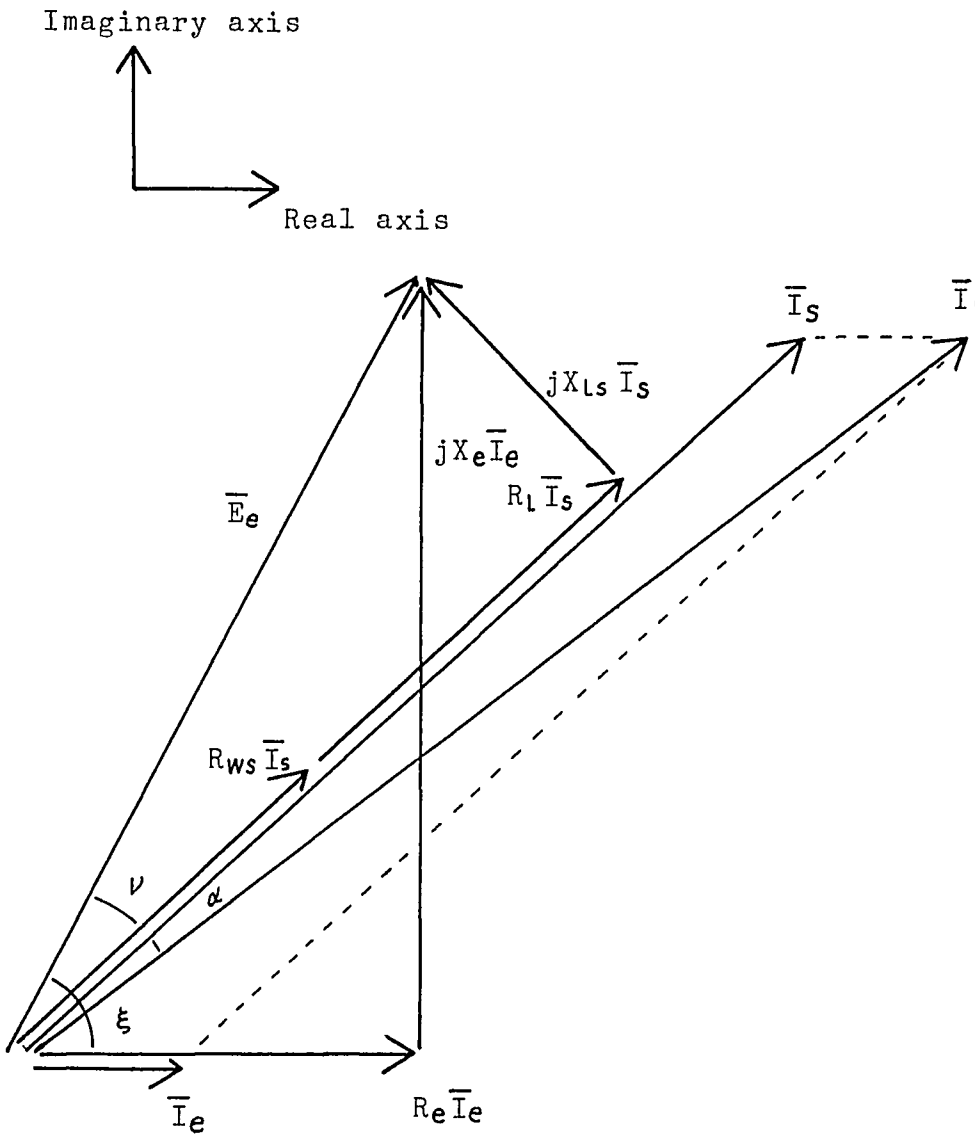

Figure A-2: Phasor diagram of the circuit in Figure 3-6

$$E_e = I_e\sqrt{R_e^2 + X_e^2} \quad . \qquad (A\text{-}5)$$

When $\overline{I}_s$ flows the voltage across jX_{Ls}, R_{ws} and R_L is also $\overline{E}_e$. Therefore,

$$E_e = I_s\sqrt{(R_L + R_{ws})^2 + X_{Ls}^2} \quad . \qquad (A\text{-}6)$$

Using equations A-5 and A-6 I_s is given by

$$I_s = I_e\sqrt{R_e^2 + X_e^2} \,/\, \sqrt{(R_L + R_{ws})^2 + X_{Ls}^2} \quad . \qquad (3\text{-}9)$$

Now the phase angle difference between $\overline{I}_s$ and $\overline{E}_e$ and the one between $\overline{I}_e$ and $\overline{E}_e$ are denoted ν and ξ respectively. ν and ξ are given by

$$\nu = \tan^{-1}(X_{Ls} / (R_{ws} + R_L))$$

$$\xi = \tan^{-1}(X_e / R_e) \quad .$$

Because $\overline{I}_l$ is the sum of $\overline{I}_s$ and $\overline{I}_e$ I_l is given by the following formula:

$$I_l = \sqrt{(I_e\cos(\xi - \nu) + I_s)^2 + (I_e\sin(\xi - \nu))^2} \quad . \qquad (3\text{-}10)$$

In the phasor diagram $\overline{I}_l$ and $\overline{I}_e$ satisfy following relation:

$$I_l \sin\alpha = I_e\sin(\xi - \nu) \quad .$$

Then α is given by

$$\alpha = \sin^{-1}((I_e / I_l)\sin(\xi - \nu)) \quad . \qquad (3\text{-}11)$$

Vita

Takashi Tsuda was born in Osaka, Japan on July 26, 1954. He is the son of Hiroshi and Towako Tsuda. He graduated from University of Osaka Prefecture in 1978 with a degree of Bachelor of Engineering in Electronics. Since 1978 he has been employed by Matsushita Electric Works, Ltd. in Osaka, Japan, where he joined several projects in Lighting Division until 1980.