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A STUDY OF TWO-DIMENSIONAL EFFECTS IN METAL/TUNNEL-OXIDE/N/P+ SILICON SWITCHING DEVICES

by

Umesh K. Mishra

A Thesis

Presented to the Graduate Committee

of Lehigh University

In Candidacy for the Degree of

Master of Science

in

Electrical Engineering

Lehigh University

1980

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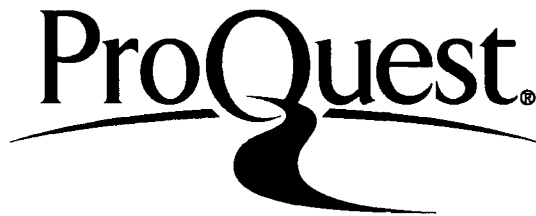

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Dec. 19, 1980.
Date

Professor in Charge

Chairman of Department

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LIST OF SYMBOLS

A^*	Richardson constant, A cm^{-2} $°K^{-2}$
A_1	effective device area $(= L + 2X_d)^2$, cm^2
A_j	isolated p^+-n junction area, cm^2
A_{ox}	tunnel-oxide area, cm^2
C_{ox}	oxide capacitance, F cm^{-2}
d_{ox}	tunnel-oxide thickness, cm
D_p	diffusion coefficient for holes, $cm^2 sec^{-1}$
$E_c(0)$	silicon conduction band edge at Si-SiO_2 interface, eV
E_{Fm}	Fermi level of metal, eV
E_{Fn}	quasi-Fermi level for electrons in neutral epi-layer, eV
$E_{Fn}(0)$	quasi-Fermi level for electrons at Si-SiO_2 interface, eV
$E_{Fp}(0)$	quasi-Fermi level for holes at Si-SiO_2 interface, eV
E_{Fp^+}	Fermi level of p^+ substrate, eV
E_g	silicon band-gap, eV
$E_v(0)$	silicon valence band edge at Si-SiO_2 interface, eV
$E_v(X_d)$	silicon valence band edge at $X = X_d$, eV
I	device current, A
I_g	generation current of the surface depletion region, A
I_H	holding current, A
I_{nj}	electron diffusion current, A
I_{nt}	electron tunnel current from metal to silicon conduction band, A
I_p	total hole current, A

I_{pi} hole current reaching $Si-SiO_2$ interface, A

I_{pj} hole diffusion current across the p^+-n junction, A

$I_{pj1}(I_{pj2}, I_{pj3})$ hole diffusion current in Region I (II,III), A

I_{pt} hole tunnel current from silicon valence band to metal, A

I_{rj} p^+-n junction recombination current, A

I_{rn} recombination current in neutral epi-layer, A

I_s switching current, A

J_{ei} injected electron current density, A cm^{-2}

J_g generation current density of the surface depletion region, A cm^{-2}

J_{nj} electron diffusion current density, A cm^{-2}

J_{nt} electron tunnel current density from metal to silicon conduction band, A cm^{-2}

J_{pj} hole diffusion current density across the p^+-n junction, A cm^{-2}

J_{pt} hole tunnel current density from silicon valence band to metal, A cm^{-2}

J_{rj} p^+-n junction recombination current density, A cm^{-2}

k Boltzman's constant, $eV°K^{-1}$

L tunnel-oxide side dimension, cm

L_f fringing length of the electron tunnel current, cm

L_p hole diffusion length, cm

M multiplication factor, dimensionless

MISS metal insulator semiconductor switch

MIST metal insulator semiconductor thyristor

OMIST optical metal insulator semiconductor thyristor

N_a acceptor concentration in p^+ substrate, cm^{-3}

N_d	donor concentration in n epi-layer, cm^{-3}
n_i	intrinsic carrier concentration, cm^{-3}
N_v	density of states at silicon valence band edge, cm^{-3}
PAR	perimeter to area ratio of device, cm^{-1}
p(0)	hole density at $Si-SiO_2$ interface, cm^{-3}
p_{no}	equilibrium hole concentration in n epi-layer, cm^{-3}
q	electronic charge, 1.6×10^{-19} coul
RFM	regenerative feedback mechanism
Q_d	depletion charge, coul cm^{-2}
Q_g	gate charge, coul cm^{-2}
Q_i	inversion charge, coul cm^{-2}
Q_{ss}	fixed interface charge density, coul cm^{-2}
r_j	equivalent radius of isolated p^+-n junction area, cm
r_o	equivalent radius of effective device area, cm
r_s	equivalent radius of short-base diode (Region II), cm
T	absolute temperature, °K
V	total voltage across the device, V
V_{bd}	avalanche breakdown voltage, V
V_H	holding voltage, V
V_j	p^+-n junction voltage, V
V_s	switching voltage, V
V_{pt}	punch-through voltage, V
V_T	thermal voltage (= kT/q), V
W_j	p^+-n junction depletion width, cm
W_n	width of neutral region, cm

X_d	surface depletion width, cm
X_e	epi-layer thickness, cm
δ	$E_{Fm} - E_c(0)$, eV
ε_{ox}	silicon dioxide dielectric constant, F cm^{-1}
ε_s	silicon dielectric constant, F cm^{-1}
τ_g	generation lifetime in p^+-n junction, sec
τ_o	hole recombination lifetime in bulk epi-layer, sec
τ_1	hole recombination lifetime in p^+-n junction depletion region, sec
ϕ_{Bi}	p^+-n junction built-in potential, V
ϕ_{ms}	metal-semiconductor work function difference, V
ψ_s	semiconductor surface potential, V
χ_n	tunnel-oxide barrier height for electrons, eV
χ_p	tunnel-oxide barrier height for holes, eV

ABSTRACT

Effects of V-groove isolation on the two-terminal D.C. characteristics of the metal/tunnel-oxide/n/p^+ silicon switching devices have been studied.

Experimental results show that the switching characteristics of non-isolated devices are strongly dependent on area and the area-to-perimeter ratio of the device. To carry out a systematic investigation of this phenomenon, devices in this study were isolated using V-grooves of various areas. For a given tunnel-oxide thickness and area, it was found that the switching voltage, V_H, and holding current, I_H, is essentially independent of isolation area. Based on this experimental observation ($I_s \simeq$ constant), a qualitative physical argument is presented which determines the switching criterion for the device, and concludes that the transition from the OFF to the ON state, and vice versa, is solely dependent on the properties of the MIS diode; in particular, the minority carrier concentration at the Si-SiO_2 interface. In agreement with experimental results, a decrease in switching current and holding current is predicted for an increase in tunnel-oxide thickness.

Finally a simple two-dimensional model has been derived which effectively explains the variation of switching voltage and holding current with changes in the p^+-n junction area.

INTRODUCTION

1.1 THE METAL INSULATOR SEMICONDUCTOR SWITCH (MISS)

Recently, the Metal-Insulator-Semiconductor-Switch (MISS) has been the focus of considerable attention. This device has been received with increasing enthusiasm because of three primary reasons:

(i) Ease of fabrication

(ii) Compatibility with existing technologies and, most importantly,

(iii) Performance of a function not hitherto obtained by an easily integrable device (a bistable switch).

The basic structure of the MISS is shown schematically in Fig. 1.1. It consists primarily of a semi-insulating film of silicon dioxide grown on the surface of an n-epitaxial layer formed on a p^+ substrate wafer of <100> orientation, sandwiched between two electrodes. Neither the choice of the semi-insulating layer, nor of the metal electrodes is limited to those just mentioned, and a wide range of materials has been investigated. Yamamoto et al (1-1, 1-2), who first demonstrated the switching behaviour of the MISS, used a 20-30 Å tunnel-oxide (SiO_2) for the semi-insulating film. Later Kroger and Wegener demonstrated the viability of Si_3N_4 (1-3) and polycrystalline silicon (1-4). Results of an in-depth investigation carried out by them, on the effect of various other semi-insulating films on device characteristics is presented in Ref. (1-5). Various metals can be used as electrodes for the device. Aluminum (1-1), platinum (1-1), gold (1-2), molybdenum

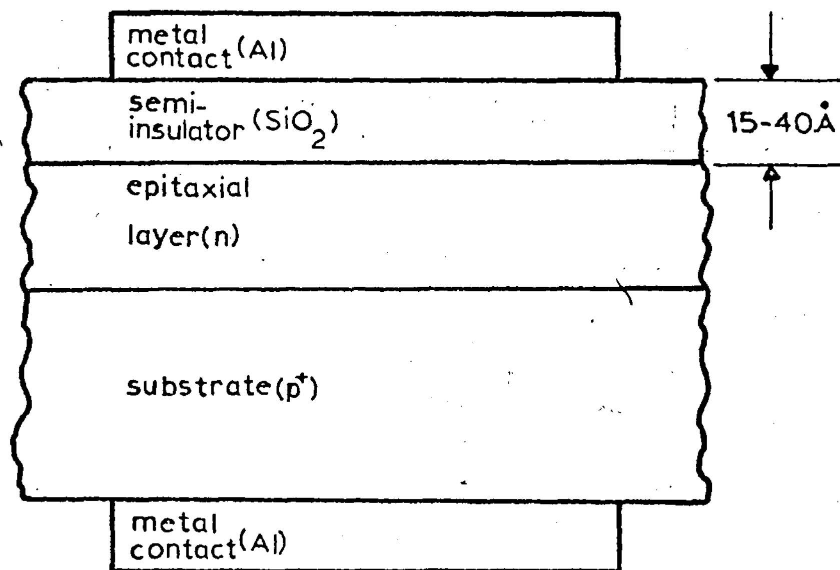

Fig. 1.1 Schematic of basic MISS structure under study (not drawn to scale).

(1-3) and chromium (1-4) are a few examples of metals that have been researched thus far. However, most of the work done to date has been on devices using a tunnel-oxide (20-40 Å SiO_2) as the semi-insulating film and aluminum as the metal electrode.

The MISS performs the function of an electronic switch, in that it exhibits two stable states, the ON and OFF states (see Fig. 1.2). The ratio of the resistance of the two states is $\sim 10^6$. As the applied voltage, V_A, is increased negatively from zero, the device exists in the high impedance or OFF state. The switching voltage, V_S, is the maximum voltage that can exist across the device before the MISS switches from the OFF to the ON state. The switching current, I_S, is the current at the switching point. The holding current, I_H, is the minimum current necessary to sustain the device in the low impedance ON state. The holding voltage, V_H, is the voltage across the MISS at the holding point. Fig. 1.2 shows a schematic of the I-V characteristics of a MISS. The basic circuit configuration in which the device is operated is presented in the inset. It will be noted that the I-V characteristic of the MISS is similar to that of a 'pnpn' (Shockley) diode. However, there are important differences between the two:

(i) The MISS possesses a higher switching speed, measured as less than two nanoseconds (1-2).

(ii) Unlike the 'pnpn' diode, the fabrication of the MISS involves very few high temperature processes, making it a simpler device to fabricate.

(iii) The most important advantage of the MISS over the 'pnpn' diode

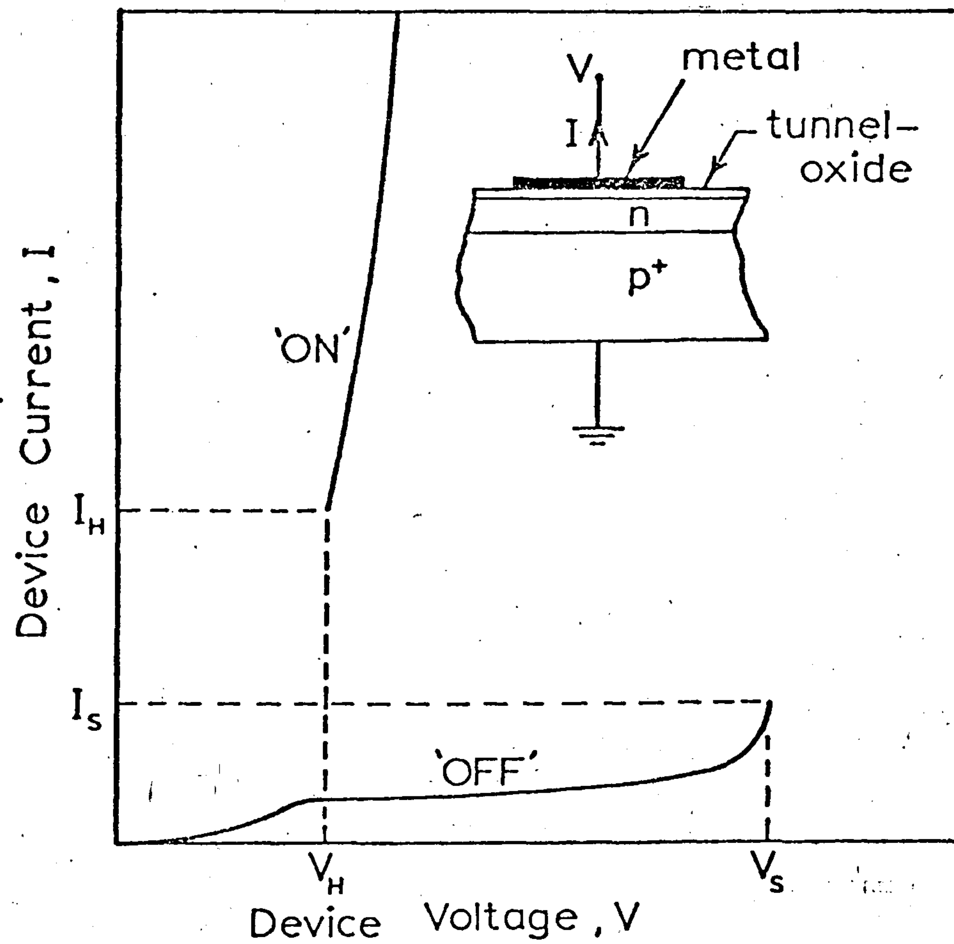

Fig. 1.2 Schematic of the I-V curve of a MISS device defining the parameters I_s, V_s, I_H and V_H that characterize the device.

INSET: Basic MISS structure.

is the ease with which it can be integrated i.e. it is amenable to fabrication with standard IC technology.

1.2 THE MISS: HISTORICAL REVIEW

In the first report of the switching phenomenon (1-1), it was speculated that the formation of an inversion layer under the oxide, caused by hole injection from the substrate, resulted in a very high voltage across the device, causing two electron currents to flow:

(a) a hot electron tunnel current from the conduction band of the nSi to the metal (note that the electrons flow from the metal to the conduction band), and

(b) a current caused by the tunneling of electrons from the metal to the Si-SiO_2 interface states and their subsequent recombination with the holes present in the inversion layer.

Kroger and Wegener (1-3) recognised the OFF state to be a deeply-depleted state in the semiconductor. This was believed to be caused by the leaky insulator allowing a finite tunneling current to drain off excess minority carriers from the Si-SiO_2 interface. This minority carrier tunneling through the semi-insulator prevented the formation of an inversion layer, forcing the MISS to remain in the high-impedance state.

Yamamoto et al. in a later publication (1-2) postulated a surface feedback mechanism based on current multiplication at the insulator-semiconductor interface (1-6) as being responsible for the negative resistance behaviour of the MISS. Simmons and El-Badry (1-7)

presented a semi-quantitative theory establishing two types of switching in the MISS: (a) the punch-through mode and (b) the avalanche mode. Those devices in which the surface depletion region extended through the lightly-doped ($N_d < 10^{16} cm^{-3}$) epitaxial layer to the underlying p^+-n junction, were recognised to be operating in the punch-through mode. On the other hand, the avalanche mode identified those devices in which avalanche breakdown in the higher doped epitaxial layer ($N_d > 10^{16} cm^{-3}$) occurred before punch-through and was responsible for switching.

Most recently, Habib (1-8) has shown that the avalanche and punch-through modes are two subclasses of a more general switching mechanism, the Regenerative Feedback Mechanism (RFM). He identified the feedback loop in terms of the various current components in the system and eventually rigorously derived the I-V characteristics of the device. Both types of switching, avalanche and punch-through, depend on the RFM for switching. The key difference between the two modes of switching is the manner in which each is initiated.

In the avalanche device, avalanche multiplication of the electron tunnel current, J_{nt} (see Fig. 1.3), and/or the generation current, J_g, in the high field depletion region, x_d, increases the electron current passing across the p^+-n junction, J_{nj}. This injected electron current is given by

$$J_{nj} = M(J_{nt} + J_g),$$

where the multiplication factor $M = 1 - (\frac{V_a}{V_{bd}})^{-1}$, and

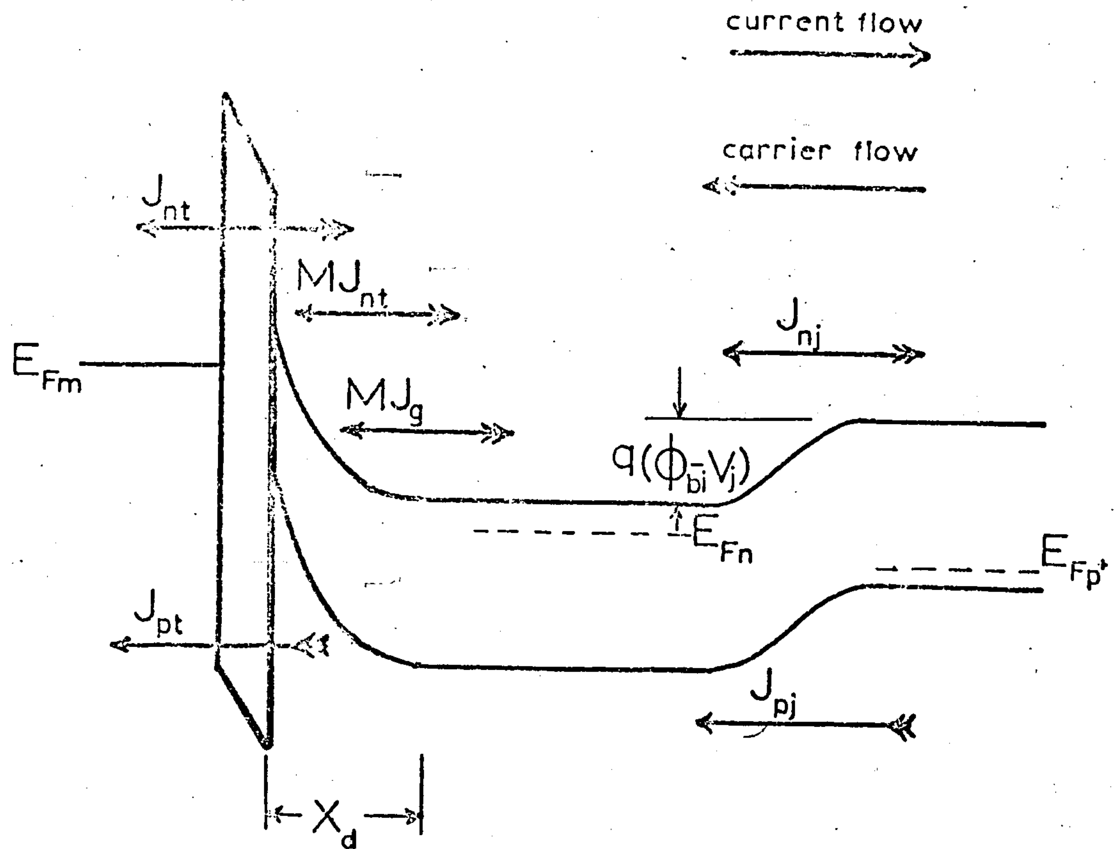

Fig. 1.3 The avalanche mode MISS just prior to switching.

V_a = voltage applied to the device,

V_{bd} = the avalanche breakdown voltage.

The electron current biases the p^+-n junction, and once the junction is sufficiently biased, the feedback mechanism is initiated. The mechanism is described in detail in Section 2.2.1. The voltage at which switching occurs in the avalanche device is dependent on the avalanche breakdown voltage of the epitaxial layer, given by (1-9)

$$V_{bd} = 60 \left(\frac{E_g}{1.1}\right)^{3/2} \left(\frac{N_d}{10^{16}}\right)^{-3/4} ,$$

where E_g is the bandgap energy and N_d is the epitaxial layer doping concentration.

In the PT device of El-Badry and Simmons (1-7) however, because of the relatively low doping of the epitaxial layer, the surface depletion region actually extends (i.e. punches through) to the p^+-n junction before the avalanche voltage, V_{bd}, can be attained. Any increase in the applied voltage will thereafter cause a decrease in the barrier potential of the p^+-n junction and the same feedback mechanism (of Section 2.2.1) as in the avalanche mode of switching is initiated.

Figure 1.4 illustrates the energy diagram for a punch-through device close to switching. The feedback loop is established when the p^+-n junction is biased sufficiently such that a critical value of hole current is injected from the p^+ substrate into the epitaxial

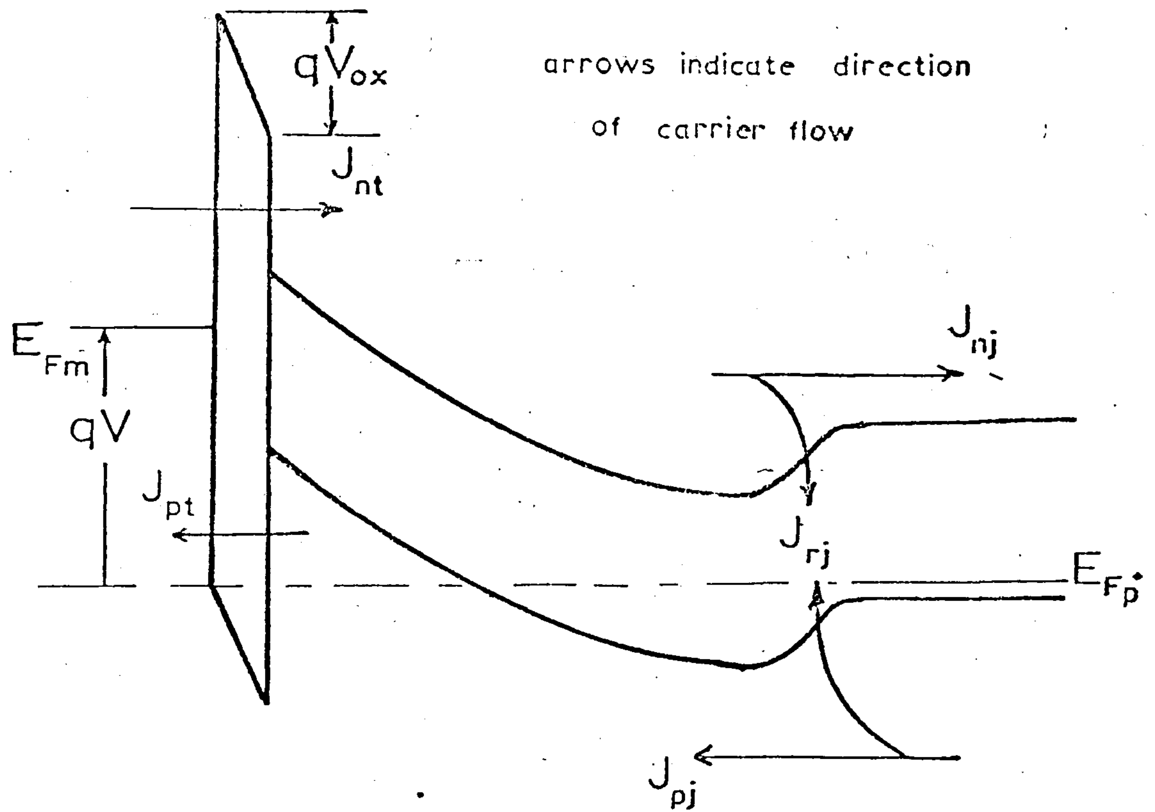

Fig. 1.4 The punch-through mode MISS close to the switching voltage.

layer. This augmented hole diffusion current, J_{pj}, will be accompanied by an incremental increase in the free hole density p(o) at the $Si-SiO_2$ interface, causing an increase in the oxide voltage, V_{ox}. This increase in V_{ox} will enhance the flow of electron tunnel current, J_{nt}, from the semiconductor conduction band to the metal. This in turn causes a further increase in the p^+-n junction bias, V_j, which is accompanied by a further increase in the hole current, J_{pj}, injected into the epitaxial layer. In this manner, a positive feedback loop is established. When the gain of the feedback loop is equal to unity, the device switches.

Two mechanisms, PT and RFM, are of special importance since the devices studied during the course of this work behaved as predicted by these two mechanisms. Hence these two mechanisms deserve more attention and will be treated in detail in the next chapter.

1.3 THE METAL INSULATOR SEMICONDUCTOR THYRISTOR

Any mechanism that will reinforce the feedback action will facilitate the device switching. Conversely, any mechanism that weakens the positive feedback action will tend to inhibit switching. Thus, electronic carrier injection (or extraction) or the appropriate p^+-n junction biasing will strengthen (or weaken) the feedback mechanism i.e. reduce (or increase) the voltage required to switch the device. Desired junction biasing can be achieved through a third terminal or gate which is in ohmic contact with the n layer via an n^+ diffusion (see Fig. 1.5). Since this device has

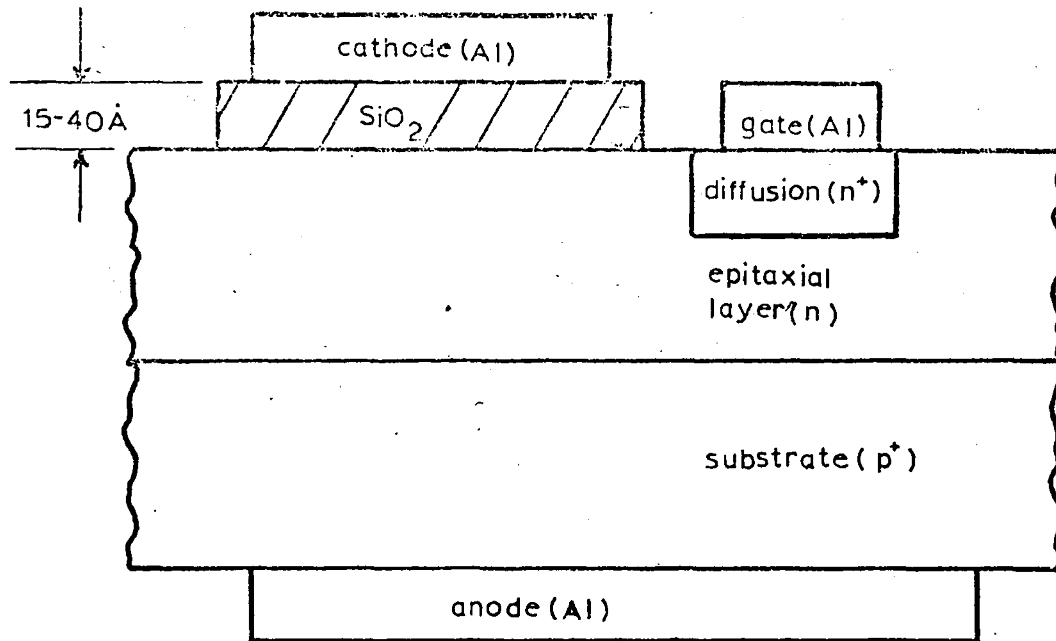

Fig. 1.5 The basic three terminal MIST structure.
(not drawn to scale)

characteristics resembling those of a thyristor, it is designated the Metal-Insulator-Semiconductor-Thyristor (MIST).

The MIST was first studied by Kroger and Wegener (1-4), who found that increasing the negative bias on the gate (or increasing the forward bias across the junction) decreased the switching voltage whereas decreasing the forward bias caused the switching voltage to increase. Yamamoto et al. (1-2) discovered that the switching voltage could be decreased with a proportionate increase in the gate terminal bias current. Chik and Simmons (1-10) carried out an extensive investigation of the dependence of the MIST I-V characteristics on gate bias (both current and voltage bias). Figure 1.6a shows the I-V characteristics of the MIST for various values of gate current, I_g. It is seen from the figure that the switching voltage, V_s, decreases monotonically with increasing I_g. The variation of V_s with I_g that they observed is presented in Figure 1.6b. Habib and Simmons (1-11) have carried out a detailed theoretical analysis of the MIST, and the calculated I-V curves they obtained with gate current as parameter are presented in Figure 1.6c. This study is of particular interest because variation of the junction isolation area (see Chapter 4) manifests itself in a change in junction bias, which is what one achieves via the gate terminal of the MIST.

1.4 THE OPTICAL MIST (OMIST)

Just as electronic minority carrier injection enhances the switching action, so does optically generated carrier injection.

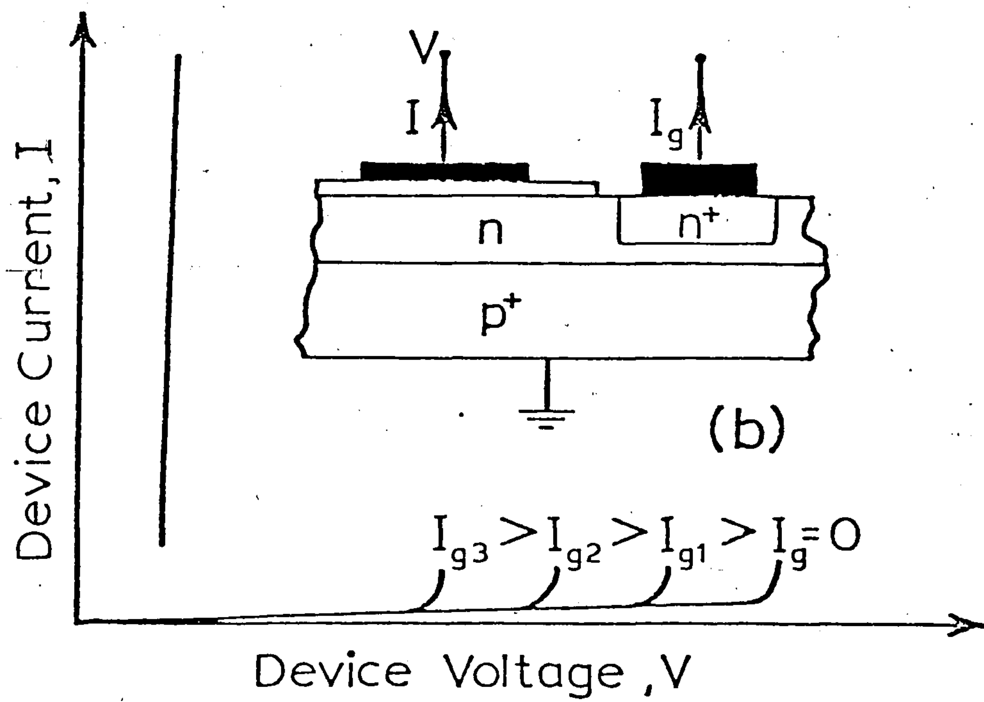

Fig. 1.6a MIST device I-V characteristics.

INSET: Basic structure.

(After Chik and Simmons [1-10]).

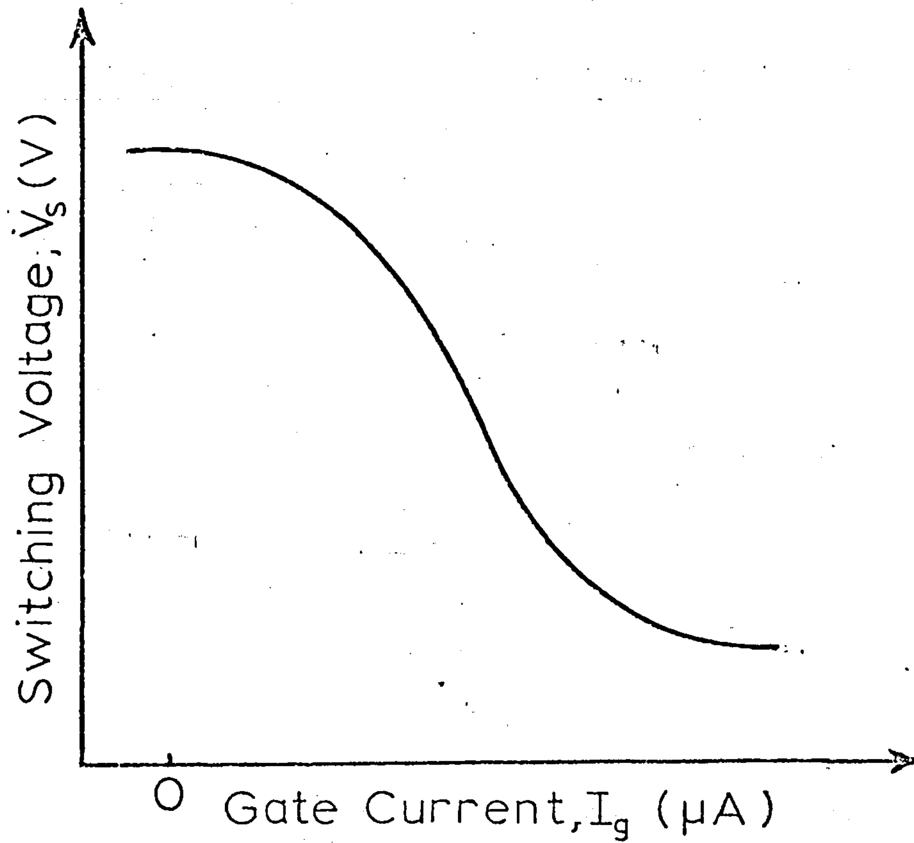

Fig. 1.6b Variation of switching voltage V_s as a function of injected gate current in the MIST device. (After Chik and Simmons [1-10]).

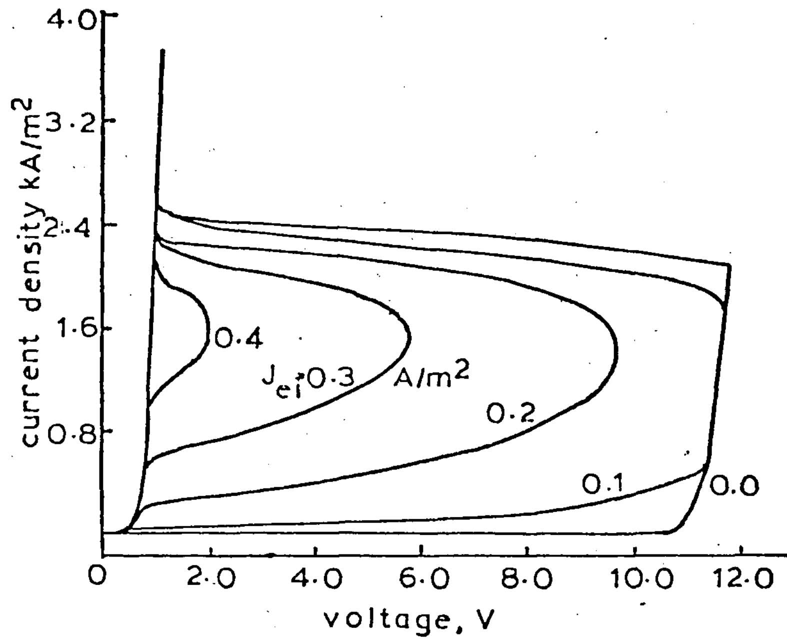

Fig. 1.6c Calculated I-V curves of the MIST with gate current J_{ei} as parameter.

(After Habib and Simmons [1-11]).

Nassibian, Calligaro and Simmons (1-12) developed theoretical expressions for the light induced hole current and correlated the experimentally observed change in the MIST switching voltage as a function of incident photon flux. They used a 150 Å thick, semi-transparent aluminium film as the cathode so that the incident light could penetrate through the metal and generate electron-hole pairs in the n epi-layer. The transmittance of the film was measured to be 0.15.

The main drawback in the structure was the poor transmittance of the Al film, which reduced the quantum efficiency of the device. Adan and Dobos (1-13) recently investigated the optical dependence of the MISS characteristics using a 1000-2000 Å thick RF sputtered film of SnO_2 as the cathode. The advantage of using SnO_2 over Al is that it is a highly conductive ($\rho \simeq 10^{-2}\,\Omega cm$) n-type semiconductor which is virtually transparent to visible light (transmittance ≃ 90%). 90%).

1.5 TWO DIMENSIONAL EFFECTS

All the theories presented to date to explain the observed I-V characteristics have been based on a one-dimensional analysis of the device. Other than the punch-through and avalanche models proposed by Habib and Simmons, there is a third model first proposed by Yamamoto et al. (1-2) and treated in greater detail by Sarrbayrouse et al. (1-14). In this model the switching is related to the formation of an inversion layer at the $Si-SiO_2$ interface. However erroneous interpretation of their experimental results led the authors

to conclusions different from those reached by Habib and Simmons. These anomalies have recently been explained by an investigation carried out by Duncan et al. (1-15).

In an extensive experimental study these authors have established that fabrication conditions, thickness of the field oxide employed and device geometry have a very strong effect on the switching charactersitics of the MISS. The experimental results obtained have been explained in a qualitative manner based on the strengthening and weakening of the regenerative feedback mechanism of Habib and Simmons (1-16).

1.6 THE OBJECTIVE AND OUTLINE OF THIS THESIS

The main objective of this thesis is to provide a two-dimensional model to explain the two-terminal DC characteristics of the MISS. To adequately model the device, it is essential to know as accurately as possible the area of the p^+-n junction active in the functioning of the device. To effectively control the junction area, the devices were isolated by means of self-terminating V-grooves. Another motivation for isolating the devices is the theoretical analysis of the MIST by Habib and Simmons (1-11). The variation of the MISS characteristics with gate bias (or junction bias) that they calculated is what is effectively simulated by changing the V-groove area.

An important outcome of the study of the variation of the I-V characteristics with changes in junction area was the experimental determination of the switching criterion of the MISS. The effect

of the tunnel oxide thickness, d_{ox} on the DC behaviour has also been investigated.

To make the presentation lucid, the thesis is organised in the following fashion:

Chapter 2 presents the punch-through and regenerative feedback theories which are essential to understand the DC behaviour of the devices under study. Observed perimeter-to-area ratio effects on the I-V characteristics of the MISS are presented and the trends explained on the basis of the RFM.

Chapter 3 presents the procedure employed to fabricate the devices and the experimental technique used to measure the DC I-V characteristics of the MISS.

Chapter 4 presents physical arguments to explain the observed two-terminal DC behaviour of the isolated MISS and establishes the switching criterion for the device.

Chapter 5 details the two-dimensional model used in predicting the variation of device parameters with changes in oxide thickness and junction area.

Chapter 6 presents the conclusions that may be drawn from the discussions in the preceding chapters and design criteria for the device are developed, based on these discussions.

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CHAPTER 2

In this chapter the DC theory essential to understanding the MISS is presented. The class of devices this theory models is those that do not depend on carrier multiplication in the surface depletion region to initiate the positive feedback mechanism (see section 1.2 for a simple treatment of avalanche devices). From now on we will refer to all such devices (i.e. other than avalanche devices) as punch-through devices. However, there are two sub-classes of the punch-through device:

(1) the "ideal" punch-through device in which the surface depletion region extends through the epilayer to the junction depletion region before the positive feedback mechanism is initiated, and

(ii) the "non-ideal" punch-through device in which the regenerative feedback is high enough to initiate switching before the surface depletion region punches through to the junction depletion edge.

Both these classes of devices will be dealt with separately and the arguments presented and used to explain, qualitatively, the area dependence of the MISS current-voltage characteristics.

2.1 THE IDEAL PUNCH-THROUGH MISS

2.1.1 High Impedance Characteristics

The switching mode of the metal-insulator-n-p^+ structure is with the metal biased negatively with respect to the p^+ substrate. This effectively reverse-biases the MIS diode into deep-depletion and forward-biases the p^+-n junction. As the bias on the metal electrode is increased negatively, the depletion region under the oxide grows toward the p^+-n junction. Electron-hole pairs are generated in the depletion region, the electrons being swept towards the p^+-n junction and holes towards the $Si\text{-}SiO_2$ interface. The electron-hole pair generation current I_g is depicted in Figure 2.1a. It is worthwhile to note that if the oxide were impervious to holes (i.e. a thick-oxide (∿1000 Å) MOS capacitor), the generated holes would accumulate at the $Si\text{-}SiO_2$ interface, causing the n-Si to invert This would limit the depletion width, X_d, to a maximum corresponding to a surface potential $\psi_s = 2\phi_n$. However, as the insulator is leaky, holes pass through the oxide at the rate that they are supplied to the interface; hence, the n-Si goes into deep-depletion (Fig. 2.1a).

For the typical values of generation lifetime encountered in bulk epitaxial silicon (∿10^{-6} Sec), the generation current is negligible compared to the magnitude of the OFF state current normally observed. The primary electron current flowing in the system is the electron tunnel current, I_{nt}, composed of electrons flowing from the metal to the conduction band of the n-Si. This current dominates I_g and will be shown in Section 2.2.1 to be the

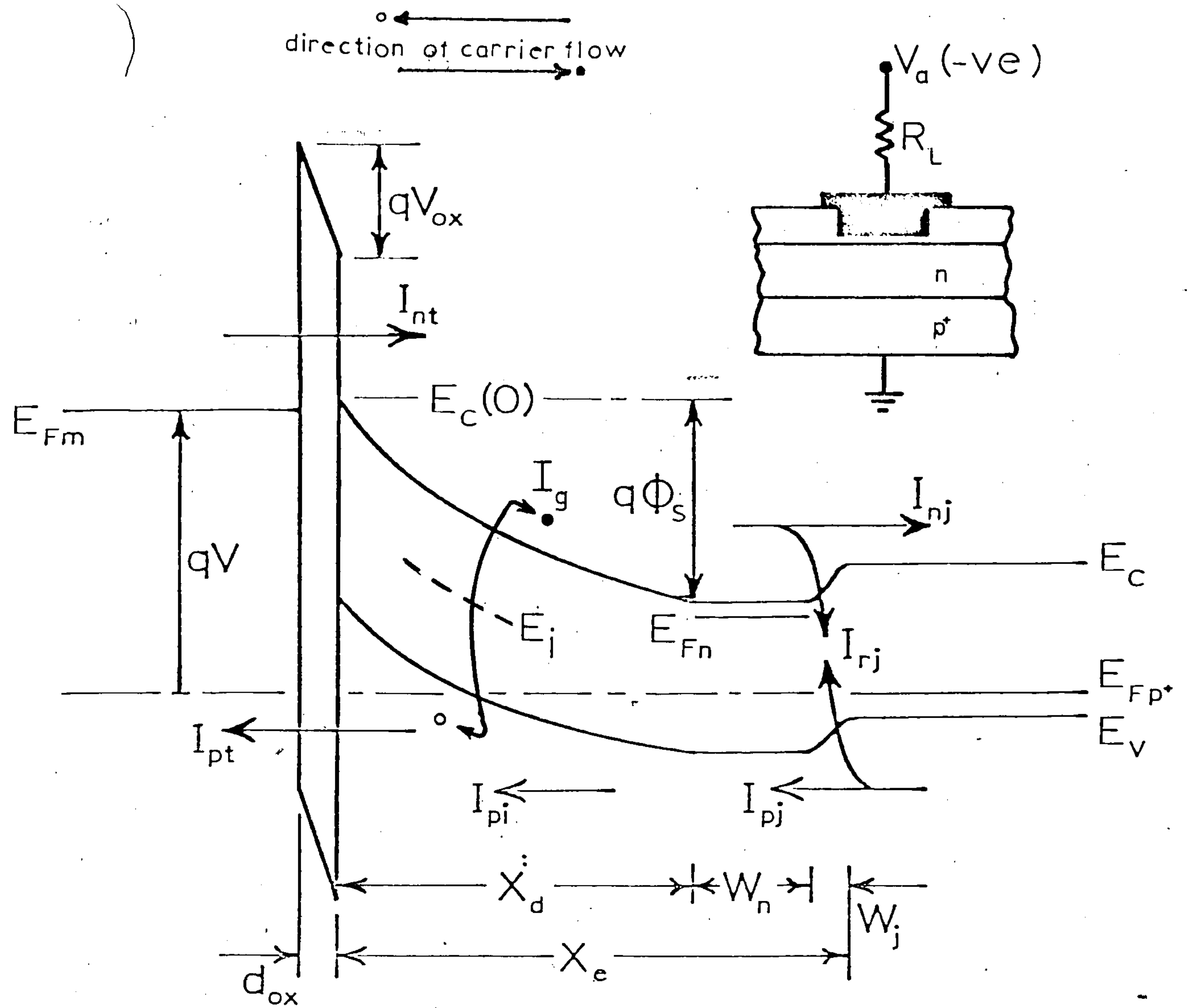

Fig. 2.1a The MISS in the OFF state with component currents.
INSET: Basic circuit configuration for the MISS.

triggering current component which initiates the RFM leading to switching.

However, the "ideal" punch-through device, by definition, is one in which the surface depletion region necessarily has to punch-through before the switching process is initiated and so more insight into device operation is gained through the voltage rather than the current equations.

The voltage, V, across the device is given by

$$V = \phi_{MS} + V_{ox} + \psi_s + V_j \tag{2.1}$$

The MISS is normally in the configuration shown in the inset of Figure 2.1a, where R_L is the load resistor used to limit the current through the device.

The applied voltage, V_A, is given by

$$V_A = V + V_R \tag{2.2}$$

where V_R is the voltage across R_L.

In the OFF state, the current through the device is limited by the reverse biased MIS diode. The device exhibits a very high dynamic impedance in the OFF state ($\sim 10^7 \Omega$); hence the increase in V_{ox} and V_j needed to accommodate the small increase in current is negligible compared to the gate voltage, V. These arguments apply only after flat-band (see Chapter 4 for details), when any increase in the gate voltage, V, is absorbed in the surface depletion region. Hence, eqn. 2.1 may be rewritten as

$$V \simeq K + \psi_s \qquad (2.3)$$

where K is a constant, of the order of 1-2V, which incorporates the effects of ϕ_{MS}, V_{ox} and V_j (see Chapter 4). The surface potential, ψ_s, is related to the depletion width, X_d, given by (2-1)

$$X_d = \left(\frac{2\varepsilon_s \psi_s}{qN_d}\right)^{\frac{1}{2}} \qquad (2.4)$$

Hence V can increase to a maximum value corresponding to the case when the depletion region extends up to the depletion edge of the p^+-n junction, or equivalently,

$$X_{d_{max}} = X_{epi} - W_j \qquad (2.5)$$

where X_{epi} is the epilayer thickness and W_j is the junction depletion width.

Using eqns. 2.3 and 2.4 the following relation for the maximum voltage V_{PT} than can be sustained across the MISS can be derived as,

$$V_{PT} = K + \psi_{s_{max}}$$

$$= K - \frac{qN_d(X_{epi} - W_j)^2}{2\varepsilon_s} \qquad (2.6)$$

Any extra voltage, ΔV, above V_{PT}, applied to the gate will cause a Schottky lowering of the p^+-n junction barrier potential, V_{bi} (2-2), and an attendant increase in current. This sudden increase in the current across the device is what triggers the switching mechanism, leading to the observed negative resistance in the MISS I-V charac-

teristic. The physical processes responsible for the negative resistance behaviour are explained in the following section.

2.1.2 The Negative Resistance Region

As stated in the previous section, at sufficiently high bias ($V=V_{PT}$), the depleted section of the epilayer reaches through to the p^+-n junction. Any further increase in the gate voltage will appear across R_L, the p^+-n junction and V_{ox}.

Consider a small incremental voltage increase, ΔV, beyond V_s. Assume also that all the voltage increase appears across R_L. Hence, the current flowing through the MISS is given by

$$I \approx \frac{V - V_{max}}{R_L} \tag{2.7}$$

In the OFF state, the current I_{off}, was typically around 10^{-6}-10^{-7} A (depending on device area). Now, however, for $V - V_{max} = 0.1V$ and $R_L = 1K\Omega$,

$$I = \frac{0.1}{10^3} = 10^{-4} A$$

which is very much greater than I_{off}. This current flows into the device, across the oxide and p^+-n junction. However, the voltage drop across the resistor is a linear function of I, whereas the voltage drop across both the oxide and the p^+-n junction depend logarithmically on I. Hence the initial assumption of most of the voltage increase being absorbed across R_L after punch-through is

justified. The above empirical argument further strengthens the statement that V_{PT} as defined by eqn. 2.6 is truly the maximum voltage that can be sustained across the device.

After punch-through, any incremental voltage ΔV causes a Schottky lowering of V_{bi} causing a sudden increase in the injected hole current I_{pj} from the p^+ substrate towards the $Si-SiO_2$ interface (see Figure 2.1b). Just prior to punch-through the voltage across the tunnel-oxide was just enough to supply the small OFF state current. Hence the sudden increase in the rate of holes reaching the interface (or equivalently, the sudden rise in I_{pj}) cannot be accommodated by the oxide, i.e. the holes reach the $Si-SiO_2$ interface faster than the existing oxide voltage can drain them. This causes an increase in the hole concentration at the interface p(o), and an attendant increase in V_{ox}. This in turn increases the electron tunnel current, which further biases the p^+-n junction, causing a larger I_{pj} to flow. The build-up of holes causes a redistribution of voltage across the device. The depletion region starts collapsing, the decrease in surface potential being taken up by the oxide, the p^+-n junction and R_L. However, because of the exponential dependence of current on V_{ox} and V_j, very small changes in V_{ox} and V_j can accommodate large changes in current. Hence, most of the voltage drop across the device caused by the shrinking depletion region is absorbed in the series resistance. This voltage <u>decrease</u> across the device accompanied by an <u>increase</u> in current leads to the negative resis-

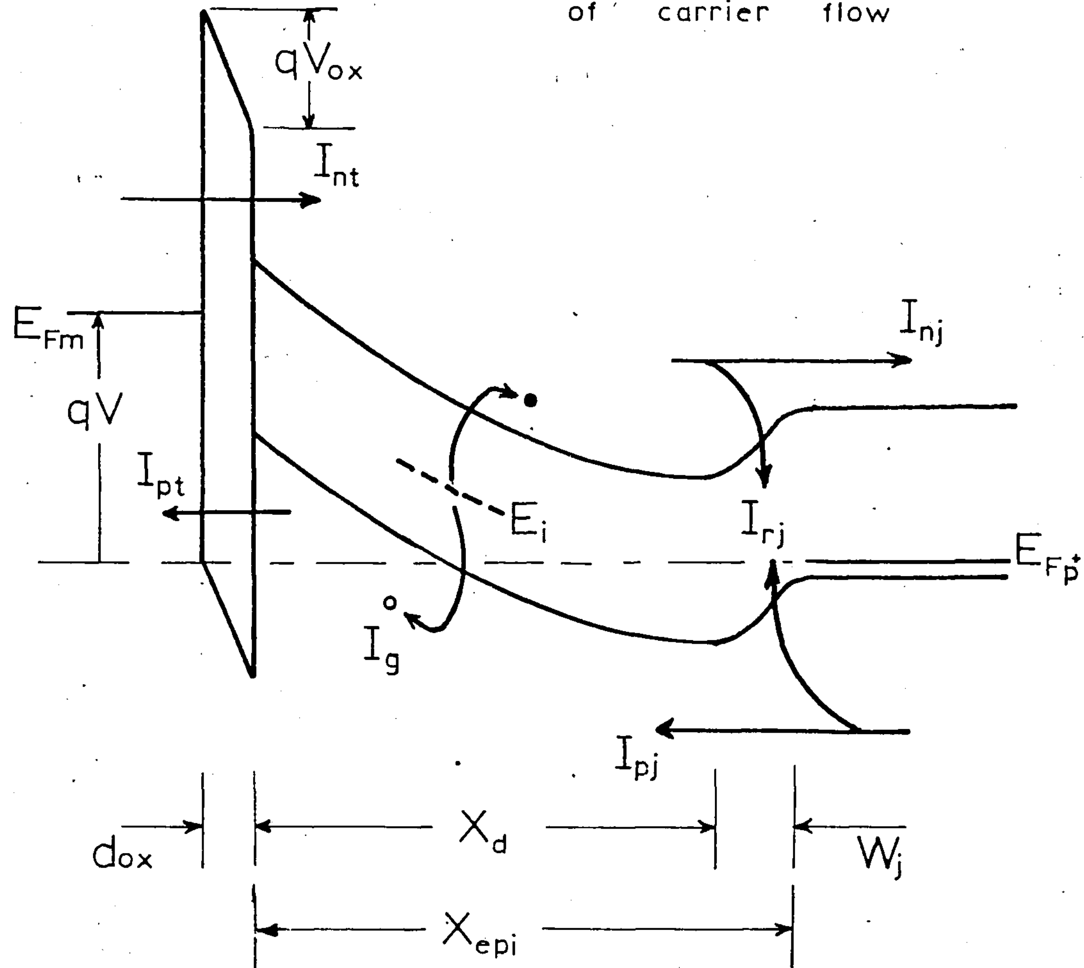

Fig. 2.1b The MISS at punch-through with component voltages and currents.

tance characteristic observed and the device switches. The voltage at which switching occurs is hence the PT voltage,

$$V_s \equiv V_{PT} \simeq K - \frac{qN_d(X_{epi} - W_j)^2}{2\varepsilon_s} \quad (2.6a)$$

2.1.3 Low Impedance ON State

During switching, the depletion region keeps collapsing and ψ_s continuously decreases. This contraction stops when ψ_s reaches the equilibrium strong inversion value (2-3),

$$\psi_s \simeq 2\phi_n = 2\{\frac{E_G}{2} - (E_c - E_{Fn})\} \quad (2.8)$$

Figure 2.1c shows the energy band diagram of the MISS in the ON state i.e. with $\psi_s \simeq 2\phi_n$. During switching, the current was limited by the rate at which holes could be transported through the oxide. In the ON state however, the field across the oxide is large ($>10^6 Vcm^{-1}$) and the oxide can be considered essentially transparent to electrons and holes. Hence in this regime of operation the current through the device is limited by the p^+-n junction and R_L.

The holding voltage, V_H, which is the minimum voltage required to keep the device in the ON state, is given by

$$V_H = \phi_{MS} + V_{ox} + 2\phi_n + V_j \quad (2.9)$$

In the low-impedance state, the p^+-n junction is fully turned on, i.e. $V_j \simeq 0.5V$ (see Chapter 5). Also $q\psi_s = 2\phi_n \simeq 0.47$ eV for a doping concentration $N_d = 10^{14} cm^{-3}$. Assuming that the tunnel-oxide thickness, d_{ox}, is 30 Å and the oxide field, ε_{ox}, is $10^6 Vcm^{-1}$, then the oxide voltage, V_{ox}, is given by

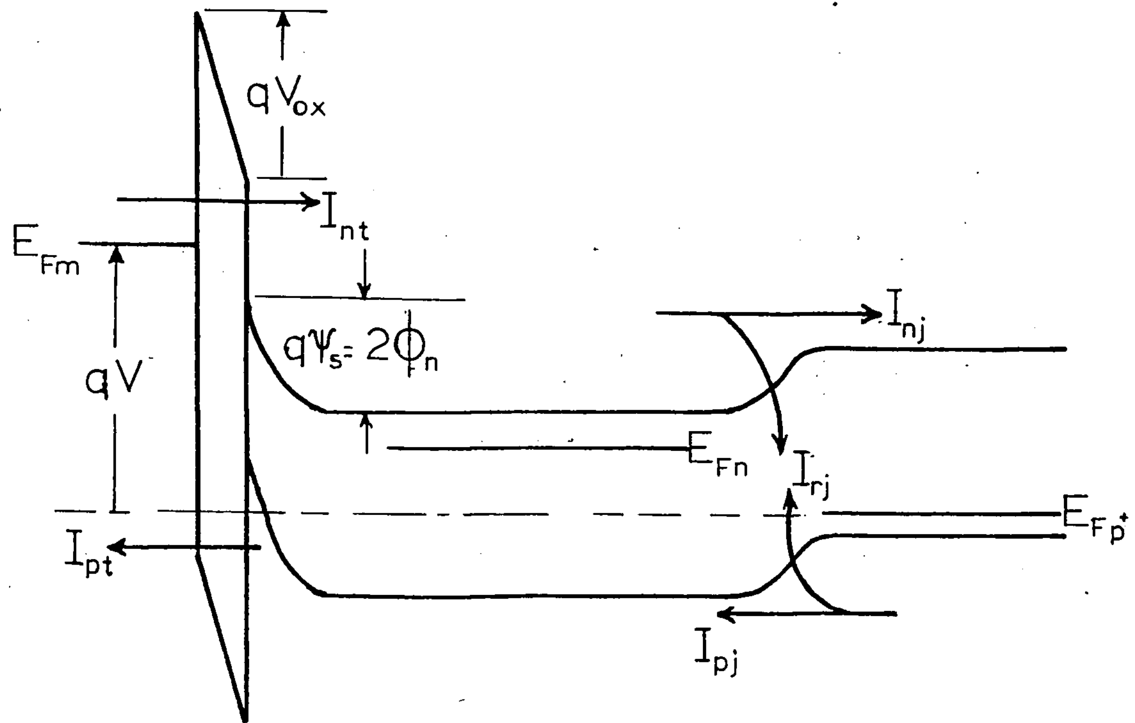

Fig. 2.1c The MISS at the holding point with component currents and voltages.

$$V_{ox} = \varepsilon_{ox} . d_{ox} = 30 \times 10^{-8} \times 10^{6} = 0.3V$$

Hence V_H is of the order of

$$V_H \simeq 0.3 + 0.5 + 0.47 + 0.34 \simeq 1.8V$$

It is also important to note that in the ON state, the I-V characteristic is determined by the p^+-n junction. In other words, it is almost identical to the familiar forward bias characteristic of a p^+-n junction with a voltage displacement due to ψ_s and V_{ox}.

2.1.4 The Switch-Off Möde

When the voltage across the device in the ON state is reduced, the current flowing through the device decreases. The decrease in the device current necessarily implies a decrease in the injected hole current, I_{pj}, from the p^+ substrate to the $Si\text{-}SiO_2$ interface. When the rate of hole supply to the silicon surface drops below a critical value, i.e. $I<I_H$, then the existing voltage across the tunnel oxide drains the holes from the $Si\text{-}SiO_2$ interface faster than they are supplied by the p^+-n junction. The reduction of hole charge at the interface reduces the oxide voltage, which in turn reduces the electron tunnel current, I_{nt}. The reduction in I_{nt} lowers the bias across the p^+-n junction which causes a decrease in I_{pj}. This negative feedback mechanism drains all the inversion charge from the $Si\text{-}SiO_2$ interface, causing the depletion region to expand and the device reverts to the OFF state. Alternatively, the voltage drop

across R_L, V_j and V_{ox} decrease now appearing across ψ_s. Furthermore, the current is again limited by the reverse-biased MIS diode and not the p^+-n junction or the load resistor.

El-Badry and Simmons (2-4) have shown that there is excellent correspondence between the predictions of the "ideal" PT theory and the observed behaviour of MISS devices fabricated on n epilayers of relatively low doping ($\sim 10^{14}$-10^{15} cm^{-3}).

2.2 THE "NON-IDEAL" PUNCH-THROUGH MODE

As stated earlier the class of devices that switch before the surface depletion region actually extends up to the p^+-n depletion edge, are said to be operating in the "non-ideal" punch-through mode, i.e. $V_s < V_{PT}$.

2.2.1 The Regenerative Feedback Mechanism (RFM)

Consider a MISS biased in the same manner as shown in the inset of Figure 2.1a, i.e. the metal biased negatively with respect to the p^+ substrate, effectively reverse biasing the MIS diode and forward biasing the p^+-n junction. The feedback loop inherent in the system is established as follows: Let the voltage drop across the p^+-n junction, V_j, be incremented by a small amount. Extra holes are thus injected from the p^+ region to the Si-SiO_2 interface. If the hole current is tunnel-limited, a build-up of the inversion charge takes place with a concomitant increase in the voltage drop across the insulator, V_{ox}, and, hence, in the electron-tunnel current,

I_{nt}. The augmented I_{nt} flows across the p^+-n junction turning it still further on. The feedback loop is thus a regenerative one. Whether the process carries on until the device switches from the OFF to the ON state, or a steady state is reached in the OFF state itself is dependent on the strength of the RFM. In particular, Habib and Simmons (2-4) have identified the criterion for switching to be when the open loop gain (G) of the device equals unity where G is defined as follows,

$$G = \frac{\Delta I_{nt}}{\Delta I_{rj}}$$

$$= 1 \text{ at switching.}$$

where ΔI_{nt} = incremental change in electron tunnel current, and

ΔI_{rj} = resultant change in junction recombination current.

The negative resistance region as explained by the RFM is the subject of discussion in the next section.

2.2.2 The Negative Resistance Region

Consider the feedback loop $\Delta I_{nt_1} \rightarrow \Delta I_{rj} \rightarrow \Delta V_j \rightarrow \Delta I_{pj}$ $(\simeq \Delta I_{pt}) \rightarrow \Delta p(o) \rightarrow \Delta V_{ox} \rightarrow \Delta I_{nt_2}$, where ΔI_{nt_1} is the initial increment in I_{nt} and ΔI_{nt_2} is the increase in I_{nt} subsequently caused by the increase in the oxide voltage. If ΔI_{nt_2} is less than ΔI_{nt_1}, then the system tends to achieve a steady state in the OFF state itself, with the increments in I_{nt} caused by the regenerative feedback loop swiftly decaying to zero. However, if the increase in electron tunnel current,

ΔI_{nt_2}, caused by the RFM is larger than the initial increment ΔI_{nt_1} then a "run-away" increase in current fuelled by the RFM occurs, increasing the voltage drops across R_L (V_R), the tunnel-oxide (V_{ox}) and the p^+-n junction (V_j). Since this voltage redistribution occurs at a fixed applied voltage (V_A), the voltage across the device, V, has to decrease to satisfy the voltage relationship across the device. This decrease in V accompanied by an increase in current gives rise to the negative resistance behaviour observed. The decrease in the voltage, V, across the device is manifested in a decrease in the surface potential, ψ_s, the electrons necessary to fill the donor states being supplied by I_{nt}.

Summarising, switching occurs when ΔI_{nt_2} is greater than ΔI_{nt_1}. Neglecting recombination in the neutral epilayer one can write the following series of equations to derive the open loop gain of the system

$$\Delta I_{nt_1} = \Delta I_{rj}$$

$$\Delta I_{pt} = \Delta I_{pj}$$

$$\frac{\Delta I_{nt_2}}{\Delta I_{pt}} = G_{ox}, \text{ the gain of the oxide}$$

$$\frac{\Delta I_{pj}}{\Delta I_{rj}} = G_j, \text{ the gain of the junction}$$

$$G \equiv \frac{\Delta I_{nt_2}}{\Delta I_{nt_1}} = \frac{\Delta I_{nt_2}}{\Delta I_{rj}}$$

$$= 1 \text{ at switching.}$$

The switch-off mode is identical to the mechanism explained in Section 2.1.4.

2.3 TWO-DIMENSIONAL EFFECTS

The punch-through theory and the more rigorous regenerative feedback theory of Habib and Simmons (2-4) adequately explain the observed I-V characteristics of large area MISS devices (>100 x 100μm^2). However, as the tunnel-oxide areas get progressively smaller the MISS characteristics cannot be explained by either of the above models. The primary reason for the strong area dependence of the MISS characteristics is that as the device dimensions become comparable to the epilayer thickness current fringing plays a dominant role in determining device behaviour. Neither of the above-mentioned models take such two-dimensional effects into account and thus cannot account for the strong area dependence of the MISS I-V characteristics.

The following section will deal exclusively with explaining the variation of device characteristics with area.

2.3.1 The Effect of Device Area

To study the two-dimensional nature of the MISS, devices were fabricated on materials with the following specifications:

Material:	n epitaxial on p^+ substrate	
Crystal Orientation:	<100>	
Epilayer resistivity:	10.8 Ωcm	(N_d = 4.2×10^{14} cm^{-3})
Substrate resistivity:	$\sim$0.005 Ωcm	($N_a \cong 10^{19}$ cm^{-3})

The field oxide employed was a ~5000 Å SiO_2 film, thermally grown in wet oxygen at 1100°C. The tunnel-oxide was grown at 700°C in dry oxygen for 6 minutes. The tunnel oxide areas were 160 x 160μm², 100 x 100 μm², 80 x 80 μm², 40 x 40 μm² and 20 x 20 μm². Aluminium was the metal used for both the gate electrode and the back contact. Details of the fabrication techniques employed are presented in Chapter 3.3.

The DC characteristics of the devices differed substantially from one device area to the next. Whereas the largest area device A1, (160 x 160μm²) switched at the low voltage of 3.5V (see Figure 2.2), the smallest area device, A5 (20 x 20μm²) did not show any switching behaviour at all (Figure 2.2). It is also apparent from Figures 2.2 that the switching voltage of the devices monotonically increased as the tunnel oxide area decreased. This, we postulate, is due to the increased current fringing which occurs in smaller dimension devices.

In Figure 2.3 a small tunnel oxide area device is shown schematically just prior to switching. The fringing effects are included as current lines intercepting an effective p^+-n junction area A_j. This effective junction area is larger than the tunnel oxide area, A_{ox}, by the additional fringing area, A_f. Or, equivalently,

$$A_j = A_{ox} + A_f \qquad (2.10)$$

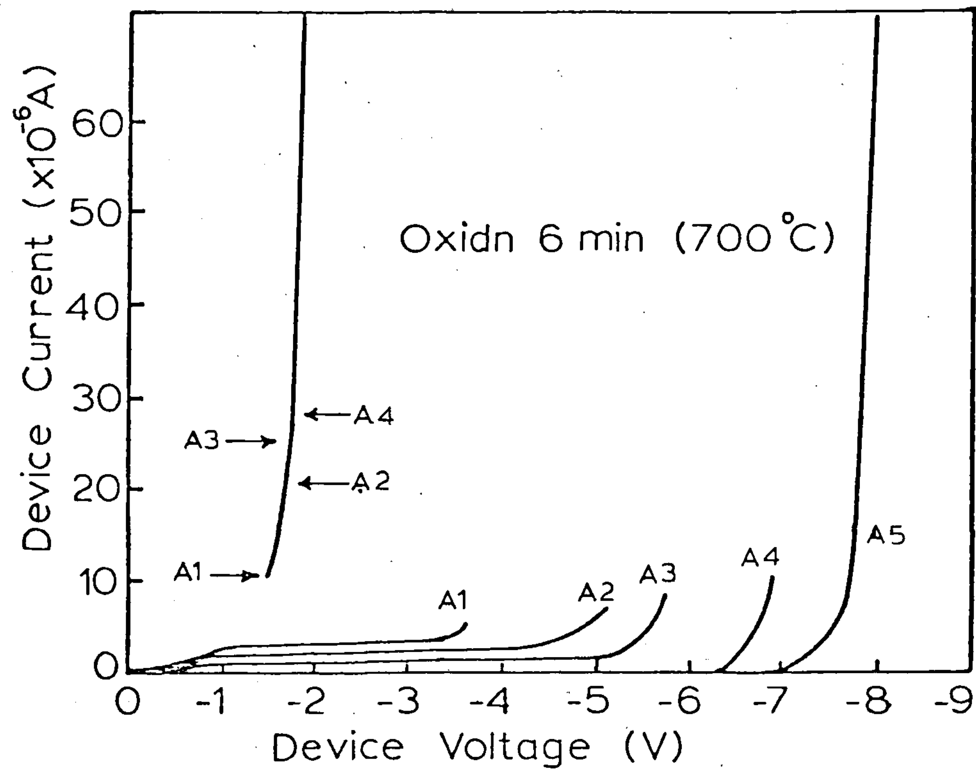

Fig. 2.2 I-V characteristics of the MISS illustrating the effect of device area on device behaviour. The tunnel-oxide areas are

A1	160 x 160 μm^2
A2	100 x 100 μm^2
A3	80 x 80 μm^2
A4	40 x 40 μm^2
A5	20 x 20 μm^2

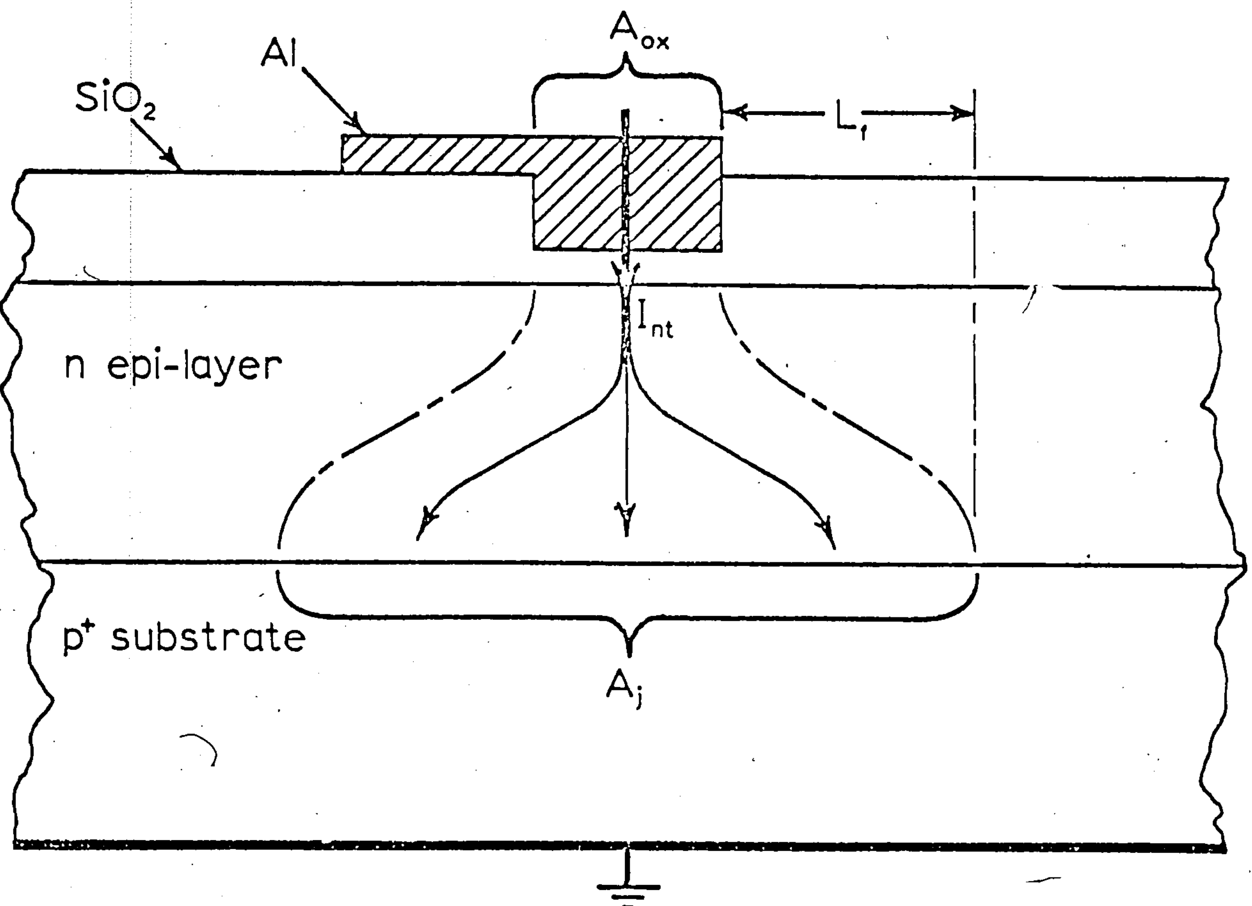

Fig. 2.3 Schematic diagram of small-area MISS, illustrating the effect of current fringing.

It is important to note that the extent of fringing is dependent mainly on the doping concentration, N_d, in the epilayer and the diffusion coefficient, D_n, of electrons, which are both constant for all the devices. Hence the fringing length is essentially constant from one device to the next.

The electron tunnel current, I_{nt}, is dependent on the tunnel oxide area, A_{ox}. Hence as the device area decreases, the tunnel current I_{nt} also decreases. Neglecting recombination in the neutral epilayer and the electron diffusion current across the junction (see Chapter 4 for details), I_{nt} is essentially absorbed in the p^+-n junction as a recombination current. Equivalently,

$$I_{nt} \simeq I_{rj} \tag{2.11}$$

Hence the reduction in I_{nt} is equivalent to a decrease in I_{rj}. Furthermore, I_{rj} is related to the bias, V_j, across the junction by (2-1)

$$I_{rj} = \frac{qA_j n_i W_j}{2\tau_1} \exp\left(\frac{qV_j}{2kT}\right)$$

where $A_j = A_{ox} + A_f$

W_j = the p^+-n junction depletion width

and τ_1 = the recombination lifetime in the p^+-n junction.

For small area devices ($A_{ox} << A_f$), A_j remains essentially unchanged from one device to the next. Hence the decrease in I_{rj} cannot be accounted for by the insignificant change in A_j. It

therefore has to manifest itself in a reduced bias across the junction. This decreased bias will weaken the RFM. Since the RFM is weakened, the gate has to be biased more strongly negative for the open loop gain to become unity, i.e. for the device to switch. In other words, the smaller the device area, the weaker is the RFM and hence higher the switching voltage, V_S, to a maximum of $V_S \approx V_{PT}$.

However, if the devices are sufficiently small, the RFM will be weakened to the point when the gain of the feedback loop can never reach unity which is necessary for switching (see section 2.2.2). Hence even after punch-through the MISS will remain in a deeply depleted state with the increase in current being mainly due to recombination, preventing the gain from ever reaching unity and thus not allowing the device to switch (device A4, Figure 2.2).

The above arguments adequately explain the area dependence of the device switching characteristics which are presented in Figures 2.2.

2.3.2 Perimeter to Area Ratio (PAR) Effects

Even though not explicitly stated, intrinsic in the arguments presented in the previous section is the fact that as the area of the devices decreased, the PAR of the devices increased, as is apparent from the following relation,

$$PAR = \frac{4(A_{ox})^{\frac{1}{2}}}{A_{ox}} = \frac{4}{(A_{ox})^{\frac{1}{2}}}$$

Hence the switching voltage, V_s, of a device with a particular tunnel-oxide thickness, d_{ox}, increases as the PAR increases.

To identify that this indeed was the case, a set of devices (B1-B5) was fabricated on the same material as devices A in the same run, with the same tunnel oxide thickness. The area of these devices was kept constant ($160 \times 160 \mu m^2$) but the PAR was varied as listed below

Device No.	Device Dimensions (μm^2)	PAR (μm^{-1})
B1	160 x 160	0.025
B2	320 x 80	0.032
B3	510 x 50	0.044
B4	850 x 30	0.069
B5	1280 x 20	0.102

The I-V characteristics of these devices are presented in Figure 2.4. It can be seen that for devices with constant area and identical tunnel oxide thickness, the switching voltage does indeed increase with increasing PAR (indicative of a weakening RFM) until device B5 which does not exhibit any switching behaviour. This trend is what was predicted from the preceding arguments and demonstrates the need for a comprehensive two-dimensional model to adequately predict the behaviour of small area devices.

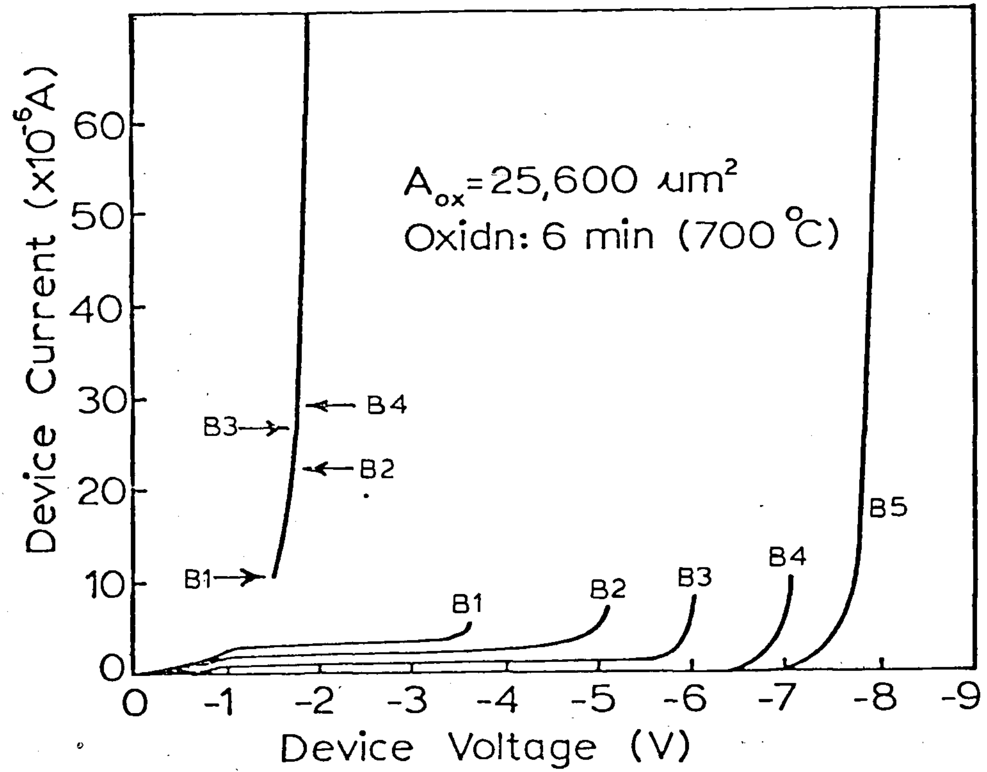

Fig. 2.4 I-V characteristics illustrating the effects of increasing tunnel-oxide perimeter for the 25,600 μm^2 area device: (B1) 640 μm, (B2) 800 μm, (B3) 1120 μm, (B4) 1760 μm and (B5) 2600 μm.

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CHAPTER 3

EXPERIMENTAL TECHNIQUES

In this chapter the processes used to fabricate the MISS devices characterised during the course of this work are described in detail. The device structure fabricated is shown in cross-section in Figure 3.1a and the plan view in Figure 3.1b.

The devices were fabricated on two batches of silicon epitaxial wafers with the following specifications:

(i) n-epitaxial material of starting thickness 7.4μm and resistivity 10.8Ωcm grown on a p^+<100> substrate of resistivity 0.005-0.01Ωcm (Batch 'X').

(ii) n-epitaxial material of starting thickness 9.7μm and resistivity 18.0Ωcm grown on a p^+<100> substrate of resistivity 0.06-0.12Ωcm (Batch 'L').

Besides fabrication, also described in this chapter is the experimental set-up used to make the DC current-voltage measurements of the MISS.

3.1 FABRICATION PROCEDURE

3.1.1 Masking Oxide Growth

The wafers were given a standard RCA pre-furnace clean (3-1). The details of this process are listed in Appendix A. The masking

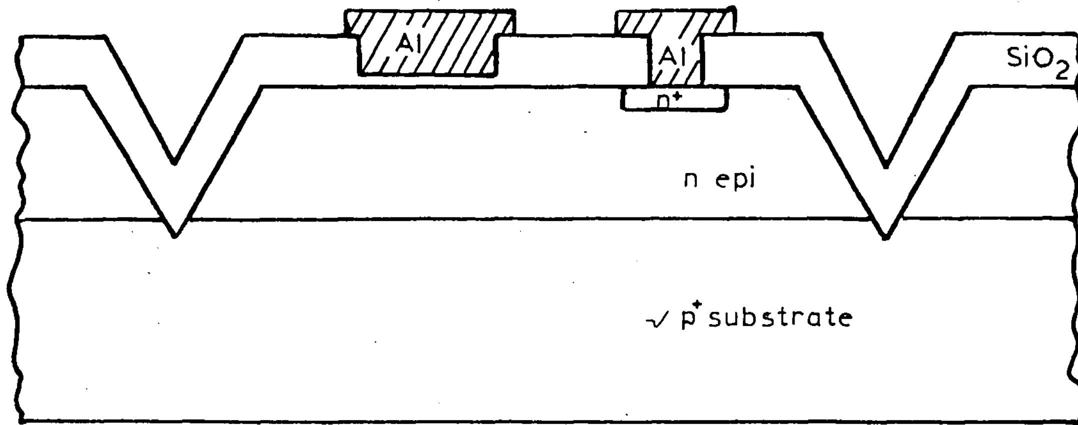

Fig. 3.1a Cross-sectional view of the isolated MISS structure.

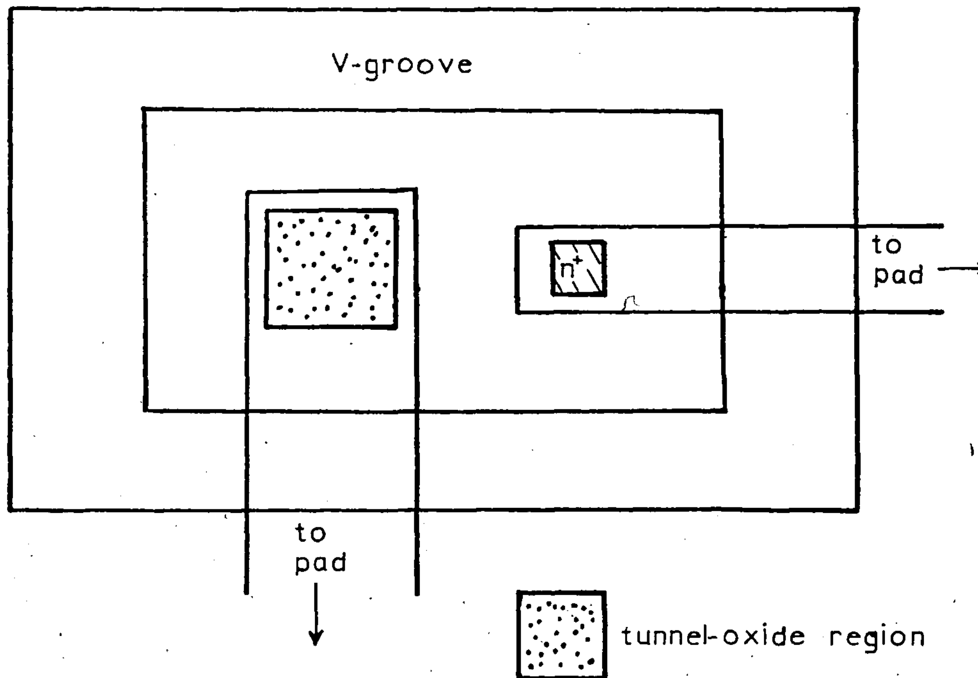

Fig. 3.1b Plan view of the isolated MISS structure.

oxides were thermally grown in a resistance-heated single-walled quartz tube in an ambient of wet oxygen under the following conditions:

Furnace temperature:	$1100^{o}C$
Water temperature (bubbler):	$95^{o}C$
Oxygen flow rate:	1 ℓ/min
Oxidation time:	10 mins.

These conditions provided an oxide thickness of approximately 2500 Å, which was sufficient to mask against any phosphorous diffusion during deposition and drive-in (3-2).

3.1.2 Phosphorous Deposition

The regions for phosphorous deposition were defined using the photolithographic techniques listed in Appendix B. The oxide was etched from these regions in a solution of buffered HF, comprising a mixture of HF reagent (49%) and NH_4F reagent (40%), supplied by Ashland Chemicals. The photoresist was removed by boiling in acetone.

The wafers were then cleaned by process A. Next, phosphorous pre-deposition was carried out under the following furnace conditions:

Furnace temperature:	$950^{o}C$
Furnace ambient:	N_2
N_2 flow rate:	1 ℓ/min.
Phosphorous source:	Grade PH-1000 Planar Diffusion Source (Carborundum)
Deposition time:	20 mins.

Four-point-probe measurements made on a test wafer diffused at the same time gave a sheet resistivity value of approximately 20Ω/□ . This agreed very well with the data sheets supplied by the Carborundum Company. Immediately after the deposition, the drive-in was done at 1100°C in O_2 (flow rate 1 ℓ/min) for 10 mins. All the oxide was then stripped off in a 30% HF solution.

3.1.3 V-Groove Etching

After etching the masking oxide, the wafers were rinsed in DI water and a masking oxide for the V-groove etching was grown under the same conditions as described in Section 3.1.1. The V-groove areas were defined photolithographically (Appendix B) and the oxide was etched from these regions in buffered HF.

Four V-groove geometries were used: $0.64 \times 10^{-4} cm^2$ ($80 \times 80 \mu m^2$), $10^{-4} cm^2$ ($100 \times 100 \mu m^2$), $1.96 \times 10^{-4} cm^2$ ($140 \times 140 \mu m^2$) and $4.8 \times 10^{-4} cm^2$ ($220 \times 220 \mu m^2$), designated as devices A, B, C and D respectively. A control epitaxial device was also prepared on the same slice (which was not isolated), labelled the N device.

The V-grooves were fabricated using an anisotropic etching solution composed of 40 gms. of KOH, 60 ml of DI H_2O and 100 ml of propanol. The temperature of the etch was maintained at 65^oC. Etching occurs along the <100> planes of silicon, resulting in the formation of an effectively self-terminating V-groove with the sides oriented at an angle of 54.7^o with the surface. Since amorphous SiO_2 is etched by the solution at a much lower rate than

<100> silicon, a relatively thin (500-1000 Å) layer of oxide can act as a mask for the etching procedure. The direction of the V-groove must be aligned parallel or perpendicular to the <110> direction, on the surface of the slice. The depth to which the groove extends is determined by the width of the oxide window. The depth, d, is approximately 0.71 times the width, w, of the silicon surface exposed to the etchant, i.e.

$$d = (\frac{w}{2}) \tan 54.7^{o}$$

A schematic of a V-groove in cross-section, defining the parameters d and w is shown in Figure 3.2.

After the V-grooves were etched, the masking oxide was removed in a solution of 30% HF.

Note: The V-groove etch also etches ∿7μ from the back of the silicon wafer, effectively removing the junction formed by phosphorous diffusing into the back. Hence the need for a separate process to remove the junction is eliminated.

3.1.4 Pattern Definition for Tunnel-Oxide Areas

Following the etching of the masking oxide, the wafers were given a pre-furnace clean (Appendix A). A field oxide of thickness ∿5000 Å was then thermally grown on the wafers under the same furnace conditions as detailed in Section 3.1.1 except for an increase in the oxidation time to 40 mins. It is essential that the field

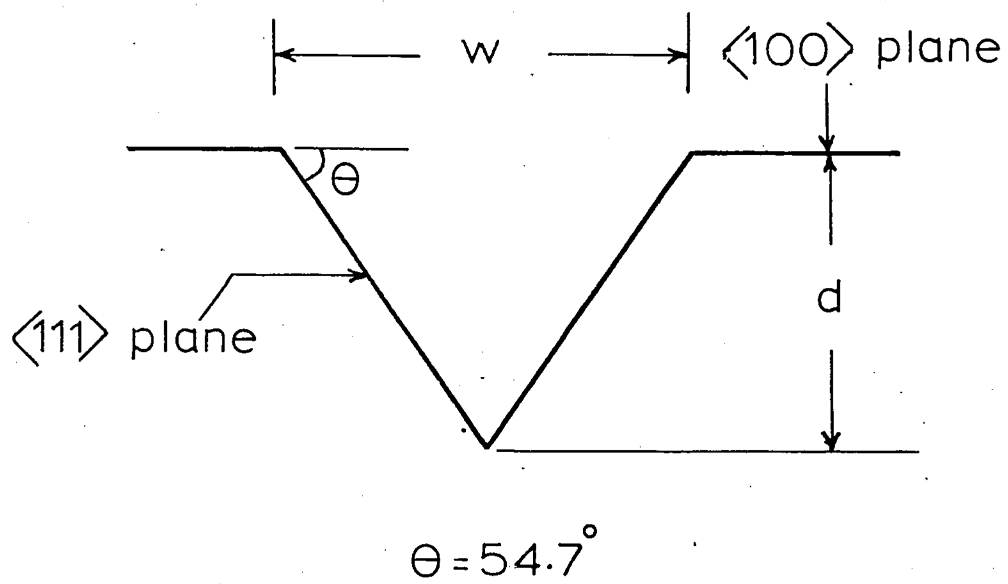

Fig. 3.2 Schematic of a V-groove defining the depth d, and width w of the groove.

oxide be thick enough to give flat-band voltages ($V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{ox}}$) greater than the punch-through voltage of the device. This is to prevent premature switching of the device triggered by inversion under the field oxide, before the onset of positive feedback of holes from the p^+ substrate. A detailed study of the effect of field oxide fabrication conditions on device switching has been carried out by Duncan et al. (3-3). Test MOS capacitors fabricated during the same run yielded flat-band voltages of $\sim$18V, much larger than the punch-through voltages of both the X(V_{PT}) = 6 V) and the L devices (V_{PT} =10.5V).

While photoresisting the V-grooved surfaces, it was noticed that spinning the photoresist at the conventional 4000 rpm caused the resist to thin at the edges of the V-groove and even completely break in some cases. To improve the adhesion the photoresisting procedure (B) was altered in three ways:

(i) After field oxide growth the wafers were baked in a single-walled quartz tube furnace at 700°C in dry O_2 (1 ℓ/min) for 15 mins. This treatment removed most of the water from the oxide surface that may have remained after the wet field oxide growth. It is well established that even traces of water (in particular OH^- ions) on the wafer surface causes a drastic degradation in the adhesion properties of the resist. The post-oxidation "drying" just described improved the adhesion of the photoresist dramatically.

(ii) The photoresist spinning speed was reduced to 2000 rpm. This resulted in a thicker film of photoresist over the wafer. Conse-

quently, the thinning of the film that results at the V-groove edge did not lead to a break in the resist as seen before with films spun at 4000 rpm.

(iii) Because of the increase in resist film thickness, the exposure time was increased to 45 secs to ensure that the full depth of the resist film was exposed.

Finally, the oxide was etched away from the desired areas in buffered HF and the photoresist removed by boiling in acetone.

3.1.5 Tunnel-Oxide Growth

After etching the oxide, the wafers were given a standard pre-furnace clean (Appendix A) with the following variation. After boiling in the peroxide-HCl solution (step IV), the wafers were rinsed in DI water and then blown dry in N_2, prior to the final HF etch. Secondly, before growing the tunnel-oxide, the wafers were baked in dry N_2 (1 ℓ/min.) at 700°C for 10 mins. in a single-walled resistance heated quartz tube furnace. These two processes were found to be essential in the fabrication of satisfactory switching devices with reproducible characteristics.

The first process ensures that the thin oxide grown during the peroxide cleans, over the regions defined for tunnel oxide growth was completely removed by the final HF etch. Hence, a fresh silicon surface (save native oxide) was exposed for tunnel-oxide growth.

The main purpose of the N_2 bake-out was to remove residual water from the wafer surface after the DI water rinse. Traces of

water can critically affect the oxidation rate of the silicon surface especially when the oxide thickness is of the order of 20 Å. Hence, to have any control on the oxidation rate the silicon surface must be absolutely dry, and the N_2 bake-out seemed to accomplish the purpose satisfactorily. However, there were no detailed studies carried out during the course of this work to determine the exact effect the N_2 treatment had on the silicon surface.

The tunnel-oxide growth was done in a single-walled resistance heated furnace in dry O_2. The furnace conditions employed for the tunnel-oxide growth are listed below.

Furnace temperature:	700^oC
Ambient:	dry O_2
Flow rate:	1 ℓ/min.
Oxidation times:	6 mins. X3; L3 8 mins. X4; L4 12 mins. X4; L5

3.1.6 First Metallization

In order to obtain reproducible switching characteristics, immediately after the tunnel-oxide growth, the wafers were loaded in a vacuum deposition system for aluminium deposition of the cathode electrode of the MISS device. However, as the metallization was done immediately after the tunnel-oxide growth, a thin oxide also covers the contact hole regions of the n^+ diffusion. Hence, the oxide has to be removed and another layer of aluminium deposited to obtain good ohmic contact. Thus, two metallizations are necessary

for the final fabrication of the device.

The aluminum used for evaporation was of 99.999% purity. Prior to loading into the filament the aluminum was cleaned using process C. Filament evaporation was the technique employed and the metallization was performed at a pressure of $\sim 10^{-6}$ torr. The resultant Al film thickness was $\sim$5000 Å.

3.1.7 Removal of the Thin Oxide over Contact Holes

Immediately after metallization, the wafers were photoresisted in a manner similar to that described in Section 3.1.4. Aluminium was etched away from the contact hole areas by dipping the wafers in PAN etch, which was maintained at a temperature of 45°C. The composition of the etch is presented below. The percentages by volume are

Phosphoric acid:	80%
Acetic acid:	5%
Nitric acid:	5%
DI water:	10%

The phosphorous pre-deposition mask was used for exposing the n^+ areas to the PAN etch. After the Al etch the wafers were rinsed in DI water and then etched in 10% HF for 10 secs to remove the tunnel-oxide grown over the contact areas. This etching was monitored from the back of the wafer (which also has a layer of tunnel-oxide) and is complete when the back surface becomes hydrophobic.

3.1.8 Second Metallization and Electrode Definition

After the HF etch, the wafers were rinsed in DI water, then boiled in acetone to remove the photo-resist and a second layer of aluminium evaporated in identical fashion to the process described in Section 3.1.7. Photoresist was applied to the wafers immediately after the evaporation, and the electrodes defined using the mask for the final electrode patterns. The aluminium etching conditions were the same as in the previous section.

After removal of the photoresist by boiling in acetone, Al was evaporated (Section 3.1.7) onto the back of the wafers to provide a good ohmic contact.

The complete fabrication procedure is presented as a flow-chart in Figure 3. 3.

3.2. MEASUREMENT TECHNIQUE

The D.C. two-terminal I-V characteristics of the MISS were obtained by applying a very slow voltage ramp (0.005 V S^{-1}) to the device via a HP 3310B function generator. A load resistor R_L=90KΩ was kept in series with the device to limit the current in the ON state. The measurement configuration used is shown in Fig. 3.4.

The voltage across the device was measured using a Keithley 616 digital electrometer with an input impedance $R_{in} = 10^{14}\ \Omega$. The high input impedance ensured that the electrometer would not shunt the MISS in the OFF state ($R_{off} \simeq 10^6\ \Omega$) and hence lead to erroneous measurements. The current through the device was measured

via a Keithley 177 microvolt digital multimeter. A graphical plot of the I-V characteristics was obtained by feeding the analog outputs from the multimeter and electrometer to the input terminals of a HP 7044A X-Y recorder.

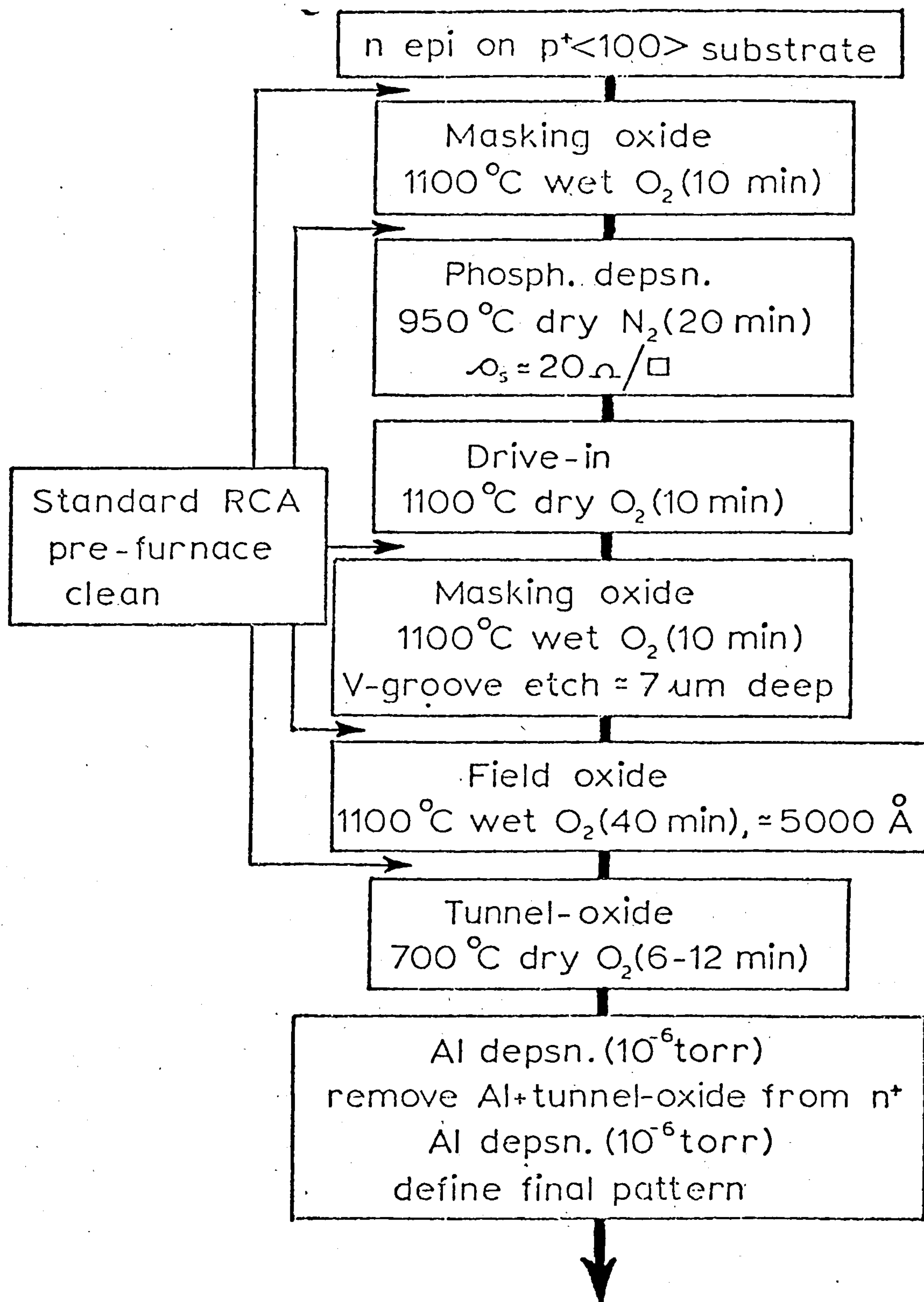

Fig. 3.3 Flow chart of the fabrication procedure employed for the isolated 3-terminal MISS, i.e. with an n^+ diffusion.

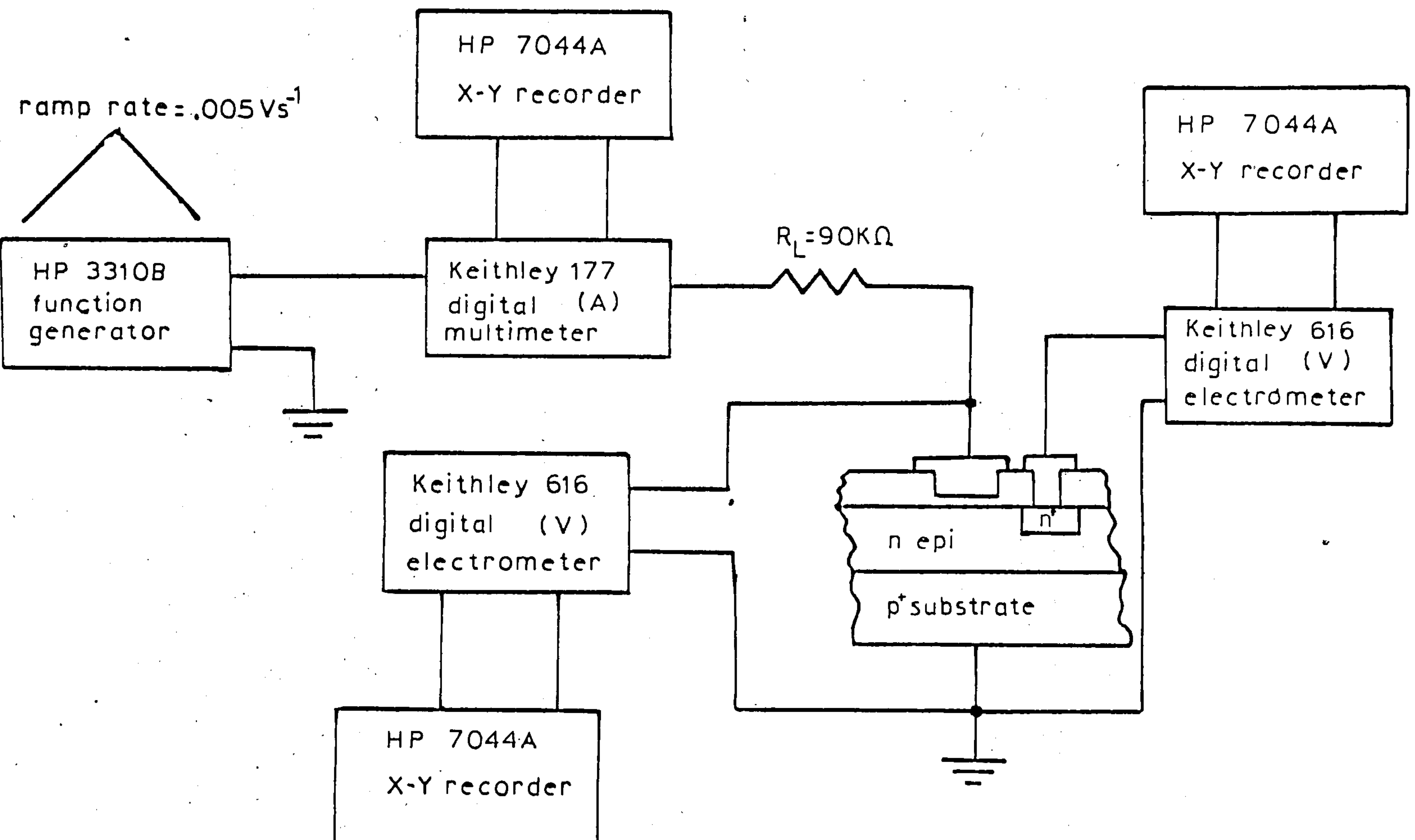

Fig. 3.4 Measurement set-up used for obtaining the D.C. I-V characteristics of the MISS device.

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3-2 H. F. Wolf, "Silicon Semiconductor Data," Pergamon Press, 1969.

3-3 K. A. Duncan, P. D. Tonner, J. G. Simmons and L. Faraone, "Characteristics of Metal/Tunnel-oxide/n/p^+ Silicon Switching Devices: Part I: Effects of Device Geometry and Fabrication Processes," (to be published).

CHAPTER 4

In this chapter the experimentally observed DC two-terminal characteristics of the isolated MISS is presented. The I-V characteristics of non-isolated devices, labeled "N," are also discussed to bring out their substantially different behaviour from the isolated MISS devices fabricated under exactly the same conditions (see Chapter 3 for fabrication details).

Figure 4.1 shows a schematic of the isolated MISS in cross-section defining the various parameters useful in qualitatively understanding the observed I-V characteristics. It is important to note that the device current is considered positive flowing away from the cathode as shown in Fig. 4.1. The reason for this convention is because the natural direction of current flow in the device is in this direction and adoption of the above convention helps eliminate a preponderance of negative signs in the writing of current-voltage equations.

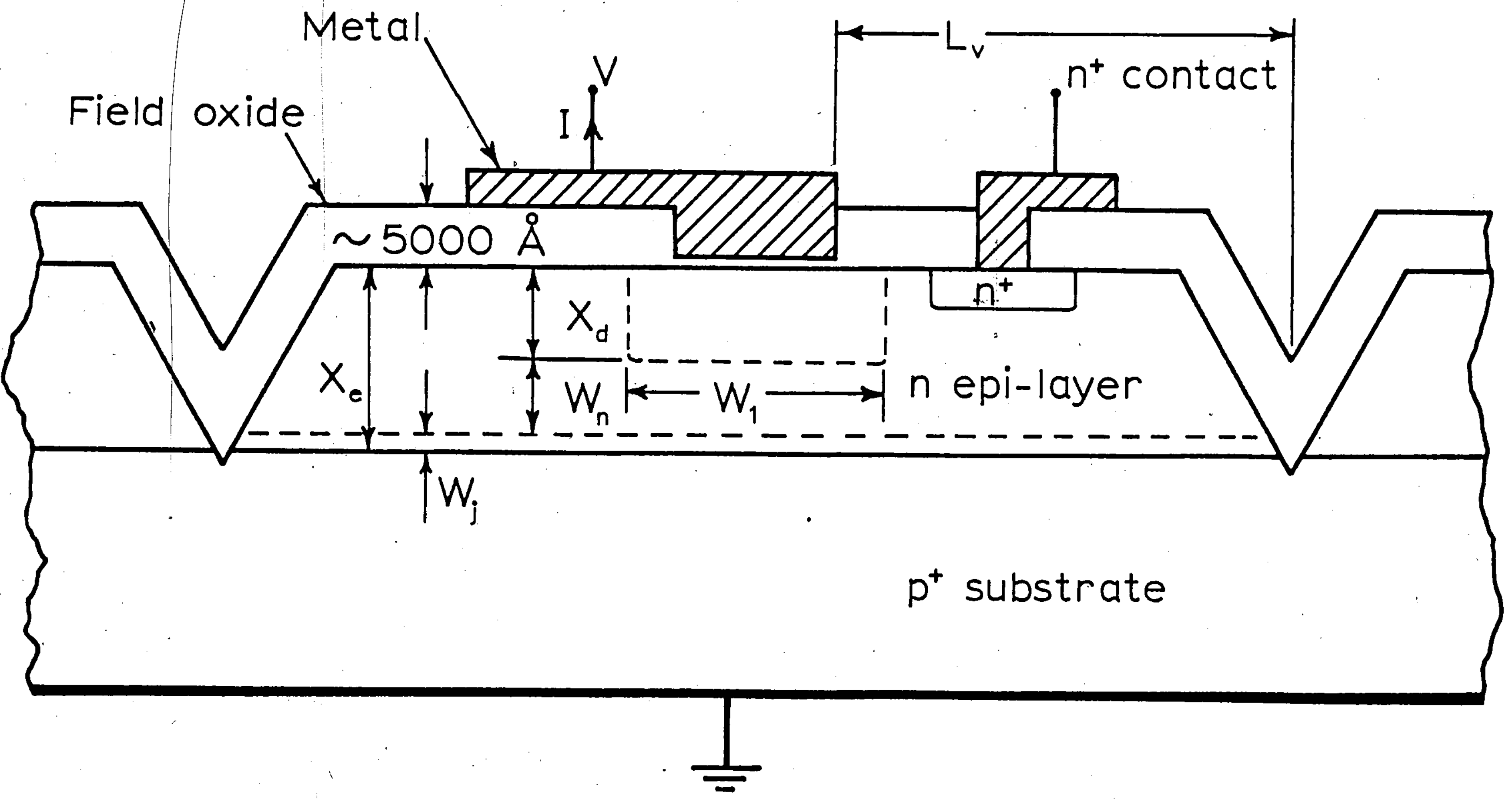


Fig. 4.1 Schematic diagram of the isolated MISS device in cross-section.

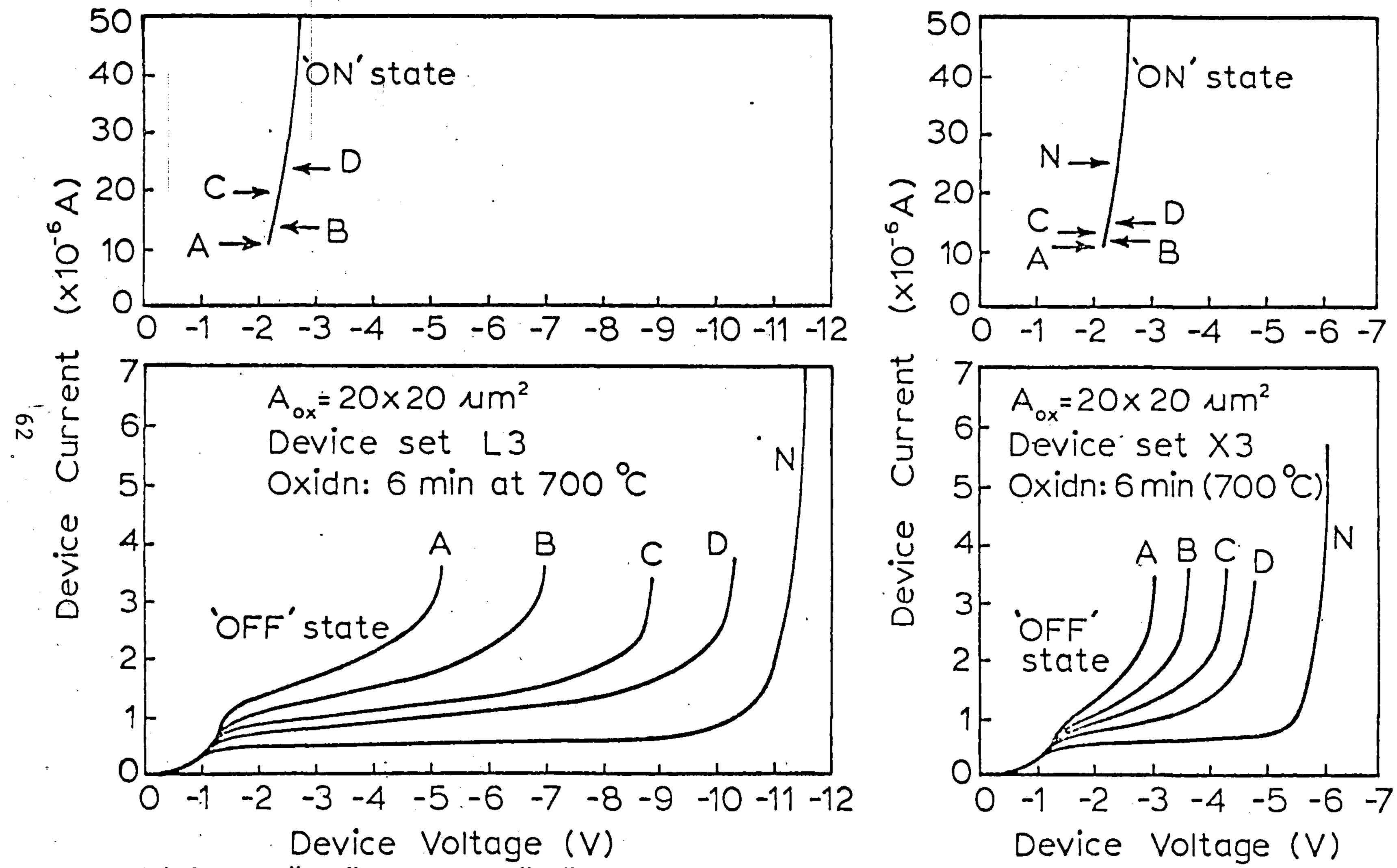
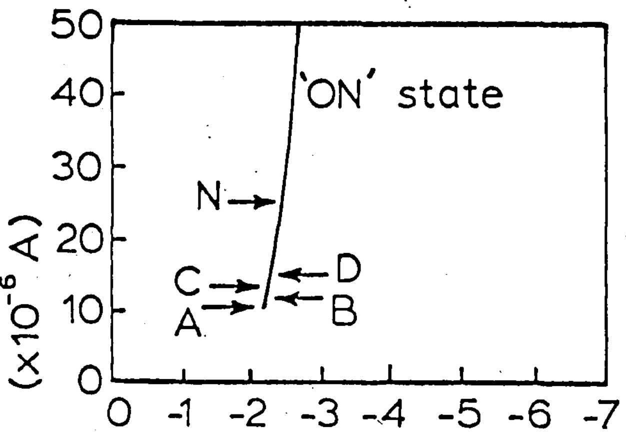
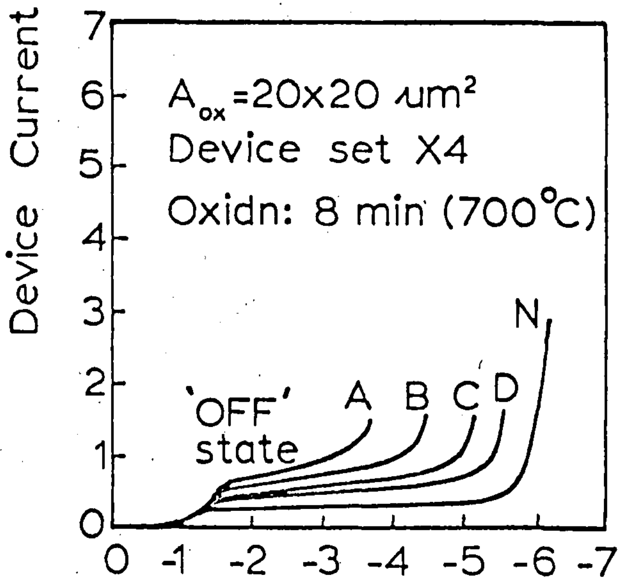
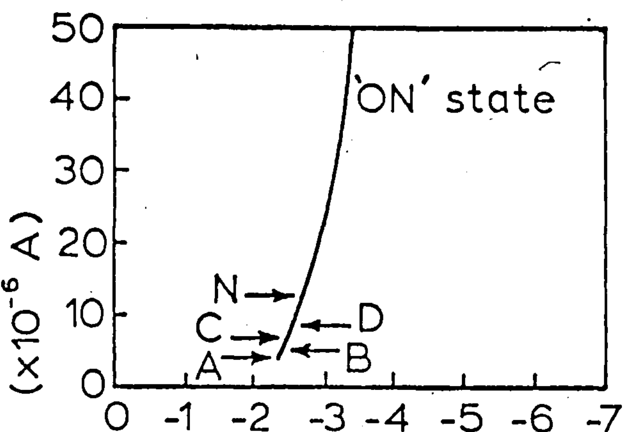


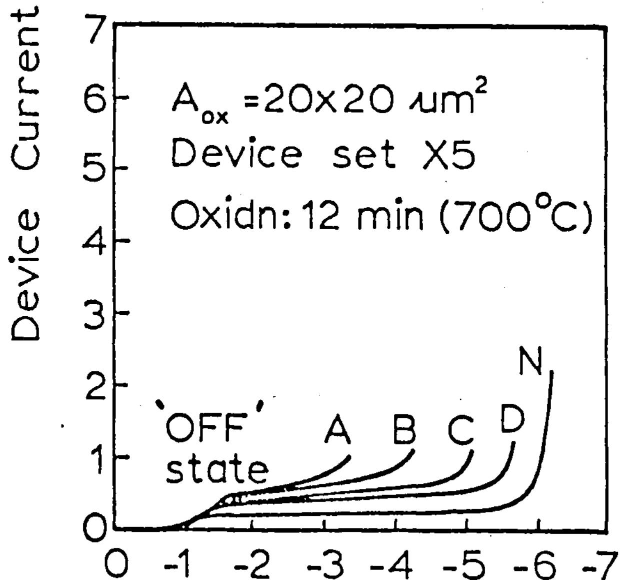
Fig. 4.2 The "OFF" state and "ON" state characteristics for each set of devices used in this study. The devices designated as "N" were non-isolated. All other devices were isolated with the following p^+-n junction areas: (see next page)





devices "A" ; 80 x 80 μm^2
devices "B" ; 100 x 100 μm^2





devices "C" ; 140 x 140 μm^2
devices "D" ; 220 x 220 μm^2

4.2 (Continued)

4.1 EXPERIMENTAL CURRENT-VOLTAGE CHARACTERISTICS

The experimental I-V curves for each set of devices are illustrated in Fig. 4.2. For ease of comparison, the characteristics are divided into ON state and OFF state.

4.1.1 Effect of Junction Area

From the OFF state characteristics shown in Fig. 4.2 it can be seen that the switching voltage, V_s, increases with increasing junction area A_j. This trend is consistently observed independent of tunnel-oxide thickness, d_{ox}, or the material parameters of the substrate. It is also important to note that the non-isolated devices (designated as "N" in Fig. 4.2) from the "X" batch of wafers all switch at 6±0.25 V. This value is in good agreement with that obtained via the "ideal" punch-through model proposed by Simmons et al. (4-1 to 4-3) (see Section 2.1) which, from the device parameters, is calculated using eqn. 2.6 to be 6.5 V. A further observation to be made from Fig. 4.2 is that the non-isolated device from set L3 does not switch to the ON state even though punch-through is reached. A physical explanation of this behaviour has been provided in Section 2.3.1 in terms of the weakening of the regenerative feedback mechanism which is responsible for the switching transition from the OFF to the ON state.

In contrast to the switching voltage, the switching current, I_s, was found to be practically insensitive to changes in either the isolated p^+-n junction area or material parameters. From the results presented in Fig. 4.2 it can be seen that, for a given d_{ox},

I_s is essentially constant for all the isolated devices. Of particular interest are the device sets L3 and X3, which were fabricated on totally different substrates.

The device parameters are listed below.

Device No.	Material Parameters
X3	n-epitaxial material of starting thickness 7.4 μm and resistivity 10.8 Ωcm grown on a p^+<100> substrate of resistivity 0.005-0.01 Ωcm.
L3	n-epitaxial material of starting thickness 9.7 μm and resistivity 18.0 Ωcm grown on a p^+<100> substrate of resistivity 0.06-0.12 Ωcm.

To ensure identical tunnel-oxide characteristics, the two wafers were oxidized simultaneously in dry O_2 at 700°C for 6 mins. The important result to note is that I_s is constant for all the isolated devices in sets X3 and L3 even though the OFF state currents and switching voltages differ substantially. This result suggests that the switching current is determined solely by the characteristics of the tunnel-oxide.

Another very important point to note from the results in Fig. 4.2 is that all the non-isolated devices (designated "N") switch at a much higher current than the corresponding isolated devices. This can be attributed to enhanced minority carrier recombination in the junction depletion region and in the neutral epi-layer due to the current fringing effects described in Section 2.3.1. Essentially, this means that a larger device current is required to supply the critical value of injected hole current under the tunnel-oxide necessary to switch the device. The observation

that a critical value of hole current, I_{pj}, is necessary to switch a device with a certain oxide thickness, d_{ox}, independent of junction area (or equivalently, constant I_s), is of paramount importance in the determination of the switching criterion of the device. A more detailed consideration of this observation is presented in Section 5.1.

From the characteristics shown in Fig. 4.2, it is seen that for a given applied voltage the current through the device in the OFF state, I_{off}, scales to lower levels with increasing A_j. In contrast to this, the holding current in the ON state, I_H, increases with increasing junction area. Furthermore, for a given tunnel-oxide thickness, the devices share the same ON state characteristic regardless of A_j.

4.1.2 Effect of Tunnel-oxide Thickness

A comparison of both the ON and OFF state I-V characteristics shown in Fig. 4.2 reveals that all the device currents I_{OFF}, I_s and I_H scale to lower magnitudes with increasing d_{ox}, i.e., increasing oxidation time. The variation of I_s and I_H with d_{ox} are presented in Figs. 4.3 and 4.4, respectively.

The experimentally observed dependence of the device parameters I_s, V_s, I_H, V_H and I_{off} on tunnel-oxide thickness and p^+-n junction area are summarized in Table 4.1.

4.2 DISCUSSION OF THE OFF STATE CHARACTERISTIC

4.2.1 Effect of Junction Area A_j

As discussed briefly in the previous section, for a given

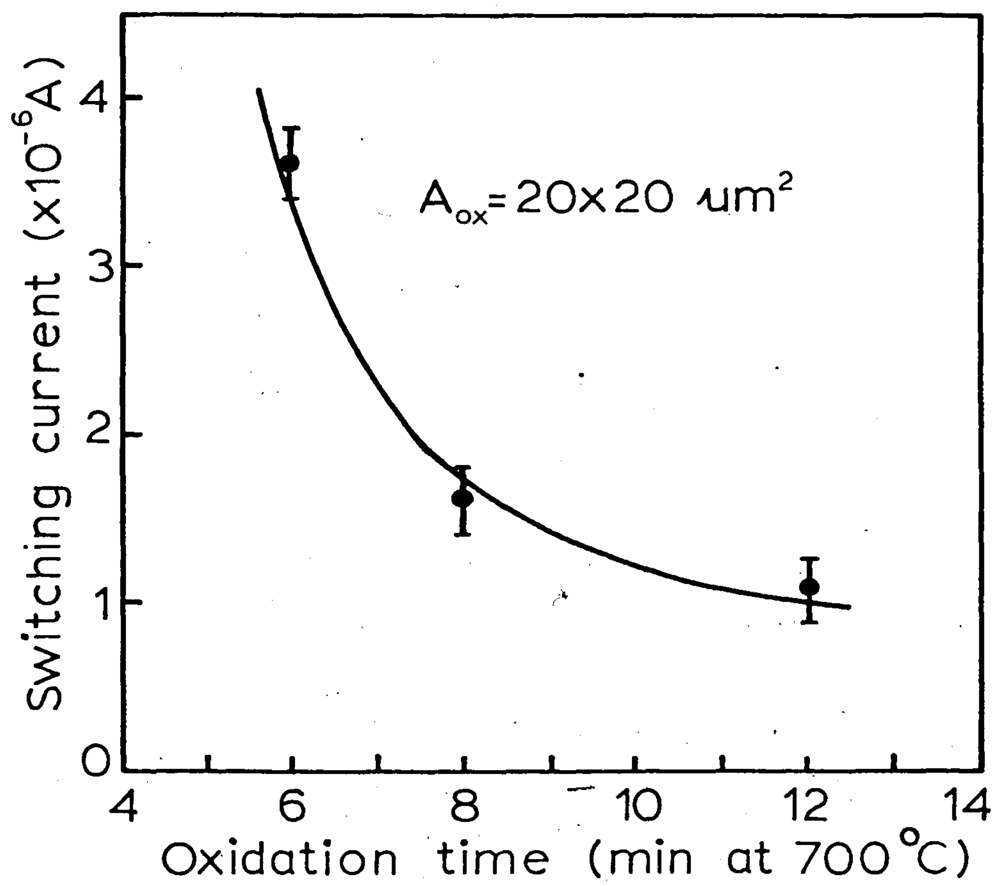


Fig. 4.3 Experimentally observed switching current as a function of oxidation time.

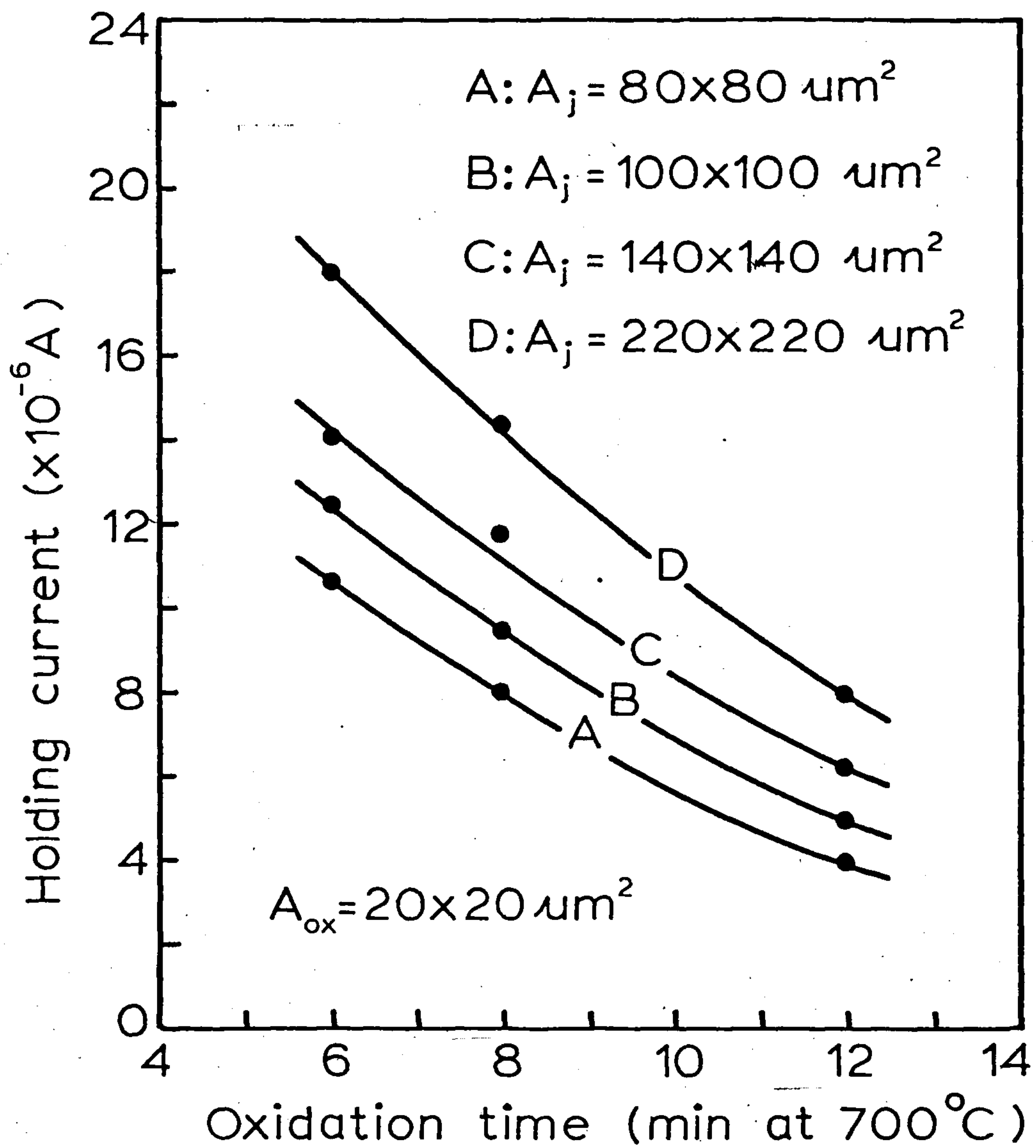


Fig. 4.4 Experimentally observed holding current as a function of oxidation time with isolated junction area as a parameter.

TABLE 4.1

	'OFF' state current, I_{OFF}	Switching current, I_S	Holding current, I_H	Switching voltage, V_S	Holding voltage, V_H
as A_j increases	decreases	independent	increases	increases	independent
as d_{ox} increases	decreases	decreases	decreases	no conclusion	increases

Variation of MISS device parameters with isolated p^+-n junction area and tunnel-oxide thickness.

applied voltage the OFF state current is seen to scale to lower levels for a corresponding increase in p^+-n junction area. For the MISS device in the OFF state, electron current continuity requires that

$$I_{nt} = I_{rj} + I_{nj} , \tag{4.1}$$

where the recombination current in the neutral epi-layer, I_{rn}, has been neglected since it is not significant for isolated devices in the OFF state (see Chapter 5), and

I_{nt} = Electron tunnel current from metal to semiconductor conduction band,

I_{rj} = Recombination current in p^+-n junction,

and I_{nj} = Electron diffusion current in p^+ substrate.

The generation current in the deep-depletion region under the tunnel-oxide has been omitted from eqn (4.1) since it is not significant for values of generation lifetime normally encountered in "device-grade" silicon. All the current components flowing in the system are shown in the energy band diagram of the MISS presented in Fig. 4.5.

For the polarity of bias we are considering, the silicon epi-layer of the MIS diode is depleted (reverse-biased), so the applied voltage is primarily absorbed in the surface deep-depletion region. Thus, for the MISS device in the OFF state, we can write

$$V = \psi_s + K , \tag{4.2}$$

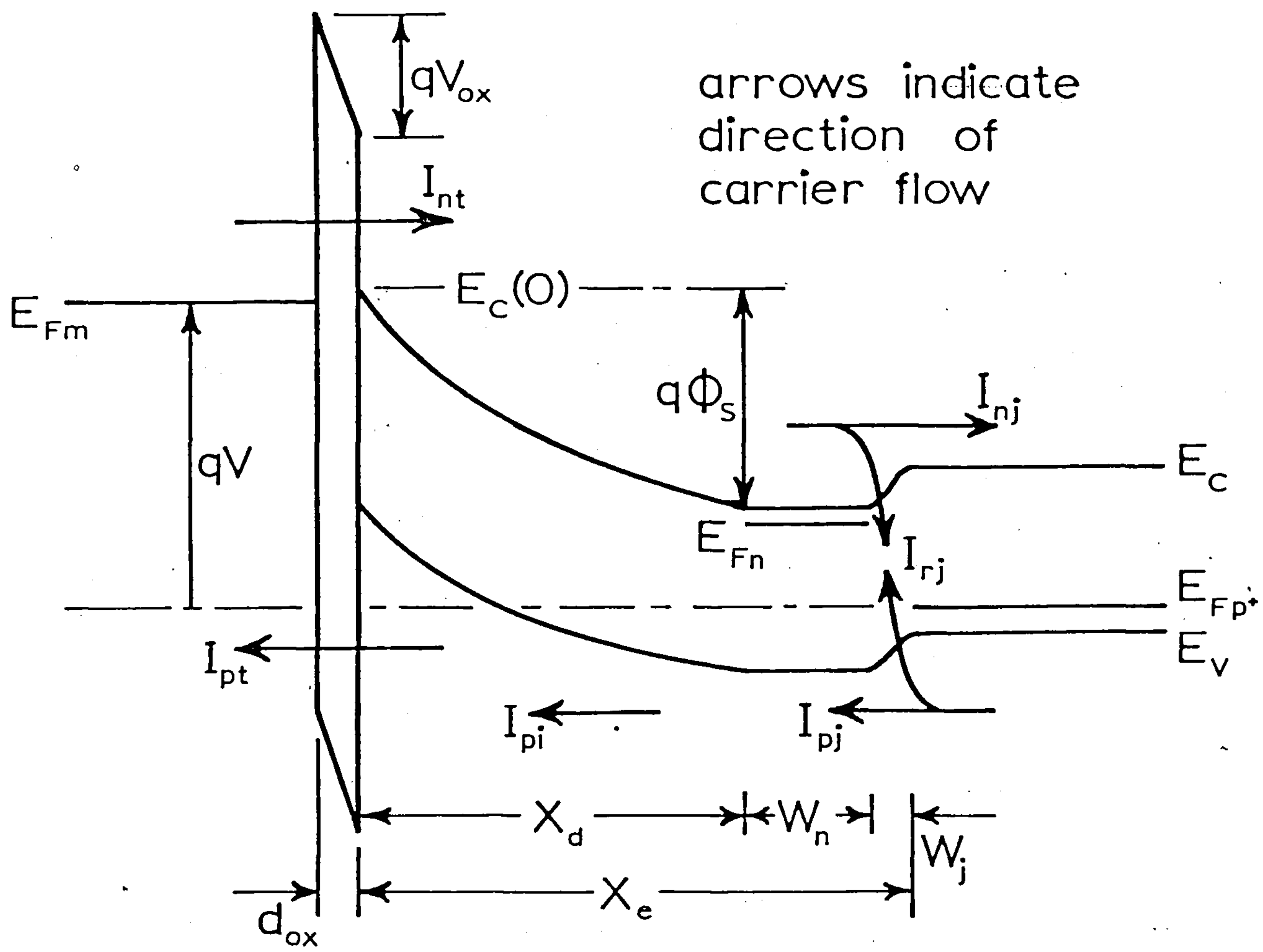


Fig. 4.5 Energy band diagram of the MISS device in the "OFF" state showing the current components flowing in the system.

where K is a constant of magnitude 1-2 volts depending on oxide thickness, and ψ_s is the surface potential at the Si-SiO_2 interface. The above equation is valid only when the magnitude of the applied voltage is greater than approximately 1.5 V, which corresponds to the characteristic "knee" seen in all OFF state curves (see Fig. 4.2). In actual fact, this point represents the applied voltage at which the semiconductor under the tunnel-oxide is at flat-band (4-4). In other words, for applied voltage magnitudes less than 1.5 V the semiconductor surface is accumulated and all the voltage is dropped across the oxide and the p^+-n junction (i.e. $V \simeq \phi_{ms} + V_{ox} + V_j$, where ϕ_{ms} is the metal-semiconductor work function difference). Beyond this point, the semiconductor surface is depleted and, consequently, any additional applied voltage is almost completely absorbed by the surface deep-depletion region. Under these conditions, eqn 4.2 is a good approximation with $K = \phi_{ms} + V_{ox} + V_j$ staying essentially constant relative to ψ_s.

For the materials used in this study, the electron diffusion current is not significant since $N_a >> N_d$. Thus, we can rewrite eqn 4.1 as

$$I_{nt} \simeq I_{rj} \; (= A_j J_{rj}) \; . \tag{4.3}$$

In other words, the electron tunnel current supplies the junction recombination current that biases the p^+-n junction. The expression for I_{rj} is given by

$$I_{rj} = A_j q \frac{n_i}{2\tau_1} W_j \exp\left(\frac{qV_j}{2kT}\right) \; , \tag{4.4}$$

where τ_1 is the recombination lifetime in the p^+-n junction depletion region, and W_j is the junction depletion width.

For the following discussion, consider a MISS device (with a relatively small p^+-n junction area A_j) biased in the OFF state at a particular value of applied voltage. Under these conditions, an electron tunnel current, I_{nt}, will flow in the device and bias the p^+-n junction according to the relations in eqns 4.3 and 4.4. If A_j is now increased, then ψ_s will remain essentially constant (from eqn 4.2). However, according to eqn 4.4, this same I_{nt} will induce a lower V_j as A_j is increased which, in turn, reduces the hole diffusion current across the p^+-n junction. As a result, the hole concentration at the Si-SiO_2 interface decreases. Thus, the field in the oxide is lowered, resulting in a reduced I_{nt} which further decreases the junction bias. The above process continues until steady-state is reached. From the above discussion it can be concluded that, for a particular applied voltage, the induced junction bias decreases as p^+-n junction area increases.

The total current flowing across the p^+-n junction is given by

$$\begin{aligned} I &= I_{rj} + I_{pj} + I_{nj} \\ &\simeq I_{rj} + I_{pj} , \end{aligned} \qquad (4.5)$$

since $N_a >> N_d$. It is important to note that when the surface of the MIS is deep-depleted (OFF state), the neutral region between the edge of the surface depletion region and the junction depletion

edge is very much smaller than the diffusion length for holes in the epi-layer. Hence, the hole diffusion current across the p^+-n junction is dominated by the component I_{pj1} flowing across region W_1 (see Fig. 4.1). Using the short-base diode approximation, I_{pj1} can be written as (4-5),

$$I_{pj1} = \frac{qA_1 D_p n_i^2}{N_d W_n} \exp\left(\frac{qV_j}{kT}\right) , \qquad (4.6)$$

where $A_1 = W_1^2$, and W_n is the width of the neutral region (see Fig. 4.1).

The results of eqns 4.2, 4.4, and 4.6 suggest that for a particular value of applied voltage we have:

(i) ψ_s (and hence X_d and W_n) is essentially constant and independent of A_j (from eqn 4.2).

(ii) the induced junction bias decreases as A_j is increased.

(iii) I_{pj1} (and hence the total device current), decreases with increasing A_j.

The above conclusions are consistent with the experimentally observed reduction in OFF state current with increasing p^+-n junction area (see Fig. 4.2).

4.2.2 Effect of Tunnel-oxide Thickness d_{ox}

The experimental results shown in Fig. 4.2 indicate that the OFF state current decreases monotonically with increasing tunnel-oxide thickness for any given junction area. For the MISS device, an increase in oxide thickness has a two-fold effect: (i) for a

given applied bias it causes a decrease in the electron tunnel current, and (ii) this, in turn, induces a lower junction bias and, consequently, a smaller hole injection current across the p^+-n junction. Both these effects contribute to the lower currents seen for thicker-oxide devices. A more rigorous treatment involving the tunnel-oxide I-V equations is considered in the following chapter.

4.3 THE SWITCHING POINT

4.3.1 Effect of Junction Area on the Switching Current

In Section 4.2.1 it was shown that, in the OFF state, changes in the applied voltage are absorbed primarily in the surface depletion region (see eqn 4.2). Hence, the higher the switching voltage the larger will be the depletion width at the switching point. This larger depletion volume would result in a higher generation current. If the generation current was a significant component of the switching current, then one would expect a higher I_s for devices with higher switching voltages. This, however, was not observed. The results presented in Fig. 4.2 give the switching current as being approximately constant (to within 0.2 μA) for devices with a particular oxide thickness, independent of junction area.

If the switching current is related in any way to the area of the p^+-n junction then again one would see a variation in I_s for the various junction areas, which range from $0.64 \times 10^{-4} cm^2$ to $4.84 \times 10^{-4} cm^2$. From the above arguments it can thus be concluded

that the MISS switching current is dependent only on the tunnel-oxide characteristics.

Further proof of the total oxide-controlled nature of the switching mechanism lies in the fact that devices made on completely different materials but having the same oxide thickness (X3 and L3), have essentially the same switching current.

4.3.2 Effect of Oxide Thickness on the Switching Current

From purely theoretical arguments, Habib and Simmons (4-3) have shown that at the switching point the hole concentration at the $Si\text{-}SiO_2$ interface, $p(0)$, is much greater than the equilibrium strong inversion concentration; i.e. $p(0) \gg N_d$. This implies that E_{Fm}, the metal Fermi level, approaches $E_c(0)$, the conduction band edge at the silicon surface. Alternatively, the following equation can be written

$$E_{Fm} \simeq E_c(0) \quad . \tag{4.7}$$

Using the above condition, and recognizing that the hole diffusion current, I_{pj}, is the dominant current in the system at switching (borne out by calculations based on the model presented in Chapter 5), the following equation can be derived:

$$I_{pj} \simeq I_{pt} = A_{ox} A^* T^2 \frac{p(o)}{N_v} \exp(-\chi_p^{\frac{1}{2}} d_{ox}); \; V=V_s \; , \tag{4.8}$$

where I_{pt} = hole tunnel current from silicon valence band to metal,

A^* = Richardson constant,

N_v = density of states at the valence band edge,

d_{ox} = tunnel-oxide thickness,

χ_p = tunnel-oxide barrier height for holes.

This equation is valid at the switching point.

It can be shown (see Section 5.2) that the p(0) required for switching decreases linearly with d_{ox}. However, for the range of tunnel-oxide thicknesses studies (18-25 Å), p(0) remains fairly constant and its weak dependence on d_{ox} is not sufficient to explain the strong dependence of I_s on d_{ox}. However, the observed decrease in I_s with increasing d_{ox} can be attributed to the factor $\exp(-\chi_p^{1/2} d_{ox})$ appearing in eqn 4.8 . This stronger dependence of switching current on d_{ox} is consistent with the experimental results shown in Fig. 4.3.

4.3.3. The Switching Voltage

As discussed in Section 4.2.1, the junction current flowing under the surface depletion region can be described by the short-base diode equation. This is especially valid close to switching, since the neutral region, W_n, is typically less than 2 μm. In addition, since W_n is very much smaller than the lateral dimensions of the device structure, it would be expected that the injected hole current from this region would be the dominant component of the current reaching the $Si\text{-}SiO_2$ interface (confirmed by calculations based on the model presented in Chapter 5).

The hole current injected by the area A_1 directly under the tunnel-oxide is given by eqn 4.6. Furthermore, in Section 4.2.1 it was determined that a larger junction area will lead to a lower bias

across the p^+-n junction, for a given surface potential. Since I_{pj1} is the dominant current flowing in the device at switching, to a good approximation we can write

$$I_s \simeq I_{pj1} . \qquad (4.9)$$

Equations 4.6 and 4.9 suggest that, in order to reach the critical value of switching current, a device with a larger junction area requires a narrower neutral region. This condition necessarily means that X_d (or equivalently the voltage V_s) is larger for devices with larger A_j. The above conclusion is consistent with the experimentally observed increase in switching voltage with increasing isolation area.

4.3.4 The Holding Point

When the MISS device is in the ON state, it is characterized by a small device voltage due to a greatly reduced depletion region under the tunnel-oxide. In point of fact, the depletion width is at its strong-inversion value (4-1,4-3,4-6) given by (4-5),

$$X_{d,inv} = \left(\frac{4\varepsilon_s \phi_n}{qN_d} \right)^{1/2} .$$

The device will remain in the ON state if the injected hole current reaching the interface, I_{pi}, is high enough to maintain the collapsed depletion region. If I_{pi} falls below a critical value, then holes at the interface are drained through the oxide faster than the junction can supply them. This lowering of hole concentra-

tion at the interface reduces the field in the oxide, causing a decrease in the electron tunnel current which consequently reduces the induced bias across the p^+-n junction. This, in turn, decreases I_{pj} and thus a negative feedback mechanism is initiated which causes the device to switch to the OFF state. The total device current at which this transition occurs is defined as the holding current, I_H.

At the holding point, in contrast to the situation at the switching point, the recombination current in the neutral epilayer is comparable to the injected hole current under the oxide. This is a consequence of several factors (consider tunnel-oxide thickness and area as being constant).

(i) Since the holding currents are much greater than the switching current (see Fig. 4.2), the induced junction bias is substantially higher to supply the required device current. This is also verified experimentally by monitoring the junction voltage via the n^+ contact (see Fig. 4.1).

(ii) The depletion width is at $X_{d,inv}$, which decreases the injected hole current contribution of the region directly under the oxide due to an increase in W_n (see eqn 4.6).

(iii) As a result of (i) and (ii), the contribution of hole diffusion current from the areas surrounding the tunnel-oxide is greatly enhanced.

The importance of recombination in the neutral epi-layer when the device is in the ON state is clearly brought out by the fact

that non-isolated devices have much higher holding currents (see Fig. 4.2). Since the hole diffusion length in the epi-layer is of the order of the lateral dimensions of the isolation areas (~50 μm), we can expect the minority carrier recombination to be much greater in the non-isolated devices where current fringing occurs (4-7). Thus the hole current that actually reaches the tunnel-oxide is much less than the hole diffusion current across the p^+-n junction; i.e., $I_{pi} << I_{pj}$. Under these conditions, the critical level of hole current required to maintain the surface inverted requires a larger current flowing through the device. This additional current is due to the enhanced recombination in the epi-layer at the higher junction biases typical for the ON state.

From the above discussion the following can be concluded: as isolated junction area is increased, the total device current at the holding point will be greater as a result of increasing recombination current within the neutral epi-layer surrounding the tunnel-oxide. This is in direct agreement with the experimental results presented in Fig. 4.4. Furthermore, similar arguments to those in Section 4.3.2 can be used to adequately explain the decrease in holding current for an increase in tunnel-oxide thickness (see Fig. 4.4).

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CHAPTER 5

In this chapter the qualitative discussion of the D.C. two-terminal behaviour of the MISS presented in the preceding chapter is put on a more rigorous theoretical footing.

The observation of a constant current I_s necessary to switch the MISS is used to determine the switching criterion. Furthermore, on the basis of current-voltage relations for the tunnel-oxide the dependence of I_s and I_H on the tunnel-oxide thickness, d_{ox}, has been adequately explained. Finally, a two-dimensional model has been formulated to effectively predict the variation of the MISS parameters I_s, I_H and V_s with changes in the p^+-n junction area, A_j.

It is worthwhile emphasizing again the sign convention for the current flowing through the MISS is chosen to be positive, flowing away from the cathode.

5.1 DETERMINATION OF THE SWITCHING CRITERION

Figure 5.1 illustrates the energy band diagram of the MISS in the OFF state with the various current components flowing in the system. As seen from the diagram, the MISS can essentially be considered as a reverse-biased MIS tunnel diode in series with a forward-biased p^+-n junction. Hence, the currents flowing in the system can be analyzed either by using the tunneling equations for the oxide or the current-voltage equations for the p^+-n junction. In the following discussion, we will consider the tunnel currents flowing in the MIS structure with a negative voltage applied to the metal electrode. (Note: The generation current occurring as a result of thermal generation within the depletion region under the oxide is not considered since it is negligible compared to other current components measured in MISS devices.)

Using standard notation (see list of symbols), the electron tunnel current density flowing from the conduction band of the n-silicon to the metal in this Al/SiO_2/n-Si structure is given by Card (5-1), as

$$J_{nt} = A^*T^2\left\{\exp\left(\frac{E_{Fm}-E_c(0)}{kT}\right) - \exp\left(\frac{E_{Fn}(0)-E_c(0)}{kT}\right)\right\}\exp(-\chi_n^{1/2}d_{ox}), \qquad (5.1)$$

where d_{ox} is in Angstroms. The hole current density flowing from the valence band of the n-silicon to the metal is given by

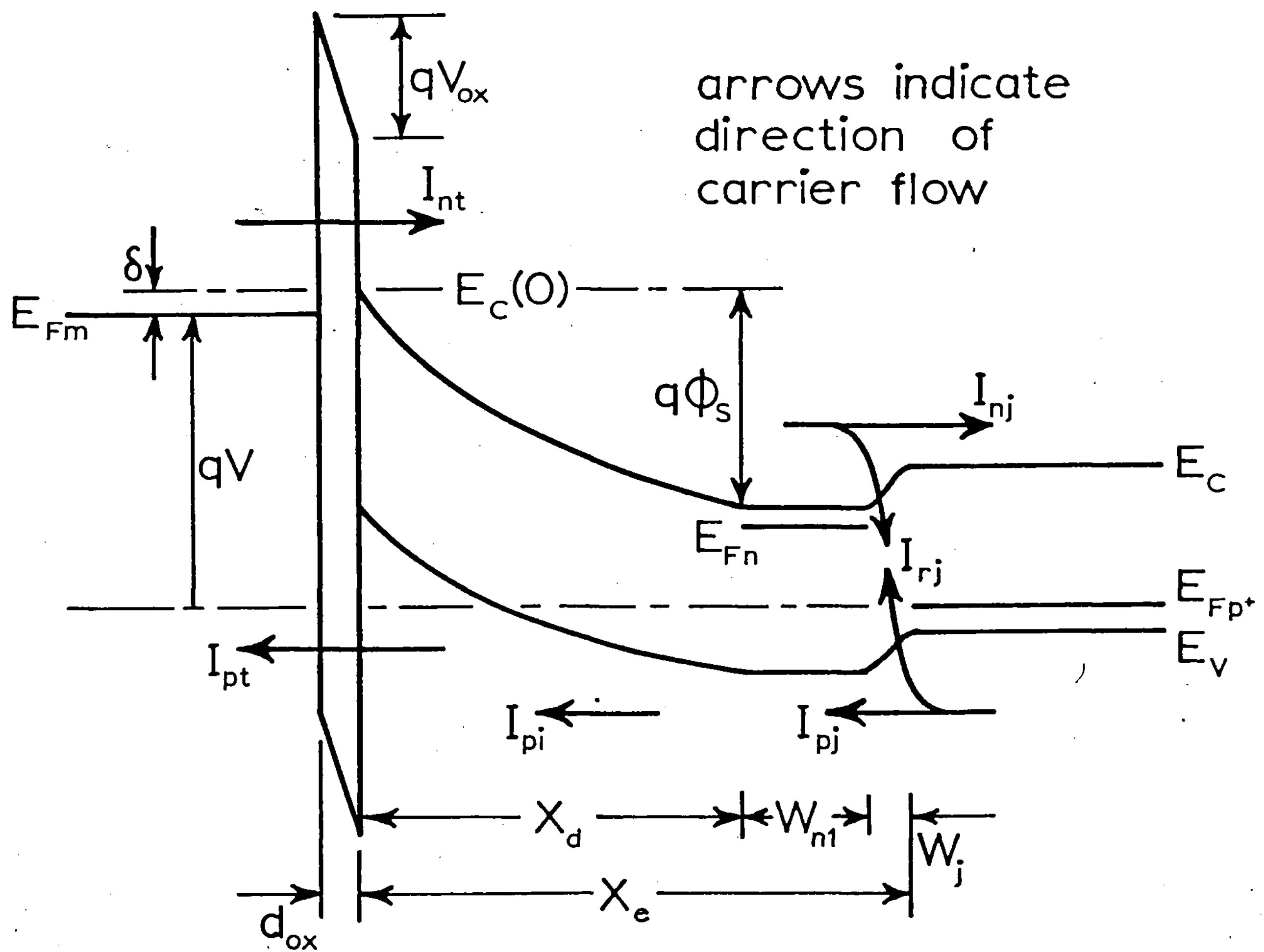

Fig. 5.1 Energy band diagram of the MISS device close to switching with the electron and hole current components.

$$J_{pt} = A^* T^2 \left\{ \exp\left(\frac{E_v(0)-E_{Fp}(0)}{kT}\right) - \exp\left(\frac{E_v(0)-E_{Fm}}{kT}\right) \right\} \exp(-\chi_p^{1/2} d_{ox}). \tag{5.2}$$

From purely theoretical arguments, Habib and Simmons (5-2) have shown that at switching the hole concentration at the interface is much greater than the equilibrium strong inversion concentration; i.e., $p(0) >> N_d$. This condition is analogous to $E_{Fp}(0)$ (the quasi-Fermi level for holes at the $Si-SiO_2$ interface), being much closer to $E_v(0)$ than to E_{Fm} (the metal Fermi level), as illustrated in Fig. 5.1. Therefore

$$\exp\left(\frac{E_v(0)-E_{Fp}(0)}{kT}\right) >> \exp\left(\frac{E_v(0)-E_{Fm}}{kT}\right) \ ; \quad V=V_s. \tag{5.3}$$

Using this inequality, eqn 5.2 can be written as

$$J_{pt} = A^* T^2 \exp\left(\frac{E_v(0)-E_{Fp}(0)}{kT}\right) \exp(-\chi_p^{1/2} d_{ox}); \quad V=V_s \tag{5.4}$$

The hole concentration at the $Si-SiO_2$ interface is related to the hole quasi-Fermi level at the surface by the equation

$$p(0) = N_v \exp\left(\frac{E_v(0)-E_{Fp}(0)}{kT}\right). \tag{5.5}$$

Hence, eqns 5.4 and 5.5 yield the following relation between J_{pt} and $p(0)$:

$$J_{pt} = A^* T^2 \frac{p(0)}{N_v} \exp(-\chi_p^{1/2} d_{ox}); \quad V=V_s \tag{5.6}$$

Since all I-V measurements were obtained by using a slow voltage ramp (essentially D.C.), the device remained in steady-state. Hence the hole current reaching the interface, I_{pi}, is always equal to the hole current tunneling through the oxide, that is,

$$I_{pi} = I_{pt} \ (= A_{ox} J_{pt}). \tag{5.7}$$

Furthermore, for the MISS device in the OFF state, recombination in the neutral epi-layer is negligible, hence I_{pi} is approximately equal to the hole diffusion current across the p^+-n junction. Thus, from eqn 5.7:

$$I_{pt} (= A_{ox} J_{pt}) \simeq I_{pj} \ . \tag{5.8}$$

From a detailed analysis of the experimental results presented in Chapter 4, it was concluded that for a given tunnel-oxide thickness and area, an essentially constant value of I_{pj} is required to switch the device. This critical value was determined to be independent of isolated junction area and material parameters, provided that $N_A >> N_d$ and junction recombination dominates over recombination in the neutral epi-layer. From the above discussion, and the expression for J_{pt} at switching given by eqn 5.6, to a first approximation it can be concluded that for a given d_{ox} an essentially constant $p(0)$ is present under the tunnel-oxide at the switching point.

5.2 SWITCHING CURRENT AND HOLDING CURRENT AS A FUNCTION OF OXIDE THICKNESS

The experimental results presented in Chapter 4 indicate that the switching current decreases for increasing d_{ox}. In the preceding section, it was stated that $p(0) >> N_d$ at the switching point. This implies that E_{Fm} approaches $E_c(0)$. In Fig. 5.1, the separation between E_{Fm} and $E_c(0)$ is represented by δ, where $\delta << E_g$. Hence, in writing the switching voltage relationship for the MISS, to a good approximation E_{Fm} can be considered to be at $E_c(0)$ (i.e., $\delta \approx 0$). Referring to the band diagram of Fig. 5.1, the following voltage relationship can be written for the MIS diode at the switching point:

$$\phi_{ms} + \frac{Q_g}{C_{ox}} + \psi_s = E_{Fm} - E_{Fn} \; ; \quad V = V_s . \tag{5.9}$$

where E_{Fn} is related to the Fermi level in the p^+ substrate by the equation

$$E_{Fn} = E_{Fp^+} + V_j \; .$$

As a consequence of $p(0) >> N_d$, the inversion charge Q_i is much greater than the depletion charge Q_d; thus $Q_g \approx -(Q_{ss} + Q_i)$ and eqn 5.9 becomes

$$\phi_{ms} - \frac{Q_{ss}+Q_i}{C_{ox}} + \psi_s = E_{Fm} - (E_{Fp^+} + V_j); \quad V=V_s \; . \tag{5.10}$$

By considering the energy band diagram of Fig. 5.1, E_{Fm} is related to $E_v(X_d)$ by

$$E_{Fm} - E_v(X_d) \simeq E_g + \psi_s \quad ; \quad V=V_s \tag{5.11}$$

since $\delta << E_g$. Using the above relation in eqn (5.10) gives

$$\phi_{ms} - \frac{Q_{ss}+Q_i}{C_{ox}} \simeq (E_v(X_d)-E_{Fp^+}) + E_g - V_j \quad ; \quad V=V_s . \tag{5.12}$$

Measurement of the junction voltage at switching via the n^+ contact showed that V_j varied between 0.35 ± 0.02 V from devices with one oxide thickness to another. Hence $(E_v(X_d)-E_{Fp^+})-V_j$ is essentially constant. Furthermore, ϕ_{ms} and E_g are both constant; thus eqn (5.12) leads to the important result that

$$\frac{Q_{ss} + Q_i}{C_{ox}} \quad \text{constant;} \qquad V=V_s \tag{5.13}$$

that is,

$$\left(\frac{Q_{ss}+Q_i}{\varepsilon_{ox}}\right) d_{ox} \quad \text{constant} \; ; \quad V=V_s \; . \tag{5.14}$$

If Q_{ss} is independent of d_{ox}, then Q_i must decrease as d_{ox} increases to satisfy the above equality. For the devices discussed in this paper, tunnel-oxide thickness varied from 18 Å to 25 Å which results in a relatively small variation of Q_i (and hence $p(0)$) as given by eqn (5.14). In other words, the change in oxide capacitance with d_{ox} is not sufficient to account for the variations of switching current with oxide thickness observed in Chapter 4. The factor that strongly affects the dependence of I_{pt} (and hence I_s) on d_{ox} is the exponential term in eqn (5.6). Assuming χ_p independent of d_{ox}, the factor $\exp(-\chi_p^{1/2} d_{ox})$ rapidly decreases with

increasing oxide thickness. Hence, from eqn (5.7), this suggests that the hole current required to switch the device also decreases rapidly with increasing d_{ox}, as observed experimentally (see Chapter 4). Similar arguments may be used to explain the experimentally observed decrease in holding current with increasing oxide thickness.

5.3 DERIVATION OF RELEVANT EQUATIONS FOR TWO-DIMENSIONAL MODEL

Figure 5.2 shows the current components in the MISS device. According to the switching mechanism discussed in Section 5.1, for a given d_{ox} and A_{ox} switching from OFF to ON occurs when the injected hole current under the oxide reaches a certain critical value. Similarly, the device switches from ON to OFF when the injected hole current falls below that value required to sustain the inversion layer under the tunnel-oxide. Thus, the important parameter to determine in any quantitative model for the device is the injected hole current reaching the $Si-SiO_2$ interface, designated as I_{pi}.

In deriving the model, several assumptions are made:

(i) The p^+ substrate is much more heavily doped than the n epi-layer, and consequently electron diffusion currents can be neglected. In the experimental resulted presented in Chapter 4, the N_a/N_d ratio varied from 3×10^3 for "L" devices to 5×10^4 for "X" devices.

(ii) At low junction bias (which occurs in the OFF state) recombination in the neutral epi-layer is negligible compared to

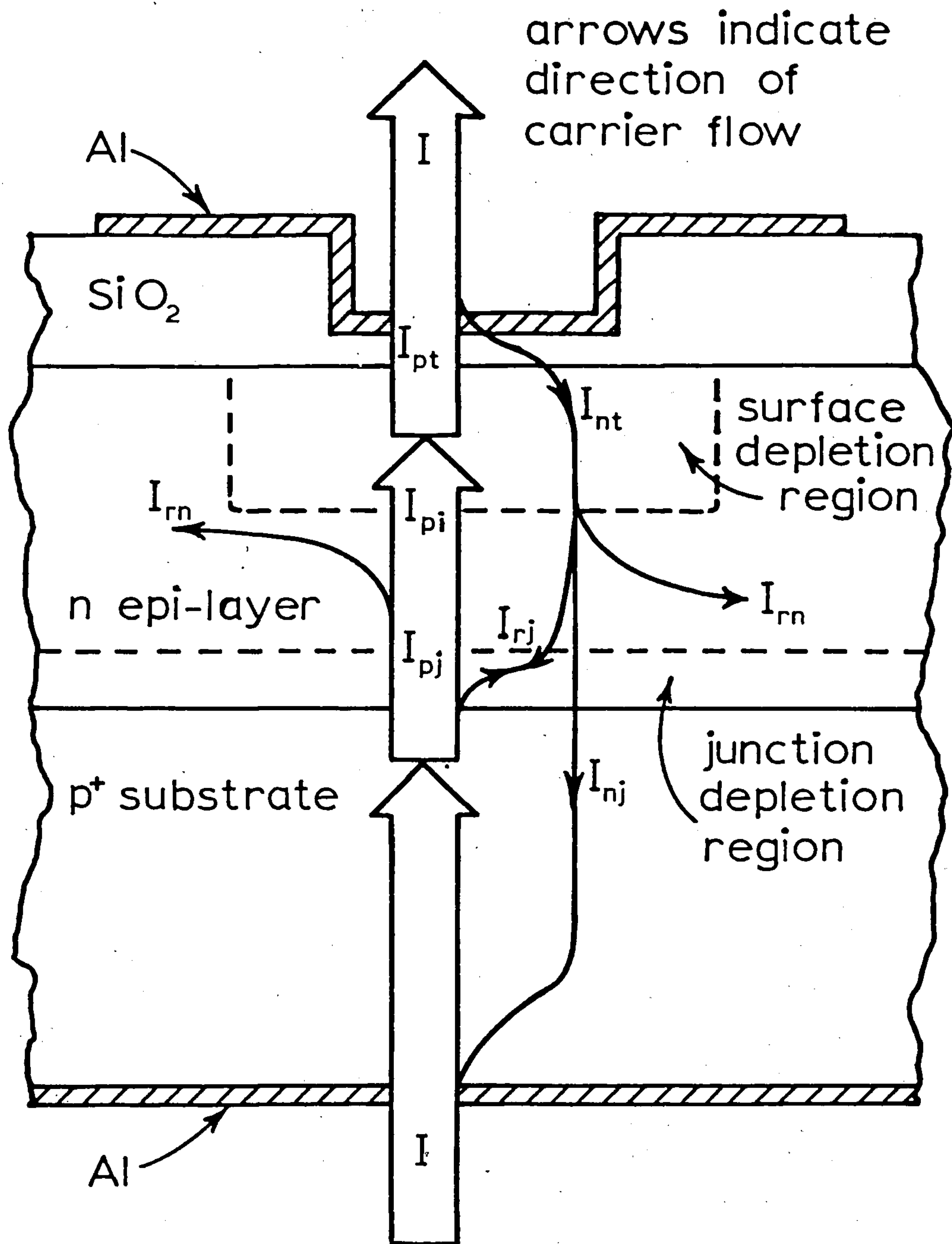

Fig. 5.2 The current components present in the MISS device close to switching.

junction recombination (this is not necessarily true when the device is in the ON state (see Chapter 4). As a consequence of using n epi-layer on p^+ substrates, a degradation of recombination lifetime within the junction region will occur as a result of lattice mismatch between the heavily doped p^+ substrate and lightly doped n epi-layer. This typically leads to an order of magnitude variation between recombination lifetime close to the junction and in the "bulk" of the epi-layer (5-3), resulting in junction recombination being dominant over recombination in the neutral epi-layer. To get an approximate value for the generation lifetime in the junction, the reverse bias I-V characteristics of the p^+-n junction was measured and the lifetime determined by the relation (5-4),

$$I_{gj} = q\, A_j \frac{n_i}{2\tau_g} W_j \exp \frac{qV_j}{2kT}$$

where I_{gj} is the generation current in p^+-n junction depletion region, and

τ_g is the generation lifetime in the junction,

and W_j is the p^+-n junction depletion width given by eqn (5.20).

The value of τ_g obtained was ~0.1 μs as compared to the typical value of 1 μs normally encountered in "bulk" epitaxial Si. The recombination lifetime, τ_1, was assumed to be equal to τ_g for computational purposes using the model presented later in this chapter.

(iii) For mathematical convenience, a circular geometry is assumed in which tunnel-oxide area and junction area are considered as two concentric circles of areas which are equivalent to the actual areas used in fabrication.

(iv) The junction voltage V_j is assumed constant across the whole area of the isolated region (modifications of this assumption are considered in Appendix E).

The particular geometry used in the following analysis is schematically shown in Fig.5.3. The current-voltage equations for the p^+-n junction are derived using the short-base diode approximation for areas within one diffusion length of the tunnel-oxide (Regions I and II). Elsewhere a long-base diode is assumed.

(i) Region I:

This is the region directly under the tunnel-oxide. For the device in the OFF state, the silicon under the oxide is deep-depleted and hence the depletion region extends into the n epi-layer. Under these conditions, the effective area of the device is increased due to the lateral spread of the depletion region. Thus the effective area A_1 is taken to be $(L + 2X_d)^2$, where L is the side dimension of the tunnel-oxide area and X_d is the surface depletion width. The equivalent radius of this region is defined as $r_o = (L+2X_d)/\sqrt{\pi}$. Since the epi-layer thickness $X_e << L_p$, the diffusion length for holes, a short-base diode approximation is appropriate. Hence the junction hole current contributed by area A_1 is given by

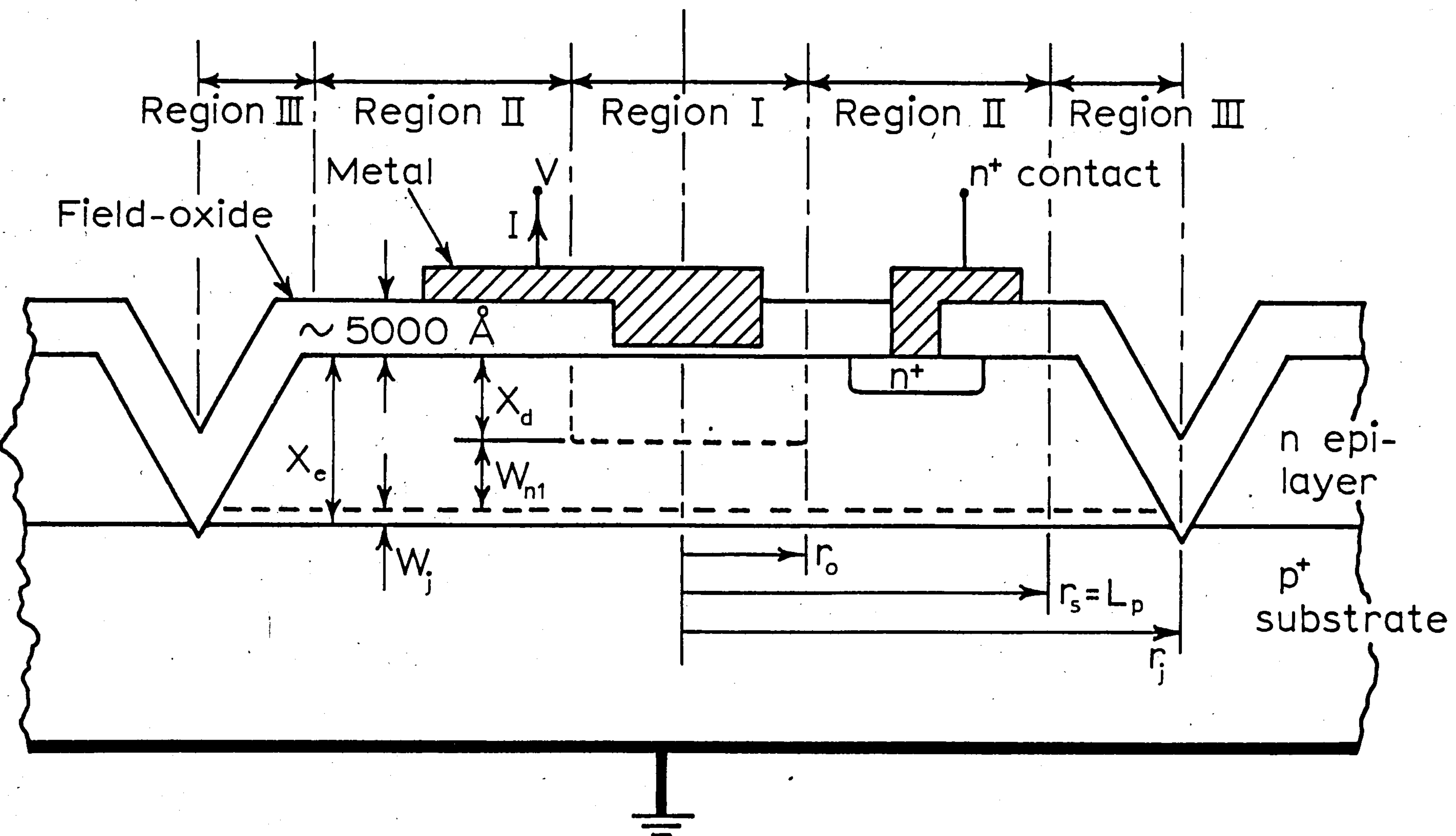

Fig. 5.3 Schematic diagram of the MISS device in cross-section. For the two-dimensional model, regions I and II are treated as short-base diodes and region III as a long-base diode.

$$I_{pj1} = q\, D_p\, p_{no} \frac{A_1}{W_{n1}} (e^{qV_j/kT} - 1) , \tag{5.15}$$

where $A_1 = (L + 2X_d)^2$,

W_{n1} = width of neutral section in Region I,

$= X_e - W_j - X_d$,

where W_j is the p^+-n junction depletion width.

(ii) Region II

This region covers the area in which the distance from the junction to the tunnel-oxide region is within one diffusion length, and extends from radius r_o to r_s, where

$$r_s = \begin{cases} L_p , & \text{if } r_j > L_p , \\ r_j , & \text{if } r_j < L_p , \end{cases} \tag{5.16}$$

where r_j is the equivalent radius of the isolated p^+-n junction (i.e., $r_j = (A_j/\pi)^{1/2}$). Since all of this region is within one diffusion length of the tunnel-oxide area, it can be approximated by a short-base diode, with the added condition that the neutral distance between the tunnel-oxide area and the junction is a function of radius. Hence the junction hole current contributed by Region II is given by

$$I_{pj2} = q\, D_p\, p_{no}(e^{qV_j/kT}-1) \int_{r_o}^{r_s} \frac{dA}{W_n(r)}$$

$$= q\, D_p\, p_{no}(e^{qV_j/kT}-1) \int_{r_o}^{r_s} \frac{2\pi r dr}{[(X_e-W_j)^2+r^2]^{1/2}}$$

$$2\pi q\, D_p\, p_{no}(e^{qV_j/kT}-1)\{L_p-[(X_e-W_j)^2 + (L+2X_d)^2/\pi]^{1/2}\}\ ,\ \text{if } r_j > L_p\ .$$

$$2\pi q\, D_p\, p_{no}(e^{qV_j/kT}-1)\{[A_j/\pi+(X_e-W_j)^2]^{1/2} - [(X_e-W_j)^2 + (L+2X_d)^2/\pi]^{1/2}\}\ ,\ \text{if } r_j < L_p\ . \tag{5.17}$$

(iii) Region III

This region exists only for very large isolated junction areas, in which the distance between tunnel-oxide and the junction edge is greater than one diffusion length; i.e., $r_j > L_p$. Within this area a long-base diode is assumed, and consequently I_{pj3} represents the hole recombination current within the neutral epi-layer which is expected to be significant for very large junction area devices. Hence the junction hole current contributed by Region III is given by

$$I_{pj3} = (q\ D_p\ p_{no}/L_p)(e^{qV_j/kT}-1)[A_j-\pi L_p^2]; \quad r_j > L_p. \tag{5.18}$$

This current domponent does not contribute to the hole current which reaches the $Si\text{-}SiO_2$ interface.

Unlike the hole injection current discussed above, junction recombination current is uniform over the whole area of the isolated junction and is given by (5-4),

$$I_{rj} = (q\ n_i\ A_j\ W_j/2\tau_1)(e^{qV_j/2kT}-1)\ , \tag{5.19}$$

where τ_1 is the recombination lifetime within the junction depletion region, and (assuming a one-sided abrupt junction)

$$W_j = \frac{2\varepsilon_s}{qN_D}(\phi_{Bi}-V_j)\ , \tag{5.20}$$

where ϕ_{Bi} is the built-in barrier potential of the p^+-n diode, calculated from

$$\phi_{Bi} = (2kT/q)\ell n(N_d/n_i)\ . \tag{5.21}$$

The total junction current is hence given by (see Fig. 5.3),

$$\begin{aligned} I &= I_{pj} + I_{nj} + I_{rj} \\ &= I_{pj} + I_{rj}\ , \text{ since } N_a \gg N_d \\ &= (I_{pj1} + I_{pj2} + I_{pj3}) + I_{rj}\ , \end{aligned} \tag{5.22}$$

and the total hole current reaching the $Si\text{-}SiO_2$ interface is

$$I_{pi} = I_{pj1} + I_{pj2}\ . \tag{5.23}$$

From the previously derived equations for I_{pj1} and I_{pj2} (eqns (5.15) and (5.17)), the total hole current reaching the $Si-SiO_2$ interface is a function of X_d and V_j. In the following sections, the effect of p^+-n junction area on X_d and V_j in relation to the switching and holding points will be considered.

5.4 RESULTS AND DISCUSSION

5.4.1 The Switching Point

From the detailed discussion presented in Section 4.1 it was concluded that the switching mechanism from OFF to ON state is completely determined by the properties of the MIS diode. For a given d_{ox} and A_{ox}, the experimentally measured switching current I_s is constant regardless of isolated p^+-n junction area (see Chapter 4). From this result, three important conditions were concluded at the switching point for a given tunnel-oxide thickness and area:

(i) the hole current reaching the $Si-SiO_2$ interface, I_{pi}, is essentially constant.

(ii) the hole concentration at the $Si-SiO_2$ interface, p(0), is essentially constant.

(iii) the metal Fermi level, E_{Fm}, approaches the conduction band edge at the $Si-SiO_2$ interface, $E_c(0)$.

The above conditions suggest that for a given d_{ox} and A_{ox}, the electron tunnel current from metal to silicon conduction band is of the same order independent of the surface potential at switching. Since recombination current in the neutral epi-layer

is negligible compared to junction recombination current (see Section 5.3), and electron diffusion current can be ignored (since $N_a >> N_d$), current continuity requires

$$I_{nt} \simeq I_{rj} \ . \quad (5.24)$$

This leads us to the conclusion that, at the switching point, devices with a different p^+-n junction area will have comparable junction recombination current. From eqn (5.19), this suggests a logarithmic relationship between junction area and junction voltages of the form

$$V_{j1} = V_{j2} + nV_T \ln(A_{j2}/A_{j1}) \ , \quad (5.25)$$

where we define $V_T = kT/q$ and n is a parameter used to generate the calculated curves in Fig. 5.4.

5.4.1.1 Comparison between calculated and experimental results. Table 5.1 shows the switching voltage for each tunnel-oxide thickness for various p^+-n junction areas. The tunnel-oxide growth times were 6 min, 8 min, and 12 min at 700°C in dry oxygen.

In order to verify the validity of our simplified model, an expression for the depletion width at switching must be formulated. The voltage equation for the MISS is given by

$$V = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_i}{C_{ox}} + \psi_s + V_j . \quad (5.26)$$

For a given d_{ox}, Q_i is approximately constant at $V=V_s$ (see Section 5.2), hence the switching voltage is given by

$$V_s \simeq \psi_s + K \ , \quad (5.27)$$

Table 5.1

Junction Area (μm^2) →	80x80 (set A)	100x100 (set B)	140x140 (set C)	220x220 (set D)	
Oxidn. Time (min at 700 °C) ↓	Switching Voltage				Switching Current ↓
6 (set X3)	3·25 V	3·8 V	4·4 V	4·85 V	3·6 μA
8 (set X4)	3·8 V	4·5 V	5·3 V	5·6 V	1·6 μA
12 (set X5)	3·4 V	4·3 V	5·2 V	5·8 V	1·1 μA

Experimental switching voltage and switching current for each set of devices for the various isolated junction areas used in this study. The basic device parameters were A_{ox} = 20x20 μm^2, X_e = 4.4 μm, $N_d = 4.2 \times 10^{14}$ cm^{-3} and $N_a \simeq 2 \times 10^{19}$ cm^{-3}.

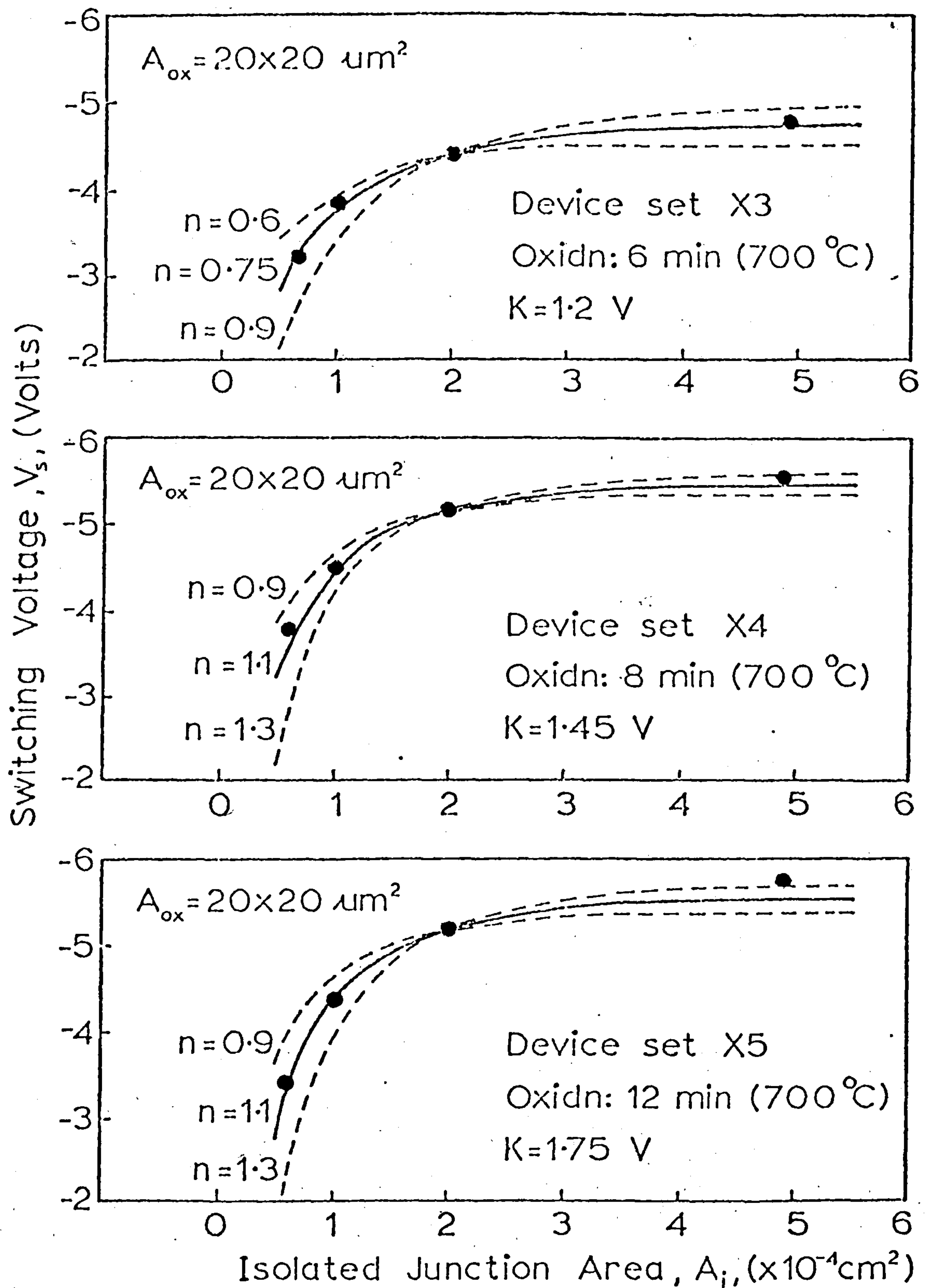

Fig. 5.4 Comparison between experimental (full circles) and calculated curves of switching voltages as a function of isolated junction area. The calculated curves have n as a parameter, which determines the logarithmic variation of V_1 with area (see eqn (5.25)). The best fit to experimental data is shown by the full lines.

where K is a constant for a particular d_{ox} and is typically of the order of 1 to 2 volts. For increasing d_{ox}, K will increase due to a decrease in C_{ox} and an increase in Q_i at switching (see Section 5.2). A reasonable estimate for K can be obtained from the ON characteristics, since in this case ψ_s does not change and is, in fact, the value for strong inversion (5-4). Using the depletion approximation, the value for X_d at switching is hence given by

$$X_d = \frac{2\varepsilon_s}{qN_d} |V_s - K| \quad ; \quad V=V_s \qquad (5.28)$$

and the particular values of K used are shown in Fig. 5.4.

The experimental and calculated values of V_s as a function of isolated junction area are shown in Fig. 5.4. The only parameter that is varied in the calculated curves is the value of n in eqn (5.25), which determines the logarithmic variation of V_j with A_j. Essentially, the calculated curves were obtained by matching the V_s for the large junction area devices and hence determining X_d from eqn (5.28). This is then used in eqns (5.15) and (5.17)-(5.19), from which V_j at switching is determined by iterating until the total current equals the experimentally measured switching current. This particular value of V_j for the large area device is then used in eqns (5.15) and (5.25) to determine the X_d required for any other particular area device to achieve the same switching current. Finally, V_s as a function of A_j can then be calculated via eqn (5.28). The particular physical and experi-

mental parameters used in the calculations are listed in Appendix D. As can be seen in Fig. 5.4, the calculated functional relationship between V_s and A_j is in good agreement with experimental results.

5.4.2 The Holding Point

At the holding point, all devices have the same surface potential, which is simply that for strong inversion (5-5). As discussed in Section 5.1, for a given d_{ox} and A_{ox}, a constant hole current reaching the interface, I_{pi}, is required to keep the device in the ON state (see Chapter 4). In addition, as oxide thickness increases, a lower value of I_{pi} is required to keep the device ON.

The experimental and calculated results are shown in Fig. 5.5, for holding current as a function of junction area. The calculated curves were generated by using I_{pi} as a parameter and hence calculating V_j at the holding point via eqn (5.23), and eqns (5.15) and (5.17). This particular value of V_j is then used in the expression for the total current (eqn 5.22)) to calculate the holding current. The physical and experimental parameters used in calculations are given in Appendix D.

As can be seen from Fig. 5.5, the calculated I_H as a function of junction area is in good agreement with experimental data for all device oxide thicknesses and junction areas except for the largest junction area. In this case, the simple model that has been used predicts a larger I_H than measured experimentally. This

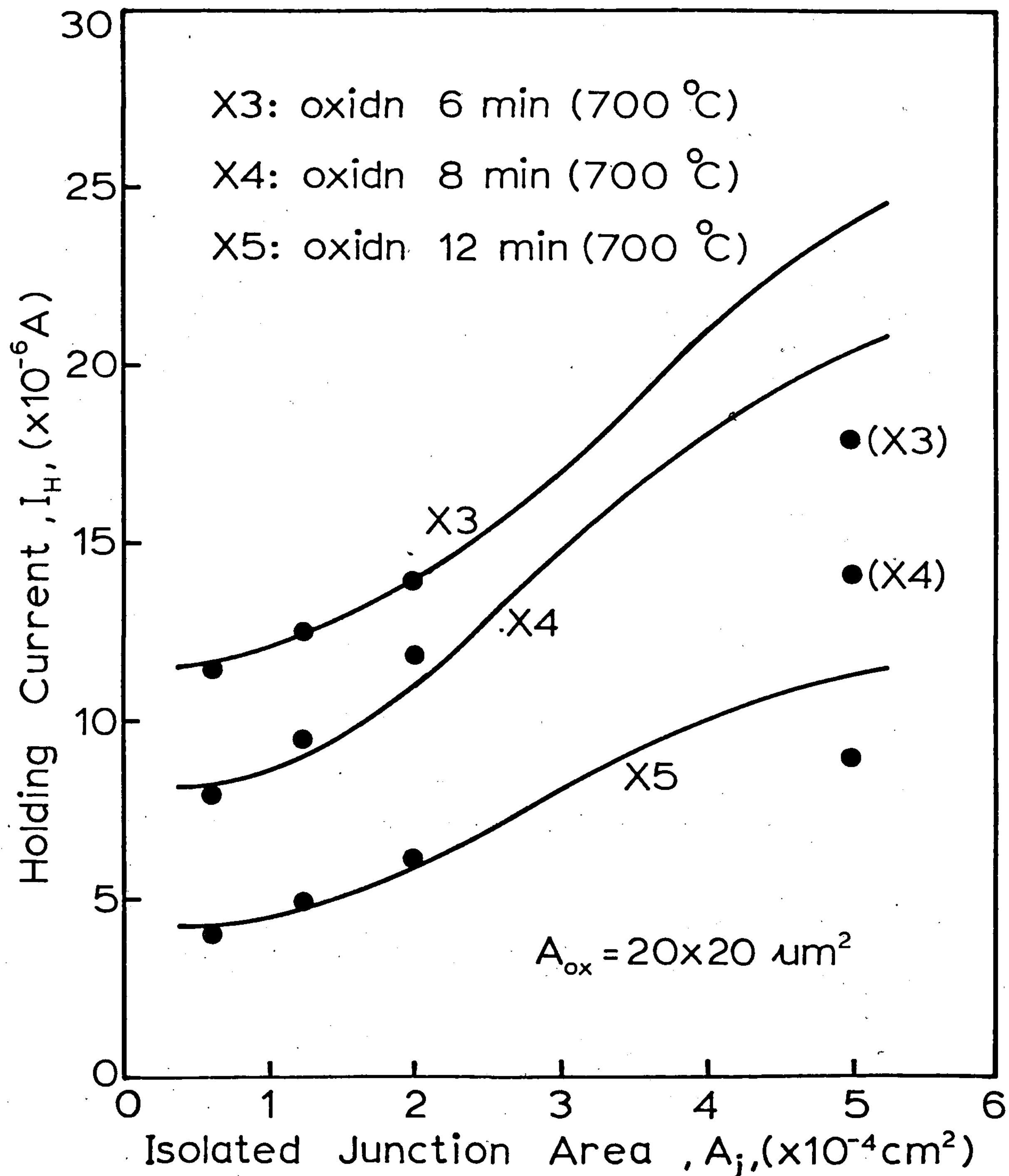

Fig. 5.5 Comparison between experimental (full circles) and calculated curves of holding current as a function of isolated junction area.

discrepancy arises because of the assumption of constant junction voltage over the whole isolated junction area. This does not affect the calculated results for the switching point (see Section 5.4.1) since the hole current immediately under the tunnel-oxide (I_{pj1}, eqn (5.15)) completely dominates all other components due to the small value of W_{n1}. However, in the ON state, X_d is small and equal to the strong inversion value. Under these conditions, the other current components become significant. A simple derivation of V_j variation with distance from the tunnel-oxide is presented in Appendix E for an idealized case.

Since V_j is expected to change significantly only for large distances from the tunnel-oxide, its effect need only be considered within Region III. As a first approximation, V_j is made to decrease linearly with distance (see Appendix E), and the calculated results for devices with 8 min tunnel-oxides are presented in Fig. E.2. The curves in this diagram suggest better agreement with the experimental results than those depicted in Fig. 5.5. Although the linear variation of junction voltage with distance is a gross over-simplification (see Fig. E.1), the curves shown in Fig. E.2 illustrate the fact that a constant V_j cannot be assumed for very large isolation areas. However, for practical device structures ($A_{ox} \simeq p^+$-n junction area) this effect is not expected to be significant.

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CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

The isolated Metal-Insulator-Semiconductor-Switch (MISS) has been studied in detail. The p^{+}-n junction area was limited using V-groove isolation. It was observed that restricting the junction area caused the I-V characteristics of the MISS to change substantially. The experimentally observed D.C. behaviour of the MISS and qualitative arguments explaining the I-V characteristics were presented in Chapter 4. It was also seen that with increasing A_j, for the same tunnel-oxide thickness and area,

(i) the switching current, I_s, remained essentially constant, an observation which helped determine the switching criterion.

(ii) The holding current, I_H, increased, and

(iii) The switching voltage, V_s, also increased.

Furthermore, devices with various tunnel-oxide thicknesses were fabricated and their D.C. I-V characteristics studied. It was observed (see Chapter 4 for details) that with increasing tunnel-oxide thickness, d_{ox},

(i) the switching current I_s, decreased,

(ii) the holding current, I_H, decreased, and

(iii) both device currents in general, I_{off} and I_{on}, decreased.

The holding voltage, V_H, however, increased slightly because of the higher voltage that is dropped across a thicker oxide. A two-dimensional model has been derived which adequately explains the variation of I_s and I_H with changes in junction area, A_j.

In Chapter 2 it was explained that decreasing the A_{ox}/A_j ratio would weaken the regenerative feedback mechanism to the extent that the MISS would not exhibit any switching behaviour. This makes it difficult to go down to tunnel-oxide dimensions of the order of 1 μm and still fabricate satisfactory switching devices. A high packing density is, however, necessary if the MISS is to be commercially employed in memory applications. Isolating the p^+-n junction overcomes this problem and has other important advantages which are listed below.

(i) Junction isolation helps reduce the junction area, A_j, and hence allows us to go down to smaller values of tunnel-oxide area A_{ox} and still maintain an A_{ox}/A_j ratio large enough to allow switching.

(ii) Reducing A_j strengthens the RFM and hence the device needs a smaller electron tunnel current, I_{nt}, to trigger switching. This implies that devices with thicker tunnel-oxides would exhibit satisfactory switching characteristics. Employing a thicker tunnel-oxide is extremely desirable because of its two-fold advantage.

a) A larger, d_{ox}, lowers the device currents and thus reduces the power consumption in the device. A low power dissipation is essential for successful fabrication of LSI memories using the MISS.

b) As the thickness of the tunnel-oxide is increased, a higher reproducibility can be achieved in its fabrication.

The isolation technique employed for our study was V-grooving. This obviously is not a very feasible method for commercial applications as the V-groove itself consumes a large silicon surface area. We propose a more acceptable way of limiting the junction area and making the device essentially one-dimensional. The envisaged device structure is shown in Fig. 6.1.

A field oxide is either thermally gown or chemically deposited on a p^+-substrate. A window is then etched through the field oxide equal to the desired tunnel-oxide area and an n epitaxial silicon layer grown over the p^+-substrate. Hence the field oxide helps isolate the n-epitaxial layer and therefore can also appropriately be called an isolation oxide. The inversion voltage of this oxide should be well known in order to assure the switching voltage of the MISS will be compatible with the needs of the circuit design. However, minimizing the area of the electrode overlap reduces the influence of the isolation oxide, as well as the parasitic capacitances. Furthermore, growing the epitaxial layer after the deposition of the field/isolation

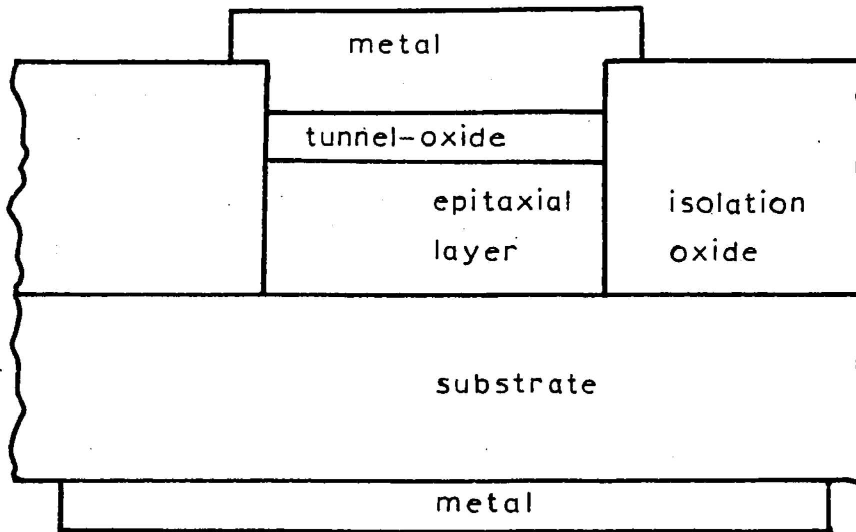

Fig. 6.1 Proposed structure for the isolated MISS device.

oxide and employment of low-temperature processes thereafter will eliminate problems caused by the up-diffusion of p^+-substrate into the n-epilayer, improving the reproducibility of device behaviour.

The MISS may be even further enhanced by using the complement structure to the one studied in this thesis, the p/n^+ epitaxial-substrate combination, which will inherently possess all of the advantages characteristic of electron minority carriers, (i.e. higher mobilities, longer diffusion lengths, etc.). However, the major disadvantage of a MISS built on p-on-n^+ silicon is that the area under the field oxide surrounding the device is normally inverted, which will cause much larger OFF state currents to flow through the device. This problem, however, may be overcome by using technology employed for fabrication of ENHANCEMENT-MODE n-channel MOSFETs. Also, other semi-insulators such as silicon nitride and polycrystalline silicon may also exhibit advantages over and above that of silicon dioxide MISS devices and the tunnel-oxide technology. Alternative isolation methods such as ion-bombardment to define current flow in desired directions may also play an important part in the evolution of the MISS as a viable device.

In conclusion, this thesis establishes beyond doubt the need for the fabrication of one-dimensional MISS devices to achieve lower power dissipation and higher reliability if the MISS is to be viewed as a superior alternative to present-day memory circuit elements.

APPENDIX A

PRE-FURNACE CLEANING PROCEDURE

Note: (i) Throughout all processing, silicon wafers were supported in Teflon wafer carriers.

(ii) All processes that involve boiling on the hot plate were carried out in pyrex or quartz containers.

(iii) All processes that involve HF acid were carried out in Teflon or polypropylene containers.

(iv) DI water used was > 10 Megohm-cm resistivity, and for final rinses > 14 Megohm-cm.

(v) All chemicals used (except for initial organic solvent boils) were "Electronic" grade.

(vi) All DI water rinses were repeated 6 times, and for final rinses at least 8 times.

(vii) Before trichloroethylene boils, care was taken to ensure that silicon wafers, wafer carrier and container were dry.

I. Organic Solvent Boils (hot plate set at 500)

1. boil in trichloroethylene (5-10 mins.)
2. boil in acetone (5-10 mins.)
3. Boil in methanol (5-10 mins.)

II. HF Etch

1. Dip in 10% HF to remove any oxide. (Note: 10 secs. is usually sufficient; however, care must be taken not to

over-etch when oxide patterns are present on the wafer. The etching process can be monitored from the back of the wafers and is complete when the surface becomes hydrophobic).

(2) Rinse in DI (X6)

III. Organic Clean (hot plate set at 500)

(1) Boil in 4:1:1 solution of Di:NH_4OH:H_2O_2 (10-15 mins).

(2) Rinse in DI (X6).

IV. Ionic Clean (hot plate set at 500)

(1) Boil in 4:1:1 solution of DI:HCl:H_2O_2 (10-15 mins.)

(2) Rinse in DI (X6).

V. HF Etch

(1) Dip in 10% HF for 10 secs. to remove any oxide grown during organic and ionic cleans. (Note: See previous comments on HF etch.)

(2) Rinse in DI (X8).

(3) Blow dry in N_2 gas as soon as possible after the final DI rinse.

APPENDIX B

SHIPLEY PHOTORESIST (PR) PROCEDURE

Note: (i) Shipley PR was applied to the wafers as soon as possible after oxidation or metallization.

(ii) For etching of oxides, buffered HF etch was kept in polypropylene or Teflon container and wafers were supported in Teflon carriers.

I. PR Application

(1) Place wafer front-face-up on PR spinner, switch on vacuum and apply several drops of Shipley PR (AZ 1350J) evenly over the whole wafer.

(2) Spin at 4000 rpm for 20 secs.

(3) Place front-face-up onto filter paper and pre-bake at 80-85°C for 20 mins.

II. PR Exposure and Development

(1) Align wafer under appropriate mask and expose under UV lamp for 30 secs. (Note: UV lamp should be allowed to warm up for at least 10 mins before using.)

(2) Place wafers in Teflon wafer carrier and develop for 45 secs. in Shipley developer (1:5 mixture of AZ 351 and DI water) under conditions of continual stirring.

(3) Rinse in DI (X4).

(4) Rinse each wafer individually under DI water tap and blow dry in N_2 gas.

(5) Place wafers front-face-up onto filter paper and post-bake at 100-105°C for 20 mins.

APPENDIX C

CLEANING PROCEDURE FOR ALUMINIUM

The Aluminium to be used for evaporation was cut into sticks of length (∿3 cms.) and cleaned by the following procedure before being loaded into the vacuum system.

I. ORGANIC SOLVENT BOILS

(i) Boil in trichloroethylene (5–10 mins).

(ii) Boil in acetone (5–10 mins).

(iii) Boil in methanol (5–10 mins).

(iv) Rinse in DI water (X10).

II. IONIC CLEAN

Note: This cleaning procedure is used to remove native Al_2O_3 from the surface and also etch a very thin layer of aluminium from the surface so that a clean fresh aluminium surface is obtained.

(i) Place the aluminium sticks in a very dilute solution of $HCl:H_2O_2$:DI water for about 2 minutes.

(ii) Rinse in DI water (X10).

(iii) Blow dry in N_2.

APPENDIX D

PHYSICAL AND EXPERIMENTAL PARAMETERS USED IN CALCULATIONS

N_d = 4.2×10^{14}, cm^{-3}

n_i = 1.45×10^{10}, cm^{-3}

D_p = $15.5\ cm^2\ sec^{-1}$

τ_o = $3\ \mu sec$

τ_1 = $0.1\ \mu sec$ (measured from reverse bias junction characteristics)

X_e = $4.4\ \mu m$

L = $20\ \mu m$

ε_s = $1.036 \times 10^{-12} F\ cm^{-1}$

KT/q = $V_T = 0.0259\ V$

APPENDIX E

JUNCTION VOLTAGE AS A FUNCTION OF RADIUS

Referring to Fig. 5.4, for the region far from the centre of the device ($r>r_s$), the carrier flow will be essentially horizontal. The incremental current dI flowing out from the area $2\pi r\, dr$ (see inset of Fig. E-1), is given by

$$dI = J_o\, e^{V_j(r)/V_T}\, 2\pi r\, dr \,, \qquad \text{(E-1)}$$

where $J_o = q\, D_p\, p_{no}/L_p$. By integrating over the region from r_s to r, the current at radius r is given by

$$I(r) = \int_{r_s}^{r} dI = \int_{r_s}^{r} 2\pi r\, J_o\, e^{V_m(r)/V_T}\, dr \,. \qquad \text{(E-2)}$$

The voltage increment due to current I(r) is

$$dV_j = I(r)dR = I(r)\,\frac{\rho\, dr}{2\pi r\, X_e} \,, \qquad \text{(E-3)}$$

where ρ is the resistivity of the material and X_e is the epilayer thickness. From eqns (E-2) and (E-3):

$$\frac{dV_j}{dr} = \frac{I(r)\rho}{2\pi r\, X_e} = \frac{\rho}{X_e}\,\frac{1}{r}\int_{r_s}^{r} J_o\, e^{V_j(r)/V_T}\, r\, dr. \qquad \text{(E-4)}$$

Differentiating eqn (E-4):

$$\frac{d^2V_j}{dr^2} + \frac{1}{r}\,\frac{dV_j}{dr} = \frac{\rho}{X_e}\, J_o\, e^{V_j(r)/V_T} \,. \qquad \text{(E-5)}$$

Equation (E-5) can be solved numerically and a typical set of

computed results is shown in Fig. E-1 for different boundary conditions.

For the situation we are considering, the boundary conditions are not known, thus a simple approximation is used; for the region $r \leq r_s$ the junction voltage is assumed constant, and for $r > r_s$ the junction voltage is assumed linearly decreasing with radius. Hence we can express $V_j(r)$ as

$$V_j(r) = V_{jo} - V_{jo}(r-r_s)M \ ; \qquad r > r_s \ , \tag{E-6}$$

where M is the slope of $V_j(r)$ and V_{jo} is the junction voltage within the region $r \leq r_s$. The expressions for I_{pj1}, I_{pj2} and I_{rj} do not change and are given by eqns (5.15), (5.17), and (5.19), respectively; however, the expression for I_{pj3} needs to be modified. Using eqn (E-6), we have

$$I_{pj3} = (q\ D_p\ p_{no}/L_p) \int_{r_s}^{r_j} 2\pi r \ \exp\left[V_{jo}(1-M(r-r_s))/V_T\right] dr$$

$$= (2\pi\ q\ D_p\ p_{no}/L_p)\ \exp\left[V_{jo}(1+Mr_s)/V_T\right] \int_{r_s}^{r_j} r\exp(-V_{jo}Mr/V_T)dr$$

$$= \left(\frac{2\pi q\ D_p\ p_{no}}{L_p}\right) \exp(V_{jo}(1+Mr_s)/V_T) \left[\frac{-V_T}{V_{jo}M} \left[r_j \ \exp\left(\frac{-V_{jo}M}{V_T}\ r_j\right)\right.\right.$$

$$\left.\left. - r_s\left(\exp\frac{-V_{jo}M}{V_T}\ r_j\right) - \left(\frac{V_T}{V_{jo}M}\right)^2 \left[\exp\left(\frac{-V_{jo}M}{V_T}\ r_j\right) - \exp\left(\frac{-V_{jo}M}{V_T}\ r_s\right)\right]\right]\right] \tag{E-7}$$

Using the above expression for I_{pj3}, the dotted curves in Fig. E-2 were calculated for various values of M.

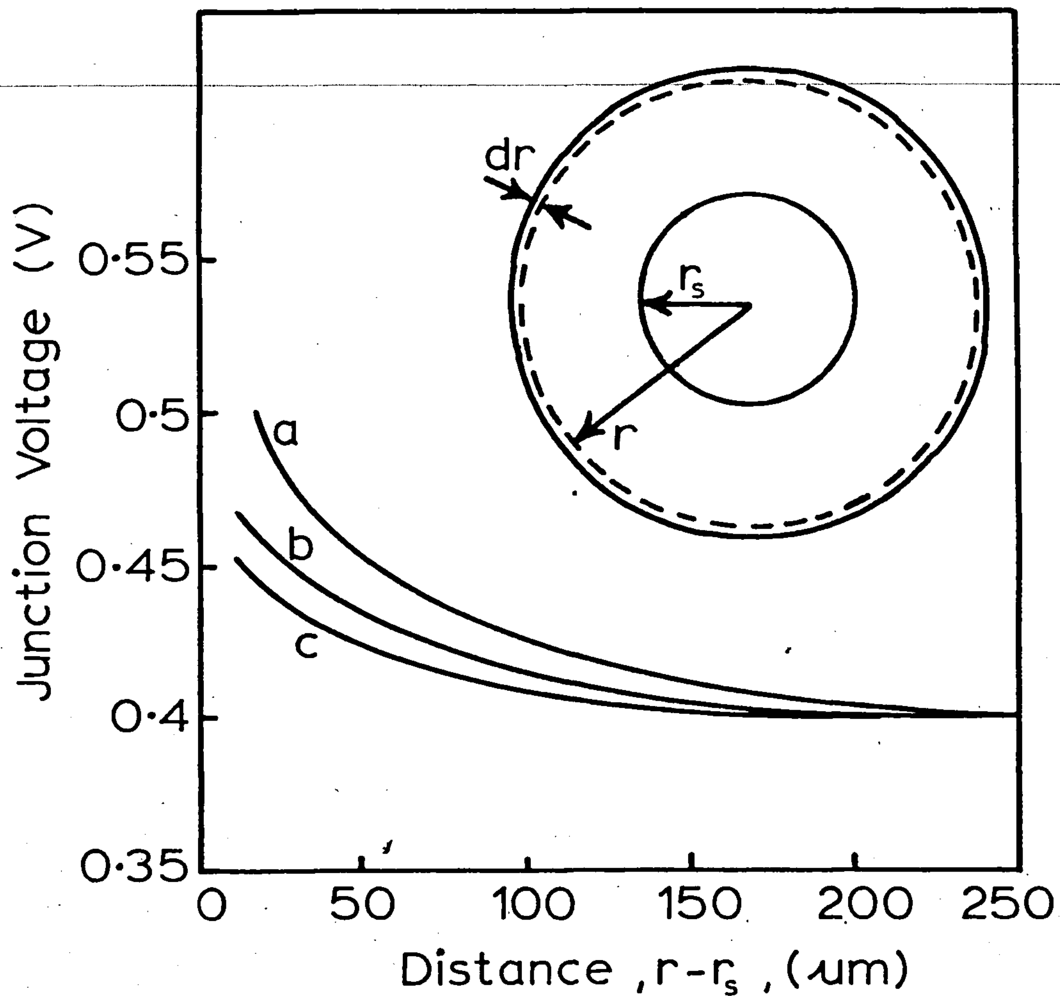

Fig. E-1 Junction voltage variation as a function of distance for the circular geometry shown in the inset. These curves were calculated by numerically integrating eqn (B-5) with the following boundary conditions at $r = 250$ µm:

curve (a): $V_j = 0.4$ V, $\frac{dV_j}{dr} = -1.0$ V/cm,

curve (b): $V_j = 0.4$ V, $\frac{dV_j}{dr} = -0.5$ V/cm,

curve (c): $V_j = 0.4$ V, $\frac{dV_j}{dr} = -0.3$ V/cm.

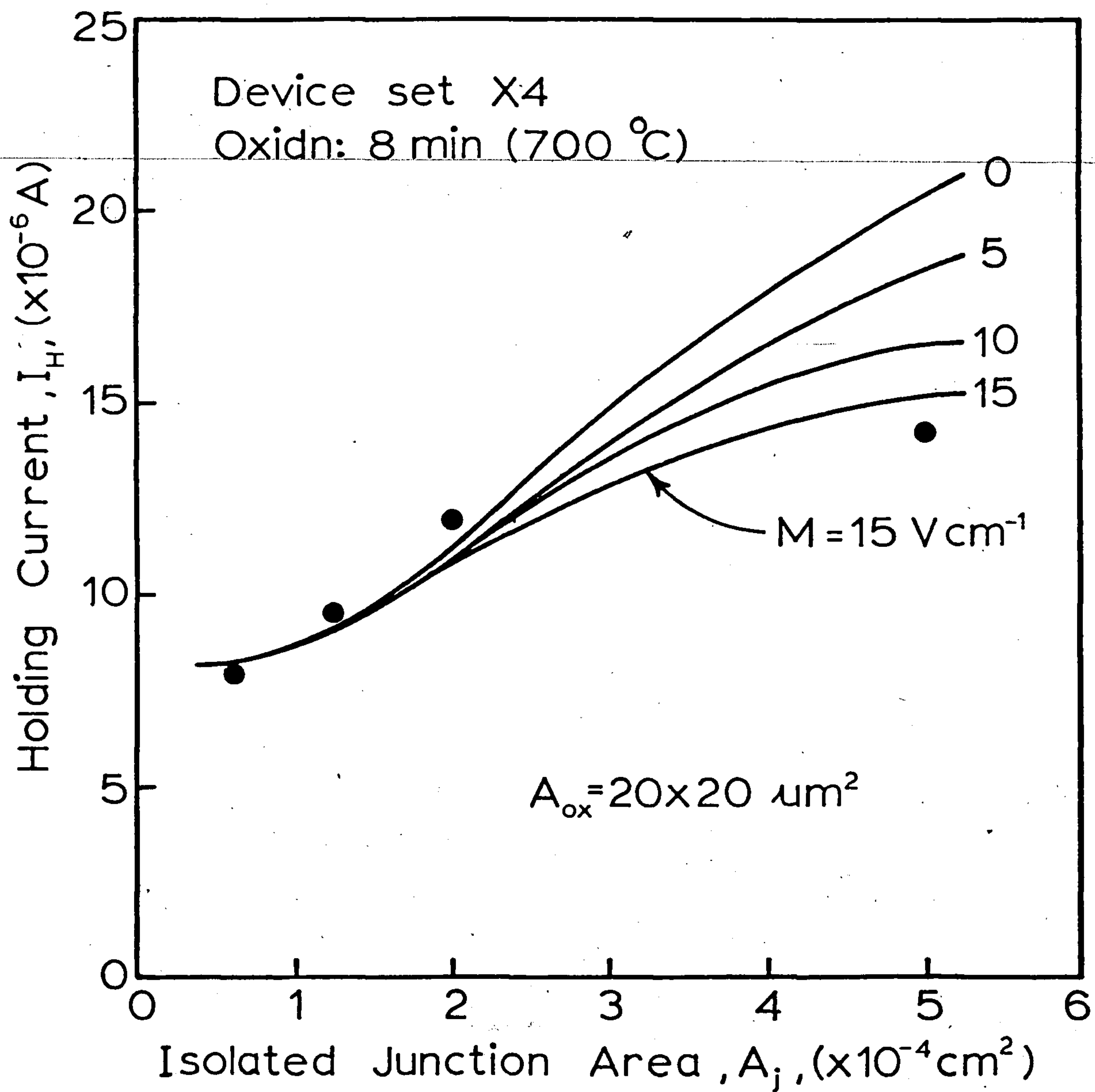

Fig. E-2 Comparison between experimental (full circles) and calculated curves of holding current as a function of isolated junction area with M as a parameter.

VITA

Umesh Mishra was born in Pune, India, on September 25, 1958, to S. Mishra and S. Devi. He obtained a Bachelor of Technology degree in Electrical Engineering from the Indian Institute of Technology, Kanpur, India, in May 1979. He has been registered in the M.S. program offered by the Department of Electrical Engineering, Lehigh University, Bethlehem, PA, since September 1979.